19-4794; Rev 0; 11/98

EVALUATION KIT AVAILABLE

+5V Single-Supply, 1Msps, 14-Bit Self-Calibrating ADC

General Description

The MAX1205 is a 14-bit, monolithic, analog-to-digital converter (ADC) capable of conversion rates up to 1Msps. This integrated circuit, built on a CMOS process, uses a fully differential, pipelined architecture with digital error correction and a short self-calibration procedure that corrects for capacitor and gain mismatches and ensures 14-bit linearity at full sample rates. An on-chip track/hold (T/H) maintains superb dynamic performance up to the Nyquist frequency. The MAX1205 operates from a single +5V supply.

The fully differential inputs allow an input swing of $\pm V_{REF}$. The reference is also differential, with the positive reference (RFPF) typically connected to +4.096V and the negative reference (RFNF) connected to analog ground. Additional sensing pins (RFPS, RFNS) are provided to compensate for any resistive-divider action that may occur due to finite internal and external resistances in the reference traces and the on-chip resistance of the reference pins. A single-ended input is also possible using two operational amplifiers.

The power dissipation is typically 257mW at +5V, at a sampling rate of 1Msps. The device employs a CMOS-compatible, 14-bit parallel, two's complement output data format. For higher sampling rates, the MAX1201 is a 2.2Msps pin-compatible upgrade to the MAX1205.

The MAX1205 is available in an MQFP package, and operates over the commercial (0°C to +70°C) and the extended (-40°C to +85°C) temperature ranges.

Applications

Imaging

Communications

Medical

Scanners

Data Acquisition

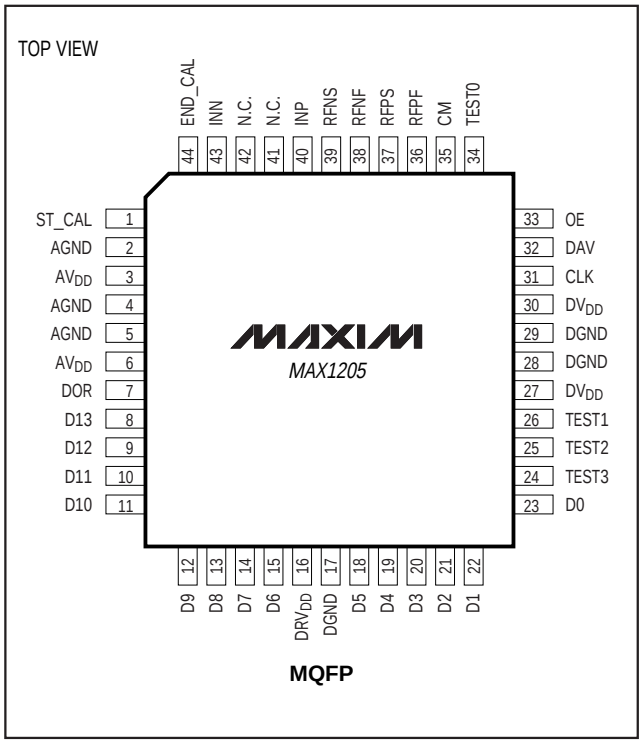
Features

- **Monolithic, 14-Bit, 1Msps ADC**
- **+5V Single Supply**
- **SNR of 80dB for f_{IN} = 500kHz**
- **SFDR of 87dB for f_{IN} = 500kHz**
- **Low Power Dissipation: 257mW**
- **On-Demand Self-Calibration**
- **Differential Nonlinearity Error: ±0.3LSB**
- **Integral Nonlinearity Error: ±1.2LSB**
- **Three-State, Two's Complement Output Data**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1205CMH	0°C to +70°C	44 MQFP
MAX1205EMH	-40°C to +85°C	44 MQFP

Pin Configuration



+5V Single-Supply, 1Msps, 14-Bit Self-Calibrating ADC

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND, DGND .....+7V
DV_{DD} to DGND, AGND .....+7V
DRV_{DD} to DGND, AGND .....+7V
INP, INN, RFPF, RFPS, RFNF, RFNS, CLK, CM .....(AGND - 0.3V) to (AV_{DD} + 0.3V)
Digital Inputs to DGND .....-0.3V to (DV_{DD} + 0.3V)
Digital Output (DAV) to DGND .....-0.3V to (DRV_{DD} + 0.3V)
Other Digital Outputs to DGND .....-0.3V to (DRV_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
44-Pin MQFP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges (T_A)
MAX1205CMH .....0°C to +70°C
MAX1205EMH .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = +5V ±5%, DV_{DD} = DRV_{DD} = +3.3V, V_{RFPS} = +4.096V, V_{RFNS} = AGND, V_{CM} = +2.048V, V_{IN} = -0.5dBFS, f_{CLK}= 2.048MHz, digital output load ≤ 20pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT						
Input Voltage Range (Notes 2, 3)	V_{IN}	Single-ended		4.096	4.5	V
		Differential		±4.096	±4.5	
Input Resistance (Note 4)	R_I			55		kΩ
Input Capacitance (Note 3)	C_I	Per side in track mode		21		pF
REFERENCE/EXTERNAL						
Reference Voltage (Note 3)	V_{REF}			4.096	4.5	V
Reference Input Resistance			700	1000		Ω
TRANSFER CHARACTERISTICS						
Resolution (no missing codes) (Note 5)	RES	After calibration, guaranteed	14			Bits
Integral Nonlinearity	INL			±1.2		LSB
Differential Nonlinearity	DNL		-1	±0.3	+1	LSB
Offset Error			-0.2	±0.003	+0.2	%FSR
Gain Error			-5	-3.0	+5	%FSR
Input-Referred Noise				75		μV_{RMS}
DYNAMIC SPECIFICATIONS (Note 6)						
Maximum Sampling Rate	f_{SAMPLE}	$f_{SAMPLE} = f_{CLK} / 2$	1.024			Msps
Conversion Time (Pipeline Delay/Latency)				4		f_{SAMPLE} Cycles
Acquisition Time	t_{ACQ}	To full-scale step (0.006%)		100		ns
Overvoltage Recovery Time	t_{OVR}			410		ns
Aperture Delay	t_{AD}			3		ns
Full-Power Bandwidth				3.3		MHz
Small-Signal Bandwidth				78		MHz

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = +5V ±5%, DV_{DD} = DRV_{DD} = +3.3V, V_{RFPS} = +4.096V, V_{RFNS} = AGND, V_{CM} = +2.048V, V_{IN} = -0.5dBFS, f_{CLK}= 2.048MHz, digital output load ≤ 20pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Signal-to-Noise Ratio (Note 5)	SNR	f_{IN} = 99.5kHz	78	83		dB
		f_{IN} = 300.5kHz		81.5		
		f_{IN} = 504.5kHz		80		
Spurious-Free Dynamic Range (Note 5)	SFDR	f_{IN} = 99.5kHz	84	91		dB
		f_{IN} = 300.5kHz		88		
		f_{IN} = 504.5kHz		87		
Total Harmonic Distortion (Note 5)	THD	f_{IN} = 99.5kHz		-86	-80	dB
		f_{IN} = 300.5kHz		-85		
		f_{IN} = 504.5kHz		-84		
Signal-to-Noise Ratio plus Distortion (Note 5)	SINAD	f_{IN} = 99.5kHz	77	82		dB
		f_{IN} = 300.5kHz		79		
		f_{IN} = 504.5kHz		78		
POWER REQUIREMENTS						
Analog Supply Voltage	AV_{DD}		4.75	5	5.25	V
Analog Supply Current	$I(AV_{DD})$			51	70	mA
Digital Supply Voltage	DV_{DD}		3		5.25	V
Digital Supply Current	$I(DV_{DD})$			0.4	1.2	mA
Output Drive Supply Voltage	DRV_{DD}		3		DV_{DD}	V
Output Drive Supply Current	$I(DRV_{DD})$	10pF loads on D0–D13 and DAV		0.1	0.6	mA
Power Dissipation	PDSS			257	377	mW
Warm-Up Time				0.1		sec
Power-Supply Rejection Ratio	PSRR	Offset	55			dB
		Gain	55			

+5V Single-Supply, 1Msps, 14-Bit Self-Calibrating ADC

TIMING CHARACTERISTICS

(AV_{DD} = +5V ±5%, DV_{DD} = DRV_{DD} = +3.3V, f_{CLK} = 2.048MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Time	t_{CONV}			4 / f_{SAMPLE}		ns
Clock Period	t_{CLK}			488		ns
Clock High Time	t_{CH}		187	244	301	ns
Clock Low Time	t_{CL}		187	244	301	ns
Acquisition Time	t_{ACQ}			t_{CLK} / 2		ns
Output Delay	t_{OD}			70	150	ns
DAV Pulse Width	t_{DAV}			1 / f_{CLK}		ns
CLK-to-DAV Rising Edge	t_S			65	145	ns
Data Access Time	t_{AC}	C_L = 20pF		16	75	ns
Bus Relinquish Time	t_{REL}			16	75	ns
Calibration Time	t_{CAL}	ST_CAL = 1, Figure 8		17,400		f_{CLK} cycles

DIGITAL INPUTS AND OUTPUTS

(AV_{DD} = +5V ±5%, DV_{DD} = DRV_{DD} = +3.3V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		DV_{DD} - 0.8			V
Input Capacitance				4		pF
CLK Input Low Voltage	CLK_{VIL}				0.8	V
CLK Input High Voltage	CLK_{VIH}		AV_{DD} - 0.8			V
CLK Input Capacitance	C_{CLK}			9		pF
Digital Input Current	$I_{IN\_}$	$V_{IN\_}$ = 0 or DV_{DD}		±0.1	±10	µA
Clock Input Current	I_{CLK}		-10	±1	+10	µA
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA		70	400	mV
Output High Voltage	V_{OH}	I_{SOURCE} = 200µA	DV_{DD} - 0.4	DV_{DD} - 0.03		V
Three-State Leakage Current	$I_{LEAKAGE}$			±0.1	±10	µA
Three-State Output Capacitance	C_{OUT}			3.5		pF

Note 1: Reference inputs driven by operational amplifiers for Kelvin-sensed operation.

Note 2: For unipolar mode, the analog input voltage V_{INP} must be within 0V and V_{REF}, V_{INN} = V_{REF} / 2; where V_{REF} = V_{RFPS} - V_{RFNS}. For differential mode, the analog inputs INP and INN must be within 0V and V_{REF}; where V_{REF} = V_{RFPS} - V_{RFNS}. The common mode of the inputs INP and INN is V_{REF} / 2.

Note 3: Minimum and maximum parameters are not tested. Guaranteed by design.

Note 4: R_I varies inversely with sample rate.

Note 5: Calibration remains valid for temperature changes within ±20°C and power-supply variations ±5%.

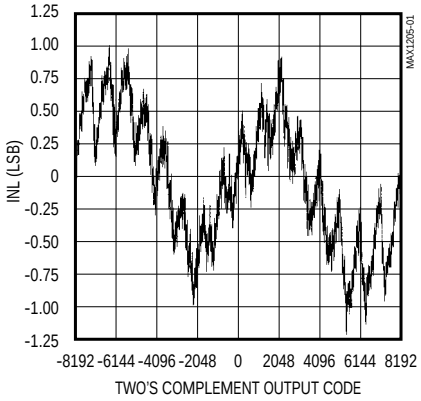
Note 6: All AC specifications are shown for the differential mode.

+5V Single-Supply, 1Msps, 14-Bit Self-Calibrating ADC

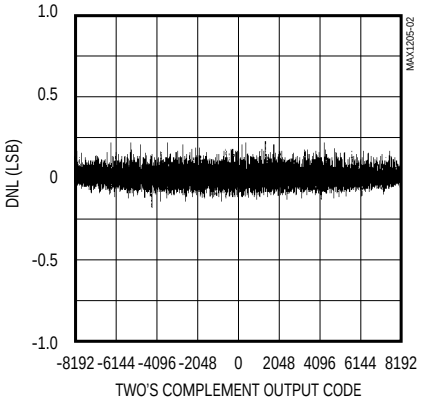
Typical Operating Characteristics

(AV_{DD} = +5V ±5%, DV_{DD} = DRV_{DD} = +3.3V, V_{RFPS} = +4.096V, V_{RFNS} = AGND, V_{CM} = +2.048V, differential input, f_{CLK}= 2.048MHz, calibrated, T_A = +25°C, unless otherwise noted.)

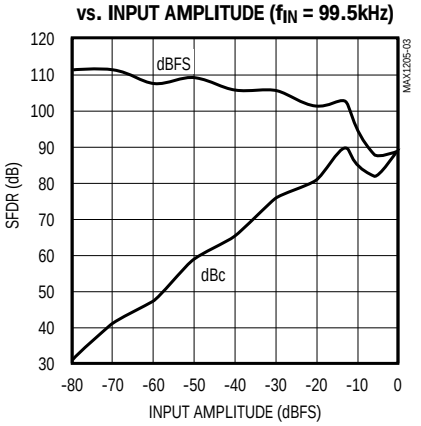
INTEGRAL NONLINEARITY vs. TWO'S COMPLEMENT OUTPUT CODE



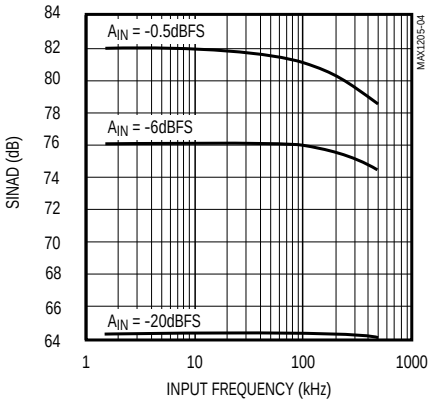
DIFFERENTIAL NONLINEARITY vs. TWO'S COMPLEMENT OUTPUT CODE



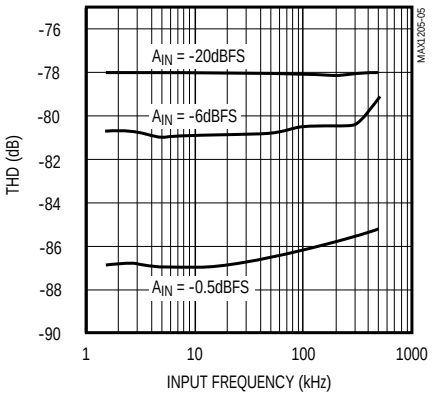
SINGLE-TONE SPURIOUS-FREE DYNAMIC RANGE vs. INPUT AMPLITUDE (f_{IN} = 99.5kHz)



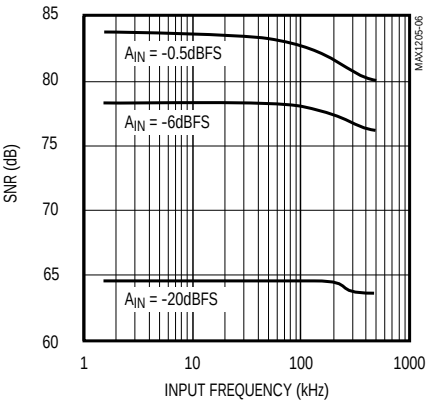
SIGNAL-TO-NOISE RATIO PLUS DISTORTION vs. INPUT FREQUENCY



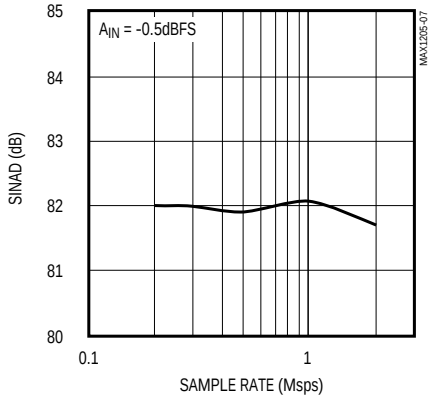
TOTAL HARMONIC DISTORTION vs. INPUT FREQUENCY



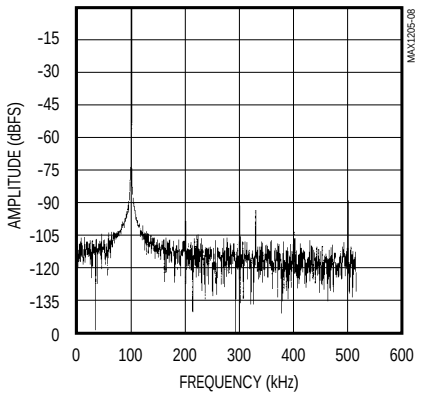
SIGNAL-TO-NOISE RATIO vs. INPUT FREQUENCY



SIGNAL-TO-NOISE RATIO PLUS DISTORTION vs. SAMPLING RATE (f_{IN} = 99.5kHz)



TYPICAL FFT (f_{IN} = 99.5kHz, 2048 VALUE RECORD)

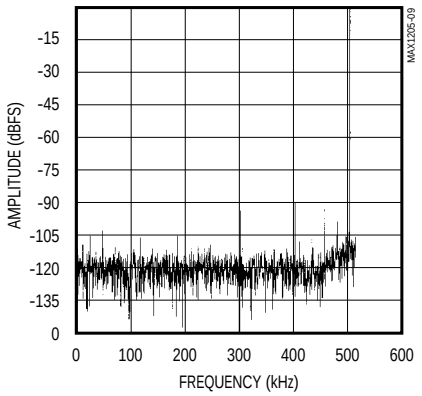


+5V Single-Supply, 1Msps, 14-Bit Self-Calibrating ADC

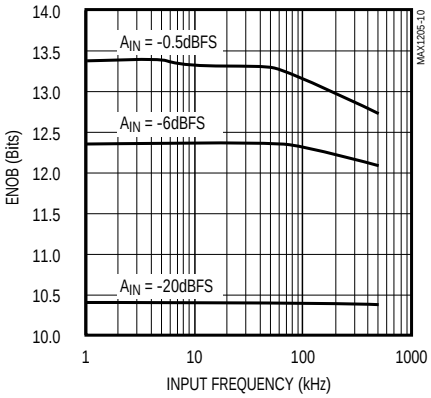
Typical Operating Characteristics (continued)

(AV_{DD} = +5V ±5%, DV_{DD} = DRV_{DD} = +3.3V, V_{RFPS} = +4.096V, V_{RFNS} = AGND, V_{CM} = +2.048V, differential input, f_{CLK}= 2.048MHz, calibrated, T_A = +25°C, unless otherwise noted.)

TYPICAL FFT
(f_{IN} = 504.5kHz, 2048 VALUE RECORD)



EFFECTIVE NUMBER OF BITS vs. INPUT FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	ST_CAL	Digital Input to Start Calibration. ST_CAL = 0: Normal conversion mode. ST_CAL = 1: Start self-calibration.
2, 4, 5	AGND	Analog Ground
3, 6	AV_{DD}	Analog Power Supply, +5V ±5%
7	DOR	Data Out-of-Range Bit
8	D13	Bit 13 (MSB)
9	D12	Bit 12
10	D11	Bit 11
11	D10	Bit 10
12	D9	Bit 9
13	D8	Bit 8
14	D7	Bit 7
15	D6	Bit 6
16	DRV_{DD}	Digital Power Supply for the Output Drivers, +3V to +5.25V, $DRV_{DD} \le DV_{DD}$
17, 28, 29	DGND	Digital Ground
18	D5	Bit 5
19	D4	Bit 4
20	D3	Bit 3
21	D2	Bit 2
22	D1	Bit 1
23	D0	Bit 0 (LSB)
24	TEST3	Test Pin 3. **Leave unconnected.**

Pin Description (continued)

PIN	NAME	FUNCTION
25	TEST2	Test Pin 2. **Leave unconnected.**
26	TEST1	Test Pin 1. **Leave unconnected.**
27, 30	DV_{DD}	Digital Power Supply, +3V to +5.25V
31	CLK	Input Clock. Receives power from AV_{DD} to reduce jitter.
32	DAV	Data Valid Clock Output. This clock can be used to transfer the data to a memory or any other data-acquisition system.
33	OE	Output Enable Input. OE = 0: D0-D13 and DOR are high impedance. OE = 1: All bits are active.
34	TEST0	Test Pin 0. **Leave unconnected.**
35	CM	Common-Mode Voltage. Analog Input. Drive midway between positive and negative reference voltages.
36	RFPF	Positive Reference Voltage. Force input.
37	RFPS	Positive Reference Voltage. Sense input.
38	RFNF	Negative Reference Voltage. Force input.
39	RFNS	Negative Reference Voltage. Sense input.
40	INP	Positive Input Voltage
41, 42	N.C.	Not Connected. No internal connection.
43	INN	Negative Input Voltage
44	END_CAL	Digital Output for End of Calibration. END_CAL = 0: Calibration in progress. END_CAL = 1: Normal conversion mode.

Detailed Description

Converter Operation

The MAX1205 is a 14-bit, monolithic, analog-to-digital converter (ADC) capable of conversion rates up to 1Msps. It uses a multistage, fully differential pipelined architecture with digital error correction and self-calibration to provide typically greater than 91dB spurious-free dynamic range at a 1Msps sampling rate. Its signal-to-noise ratio, harmonic distortion, and intermodulation products are also consistent with 14-bit accuracy up to the Nyquist frequency. This makes the device suitable for applications such as imaging, scanners, data acquisition, and digital communications.

Figure 1 shows the simplified, internal structure of the ADC. A switched-capacitor pipelined architecture is used to digitize the signal at a high throughput rate. The first four stages of the pipeline use a low-resolution quantizer to approximate the input signal. The multiplying digital-to-analog converter (MDAC) stage is used to subtract the quantized analog signal from the input. The residue is then amplified with a fixed gain and passed on to the next stage. The accuracy of the converter is improved by a digital calibration algorithm which corrects for mismatches between the capacitors in the switched capacitor MDAC. Note that the pipeline introduces latency of four sampling periods between the input being sampled and the output appearing at D13–D0.

While the device can handle both single-ended and differential inputs (see *Requirements for Reference and Analog Signal Inputs*), the latter mode of operation will guarantee best THD and SFDR performance. The differential input provides the following advantages compared to a single-ended operation:

- Twice as much signal input span
- Common-mode noise immunity
- Virtual elimination of the even-order harmonics
- Less stringent requirements on the input signal processing amplifiers

+5V Single-Supply, 1Msps, 14-Bit Self-Calibrating ADC

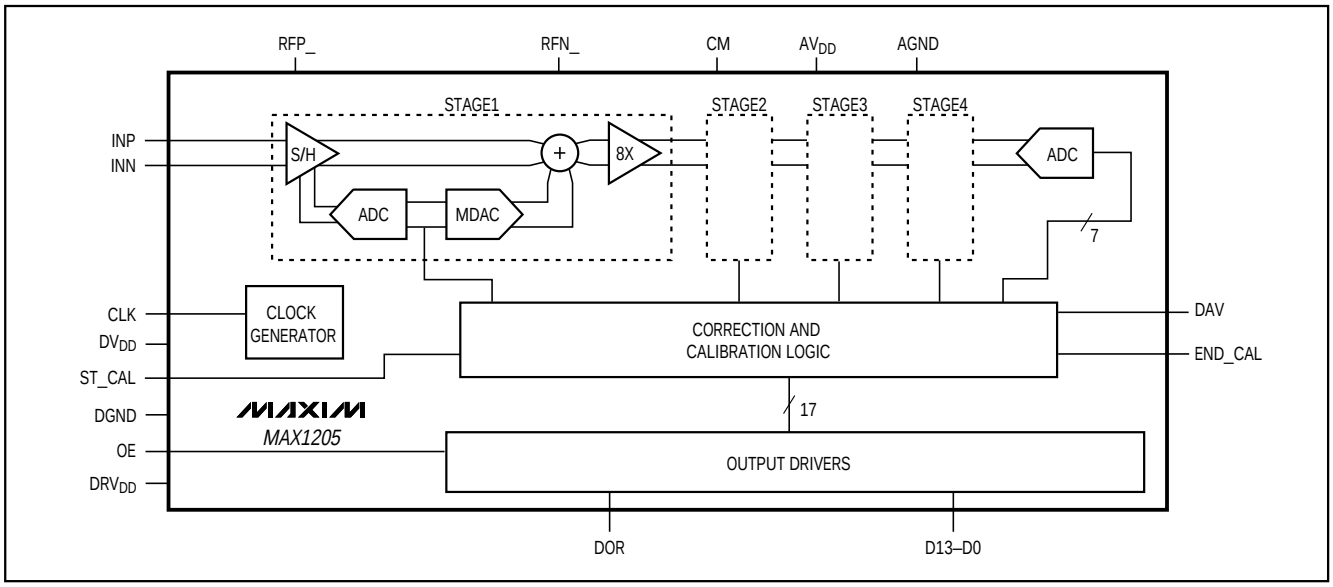


Figure 1. Internal Block Diagram

Requirements for Reference and Analog Signal Inputs

Fully differential switched-capacitor circuits (SC) are used for both the reference and analog inputs (Figure 2). This allows either single-ended or differential signals to be used in the reference and/or analog signal paths. The signal voltage on these pins (INP, INN, RFN_, RFP_) should never exceed the analog supply rail, AV_{DD}, and should not fall below ground.

Choice of Reference

It is important to choose a low-noise reference, such as the MAX6341, which can provide both excellent load regulation and low temperature drift. The equivalent input circuit for the reference pins is shown in Figure 3. Note that the reference pins drive approximately 1kΩ of resistance on chip. They also drive a switched capacitor of 21pF. To meet the dynamic performance, the reference voltage is required to settle to 0.0015% within one clock cycle. Accomplish this by choosing an appropriate driving circuit (Figure 4). The capacitors at the reference pins (RFPF, RFNF) provide the dynamic charge required during each clock cycle, while the op amps ensure accuracy of the reference signals. These capacitors must have low dielectric-absorption characteristics, such as polystyrene or teflon capacitors.

The reference pins can be connected to either single-ended or differential voltages within the specified maximum levels. Typically the positive reference pin (RFPF) would be driven to 4.096V, and the negative reference pin (RFNF) connected to analog ground. There are sense pins, RFPS and RFNS, which can be used with

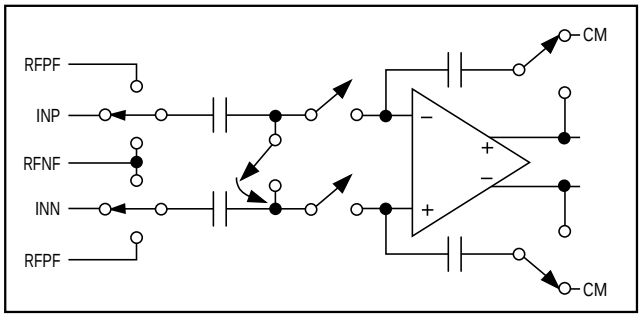


Figure 2. Simplified MDAC Architecture

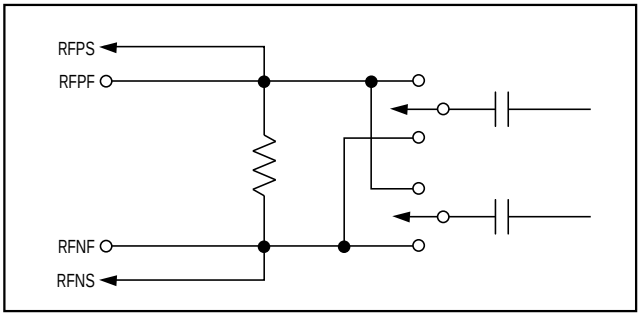


Figure 3. Equivalent Input at the Reference Pins. The sense pins should not draw any DC current.

external amplifiers to compensate for any resistive drop on these lines, internal or external to the chip. Ensure a correct reference voltage by using proper Kelvin connections at the sense pins.

Common-Mode Voltage

The switched capacitor input circuit at the analog input allows signals between AGND and the analog power supply. Since the common-mode voltage has a strong influence on the performance of the ADC, the best results are obtained by choosing V_{CM} to be at half the difference between the reference voltages V_{RFP} and V_{RFN}. Achieve this by using a resistive divider between the two reference potentials. Figure 4 shows a typical driving circuit for good dynamic performance.

Analog Signal Conditioning

For single-ended inputs the negative analog input pin (INN) is connected to the common-mode voltage pin (CM), and the positive analog input pin (INP) is connected to the input.

To take full advantage of the ADC's superior AC performance up to the Nyquist frequency, drive the chip with differential signals. In communication systems, the signals may inherently be available in differential mode. Medical and/or other applications may only provide single-ended inputs. In this case, convert the single-ended signals into differential ones by using the circuit recommended in Figure 5. Use low-noise, wideband amplifiers such as the MAX4108 to maintain the signal purity over the full-power bandwidth of the MAX1205 input.

Lowpass or bandpass signals may be required to improve the signal-to-noise-and-distortion ratio of the incoming signal. For low-frequency signals (<100kHz), active filters may be used. For higher frequencies, passive filters are more convenient.

Single-Ended to Differential Conversion Using Transformers

An alternative single-ended to differential-ended conversion method is a balun transformer such as the CTX03-13675 from Coiltronics. An important benefit of these transformers is their ability to level-shift single-ended signals referred to ground on the primary side to optimum common-mode voltages on the secondary side. At frequencies below 20kHz, the transformer core begins to saturate, causing odd-order harmonics.

Clock Source Requirements

Pipelined ADCs typically need a 50% duty cycle clock. To avoid this constraint, the MAX1205 provides a

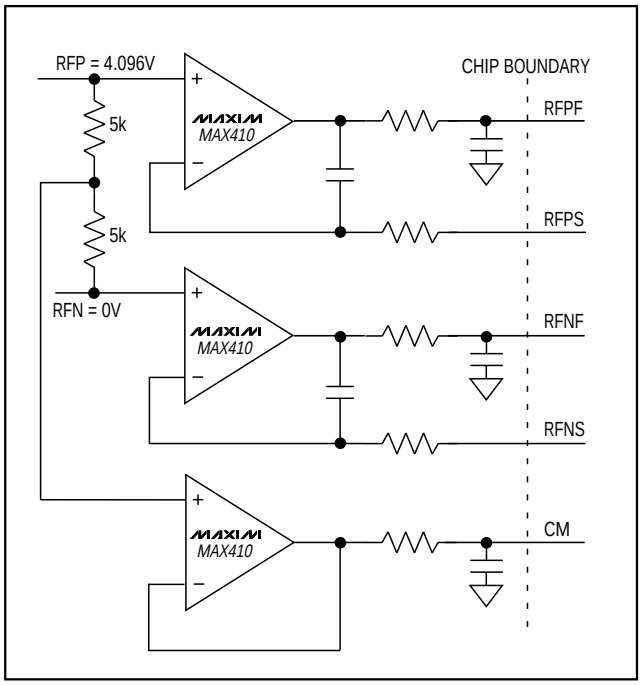


Figure 4. Drive Circuit for the Reference Pins and the Common-Mode Pin

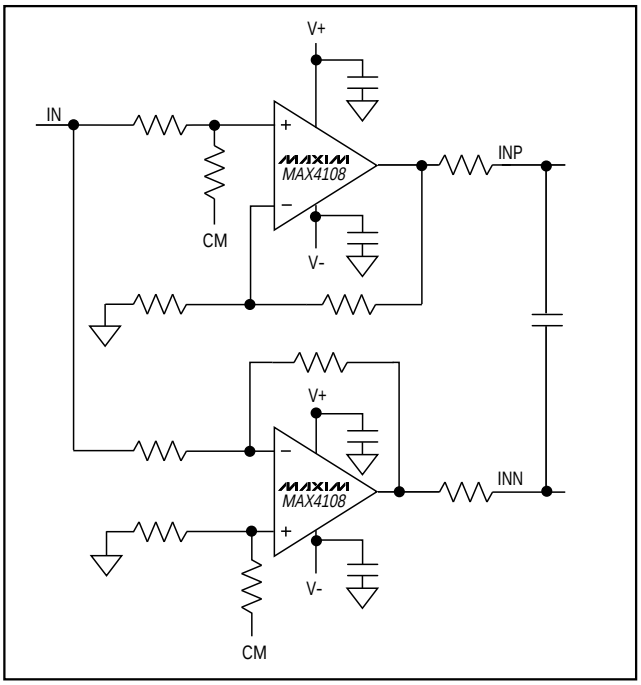


Figure 5. A simple circuit generates differential signals from a single-ended input referred to analog ground. The common-mode voltage at INP and INN is the same as CM.

+5V Single-Supply, 1Msps, 14-Bit Self-Calibrating ADC

divide-by-two circuit, which relaxes this requirement. The clock generator should be chosen commensurate with the frequency range, amplitude, and slew rate of the signal source. If the slew rate of the input signal is small, the jitter requirement on the clock is relaxed. However, if the slew rate is high, the clock jitter needs to be kept at a minimum. For a full-scale amplitude input sine wave, the maximum possible signal-to-noise ratio (SNR) due completely to clock jitter is given by:

$$SNR_{MAX} = \frac{1}{2\pi f_{IN}\sigma_{JITTER}}$$

For example, if f_{IN} is 0.5MHz and σ_{JITTER} is 20ps RMS, then the SNR limit due to jitter is about 84dB. Generating such a clock source requires a low-noise comparator and a low-phase-noise signal generator. The clock circuit shown in Figure 6 is a possible solution.

Calibration Procedure

Since the MAX1205 is based on a pipelined architecture, low-resolution quantizers (“coarse ADCs”) are used to approximate the input signal. MDACs of the same resolution are then used to reconstruct the input signal, which is subtracted from the input and the residue amplified by the SC gain stage. This residue is then passed on to the next stage.

The accuracy of the MAX1205 is limited by the precision of the MDAC, which is strongly dependent on the matching of the capacitors used. The mismatch between the capacitors is determined and stored in an on-chip memory, which is later used during the conversion of the input signal.

During the calibration procedure, the clock must be running continuously. ST_CAL (start of calibration) is initiated by a positive pulse with a minimum width of four clock cycles, but no longer than about 17,400 clock cycles (Figure 8).

The ST_CAL input may be asynchronous with the clock, since it is retimed internally. With ST_CAL activated, END_CAL goes low one or two clock cycles later and remains low until the calibration is complete. During this period, the reference voltages must be stable to less than 0.01%; otherwise the calibration will be invalid. During calibration, the analog inputs INP and INN are not used; however, better performance is achieved if these inputs are static. Once END_CAL goes high (indicating that the calibration procedure is complete), the ADC is ready for conversion.

Once calibrated, the MAX1205 is insensitive to small changes (<5%) in power-supply voltage or temperature. Following calibration, if the temperature changes more than ±20°C, the device should be recalibrated to maintain optimum performance.

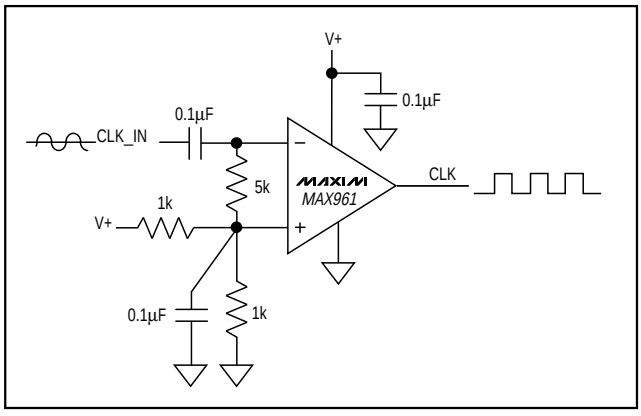


Figure 6. Clock Generation Circuit Using a Low-Noise Comparator

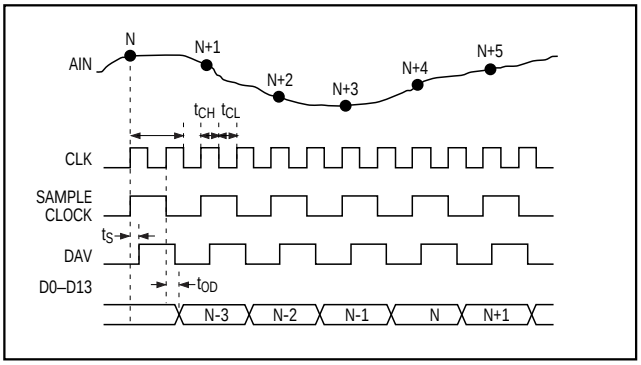


Figure 7. Main Timing Diagram

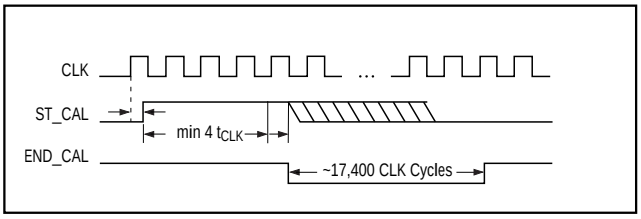


Figure 8. Timing for Start and End of Calibration

Figure 9. Timing for Bus Access and Bus Relinquish—Controlled by Output Enable (OE)

Two's Complement Output

The MAX1205 outputs data in two's complement format. Table 1 shows how to convert the various full-scale inputs into their two's complement output codes.

Applications Information

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{(MAX)} = (6.02N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise including thermal noise, reference noise, clock jitter, etc. Therefore, SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first nine harmonics, and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is the ratio of the fundamental input frequency's RMS amplitude to all other ADC output signals:

$$SINAD\ (dB) = 20\log\left[(Signal_{RMS} / (Noise + Distortion)_{RMS}\right]$$

Effective Number of Bits (ENOB)

ENOB indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range for the ADC, the effective number of bits can be calculated as follows:

$$ENOB = (SINAD - 1.76) / 6.02$$

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first nine harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20\log\left[\frac{\sqrt{\left(V_2^2 + V_3^2 + V_4^2 + \cdots + V_9^2\right)}}{V_1}\right]$$

where V_1 is the fundamental amplitude, and V_2 through V_9 are the amplitudes of the 2nd through 9th order harmonics.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset.

Grounding and Power-Supply Decoupling

Grounding and power-supply decoupling strongly influence the performance of the MAX1205. At 14-bit resolution, unwanted digital crosstalk may couple through the input, reference, power-supply, and ground connections; this adversely affects the SNR or SFDR. In addition, electromagnetic interference (EMI) can either couple into or be generated by the MAX1205. Therefore, grounding and power-supply decoupling guidelines should be closely followed.

Table 1. Two's Complement Conversion

SCALE	OFFSET BINARY	TWO'S COMPLEMENT	ONE'S COMPLEMENT
+FSR - 1LSB	1111....1111	0111....1111	0111....1111
+3/4FSR	1110....0000	0110....0000	0110....0000
+1/2FSR	1100....0000	0100....0000	0100....0000
+1/4FSR	1010....0000	0010....0000	0010....0000
+0	1000....0000	0000....0000	0000....0000
-0	—	—	1111....1111
-1/4FSR	0110....0000	1110....0000	1101....1111
-1/2FSR	0100....0000	1100....0000	1011....1111
-3/4FSR	0010....0000	1010....0000	1001....1111
-FSR + 1LSB	0000....0001	1000....0001	1000....0000
-FSR	0000....0000	1000....0000	—

+5V Single-Supply, 1Msps, 14-Bit Self-Calibrating ADC

First, a multilayer printed circuit board (PCB) with separate ground and power-supply planes is recommended. Run high-speed signal traces directly above the ground plane. Since the MAX1205 has separate analog and digital ground buses (AGND and DGND respectively), the PCB should also have separate analog and digital ground sections connected at only one point (star ground). Digital signals should run above the digital ground plane and analog signals should run above the analog ground plane. Digital signals should be kept far away from the sensitive analog inputs, reference inputs senses, common-mode input, and clock input.

The MAX1205 has three power-supply inputs: analog V_{DD} (AV_{DD}), digital V_{DD} (DV_{DD}), and drive V_{DD} (DRV_{DD}). Each AV_{DD} input should be decoupled with parallel ceramic-chip capacitors of values 0.1µF and 0.001µF, with these capacitors as close to the pin as possible and with the shortest possible connection to the ground plane. The DV_{DD} pins should also have separate 0.1µF capacitors adjacent to their respective pins, as should the DRV_{DD} pin. Minimize the digital load capacitance. However, if the total load capacitance on each digital output exceeds 20pF, the DRV_{DD} decoupling capacitor should be increased or, preferably, digital buffers should be added.

The power-supply voltages should be decoupled with large tantalum or electrolytic capacitors at the point they enter the PCB. Ferrite beads with additional decoupling capacitors forming a pi-network may improve performance.

The analog power-supply input (AV_{DD}) for the MAX1205 is typically +5V while the digital supplies can vary from +5V to +3V. Usually, DV_{DD} and DRV_{DD} pins are connected to the same power supply. Note that the DV_{DD} supply voltage must be greater than or equal to the DRV_{DD} voltage. For example, a digital +3.3V supply could be connected to DRV_{DD} while a cleaner +5V supply is connected to DV_{DD}, resulting in slightly improved performance. Alternatively, the +3.3V supply could be connected to both DRV_{DD} and DV_{DD}. However, the +3.3V supply should not be connected to DV_{DD} while the +5V supply is connected to DRV_{DD} (Table 2).

Table 2. Power-Supply Voltage Combinations

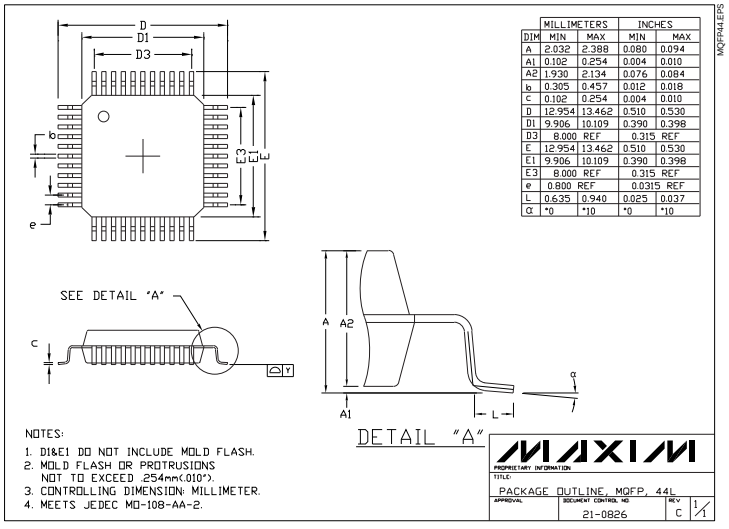
AV_{DD} (V)	DV_{DD} (V)	DRV_{DD} (V)	ALLOWED/NOT ALLOWED
+5	+5	+5	Allowed
+5	+5	+3.3	Allowed
+5	+3.3	+3.3	Allowed
+5	+3.3	+5	Not Allowed

Chip Information

TRANSISTOR COUNT: 56,577

SUBSTRATE CONNECTED TO: AGND

Package Information



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.032	2.388	0.080	0.094
A1	0.102	0.254	0.004	0.010
A2	1.930	2.134	0.076	0.084
b	0.305	0.457	0.012	0.018
c	0.102	0.254	0.004	0.010
D	12.954	13.462	0.510	0.530
D1	9.906	10.109	0.390	0.398
D3	8.000 REF		0.315 REF	
E	12.954	13.462	0.510	0.530
E1	9.906	10.109	0.390	0.398
E3	8.000 REF		0.315 REF	
e	0.800 REF		0.0315 REF	
L	0.635	0.940	0.025	0.037
α	*0	*10	*0	*10