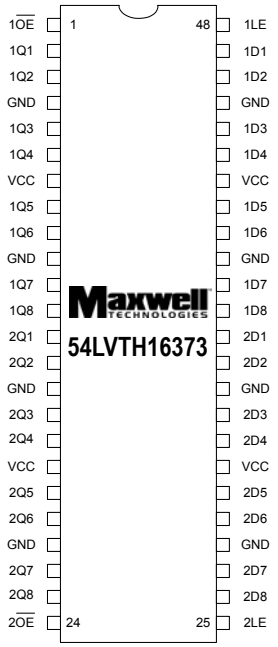
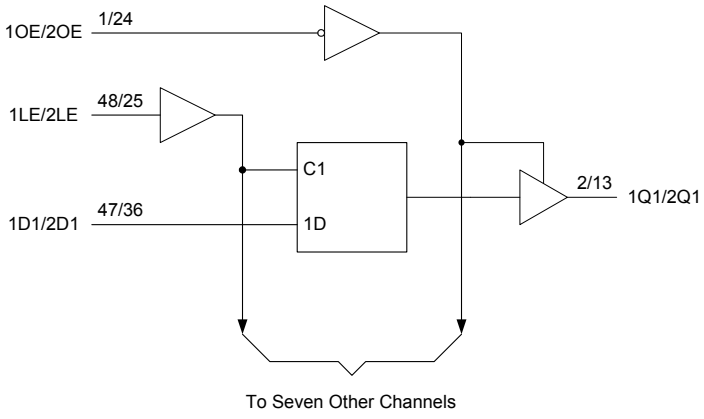
PRELIMINARY

54LVTH16373
3.3V ABT16-Bit Transparent D-Type Latches





Logic Diagram

FEATURES:

- 3.3V low voltage advanced BiCMOS technology (LVT) 16-bit transparent D-type latches with 3-state outputs
- Total dose hardness:
  - > 100 krad (Si), dependent upon space mission
- Single event effect:
  - SEL_{TH} : No LU > 119 MeV/mg/cm^2
- Package: 48 pin RAD-PAK® flat package
- Operating temperature range:
  - 55 to 125°C
- Distributed V_{CC} and GND pin configuration minimizes high-speed switching noise
- Supports mixed-mode signal operation
  - 5V input and output voltages with 3.3V V_{CC}
- Supports unregulated battery operation down to 2.7V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC}=3.3V, T_A=25°C
- Latch-up performance exceeds 500mA per JEDEC standard
- Supports live insertion
- Bus-hold data inputs eliminate the need for external pullup resistors

DESCRIPTION:

Maxwell Technologies' 54LVTH16373 16-bit transparent D-type latches with 3-state output features a greater than 100 krad (Si) total dose tolerance, dependent upon space mission. The 54LVTH16373 is designed for low voltage (3.3V) V_{CC} operation, but with the capability to provide a TTL interface to a 5V system environment. It is suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The 54LVTH16373 can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is low, the Q output are latched at the levels set up at the data (D) inputs. When LE is high, the Q outputs follow the D inputs. A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state or a high impedance state. In the high impedance state, the outputs neither load nor drive the bus lines significantly. The high impedance state and the increased drive provide the capability to drive bus lines without the need for interface or pullup components. $\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high impedance state.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Class S.

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TABLE 1. PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1, 24	$1\overline{OE}$-$2\overline{OE}$	Output Enable
2, 3, 5, 6, 8, 9, 11, 12	1Q1-1Q8	Outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground
7, 31, 42	V_{CC}	Power Supply
13, 14, 16, 17, 19, 20, 22, 23	2Q1-2Q8	Outputs
25, 48	2LE-1LE	Latch Enable
26, 27, 29, 30, 32, 31, 32, 33, 35, 36	2D8-2D1	Inputs
37, 38, 40, 41, 43, 44, 46, 47	1D8-1D1	Inputs

TABLE 2. 54LVTH16373 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply voltage range	V_{CC}	-0.5	4.6	V
Input voltage range [1]	V_I	-0.5	7	V
Voltage range applied to any output in the high state or power-off state [1]	V_O	-0.5	7	V
Current into any output in the low state	I_O	--	96	mA
Current into any output in the high state [2]	I_O	--	48	mA
Input clamp current (V_I < 0)	I_{IK}	--	-50	mA
Output clamp current (V_O < O)	I_{OK}	--	-50	mA
Maximum power dissipation at TA = 55°C [3]	P_D	--	0.85	mW
Storage temperature range	T_S	-65	150	˚C

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150˚C and a board trace length of 750 mils.

TABLE 3. DELTA LIMITS

PARAMETER	VARIATION
$I_{CC(OL)}$	±10% of specified value in Table 5
$I_{CC(OH)}$	±10% of specified value in Table 5
$I_{CC(OD)}$	±10% of specified value in Table 5

TABLE 4. 54LVTH16373 RECOMMENDED OPERATING CONDITIONS [1]

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply voltage	V_{CC}	2.7	3.6	V
High-level input voltage	V_{IH}	2	--	V
Low-level input voltage	V_{IL}	--	0.8	V
Input voltage	V_I	--	5.5	V
High-level output current	I_{OH}	--	-24	mA
Low-level output current	I_{OL}	--	68	mA
Input transition rise or fall rate (outputs enabled)	$\Delta t/\Delta v$	--	10	ns/V
Operating free-air temperature	T_A	-55	125	˚C

1. Unused control inputs must be held high or low to prevent them from floating.

TABLE 5. 54LVTH16373 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±10%, T_A = -55 to 125˚C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS			MIN	MAX	UNIT
Input Clamp Voltage	V_{IK}	V_{CC} = 2.7	I_I = -18mA		--	-1.2	V
High-Level Output Voltage	V_{OH}	V_{CC} = 2.7V to 3.6V	I_{OH} = -100µA		V_{CC} -0.2	--	V
		V_{CC} = 2.7V	I_{OH} = -8mA		2.4	--	
		V_{CC} = 3V,	I_{OH} = -32mA		2.0	--	
Low-Level Output Voltage	V_{OL}	V_{CC} = 2.7V	I_{OL} = 100µA		--	0.2	V
			I_{OL} = 24mA		--	0.5	
		V_{CC} = 3V	I_{OL} = 16mA		--	0.4	
			I_{OL} = 32mA		--	0.5	
Input Current	I_I	V_{CC} = 0 or 3.6V	V_I = 5.5V			10	µA
		V_{CC} = 3.6V	V_I = V_{CC} or GND	Control Inputs	--	±1	
		V_{CC} = 3.6V	V_I = V_{CC}	Data Inputs	--	1	
			V_I = 0		--	-5	

TABLE 5. 54LVTH16373 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±10%, T_A = -55 to 125˚C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS			MIN	MAX	UNIT
Hold Current	$I_{I(HOLD)}$	V_{CC} = 3V	V_I = 0.8V	Data Inputs	75	--	µA
			V_I = 2V		-75	--	
Output Disabled Leakage Current - High	I_{OZH}	V_{CC} = 3.6V, V_O = 3V			--	5	µA
Output Disabled Leakage Current - Low	I_{OZL}	V_{CC} = 3.6V, V_O = 0.5V			--	-5	µA
Power Up Current	I_{OZPU}[2]	V_{CC} = 0 to 1.5V, V_O = 0.5V to 3V, $\overline{OE}$ = don't care			--	±100	µA
Power Down Current	I_{OZPD}[2]	V_{CC} = 1.5V to 0, V_O = 0.5V to 3V, $\overline{OE}$ = don't care			--	±100	µA
Supply Current	I_{CC}	V_{CC} = 3.6V I_O = 0 V_I = V_{CC} or GND		Outputs high	--	0.19	mA
				Outputs low	--	5	
				Outputs disabled	--	0.19	
Delta Supply Current	ΔI_{CC}[1]	V_{CC} = 3V to 3.6V, One input at V_{CC} -0.6V, Other inputs at V_{CC} or GND			--	0.2	mA
Input Capacitance	C_I[2]	V_I = 3V or 0			--	10	pF
Input Output Capacitance	C_O[2]	V_O = 3V or 0			--	15	pF

1. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
2. Guaranteed by design.

TABLE 6. 54LVTH16373 AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±10%, T_A = -55 to 125˚C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	V_{CC} = 3.3V ± 0.3V		V_{CC} = 2.7V		UNIT
		MIN	MAX	MIN	MAX	
Pulse duration, LE high	t_W	3.3	--	3.3	--	ns
Setup time, data before LEØ	t_{SU}	0.5	--	0.5	--	ns
Hold time, data after LEØ	t_H	1.8	--	2	--	ns
Propagation Delay Time D to Q	t_{PLH}	2.7	5	--	5.7	ns
	t_{PHL}	2.9	4.9	--	5.7	
Propagation Delay Time LE to Q	t_{PLH}	3.6	6	--	6.8	ns
	t_{PHL}	4.7	6.9	--	8.8	
Output Enable Time $\overline{OE}$ to Q	t_{PZH}	2.9	5.3	--	6.3	ns
	t_{PZL}	3	5.1	--	5.9	

TABLE 6. 54LVTH16373 AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±10%, T_A = -55 to 125˚C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	V_{CC} = 3.3V ± 0.3V		V_{CC} = 2.7V		UNIT
		MIN	MAX	MIN	MAX	
Output Disable Time $\overline{OE}$ to Q	t_{PHZ}	4.3	6.8	--	7.6	ns
	t_{PLZ}	4	5.8	--	5.9	

TABLE 7. FUNCTION TABLE

(EACH 8-BIT SECTION)

INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

FIGURE 1. LOAD CIRCUIT FOR OUTPUTS

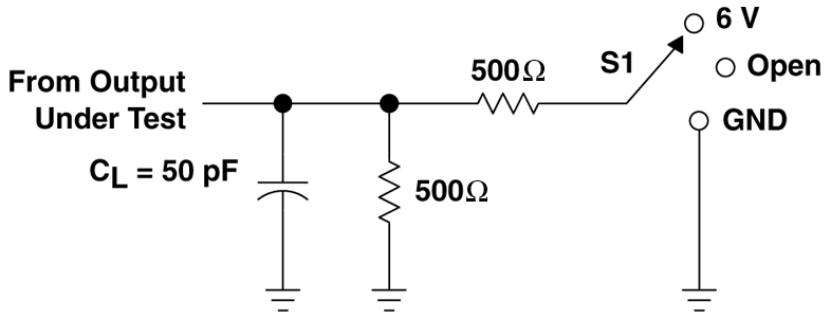


Figure Note:

1. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

TEST	S1
T_{PLH}/T_{PHL}	Open
T_{PLZ}/T_{PZL}	6V
T_{PHZ}/T_{PZH}	GND

FIGURE 2. PULSE DURATION

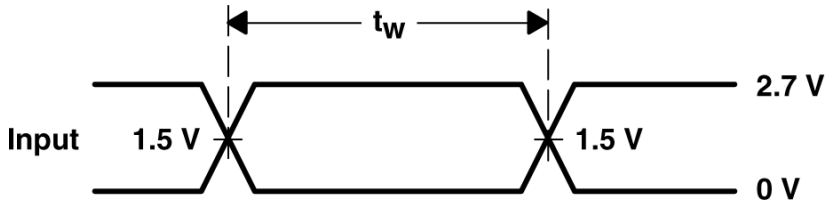


FIGURE 3. SETUP AND HOLD TIMES

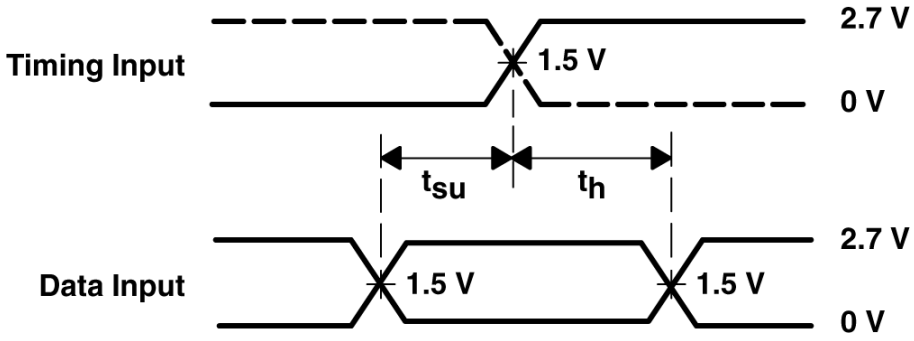


FIGURE 4. PROPAGATION DELAY TIMES INVERTING AND NON-INVERTING OUTPUTS

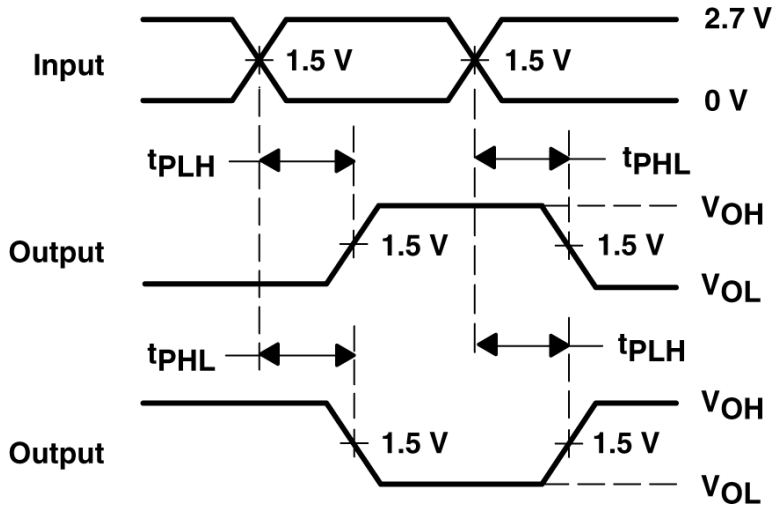


FIGURE 5. ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

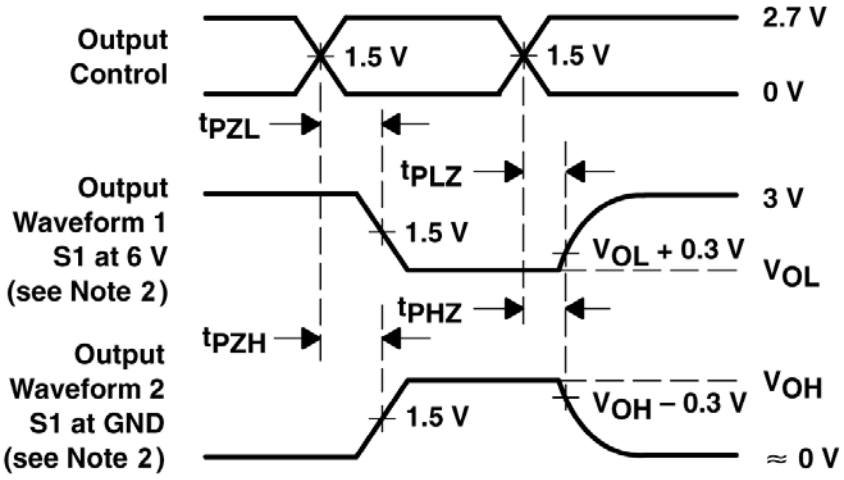
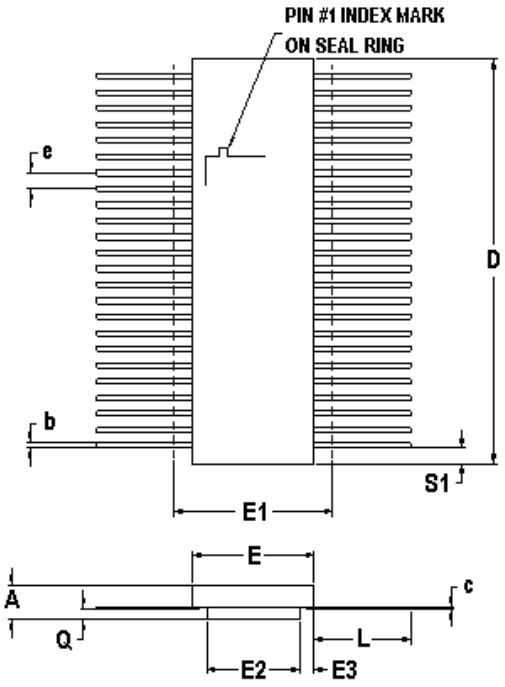


FIGURE NOTES:

2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, ZO = 5Ω, tr ≤ 2.5 ns, tf ≤ 2.5 ns.
4. The outputs are measured one at a time with one transition per measurement.



48 PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.144	0.160	0.176
b	0.008	0.010	0.014
c	0.004	0.006	0.007
D	--	0.620	0.640
E	0.370	0.380	0.390
E1	--	--	0.410
E2	0.200	0.210	0.220
E3	0.075	0.085	--
e	0.025 BSC		
L	0.275	0.285	0.295
Q	0.013	0.019	0.045
S1	0.005	0.018	--
N	48		

F48-01
Note: All dimensions in inches

Important Notice:

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