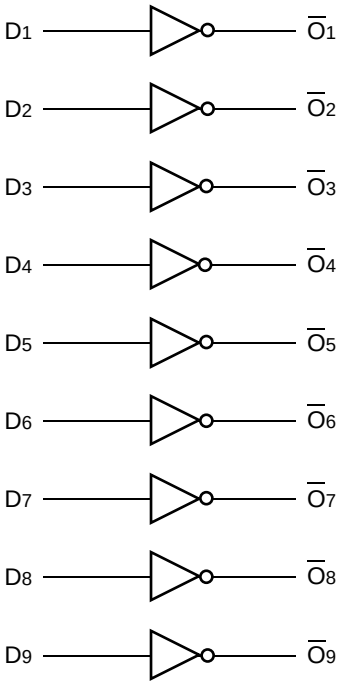
FEATURES

- Max. propagation delay of 700ps
- I_{EE} min. of –55mA
- Extended supply voltage option: V_{EE} = –4.2V to –5.5V
- Voltage and temperature compensation for improved noise immunity
- 70% faster than Fairchild 300K at lower power
- Internal 75KΩ input pull-down resistors
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

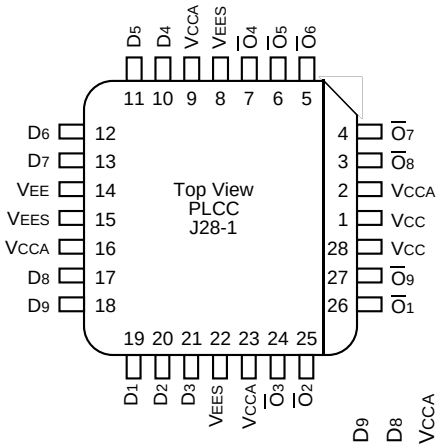
BLOCK DIAGRAM

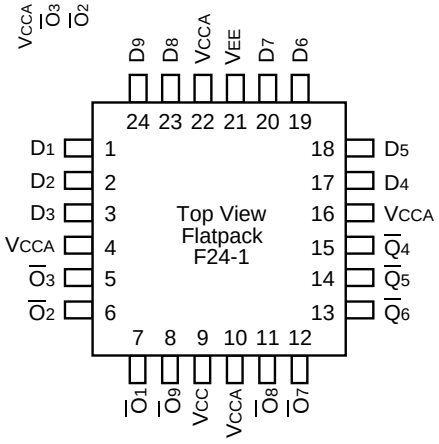


DESCRIPTION

The SY100S321 is a monolithic 9-bit inverter. The device contains nine inverting buffer gates with single input and output.

PIN CONFIGURATIONS





PIN NAMES

Pin	Function
D_1 – D_9	Data Inputs
$\overline{Q}_1$ – $\overline{Q}_9$	Data Outputs
V_{EES}	V_{EE} Substrate
V_{CCA}	V_{CCO} for ECL Outputs

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current	—	—	200	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–55	–41	–25	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay[1] Data to Output	300	800	300	800	300	800	ps	
t_{TLH} t_{THL}	Transition Time[1] 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t_S, G–G	Skew, Gate-to-Gate	—	200	—	200	—	200	ps	

NOTE:

1. Reference figures 1 and 2

PLCC

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay[1] Data to Output	300	700	300	700	300	700	ps	
t_{TLH} t_{THL}	Transition Time[1] 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t_S, G–G	Skew, Gate-to-Gate	—	200	—	200	—	200	ps	

NOTE:

1. Reference figures 1 and 2

TEST CIRCUITRY(1)

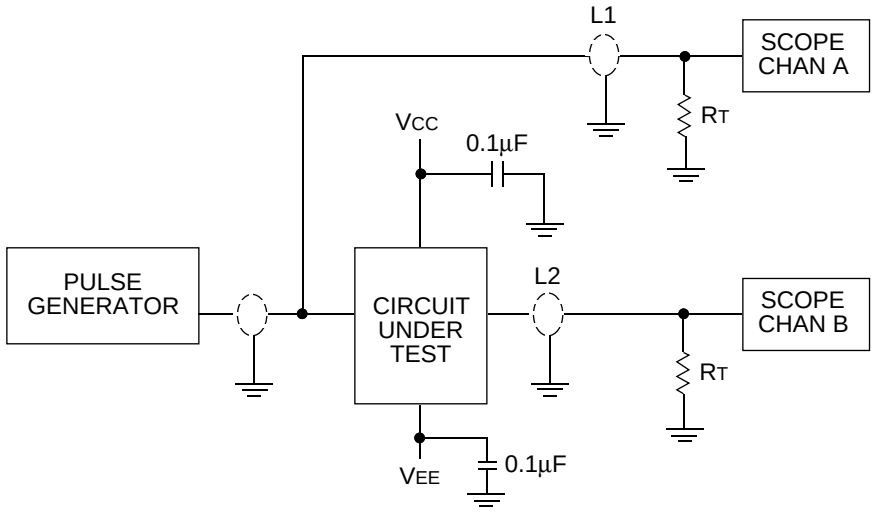


Figure 1. AC Test Circuit

NOTE:

1. V_{CC}, V_{CCA} = +2V, V_{EE} = –2.5V.
   L1 and L2 = equal length 50Ω impedance lines.
   R_T = 50Ω terminator internal to scope.
   Decoupling 0.1µF from GND to V_{CC} and V_{EE}.
   All unused outputs are loaded with 50Ω to GND.
   C_L = Fixture and stray capacitance ≤ 3pF.

SWITCHING WAVEFORMS

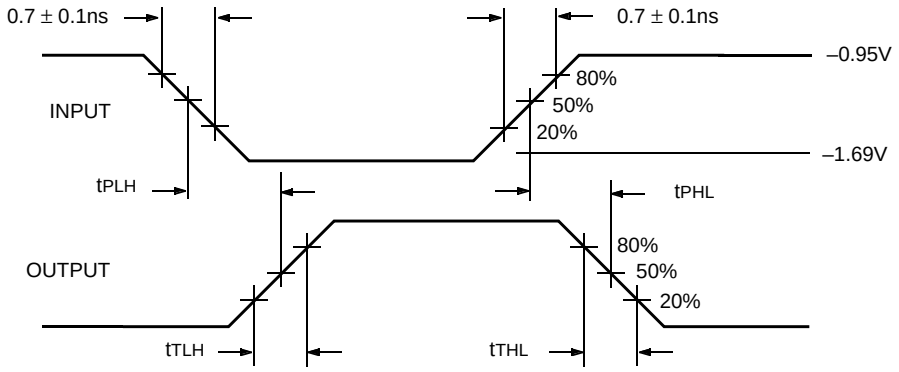


Figure 2. Propagation Delay and Transition Times

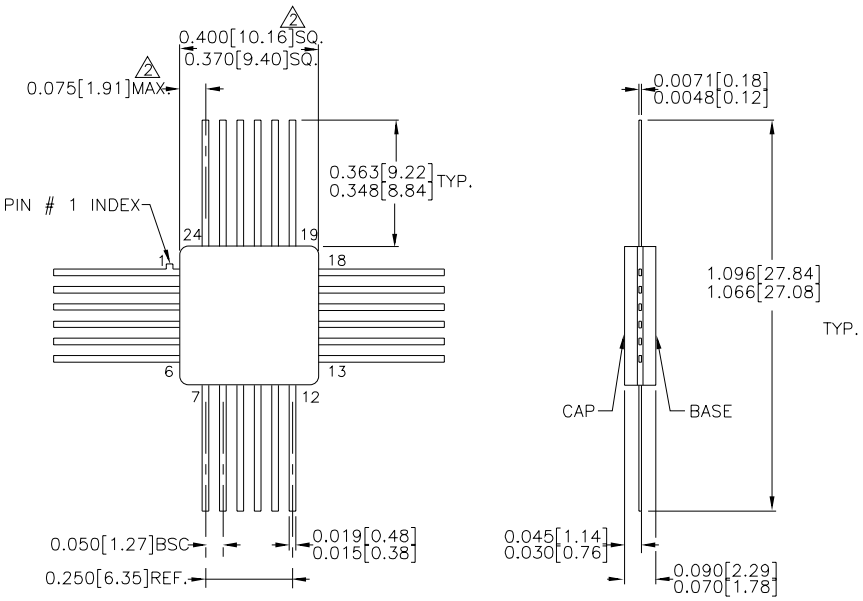
NOTE:

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S321FC	F24-1	Commercial
SY100S321JC	J28-1	Commercial
SY100S321JCTR	J28-1	Commercial

24 LEAD CERPACK (F24-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

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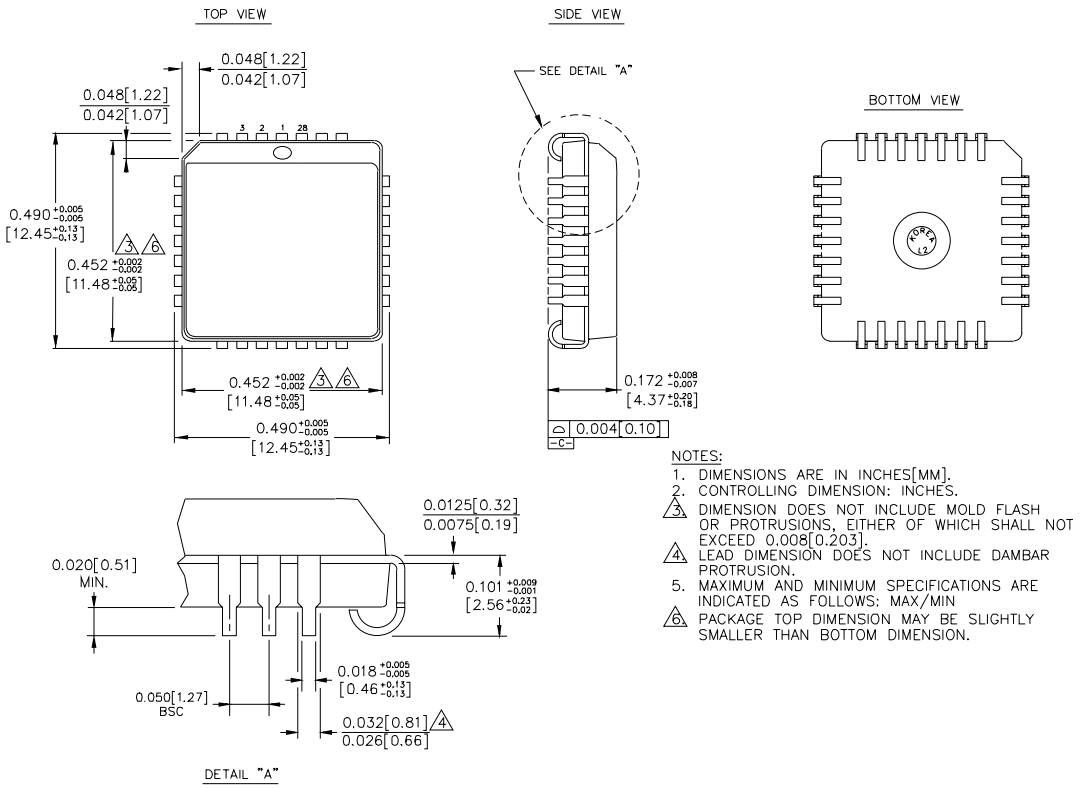
28 LEAD PLCC (J28-1)



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