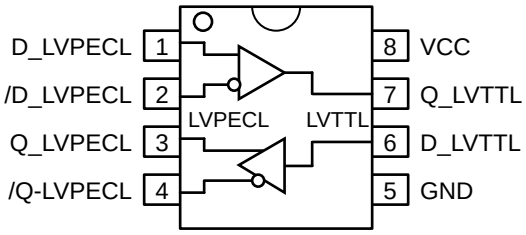
3V LVTTL-TO-DIFFERENTIAL LVPECL AND DIFFERENTIAL LVPECL-TO-LVTTL TRANSLATOR

FEATURES

- 3.3V ±10% power supply
- Guaranteed AC parameters over temperature: f_{MAX} > 275MHz (LVTTL)
- < 2ns LVPECL-to-LVTTL propagation delay
- < 600ps LVTTL-to-LVPECL propagation delay
- Internal 75kΩ input pull-down resistors
- Industrial temperature range: –40°C to +85°C
- Available in 8-pin MSOP and SOIC packages

ECL Pro™

PIN CONFIGURATION/BLOCK DIAGRAM



TOP VIEW
(Available in MSOP or SOIC package)

DESCRIPTION

The SY10/100EPT28L is a differential LVPECL-to-LVTTL translator and a LVTTL-to-differential LVPECL translator in a single package. Because LVPECL (Positive ECL) levels are used, only +3.3V and ground are required. The small outline 8-pin package and the dual translation design of the EPT28L makes it ideal for applications which are sending and receiving signals across a backplane.

The 100K series includes temperature compensation. Thus, logic levels are constant over temperature.

PIN NAMES

Pin	Function
D_LVTTL	Low Voltage TTL Input
Q_LVTTL	Low Voltage TTL Output
D_LVPECL /D_LVPECL	Low Voltage Differential PECL Inputs with 75kΩ internal pull-down
Q_LVPECL /Q_LVPECL	Low Voltage Differential PECL Outputs
V_{CC}	3.3V Positive Supply
GND	Ground

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{CC}	Power Supply Voltage		–0.5 to +3.8	V
V_{IN}	Input Voltage		0 to V_{CC}	V
I_{OUT}	LVPECL Output Current	–Continuous –Surge	50 100	mV
T_A	Operating Temperature Range		–40 to +85	°C
T_{store}	Storage Temperature Range		–65 to +150	°C
θ_{JA}	Package Thermal Resistance (Junction-to-Ambient)	–Still-Air (SOIC) –500lfpm (SOIC) –Still-Air (MSOP) –500lfpm (MSOP)	160 109 206 155	°C/W °C/W
θ_{JC}	Package Thermal Resistance (Junction-to-Case)	(SOIC) (MSOP)	39 39	°C/W

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS(1)

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	3.0	3.3	3.6	3.0	3.3	3.6	V	
I_{CC}	Power Supply Current	—	20	40	—	22	40	—	25	40	mA	

Note 1. 10/100KEPT circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

LVPECL DC ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 3.3V ±10%

Symbol	Parameter		T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{OH}	Output HIGH(2) Voltage	10EPT 100EPT	2165 2155	2290 2280	2415 2405	2230 2155	2355 2280	2480 2405	2290 2155	2415 2280	2540 2405	mV	
V_{OL}	Output LOW(2) Voltage	10EPT 100EPT	1365 1355	1490 1480	1615 1605	1430 1355	1555 1480	1680 1605	1490 1355	1615 1480	1740 1605	mV	
V_{IH}	Input HIGH(2) Voltage	10EPT 100EPT	2090 2075	— —	2415 2420	2155 2075	— —	2480 2420	2215 2075	— —	2540 2420	mV	
V_{IL}	Input LOW(2) Voltage	10EPT 100EPT	1365 1355	— —	1690 1675	1430 1355	— —	1755 1675	1490 1355	— —	1815 1675	mV	
I_{IH}	Input HIGH Current		—	—	150	—	—	150	—	—	150	µA	V_{IN} = 3.46V
I_{IL}	Input LOW Current	/D, D	0.5	—	0.5	—	—	0.5	—	—	0.5	µA	
C_{IN}	Input Capacitance	(SOIC) (MSOP)	— —	— —	— —	— —	0.75 1.1	— —	— —	— —	— —	pF pF	

Note 1. 10/100KEPT circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

Note 2. Input and output parameters vary 1:1 with V_{CC}.

LVTTL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 3.3V ±10%

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{OH}	Output HIGH Voltage	2.0	—	—	2.0	—	—	2.0	—	—	V	I_{OH} = –3mA
V_{OL}	Output LOW Voltage	—	—	0.5	—	—	0.5	—	—	0.5	V	I_{OH} = –24mA
V_{IH}	Input HIGH Voltage	2.0	—	—	2.0	—	—	2.0	—	—	V	
V_{IL}	Input LOW Voltage	—	—	0.8	—	—	0.8	—	—	0.8	V	
V_{IK}	Input Clamp Voltage	—	—	–1.2	—	—	–1.2	—	—	–1.2	V	I_{IK} = –18mA
I_{IH}	Input HIGH Current	—	—	20	—	—	20	—	—	20	µA	V_{IN} = 2.7V
		—	—	100	—	—	100	—	—	100	µA	V_{IN} = V_{CC}
I_{IL}	Input LOW Current	—	—	–0.2	—	—	–0.2	—	—	–0.2	µA	V_{IN} = 0.5V
$I_{OUT(SC)}$	LVTTL Output Short-Circuit Current	–275	—	–80	–275	—	–80	–275	—	–80	mA	V_{OUT} = 0V
C_{IN}	Input Capacitance (SOIC) (MSOP)	— —		— —	— —	0.75 1.1	— —	— —		— —	pF pF	

Note 1. 10/100KEPT circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±10%

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{MAX}	Maximum Frequency LVPECL LVTTL	 700 275	 — 350	 — —	 700 275	 — 350	 — —	 700 275	 — 350	 — —	 MHz MHz	Output Toggle Frequency
t_{PLH} t_{PHL}	Propagation Delay D_LVPECL → Q_LVTTL	1.5	—	2.5	1.5	—	2.5	1.5	—	2.5	ns	C_L = 20pF
	Q_LVTTL → D_LVPECL	100	400	600	100	400	600	100	400	600	ps	50Ω to V_{CC}–2.0
V_{CMR}	LVPECL Common Mode Range	1.2	—	V_{CC}	1.2	—	V_{CC}	1.2	—	V_{CC}	V	
V_{PP}	LVPECL Input Voltage Swing (Single-Ended)[1]	100	—	—	100	—	—	100	—	—	mV	
t_r, t_f	LVPECL Output Rise/Fall Times (20% to 80%)	200	—	500	200	—	500	200	—	500	ns	50Ω to V_{CC}–2.0
	LVTTL Output Rise/Fall Times (10% to 90%)	0.5	—	1.0	0.5	—	1.0	0.5	—	1.0	ns	C_L = 20pF
t_{DC}	Duty Cycle	45	50	55	45	50	55	45	50	55	%	
t_{JITTER}	Cycle-to-Cycle Jitter (rms)	—	0.2	< 1	—	0.2	< 1	—	0.2	< 1	ps	RMS

Note 1. V_{PP} (min) is the minimum input swing for which AC parameters are guaranteed.

TERMINATION RECOMMENDATIONS

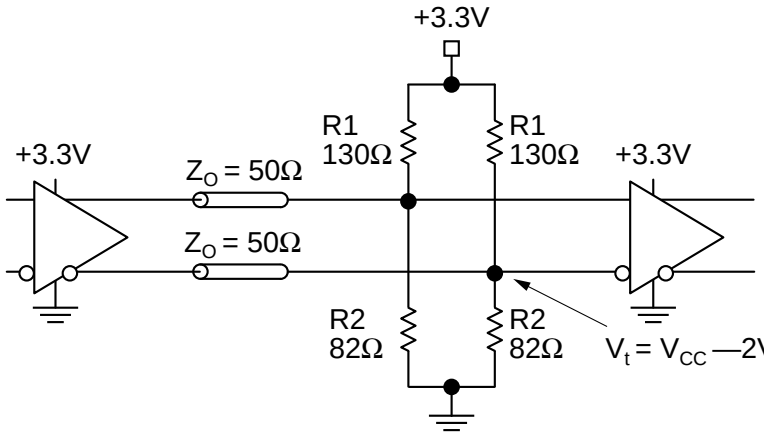


Figure 1. LVPECL Parallel Termination–Thevenin Equivalent

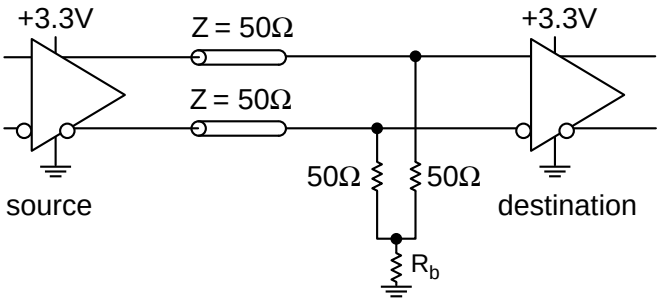


Figure 2. LVPECL Three-Resistor "Y–Termination"

Note 1. Power-saving alternative to 4-resistor, Thevenin termination.

Note 2. Place termination resistors as close to destination inputs as possible.

Note 3. R_b resistor sets the DC bias voltage, equal to V_t. For 3.3V supply, R_b value is between 46Ω to 50Ω.

PRODUCT ORDERING CODE

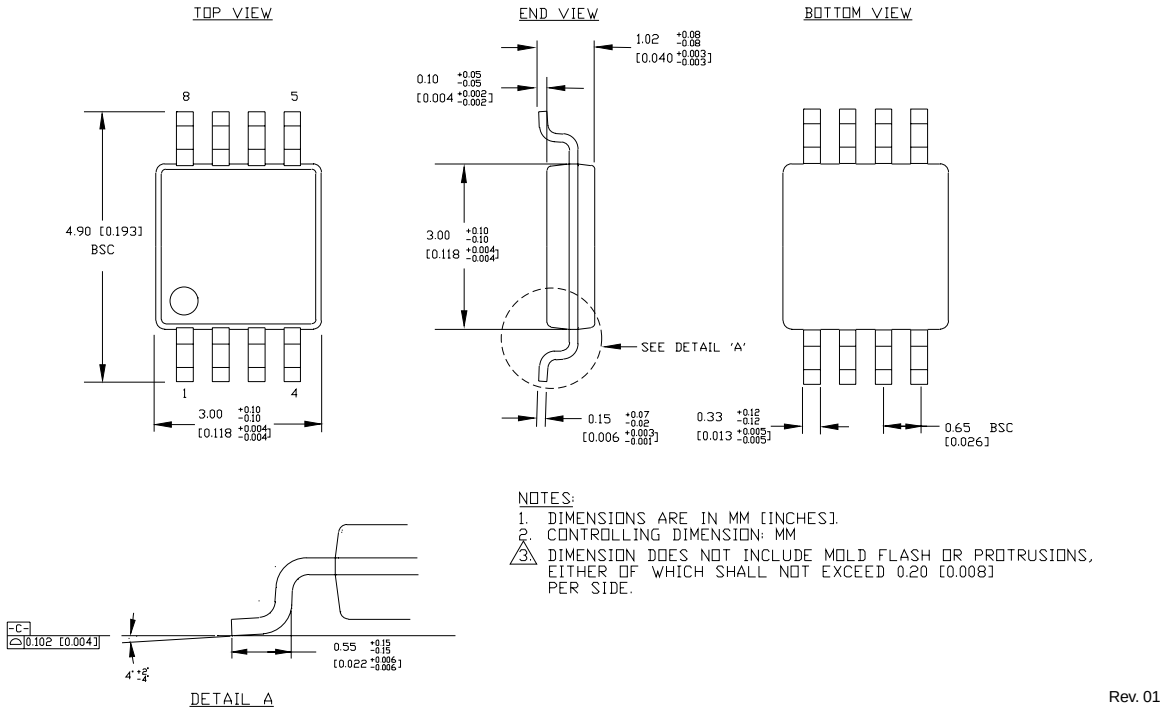
Ordering Code	Package Type	Operating Range	Package Marking
SY10EPT28LZC	Z8-1	Commercial	HEP28
SY10EPT28LZCTR(1)	Z8-1	Commercial	HEP28
SY100EPT28LZC	Z8-1	Commercial	XEP28
SY100EPT28LZCTR(1)	Z8-1	Commercial	XEP28
SY10EPT28LKC	K8-1	Commercial	HP28
SY10EPT28LKCTR(1)	K8-1	Commercial	HP28
SY100EPT28LKC	K8-1	Commercial	XP28
SY100EPT28LKCTR(1)	K8-1	Commercial	XP28

Ordering Code	Package Type	Operating Range	Package Marking
SY10EPT28LZI(2)	Z8-1	Industrial	HEP28
SY10EPT28LZITR(1, 2)	Z8-1	Industrial	HEP28
SY100EPT28LZI(2)	Z8-1	Industrial	XEP28
SY100EPT28LZITR(1, 2)	Z8-1	Industrial	XEP28
SY10EPT28LKI(2)	K8-1	Industrial	HP28
SY10EPT28LKITR(1, 2)	K8-1	Industrial	HP28
SY100EPT28LKI(2)	K8-1	Industrial	XP28
SY100EPT28LKITR(1, 2)	K8-1	Industrial	XP28

Note 1. Tape and Reel.

Note 2. Recommended for new designs.

8 LEAD MSOP (K8-1)



NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

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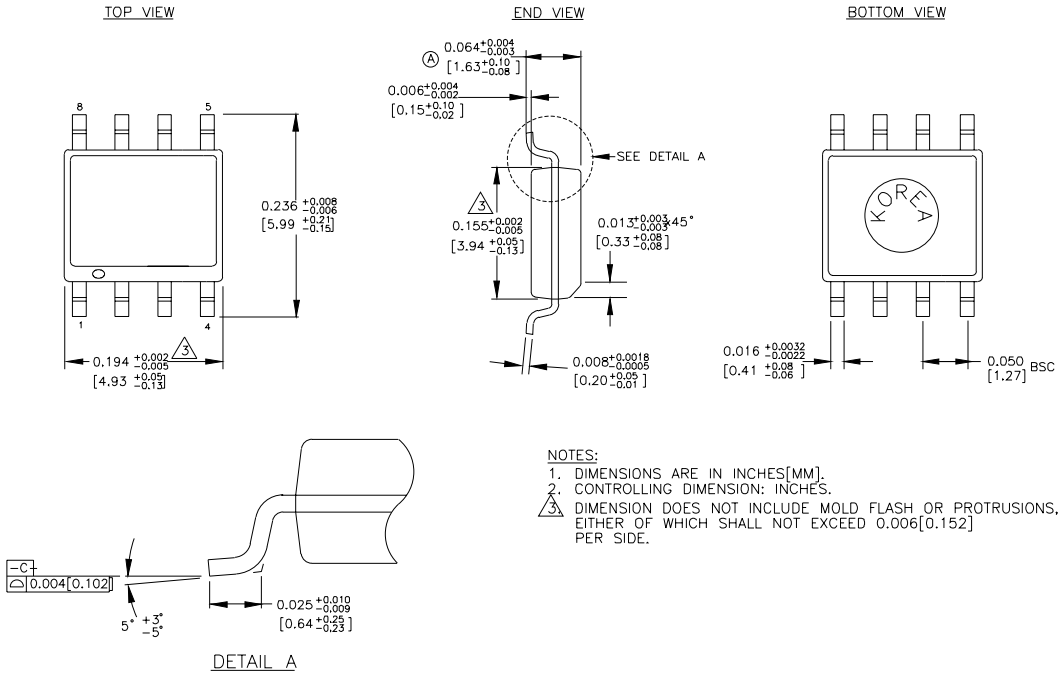
8 LEAD SOIC .150" WIDE (Z8-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.152] PER SIDE.

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