## FEATURES

- 2:1 PECL/ECL multiplexer
- Guaranteed AC–performance over temperature/voltage
  - >3GHz $f_{MAX}$ (toggle)
  - <200ps rise/fall time
  - <420ps propagation delay (D-to-Q)
- Low jitter performance
  - Random jitter: <1ps (rms)
  - Deterministic jitter: <15ps (pk-pk)
  - Total jitter (clock): <1ps (pk-pk)
- Flexible supply voltage: 3V to 5.5V
- Wide operating temperature range: –40°C to +85°C
- Available in 8-pin MSOP and SOIC packages

## APPLICATIONS

- SONET
- Gig Ethernet
- Fibre Channel
- Transponders

ECL Pro™

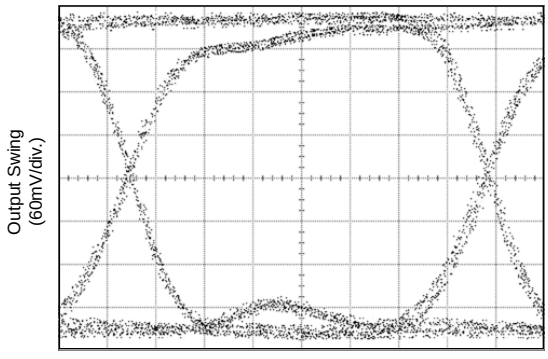
## DESCRIPTION

The SY10/100EP58V are 3.3V/5V, precision, high-speed, 2:1 multiplexers. Both devices are pin-for-pin, plug-in replacements for the MC10/100EP58D/DT in 8-pin SOIC and 6-pin TSSOP (MSOP) packages. The signal-path inputs (Da and Db) are single-ended PECL/ECL compatible, and can accept a signal swing as low as 150mV. All I/O pins are 10K/100K EP ECL/PECL compatible.

AC–performance is guaranteed over the industrial –40°C to +85°C temperature range and 3.0V to 5.5V supply voltage range. Maximum throughput ($f_{MAX}$) is guaranteed to be 3GHz with a differential output swing ≥400mV. In addition, these multiplexers are optimized for low-jitter applications. The SY10EP58V and SY100EP58V are designed to operate in either ECL/PECL or PECL/LVPECL mode. The SY100EP58V is internally temperature compensated, thus is 100K EP ECL/PECL compatible—I/O logic levels remain constant over temperature.

The SY10/100EP58V is part of Micrel's high-speed, Precision Edge timing and distribution family. For applications that require a differential I/O combination, consult the Micrel website at *www.micrel.com*, and choose from a comprehensive product line of high-speed, low skew fanout buffers, translators, and clock dividers.

## TYPICAL PERFORMANCE



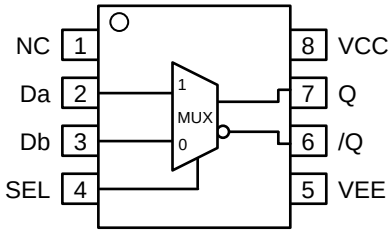

**2.7Gbps, $2^{23}$ – 1 PRBS**

## CROSS REFERENCE TABLE

| Micrel Semiconductor | On Semiconductor | Package |
|---|---|---|
| SY10EP58VZI | MC10EP58D | 8-pin SOIC |
| SY10EP58VZITR | MC10EP58DR2 | 8-pin SOIC TR* |
| SY10EP58VKI | MC10EP58DT | 8-pin MSOP/TSSOP |
| SY10EP58VKITR | MC10EP58DTR2 | 8-pin MSOP/TSSOP TR* |
| SY100EP58VZI | MC100EP58D | 8-pin SOIC |
| SY100EP58VZITR | MC100EP58DR2 | 8-pin SOIC TR* |
| SY100EP58VKI | MC100EP58DT | 8-pin MSOP/TSSOP |
| SY100EP58VKITR | MC100EP58DTR2 | 8-pin MSOP/TSSOP TR* |

*Tape and Reel

## PACKAGE/ORDERING INFORMATION




**8-Pin MSOP (K8-1)**
**8-Pin SOIC (Z8-1)**

### Ordering Information

| Part Number | Package Type | Operating Range | Package Marking |
|---|---|---|---|
| SY10EP58VZC | Z8-1 | Commercial | HEP58V |
| SY10EP58VZCTR[1] | Z8-1 | Commercial | HEP58V |
| SY100EP58VZC | Z8-1 | Commercial | EP58V |
| SY100EP58VZCTR[1] | Z8-1 | Commercial | EP58V |
| SY10EP58VKC | K8-1 | Commercial | HP58V |
| SY10EP58VKCTR[1] | K8-1 | Commercial | HP58V |
| SY100EP58VKC | K8-1 | Commercial | EP58V |
| SY100EP58VKCTR[1,2] | K8-1 | Commercial | EP58V |
| SY10EP58VZI[2] | Z8-1 | Industrial | HEP58V |
| SY10EP58VZITR[1,2] | Z8-1 | Industrial | HEP58V |
| SY100EP58VZI[2] | Z8-1 | Industrial | EP58V |
| SY100EP58VZITR[1,2] | Z8-1 | Industrial | EP58V |
| SY10EP58VKI[2] | K8-1 | Industrial | HP58V |
| SY10EP58VKITR[1,2] | K8-1 | Industrial | HP58V |
| SY100EP58VKI[2] | K8-1 | Industrial | EP58V |
| SY100EP58VKITR[1,2] | K8-1 | Industrial | EP58V |

**Note 1.** Tape and Reel.

**Note 2.** Recommended for new designs.

## PIN DESCRIPTION

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 1 | NC | No connect. |
| 2, 3 | Da, Db[1] | 100KEP PECL/ECL single-ended input channels a and b. Multiplexing of these inputs are controlled by SEL. The signal inputs include internal 75kΩ pull-down resistors. Default condition is LOW when left floating. The input signal should be terminated externally. See “Termination Recommendations” section. |
| 4 | SEL | 100KEP PECL/ECL compatible 2:1 mux select control. See “Mux Select Truth Table.” Enable pin includes an intenal 75kΩ pull-down resistor. Default condition is LOW. |
| 5 | VEE | Negative Power Supply: For PECL/LVPECL connect to ground. Both $V_{EE}$ pins must be connected together, externally on the PCB, for proper operation. |
| 6, 7 | /Q, Q | 100KEP PECL/ECL compatible differential output. PECL/ECL termination is with a 50Ω resistor to $V_{CC}$ –2V. Unused single-ended outputs must have a balanced load. For AC–coupled applications, the output stage emitter follower must have a DC current path to ground. See “Termination Recommendations” section. |
| 8 | VCC | Positive Power Supply. All $V_{CC}$ pins must be connected to the same power supply externally. Bypass with 0.1µF//0.01µF low ESR capacitors. |

**Note 1.** If the inputs are AC–coupled, teh outputs Q, and /Q will experience duty cycle distoration because the input levels do not track the internal reference voltage.

## MUX SELECT TRUTH TABLE

| SEL1 | DATA OUT |
|---|---|
| L | D0 |
| H | D1 |

## Absolute Maximum Ratings(Note 1)

Supply Voltage ($V_{IN}$) ..... –6.0V to 0V
Output Current ($I_{OUT}$)
  Continuous ..... 50mA
  Surge ..... 100mA
Storage Temperature ($T_S$) ..... –65°C to +150°C

**Note 1.** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

**Note 2.** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

## Operating Ratings(Note 2)

Supply Voltage $|V_{CC}–V_{EE}|$ ..... +3.0V to +5.5V
Ambient Temperature ($T_A$) ..... –40°C to +85°C
Package Thermal Resistance
  MSOP ($\theta_{JA}$)
    Still-air ..... 206°C/W
    500lfpm ..... 155°C/W
  SOIC ($\theta_{JA}$)
    Still-air ..... 160°C/W
    500lfpm ..... 109°C/W
  MSOP ($\theta_{JC}$) ..... 39°C/W
  SOIC ($\theta_{JC}$) ..... 39 °C/W

## DC ELECTRICAL CHARACTERISTICS(1)

| Symbol | Parameter | $T_A$ = –40°C | | | $T_A$ = +25°C | | | $T_A$ = +85°C | | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| $V_{CC}$ | Power Supply Voltage | | | | | | | | | | V | |
| | (PECL) | 4.5 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | | |
| | (LVPECL) | 3.0 | — | 3.8 | 3.0 | — | 3.8 | 3.0 | — | 3.8 | | |
| | (ECL) | –5.5 | –5.0 | –4.5 | –5.5 | –5.0 | –4.5 | –5.5 | –5.0 | –4.5 | | |
| | (LVECL) | –3.8 | –3.3 | –3.0 | –3.8 | –3.3 | –3.0 | –3.8 | –3.3 | –3.0 | | |
| $I_{EE}$ | Supply Current | — | 35 | 50 | — | 35 | 50 | — | 35 | 50 | mA | No Load |
| $I_{IH}$ | Input HIGH Current | — | — | 75 | — | — | 75 | — | — | 80 | µA | $V_{IN} = V_{IH}$ |
| $I_{IL}$ | Input LOW Current | | | | | | | | | | | |
| | All Inputs | 0.5 | — | — | 0.5 | — | — | 0.5 | — | — | µA | $V_{IN} = V_{IL}$ |
| $C_{IN}$ | Input Capacitance (MSOP) | — | — | — | — | 1.0 | — | — | — | — | pF | |
| | (SOIC) | — | — | — | — | 1.0 | — | — | — | — | pF | |

**Note 1.** 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

## 10K DC ELECTRICAL CHARACTERISTICS(1)

$V_{CC}$ = 3.0V to 5.5V; $V_{EE}$ = 0V(2) $V_{CC}$ = 0V or $V_{EE}$ = –5.5V to –3.0V

| Symbol | Parameter | $T_A$ = –40°C | | | $T_A$ = +25°C | | | $T_A$ = +85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $I_{EE}$ | Power Supply Current(3) | — | — | 40 | — | 30 | 40 | — | — | 40 | mA |
| $V_{OH}$ | Output HIGH Voltage(4) | –1135 | — | –0885 | –1070 | –0945 | –0820 | –1010 | — | –0760 | mV |
| $V_{OL}$ | Output LOW Voltage(4) | –1935 | — | –1685 | –1870 | –1745 | –1620 | –1810 | — | –1560 | mV |
| $V_{IH}$ | Input HIGH Voltage | –1210 | — | –0885 | –1145 | — | –0820 | –1085 | — | –0760 | mV |
| $V_{IL}$ | Input LOW Voltage | –1935 | — | –1610 | –1870 | — | –1545 | –1810 | — | –1485 | mV |
| $I_{IH}$ | Input HIGH Current | — | — | 150 | — | — | 150 | — | — | 150 | µA |
| $I_{IL}$ | Input LOW Current D | 0.5 | — | — | 0.5 | — | — | 0.5 | — | — | µA |

**Note 1.** 10KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

**Note 2.** Input and output parameters vary 1:1 with $V_{CC}$.

**Note 3.** $V_{CC}$ = 0V, $V_{EE}$ = $V_{EE}$(min) to $V_{EE}$(max), all other pins floating.

**Note 4.** All loading with 50Ω to $V_{CC}$ – 2.0V.

## (100KEP) LVPECL DC ELECTRICAL CHARACTERISTICS[1]

$V_{CC}$ = 3.3V ±10%, $V_{EE}$ = 0V

| Symbol | Parameter | $T_A$ = –40°C | | | $T_A$ = +25°C | | | $T_A$ = +85°C | | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | 1355 | — | 1675 | 1355 | — | 1675 | 1355 | — | 1675 | mV | |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 2075 | — | 2420 | 2075 | — | 2420 | 2075 | — | 2420 | mV | |
| $V_{OL}$ | Outuput LOW Voltage | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV | 50Ω to $V_{CC}$–2V |
| $V_{OH}$ | Output HIGH Voltage | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV | 50Ω to $V_{CC}$–2V |
| $V_{BB}$ | Output Reference Voltage | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | mV | |
| $V_{IHCMR}$ | Input HIGH Voltage[2] Common Mode Range | 2.0 | — | $V_{CC}$ | 2.0 | — | $V_{CC}$ | 2.0 | — | $V_{CC}$ | V | |

**Note 1.** 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters are at $V_{CC}$ = 3.3V. They vary 1:1 with $V_{CC}$.

**Note 2.** The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

## (100KEP) PECL DC ELECTRICAL CHARACTERISTICS[1]

$V_{CC}$ = 5.0V ±10%, $V_{EE}$ = 0V

| Symbol | Parameter | $T_A$ = –40°C | | | $T_A$ = +25°C | | | $T_A$ = +85°C | | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | 3055 | — | 3375 | 3055 | — | 3375 | 3055 | — | 3375 | mV | |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 3775 | — | 4120 | 3775 | — | 4120 | 3775 | — | 4120 | mV | |
| $V_{OL}$ | Outuput LOW Voltage | 3055 | 3180 | 3305 | 3055 | 3180 | 3305 | 3055 | 3180 | 3305 | mV | 50Ω to $V_{CC}$–2V |
| $V_{OH}$ | Output HIGH Voltage | 3855 | 3980 | 4105 | 3855 | 3980 | 4105 | 3855 | 3980 | 4105 | mV | 50Ω to $V_{CC}$–2V |
| $V_{BB}$ | Output Reference Voltage | 3475 | 3575 | 3675 | 3475 | 3575 | 3675 | 3475 | 3575 | 3675 | mV | |
| $V_{IHCMR}$ | Input HIGH Voltage[2] Common Mode Range | 2.0 | — | $V_{CC}$ | 2.0 | — | $V_{CC}$ | 2.0 | — | $V_{CC}$ | V | |

**Note 1.** 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters are at $V_{CC}$ = 5.0V. They vary 1:1 with $V_{CC}$.

**Note 2.** The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

## (100KEP) ECL/LVECL DC ELECTRICAL CHARACTERISTICS[1]

$V_{CC}$ = 0V, $V_{EE}$ = –5.5V to –3.0V

| Symbol | Parameter | $T_A$ = –40°C | | | $T_A$ = +25°C | | | $T_A$ = +85°C | | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| $V_{IL}$ | Input LOW Voltage | –1945 | — | –1625 | –1945 | — | –1625 | –1945 | — | –1625 | mV | |
| $V_{IH}$ | Input HIGH Voltage | –1225 | — | –880 | –1225 | — | –880 | –1225 | — | –880 | mV | |
| $V_{OL}$ | Outuput LOW Voltage | –1945 | –1820 | –1695 | –1945 | –1820 | –1695 | –1945 | –1820 | –1695 | mV | 50Ω to $V_{CC}$–2V |
| $V_{OH}$ | Output HIGH Voltage | –1145 | –1020 | –895 | –1145 | –1020 | –895 | –1145 | –1020 | –895 | mV | 50Ω to $V_{CC}$–2V |
| $V_{BB}$ | Output Reference Voltage | –1525 | –1425 | –1325 | –1525 | –1425 | –1325 | –1525 | –1425 | –1325 | mV | |
| $V_{IHCMR}$ | Input HIGH Voltage[2] Common Mode Range | $V_{EE}$ +2.0 | | 0.0 | $V_{EE}$ +2.0 | | 0.0 | $V_{EE}$ +2.0 | | 0.0 | V | |

**Note 1.** 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

**Note 2.** The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

## AC ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 3.0V to 5.5V, $V_{EE}$ = 0V or $V_{CC}$ = 0V; $V_{EE}$ = –3.0V to –5.5V

| Symbol | Parameter | $T_A$ = –40°C | | | $T_A$ = +25°C | | | $T_A$ = +85°C | | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| $f_{MAX}$ | Max. Toggle Frequency[1] | 3 | — | — | 3 | — | — | 3 | — | — | GHz | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay (Differential) SEL to Q, /Q; D to Q, /Q | 170 | — | 380 | 190 | 230 | 410 | 210 | — | 420 | ps | |
| $t_{SKEW}$ | Part-to-Part Skew[2] | — | — | 200 | — | — | 200 | — | — | 200 | ps | |
| $t_{JITTER}$ | Cycle-to-Cycle Jitter (rms)[3] | — | 0.2 | <1 | — | 0.2 | <1 | — | 0.2 | <1 | $ps_{pk-pk}$ | |
| | Random Jitter[4] | — | — | — | — | — | <1 | — | — | — | $ps_{pk-pk}$ | Note 3 |
| | Deterministic Jitter[5] @1.25Gbps<br>@2.5Gbps | —<br>— | —<br>— | —<br>— | —<br>— | 7<br>10 | <15<br><25 | —<br>— | —<br>— | —<br>— | $ps_{pk-pk}$ | Note 4 |
| | Total Jitter[6] | — | <1 | — | — | <1 | — | — | <1 | — | $ps_{pk-pk}$ | |
| $V_{IN}$ | Differential Input Voltage Range | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV | |
| $t_r$, $t_f$ | Output Rise/Fall Time Q, /Q (20% to 80%) | — | — | 170 | — | 140 | 180 | — | — | 200 | ps | |

**Note 1.** Measured with 750mV input signal, 50% duty cycle. Output swing ≥ 400mV. All loading with a 50Ω to $V_{CC}$ –2.0V.

**Note 2.** Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

**Note 3.** The variation in period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER\_CC} = t_n - t_n + 1$, where t is the time between rising edges of the output signal.

**Note 4.** RJ is measured with a K28.7 comma detect character pattern, measured at 1.25Gbps and 2.5Gbps.

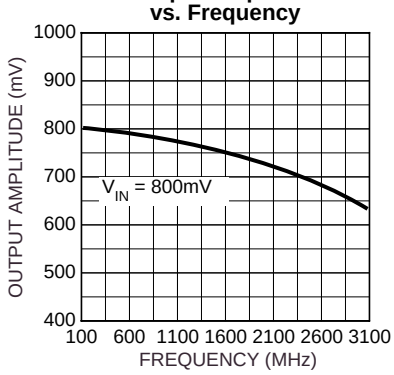
**Note 5.** DJ is measured at 1.25Gbps and 2.5Gbps, with both K28.5 and $2^{23}$–1 PRBS pattern.

**Note 6.** Total Jitter is defined as an ideal clock input, no more than 1 output edge in $10^{12}$ output edges will deviate by more than specifed peak-to-peak jitter value.

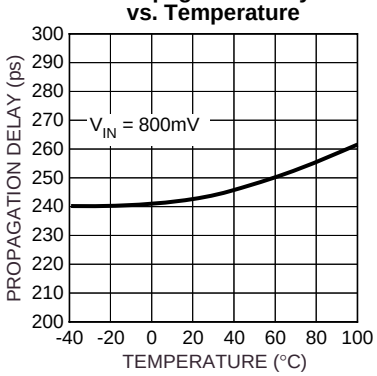
## TYPICAL OPERATING CHARACTERISTICS

(Conditions: $V_{CC}$ = 3.3V, $V_{EE}$ = GND, $T_A$ = 25°C, unless otherwise stated.)

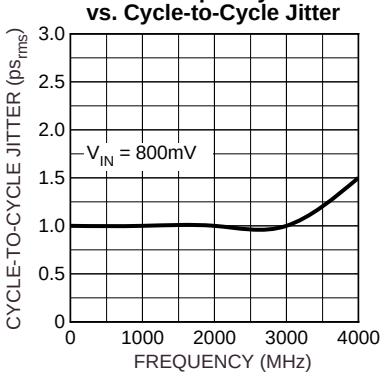
**Output Amplitude vs. Frequency**



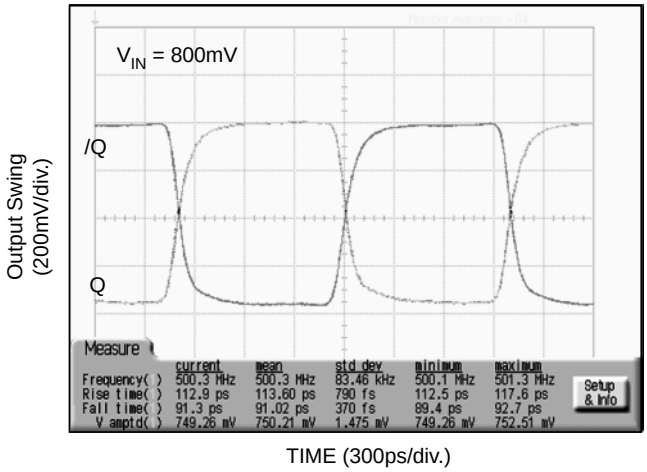

**Propagation Delay vs. Temperature**




**Frequency vs. Cycle-to-Cycle Jitter**

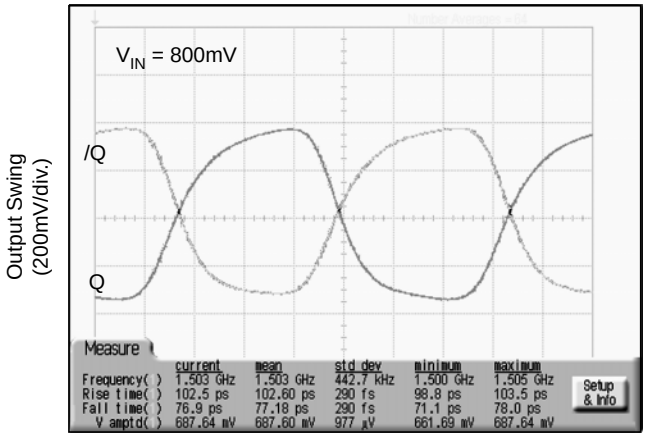



**500MHz Output**



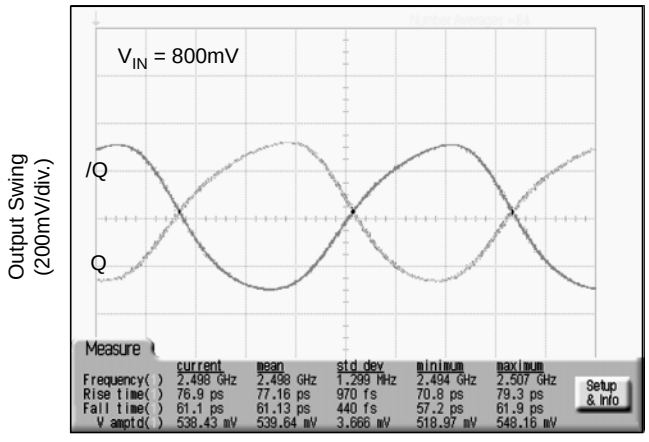

TIME (300ps/div.)

**1.5GHz Output**



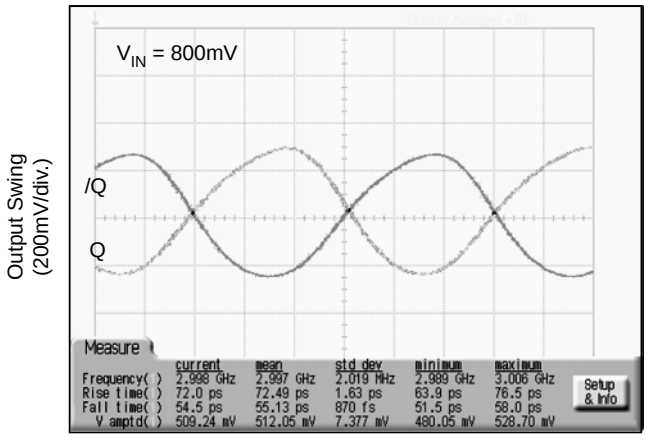

TIME (100ps/div.)

**2.5GHz Output**




TIME (60ps/div.)

**3.0GHz Output**




TIME (55ps/div.)

## TERMINATION RECOMMENDATIONS

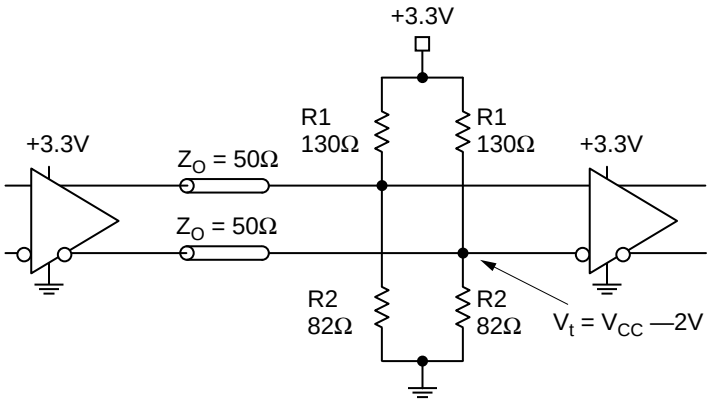



**Figure 1. Parallel Termination–Thevenin Equivalent**

**Note 1.** For +5.0V systems: R1 = 82Ω, R2 = 130Ω

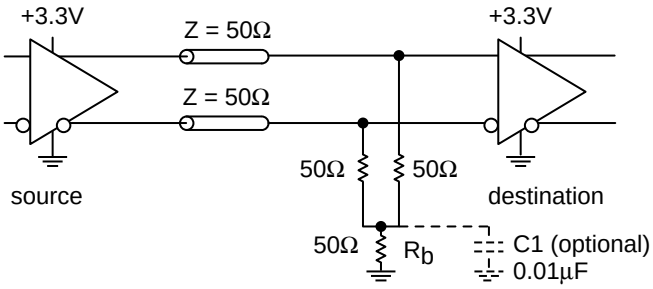


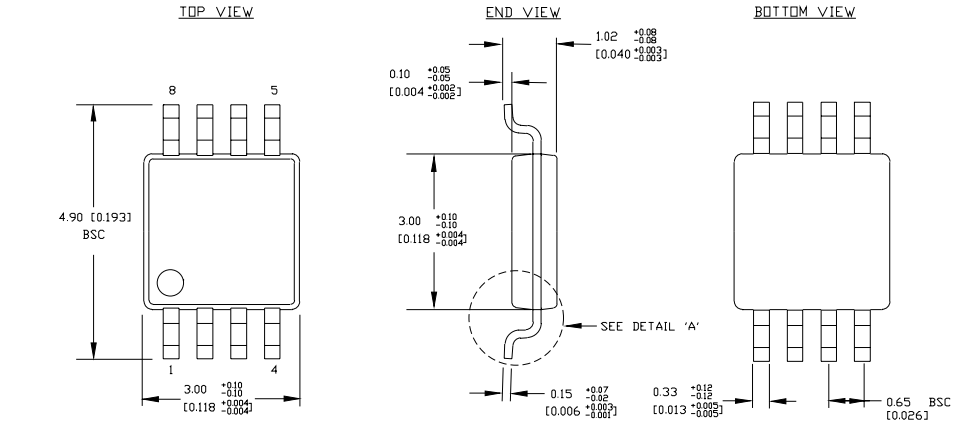

**Figure 2. Three-Resistor "Y–Termination"**

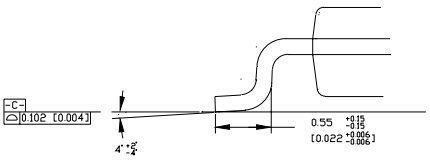
**Note 1.** Power-saving alternative to Thevenin termination.

**Note 2.** Place termination resistors as close to destination inputs as possible.

**Note 3.** $R_b$ resistor sets the DC bias voltage, equal to $V_t$. For +3.3V systems $R_b$ = 46Ω to 50Ω. For +5V systems, $R_b$ = 110Ω.

# 8 LEAD MSOP (K8-1)



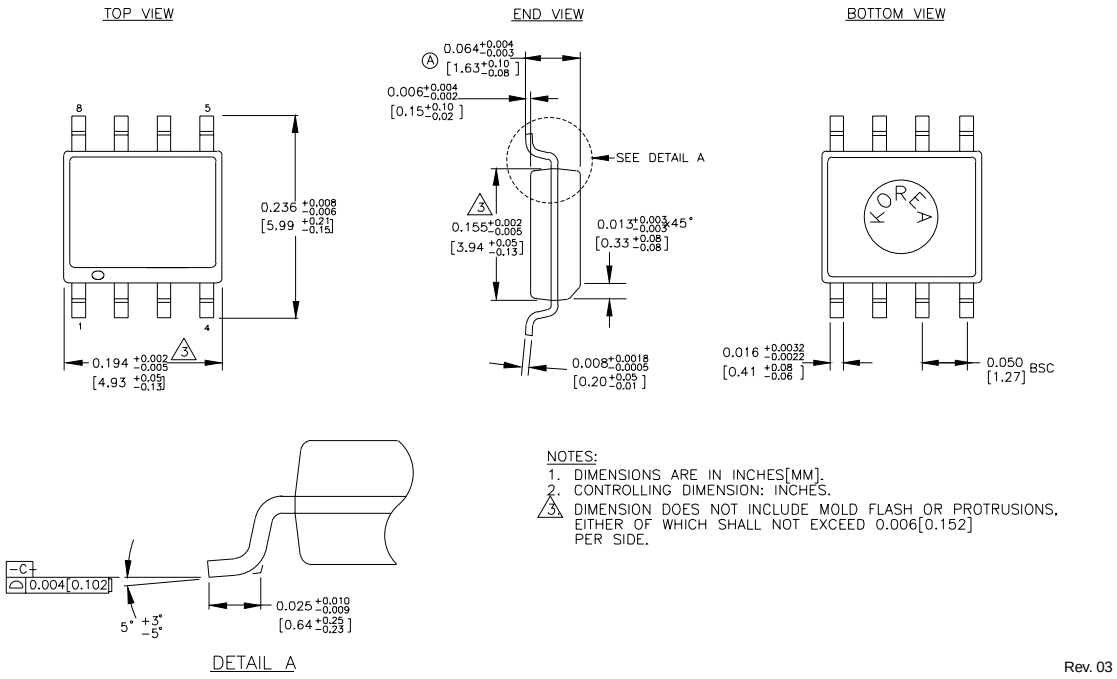




DETAIL A

NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

Rev. 01

## 8 LEAD SOIC (Z8-1)




Rev. 03

**MICREL, INC. 1849 FORTUNE DRIVE SAN JOSE, CA 95131 USA**

TEL + 1 (408) 944-0800 FAX + 1 (408) 944-0970 WEB http://www.micrel.com