6GHz, 1:6 400mV LVPECL FANOUT BUFFER w/2:1 MUX INPUT and INTERNAL TERMINATION

Precision Edge™
SY58036U

FEATURES

- Provides six ultra-low skew copies of the selected input
- 2:1 MUX input included for clock switchover applications
- Guaranteed AC performance over temperature and voltage:
  - Clock frequency range: DC to > 6GHz
  - < 270ps IN-to-OUT t_{pd}
  - < 80ps t_r / t_f times
  - < 20ps skew (output-to-output)
- Ultra-low jitter design:
  - < $1ps_{rms}$ random jitter
  - < $10ps_{p-p}$ total jitter (clock)
  - < $1ps_{rms}$ cycle-to-cycle jitter
  - < $0.7ps_{rms}$ crosstalk-induced jitter
- Low supply voltage operation: 2.5V and 3.3V
- Unique input termination and V_T pin accepts DC-coupled and AC-coupled inputs (CML, PECL, LVDS)
- Unique input isolation design minimizes crosstalk
- 400mV LVPECL (100k compatible) output swing
- –40°C to +85°C temperature range
- Available in 32-pin (5mm × 5mm) MLF™ package

APPLICATIONS

- Redundant clock distribution
- All SONET/SDH clock distribution
- All Fibre Channel distribution
- All Gigabit Ethernet clock distribution

Precision Edge™

DESCRIPTION

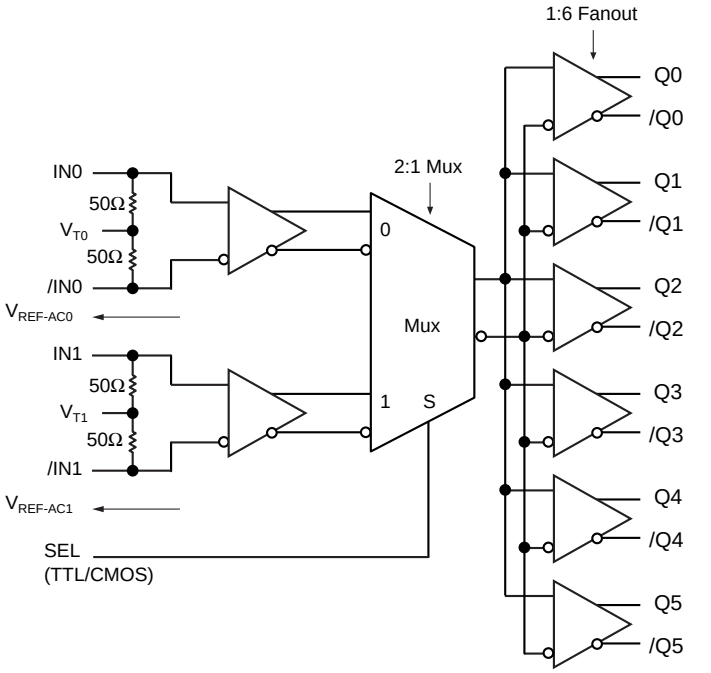
The SY58036U is a 2.5V/3.3V precision, high-speed, 1:6 fanout buffer capable of handling clocks up to 6GHz. A differential 2:1 MUX input is included for redundant clock switchover applications.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows the device to interface to any differential signal (AC- or DC-coupled) as small as 100mV without any level shifting or termination resistor networks in the signal path. The outputs are 400mV LVPECL (100k temperature compensated), with extremely fast rise/fall times guaranteed to be less than 80ps.

The SY58036U operates from a 2.5V ±5% supply or a 3.3V ±10% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. For applications that require CML outputs, consider the SY58034U or for 800mV LVPECL outputs the SY58035U. The SY58036U is part of Micrel's high-speed, Precision Edge™ product line.

All support documentation can be found on Micrel's web site at www.micrel.com.

FUNCTIONAL BLOCK DIAGRAM



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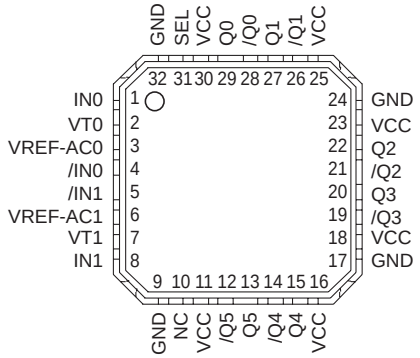
MLF and *Micro*LeadFrame are trademarks of Amkor Technology, Inc.

PACKAGE/ORDERING INFORMATION



32-Pin MLF™

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking
SY58036UMI	MLF-32	Industrial	SY58036U
SY58036UMITR[2]	MLF-32	Industrial	SY58036U

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1, 4 8, 5	IN0, /IN0 IN1, /IN1	Differential Input: This input pairs are the differential signal inputs to the device. These inputs accept AC- or DC-coupled signals as small as 100mV. Each pin of a pair internally terminates to a V_T pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Please refer to the *"Input Interface Applications"* section for more details.
2, 7	VT0, VT1	Input Termination Center-Tap: Each side of the differential input pair terminates to a V_T pin. The V_{T0} and V_{T1} pins provide a center-tap to a termination network for maximum interface flexibility. See *"Input Interface Applications"* section for more details.
31	SEL	This single-ended TTL/CMOS compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. The MUX select switchover function is asynchronous. Switching must occur within setup/hold time in order to prevent short cycles.
10	NC	No connect.
11, 16, 18, 23, 25, 30	VCC	Positive Power Supply: Bypass with 0.1µF||0.01µF low ESR capacitors.
29, 28 27, 26 22, 21 20, 19 15, 14 13, 12	Q0, /Q0, Q1, /Q1, Q2, /Q2, Q3, /Q3, Q4, /Q4, Q5, /Q5	Differential Outputs: These 100k (temperature compensated) LVPECL output pairs are low skew copies of the selected input. Unused output pins may be left floating. Please refer to the *"Truth Table"* for details.
9, 17, 24, 32	GND, Exposed Pad	Ground. Ground pin and exposed pad must be connected to the same ground plane.
3, 6	VREF-AC0 VREF-AC1	Reference Voltage: This output biases to V_{CC}–1.2V. It is used for AC-coupling inputs (IN, /IN). Connect V_{REF-AC} directly to the V_T pin. Bypass with 0.01µF low ESR capacitor to V_{CC}. See *"Input Interface Applications"* section. Maximum sink/source is ±0.5mA.

TRUTH TABLE

SEL	
0	IN0 Input Selected
1	IN1 Input Selected

Absolute Maximum Ratings[1]

Power Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Termination Current[3]
  Source or sink current on V_T pin ..... ±100mA
Input Current
  Source or sink current on IN, /IN pin ..... ±50mA
Lead Temperature (soldering, 10 sec.) ..... 220°C
Storage Temperature Range (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Power Supply Voltage (V_{CC}) ..... +2.375V to +2.625V
  ..... +3.0V to +3.6V
Ambient Temperature Range (T_A) ..... –40°C to +85°C
Package Thermal Resistance[4]
  MLF™ (θ_{JA})
    Still-Air ..... 35°C/W
    500lpfm ..... 28°C/W
  MLF™ (ψ_{JB})
    Junction-to-Board ..... 20°C/W

DC ELECTRICAL CHARACTERISTICS[5]

T_A= –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	V_{CC} = 2.5V	2.375	2.5	2.625	V
		V_{CC} = 3.3V	3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}		125	250	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		80	100	120	Ω
R_{IN}	Input Resistance (IN-to-/IN)		40	50	60	Ω
V_{IH}	Input HIGH Voltage (IN-to-/IN)	**Note 6**	V_{CC}–1.6		V_{CC}	V
V_{IL}	Input LOW Voltage (IN-to-/IN)		0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN-to-/IN)	See Figure 1a	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing (IN-to-/IN)	See Figure 1b	0.2			V
V_T IN	IN to V_T (IN-to-/IN)				1.28	V
V_{REF-AC}	Reference Voltage		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V

Notes:

1. Permanent device damage may occur if *"Absolute Maximum Ratings"* are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to *"Absolute Maximum Ratings"* conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability, use for input of the same package only.
4. Thermal performance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. Ψ_{JB} uses 4-layer θ_{JA} in still-air number unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. V_{IH} (min), not lower than 1.2V.

LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS[7]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to +85°C; R_L = 50Ω to V_{CC}–2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage		V_{CC}–1.145		V_{CC}–0.895	V
V_{OL}	Output LOW Voltage		V_{CC}–1.545		V_{CC}–1.295	V
V_{OUT}	Output Differential Swing	See Figure 1a	150	400		mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 1b	300	800		mV

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS[7]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current				40	µA
I_{IL}	Input LOW Current				–300	µA

Note:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS[8]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to +85°C, R_L = 50Ω to V_{CC}–2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	$V_{OUT} \geq$ 200mV	6	7		GHz
t_{pd}	Differential Propagation Delay (IN0 or IN1-to-Q)		150	220	300	ps
	(SEL-to-Q)		100	220	400	ps
Δt_{pd} Tempco	Differential Propagation Delay Temperature Coefficient			65		fs/°C
t_{SKEW}	Output-to-Output	**Note 9**			20	ps
	Part-to-Part	**Note 10**			100	ps
t_{JITTER}	Clock Cycle-to-Cycle Jitter	**Note 11**			1	ps_{rms}
	Random Jitter (RJ)	**Note 12**			1	ps_{rms}
	Total Jitter (TJ)	**Note 13**			10	ps_{p-p}
	Adjacent Channel Crosstalk-Induced Jitter	**Note 14**			0.7	ps_{rms}
t_r, t_f	Output Rise/Fall Time	Full Swing, 20% to 80%	20	40	80	ps

Notes:

8. High frequency AC electricals are guaranteed by design and characterization.
9. Output-to-output skew is measured between outputs under identical input conditions.
10. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
11. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, T_n–T_{n-1} where T is the time between rising edges of the output signal.
12. Random jitter is measured with a K28.7 comma detect character pattern, measured at 2.5Gbps to 3.2Gbps.
13. Total jitter definition: with an ideal clock input of frequency ≤ f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
14. Crosstalk is measured at the output while applying two similar clock frequencies that are asynchronous with respect to each other at the inputs.

SINGLE-ENDED AND DIFFERENTIAL SWINGS

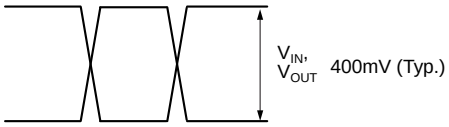


Figure 1a. Single-Ended Voltage Swing

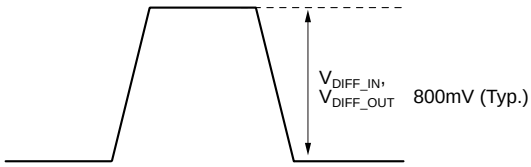
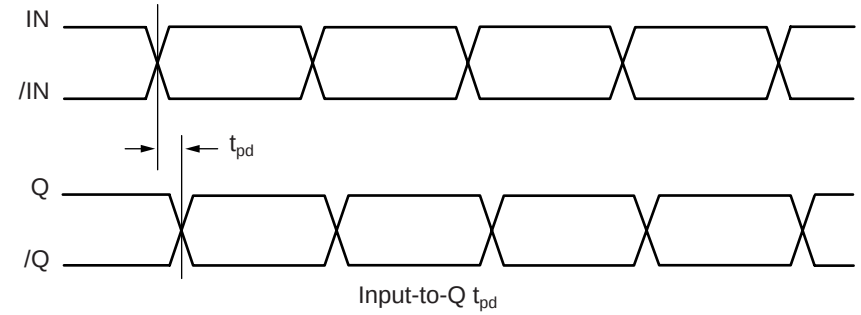
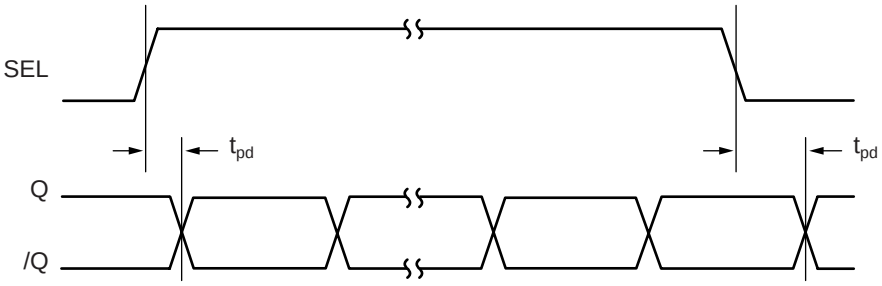


Figure 1b. Differential Voltage Swing

TIMING DIAGRAMS



Input-to-Q t_{pd}

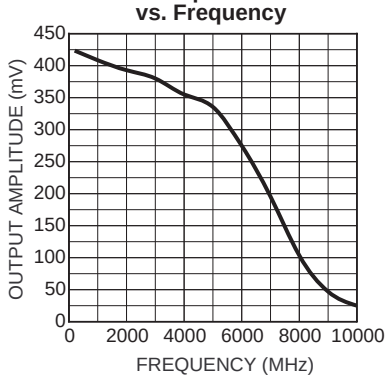


Select-to-Q t_{pd}

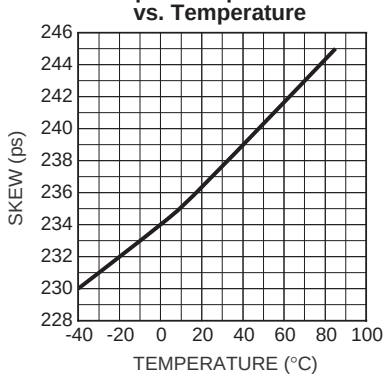
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 2.5V, GND = 0, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.

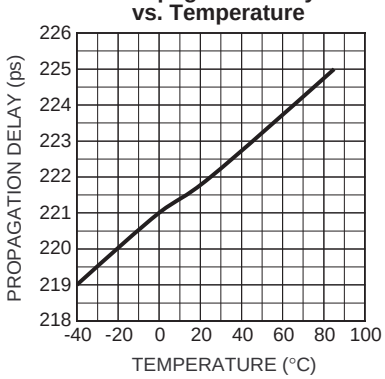
Amplitude vs. Frequency



Input-to-Input Skew vs. Temperature



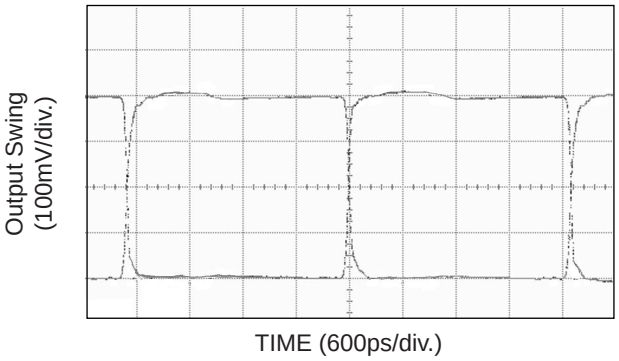
Propagation Delay vs. Temperature



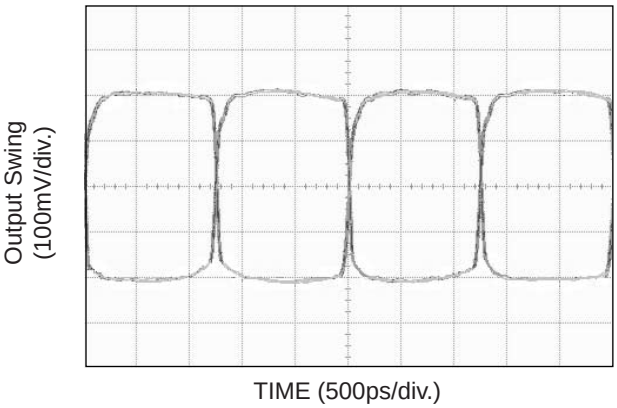
FUNCTIONAL CHARACTERISTICS

V_{CC} = 3.3V, GND = 0, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.

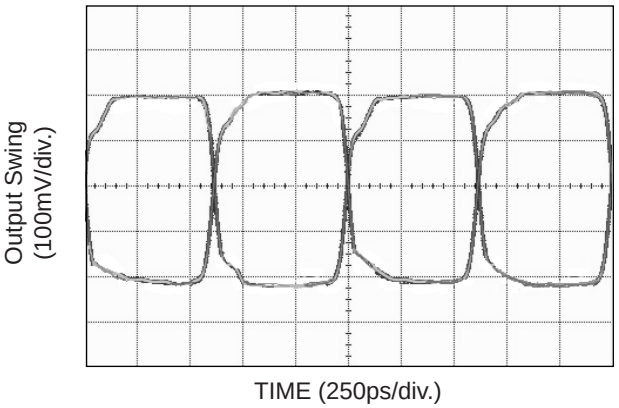
200MHz Output



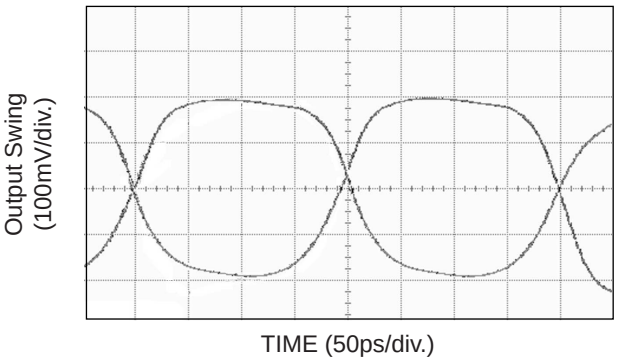
400MHz Output



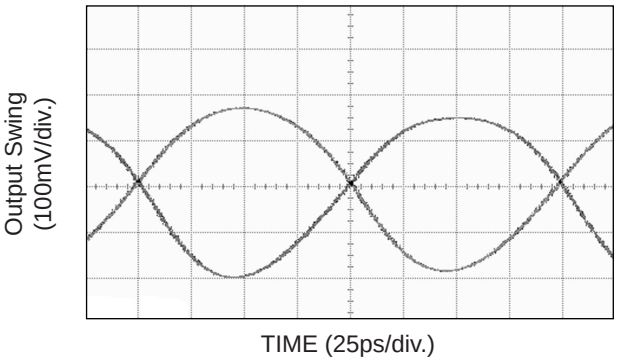
800MHz Output



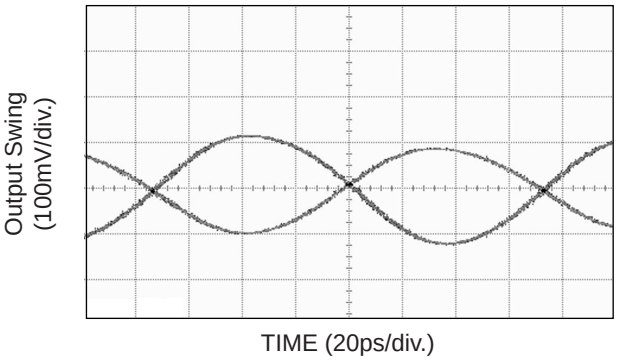
2.5GHz Output



5GHz Output



7GHz Output



INPUT AND OUTPUT STAGES

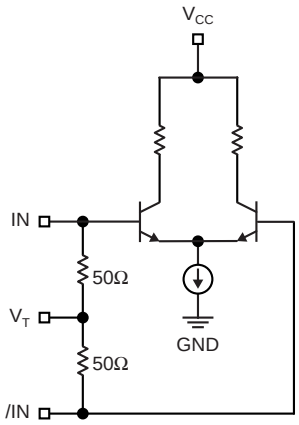


Figure 2a. Simplified Differential Input Stage

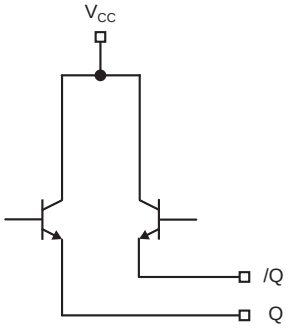


Figure 2b. Simplified LVPECL Output Stage

INPUT INTERFACE APPLICATIONS

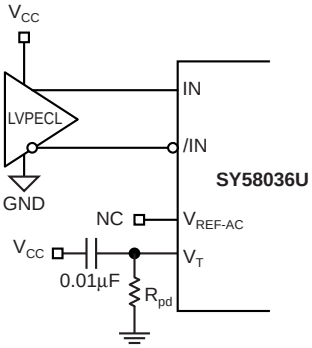


Figure 3a. LVPECL Interface (DC-Coupled)

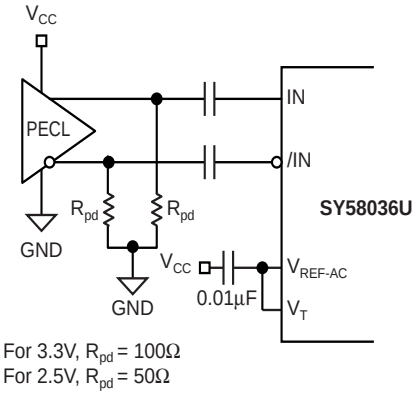


Figure 3b. LVPECL Interface (AC-Coupled)

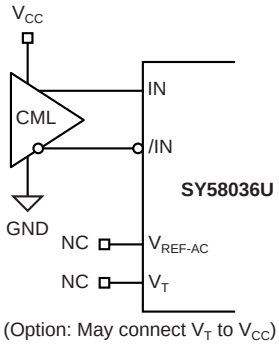


Figure 3c. CML Interface (DC-Coupled)

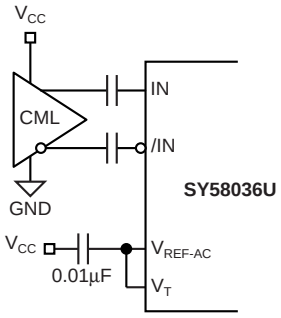


Figure 3d. CML Interface (AC-Coupled)

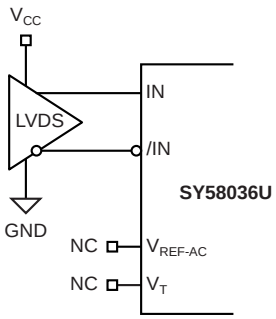


Figure 3e. LVDS Interface

OUTPUT INTERFACE APPLICATIONS

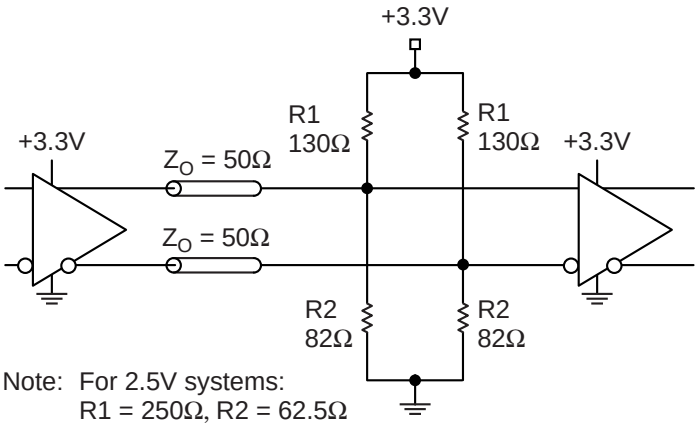


Figure 4a. Parallel Thevenin-Equivalent Termination

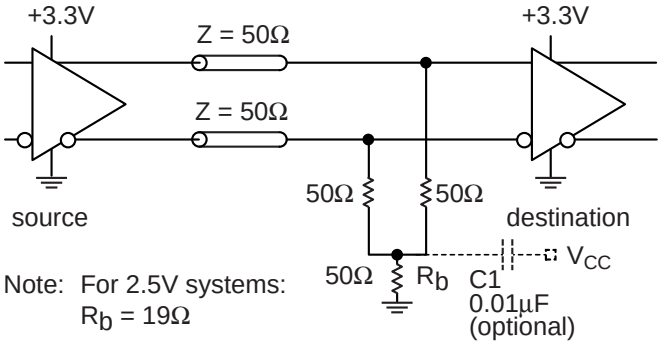
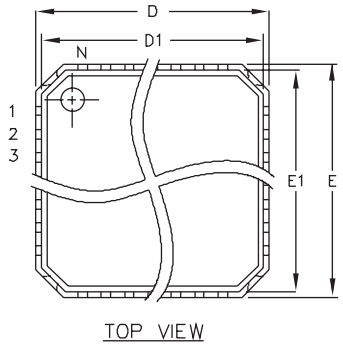


Figure 4b. Parallel Termination (3-Resistor)

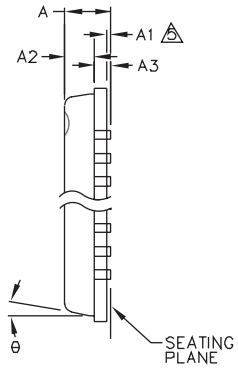
RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY58034U	6GHz, 1:6 CML Fanout Buffer w/2:1 MUX Input and Internal I/O Termination	http://www.micrel.com/product-info/products/sy58034u.shtml
SY58035U	4.5GHz, 1:6 LVPECL Fanout Buffer w/2:1 MUX Input and Internal Termination	http://www.micrel.com/product-info/products/sy58035u.shtml
SY58036U	6GHz, 1:6 400mV LVPECL Fanout Buffer w/2:1 MUX Input and Internal Termination	http://www.micrel.com/product-info/products/sy58036u.shtml
	MLF™ Application Note	www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

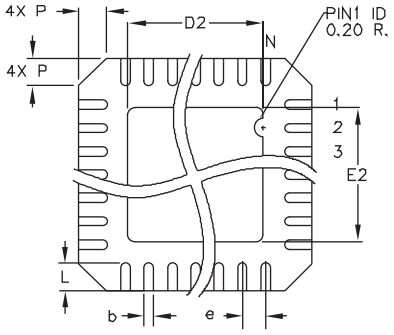
32 LEAD *Micro*LeadFrame™ (MLF-32)



TOP VIEW



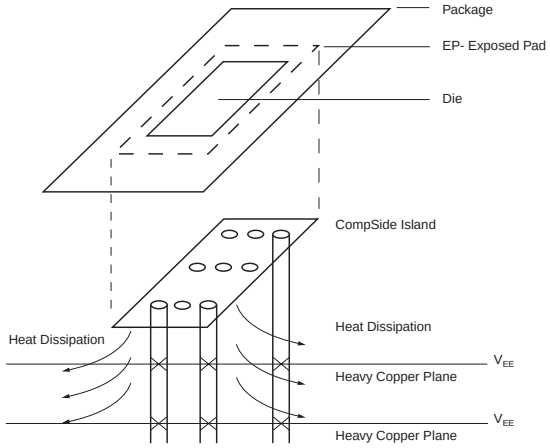
	DIMENSION (mm)	
	MIN.	MAX.
A	–	0.90
A1	0.00	0.05
A2	–	0.70
A3	0.20 REF.	
D	5.00 BSC	
D1	4.75 BSC	
D2	2.95	3.45
E	5.00 BSC	
E1	4.75 BSC	
E2	2.95	3.45
θ		12°
P	0.24	0.60
e	0.50 BSC	
N	32	
L	0.30	0.50
b	0.18	0.30



BOTTOM VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE NUMBER OF TERMINALS.
   THE NUMBER OF TERMINALS PER SIDE IS N/4.
3. THE PIN#1 IDENTIFIRE MUST BE EXISTED ON THE TOP SURFACE OF PACKAGE BY USING IDENTIFICATION MARK OR OTHER FEATURE OF PACKAGE BODY.
4. PACKAGE WARPAGE MAX 0.05mm.
5. APPLIED FOR EXPOSED PAD AND TERMINALS.

Rev. 01



PCB Thermal Consideration for 32-Pin MLF™ Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

MICREL, INC. 1849 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 944-0970 WEB http://www.micrel.com