# ULTRA-PRECISION CML DATA AND CLOCK SYNCHRONIZER W/ INTERNAL INPUT AND OUTPUT TERMINATION

**Precision Edge™**
**SY58052U**

## FEATURES

- Resynchronizes data to a reference clock
- Guaranteed AC performance over temperature and voltage:
  - DC-to > 10.7Gbps data rate throughput
  - DC-to > 7GHz clock $f_{MAX}$
  - < 190ps Any In-to-Out $t_{pd}$
  - $t_r$ / $t_f$ < 60ps
- Ultra low-jitter design:
  - < 1ps$_{rms}$ random jitter
  - < 10ps$_{pp}$ deterministic jitter
  - < 10ps$_{pp}$ total jitter (clock)
- Internal 50Ω input termination
- Unique input termination and $V_T$ pin accepts DC-coupled and AC-coupled inputs (CML, PECL)
- Internal 50Ω output source termination
- 400mV CML output swing
- Power supply 2.5V ±5% or 3.3V ±10%
- –40°C to 85°C temperature range
- Available in a 16-pin (3mm × 3mm) MLF™ package

## APPLICATIONS

- Data communication systems
- Serial OC-192, OC-192+FEC data-to-clock realignment
- Parallel 10Gbps for OC768
- All SONET OC-3 — OC-768 applications
- All Fibre Channel applications
- All GigE applications

Precision Edge™

## DESCRIPTION

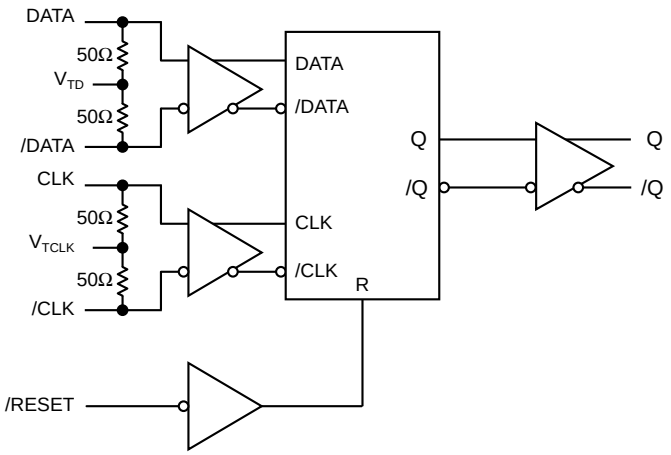
The SY58052U is an ultra-fast, precision, low jitter data-to-clock resynchronizer with a guaranteed maximum data and clock throughput of 10.7Gbps or 7GHz, respectively. The SY58052U is an ideal solution for backplane retiming or retiming after the data passes through long trace lengths. Serial data comes into the data input, and the CML output is synchronous to the input reference clock's rising edge.

The SY58052U differential inputs include a unique, internal termination design that allows access to the termination network through a $V_T$ pin. This feature allows the device to easily interface to different logic standards, both AC- and DC-coupled, without external resistor-bias and termination networks. The result is a clean, stub-free, low-jitter interface solution. The differential CML output is optimized for 50Ω environments with internal 50Ω source termination and a 400mV output swing.

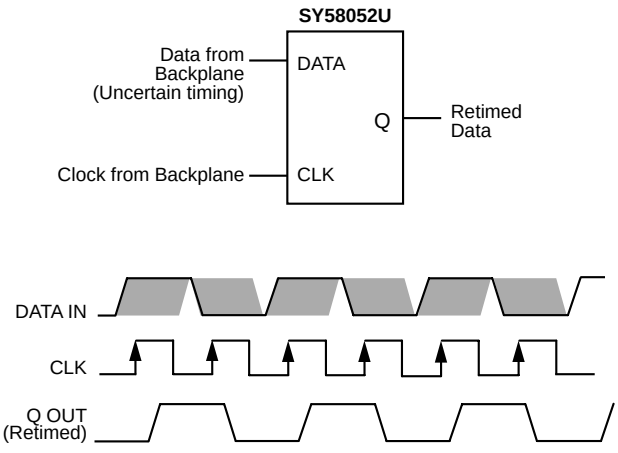
The SY58052U operates from a 2.5V or 3.3V supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). The SY58052U is part of a Micrel's Precision Edge™ product family.

All support documentation can be found on Micrel's web site at www.micrel.com.

## FUNCTIONAL BLOCK DIAGRAM

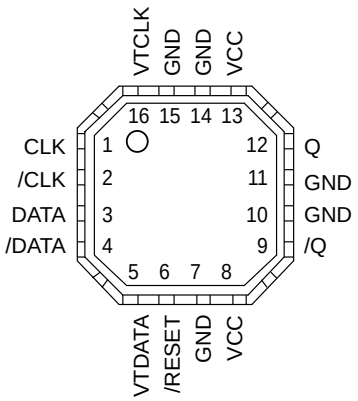



## TYPICAL APPLICATION




Precision Edge is a trademark of Micrel, Inc. and AnyGate is a registered trademark of Micrel, Inc.
*Micro*LeadFrame and MLF are trademarks of Amkor Technology, Inc.

## PACKAGE/ORDERING INFORMATION




**16-Pin MLF™ (MLF-16)**

### Ordering Information[1]

| Part Number | Package Type | Operating Range | Package Marking |
|---|---|---|---|
| SY58052UMI | DIE | Ambient | — |
| SY58052UMI | MLF-16 | Industrial | 052U |
| SY58052UMITR[2] | MLF-16 | Industrial | 052U |

**Notes:**

1. Contact factory for die availability. Die is guaranteed at $T_A$ = 25°C, DC electricals only.
2. Tape and Reel.

## PIN DESCRIPTION

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 1, 2 | CLK, /CLK | Differential Input: This input pair is the clock signal that re-times the data signal at DATA, /DATA. Each pin of this pair internally terminates to the $V_{TCLK}$ pin to 50Ω. Note that this input will default to an indeterminate state if left open. See “Input Interface Applications” section. |
| 3, 4 | DATA, /DATA | Differential Input: This input pair is the signal to be synchronized by the CLK, /CLK signal. Each pin of this pair internally terminates to the $V_{TD}$ pin to 50Ω. Note that this input will default to an indeterminate state if left open. See “Input Interface Applications” section. |
| 5 | VTData | Input Termination Center-Tap: Each of the two inputs, DATA, /DATA terminates to this pin. The VTData pin provides a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section. |
| 6 | /RESET | TTL/CMOS-Compatible Input: The /RESET input asynchronously forces the Q output to a logic “0” state whenever it is active low. Possible state changes due to rising edges on CLK, /CLK are ignored until /RESET goes inactive high. |
| 7, 10, 11, 14, 15 | GND (Exposed Pad) | Ground. Exposed pad must be connected to the same potential as the GND pin. |
| 8, 13 | VCC | Positive Power Supply. Bypass with 0.1µF\|\|0.01µF low ESR capacitors. |
| 12, 9 | Q, /Q | Differential Output: This CML output pair is the output of the flip-flop. The Data input is transferred to the Q output at the rising edge of CLK (falling edge of /CLK). See “Input Interface Applications” section. |
| 16 | VTCLK | Input Termination Center-Tap: Each of the two inputs, CLK, /CLK terminates to this pin. The VTCLK pin provides a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section. |

## TRUTH TABLES

| DATA | /DATA | CLK | /CLK | /RESET | Q | /Q |
|---|---|---|---|---|---|---|
| X | X | X | X | 0 | 0 | 1 |
| X | X | 0 | 1 | 1 | $Q_{N-1}$ | $/Q_{N-1}$ |
| X | X | 1 | 0 | 1 | $Q_{N-1}$ | $/Q_{N-1}$ |
| 0 | 1 | ↓ | ↓ | 1 | 0 | 1 |
| 1 | 0 | ↓ | ↓ | 1 | 1 | 0 |

## Absolute Maximum Ratings[1]

Supply Voltage ($V_{CC}$) ..... –0.5V to +4.0V
Input Voltage ($V_{IN}$) ..... –0.5V to $V_{CC}$
CML Output Voltage ($V_{OUT}$) ..... $V_{CC}$ –1.0V to $V_{CC}$ +5.0V
Termination Current[3]
  Source or Sink Current on $V_{TD}$, $V_{CLK}$ ..... ±60mA
Input Current
  Source or Sink Current on D, /D, CLK, /CLK ..... ±30mA
Lead Temperature (soldering, 10 sec.) ..... +265°C
Storage Temperature ($T_S$) ..... –65°C to +150°C

## Operating Ratings[2]

Supply Voltage ($V_{CC}$) ..... +2.375V to +2.625V
  ..... +3.0V to +3.6V
Ambient Temperature ($T_A$) ..... –40°C to +85°C
Package Thermal Resistance[4]
  MLF™ ($\theta_{JA}$)
    Still-Air ..... 61°C/W
  MLF™ ($\psi_{JB}$)
    Junction-to-Board ..... 38°C/W

## DC ELECTRICAL CHARACTERISTICS[5]

$T_A$ = –40°C to +85°C, unless otherwise noted.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply | | 2.375<br>3.0 | | 2.625<br>3.6 | V<br>V |
| $I_{CC}$ | Power Supply Current | No load, max. $V_{CC}$. | | 60 | 90 | mA |
| $R_{IN}$ | Differential Input Resistance<br>(D, /D or CLK, /CLK) | | 80 | 100 | 120 | Ω |
| $V_{IH}$ | Input HIGH Voltage<br>(D, /D or CLK, /CLK) | **Note 6** | 1.2 | | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage<br>(D, /D or CLK, /CLK) | **Note 6** | 0 | | $V_{IH}$–0.1 | V |
| $V_{IN}$ | Input Voltage Swing<br>(D, /D or CLK, /CLK) | **Note 6** | 100 | | | mV |
| $V_{DIFF\_IN}$ | Differential Input Voltage Swing<br>\|D, /D\| or \|CLK, /CLK\| | **Note 6**<br>See Figure 2a. | 200 | | | mV |
| $\|I_{IN}\|$ | Input Current<br>(IN, /IN) | **Note 6**<br>See Figure 2b. | | | 21 | mA |

**Notes:**

1. Permanent device damage may occur if the ratings in the “Absolute Maximum Ratings” section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability use for input of the same package only.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device’s most negative potential on the PCB. $\psi_{JB}$ uses 4-layer $\theta_{JA}$ in still-air, unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. Due to the internal termination (see “ Input Structures” section) the input current depends on the applied voltages at D, /D and $V_{TD}$ inputs, the CLK, /CLK and $V_{TCLK}$ inputs or the S, /S and $V_{TS}$ inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit!

## LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS[7]

$V_{CC}$ = 2.5V ±5% or 3.3V ±10%; $T_A$ = –40°C to +85°C; unless otherwise noted.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | mV |
| $I_{IH}$ | Input HIGH Current | | –125 | | 20 | µA |
| $I_{IL}$ | Input LOW Current | | | | –300 | µA |

## CML OUTPUTS DC ELECTRICAL CHARACTERISTICS[7]

$V_{CC}$ = 2.5V ±5% or 3.3V ±10%; $R_L$ = 100Ω across output pair or equivalent; $T_A$ = –40°C to +85°C; unless otherwise noted.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage Q, /Q | | $V_{CC}$–0.020 | | $V_{CC}$ | V |
| $V_{OUT}$ | Output Voltage Swing Q, /Q | See Figure 2a. | 325 | 400 | 500 | mV |
| $V_{DIFF\_OUT}$ | Differential Output Voltage Swing Q, /Q | See Figure 2b. | 650 | 800 | 1000 | mV |
| $R_{OUT}$ | Output Source Impedance Q, /Q | | 40 | 50 | 60 | Ω |

## AC ELECTRICAL CHARACTERISTICS[8]

$V_{CC}$ = 2.5V ±5% or 3.3V ±10%; $R_L$ = 100Ω across output pair or equivalent; $T_A$ = –40°C to +85°C; unless otherwise noted.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Operating Frequency | | 10.7 | | | GHz |
| $t_{pd}$ | Propagation Delay (CLK-to-Q) | | 70 | | 190 | ps |
| $t_{RESET}$ | Propagation Delay (RESET-to-Q) | $V_{TH} = V_{CC}/2$ | | | 600 | ps |
| $t_S$ | Set-Up Time | | 20 | | | ps |
| $t_H$ | Hold Time | | 20 | | | ps |
| $t_{RR}$ | Reset Recovery Time | | 500 | | | ps |
| $t_{JITTER}$ | Random Jitter (RJ) | **Note 9** | | | 1 | $ps_{rms}$ |
| | Deterministic Jitter (DJ) | **Note 10** | | | 10 | $ps_{pp}$ |
| | Total Jitter (TJ) | 10GHz Clock, $1\times 10^{-12}$ BER, **Note 11**<br>10GHz Data, $1\times 10^{-12}$ BER, **Note 11** | | | 10<br>14 | $ps_{pp}$<br>$ps_{pp}$ |
| $t_r$, $t_f$ | Rise/Fall Times (20% to 80%) | At full output swing. | 20 | 30 | 60 | ps |

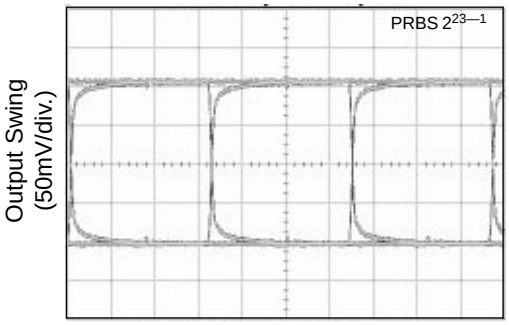
**Notes:**

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
8. Measured with 100mV input swing. See “Timing Diagrams” section for definition of parameters. High-frequency AC-parameters are guaranteed by design and characterization.
9. RJ is measured with a K28.7 comma detect character pattern, measured at 10.7Gbps and 2.5Gbps.
10. DJ is measured at 10.7Gbps and 2.5Gbps, with both K28.5 and $2^{23}$–1 PRBS pattern
11. Total jitter definition: with an ideal clock input frequency of ≤ $f_{MAX}$, no more than one output edge in $10^{12}$ output edges will deviate by more than the specified peak-to-peak jitter value.

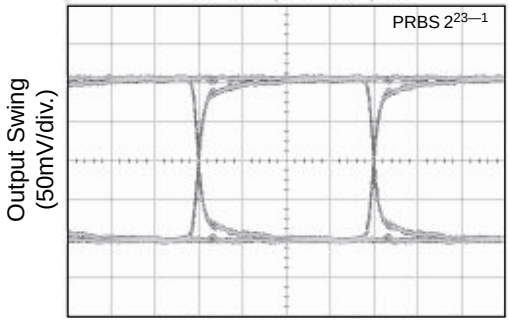
## TYPICAL OPERATING CHARACTERISTICS

$V_{CC}$ = 3.3V, GND = 0V, CLK = 400mV, D = 400mV, $T_A$ = 25°C.

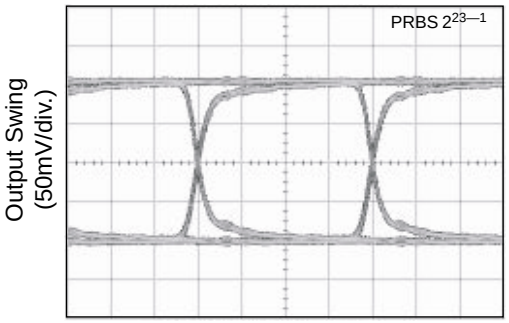
**622Mbps Output**



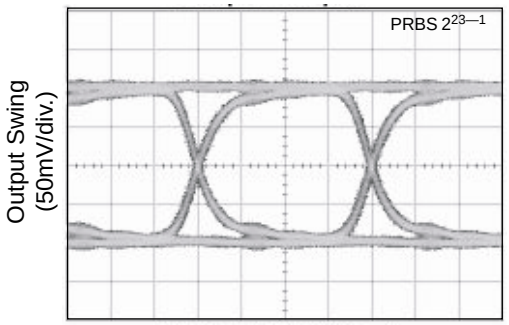

**1.25Gbps Output**



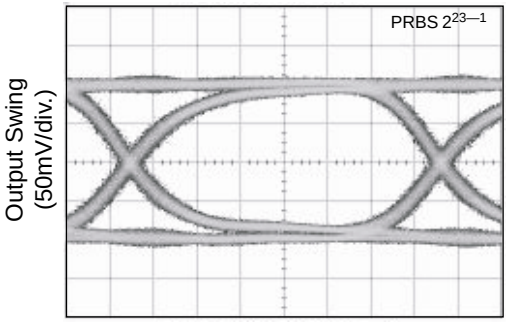

**2.5Gbps Output**



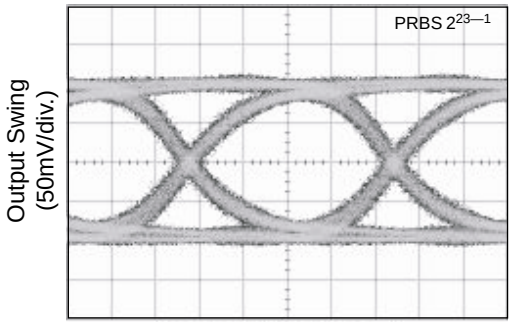

**5Gbps Output**



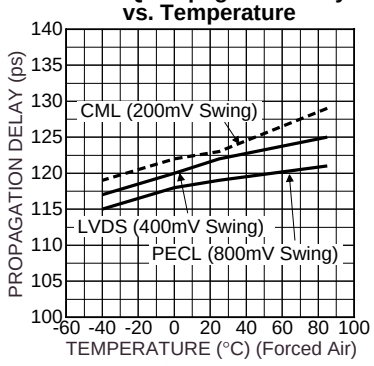

**7Gbps Output**



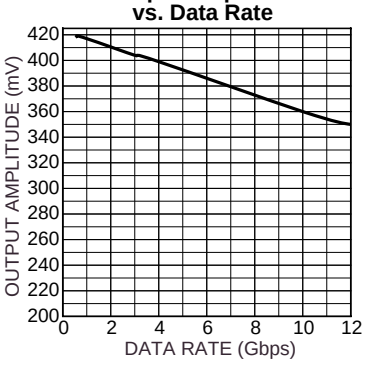

**10.7Gbps Output**



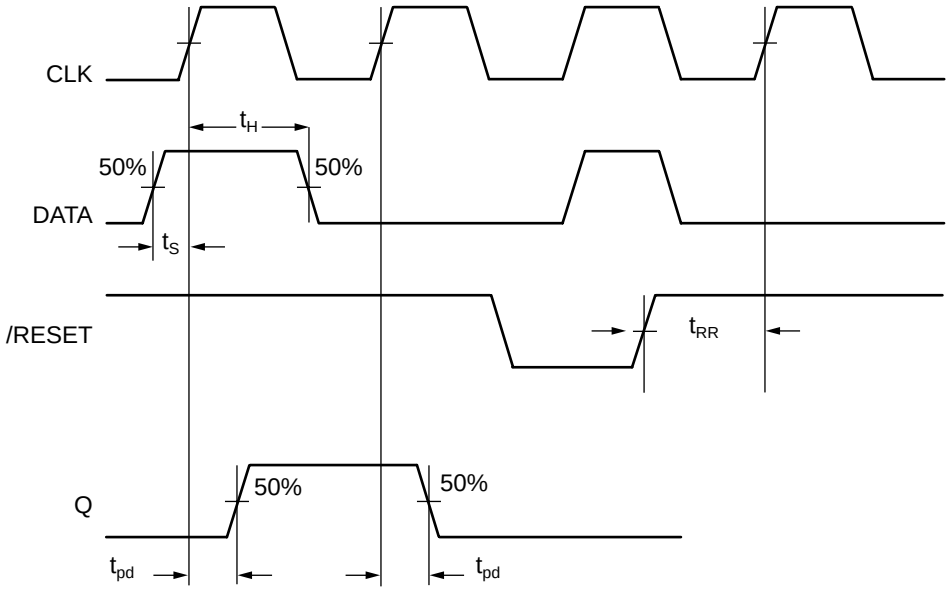

**IN to Q Propagation Delay vs. Temperature**




**Output Amplitude vs. Data Rate**



## TIMING DIAGRAM




## INPUT AND OUTPUT STAGE INTERNAL TERMINATION

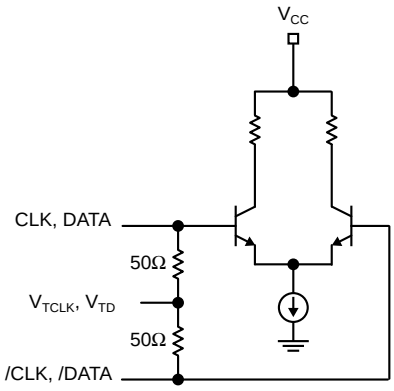



**Figure 1a. Simplified Differential Input Stage**

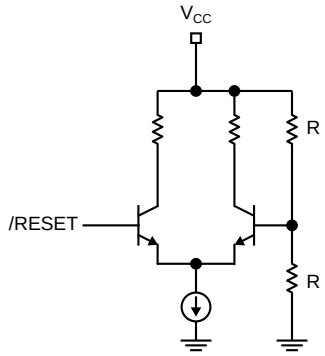



**Figure 1b. Simplified TTL/CMOS Input**

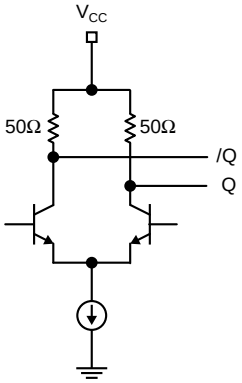



**Figure 1c. Simplified Differential Output Stage**

## OPERATING CHARACTERISTICS

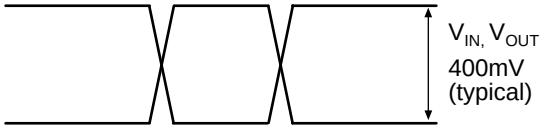



**Figure 2a. Single-Ended Swing**

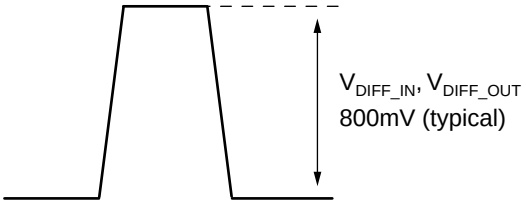



**Figure 2b. Differential Swing**

**Definition of Single-Ended and Differential Swings**

## INPUT INTERFACE APPLICATIONS

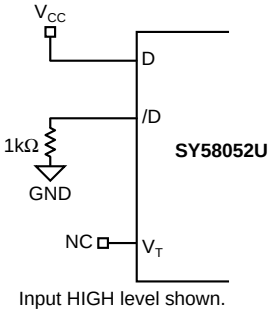



**Figure 3a. Static Input Level**

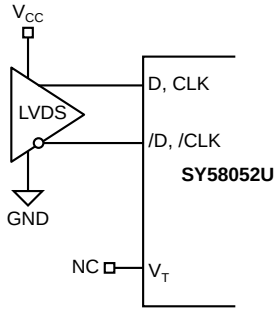



**Figure 3b. LVDS Interface (DC-Coupled)**

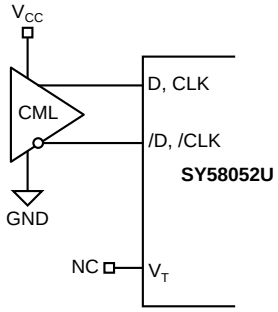



**Figure 3c. CML Interface (DC-Coupled)**

*Option: $V_T$ may be connected to $V_{CC}$.*

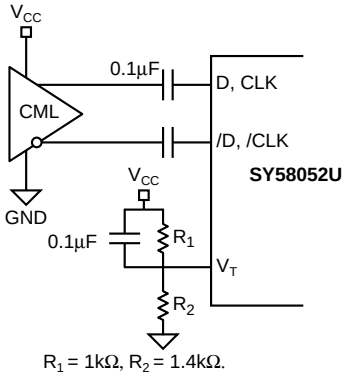



**Figure 3d. CML Interface (AC-Coupled)**

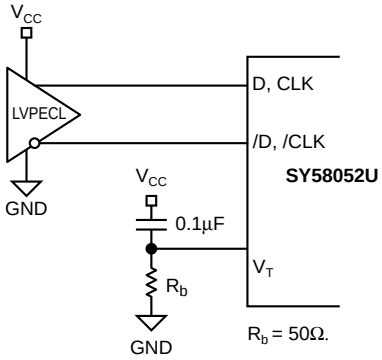



**Figure 3e. LVPECL Interface (DC-Coupled)**

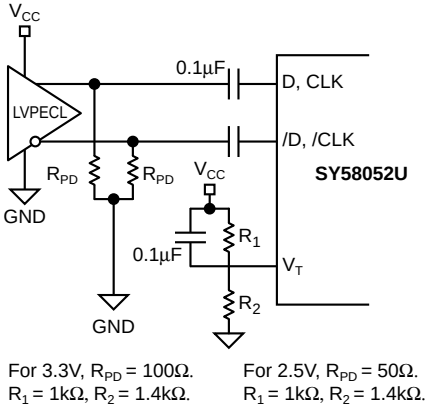
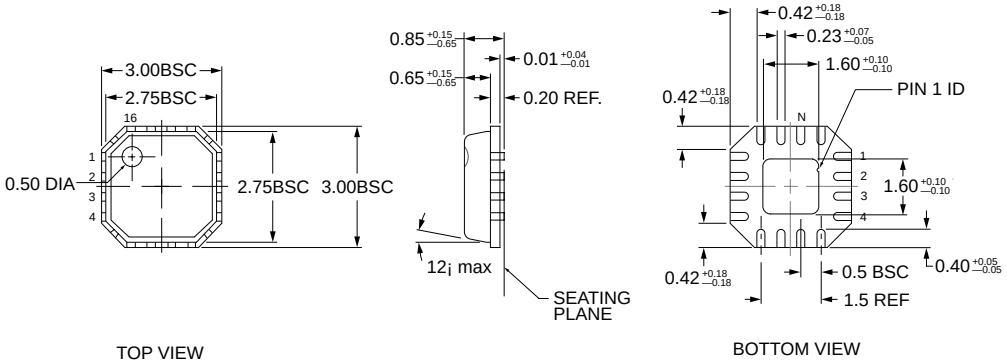



**Figure 3f. LVPECL Interface (AC-Coupled)**

## RELATED PRODUCT AND SUPPORT DOCUMENTATION

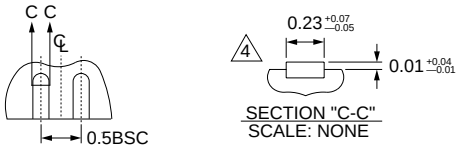
| Part Number | Function | Data Sheet Link |
|---|---|---|
| SY58016L | 3.3V 10Gbps Differential CML Line Driver/ Receiver with Internal Termination | www.micrel.com/product-info/products/sy58016l.shtml |
| SY58051U | 10.7Gbps AnyGate® with Internal Input and Output Termination | www.micrel.com/product-info/products/sy58051u.shtml |
| | MLF™ Application Note | www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf |
| HBW Solutions | New Products and Applications | www.micrel.com/product-info/products/solutions.shtml |

## 16 LEAD *Micro*LeadFrame™ (MLF-16)



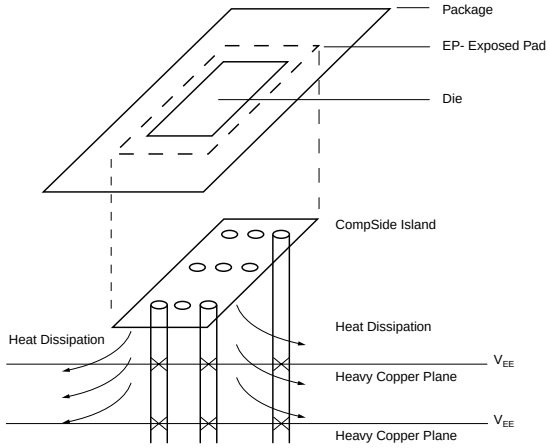

TOP VIEW

BOTTOM VIEW




1. DIMENSIONS ARE IN mm.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAX.
3. PACKAGE WARPAGE MAX 0.05mm.
4. THIS DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20mm AND 0.25mm FROM TIP.
5. APPLIES ONLY FOR TERMINALS

Rev. 02




**PCB Thermal Consideration for 16-Pin MLF™ Package**
**(Always solder, or equivalent, the exposed pad to the PCB)**

**Package Notes:**

1. Package meets Level 2 qualification.
2. All parts dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

**MICREL, INC. 1849 FORTUNE DRIVE SAN JOSE, CA 95131 USA**

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB http://www.micrel.com