FEATURES

- 3.3V and 5V power supply options
- 250ps propagation delay
- Very high voltage gain
- Ideal for Pulse Amplifier and Limiting Amplifier applications
- Data synchronous Enable/Disable (/EN) on Q_{HG} and $/Q_{HG}$ provides for complete glitchless gating of the outputs
- Ideal for gating timing signals
- Complete solution for high quality, high frequency crystal oscillator applications
- Available in an ultra-small 8-pin (2mm × 2mm) MLF™ package

APPLICATIONS

- Oscillator modules

Precision Edge™

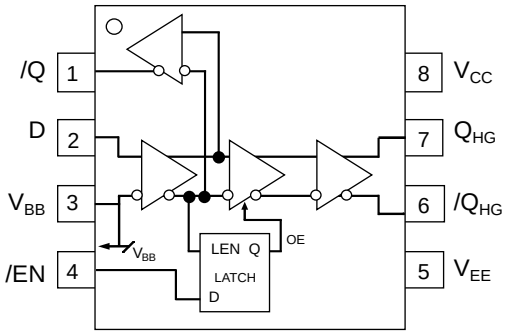
DESCRIPTION

The SY89250V is a differential PECL/ECL receiver/buffer in a space saving (2mm × 2mm) MLF™ package. The device is functionally equivalent to the SY100EL16VC, but features a 70% smaller footprint. It provides a V_{BB} output for either single-ended application or as a DC bias for AC-coupling to the device.

The SY89250V provides an /EN input which is synchronized with the data input (D) signal in a way that provides glitchless gating of the Q_{HG} and $/Q_{HG}$ outputs. When the /EN signal is LOW, the input is passed to the outputs and the data output equals the data input. When the data input is HIGH and the /EN goes HIGH, it will force the Q_{HG} LOW and the $/Q_{HG}$ HIGH on the next negative transition of the data input. If the data input is LOW when the /EN goes HIGH, the next data transition to a HIGH is ignored and Q_{HG} remains LOW and $/Q_{HG}$ remains HIGH. The next positive transition of the data input is not passed on to the data outputs under these conditions. The Q_{HG} and $/Q_{HG}$ outputs remain in their disabled state as long as the /EN input is held HIGH. The /EN input has no influence on the /Q output and the data input is passed on (inverted) to this output whether /EN is HIGH or LOW. This configuration is ideal for crystal oscillator applications, where the oscillator can be free running and gated on and off synchronously without adding extra counts to the output.

All support documentation can be found on Micrel's web site at www.micrel.com.

BLOCK DIAGRAM

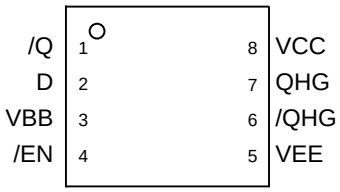


FUNCTIONAL CROSS REFERENCE

Micrel Part Number	PECL/ECL	Functional Cross
SY89250V	100k	SY100EL16VC

Precision Edge is a trademark of Micrel, Inc.
*Micro*LeadFrame and MLF are trademarks of Amkor Technology, Inc.

PACKAGE/ORDERING INFORMATION



8-Pin MLF™
(Ultra-Small Outline)

Ordering Information

Part Number	Package Type	PECL/ECL Logic	Operating Range	Package Marking
SY89250VMI	MLF-8	100KEL	Industrial	250
SY89250VMITR(1)	MLF-8	100KEL	Industrial	250

Note:

1. Tape and Reel.

PIN DESCRIPTION

Pin Number	Pin Name	Type	Pin Function
1	/Q	100k	Single-Ended PECL/ECL Feedback Output.
2	D	100k	Single-Ended PECL/ECL Input: The signal input includes an internal 75kΩ pull-down ECL Input resistor. If input is left open, Q output will default to LOW. See "Input *Interface Applications"* section for single-ended inputs.
3	VBB	Reference Output Voltage	Bias Voltage: VCC–1.3V. Used as reference voltage when AC-coupling to the D input. Max sink/source is ±0.5mA.
4	/EN	Enable Input	/EN Input which is synchronized with data input (D) signal in a way that provides glitchless gating of Q_{HG} and $/Q_{HG}$ outputs. Includes internal 75kΩ pull-down resistor. Default is LOW
5	VEE, Exposed Pad	Negative Power Supply	Negative Power Supply: V_{EE} and exposed pad must be tied to most negative supply. For PECL/LVPECL connect to ground.
6, 7	/QHG, QHG	100k ECL Output	Differential PECL/ECL Output: Defaults to LOW if D inputs left open. See *"Output Interface Applications"* section for recommendations on terminations.
8	VCC	Positive Power Supply	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors.

TRUTH TABLE

/EN	Q_{HG} Output
0	Data
1	Logic Low

Absolute Maximum Ratings[1]

Power Supply Voltage (V_{CC}) ..... –0.5V to +6.0V
ECL Input Voltage (V_{IN}) ..... 0V to V_{CC} +0.5V
Voltage Applied to Output at HIGH State
(V_{OUT}) ..... –0.5V to V_{CC}
Current Applied to Output at LOW State
(I_{OUT}) ..... Twice the rated I_{OL} mA
Lead Temperature (soldering, 10 sec.) ..... 220°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Power Supply Voltage $|V_{CC}–V_{EE}|$ .... 3.3V ±10% or 5V ±10%
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance,[3]
MLF™ (θ_{JA})
Still-Air ..... 93°C/W
MLF™ (ψ_{JB}), ... 60°C/W

DC ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C; unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{EE}	Power Supply	$\|V_{CC}–V_{EE}\|$ $\|V_{CC}–V_{EE}\|$	3.0 4.5	3.3 5.0	3.6 5.5	V V
I_{EE}	Power Supply Current				46	mA
I_{IH}	Input HIGH Current				150	µA
V_{BB}	Output Reference Voltage		V_{CC} –1.38	V_{CC} –1.32	V_{CC} –1.26	V

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±10% or +5V ±10% and V_{EE} = 0V; V_{CC} = 0V and V_{EE} = –3.3V ±10% or –5V ±10%; T_A = –40°C to +85°C; unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	Note 4	V_{CC}–1.085		V_{CC}–0.880	V
V_{OL}	Output LOW Voltage	Note 4	V_{CC}–1.830		V_{CC}–1.555	V
V_{IH}	Input HIGH Voltage		V_{CC}–1.165		V_{CC}–0.880	V
V_{IL}	Input LOW Voltage		V_{CC}–1.810		V_{CC}–1.475	V
V_{BB}	Output Reference Voltage		V_{CC}–1.38		V_{CC}–1.26	V
V_{PP}	Minimum Input Swing		150			mV
I_{IH}	Input HIGH Current				150	µA
I_{IL}	Input LOW Current		0.5			µA

Notes:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.
4. Output loaded with 50Ω to V_{CC}–2V.

AC ELECTRICAL CHARACTERISTICS

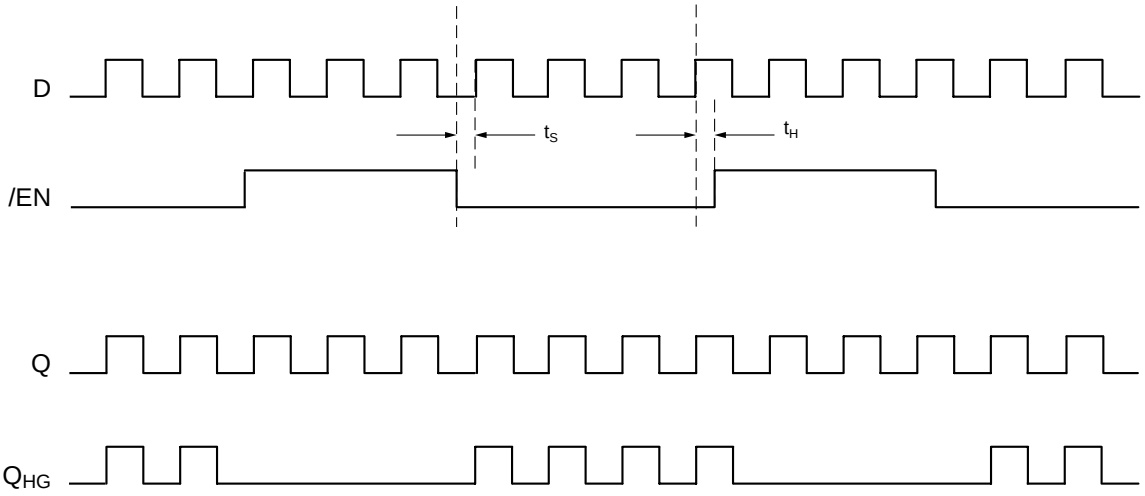
$V_{EE} = V_{EE}$(min) to V_{EE}(max); V_{CC} = GND; T_A = –40°C to +85°C; unless otherwise stated.

Symbol	Parameter		Condition	Min	Typ	Max	Units
t_{pd}	Propagation Delay to:						
	Q, /Q Output	D (Diff)				380	ps
		D (SE)				430	ps
	QHG, /QHG Output	D (Diff)				730	ps
		D (SE)				780	ps
t_S	Set-Up Time	/EN			150		ps
t_H	Hold Time	/EN			150		ps
t_{SKEW}	Duty Cycle Skew	(Diff)	(5)		5	20	ps
V_{PP}	Minimum Input Swing	/EN	(6)	150			mV
V_{CMR}	Common Mode Range	/EN	(7)	–1.3		–0.4	V
t_r, t_f	Output Q Rise/Fall Times (20% to 80%)		At full output swing	100	225	350	ps

Notes:

5. Duty cycle skew is the difference between a t_{pd} propagation delay through a device.
6. Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈ 40 to Q, /Q outputs and a DC gain of ≈ 200 or higher to /Q_{HG}, Q_{HG} outputs.
7. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}(min) and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –3.3V. Note for PECL operation, the V_{CMR}(min) will be fixed at 3.3V – |V_{CMR}(min)|.

TIMING DIAGRAM



OUTPUT INTERFACE APPLICATIONS

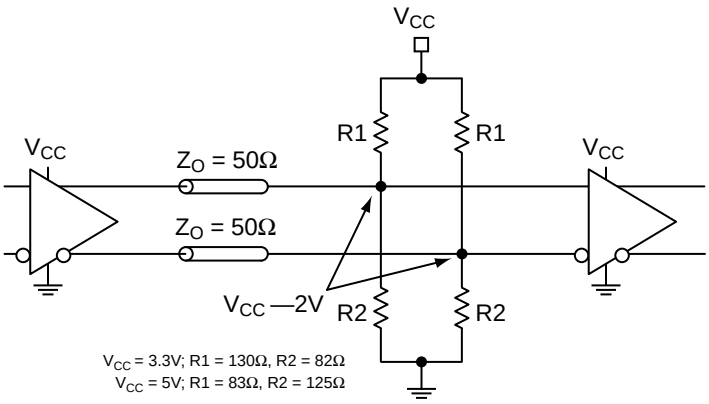


Figure 1a. Parallel Thevenin-Equivalent Termination

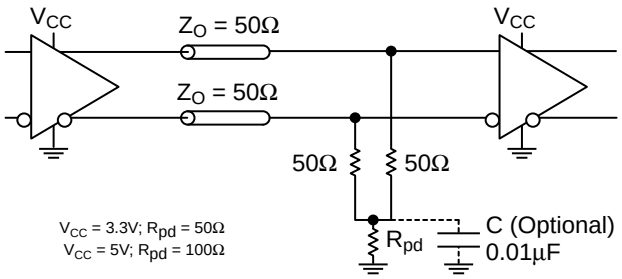


Figure 1b. Three Resistor "Y Termination"

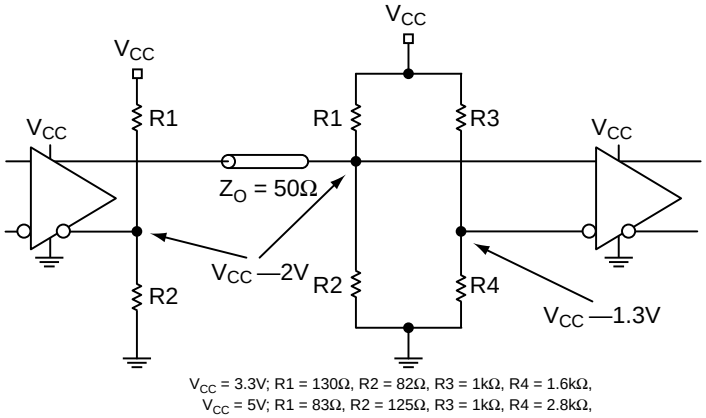
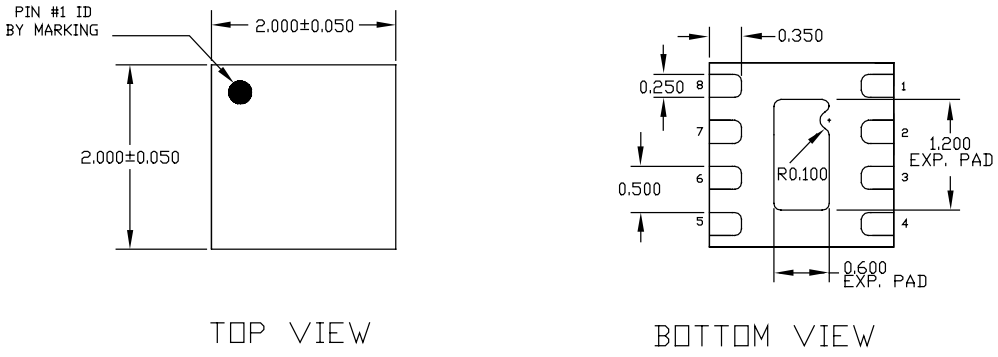


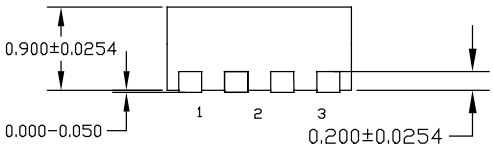
Figure 1c. Terminating Unused I/O

RELATED PRODUCT AND SUPPORT DOCUMENTATION

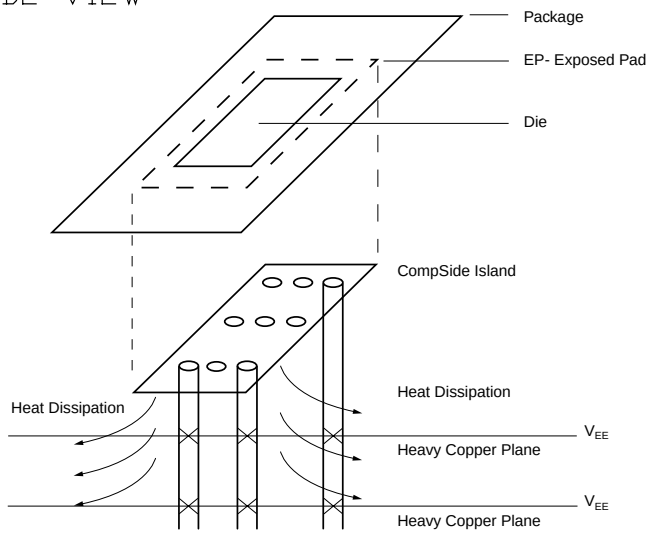
Part Number	Function	Data Sheet Link
SY89306/316V	3.3V/5V 2.5GHz PECL/ECL Differential Receiver/Buffer	www.micrel.com/product-info/products/sy89306-316v.shtml
SY89206/216V	3.3V/5V 1GHz PECL/ECL Differential Receiver/Buffer	www.micrel.com/product-info/products/sy89206-216v.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

8 LEAD ULTRA-SMALL EPAD-*Micro*LeadFrame™ (MLF-8)





NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 8-Pin MLF™ Package

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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