



MMC 4041

QUAD TRUE/COMPLEMENT BUFFER

GENERAL DESCRIPTION

The MMC 4041 is a monolithic integrated circuit processed in standard Al-gate CMOS technology. The MMC 4041 contains four true/complement buffers consisting of n- and p-channel units having low channel resistance and high current (sourcing and sinking) capability. The MMC 4041 is intended for use as a buffer, line driver, or CMOS-to-TTL driver. It can be used as an ultra-low power resistor-network driver for A/D and D/A conversion, as a transmission-line driver, and in other applications where high noise immunity and low-power dissipation are primary design requirements.

FEATURES

- Balanced sink and source current; approximately 4 times standard „B“ drive
- Equalized delay to true and complement outputs

ABSOLUTE MAXIMUM RATINGS

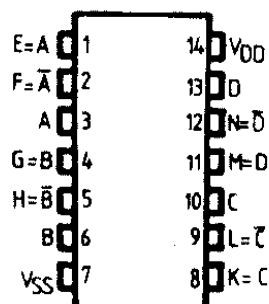
V_{DD}^*	Supply voltage: G and H types	-0.5 to 20	V
	E and F types	-0.5 to 18	V
V_i	Input voltage	-0.5 to $V_{DD} + 0.5$	V
I_i	DC input current (any one input)	± 10	mA
P_{tot}^*	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_A = full package-temperature range	100	mW
T_A	Operating temperature: G and H types	-55 to 125	°C
	E and F types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

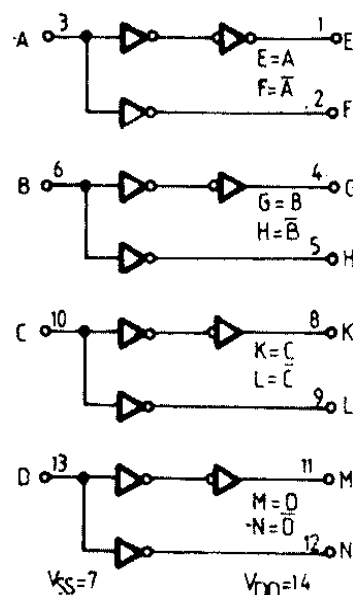
RECOMMENDED OPERATING CONDITIONS

V_{DD}^*	Supply voltage: G and H types	3 to 18	V
	E and F types	3 to 15	V
V_i	Input voltage	0 to V_{DD}	V
T_A	Operating temperature: G and H types	-55 to 125	°C
	E and F types	-40 to 85	°C

CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _{LOW}		25°C			T _{HIGH}		
							min.	max.	min.	typ	max.	min.	max.	
I _i Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA	
		0/10			10		2		0.02	2		60		
		0/15			15		4		0.02	4		120		
		0/20			20		20		0.04	20		600		
	E, F types	0/ 5			5		4		0.02	4		30		
		0/10			10		8		0.02	8		60		
		0/15			15		16		0.02	16		120		
V _{OH} Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V	
		0/10		< 1	10	9.95		9.95			9.95			
		0/15		< 1	15	14.95		14.95			14.95			
V _{OL} Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V	
		10/0		< 1	10		0.05			0.05		0.05		
		15/0		< 1	15		0.05			0.05		0.05		
V _{IH} —Input high voltage			0.5/4.5	< 1	5	4		4			4		V	
			1/9	< 1	10	8		8			8			
			1.5/13.5	< 1	15	12		12			12			
V _{IL} —Input low voltage			4.5/0.5	< 1	5		1			1		1	V	
			9/1	< 1	10		2			2		2		
			13.5/1.5	< 1	15		2.5			2.5		2.5		
I _{OH} Output drive current	G, H types	0/ 5	2.5		5	-8.4		-6.4	-12.8		-4.6		mA	
		0/ 5	4.6		5	-2.1		-1.6	-3.2		-1.2			
		0/10	9.5		10	-6.25		-5	-10		-3.5			
		0/15	13.5		15	-24		-19	-38		-13			
	E, F types	0/ 5	2.5		5	-6.8		-5.44	-12.8		-4.08			
		0/ 5	4.6		5	-1.7		-1.36	-3.2		-1.02			
		0/10	9.5		10	-5.31		-4.25	-10		-3.18			
		0/15	13.5		15	-20.18		-16.15	-38		-12.1			
I _{OL} Output sink current	G, H types	0/ 5	0.4		5	2.1		1.6	3.2		1.2		mA	
		0/10	0.5		10	6.25		5	10		3.5			
		0/15	1.5		15	24		19	38		13			
	E, F types	0/ 5	0.4		5	1.7		1.36	3.2		1.02			
		0/10	0.5		10	5.31		4.25	10		3.18			
		0/15	1.5		15	20.18		16.15	38		12.11			
I _{IH} , I _{IL} Input leakage current	G, H types	0/18	Any input		18		±0.1		±10 ⁻⁵	±0.1		±1	μA	
	E, F types	0/15			15		±0.3		±10 ⁻⁵	±0.3		±1		
C _i Input capacitance			Any input.						15	225			pF	

 $T_{LOW} = -55^\circ\text{C}$ for G, H devices; -40°C for E, F devices $T_{HIGH} = +125^\circ\text{C}$ for G, H devices; $+85^\circ\text{C}$ for E, F devices

The Noise Margin for both "1" and "0" level is

1 V min. with $V_{DD} = 5\text{ V}$ 2 V min. with $V_{DD} = 10\text{ V}$ 2.5 V min. with $V_{DD} = 15\text{ V}$

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ kohm}$, typical temperature coefficient for all V_{DD} values is $0.3\%/^\circ\text{C}$, all input rise and fall times = 20 ns)

PARAMETER	TEST CONDITIONS	VALUES			UNIT
	VDD(V)	min.	typ.	max.	
t_{PLH} Propagation delay time t_{PHL}	5		60	120	ns
	10		35	70	
	15		25	50	
t_{THL} Transition time t_{THL}	5		40	80	ns
	10		20	40	
	15		15	30	

SCHEMATIC DIAGRAM