



MMC 4095 MMC 4096

GATED J-K MASTER-SLAVE FLIP-FLOPS

GENERAL DESCRIPTION

The MMC 4095/4096 (intermediate or extended temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package.

The MMC 4095 and MMC 4096 are J-K Master-Slave Flip-Flops featuring separate AND gating of multiple J and K inputs. The gated J-K inputs control transfer of information into the master section during clocked operation. Information on the J-K inputs is transferred to the Q and $\bar{Q}$ outputs on the positive edge of the clock pulse. SET and RESET inputs (active high) are provided for asynchronous operation.

FEATURES

- 16 MHz toggle rate (typ.) at $V_{DD} - V_{SS} = 10\text{ V}$
- Gated inputs.

ABSOLUTE MAXIMUM RATINGS

V_{DD}^*	Supply voltage: G and H types	-0.5 to 20	V
	E and F types	-0.5 to 18	V
V_i	Input voltage	-0.5 to $V_{DD}+0.5$	V
I_i	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_A = full package-temperature range	100	mW
T_A	Operating temperature: G and H types	-55 to 125	°C
	E and F types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

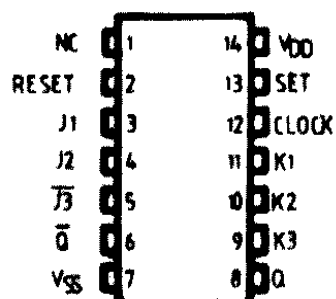
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

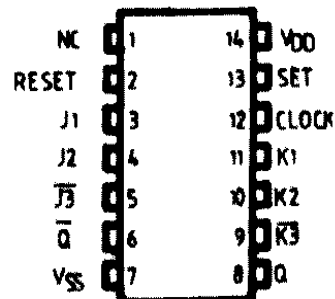
V_{DD}^*	Supply voltage: G and H types	3 to 18	V
	E and F types	3 to 15	V
V_i	Input voltage	0 to V_{DD}	V
T_A	Operating temperature: G and H types	-55 to 125	°C
	E and F types	-40 to 85	°C

CONNECTION DIAGRAM

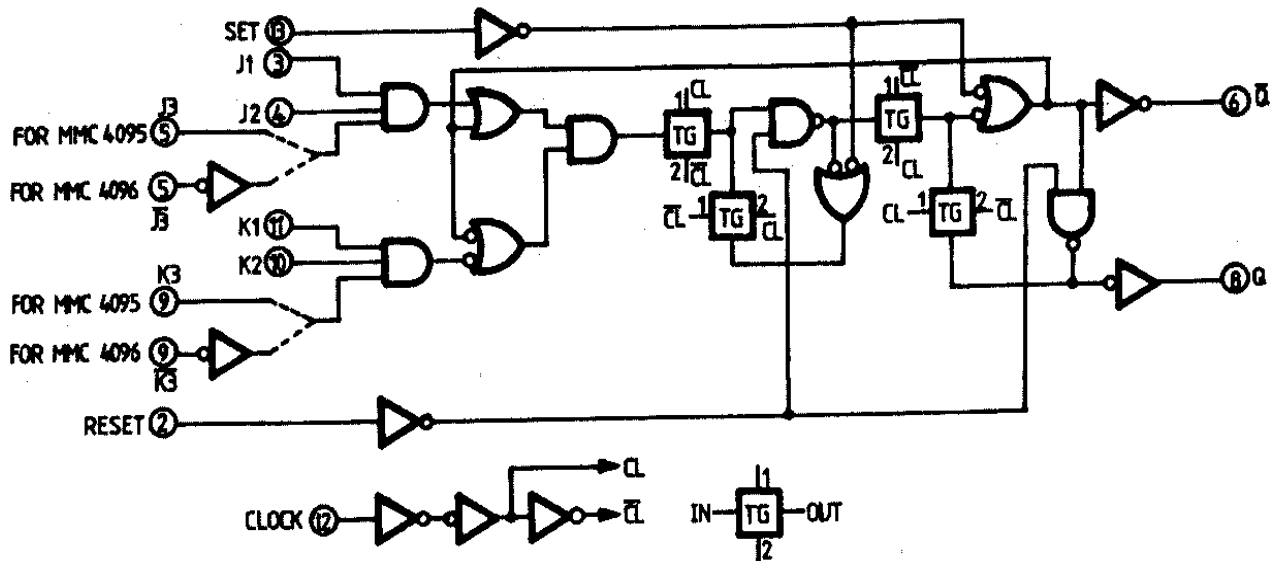
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LOGIC DIAGRAM



TRUTH TABLES

SYNCHRONOUS OPERATION

(S = 0 R = 0)

Inputs before positive clock transition		Outputs after positive clock transition	
J*	K*	Q	Q
0	0	No change	
0	1		
1	0	0	1
1	1	1	0
		Toggles	

* For MMC 4095

For MMC 4096

 $J = J1 \cdot J2 \cdot J3$ $J = J1 \cdot J2 \cdot \bar{J3}$ $K = K1 \cdot K2 \cdot K3$ $K = K1 \cdot K2 \cdot \bar{K3}$

ASYNCHRONOUS OPERATION

(J and K — DON'T CARE)

S	R	Q	Q
0	0	No change	
0	1		
1	0	1	0
1	1	0	0

0 = V_{SS} , 1 = V_{DD}

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES						UNIT	
			V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _{LOW} *		25°C			T _{HIGH} *		
							min.	max.	min.	typ	max.	min.		max.
I _L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
	E, F types	0/ 5			5		4		0.02	4		30		
		0/10			10		8		0.02	8		60		
0/15				15		16		0.02	16		120			
V _{OH}	Output high voltage	0/ 5		< 1	5	4.95		4.95			4.95		V	
		0/10		< 1	10	9.95		9.95			9.95			
		0/15		< 1	15	14.95		14.95			14.95			
V _{OL}	Output low voltage	5 /0		< 1	5		0.05			0.05		0.05	V	
		10/0		< 1	10		0.05			0.05		0.05		
		15/0		< 1	15		0.05			0.05		0.05		

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PARAMETER			TEST CONDITIONS						VALUES			UNIT	
			V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)			T _{LOW}		25°C		
							min.	max.	min.	typ	max.	min.	max.
V _{IH}	Input high voltage		0.5/4.5 1/9 1.5/13.5	< 1 < 1 < 1	5 10 15	3.5 7 11		3.5 7 11			3.5 7 11		V
V _{IL}	Input low voltage		4.5/0.5 9/1 13.5/1.5	< 1 < 1 < 1	5 10 15		1.5 3 4			1.5 3 4		1.5 3 4	V
I _{OH}	Output drive current	C, H types	0/ 5	2.5	5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6	5	-0.64		-0.51	-1		-0.36		
			0/10	9.5	10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5	15	-4.2		-3.4	-6.8		-2.4		
		E, F types	0/ 5	2.5	5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6	5	-0.52		-0.44	-1		-0.36		
			0/10	9.5	10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5	15	-3.6		-3.0	-6.8		-2.4		
I _{OL}	Output sink current	G, H types	0/ 5	0.4	5	0.64		0.51	1		0.36		mA
			0/10	0.5	10	1.6		1.3	2.6		0.9		
			0/15	1.5	15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4	5	0.52		0.44	1		0.36		
			0/10	0.5	10	1.3		1.1	2.6		0.9		
			0/15	1.5	15	3.6		3.0	6.8		2.4		
I _{IH} , I _{IL}	Input leakage current	G, H types	0/18	Any input	18		±0.1		±10 ⁻⁵	±0.1		±1	μA
		E, F types	0/15		15		±0.3		±10 ⁻⁵	±0.3		±1	
C _I	Input capacitance		Any input						5	7.5			pF

* $T_{LOW} = -55^\circ\text{C}$ for G, H devices; -40°C for E, F devices.

* $T_{HIGH} = +125^\circ\text{C}$ for G, H devices; $+85^\circ\text{C}$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V

2 V min. with $V_{DD} = 10$ V

2.5 V min. with $V_{DD} = 15$ V

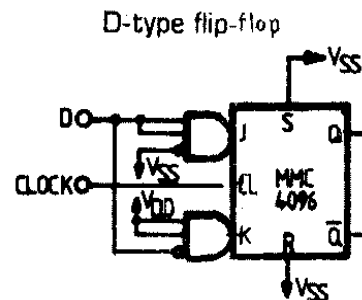
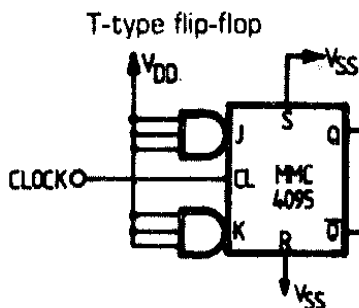
DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$, $C_L = 50$ pF, $R_L = 200$ kohm, typical temperature coefficient for all $V_{DD} = 0.3\%/^\circ\text{C}$ all input rise and fall times = 20 ns).

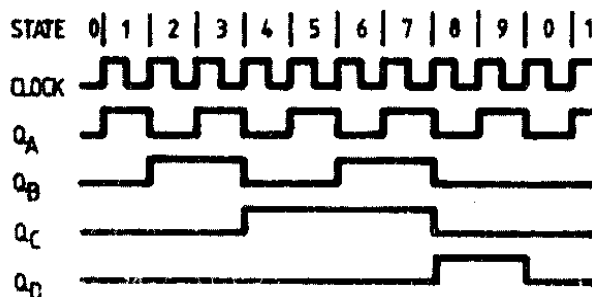
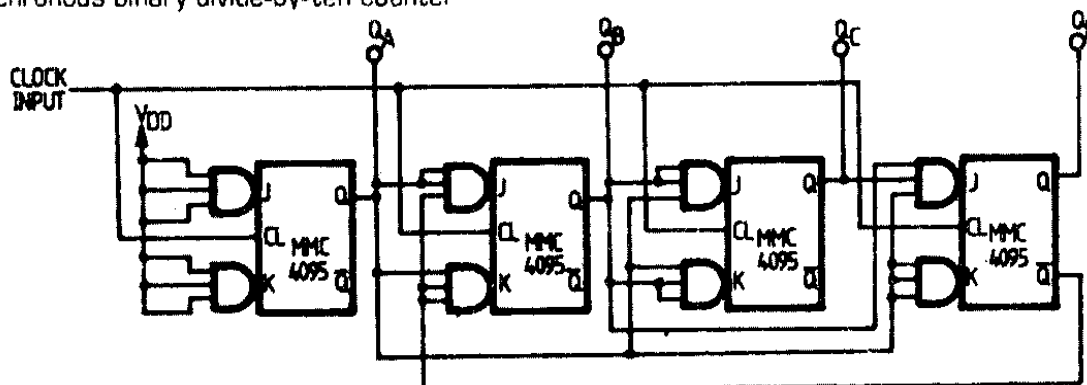
PARAMETER		TEST CONDITIONS		VALUES			UNIT
		V_{DD} (V)		min.	typ.	max.	
t_{PLH}	Propagation delay time	5			250	500	ns
t_{PHL}		10			100	200	
		15			75	150	
t_{PLH}	Propagation delay time (Set or reset)	5			150	300	ns
t_{PHL}		10			75	150	
		15			50	100	

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PARAMETER	TEST CONDITIONS	VALUES				UNIT
		V _{DD} (V)	min.	typ.	max.	
t_{THL} Transition time		5		100	200	ns
t_{TLH}		10		50	100	
		15		40	80	
f_{cl} Maximum clock input frequency		5	3.5	7		MHz
		10	8	16		
		15	12	24		
t_W Clock pulse width		5	140	70		ns
		10	60	30		
		15	40	20		
t_w, t_f Clock input rise or fall time		5			15	μ s
		10			5	
		15			5	
t_W Set or reset pulse width		5	200	100		ns
		10	100	50		
		15	50	25		
t_{setup} Data setup time		5	400	200		ns
		10	160	80		
		15	100	50		

TYPICAL APPLICATIONS

Synchronous binary divide-by-ten counter

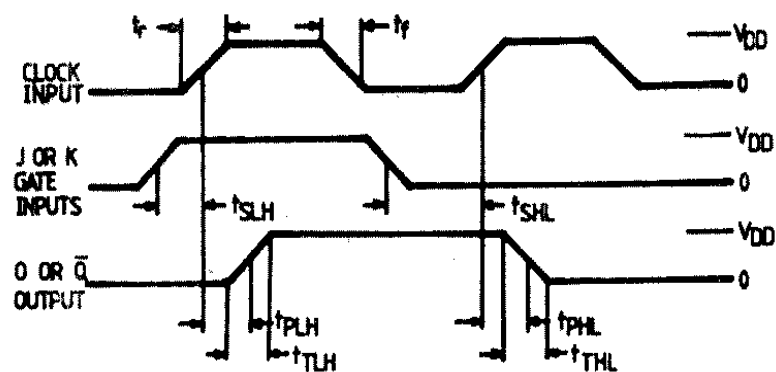


STATE	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

In all MMC 4095 units the Set and Reset are connected to V_{SS}

WAVEFORMS

Propagation delay, transition and setup-time



Clock pulse rise and fall time

