

# SYNCHRONOUS DRAM MODULE

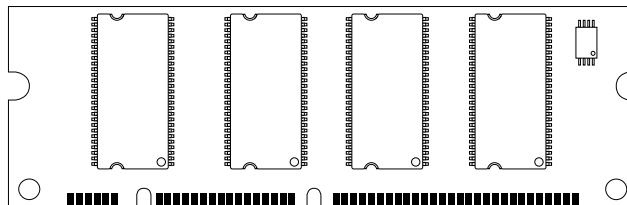
**MT4LSDT1632U - 64MB; MT8LSDT1632U - 64MB  
MT8LSDT3232U - 128MB; MT8LSDT6432U - 256MB**

For the latest data sheet, please refer to the Micron® Web site:  
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## Features

- JEDEC pinout in a 100-pin, dual in-line memory module (DIMM)
- 64MB (16 Meg x 32) , 128MB (32 Meg x 32), and 256MB (64 Meg x 32)
- Utilizes 100 MHz and 125 MHz SDRAM components
- Single +3.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge and Auto Refresh Modes  
64MB and 128 MB modules; 64ms, 4,096-cycle refresh (15.625µs refresh interval); 256MB modules; 64ms, 8,192-cycle refresh (7.81µs refresh interval)
- LVTTL-compatible inputs and outputs
- Serial Presence-Detect (SPD)

**Figure 1: 100-Pin DIMM (MO-161)**



## OPTIONS

- Package  
100-pin DIMM (Gold)  
100-pin DIMM (Lead-Free)
- Frequency / CAS Latency  
133 MHz (7.5ns) / CL = 3  
125 MHz (8ns) / CL = 3  
100 MHz (10ns) / CL = 2

## MARKING

G  
Y  
-75  
-8  
-10

**Table 1: Timing Parameters**

CL = CAS (READ) latency

MODULE MARKING	CLOCK FREQUENCY	ACCESS TIME		SETUP TIME	HOLD TIME
		CL = 2	CL = 3		
-75	133 MHz	–	5.4ns	1.5ns	0.8ns
-8	125 MHz	6ns	6ns	2ns	1ns
-10	100 MHz	9ns	7.5ns	2ns	1ns

**Table 2: Address Table**

MODULE DENSITY	MT4LSDT1632U	MT8LSDT1632U	MT8LSDT3232U	MT8LSDT6432U
Refresh Count	4K	4K	4K	8K
Device Banks	4 (BA0-BA1)	4 (BA0-BA1)	4 (BA0-BA1)	4 (BA0-BA1)
Device Configuration	16 Meg x 8	8 Meg x 8	16 Meg x 8	32 Meg x 8
Device Row Addressing	4K (A0-A11)	4K (A0-A11)	4K (A0-A11)	8K (A0-A12)
Device Column Addressing	1K (A0-A9)	512 (A0-A8)	1K (A0-A9)	1K (A0-A9)
Module Ranks	1 (S0#, S2#)	2 (S0#, S2#; S1#, S3#)	2 (S0#, S2#; S1#, S3#)	2 (S0#, S2#; S1#, S3#)

**Table 3: Part Numbers**

PART NUMBER	CONFIGURATION	SYSTEM BUS SPEED
MT4LSDT1632UG-75__	16 Meg x 32	133 MHz
MT4LSDT1632UY-75__	16 Meg x 32	133 MHz
MT4LSDT1632UG-8__	16 Meg x 32	125 MHz
MT4LSDT1632UY-8__	16 Meg x 32	125 MHz
MT4LSDT1632UG-10__	16 Meg x 32	100 MHz
MT4LSDT1632UY-10__	16 Meg x 32	100 MHz
MT8LSDT1632UG-75__	16 Meg x 32	133 MHz
MT8LSDT1632UY-75__	16 Meg x 32	133 MHz
MT8LSDT1632UG-8__	16 Meg x 32	125 MHz
MT8LSDT1632UY-8__	16 Meg x 32	125 MHz
MT8LSDT1632UG-10__	16 Meg x 32	100 MHz
MT8LSDT1632UY-10__	16 Meg x 32	100 MHz
MT8LSDT3232UG-75__	32 Meg x 32	133 MHz
MT8LSDT3232UY-75__	32 Meg x 32	133 MHz
MT8LSDT3232UG-8__	32 Meg x 32	125 MHz
MT8LSDT3232UY-8__	32 Meg x 32	125 MHz
MT8LSDT3232UG-10__	32 Meg x 32	100 MHz
MT8LSDT3232UY-10__	32 Meg x 32	100 MHz
MT8LSDT6432UG-75__	64 Meg x 32	133 MHz
MT8LSDT6432UY-75__	64 Meg x 32	133 MHz
MT8LSDT6432UG-8__	64 Meg x 32	125 MHz
MT8LSDT6432UY-8__	64 Meg x 32	125 MHz
MT8LSDT6432UG-10__	64 Meg x 32	100 MHz
MT8LSDT6432UY-10__	64 Meg x 32	100 MHz

**Table 4: Pin Assignment Front (100-Pin DIMM)**

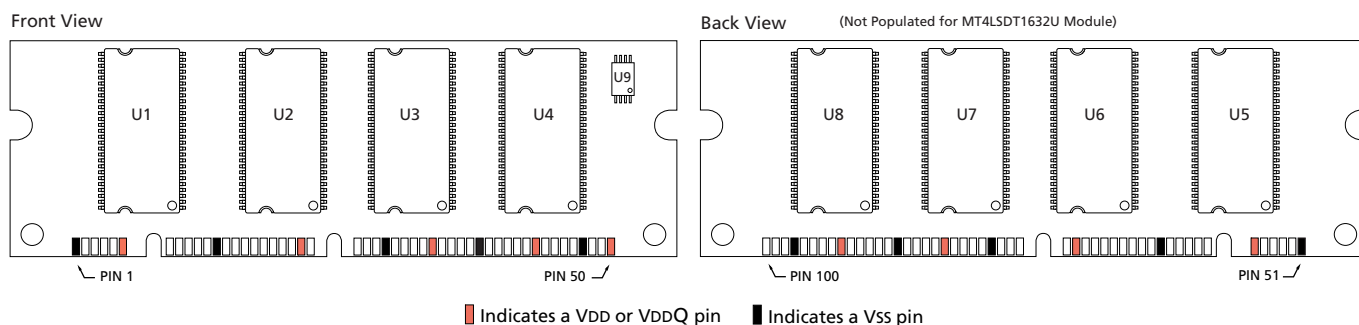
PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	13	A0	26	Vss	38	DQ16
2	DQ0	14	A2	27	CKE0	39	DQ17
3	DQ1	15	A4	28	WE#	40	DQ18
4	DQ2	16	A6	29	S0#	41	DQ19
5	DQ3	17	A8	30	S2#	42	VDD
6	VDD	18	A10	31	VDD	43	DQ20
7	DQ4	19	BA1	32	NC	44	DQ21
8	DQ5	20	A12/NC	33	NC	45	DQ22
9	DQ6	21	VDD	34	NC	46	DQ23
10	DQ7	22	NC	35	NC	47	Vss
11	DQMB0	23	RFU	36	Vss	48	SDA
12	Vss	24	RFU	37	DQMB2	49	SCL
		25	CK0			50	VDD

**Table 5: Pin Assignment Back (100-Pin DIMM)**

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
51	Vss	63	A1	76	Vss	88	DQ24
52	DQ8	64	A3	77	CKE1	89	DQ25
53	DQ9	65	A5	78	NC	90	DQ26
54	DQ10	66	A7	79	S1#	91	DQ27
55	DQ11	67	A9	80	S3#	92	VDD
56	VDD	68	BA0	81	VDD	93	DQ28
57	DQ12	69	A11	82	NC	94	DQ29
58	DQ13	70	NC	83	NC	95	DQ30
59	DQ14	71	VDD	84	NC	96	DQ31
60	DQ15	72	RAS#	85	NC	97	Vss
61	DQMB1	73	CAS#	86	Vss	98	SA0
62	Vss	74	RFU	87	DQMB3	99	SA1
		75	CK1			100	SA2

NOTE:

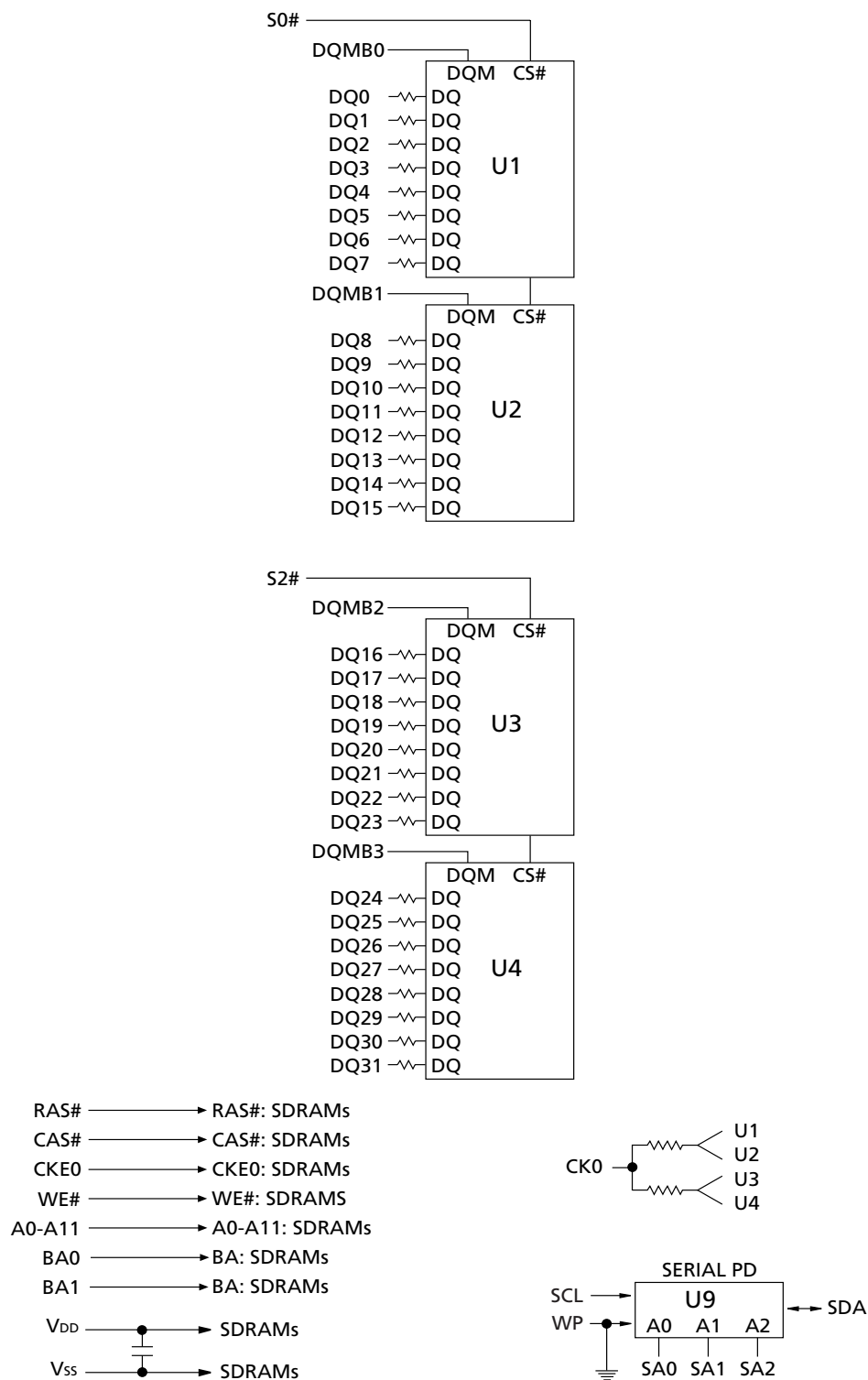
Pin 20 is A12 for 256MB module; for all others NC.

**Figure 2: Pin Locations (100-Pin DIMM)**


**Table 6: Pin Descriptions**

Pin numbers may not correlate with symbols. Refer to the Pin Assignment Tables on page 2 for more information

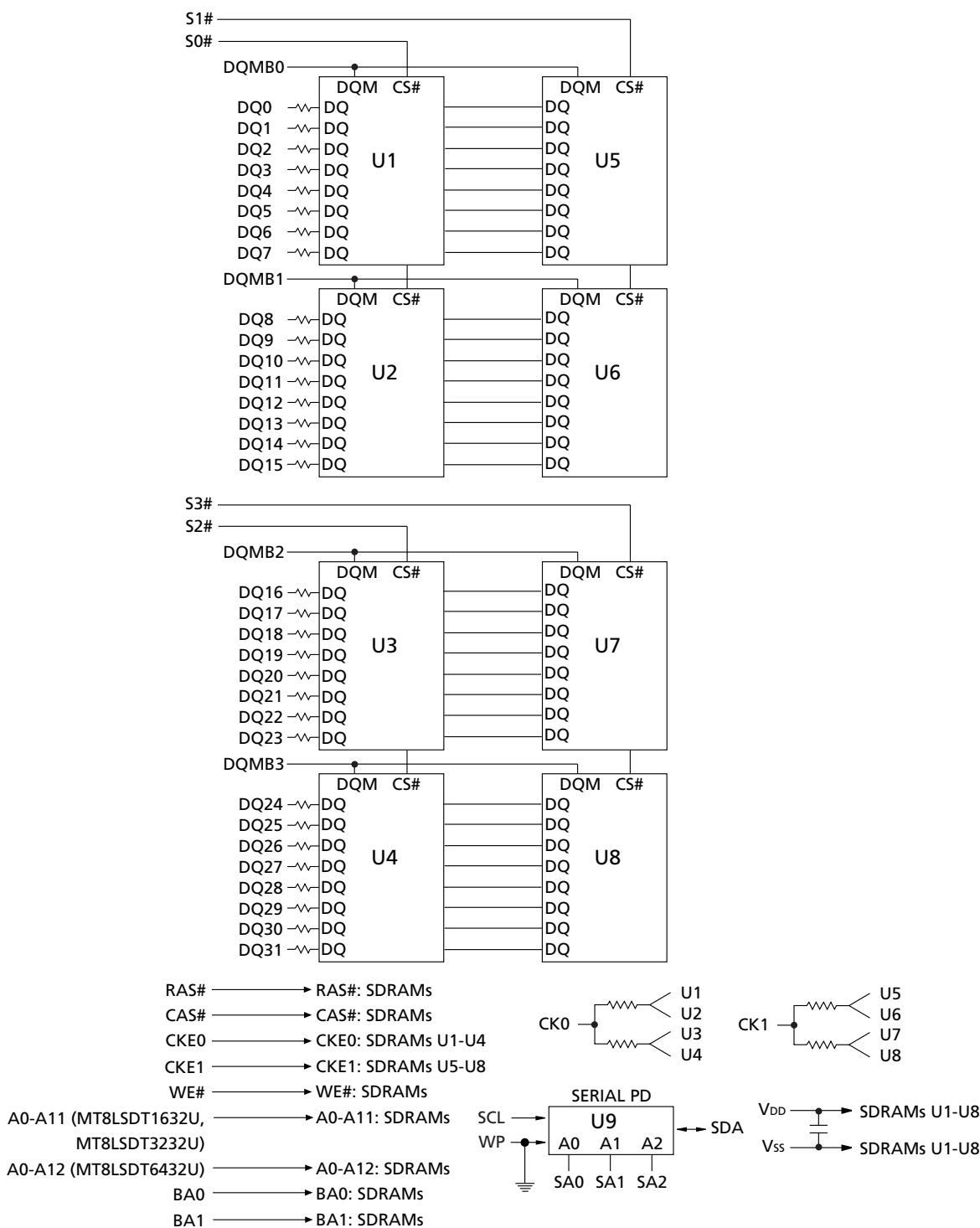
PIN NUMBER	SYMBOL	TYPE	DESCRIPTION
28, 72, 73	WE#, RAS#, CAS#	Input	Command Inputs: RAS#, CAS# and WE# (along with S#) define the command being entered.
25, 75	CK0, CK1	Input	Clock: CK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.
27, 77	CKE0, CKE1	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CK signal. Deactivating the clock provides POWER-DOWN and SELF REFRESH operation (all banks idle), or CLOCK SUSPEND operation (burst access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CK, are disabled during power-down and self refresh modes, providing low standby power.
29, 30, 79, 80	S0#-S3#	Input	Chip Select: S# enables (registered LOW) or disables (registered HIGH) the the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
11, 37, 61, 87	DQMB0-DQMB3	Input	Input/Output Mask: DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (after a two-clock latency) when DQMB is sampled HIGH during a READ cycle.
19, 68	BA0, BA1	Input	Device Bank Address: BA0 and BA1 define to which device bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
13, 14, 15, 16, 17, 18, 20 (256MB), 63, 64, 65, 66, 67, 69	A0-A11 (64MB, 128MB) A0-A12 (256MB)	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
49	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
98-100	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
2-5, 7-10, 38-41, 43-46, 52-55, 57-60, 88-91, 93-96	DQ0-DQ31	Input/Output	Data I/Os: Data bus.
48	SDA	Input/Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
6, 21, 31, 42, 50, 56, 71, 81, 92	VDD	Supply	Power Supply: +3.3V ±0.3V.
1, 12, 26, 36, 47, 51, 62, 76, 86, 97	VSS	Supply	Ground.
23, 24, 74	RFU	–	Reserved for Future Use: These pins should be left unconnected.
20 (64MB, 128MB), 22, 32-35, 70, 78, 82-85	NC	–	Not connected.

**Figure 3: Functional Block Diagram (MT4LSDT1632U)**

**NOTE:**

1. All resistor values are 10Ω unless otherwise specified.
2. Per industry standard, Micron utilizes various component speed grades as referenced in the Module Part Numbering Guide at [www.micron.com/numberguide](http://www.micron.com/numberguide).

SDRAMs – MT48LB16M8A2TG for MT4LSDT1632U

**Figure 4: Functional Block Diagram  
(MT8LSDT1632U, MT8LSDT3232U, and MT8LSDT6432U)**



**NOTE:**

1. All resistor values are 10Ω unless otherwise specified.
2. Per industry standard, Micron utilizes various component speed grades as referenced in the Module Part Numbering Guide at [www.micron.com/numberguide](http://www.micron.com/numberguide).

SDRAMs = MT48LC8M8A2TG for MT8LSDT1632U  
SDRAMs = MT48LC16M8A2TG for MT8LSDT3232U  
SDRAMs = MT48LC32M8A2TG for MT8LSDT6432U

## General Description

The MT4LSDT1632U, MT8LSDT1632U, MT8LSDT3232U, and MT8LSDT6432U are high-speed CMOS, dynamic random-access, 64MB, 128MB and 256MB memory modules organized in a x32 configuration. These modules use SDRAM devices which are internally configured as quad-bank DRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signals).

Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select the device bank, A0–A11 [MT4LSDT1632U, MT8LSDT1632U, and MT8LSDT3232U]; or A0–A12 [MT8LSDT6432U]). The address bits registered coincident with the READ or WRITE command (A0–A8 MT4LSDT1632U; A0–A9 MT8LSDT1632U, MT8LSDT3232U, and MT8LSDT6432U). are used to select the starting device column location for the burst access.

These modules provide for programmable READ or WRITE burst lengths of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. These modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the  $2n$  rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one device bank while accessing one of the other three device banks will hide the PRECHARGE cycles and provide seamless, high-speed, random access operation.

These modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs, outputs, and clocks are LVTTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal device banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 64Mb, 128Mb, or 256Mb SDRAM component data sheets.

## Serial Presence-Detect Operation

These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I<sup>2</sup>C bus using the DIMM's SCL (clock) and SDA (data) signals. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

## Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to VDD and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100μs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100μs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

Once the 100μs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All device banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

## Mode Register Definition

The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in Figure 5, Mode Register Definition Diagram. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.



Mode register bits M0–M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4–M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 and M11 are reserved for future use. For the MT8LSDT6432U module, address A12 (M12) is undefined but should be driven LOW during loading of the mode register.

The mode register must be loaded when all device banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

## Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 5, Mode Register Definition Diagram. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached, as shown in Table 7, Burst Definition Table, on page 8. The block is uniquely selected by A1–A8 (MT8LSDT1632U) or A1–A9 (MT4LSDT1632U, MT8LSDT3232U, and MT8LSDT6432U) when the burst length is set to two; by A2–A8 or A2–A9 when the burst length is set to four; and by A3–A8 or A3–A9 when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached, as shown in Table 7, Burst Definition Table, on page 8.

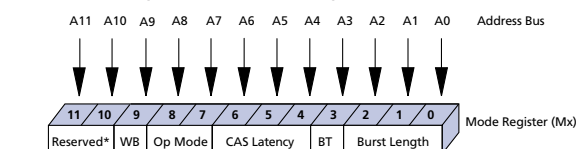
## Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table 7, Burst Definition Table, on page 8.

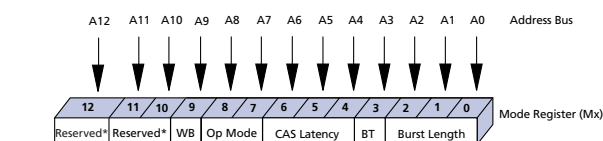
**Figure 5: Mode Register Definition Diagram**

MT4LSDT1632U, MT8LSDT1632U, MT8LSDT3232U



\*Should program M11, M10 = "0, 0" to ensure compatibility with future devices.

MT8LSDT6432U



\*Should program M12, M11, M10 = "0, 0, 0" to ensure compatibility with future devices.

Burst Length			
M2	M1	M0	
0	0	0	M3 = 0: 1
0	0	1	M3 = 1: 2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Full Page

M3	Burst Type
0	Sequential
1	Interleaved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M8	M7	M6-M0	Operating Mode
0	0	Defined	Standard Operation
-	-	-	All other states reserved

M9	Write Burst Mode
0	Programmed Burst Length
1	Single Location Access

**TABLE 7: Burst Definition Table**

BURST LENGTH	STARTING COLUMN ADDRESS	ORDER OF ACCESSES WITHIN A BURST	
		TYPE = SEQUENTIAL	TYPE = INTERLEAVED
2	<b>A0</b>		
	0	0-1	0-1
	1	1-0	1-0
4	<b>A1 A0</b>		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	<b>A2 A1 A0</b>		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-4-5-6-7-0-1-2
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A0-Ai (location 0-y)	Cn, Cn + 1, Cn + 2, Cn + 3, Cn + 4 . . . Cn - 1, Cn . . .	Not supported

NOTE:

- For full-page accesses: y = 512 (MT4LSDT1632U); y = 1,024 (128Mb-based MT8LSDT1632U, MT8LSDT3232U, and MT8LSDT6432U).
- For a burst length of two, A1-Ai select the block-of-two burst; A0 selects the starting column within the block.
- For a burst length of four, A2-Ai select the block-of-four burst; A0-A1 select the starting column within the block.
- For a burst length of eight, A3-Ai select the block-of-eight burst; A0-A2 select the starting column within the block.
- For a full-page burst, the full row is selected and A0-Ai select the starting column.
- Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
- For a burst length of one, A0-Ai select the unique column to be accessed, and mode register bit M3 is ignored.
- i = 8 for MT8LSDT1632U  
i = 9 for MT4LSDT1632U, MT8LSDT3232U, and MT8LSDT6432U

## CAS Latency

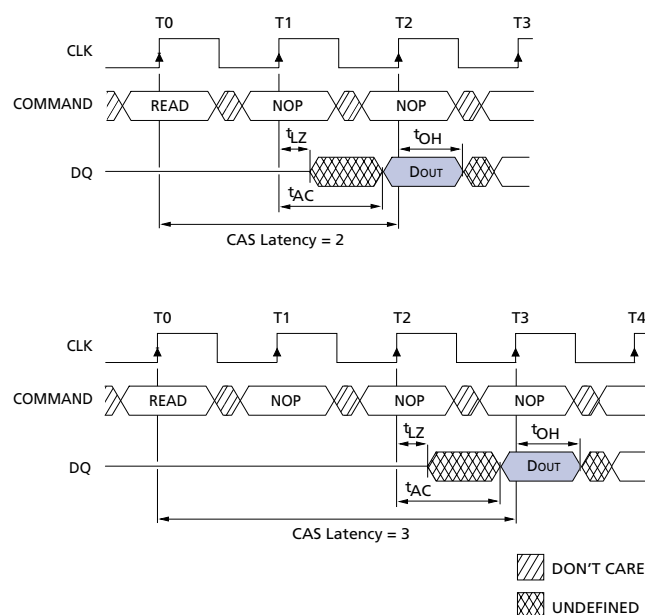
The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge  $n$ , and the latency is  $m$  clocks, the data will be available by clock edge  $n + m$ . The DQs will start driving as a result of the clock edge one cycle earlier ( $n + m - 1$ ), and provided that the relevant access times are met, the data will be valid by clock edge  $n + m$ . For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 6, CAS Latency Diagram. Table 8, CAS Latency Table, indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

## Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

**Figure 6: CAS Latency Diagram**




Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

### **Write Burst Mode**

When M9 = 0, the burst length programmed via M0–M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (non-burst) accesses.

**Table 8: CAS Latency Table**

SPEED	ALLOWABLE OPERATING CLOCK FREQUENCY (MHz)	
	CAS LATENCY = 2	CAS LATENCY = 3
-75	≤ 100	≤ 133
-8	≤ 100	≤ 125
-10	≤ 66	≤ 100

## Commands

Table 9, Truth Table – Commands and DQMB Operation, provides a general reference of available commands. For a more detailed description of commands

and operations, refer to the 64Mb, 128Mb, or 256Mb SDRAM component data sheets.

**Table 9: Truth Table – Commands and DQMB Operation**

Note: 1

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQMB	ADDR	DQ	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select device bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select device bank and column, and start READ burst)	L	H	L	H	L/H <sup>8</sup>	Bank/Col	X	4
WRITE (Select device bank and column, and start WRITE burst)	L	H	L	L	L/H <sup>8</sup>	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in device bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	2
Write Enable/Output Enable	–	–	–	–	L	–	Active	8
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	8

### NOTE:

1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A0–A11 define the op-code written to the Mode Register. For MT8LSDT6432U, A12 should be driven LOW.
3. A0–A11 (MT4LSDT1632U, MT8LSDT1632U, MT8LSDT3232U), or A0–A12 (MT8LSDT6432U) provide row address and BA0 and BA1 determine which device bank is made active.
4. A0–A8 (MT4LSDT1632U) or A0–A9 (MT8LSDT1632U, MT8LSDT3232U, and MT8LSDT6432U) provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0 and BA1 determine which device bank is being read from or written to.
5. A10 LOW: BA0 and BA1 determine which device bank is being precharged. A10 HIGH: both device banks are precharged and BA0 and BA1 are “Don’t Care.”
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
8. Activates or deactivates the DQ during WRITE (zero-clock delay) and READ (two-clock delay).

## Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the opera-

tional sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Voltage on VDD Supply  
Relative to VSS . . . . . -1V to +4.6V  
Voltage on Inputs, NC, or I/O Pins  
Relative to VSS . . . . . -1V to +4.6V  
Operating Temperature  
T<sub>A</sub> (ambient) . . . . . 0°C to +70°C

Storage Temperature (plastic) . . . . . -55°C to +125°C  
Power Dissipation  
(Single Rank) . . . . . 4W  
(Dual Rank) . . . . . 8W

**Table 10: DC Electrical Characteristics and Operating Conditions  
Single-Rank Module**

Notes: 1; notes appear on page 17; all voltages referenced to VSS; VDD = +3.3V ±0.3V

PARAMETER/CONDITION		SYM	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE		VDD	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs		V <sub>IH</sub>	2	VDD + 0.3	V	3
INPUT LOW VOLTAGE: Logic 0; All inputs		V <sub>IL</sub>	-0.3	0.8	V	3
INPUT LEAKAGE CURRENT: Any input 0V ≤ V <sub>IN</sub> ≤ VDD (All other pins not under test = 0V)	WE#, RAS#, CAS#, A0-A11, BA0-BA1, CK, CKE	I <sub>I1</sub>	-20	20	μA	32
	S#	I <sub>I2</sub>	-10	10	μA	32
	DQMB	I <sub>I3</sub>	-5	5	μA	32
OUTPUT LEAKAGE CURRENT: DQ disabled; 0V ≤ V <sub>OUT</sub> ≤ VDD	DQ	I <sub>OZ</sub>	-5	5	μA	32
OUTPUT LEVELS: Output High Voltage (I <sub>OUT</sub> = -4mA) Output Low Voltage (I <sub>OUT</sub> = 4mA)		V <sub>OH</sub>	2.4	–	V	
		V <sub>OL</sub>	–	0.4	V	

**Table 11: DC Electrical Characteristics and Operating Conditions  
Dual-Rank Modules**

Notes: 1; notes appear on page 17; VDD = +3.3V ±0.3V

PARAMETER/CONDITION		SYM	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE		VDD	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs		V <sub>IH</sub>	2	VDD + 0.3	V	3
INPUT LOW VOLTAGE: Logic 0; All inputs		V <sub>IL</sub>	-0.3	0.8	V	3
INPUT LEAKAGE CURRENT: Any input 0V ≤ V <sub>IN</sub> ≤ VDD (All other pins not under test = 0V)	WE#, RAS#, CAS#, A0-A12, BA0-BA1	I <sub>I1</sub>	-40	40	μA	32
	CK, CKE	I <sub>I2</sub>	-20	20	μA	32
	S#, DQMB	I <sub>I3</sub>	-10	10	μA	32
OUTPUT LEAKAGE CURRENT: DQ disabled; 0V ≤ V <sub>OUT</sub> ≤ VDD	DQ	I <sub>OZ</sub>	-10	10	μA	32
OUTPUT LEVELS: Output High Voltage (I <sub>OUT</sub> = -4mA) Output Low Voltage (I <sub>OUT</sub> = 4mA)		V <sub>OH</sub>	2.4	–	V	
		V <sub>OL</sub>	–	0.4	V	

**Table 12: I<sub>DD</sub> Specifications and Conditions: MT4LSDT1632U**

DRAM components only; notes: 1, 5, 6, 11, 13; notes appear on page 17; V<sub>DD</sub> = V<sub>DDQ</sub> = +3.3V ±0.3V

		MAX					
PARAMETER/CONDITION	SYMBOL	-75	-8	-10	UNITS	NOTES	
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; $t_{RC} = t_{RC} \text{ (MIN)}$	I <sub>DD1</sub>	115	600	560	mA	3, 18, 19, 30	
STANDBY CURRENT: Power-Down Mode; all device banks idle; CKE = LOW	I <sub>DD2</sub>	2	8	8	mA	30	
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; all device banks active after $t_{RCD}$ met; no accesses in progress	I <sub>DD3</sub>	45	200	160	mA	3, 12, 19, 30	
OPERATING CURRENT: Burst Mode; continuous burst; READ or WRITE; all device banks active	I <sub>DD4</sub>	140	600	560	mA	3, 18, 19, 30	
AUTO REFRESH CURRENT CKE = HIGH; CS# = HIGH	$t_{RFC} = t_{RFC} \text{ (MIN)}$	I <sub>DD5</sub>	210	1,240	1,080	mA	3, 12
	$t_{RFC} = 15.625\mu\text{s}$	I <sub>DD6</sub>	3	12	12	mA	18, 19, 30, 31
SELF REFRESH CURRENT: CKE ≤ 0.2V	I <sub>DD7</sub>	1	8	8	mA	4	

**Table 13: I<sub>DD</sub> Specifications and Conditions: MT8LSDT1632U**

DRAM components only; notes: 1, 5, 6, 11, 13; notes appear on page 17; V<sub>DD</sub> = V<sub>DDQ</sub> = +3.3V ±0.3V

		MAX					
PARAMETER/CONDITION	SYMBOL	-75	-8	-10	UNITS	NOTES	
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; $t_{RC} = t_{RC} \text{ (MIN)}$	I <sub>DD1</sub> <sup>a</sup>	115	468	388	mA	3, 18, 19, 30	
STANDBY CURRENT: Power-Down Mode; all device banks idle; CKE = LOW	I <sub>DD2</sub> <sup>b</sup>	2	16	16	mA	30	
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; all device banks active after $t_{RCD}$ met; no accesses in progress	I <sub>DD3</sub> <sup>a</sup>	45	188	148	mA	3, 12, 19, 30	
OPERATING CURRENT: Burst Mode; continuous burst; READ or WRITE; all device banks active	I <sub>DD4</sub> <sup>a</sup>	140	568	488	mA	3, 18, 19, 30	
AUTO REFRESH CURRENT CKE = HIGH; CS# = HIGH	$t_{RFC} = t_{RFC} \text{ (MIN)}$	I <sub>DD5</sub> <sup>b</sup>	210	1,680	1,520	mA	3, 12
	$t_{RFC} = 15.625\mu\text{s}$	I <sub>DD6</sub> <sup>b</sup>	3	24	24	mA	18, 19, 30, 31
SELF REFRESH CURRENT: CKE ≤ 0.2V	I <sub>DD7</sub> <sup>b</sup>	1	8	8	mA	4	

**NOTE:**

- a - Value calculated as one module rank in this operating condition, and all other module ranks in power-down mode.
- b - Value calculated reflects all module ranks in this operating condition.

**Table 14: I<sub>DD</sub> Specifications and Conditions: MT8LSDT3232U**

DRAM components only; notes: 1, 5, 6, 11, 13; notes appear on page 17; V<sub>DD</sub>, V<sub>DDQ</sub> = +3.3V ±0.3V

PARAMETER/CONDITION		SYMBOL	MAX			UNITS	NOTES
			-75	-8	-10		
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; t <sub>RC</sub> = t <sub>RC</sub> (MIN)		I <sub>DD1</sub> <sup>a</sup>	150	608	568	mA	3, 18, 19, 30
STANDBY CURRENT: Power-Down Mode; all device banks idle; CKE = LOW		I <sub>DD2</sub> <sup>b</sup>	2	16	16	mA	30
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; all device banks active after t <sub>RCD</sub> met; no accesses in progress		I <sub>DD3</sub> <sup>a</sup>	50	208	168	mA	3, 12, 19, 30
OPERATING CURRENT: Burst Mode; continuous burst; READ or WRITE; all device banks active		I <sub>DD4</sub> <sup>a</sup>	150	608	568	mA	3, 18, 19, 30
AUTO REFRESH CURRENT CKE = HIGH; CS# = HIGH	t <sub>RFC</sub> = t <sub>RFC</sub> (MIN)	I <sub>DD5</sub> <sup>b</sup>	310	2,480	2,160	mA	3, 12
	t <sub>RFC</sub> = 15.625μs	I <sub>DD6</sub> <sup>b</sup>	3	24	24	mA	18, 19, 30, 31
SELF REFRESH CURRENT: CKE ≤ 0.2V		I <sub>DD7</sub> <sup>b</sup>	2	16	16	mA	4

NOTE:

- a - Value calculated as one module rank in this operating condition, and all other module ranks in power-down mode.
- b - Value calculated reflects all module ranks in this operating condition.

**Table 15: I<sub>DD</sub> Specifications and Conditions: MT8LSDT6432U**

DRAM components only; notes: 1, 5, 6, 11, 13; notes appear on page 17; V<sub>DD</sub>, V<sub>DDQ</sub> = +3.3V ±0.3V

PARAMETER/CONDITION		SYMBOL	MAX			UNITS	NOTES
			-75	-8	-10		
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; t <sub>RC</sub> = t <sub>RC</sub> (MIN)		I <sub>DD1</sub> <sup>a</sup>	125	508	508	mA	3, 18, 19, 30
STANDBY CURRENT: Power-Down Mode; all device banks idle; CKE = LOW		I <sub>DD2</sub> <sup>b</sup>	2	16	16	mA	30
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; all device banks active after t <sub>RCD</sub> met; no accesses in progress		I <sub>DD3</sub> <sup>a</sup>	40	168	168	mA	3, 12, 19, 30
OPERATING CURRENT: Burst Mode; continuous burst; READ or WRITE; all device banks active		I <sub>DD4</sub> <sup>a</sup>	135	548	548	mA	3, 18, 19, 30
AUTO REFRESH CURRENT CKE = HIGH; CS# = HIGH	t <sub>RFC</sub> = t <sub>RFC</sub> (MIN)	I <sub>DD5</sub> <sup>b</sup>	270	2,160	2,160	mA	3, 12
	t <sub>RFC</sub> = 7.8125μs	I <sub>DD6</sub> <sup>b</sup>	3.5	28	28	mA	18, 19, 30, 31
SELF REFRESH CURRENT: CKE ≤ 0.2V		I <sub>DD7</sub> <sup>b</sup>	2.5	20	20	mA	4

NOTE:

- a - Value calculated as one module rank in this operating condition, and all other module ranks in power-down mode.
- b - Value calculated reflects all module ranks in this operating condition.

**Table 16: Capacitance (Single-Rank Module)**

Note: 1; this parameter is sampled; VDD = +3.3V; f = 1 MHz

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Capacitance: A0-A11, BA0, BA1, RAS#, CAS#, WE#, CE	C <sub>I1</sub>	10	15.2	pF
Input Capacitance: CK	C <sub>I2</sub>	10	14	pF
Input Capacitance: S#	C <sub>I3</sub>	5	7.6	pF
Input Capacitance: DQMB#	C <sub>I4</sub>	2.5	3.8	pF
Input Capacitance: SCL, SA	C <sub>I5</sub>	–	6	pF
Input/Output Capacitance: DQ0-DQ31, SDA	C <sub>IO</sub>	4	6	pF

**Table 17: Capacitance (Dual-Rank Modules)**

Note: 1; this parameter is sampled; VDD = +3.3V; f = 1 MHz

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Capacitance: A0-A11/A12, BA0, BA1, RAS#, CAS#, WE#	C <sub>I1</sub>	20	30.4	pF
Input Capacitance: CE	C <sub>I2</sub>	10	15.2	pF
Input Capacitance: CK	C <sub>I3</sub>	10	14	pF
Input Capacitance: S#, DQMB#	C <sub>I4</sub>	5	7.6	pF
Input Capacitance: SCL, SA0-SA2	C <sub>I5</sub>	–	6	pF
Input/Output Capacitance: DQ0-DQ31, SDA	C <sub>IO</sub>	8	12	pF



**Table 18: SDRAM Component AC Electrical Characteristics**

Notes: 1–5; notes appear on page 17; SDRAM component specifications

PARAMETER	SYMBOL	-75		-8		-10		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Access time from CLK (positive edge)	CL = 3	$t_{AC}$	5.4		6		7.5	ns	
	CL = 2	$t_{AC}$	6		6		9	ns	
Address hold time		$t_{AH}$	0.8	1		1		ns	
Address setup time		$t_{AS}$	1.5	2		2		ns	
CLK high-level width		$t_{CH}$	2.5	3		3		ns	
CLK low-level width		$t_{CL}$	3	3		3		ns	
Clock cycle time	CL = 3	$t_{CK}$	7.5	8		10		ns	6
	CL = 2	$t_{CK}$	10	10		15		ns	6
CKE hold time		$t_{CKH}$	0.8	1		1		ns	
CKE setup time		$t_{CKS}$	1.5	2		2		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		$t_{CMH}$	0.8	1		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		$t_{CMS}$	1.5	2		2		ns	
Data-in hold time		$t_{DH}$	0.8	1		1		ns	
Data-in setup time		$t_{DS}$	1.5	2		2		ns	
Data-out high-impedance time	CL = 3	$t_{HZ}$	5.4		6		8	ns	7
	CL = 2	$t_{HZ}$	6		7		10	ns	7
Data-out low-impedance time		$t_{LZ}$	1	1		2			
Data-out hold time (load)		$t_{OH}$	3	3		3		ns	7
Data-out hold time (no load)		$t_{OHn}$	1.8	1.8		1.8		ns	7
ACTIVE to PRECHARGE command period		$t_{RAS}$	44	120,000	50	120,000	60	120,000	ns
ACTIVE to ACTIVE command period		$t_{RC}$	66		70		90		ns
AUTO REFRESH period		$t_{RCAR}$	20		70		90		ns
ACTIVE to READ or WRITE delay		$t_{RCD}$	15		20		30		ns
Refresh period (4,096 cycles)		$t_{REF}$		64		64		64	ns
PRECHARGE command period		$t_{RP}$	20		20		30		ns
ACTIVE bank A to ACTIVE bank B command period		$t_{RRD}$	20		20		20		ns
Transition time		$t_T$	0.3	1.2	0.3	1.2	1	1.2	ms
WRITE recovery time		$t_{WR}$	1 CLK + 7ns		1 CLK + 7ns		1 CLK + 7n		ns
			15		15		15		ns
Exit SELF REFRESH to ACTIVE command		$t_{XSR}$	75		80		90		ns

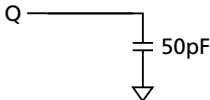
**Table 19: AC Functional Characteristics**

Notes: 1–5; notes appear on page 17

PARAMETER		SYMBOL	-75	-8	-10	UNITS	NOTES
READ/WRITE command to READ/WRITE command		$t_{CCD}$	1	1	1	$t_{CK}$	6
CKE to clock disable or power-down entry mode		$t_{CKED}$	1	1	1	$t_{CK}$	7
CKE to clock enable or power-down exit setup mode		$t_{PED}$	1	1	1	$t_{CK}$	7
DQM to input data delay		$t_{DQD}$	0	0	0	$t_{CK}$	6
DQM to data mask during WRITES		$t_{DQM}$	0	0	0	$t_{CK}$	6
DQM to data high-impedance during READs		$t_{DQZ}$	2	2	2	$t_{CK}$	6
WRITE command to input data delay		$t_{DWD}$	0	0	0	$t_{CK}$	6
Data-in to ACTIVATE command		$t_{DAL}$	5	4	4	$t_{CK}$	8, 9
Data-in to precharge		$t_{DPL}$	2	2	2	$t_{CK}$	9, 10
Last data-in to BURST STOP command		$t_{BDL}$	1	1	1	$t_{CK}$	6
Last data-in to new READ/WRITE command		$t_{CDL}$	1	1	1	$t_{CK}$	6
Last data-in to PRECHARGE command		$t_{RDL}$	2	2	2	$t_{CK}$	9, 10
LOAD MODE REGISTER command to ACTIVE or REFRESH command		$t_{MRD}$	2	2	2	$t_{CK}$	11
Data-out to high-impedance from PRECHARGE command	CL = 3	$t_{ROH}$	3	3	3	$t_{CK}$	6
	CL = 2	$t_{ROH}$	2	2	2	$t_{CK}$	6

## Notes

1. All voltages referenced to VSS.
2. This parameter is sampled. VDD, VDDQ = +3.3V; f = 1 MHz; T<sub>A</sub> = 25°C; pin under test biased at 1.4V.
3. IDD is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured (0°C ≤ T<sub>A</sub> ≤ +70°C).
6. An initial pause of 100μs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (VDD and VDDQ must be powered up simultaneously. VSS and VSSQ must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the t<sub>REF</sub> refresh requirement is exceeded.
7. AC characteristics assume t<sub>T</sub> = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between V<sub>IH</sub> and V<sub>IL</sub> (or between V<sub>IL</sub> and V<sub>IH</sub>) in a monotonic manner.
9. Outputs measured at 1.5V with equivalent load:
 


10. t<sub>HZ</sub> defines the time at which the output achieves the open circuit condition; it is not a reference to V<sub>OH</sub> or V<sub>OL</sub>. The last valid data element will meet t<sub>OH</sub> before going High-Z.
11. AC timing and IDD tests have V<sub>IL</sub> = 0V and V<sub>IH</sub> = 3V, with timing referenced to 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at V<sub>IL</sub> (MAX) and V<sub>IH</sub> (MIN) and no longer at the ISV crossover point.
12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V<sub>IH</sub> or V<sub>IL</sub> levels.
13. IDD specifications are tested after the device is properly initialized.
14. Timing actually specified by t<sub>CKS</sub>; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by t<sub>WR</sub> plus t<sub>RP</sub>; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by t<sub>WR</sub>.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The IDD current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on t<sub>CK</sub> = 10ns for -10; t<sub>CK</sub> = 7.5ns for -8.
22. V<sub>IH</sub> overshoot: V<sub>IH</sub> (MAX) = VDDQ + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V<sub>IL</sub> undershoot: V<sub>IL</sub> (MIN) = -2V for a pulse width ≤ 3ns.
23. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including t<sub>WR</sub>, and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only. The precharge timing budget (t<sub>RP</sub>) begins 7.5ns for -8; and 7ns for -10 after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.
25. Precharge mode only.
26. JEDEC and PC100 specify three clocks.
27. t<sub>AC</sub> for -9 at CL = 3 with no load is 4.6ns and is guaranteed by design.
28. Parameter guaranteed by design.
29. For -8, CL = 3 and t<sub>CK</sub> = 7.5ns; for -10, CL = 2 and t<sub>CK</sub> = 10ns.
30. CKE is HIGH during refresh command period t<sub>RFC</sub> (MIN), otherwise CKE is LOW. The IDD6 limit is actually a nominal value and does not result in a fail value.
31. Refer to device data sheet for timing waveforms.
32. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.

## SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (as shown in Figure 7, Data Validity, and Figure 8, Definition of Start and Stop).

### SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

### SPD Stop Condition

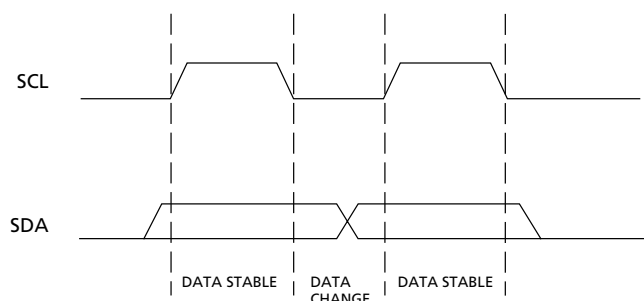
All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

## SPD Acknowledge

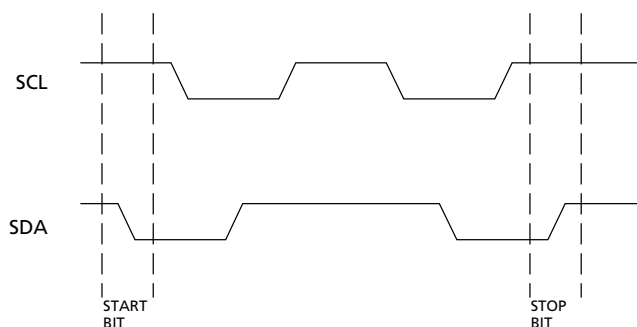
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (as shown in Figure 9, Acknowledge Response from Receiver).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode, the SPD device will transmit eight bits of data, release the SDA line, and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

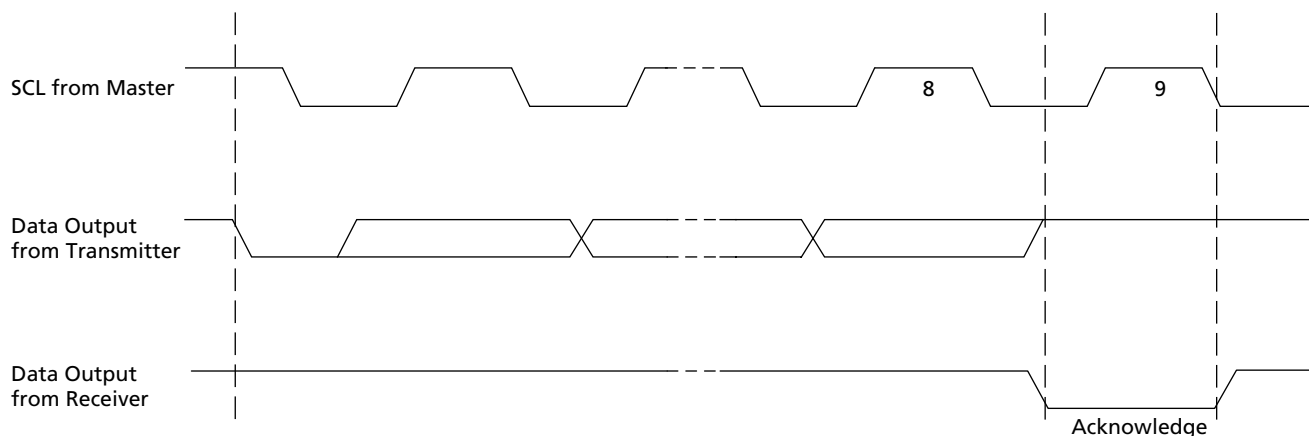
**Figure 7: Data Validity**



**Figure 8: Definition of Start and Stop**



**Figure 9: Acknowledge Response from Receiver**



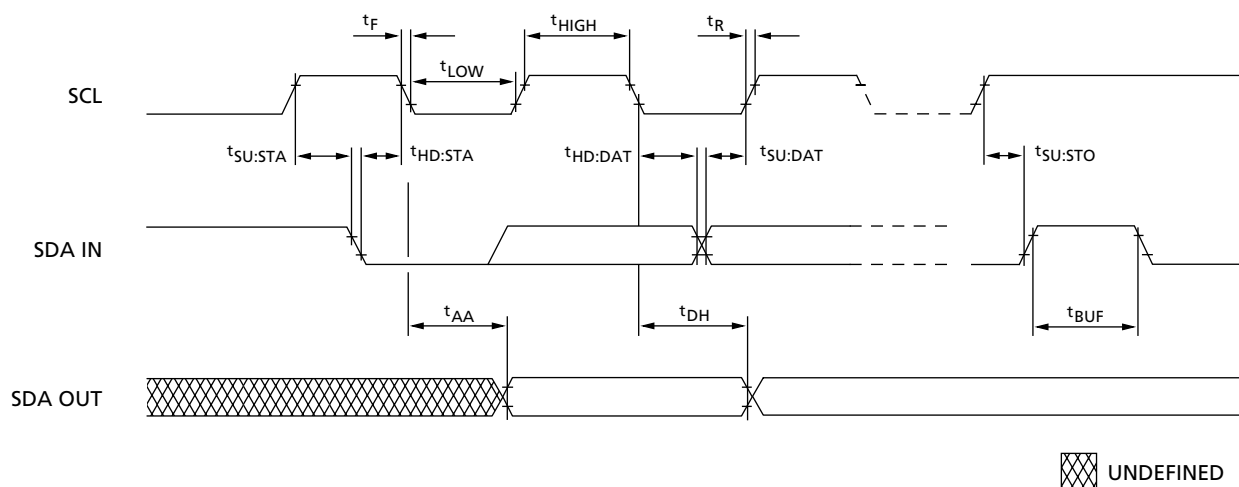
**Table 20: EEPROM Device Select Code**

Most significant bit (b7) is sent first

SELECT CODE	DEVICE TYPE IDENTIFIER				CHIP ENABLE			R $\overline{W}$
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	SA2	SA1	SA0	R $\overline{W}$
Protection Register Select Code	0	1	1	0	SA2	SA1	SA0	R $\overline{W}$

**Table 21: EEPROM Operating Modes**

MODE	R $\overline{W}$ BIT	W $\overline{C}$	BYTES	INITIAL SEQUENCE
Current Address Read	1	V <sub>IH</sub> or V <sub>IL</sub>	1	Start, Device Select, R $\overline{W}$ = 1
RandomAddressRead	0	V <sub>IH</sub> or V <sub>IL</sub>	1	Start, Device Select, R $\overline{W}$ = 0, Address
	1	V <sub>IH</sub> or V <sub>IL</sub>		RESTART, Device Select, R $\overline{W}$ = 1
Sequential Read	1	V <sub>IH</sub> or V <sub>IL</sub>	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V <sub>IL</sub>	1	START, Device Select, R $\overline{W}$ = 0
Page Write	0	V <sub>IL</sub>	≤ 16	START, Device Select, R $\overline{W}$ = 0

**Figure 10: SPD EEPROM**


**Table 22: Serial Presence-Detect EEPROM DC Operating Conditions**

All voltages referenced to V<sub>SS</sub>; V<sub>DD</sub> = +3.3V ±0.3V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	V <sub>DD</sub>	3	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	V <sub>IH</sub>	V <sub>DD</sub> x 0.7	V <sub>DD</sub> + 0.5	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V <sub>IL</sub>	-1	V <sub>DD</sub> x 0.3	V
OUTPUT LOW VOLTAGE: I <sub>OUT</sub> = 3mA	V <sub>OL</sub>	–	0.4	V
INPUT LEAKAGE CURRENT: V <sub>IN</sub> = GND to V <sub>DD</sub>	I <sub>LI</sub>	–	10	μA
OUTPUT LEAKAGE CURRENT: V <sub>OUT</sub> = GND to V <sub>DD</sub>	I <sub>LO</sub>	–	10	μA
STANDBY CURRENT: SCL = SDA = V <sub>DD</sub> - 0.3V; All other inputs = V <sub>DD</sub> or V <sub>SS</sub>	I <sub>SB</sub>	–	30	μA
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I <sub>DD</sub>	–	2	mA

**Table 23: Serial Presence-Detect EEPROM AC Electrical Characteristics**

All voltages referenced to V<sub>SS</sub>; V<sub>DD</sub> = +3.3V ±0.3V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	t <sub>AA</sub>	0.3	3.5	μs	
Time the bus must be free before a new transition can start	t <sub>BUF</sub>	4.7		μs	
Data-out hold time	t <sub>DH</sub>	300		ns	
SDA and SCL fall time	t <sub>F</sub>		300	ns	
Data-in hold time	t <sub>HD:DAT</sub>	0		μs	
Start condition hold time	t <sub>HD:STA</sub>	4		μs	
Clock HIGH period	t <sub>HIGH</sub>	4		μs	
Noise suppression time constant at SCL, SDA inputs	t <sub>I</sub>		100	ns	
Clock LOW period	t <sub>LOW</sub>	4.7		μs	
SDA and SCL rise time	t <sub>R</sub>		1	μs	
SCL clock frequency	t <sub>SCL</sub>		100	KHz	
Data-in setup time	t <sub>SU:DAT</sub>	250		ns	
Start condition setup time	t <sub>SU:STA</sub>	4.7		μs	
Stop condition setup time	t <sub>SU:STO</sub>	4.7		μs	
WRITE cycle time	t <sub>WRC</sub>		10	ms	1

NOTE:

1. The SPD EEPROM WRITE cycle time (t<sub>WRC</sub>) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to the pull-up resistor, and the EEPROM does not respond to its slave address.



**Table 24: Serial Presence-Detect Matrix**

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

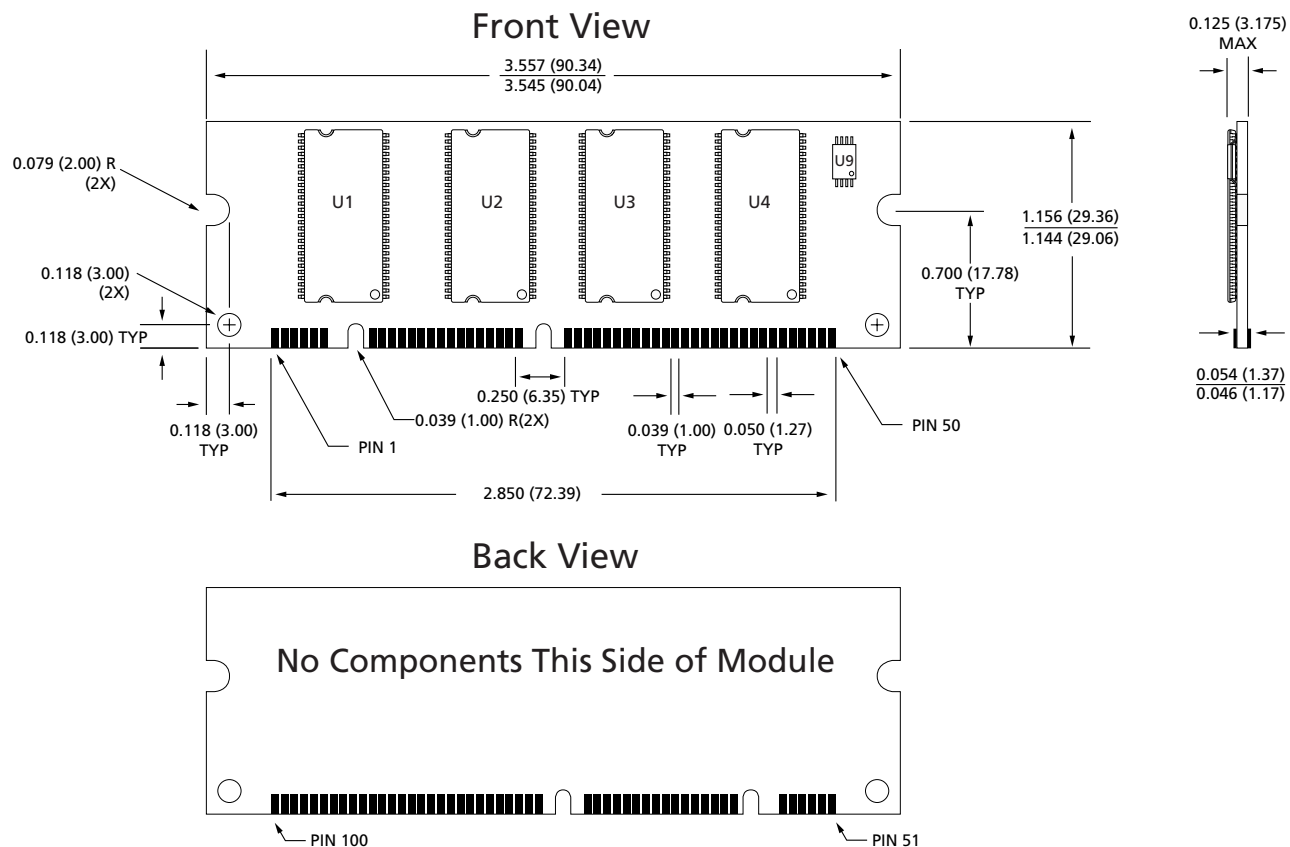
BYTE	DESCRIPTION	ENTRY (VERSION)	MT4LSDT1632U	MT8LSDT1632U	MT8LSDT3232U	MT8LSDT6432U
0	Number of Bytes Used By Micron	128	80	80	80	80
1	Total Number of SPD Memory Bytes	256	08	08	08	08
2	Memory Type	SDRAM	04	04	04	04
3	Number of Row Addresses	12 or 13	0C	0C	0C	0D
4	Number of Column Addresses	9 or 10	A0	09	0A	0A
5	Number of Module Ranks	1 or 2	01	02	02	02
6	Module Data Width	32	20	20	20	20
7	Module Data Width (Continued)	0	00	00	00	00
8	Module Voltage Interface Levels	LVTTL	01	01	01	01
9	SDRAM Cycle Time, $t_{CK}$ (CAS Latency = 3)	10ns (-10) 8ns (-8) 7.5ns (-75)	A0 80 75	A0 80 75	A0 80 75	A0 80 75
10	SDRAM Access From Clock, $t_{AC}$ , (CAS Latency = 3)	7.5ns (-10) 6ns (-8) 7.5ns (-75)	75 60 54	75 60 54	75 60 54	75 60 54
11	Module Configuration Type	None	00	00	00	00
12	Refresh Rate/type	15.62 $\mu$ s or 7.81 $\mu$ s/Self	80	80	80	82
13	SDRAM Width (Primary SDRAM)	8	08	08	08	08
14	Error-checking SDRAM Data Width	0	00	00	00	00
15	Minimum Clock Delay, $t_{CCD}$	1 $t_{CK}$	01	01	01	01
16	Burst Lengths Supported	1, 2, 4, 8, Page	8F	8F	8F	8F
17	Number of Banks on SDRAM Device	4	04	04	04	04
18	CAS Latencies Supported	2, 3	06	06	06	06
19	CS Latency	0	01	01	01	01
20	WE Latency	0	01	01	01	01
21	SDRAM Module Attributes	Unbuffered	00	00	00	00
22	SDRAM Device Attributes: General	Attributes	0E	0E	0E	0E
23	SDRAM Cycle Time, $t_{CK}$ (CAS Latency = 2)	15ns (-10) 10ns (-8, -75)	F0 A0	F0 A0	F0 A0	F0 A0
24	SDRAM Access From Clock, $t_{AC}$ , (CAS Latency = 2)	9ns (-10) 6ns (-8, -75)	90 60	90 60	90 60	90 60
25	SDRAM Cycle Time, $t_{CK}$ (CAS Latency = 1)	Not Supported	00	00	00	00
26	SDRAM Access From Clock, $t_{AC}$ , (CAS Latency = 1)	Not Supported	00	00	00	00
27	Minimum Row Precharge Time, $t_{RP}$	30ns (-10) 20ns (-8, -75)	1E 14	1E 14	1E 14	1E 14

**Table 24: Serial Presence-Detect Matrix (Continued)**

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

BYTE	DESCRIPTION	ENTRY (VERSION)	MT4LSDT1632U	MT8LSDT1632U	MT8LSDT3232U	MT8LSDT6432U
28	Minimum Row Active To Row Active, <sup>t</sup> RRD	20ns (-10, -8) 15ns (-75)	14 0F	14 0F	14 0F	14 0F
29	Minimum RAS# to CAS# Delay, <sup>t</sup> RCD	30ns (-10) 20ns (-8, -75)	1E 14	1E 14	1E 14	1E 14
30	Minimum RAS# Pulse Width, <sup>t</sup> RAS	60ns (-10) 50ns (-8) 44ns (-75)	3C 32 2C	3C 32 2C	3C 32 2C	3C 32 2C
31	Module Rank Density	32MB 64MB 128MB	10	8	10	20
32	Command/Address Setup, <sup>t</sup> AS	2ns (-10, -8) 1.5ns (-75)	20 15	20 15	20 15	20 15
33	Command/Address Hold, <sup>t</sup> AH	1ns (-10, -8) 0.8ns (-75)	10 8	10 8	10 8	10 8
34	Data Signal Input Setup, <sup>t</sup> DS	2ns (-10, -8) 1.5ns (-75)	20 15	20 15	20 15	20 15
35	Data Signal Input Hold, <sup>t</sup> DH	1ns (-10, -8) 0.8ns (-75)	10 8	10 8	10 8	10 8
36-61	RESERVED BYTES	—	00	00	00	00
62	SPD Revision	REV. 2	02	02	02	02
63	Checksum for Bytes 0-62	(-10) (-8) (-75)	89 B6 6E	81 AE 66	8A B7 6F	9D CA 82
64	Manufacturer's JEDEC ID Code	MICRON		2C	2C	2C
65-71	Manufacturer's JEDEC ID Code (Cont.)			FF	FF	FF
72	Manufacturing Location	1-11		01-0B	01-0B	01-0B
73-90	Module Part Number (ASCII)			Variable Data	Variable Data	Variable Data
91	PCB Identification Code	1-9		01-09	01-09	01-09
92	Identification Code (Cont.)	0		00	00	00
93	Year of Manufacture in BCD			Variable Data	Variable Data	Variable Data
94	Week of Manufacture in BCD			Variable Data	Variable Data	Variable Data
95-98	Module Serial Number			Variable Data	Variable Data	Variable Data
99-127	Manufacturer-Specific Data (RSVD)			—	—	—

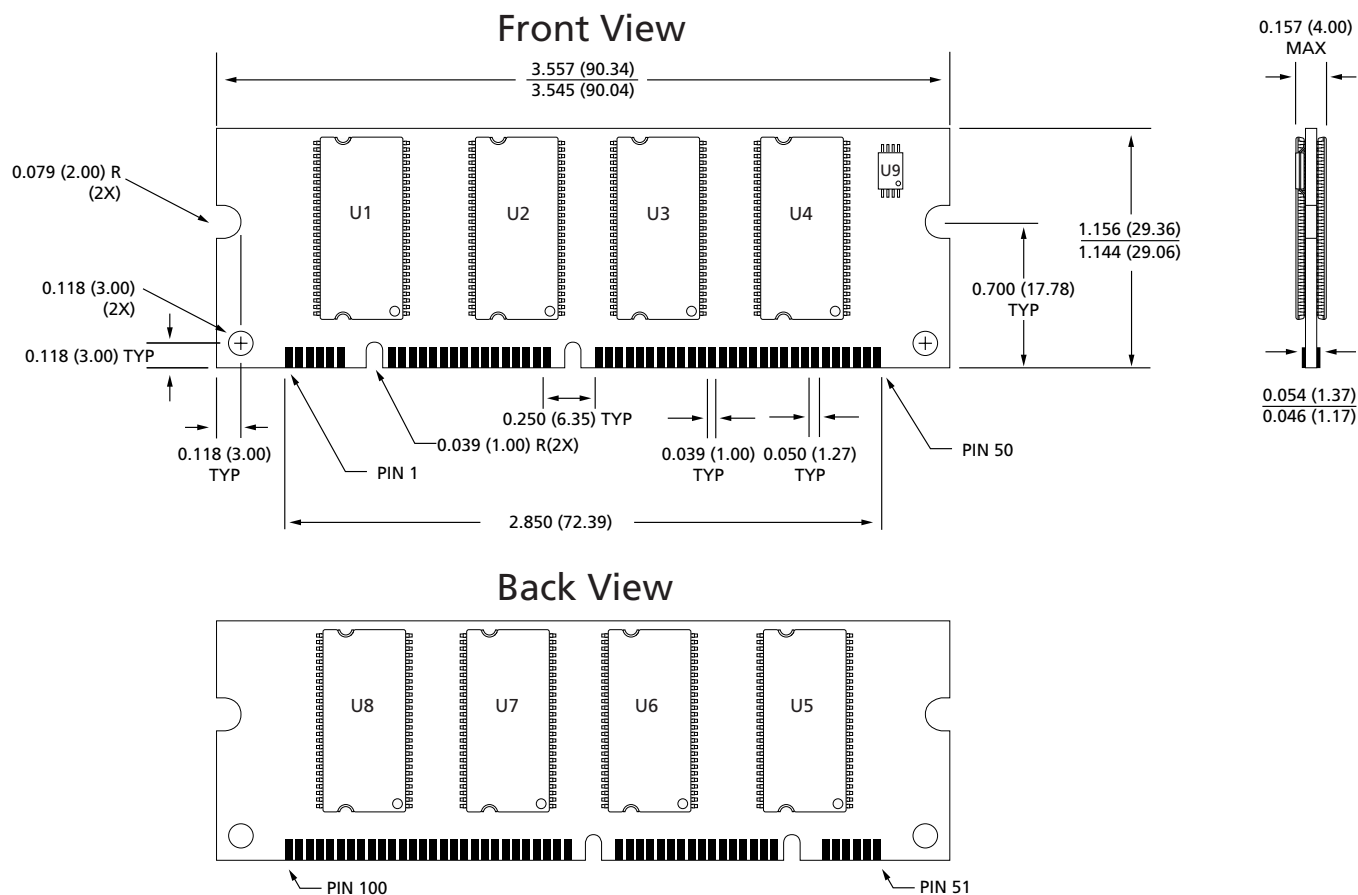
**Figure 11: Single-Rank 100-Pin DIMM Dimensions  
MT4LSDT1632U**



**NOTE:**

All dimensions in inches (millimeters)  $\frac{\text{MAX}}{\text{MIN}}$  or typical where noted.

**Figure 12: Dual Rank 100-Pin DIMM Dimensions**  
**MT8LSDT1632U, MT8LSDT3232U, MT8LSDT6432U**



NOTE:

All dimensions in inches (millimeters)  $\frac{\text{MAX}}{\text{MIN}}$  or typical where noted.

## Data Sheet Designation

**Released (No Mark):** This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices.

Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.



8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900

E-mail: [prodmktg@micron.com](mailto:prodmktg@micron.com), Internet: <http://www.micron.com>, Customer Comment Line: 800-932-4992

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