# SYNCHRONOUS DRAM MODULE

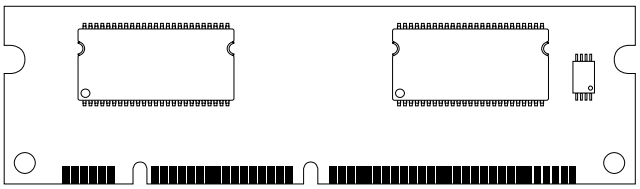
## MT2LSDT132U - 4MB
## MT4LSDT232UD - 8MB

*For the latest data sheet, please refer to the Micron® Web site: www.micron.com/moduleds*

### Features

- JEDEC pinout in a 100-pin, dual in-line memory module (DIMM)
- 4MB (1 Meg x32) and 8MB (2 Meg x32)
- Utilizes 100 MHz and 125 MHz SDRAM components
- Single +3.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal SDRAM device pipelined operation, compatible with 2*n* prefetch architecture, allows column address changes every clock cycle
- Internal SDRAM device banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge and Auto Refresh Modes
  64ms, 2,048-cycle refresh (31.25µs refresh interval for power saving); or 64ms, 2,048-cycle refresh (15.625µs refresh interval)
- LVTTL-compatible inputs and outputs
- Serial Presence-Detect (SPD)

### Figure 1: 100-Pin DIMM (MO–161)



| OPTIONS | MARKING |
|---|---|
| • Package | |
| 100-pin DIMM (Gold) | G |
| 100-pin DIMM (Lead-free) | Y |
| • Frequency / CAS Latency | |
| 125 MHz (8ns) / CL = 3 | -8 |
| 100 MHz (10ns) / CL = 2 | -10 |

### Table 1: Timing Parameters

CL = CAS (READ) latency

| MODULE MARKING | CLOCK FREQUENCY | ACCESS TIME | | SETUP TIME | HOLD TIME |
|---|---|---|---|---|---|
| | | CL = 2 | CL = 3 | | |
| -8 | 125 MHz | – | 6ns | 2ns | 1ns |
| -10 | 100 MHz | 10ns | – | 2ns | 1ns |

### Table 2: Part Numbers

| PART NUMBER | CONFIGURATION | SYSTEM BUS SPEED |
|---|---|---|
| MT2LSDT132UG-8_ | 1 Meg x32 | 125 MHz |
| MT2LSDT132UY-8_ | 1 Meg x32 | 125 MHz |
| MT2LSDT132UG-10_ | 1 Meg x32 | 100 MHz |
| MT2LSDT132UY-10_ | 1 Meg x32 | 100 MHz |
| MT4LSDT232UDG-8_ | 2 Meg x32 | 125 MHz |
| MT4LSDT232UDY-8_ | 2 Meg x32 | 125 MHz |
| MT4LSDT232UDG-10_ | 2 Meg x32 | 100 MHz |
| MT4LSDT232UDY-10_ | 2 Meg x32 | 100 MHz |

### Table 3: Address Table

| MODULE DENSITY | 4MB | 8MB |
|---|---|---|
| Refresh Count | 2K or 4K | 2K or 4K |
| Device Banks | 2 (BA0) | 2 (BA0) |
| Device Configuration | 1 Meg x 16 | 1 Meg x 16 |
| Device Row Addressing | 2K (A0 - A10) | 2K (A0 - A10) |
| Device Column Addressing | 256 (A0 - A7) | 256 (A0 - A7) |
| Module Ranks | 1 (S0#, S2#) | 2 (S0#, S2#; S1#, S3#) |

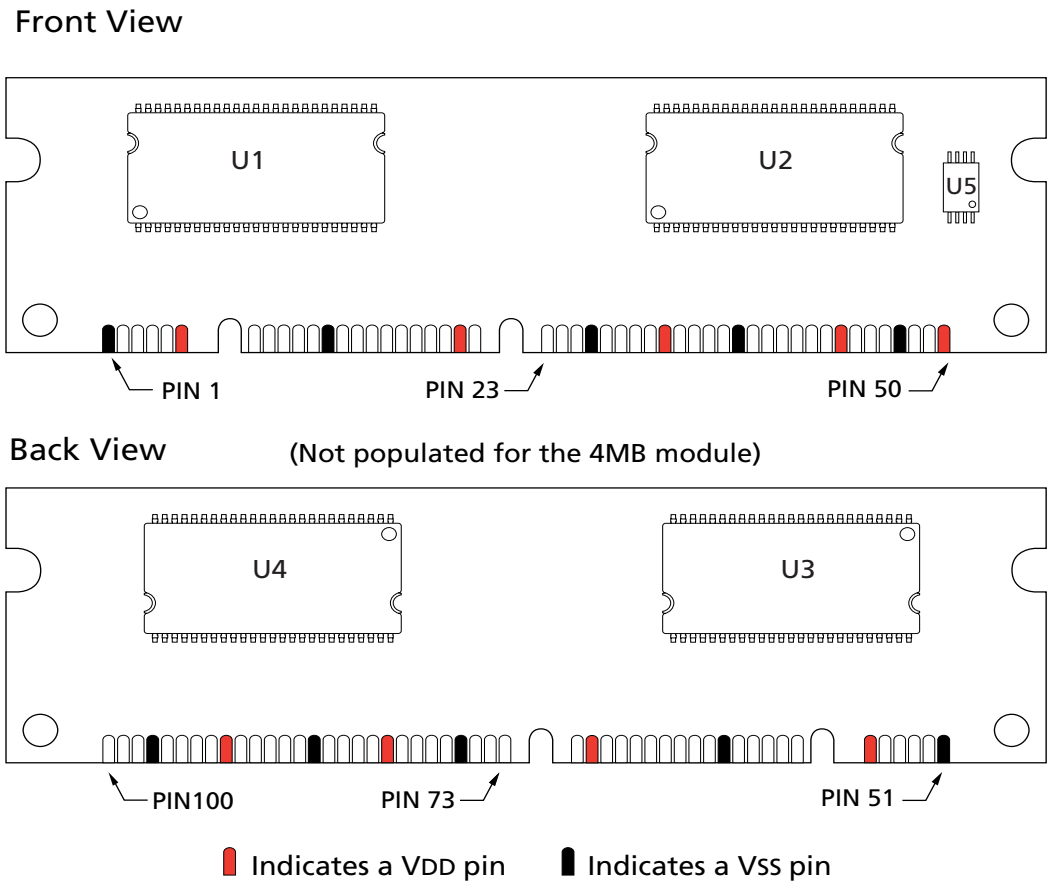
## Table 4: Pin Assignment Front (100-Pin DIMM)

| PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL |
|---|---|---|---|---|---|---|---|
| 1 | Vss | 13 | A0 | 26 | Vss | 38 | DQ16 |
| 2 | DQ0 | 14 | A2 | 27 | CKE0 | 39 | DQ17 |
| 3 | DQ1 | 15 | A4 | 28 | WE# | 40 | DQ18 |
| 4 | DQ2 | 16 | A6 | 29 | S0# | 41 | DQ19 |
| 5 | DQ3 | 17 | A8 | 30 | S2# | 42 | VDD |
| 6 | VDD | 18 | A10 | 31 | VDD | 43 | DQ20 |
| 7 | DQ4 | 19 | NC | 32 | NC | 44 | DQ21 |
| 8 | DQ5 | 20 | NC | 33 | NC | 45 | DQ22 |
| 9 | DQ6 | 21 | VDD | 34 | NC | 46 | DQ23 |
| 10 | DQ7 | 22 | NC | 35 | NC | 47 | Vss |
| 11 | DQMB0 | 23 | RFU | 36 | Vss | 48 | SDA |
| 12 | Vss | 24 | RFU | 37 | DQMB2 | 49 | SCL |
| | | 25 | CK0 | | | 50 | VDD |

## Table 5: Pin Assignment Back (100-Pin DIMM)

| PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL |
|---|---|---|---|---|---|---|---|
| 51 | Vss | 63 | A1 | 76 | Vss | 88 | DQ24 |
| 52 | DQ8 | 64 | A3 | 77 | CKE1 | 89 | DQ25 |
| 53 | DQ9 | 65 | A5 | 78 | NC | 90 | DQ26 |
| 54 | DQ10 | 66 | A7 | 79 | S1# | 91 | DQ27 |
| 55 | DQ11 | 67 | A9 | 80 | S3# | 92 | VDD |
| 56 | VDD | 68 | BA0 | 81 | VDD | 93 | DQ28 |
| 57 | DQ12 | 69 | NC | 82 | NC | 94 | DQ29 |
| 58 | DQ13 | 70 | NC | 83 | NC | 95 | DQ30 |
| 59 | DQ14 | 71 | VDD | 84 | NC | 96 | DQ31 |
| 60 | DQ15 | 72 | RAS# | 85 | NC | 97 | Vss |
| 61 | DQMB1 | 73 | CAS# | 86 | Vss | 98 | SA0 |
| 62 | Vss | 74 | RFU | 87 | DQMB3 | 99 | SA1 |
| | | 75 | CK1 | | | 100 | SA2 |

## Figure 2: Pin Locations (100-Pin DIMM)

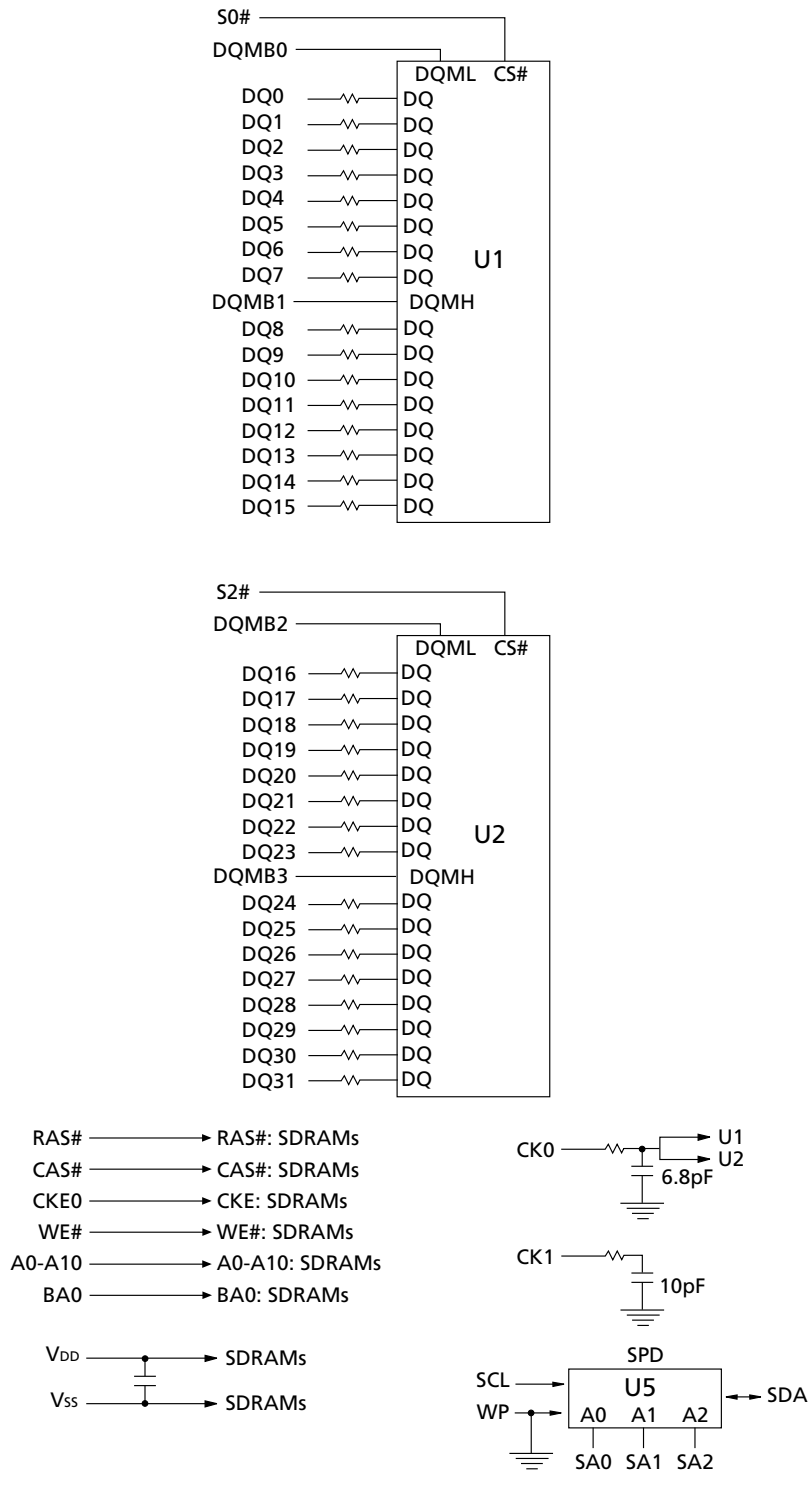


## Table 6: Pin Descriptions

Pin numbers may not correlate with symbols. Refer to the Pin Assignment Tables on page 2 for more information.

| PIN NUMBER | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|
| 28, 72, 73 | WE#, RAS#, CAS# | Input | Command Inputs: RAS#, CAS# and WE# (along with S#) define the command being entered. |
| 25, 75 | CK0, CK1 | Input | Clock: CK is driven by the system clock. All SDRAM input signals are sampled on the positive edge SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers. |
| 27, 77 | CKE0, CKE1 | Input | Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CK signal. Deactivating the clock provides POWER-DOWN and SELF REFRESH operation (all banks idle), or CLOCK SUSPEND operation (burst access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CK, are disabled during power-down and self refresh modes, providing low standby power. |
| 29, 30, 79, 80 | S0#-S3# | Input | Chip Select: S# enables (registered LOW) or disables (registered HIGH) the the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code. |
| 11, 37, 61, 87 | DQMB0-DQMB3 | Input | Input/Output Mask: DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (after a two-clock latency) when DQMB is sampled HIGH during a READ cycle. |
| 68 | BA0 | Input | Bank Address: BA0 defines to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. |
| 13, 14, 15, 16, 17, 18, 63, 64, 65, 66, 67 | A0-A10 | Input | Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 is sampled during a PRECHARGE command to determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command. |
| 49 | SCL | Input | Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module. |
| 98-100 | SA0-SA2 | Input | Presence-Detect Address Inputs: These pins are used to configure the presence-detect device. |
| 2-5, 7-10, 38-41, 43-46, 52-55, 57-60, 88-91, 93-96 | DQ0-DQ31 | Input/ Output | Data I/Os: Data bus. |
| 48 | SDA | Input/ Output | Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module. |
| 6, 21, 31, 42, 50, 56, 71, 81, 92 | $V_{DD}$ | Supply | Power Supply: +3.3V ±0.3V. |
| 1, 12, 26, 36, 47, 51, 62, 76, 86, 97 | $V_{SS}$ | Supply | Ground. |
| 23, 24, 74 | RFU | – | Reserved for Future Use: These pins should be left unconnected. |
| 19, 20, 22, 32-35, 69, 70, 78, 82-85 | NC | – | Not connected. |

## Figure 3: Functional Block Diagram ( MT2LSDT132U)

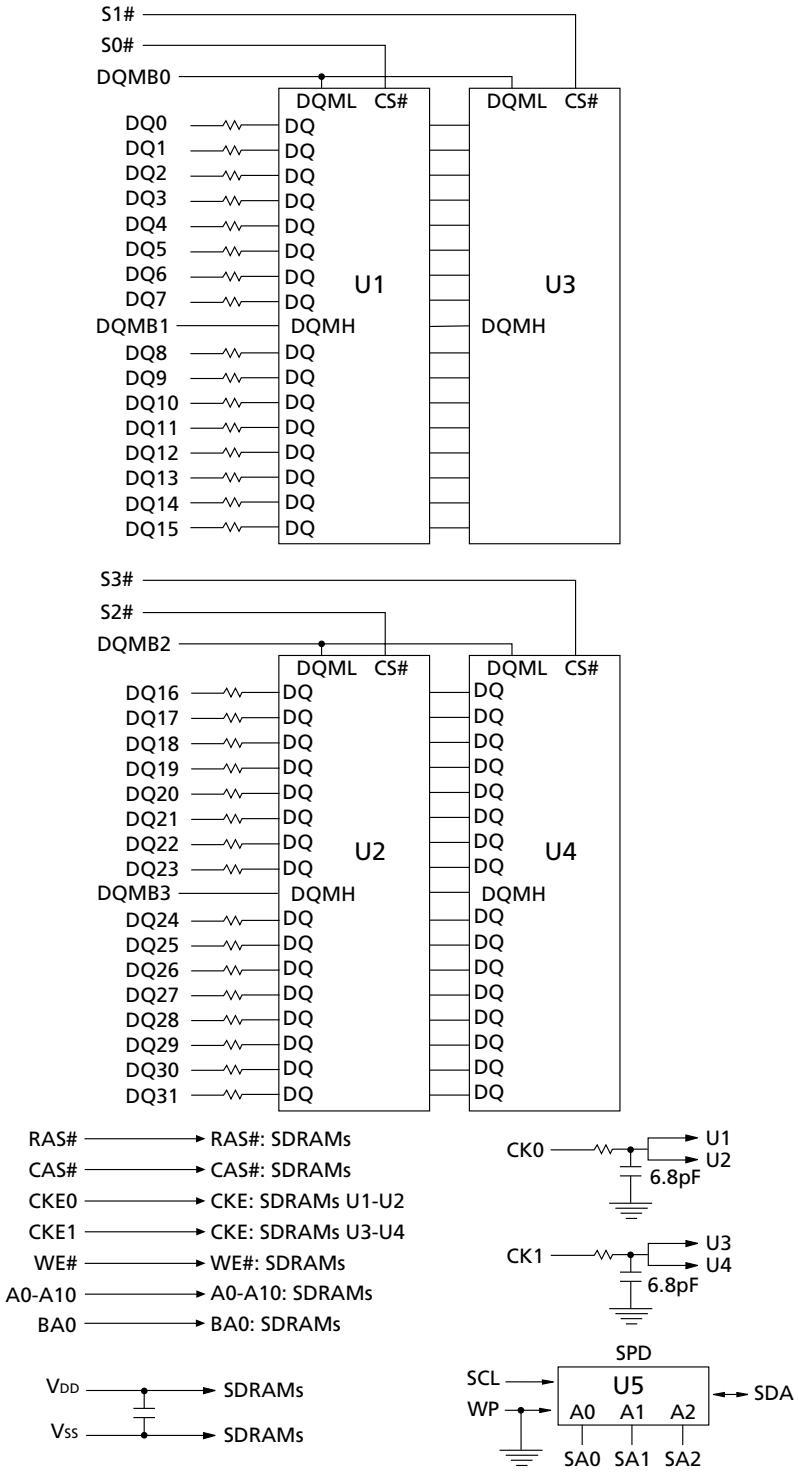



SDRAMs = MT48LC1M16A1TG

NOTE:

1. All resistor values are 22Ω unless otherwise specified.
2. Per industry standard, Micron utilizes various component speed grades as referenced in the Module Part Numbering Guide at www.micron.com/numberguide.

## Figure 4: Functional Block Diagram (MT4LSDT232UD)




NOTE:

1. All resistor values are 22Ω unless otherwise specified.
2. Per industry standard, Micron utilizes various component speed grades as referenced in the Module Part Numbering Guide at www.micron.com/numberguide.

SDRAMs = MT48LC1M16A1TG

## General Description

The Micron MT2LSDT132U and MT4LSDT232UD are high-speed CMOS, dynamic random-access, 4MB and 8MB memory modules organized in a x32 configuration. These modules use SDRAM devices which are internally configured as dual-bank DRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signal CK).

Read and write accesses to these SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0 selects the device bank, A0–A10 for device row). The address bits registered coincident with the READ or WRITE command (BA0, A0–A7) are used to select the starting device bank and column location for the burst access.

These modules provide for programmable READ or WRITE burst lengths of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. These modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one device bank while accessing the other device bank will hide the PRECHARGE cycles and provide seamless, high-speed, random access operation.

These modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs, outputs, and clocks are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 16Mb SDRAM component data sheet.

## Serial Presence-Detect Operation

These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard $I^2C$ bus using the DIMM's SCL (clock) and SDA (data) signals. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

### *Initialization*

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to $V_{DD}$ and $V_{DD}Q$ (simultaneously) and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

Once the 100µs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All device banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

### *Mode Register Definition*

The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in Figure 5, Mode Register Definition Diagram, on page 7. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0–M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4–M6 specify the CAS latency, M7 and M8

specify the operating mode, M9 specifies the write burst mode, and M10 and M11 are reserved for future use.

The mode register must be loaded when all device banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

## Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 5, Mode Register Definition Diagram. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

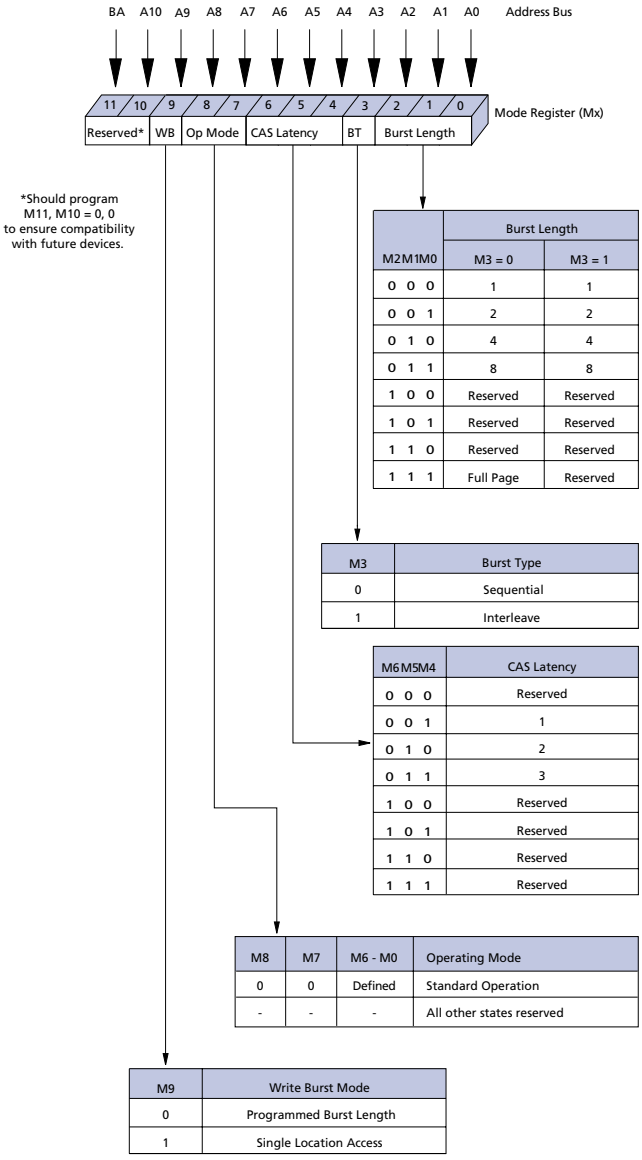
When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached, as shown in Table 7, Burst Definition Table, on page 8. The block is uniquely selected by A1–A7 when the burst length is set to two; by A2–A7 when the burst length is set to four; and by A3–A7 when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached, as shown in Table 7, Burst Definition Table, on page 8.

## Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 7, Burst Definition Table, on page 8.

**Figure 5: Mode Register Definition Diagram**



## TABLE 7: Burst Definition Table

| BURST LENGTH | STARTING COLUMN ADDRESS | ORDER OF ACCESSES WTHIN A BURST | |
|---|---|---|---|
| | | TYPE = SEQUENTIAL | TYPE = INTERLEAVED |
| 2 | A0 | | |
| | 0 | 0-1 | 0-1 |
| | 1 | 1-0 | 1-0 |
| 4 | A1 A0 | | |
| | 0 0 | 0-1-2-3 | 0-1-2-3 |
| | 0 1 | 1-2-3-0 | 1-0-3-2 |
| | 1 0 | 2-3-0-1 | 2-3-0-1 |
| | 1 1 | 3-0-1-2 | 3-2-1-0 |
| 8 | A2 A1 A0 | | |
| | 0 0 0 | 0-1-2-3-4-5-6-7 | 0-1-2-3-4-5-6-7 |
| | 0 0 1 | 1-2-3-4-5-6-7-0 | 1-0-3-2-5-4-7-6 |
| | 0 1 0 | 2-3-4-5-6-7-0-1 | 2-3-0-1-6-7-4-5 |
| | 0 1 1 | 3-4-5-6-7-0-1-2 | 3-4-5-6-7-0-1-2 |
| | 1 0 0 | 4-5-6-7-0-1-2-3 | 4-5-6-7-0-1-2-3 |
| | 1 0 1 | 5-6-7-0-1-2-3-4 | 5-4-7-6-1-0-3-2 |
| | 1 1 0 | 6-7-0-1-2-3-4-5 | 6-7-4-5-2-3-0-1 |
| | 1 1 1 | 7-0-1-2-3-4-5-6 | 7-6-5-4-3-2-1-0 |
| Full Page (256) | n = A0-A7 (location 0-255) | Cn, Cn + 1, Cn + 2, Cn + 3, Cn + 4. . . Cn - 1, Cn . . . | Not supported |

NOTE:

1. For a burst length of two, A1–A7 select the block-of-two burst; A0 selects the starting column within the block.
2. For a burst length of four, A2–A7 select the block-of-four burst; A0–A1 select the starting column within the block.
3. For a burst length of eight, A3–A7 select the block-of-eight burst; A0–A2 select the starting column within the block.
4. For a full-page burst, the full row is selected and A0–A7 select the starting column.
5. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
6. For a burst length of one, A0–A7 select the unique column to be accessed, and mode register bit M3 is ignored.

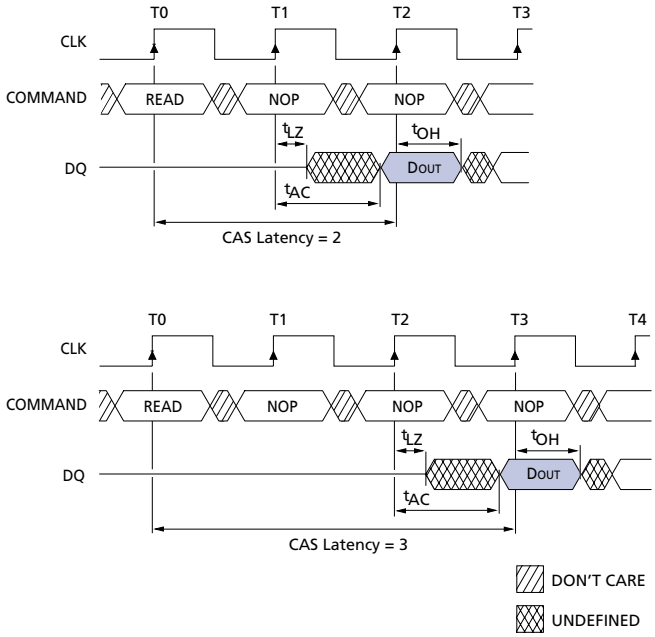
## CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available by clock edge *n* + *m*. The DQs will start driving as a result of the clock edge one cycle earlier (*n* + *m* - 1), and provided that the relevant access times are met, the data will be valid by clock edge *n* + *m*. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 6, CAS Latency Diagram. Table 8, CAS Latency Table, on page 9, indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

### Figure 6: CAS Latency Diagram




## Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

### *Write Burst Mode*

When M9 = 0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (non-burst) accesses.

**TABLE 8: CAS Latency Table**

| SPEED | ALLOWABLE OPERATING CLOCK FREQUENCY (MHz) | |
|---|---|---|
| | CAS LATENCY = 2 | CAS LATENCY = 3 |
| -8 | ≤ 100 | ≤ 125 |
| -10 | ≤ 66 | ≤ 100 |

## Commands

Table 9, Truth Table – Commands and DQMB Operation, provides a general reference of available commands. For a more detailed description of commands and operations, refer to the 16Mb SDRAM component data sheets.

### Table 9: Truth Table – Commands and DQMB Operation

Note: 1

| NAME (FUNCTION) | CS# | RAS# | CAS# | WE# | DQMB | ADDR | DQ | NOTES |
|---|---|---|---|---|---|---|---|---|
| COMMAND INHIBIT (NOP) | H | X | X | X | X | X | X | |
| NO OPERATION (NOP) | L | H | H | H | X | X | X | |
| ACTIVE (Select bank and activate row) | L | L | H | H | X | Bank/ Row | X | 3 |
| READ (Select bank and column, and start READ burst) | L | H | L | H | L/H[8] | Bank/Col | X | 4 |
| WRITE (Select bank and column, and start WRITE burst) | L | H | L | L | L/H[8] | Bank/Col | Valid | 4 |
| BURST TERMINATE | L | H | H | L | X | X | Active | |
| PRECHARGE (Deactivate row in bank or banks) | L | L | H | L | X | Code | X | 5 |
| AUTO REFRESH or SELF REFRESH (Enter self refresh mode) | L | L | L | H | X | X | X | 6, 7 |
| LOAD MODE REGISTER | L | L | L | L | X | Op-Code | X | 2 |
| Write Enable/Output Enable | – | – | – | – | L | – | Active | 8 |
| Write Inhibit/Output High-Z | – | – | – | – | H | – | High-Z | 8 |

NOTE:

1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A0–A10 define the op-code written to the Mode Register.
3. A0–A10 provide row address and BA0 determine which bank is made active.
4. A0–A7 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0 determine which bank is being read from or written to.
5. A10 LOW: BA0 determine which bank is being precharged. A10 HIGH: both banks are precharged and BA0 is "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Activates or deactivates the DQ during WRITE (zero-clock delay) and READ (two-clock delay).

## Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Voltage on $V_{DD}$ Supply
Relative to $V_{SS}$ . . . . . -1V to +4.6V
Voltage on Inputs, NC or I/O Pins
Relative to $V_{SS}$ . . . . . -1V to +4.6V
Operating Temperature
$T_A$ (ambient) . . . . . 0°C to +70°C
Storage Temperature (plastic) . . . . . -55°C to +125°C
Power Dissipation
Single Rank . . . . . 2W
Dual Rank . . . . . 4W

## Table 10: DC Electrical Characteristics and Operating Conditions (4MB)

Note: 1; notes appear on page 16; $V_{DD}$ = +3.3V ±0.3V

| PARAMETER/CONDITION | | SYM | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| SUPPLY VOLTAGE | | $V_{DD}$ | 3.0 | 3.6 | V | |
| INPUT HIGH VOLTAGE: Logic 1; All inputs | | $V_{IH}$ | 2.2 | $V_{DD}$ + 0.3 | V | 22 |
| INPUT LOW VOLTAGE: Logic 0; All inputs | | $V_{IL}$ | -0.3 | 0.8 | V | 22 |
| INPUT LEAKAGE CURRENT: Any input 0V ≤ $V_{IN}$ ≤ $V_{DD}$ (All other pins not under test = 0V) | WE#, RAS#, CAS#, A0-A10, BA0, CK, CKE | $I_{I1}$ | -10 | 10 | µA | 30 |
| | S# | $I_{I2}$ | -5 | 5 | µA | 30 |
| | DQMB | $I_{I3}$ | -5 | 5 | µA | 4, 30 |
| OUTPUT LEAKAGE CURRENT: DQ disabled; 0V ≤ $V_{OUT}$ ≤ $V_{DD}$ | DQ | $I_{OZ}$ | -10 | 10 | µA | 4, 30 |
| OUTPUT LEVELS: Output High Voltage ($I_{OUT}$ = -4mA) | | $V_{OH}$ | 2.4 | – | V | |
| Output Low Voltage ($I_{OUT}$ = 4mA) | | $V_{OL}$ | – | 0.4 | V | |

## Table 11: DC Electrical Characteristics and Operating Conditions (8MB)

Note: 1; notes appear on page 16; $V_{DD}$ = +3.3V ±0.3V

| PARAMETER/CONDITION | | SYM | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| SUPPLY VOLTAGE | | $V_{DD}$ | 3.0 | 3.6 | V | |
| INPUT HIGH VOLTAGE: Logic 1; All inputs | | $V_{IH}$ | 2.2 | $V_{DD}$ + 0.3 | V | 22 |
| INPUT LOW VOLTAGE: Logic 0; All inputs | | $V_{IL}$ | -0.3 | 0.8 | V | 22 |
| INPUT LEAKAGE CURRENT: Any input 0V ≤ $V_{IN}$ ≤ $V_{DD}$ (All other pins not under test = 0V) | WE#, RAS#, CAS#, A0-A10, BA0 | $I_{I1}$ | -20 | 20 | µA | 30 |
| | CK, CKE | $I_{I2}$ | -10 | 10 | µA | 30 |
| | S# | $I_{I3}$ | -5 | 5 | µA | 30 |
| | DQMB | $I_{I4}$ | -10 | 10 | µA | 4, 30 |
| OUTPUT LEAKAGE CURRENT: DQ disabled; 0V ≤ $V_{OUT}$ ≤ $V_{DD}$ | DQ | $I_{OZ}$ | -20 | 20 | µA | 4, 30 |
| OUTPUT LEVELS: Output High Voltage ($I_{OUT}$ = -4mA) | | $V_{OH}$ | 2.4 | – | V | |
| Output Low Voltage ($I_{OUT}$ = 4mA) | | $V_{OL}$ | – | 0.4 | V | |

## Table 12: IDD Specifications and Conditions (4MB)

DRAM components only
Notes: 1, 5, 6, 11, 13; notes appear on page 16; VDD = VDDQ = +3.3V ±0.3V

| | | MAX | | | |
|---|---|---|---|---|---|
| **PARAMETER/CONDITION** | **SYMBOL** | **-8** | **-10** | **UNITS** | **NOTES** |
| OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; $^{t}$RC = $^{t}$RC (MIN) | IDD1 | 270 | 260 | mA | 3, 18, 19, 27 |
| STANDBY CURRENT: Power-Down Mode; All device device banks idle; CKE = LOW | IDD2 | 4 | 4 | mA | 27 |
| STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; All device banks active after $^{t}$RCD met; No accesses in progress | IDD3 | 70 | 60 | mA | 3, 12, 19, 27 |
| OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All device banks active | IDD4 | 200 | 160 | mA | 3, 18, 19, 27 |
| AUTO REFRESH CURRENT: $^{t}$RC = 15.625 µs; CAS latency = 3; CS# = HIGH; CKE = HIGH; $^{t}$CK = 15ns (10ns for -8) | IDD5 | 70 | 60 | mA | 3, 12, 18, 19, 27 |
| SELF REFRESH CURRENT: CKE ≤ 0.2V | IDD6 | 2 | 2 | mA | 4 |

## Table 13: IDD Specifications and Conditions (8MB)

DRAM components only
Notes: 1, 5, 6, 11, 13; notes appear on page 16; VDD = VDDQ = +3.3V ±0.3V

| | | MAX | | | |
|---|---|---|---|---|---|
| **PARAMETER/CONDITION** | **SYMBOL** | **-8** | **-10** | **UNITS** | **NOTES** |
| OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; $^{t}$RC = $^{t}$RC (MIN) | IDD1[a] | 274 | 264 | mA | 3, 18, 19, 27 |
| STANDBY CURRENT: Power-Down Mode; All device device banks idle; CKE = LOW | IDD2[b] | 8 | 8 | mA | 27 |
| STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; All device banks active after $^{t}$RCD met; No accesses in progress | IDD3[a] | 74 | 64 | mA | 3, 12, 19, 27 |
| OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All device banks active | IDD4[a] | 204 | 164 | mA | 3, 18, 19, 27 |
| AUTO REFRESH CURRENT: $^{t}$RC = 15.625 µs; CAS latency = 3; CS# = HIGH; CKE = HIGH; $^{t}$CK = 15ns (10ns for -8) | IDD5[b] | 140 | 120 | mA | 3, 12, 18, 19, 27 |
| SELF REFRESH CURRENT: CKE ≤ 0.2V | IDD6[b] | 4 | 4 | mA | 4 |

NOTE:
a - Value calculated as one module rank in this operating condition, and all other module ranks in Power-Down Mode.
b - Value calculated reflects all module ranks in this operating condition.

## Table 14: Capacitance (4MB)

Notes: 1, 2; this parameter is sampled; notes appear on page 16; $V_{DD}$ = +3.3V; f = 1 MHz

| PARAMETER | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|
| Input Capacitance: A0-A10, BA0, RAS#, CAS#, WE#, CKE | $C_{I1}$ | 5 | 10 | pF |
| Input Capacitance: CK | $C_{I3}$ | 11.8 | 14.8 | pF |
| Input Capacitance: S# | $C_{I4}$ | 2.5 | 5 | pF |
| Input Capacitance: DQMB | $C_{I5}$ | 2.5 | 5 | pF |
| Input Capacitance: SCL, SA0-SA2, SDA | $C_{I6}$ | – | 6 | pF |
| Input/Output Capacitance: DQ | $C_{IO}$ | 4 | 6.5 | pF |

## Table 15: Capacitance (8MB)

Notes: 1, 2; this parameter is sampled; notes appear on page 16; $V_{DD}$ = +3.3V; f = 1 MHz

| PARAMETER | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|
| Input Capacitance: A0-A10, BA0, RAS#, CAS#, WE# | $C_{I1}$ | 10 | 20 | pF |
| Input Capacitance: CKE | $C_{I2}$ | 5 | 10 | pF |
| Input Capacitance: CK | $C_{I3}$ | 11.8 | 14.8 | pF |
| Input Capacitance: S# | $C_{I4}$ | 2.5 | 5 | pF |
| Input Capacitance: DQMB | $C_{I5}$ | 5 | 10 | pF |
| Input Capacitance: SCL, SA0-SA2, SDA | $C_{I6}$ | – | 6 | pF |
| Input/Output Capacitance: DQ | $C_{IO}$ | 8 | 13 | pF |

## Table 16: SDRAM Component AC Electrical Characteristics

Notes: 1–5, 29; notes appear on page 16; SDRAM component specifications

| PARAMETER | | SYMBOL | -8 | | -10 | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | | |
| Access time from CLK (positive edge) | CL = 3 | $^{t}AC$ | | 6 | | 7.5 | ns | |
| | CL = 2 | $^{t}AC$ | | 9 | | 9 | ns | 22 |
| | CL = 1 | $^{t}AC$ | | 22 | | 27 | ns | 22 |
| Address hold time | | $^{t}AH$ | 1 | | 1 | | ns | |
| Address setup time | | $^{t}AS$ | 2 | | 3 | | ns | |
| CLK high-level width | | $^{t}CH$ | 3 | | 3.5 | | ns | |
| CLK low-level width | | $^{t}CL$ | 3 | | 3.5 | | ns | |
| Clock cycle time | CL = 3 | $^{t}CK$ | 8 | | 10 | | ns | 23 |
| | CL = 2 | $^{t}CK$ | 13 | | 15 | | ns | 22, 23 |
| | CL = 1 | $^{t}CK$ | 25 | | 30 | | ns | 23 |
| CKE hold time | | $^{t}CKH$ | 1 | | 1 | | ns | |
| CKE setup time | | $^{t}CKS$ | 3 | | 3 | | ns | |
| CS#, RAS#, CAS#, WE#, DQM hold time | | $^{t}CMH$ | 1 | | 1 | | ns | |
| CS#, RAS#, CAS#, WE#, DQM setup time | | $^{t}CMS$ | 2 | | 3 | | ns | |
| Data-in hold time | | $^{t}DH$ | 1 | | 1 | | ns | |
| Data-in setup time | | $^{t}DS$ | 2 | | 3 | | ns | |
| Data-out high-impedance time | CL = 3 | $^{t}HZ$ | | 6 | | 8 | ns | 10 |
| | CL = 2 | $^{t}HZ$ | | 7 | | 10 | ns | 10 |
| | CL = 1 | $^{t}HZ$ | | 15 | | 15 | ns | 10 |
| Data-out low-impedance time | | $^{t}LZ$ | 1 | | 2 | | | |
| Data-out hold time (load) | | $^{t}OH$ | 2.5 | | 2.5 | | ns | |
| ACTIVE to PRECHARGE command period | | $^{t}RAS$ | 48 | 120,000 | 50 | 120,000 | ns | |
| ACTIVE to ACTIVE command period | | $^{t}RC$ | 80 | | 80 | | ns | 22 |
| AUTO REFRESH period | | $^{t}REF$ | 64 | | 64 | | ns | 9 |
| ACTIVE to READ or WRITE delay | | $^{t}RCD$ | 24 | | 30 | | ns | 22 |
| Refresh period (4,096 cycles) | | $^{t}REF$ | | 64 | | 64 | ns | |
| PRECHARGE command period | | $^{t}RP$ | 24 | | 30 | | ns | 22 |
| ACTIVE bank A to ACTIVE bank B command period | | $^{t}RRD$ | 16 | | 20 | | ns | |
| Transition time | | $^{t}T$ | 0.3 | 10 | 1 | 20 | ns | 7 |
| WRITE recovery time | | $^{t}WR$ | 1 CLK + 2ns | | 1 CLK | | $^{t}CK$ | 24 |
| | | | 10 | | 10 | | ns | 25 |
| Exit SELF REFRESH to ACTIVE command | | $^{t}XSR$ | 80 | | 90 | | ns | 20 |

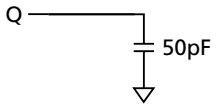
## Table 17: AC Functional Characteristics

Notes: 5– 9, 11; notes appear on page 16

| PARAMETER | | SYMBOL | -8 | -10 | UNITS | NOTES |
|---|---|---|---|---|---|---|
| READ/WRITE command to READ/WRITE command | | $^{t}CCD$ | 1 | 1 | $^{t}CK$ | 17 |
| CKE to clock disable or power-down entry mode | | $^{t}CKED$ | 1 | 1 | $^{t}CK$ | 14 |
| CKE to clock enable or power-down exit setup mode | | $^{t}PED$ | 1 | 1 | $^{t}CK$ | 14 |
| DQM to input data delay | | $^{t}DQD$ | 0 | 0 | $^{t}CK$ | 17 |
| DQM to data mask during WRITEs | | $^{t}DQM$ | 0 | 0 | $^{t}CK$ | 17 |
| DQM to data high-impedance during READs | | $^{t}DQZ$ | 2 | 2 | $^{t}CK$ | 17 |
| WRITE command to input data delay | | $^{t}DWD$ | 0 | 0 | $^{t}CK$ | 17 |
| Data-in to ACTIVATE command | CL = 3 | $^{t}DAL$ | 5 | 4 | $^{t}CK$ | 15, 21 |
| | CL = 2 | $^{t}DAL$ | 4 | 3 | $^{t}CK$ | 15, 21 |
| | CL = 1 | $^{t}DAL$ | 3 | 4 | $^{t}CK$ | 15, 21 |
| Data-in to precharge | | $^{t}DPL$ | 2 | 1 | $^{t}CK$ | 16 |
| Last data-in to BURST STOP command | | $^{t}BDL$ | 0 | 0 | $^{t}CK$ | 17 |
| Last data-in to new READ/WRITE command | | $^{t}CDL$ | 1 | 1 | $^{t}CK$ | 17 |
| Last data-in to PRECHARGE command | | $^{t}RDL$ | 1 | 1 | $^{t}CK$ | 21, 26 |
| LOAD MODE REGISTER command to ACTIVE or REFRESH command | | $^{t}MRD$ | 2 | 2 | $^{t}CK$ | 11 |
| Data-out to high-impedance from PRECHARGE command | CL = 3 | $^{t}ROH$ | 3 | 3 | $^{t}CK$ | 6 |
| | CL = 2 | $^{t}ROH$ | 2 | 2 | $^{t}CK$ | 6 |
| | CL = 1 | $^{t}ROH$ | 1 | 1 | $^{t}CK$ | 6 |

## Notes

1. All voltages referenced to $V_{SS}$.
2. This parameter is sampled. $V_{DD}$, $V_{DD}Q$ = +3.3V; f = 1 MHz; $T_A$ = 25°C; pin under test biased at 1.4V.
3. $I_{DD}$ is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured (0°C ≤ $T_A$ ≤ +70°C).
6. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. ($V_{DD}$ and $V_{DD}Q$ must be powered up simultaneously. $V_{SS}$ and $V_{SS}Q$ must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the $^{t}$REF refresh requirement is exceeded.
7. AC characteristics assume $^{t}$T = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
9. Outputs measured at 1.5V with equivalent load:




10. $^{t}$HZ defines the time at which the output achieves the open circuit condition; it is not a reference to $V_{OH}$ or $V_{OL}$. The last valid data element will meet $^{t}$OH before going High-Z.
11. AC timing and $I_{DD}$ tests have $V_{IL}$ = 0V and $V_{IH}$ = 3V, with timing referenced to 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at $V_{IL}$ (MAX) and $V_{IH}$ (MIN) and no longer at the ISV crossover point.
12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid $V_{IH}$ or $V_{IL}$ levels.
13. $I_{DD}$ specifications are tested after the device is properly initialized.
14. Timing actually specified by $^{t}$CKS; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by $^{t}$WR plus $^{t}$RP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by $^{t}$WR.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The $I_{DD}$ current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on $^{t}$CK = 100 MHz for -10; $^{t}$CK = 125 MHz for -8.
22. $V_{IH}$ overshoot: $V_{IH}$ (MAX) = $V_{DD}Q$ + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. $V_{IL}$ undershoot: $V_{IL}$ (MIN) = -2V for a pulse width ≤ 3ns.
23. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including $^{t}$WR, and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only. The precharge timing budget ($^{t}$RP) begins 7.5ns for -10; and 7ns for -8 after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.
25. Precharge mode only.
26. JEDEC and PC100 specify three clocks.
27. For -8, CL = 3 and $^{t}$CK = 7.5ns; for -10, CL = 2 and $^{t}$CK = 10ns.
28. CKE is HIGH during refresh command period $^{t}$RFC (MIN) else CKE is LOW. The $I_{DD}6$ limit is actually a nominal value and does not result in a fail value.
29. Refer to device data sheet for timing waveforms.
30. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.

## SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (as shown in Figure 7, Data Validity, and Figure 8, Definition of Start and Stop).

### SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

### SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

### SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (as shown in Figure 9, Acknowledge Response from Receiver).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

**Figure 7: Data Validity**

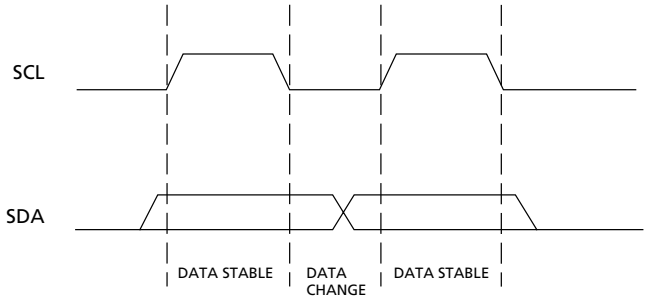



**Figure 8: Definition of Start and Stop**

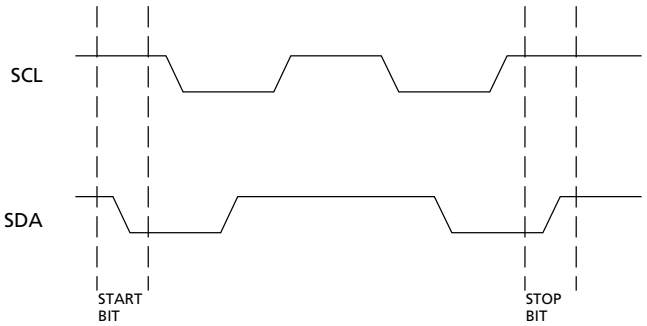
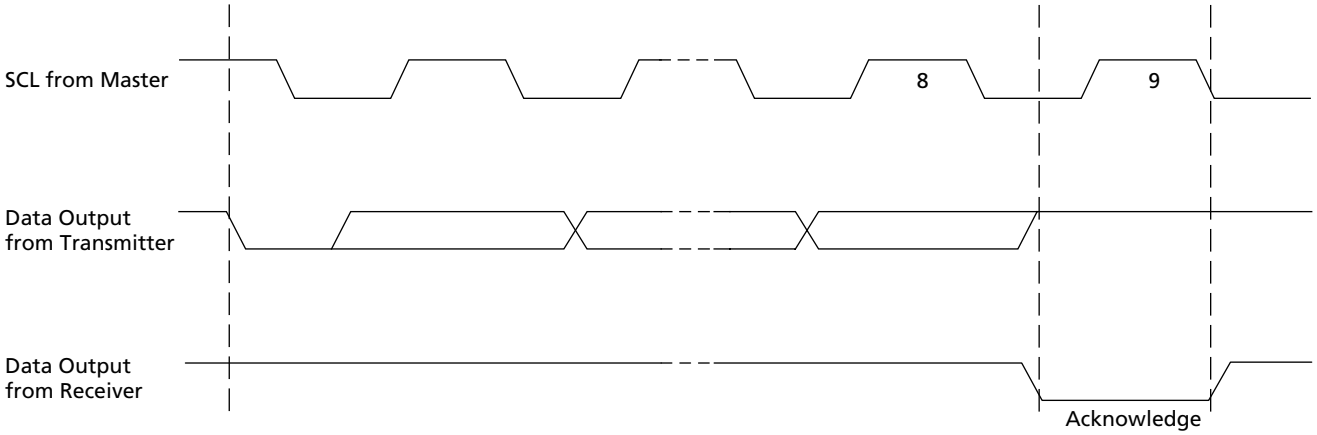



**Figure 9: Acknowledge Response from Receiver**



## Table 18: EEPROM Device Select Code

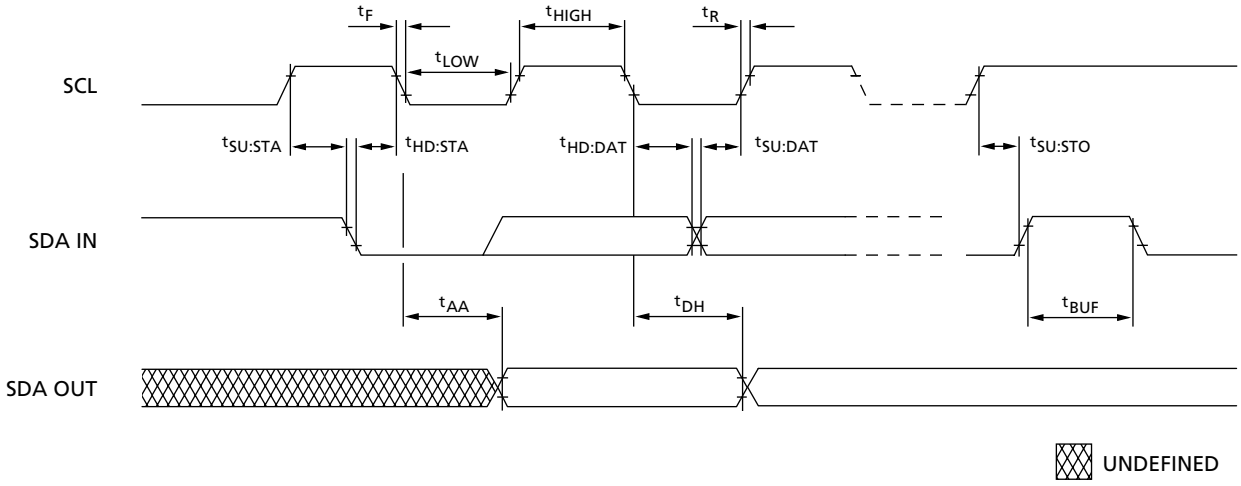
Most significant bit (b7) is sent first

| SELECT CODE | DEVICE TYPE IDENTIFIER | | | | CHIP ENABLE | | | RW |
|---|---|---|---|---|---|---|---|---|
| | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Memory Area Select Code (two arrays) | 1 | 0 | 1 | 0 | SA2 | SA1 | SA0 | RW |
| Protection Register Select Code | 0 | 1 | 1 | 0 | SA2 | SA1 | SA0 | RW |

## Table 19: EEPROM Operating Modes

| MODE | RW BIT | WC | BYTES | INITIAL SEQUENCE |
|---|---|---|---|---|
| Current Address Read | 1 | VIH or VIL | 1 | Start, Device Select, RW = 1 |
| RandomAddressRead | 0 | VIH or VIL | 1 | Start, Device Select, RW= 0, Address |
| | 1 | VIH or VIL | | RESTART, Device Select, RW= 1 |
| Sequential Read | 1 | VIH or VIL | ≥ 1 | Similar to Current or Random Address Read |
| Byte Write | 0 | VIL | 1 | START, Device Select, RW = 0 |
| Page Write | 0 | VIL | ≤ 16 | START, Device Select, RW = 0 |

## Figure 10: SPD EEPROM



## Table 20: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to $V_{SS}$; $V_{DD}$= +3.3V ±0.3V

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| SUPPLY VOLTAGE | $V_{DD}$ | 3 | 3.6 | V | |
| INPUT HIGH VOLTAGE: Logic 1; All inputs | $V_{IH}$ | $V_{DD}$ x 0.7 | $V_{DD}$ + 0.5 | V | |
| INPUT LOW VOLTAGE: Logic 0; All inputs | $V_{IL}$ | -1 | $V_{DD}$ x 0.3 | V | |
| OUTPUT LOW VOLTAGE: $I_{OUT}$ = 3mA | $V_{OL}$ | – | 0.4 | V | |
| INPUT LEAKAGE CURRENT: $V_{IN}$ = GND to $V_{DD}$ | $I_{LI}$ | – | 10 | µA | |
| OUTPUT LEAKAGE CURRENT: $V_{OUT}$ = GND to $V_{DD}$ | $I_{LO}$ | – | 10 | µA | |
| STANDBY CURRENT:<br>SCL = SDA = $V_{DD}$ - 0.3V; All other inputs = $V_{DD}$ or $V_{SS}$ | $I_{SB}$ | – | 30 | µA | |
| POWER SUPPLY CURRENT:<br>SCL clock frequency = 100 KHz | $I_{DD}$ | – | 2 | mA | |

## Table 21: Serial Presence-Detect EEPROM AC Electrical Characteristics

All voltages referenced to $V_{SS}$; $V_{DD}$ = +3.3V ±0.3V

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| SCL LOW to SDA data-out valid | $^{t}AA$ | 0.3 | 3.5 | µs | |
| Time the bus must be free before a new transition can start | $^{t}BUF$ | 4.7 | | µs | |
| Data-out hold time | $^{t}DH$ | 300 | | ns | |
| SDA and SCL fall time | $^{t}F$ | | 300 | ns | |
| Data-in hold time | $^{t}HD:DAT$ | 0 | | µs | |
| Start condition hold time | $^{t}HD:STA$ | 4 | | µs | |
| Clock HIGH period | $^{t}HIGH$ | 4 | | µs | |
| Noise suppression time constant at SCL, SDA inputs | $^{t}I$ | | 100 | ns | |
| Clock LOW period | $^{t}LOW$ | 4.7 | | µs | |
| SDA and SCL rise time | $^{t}R$ | | 1 | µs | |
| SCL clock frequency | $^{t}SCL$ | | 100 | KHz | |
| Data-in setup time | $^{t}SU:DAT$ | 250 | | ns | |
| Start condition setup time | $^{t}SU:STA$ | 4.7 | | µs | |
| Stop condition setup time | $^{t}SU:STO$ | 4.7 | | µs | |
| WRITE cycle time | $^{t}WRC$ | | 10 | ms | 1 |

NOTE:

1. The SPD EEPROM WRITE cycle time ($^{t}WRC$) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to the pull-up resistor, and the EEPROM does not respond to its slave address.

## Table 22: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

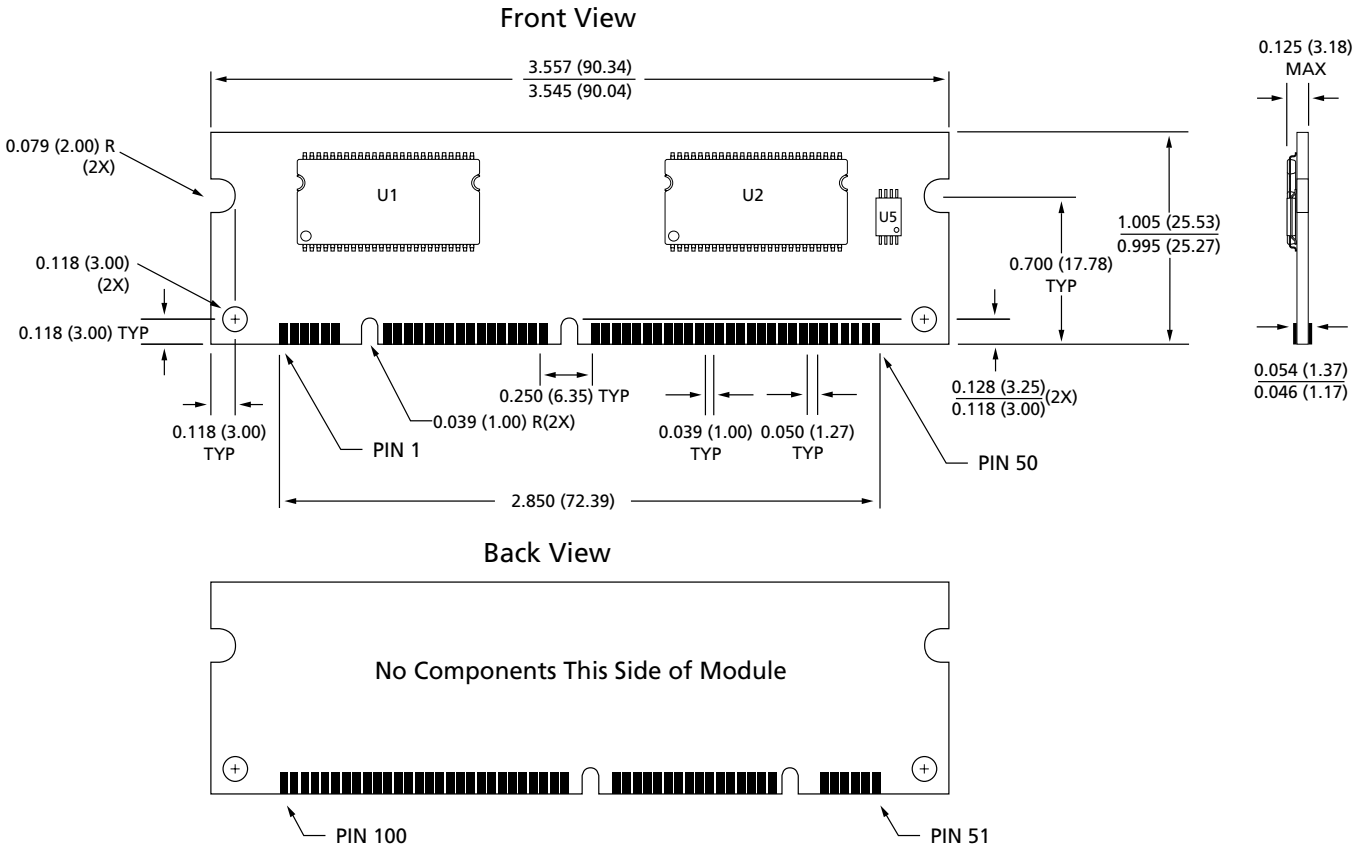
| BYTE | DESCRIPTION | ENTRY (VERSION) | MT2LSDT132U | MT4LSDT232UD |
|---|---|---|---|---|
| 0 | Number of Bytes Used by Micron | 128 | 80 | 80 |
| 1 | Total Number of SPD Memory Bytes | 256 | 08 | 08 |
| 2 | Memory Type | SDRAM | 04 | 04 |
| 3 | Number of Row Addresses | 11 | 0B | 0B |
| 4 | Number of Column Addresses | 8 | 08 | 08 |
| 5 | Number of Module Ranks | 1or 2 | 01 | 02 |
| 6 | Module Data Width | 32 | 20 | 20 |
| 7 | Module Data Width (continued) | 0 | 00 | 00 |
| 8 | Module Voltage Interface Levels | LVTTL | 01 | 01 |
| 9 | SDRAM Cycle Time, $^{t}$CK<br>(CAS Latency = 3) | 10ns (-10)<br>8ns (-8) | A0<br>80 | A0<br>80 |
| 10 | SDRAM Access From Clock, $^{t}$AC<br>(CAS Latency = 3) | 7.5ns (-10)<br>6ns (-8) | 75<br>60 | 75<br>60 |
| 11 | Module Configuration Type | None | 00 | 00 |
| 12 | Refresh Rate/Type | 15.62µs / Self | 80 | 80 |
| 13 | SDRAM Width (Primary SDRAM) | 16 | 16 | 16 |
| 14 | Error-checking SDRAM Data Width | 0 | 00 | 00 |
| 15 | Minimum Clock Delay, $^{t}$CCD | 1 $^{t}$CK | 01 | 01 |
| 16 | Burst Lengths Supported | 1, 2, 4, 8,<br>Page | 8F | 8F |
| 17 | Number of Banks on SDRAM Device | 2 | 02 | 02 |
| 18 | CAS Latencies Supported | 1, 2, 3 | 07 | 07 |
| 19 | CS Latency | 0 | 01 | 01 |
| 20 | WE Latency | 0 | 01 | 01 |
| 21 | SDRAM Module Attributes | Unbuffered | 00 | 00 |
| 22 | SDRAM Device Attributes: General | Attributes | 0E | 0E |
| 23 | SDRAM Cycle Time, $^{t}$CK<br>(CAS Latency = 2) | 15ns (-10)<br>10ns (-8) | F0<br>A0 | F0<br>A0 |
| 24 | SDRAM Access From Clock, $^{t}$AC, (CAS Latency = 2) | 9ns | 90 | 90 |
| 25 | SDRAM Cycle Time, $^{t}$CK<br>(CAS Latency = 1) | 30ns (-10)<br>25ns (-8) | 78<br>64 | 78<br>64 |
| 26 | SDRAM Access From Clock, $^{t}$AC, (CAS Latency = 1) | 27ns (-10)<br>22ns (-8) | 6C<br>58 | 6C<br>58 |
| 27 | Minimum Row Precharge Time, $^{t}$RP | 30ns (-10)<br>20ns (-8) | 1E<br>14 | 1E<br>14 |
| 28 | Minimum Row Active to Row Active, $^{t}$RRD | 20ns | 14 | 14 |
| 29 | Minimum RAS# to CAS# Delay, $^{t}$RCD | 30ns (-10)<br>20ns (-8) | 1E<br>14 | 1E<br>14 |
| 30 | Minimum RAS# Pulse Width, $^{t}$RAS | 60ns (-10)<br>50ns (-8) | 3C<br>32 | 3C<br>32 |
| 31 | Module Rank Density | 4MB | 01 | 01 |
| 32 | Command/Address Setup, $^{t}$AS | 3ns (-10)<br>2ns (-8) | 30<br>20 | 30<br>20 |
| 33 | Command/Address Hold, $^{t}$AH | 1ns | 10 | 10 |
| 34 | Data Signal Input Setup, $^{t}$DS | 3ns (-10)<br>2ns (-8) | 30<br>20 | 30<br>20 |
| 35 | Data Signal Input Hold, $^{t}$DH | 1ns | 10 | 10 |

## Table 22: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

| BYTE | DESCRIPTION | ENTRY (VERSION) | MT2LSDT132U | MT4LSDT232UD |
|---|---|---|---|---|
| 36-61 | RESERVED BYTES | – | 00 | 00 |
| 62 | SPD Revision | REV. 2 | 02 | 02 |
| 63 | Checksum for Bytes 0-62 | (-10)<br>(-8) | 7E<br>C9 | 7F<br>CA |
| 64 | Manufacturer's JEDEC ID Code | MICRON | | 2C |
| 65-71 | Manufacturer's JEDEC ID Code (Cont.) | | | FF |
| 72 | Manufacturing Location | 1-11 | | 01-0B |
| 73-90 | Module Part Number (ASCII) | | | Variable Data |
| 91 | PCB Identification Code | 1-9 | | 01-09 |
| 92 | Identification Code (Cont.) | 0 | | 00 |
| 93 | Year of Manufacture in BCD | | | Variable Data |
| 94 | Week of Manufacture in BCD | | | Variable Data |
| 95-98 | Module Serial Number | | | Variable Data |
| 99-127 | Manufacturer-Specific Data (RSVD) | | | – |

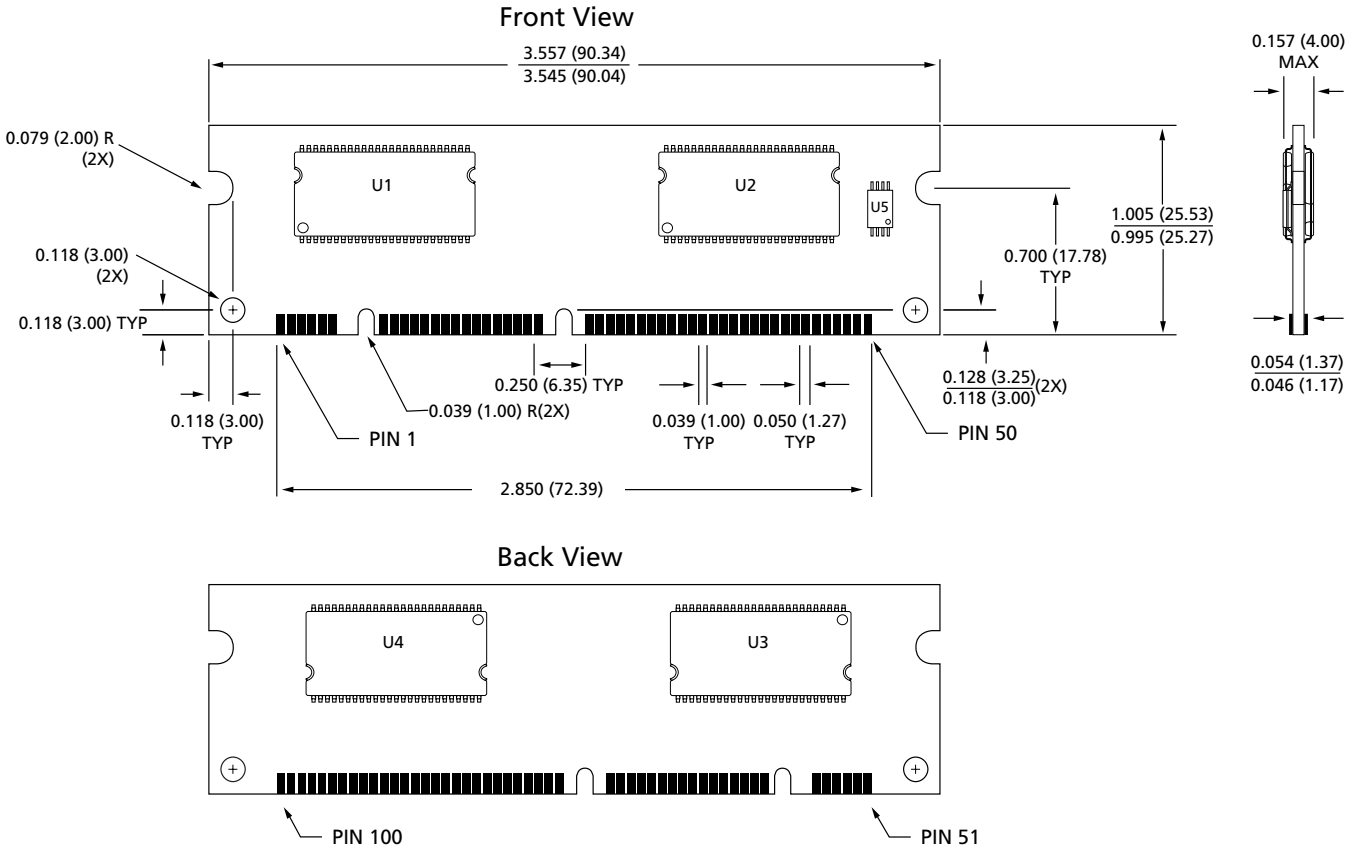
## Figure 11: 100-Pin DIMM Dimensions (4MB)




NOTE:

All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

## Figure 12: 100-Pin DIMM Dimensions (MT4LSDT232UD)




NOTE:

All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

## Data Sheet Designation

**Released (No Mark):** This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices.

Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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