4 MEG x 72 NONBUFFERED DRAM DIMM

DRAM MODULE

MT5LDT472A (X)

For the latest full-length data sheets, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- JEDEC-standard ECC pinout in a 168-pin, dual in-line memory module (DIMM)
- 32MB (4 Meg x 72)
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR) and HIDDEN
- All inputs are buffered except RAS#
- 4,096 cycles (12 row, 10 column addresses)
- FAST-PAGE-MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles

OPTIONS — MARKING

- Package
  168-pin DIMM (gold) — G
- Timing
  50ns access — -5
  60ns access — -6
- Access Cycles
  FAST PAGE MODE — None
  EDO PAGE MODE — X

KEY TIMING PARAMETERS

EDO Operating Mode

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tCAS
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

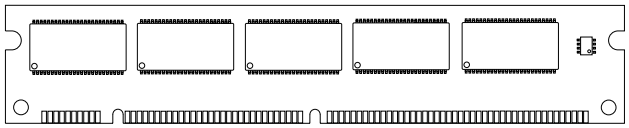
FPM Operating Mode

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-5	90ns	50ns	30ns	25ns	13ns	30ns
-6	110ns	60ns	35ns	30ns	15ns	40ns

NOTE: 1. Pin symbols in parentheses are not used on this module but may be used for other modules in this product family. They are for reference only.

PIN ASSIGNMENT (Front View)

168-Pin DIMM[1]



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	OE2#	86	DQ32	128	RFU
3	DQ1	45	RAS2#	87	DQ33	129	RAS3#
4	DQ2	46	CAS2#	88	DQ34	130	CAS6#
5	DQ3	47	CAS3#	89	DQ35	131	CAS7#
6	VDD	48	WE2#	90	VDD	132	RFU
7	DQ4	49	VDD	91	DQ36	133	VDD
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VDD	101	DQ45	143	VDD
18	VDD	60	DQ20	102	VDD	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	RFU	104	DQ47	146	RFU
21	CB0	63	NC	105	CB4	147	NC
22	CB1	64	VSS	106	CB5	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VDD	68	VSS	110	VDD	152	VSS
27	WE0#	69	DQ24	111	RFU	153	DQ56
28	CAS0#	70	DQ25	112	CAS4#	154	DQ57
29	CAS1#	71	DQ26	113	CAS5#	155	DQ58
30	RAS0#	72	DQ27	114	NC (RAS1#)	156	DQ59
31	OE0#	73	VDD	115	RFU	157	VDD
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	A11	164	NC
39	NC (A12)	81	NC	123	NC (A13)	165	SA0
40	VDD	82	SDA	124	VDD	166	SA1
41	VDD	83	SCL	125	RFU	167	SA2
42	RFU	84	VDD	126	RFU	168	VDD

PART NUMBERS

EDO Operating Mode

PART NUMBER	CONFIGURATION	SPEED
MT5LDT472AG-5 X	4 Meg x 72	50ns
MT5LDT472AG-6 X	4 Meg x 72	60ns

FPM Operating Mode

PART NUMBER	CONFIGURATION	SPEED
MT5LDT472AG-5	4 Meg x 72	50ns
MT5LDT472AG-6	4 Meg x 72	60ns

GENERAL DESCRIPTION

The MT5LDT472A (X) is a randomly accessed 32MB memory organized in a x72 configuration. It is specially processed to operate from 3V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 12 bits (A0-A11) at RAS# time and 10 bits (A0-A9) at CAS# time.

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# was taken LOW. During EARLY WRITE cycles, the data-outputs (Q) will remain High-Z regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data-outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no WRITE will occur, and the data-outputs will drive read data from the accessed location.

FAST PAGE MODE

FAST-PAGE-MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST-PAGE-MODE cycle is always initiated with a row address strobed in by RAS#, followed by a column address strobed in by CAS#. Additional columns may be accessed by providing valid column addresses, strobing CAS# and holding RAS# LOW, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST-PAGE-MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipelined READs.

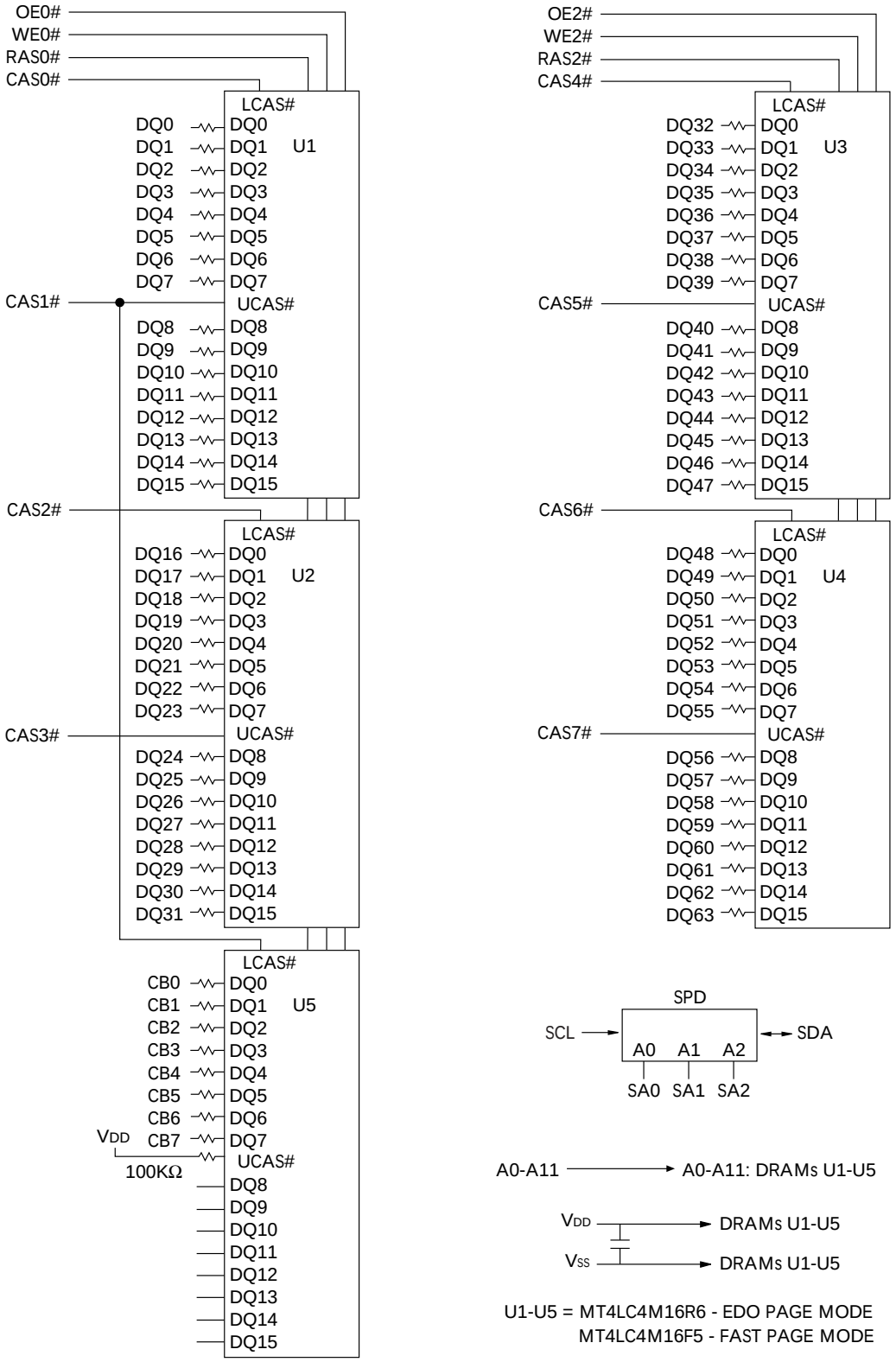
FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO-PAGE-MODE DRAMs operate like FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS# goes HIGH during READs, provided RAS# and OE# are held LOW. If OE# is pulsed while RAS# and CAS# are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE# is toggled or pulsed after CAS# goes HIGH while RAS# remains LOW, data will transition to and remain High-Z.

During an application, if the DQ outputs are wire OR'd, OE# must be used to disable idle banks of DRAMs. Alternatively, pulsing WE# to the idle banks during CAS# HIGH time will also tristate the outputs. Independent of OE# control, the outputs will disable after ^{t}OFF, which is referenced from the rising edge of RAS# or CAS#, whichever occurs last. (Refer to the 4 Meg x 16 [MT4LC4M16R6] DRAM data sheet for additional information on EDO functionality.)

REFRESH

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time. Correct memory cell data is preserved by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses are executed at least every ^{t}REF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing.

FUNCTIONAL BLOCK DIAGRAM
MT5LDT472A (X) (32MB)



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45	RAS0#, RAS2#	Input	Row-Address Strobe: RAS# is used to clock in the row-address bits. Two RAS# inputs allow for one x72 bank or two x36 banks.
28, 29, 46, 47, 112, 113, 130, 131	CAS0#-CAS7#	Input	Column-Address Strobe: CAS# is used to clock in the column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles.
27, 48	WE0#, WE2#	Input	Write Enable: WE# is the READ/WRITE control for the DQ pins. If WE# is LOW prior to CAS# going LOW, the access is an EARLY WRITE cycle. If WE# is HIGH while CAS# is LOW, the access is a READ cycle, provided OE# is also LOW. If WE# goes LOW after CAS# goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	OE0#, OE2#	Input	Output Enable: OE# is the input/output control for the DQ pins. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-122	A0-A11	Input	Address Inputs: These inputs are multiplexed and clocked by RAS# and CAS#.
2-5, 7-11, 13-17, 19, 20, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103, 104, 139-142, 144, 149-151, 153-156, 158-161	DQ0-DQ63	Input/Output	Data I/Os: For WRITE cycles, DQ0-DQ63 act as inputs to the addressed DRAM location. For READ access cycles, DQ0-DQ63 act as outputs for the addressed DRAM location.
21, 22, 52, 53, 105, 106, 136, 137	CB0-CB7	Input/Output	Check Bits.
42, 62, 111, 115, 125-126, 128, 132, 146	RFU	–	Reserved for Future Use: These pins should be left unconnected.
6, 18, 26, 40, 41, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
1, 12, 23, 32, 43, 54, 64, 68, 78, 85, 96, 107, 116, 127, 138, 148, 152, 162	V_{SS}	Supply	Ground.
82	SDA	Input/Output	Serial Presence-Detect Data. SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
83	SCL	Input	Serial Clock for Presence-Detect. SCL is used to synchronize the presence-detect data transfer to and from the module.
165-167	SA0-SA2	Input	Presence-Detect Address Inputs. These pins are used to configure the presence-detect device.

SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	ENTRY (VERSION)	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
0	NUMBER OF BYTES USED BY MICRON	128	1	0	0	0	0	0	0	0	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256	0	0	0	0	1	0	0	0	08
2	MEMORY TYPE	FAST PAGE MODE	0	0	0	0	0	0	0	1	01
		EDO PAGE MODE	0	0	0	0	0	0	1	0	02
3	NUMBER OF ROW ADDRESSES	12	0	0	0	0	1	1	0	0	0C
4	NUMBER OF COLUMN ADDRESSES	10	0	0	0	0	1	0	1	0	0A
5	NUMBER OF BANKS	1	0	0	0	0	0	0	0	1	01
6	DATA WIDTH	x72	0	1	0	0	1	0	0	0	48
7	DATA WIDTH (continued)	NONE	0	0	0	0	0	0	0	0	00
8	VOLTAGE INTERFACE	LVTTL	0	0	0	0	0	0	0	1	01
9	RAS# ACCESS TIME (^{t}RAC)	50ns (-5)	0	0	1	1	0	0	1	0	32
		60ns (-6)	0	0	1	1	1	1	0	0	3C
10	CAS# ACCESS TIME (^{t}CAC)	13ns (-5)	0	0	0	0	1	1	0	1	0D
		15ns (-6)	0	0	0	0	1	1	1	1	0F
11	MODULE CONFIGURATION TYPE	ECC	0	0	0	0	0	0	1	0	02
12	REFRESH RATES	15.625µs/NORMAL	0	0	0	0	0	0	0	0	00
13	DRAM WIDTH (PRIMARY DRAM)	x16	0	0	0	1	0	0	0	0	10
14	ERROR-CHECKING DRAM DATA WIDTH	x16	0	0	0	1	0	0	0	0	10
15-61	RESERVED		0	0	0	0	0	0	0	0	00
62	SPD REVISION	REV. 0	0	0	0	0	0	0	0	0	00
63	CHECKSUM FOR BYTES 0-62	32MB -5 (EDO)	0	1	0	0	1	0	1	1	4B
		32MB -6 (EDO)	0	1	0	1	0	1	1	1	57
		32MB -6 (FPM)	0	1	0	1	0	1	1	0	56
64	MANUFACTURER'S JEDEC ID CODE	MICRON	0	0	1	0	1	1	0	0	2C
65-71	MANUFACTURER'S JEDEC CODE (CONT.)		1	1	1	1	1	1	1	1	FF
72	MANUFACTURING LOCATION		0	0	0	0	0	0	0	1	01
			0	0	0	0	0	0	1	0	02
			0	0	0	0	0	0	1	1	03
			0	0	0	0	0	1	0	0	04
73-90	MODULE PART NUMBER (ASCII)		x	x	x	x	x	x	x	x	xx
91	PCB IDENTIFICATION CODE	1	0	0	0	0	0	0	0	1	01
		2	0	0	0	0	0	0	1	0	02
		3	0	0	0	0	0	0	1	1	03
		4	0	0	0	0	0	1	0	0	04
92	IDENTIFICATION CODE (CONT.)	0	0	0	0	0	0	0	0	0	00
93	YEAR OF MANUFACTURE IN BCD		x	x	x	x	x	x	x	x	xx
94	WEEK OF MANUFACTURE IN BCD		x	x	x	x	x	x	x	x	xx
95-98	MODULE SERIAL NUMBER		x	x	x	x	x	x	x	x	xx
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)		–	–	–	–	–	–	–	–	–

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
2. x = Variable Data.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Pin Relative to V_{SS} ..... -1V to +4.6V
Voltage on Inputs or I/O Pins
Relative to V_{SS} ..... -1V to +4.6V
Operating Temperature, T_A (ambient) ... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 5W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 30) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE		V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs		V_{IH}	2	V_{DD} + 0.3	V	31
INPUT LOW VOLTAGE: Logic 0; All inputs		V_{IL}	-0.5	0.8	V	31
INPUT LEAKAGE CURRENT:	CAS0#, CAS2#-CAS7#	I_{I1}	-2	2	µA	
Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V	CAS1#, OE2#, WE2#, RAS2#	I_{I2}	-4	4	µA	
(All other pins not under test = 0V)	OE0#, WE0#, RAS0#	I_{I3}	-6	6	µA	
	A0-A11	I_{I4}	-10	10	µA	
OUTPUT LEAKAGE CURRENT: DQ is disabled; 0V ≤ V_{OUT} ≤ V_{DD} + 0.3V	DQ0-DQ63, CB0-CB7	I_{OZ}	-5	5	µA	
OUTPUT LEVELS:		V_{OH}	2.4	–	V	
Output High Voltage (I_{OUT} = -2mA)						
Output Low Voltage (I_{OUT} = 2mA)		V_{OL}	–	0.4	V	

I_{DD} OPERATING CONDITIONS AND MAXIMUM LIMITS

(Notes: 1, 5, 6) (V_{DD} = +3.3V ±0.3V)

		MAX			
PARAMETER/CONDITION	**SYMBOL**	**-5**	**-6**	**UNITS**	**NOTES**
STANDBY CURRENT: TTL (RAS# = CAS# = V_{IH})	I_{DD1}	5	5	mA	
STANDBY CURRENT: CMOS (RAS# = CAS# = V_{DD} - 0.2V)	I_{DD2}	2.5	2.5	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: ^{t}RC = ^{t}RC [MIN])	I_{DD3}	875	825	mA	3, 29
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^{t}PC = ^{t}PC [MIN])	I_{DD4}	525	475	mA	3, 29
OPERATING CURRENT: EDO PAGE MODE ("X" version only) Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^{t}PC = ^{t}PC [MIN])	I_{DD5}	775	625	mA	3, 29
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: ^{t}RC = ^{t}RC [MIN])	I_{DD6}	875	825	mA	3, 29
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^{t}RC = ^{t}RC [MIN])	I_{DD7}	875	825	mA	3, 4

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A11	C_{I1}	28	pF	2
Input Capacitance: CAS0#, CAS2#-CAS7#, SCL, SA0-SA2	C_{I2}	10	pF	2
Input Capacitance: CAS1#, OE2#, WE2#, RAS2#	C_{I3}	17	pF	2
Input Capacitance: OE0#, WE0#, RAS0#	C_{I4}	24	pF	2
Input/Output Capacitance: DQ0-DQ63, CB0-CB7, SDA	C_{IO}	10	pF	2

FAST PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 35) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-5		-6			
PARAMETER	**SYMBOL**	**MIIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from column address	^tAA		25		30	ns	
Column-address hold time (referenced to RAS#)	^tAR	40		45		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Column address to WE# delay time	^tAWD	48		55		ns	23
Access time from CAS#	^tCAC		13		15	ns	14
Column-address hold time	^tCAH	8		10		ns	
CAS# pulse width	^tCAS	13	10,000	15	10,000	ns	
CAS# hold time (CBR Refresh)	^tCHR	15		15		ns	4
CAS# to output in Low-Z	^tCLZ	3		3		ns	25
CAS# precharge time	^tCP	8		10		ns	15
Access time from CAS# precharge	^tCPA		30		35	ns	
CAS# to RAS# precharge time	^tCRP	5		5		ns	
CAS# hold time	^tCSH	50		60		ns	
CAS# setup time (CBR Refresh)	^tCSR	5		5		ns	4
CAS# to WE# delay time	^tCWD	36		40		ns	23
WRITE command to CAS# lead time	^tCWL	13		15		ns	
Data-in hold time	^tDH	8		10		ns	22
Data-in setup time	^tDS	0		0		ns	22
Output disable	^tOD	3	13	3	15	ns	
Output enable	^tOE		13		15	ns	
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^tOEH	13		15		ns	21
Output buffer turn-off delay	^tOFF	3	13	3	15	ns	19, 25, 26
OE# setup prior to RAS# during HIDDEN REFRESH cycle	^tORD	0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	30		35		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	76		85		ns	
Access time from RAS#	^tRAC		50		60	ns	13
RAS# to column-address delay time	^tRAD	13		15		ns	17
Row-address hold time	^tRAH	8		10		ns	
RAS# pulse width	^tRAS	50	10,000	60	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	^tRASP	50	125,000	60	125,000	ns	

FAST PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 35) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-5		-6			
PARAMETER	SYMBOL	MIIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	90		110		ns	
RAS# to CAS# delay time	^tRCD	18		20		ns	16
READ command hold time (referenced to CAS#)	^tRCH	0		0		ns	18
READ command setup time	^tRCS	0		0		ns	
Refresh period (4,096 cycles)	^tREF		64		64	ms	
RAS# precharge time	^tRP	30		40		ns	
RAS# to CAS# precharge time	^tRPC	0		0		ns	
READ command hold time (referenced to RAS#)	^tRRH	0		0		ns	18
RAS# hold time	^tRSH	13		15		ns	
READ-WRITE cycle time	^tRWC	131		155		ns	
RAS# to WE# delay time	^tRWD	73		85		ns	23
WRITE command to RAS# lead time	^tRWL	13		15		ns	
Transition time (rise or fall)	^tT	2	50	2	50	ns	
WRITE command hold time	^tWCH	8		10		ns	
WRITE command hold time (referenced to RAS#)	^tWCR	40		45		ns	
WE# command setup time	^tWCS	0		0		ns	23
WRITE command pulse width	^tWP	8		10		ns	
WE# hold time (CBR Refresh)	^tWRH	10		10		ns	
WE# setup time (CBR Refresh)	^tWRP	10		10		ns	

EDO PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 29) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column address	^tAA		25		30	ns	
Column-address setup to CAS# precharge during WRITEs	^tACH	12		15		ns	
Column-address hold time (referenced to RAS#)	^tAR	38		45		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Column address to WE# delay time	^tAWD	42		49		ns	23
Access time from CAS#	^tCAC		13		15	ns	14
Column-address hold time	^tCAH	8		10		ns	
CAS# pulse width	^tCAS	8	10,000	10	10,000	ns	
CAS# hold time (CBR Refresh)	^tCHR	8		10		ns	4
CAS# to output in Low-Z	^tCLZ	0		0		ns	
Data output hold after CAS# LOW	^tCOH	3		3		ns	
CAS# precharge time	^tCP	8		10		ns	15
Access time from CAS# precharge	^tCPA		28		35	ns	
CAS# to RAS# precharge time	^tCRP	5		5		ns	
CAS# hold time	^tCSH	38		45		ns	
CAS# setup time (CBR Refresh)	^tCSR	5		5		ns	4
CAS# to WE# delay time	^tCWD	28		35		ns	23
WRITE command to CAS# lead time	^tCWL	8		10		ns	
Data-in hold time	^tDH	8		10		ns	22
Data-in setup time	^tDS	0		0		ns	22
Output disable	^tOD	0	12	0	15	ns	
Output enable	^tOE		12		15	ns	
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^tOEH	8		10		ns	
OE# HIGH hold time from CAS# HIGH	^tOEHC	5		10		ns	
OE# HIGH pulse width	^tOEP	5		5		ns	
OE# LOW to CAS# HIGH setup time	^tOES	4		5		ns	
Output buffer turn-off delay	^tOFF	0	12	0	15	ns	19, 27
OE# setup prior to RAS# during HIDDEN REFRESH cycle	^tORD	0		0		ns	19
EDO-PAGE-MODE READ or WRITE cycle time	^tPC	20		25		ns	
EDO-PAGE-MODE READ-WRITE cycle time	^tPRWC	47		56		ns	
Access time from RAS#	^tRAC		50		60	ns	13
RAS# to column-address delay time	^tRAD	9		12		ns	17
Row-address hold time	^tRAH	9		10		ns	
RAS# pulse width	^tRAS	50	10,000	60	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	^tRASP	50	125,000	60	125,000	ns	
Random READ or WRITE cycle time	^tRC	84		104		ns	
RAS# to CAS# delay time	^tRCD	11		14		ns	16
READ command hold time (referenced to CAS#)	^tRCH	0		0		ns	18
READ command setup time	^tRCS	0		0		ns	

EDO PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 29) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Refresh period (4,096 cycles)	^{t}REF		64		64	ms	
RAS# precharge time	^{t}RP	30		40		ns	
RAS# to CAS# precharge time	^{t}RPC	5		5		ns	
READ command hold time (referenced to RAS#)	^{t}RRH	0		0		ns	18
RAS# hold time	^{t}RSH	13		15		ns	
READ-WRITE cycle time	^{t}RWC	116		140		ns	
RAS# to WE# delay time	^{t}RWD	67		79		ns	23
WRITE command to RAS# lead time	^{t}RWL	13		15		ns	
Transition time (rise or fall)	^{t}T	2	50	2	50	ns	
WRITE command hold time	^{t}WCH	8		10		ns	
WRITE command hold time (referenced to RAS#)	^{t}WCR	38		45		ns	
WE# command setup time	^{t}WCS	0		0		ns	
Output disable delay from WE# (CAS# HIGH)	^{t}WHZ		12		15	ns	
WRITE command pulse width	^{t}WP	5		5		ns	
WE# pulse width for output disable when CAS# HIGH	^{t}WPZ	10		10		ns	
WE# hold time (CBR Refresh)	^{t}WRH	8		10		ns	
WE# setup time (CBR Refresh)	^{t}WRP	8		10		ns	

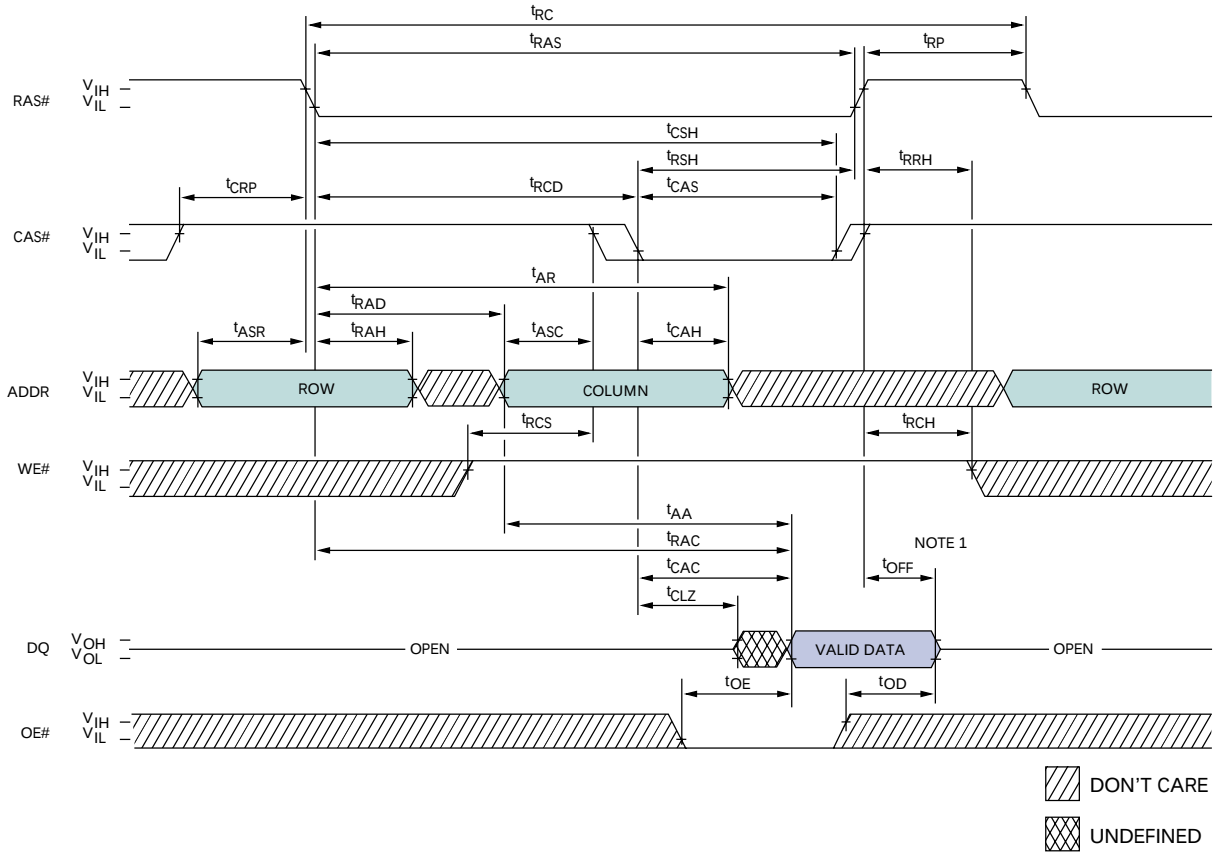
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{DD} = +3.3V; f = 1 MHz.
3. I_{DD} is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# REFRESH cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 5ns for FPM and 2.5ns for EDO.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. For FPM: If CAS# = V_{IH}, data output is High-Z. For EDO: If CAS# and RAS# = V_{IH}, data output is High-Z.
11. If CAS# = V_{IL}, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF and V_{OL} = 0.8V and V_{OH} = 2V.
13. Requires that ^{t}AA and ^{t}CAC are not violated.
14. Requires that ^{t}AA and ^{t}RAC are not violated.
15. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ^{t}CP.
16. The ^{t}RCD (MAX) limit is no longer specified. ^{t}RCD (MAX) was specified as a reference point only. If ^{t}RCD was greater than the specified ^{t}RCD (MAX) limit, then access time was controlled exclusively by ^{t}CAC (^{t}RAC [MIN] no longer applied). With or without the ^{t}RCD (MAX) limit, ^{t}AA and ^{t}CAC must always be met.
17. The ^{t}RAD (MAX) limit is no longer specified. ^{t}RAD (MAX) was specified as a reference point only. If ^{t}RAD was greater than the specified ^{t}RAD (MAX) limit, then access time was controlled exclusively by ^{t}AA (^{t}RAC and ^{t}CAC no longer applied). With or without the ^{t}RAD (MAX) limit, ^{t}AA, ^{t}RAC and ^{t}CAC must always be met.
18. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
19. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
21. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
22. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
23. A +5ns timing skew from the DRAM to the module resulted from the addition of line drivers.
24. A -2ns (MIN) and a -5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
25. A +2ns (MIN) and a +5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
26. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS# remains LOW and OE# is taken back LOW after ^{t}OEH is met. If CAS# goes HIGH prior to OE# going back LOW, the DQs will remain open.
27. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
28. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}WCS < ^{t}WCS (MIN) and ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW result in a LATE WRITE (OE#-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
29. Column address changed once each cycle.
30. The 3ns minimum parameter guaranteed by design.

NOTES (continued)

31. ^{t}PDOFF MAX is determined by the pull-up resistor value. Care must be taken to ensure adequate recovery time prior to reading valid up-level on subsequent DIMM position.
32. Measured with specified current load and 100pF.
33. With the FPM option, ^{t}OFF is determined by the first RAS# or CAS# signal to transition HIGH. In comparison, ^{t}OFF on an EDO option is determined by the latter of the RAS# and CAS# signals to transition HIGH.
34. Applies to both FPM and EDO operating modes.
35. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
36. V_{IH} overshoot: V_{IH} (MAX) = V_{DD} + 2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate.

READ CYCLE [34]



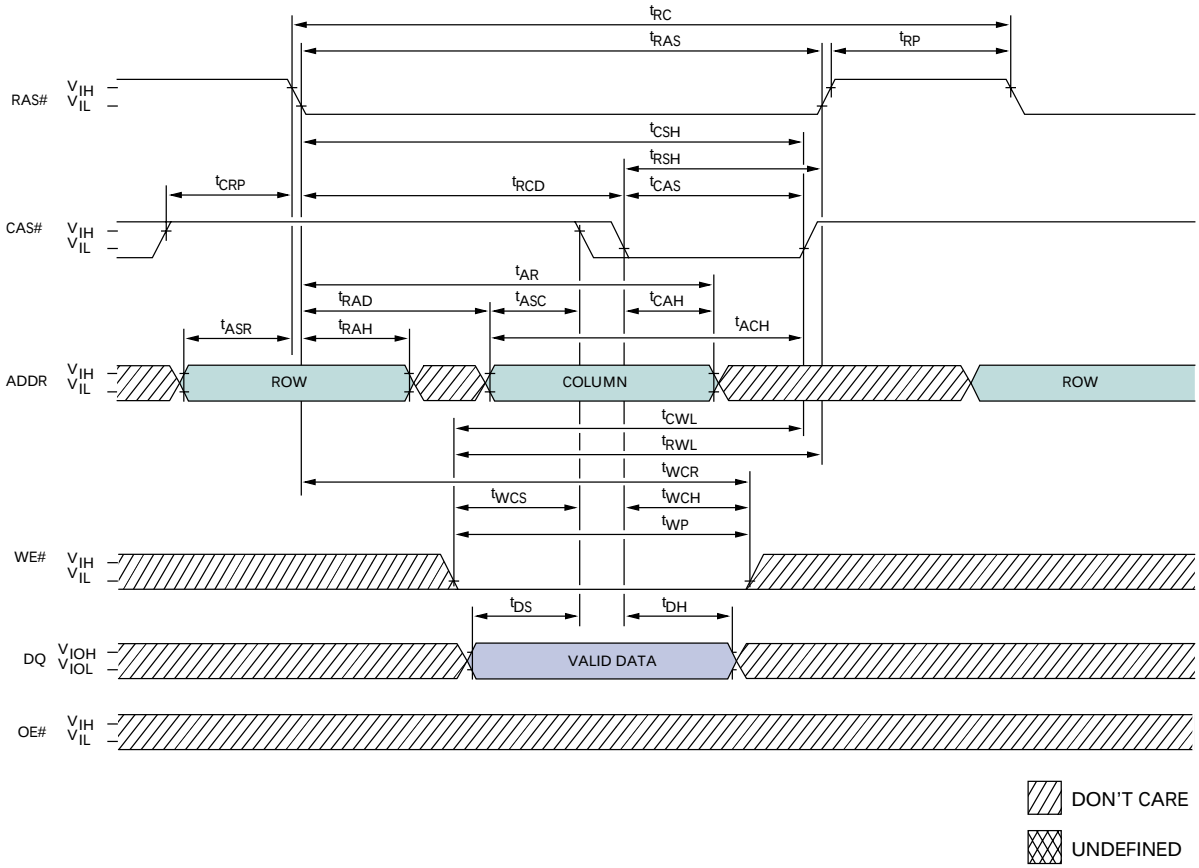
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH (EDO)	12		15		ns
tAR (FPM)	40		45		ns
tAR (EDO)	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS (FPM)	13	10,000	15	10,000	ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCLZ (FPM)	3		3		ns
tCLZ (EDO)	0		0		ns
tCRP	5		5		ns
tCSH (FPM)	50		60		ns
tCSH (EDO)	38		45		ns
tOD (FPM)	3	13	3	15	ns
tOD (EDO)	0	12	0	15	ns
tOE (FPM)		13		15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE (EDO)		12		15	ns
tOFF (FPM)	3	13	3	15	ns
tOFF (EDO)	0	12	0	15	ns
tRAC		50		60	ns
tRAD (FPM)	13		15		ns
tRAD (EDO)	9		12		ns
tRAH (FPM)	8		10		ns
tRAH (EDO)	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRC (FPM)	90		110		ns
tRC (EDO)	84		104		ns
tRCD (FPM)	18		20		ns
tRCD (EDO)	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

NOTE: 1. tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs last.

EARLY WRITE CYCLE [34]

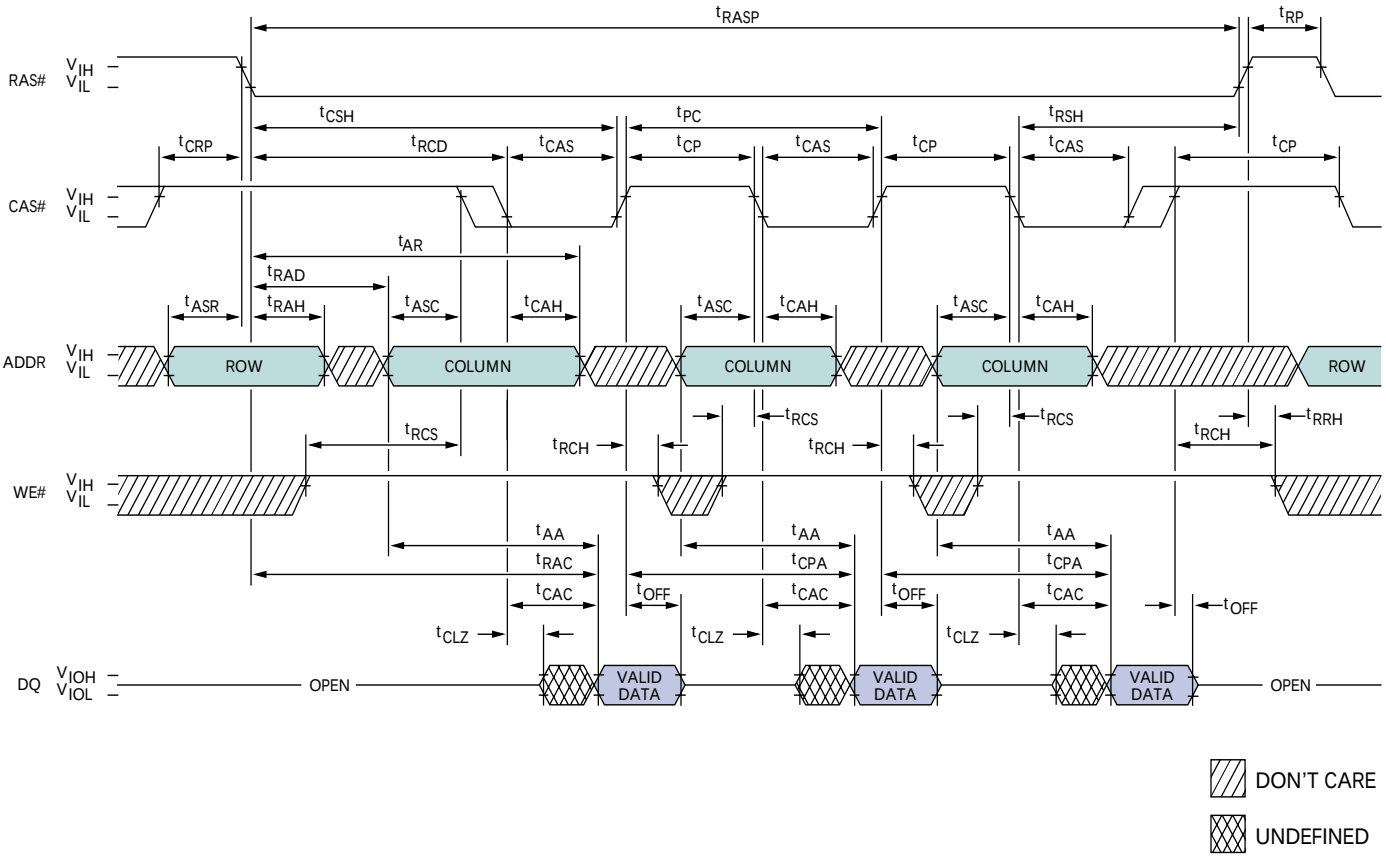


FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tACH (EDO)	12		15		ns
tAR (FPM)	40		45		ns
tAR (EDO)	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS (FPM)	13	10,000	15	10,000	ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCRP	5		5		ns
tCSH (FPM)	50		60		ns
tCSH (EDO)	38		45		ns
tCWL (FPM)	13		15		ns
tCWL (EDO)	8		10		ns
tDH	8		10		ns
tDS	0		0		ns
tRAD (FPM)	13		15		ns
tRAD (EDO)	9		12		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRAH (FPM)	8		10		ns
tRAH (EDO)	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRC (FPM)	90		110		ns
tRC (EDO)	84		104		ns
tRCD (FPM)	18		20		ns
tRCD (EDO)	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR (FPM)	40		45		ns
tWCR (EDO)	38		45		ns
tWCS	0		0		ns
tWP (FPM)	8		10		ns
tWP (EDO)	5		5		ns

FAST-PAGE-MODE READ CYCLE

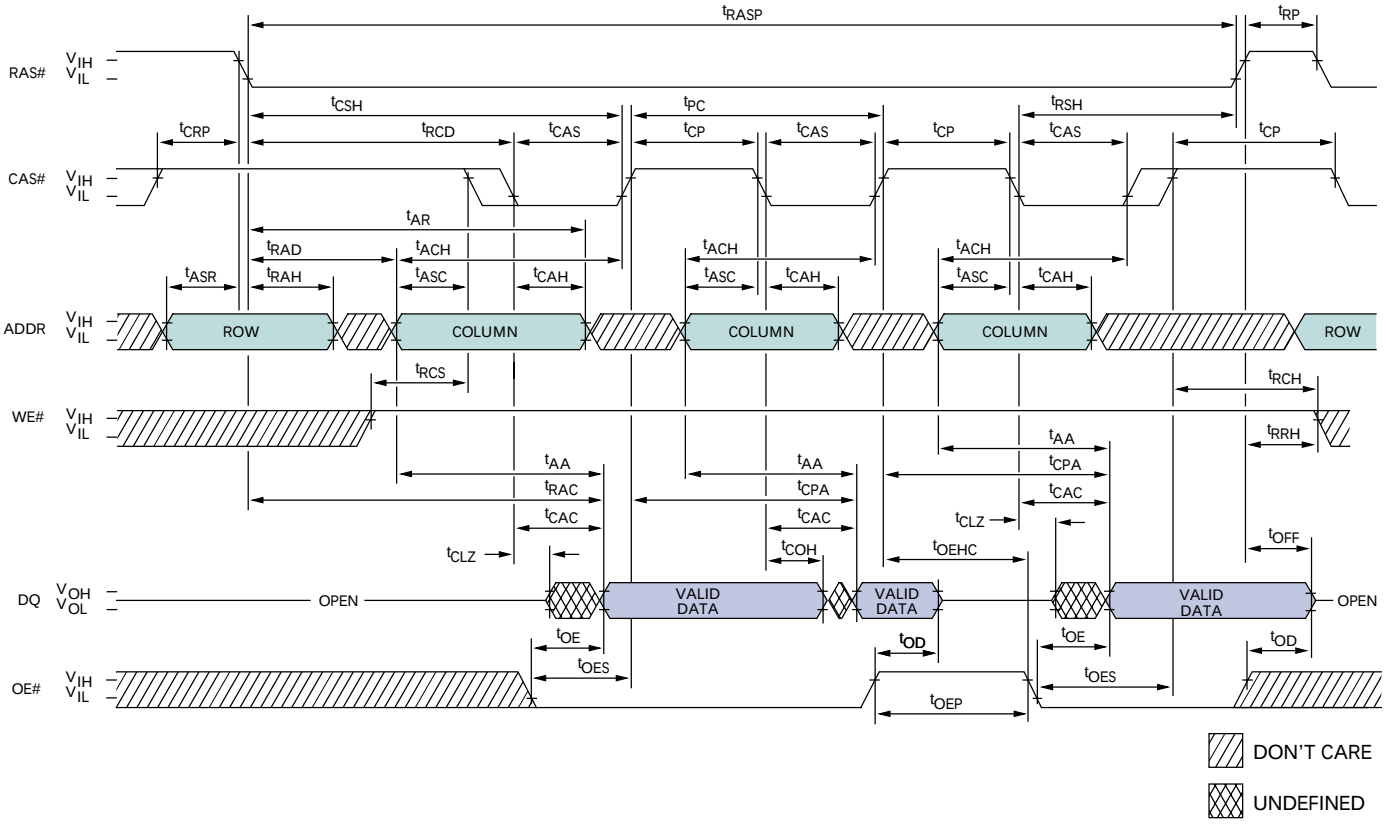


FAST PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	40		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	13	10,000	15	10,000	ns
tCLZ	3		3		ns
tCP	8		10		ns
tCPA		30		35	ns
tCRP	5		5		ns
tCSH	50		60		ns
tOD	3	13	3	15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE		13		15	ns
tOFF	3	13	3	15	ns
tPC	30		35		ns
tRAC		50		60	ns
tRAD	13		15		ns
tRAH	8		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	18		20		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

EDO-PAGE-MODE READ CYCLE

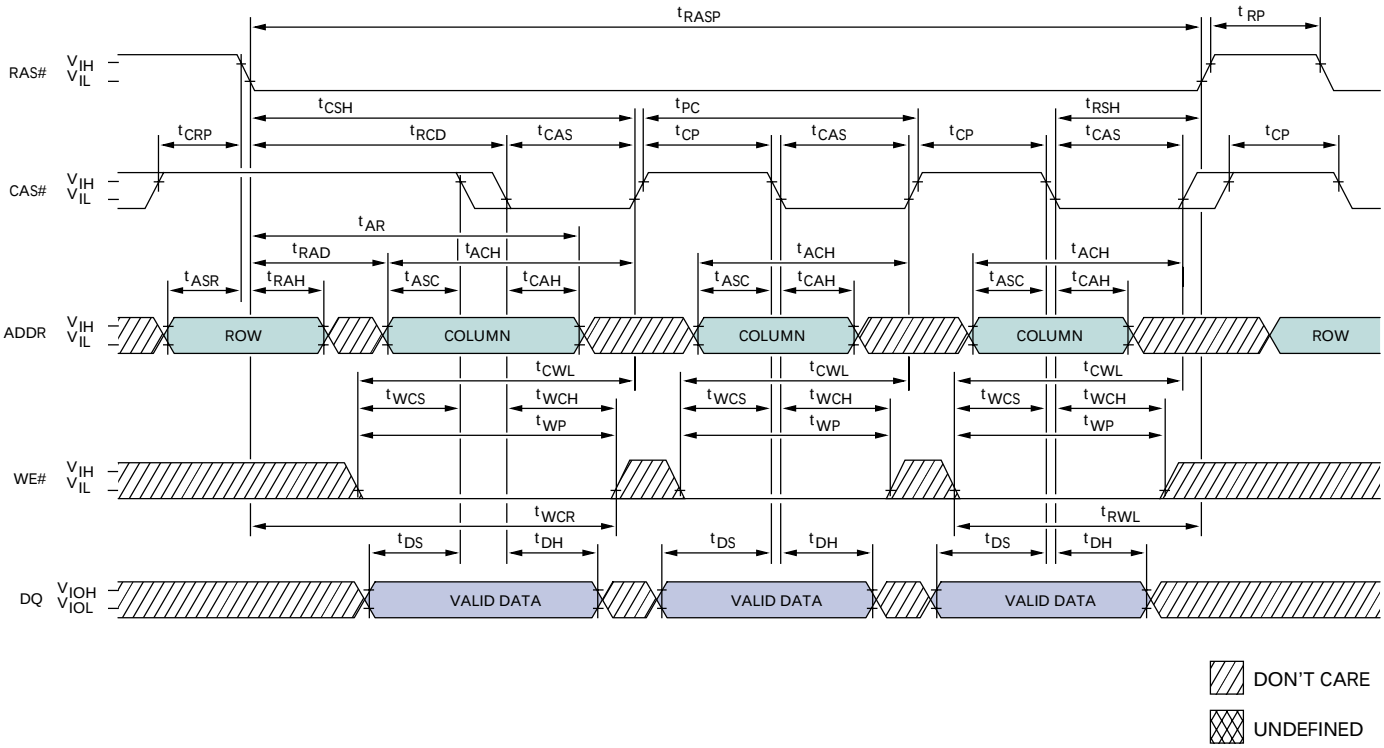


EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tOD	0	12	0	15	ns
tOE		12		15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOEHC	5		10		ns
tOEP	5		5		ns
tOES	4		5		ns
tOFF	0	12	0	15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

FAST/EDO-PAGE-MODE EARLY WRITE CYCLE [34]



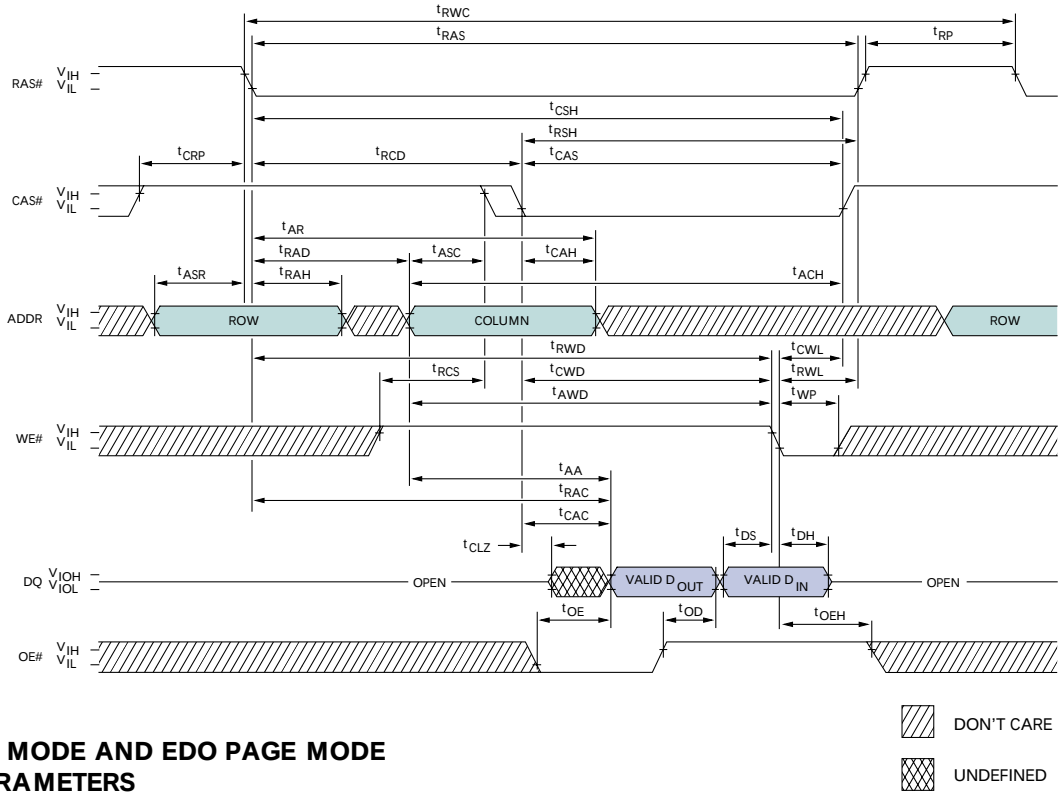
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tACH (EDO)	12		15		ns
tAR (FPM)	40		45		ns
tAR (EDO)	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS (FPM)	13	10,000	15	10,000	ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCP	8		10		ns
tCRP	5		5		ns
tCSH (FPM)	50		60		ns
tCSH (EDO)	38		45		ns
tCWL (FPM)	13		15		ns
tCWL (EDO)	8		10		ns
tDH	8		10		ns
tDS	0		0		ns
tPC (FPM)	30		35		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tPC (EDO)	20		25		ns
tRAD (FPM)	13		15		ns
tRAD (EDO)	9		12		ns
tRAH (FPM)	8		10		ns
tRAH (EDO)	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD (FPM)	18		20		ns
tRCD (EDO)	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR (FPM)	40		45		ns
tWCR (EDO)	38		45		ns
tWCS	0		0		ns
tWP (FPM)	8		10		ns
tWP (EDO)	5		5		ns

READ-WRITE CYCLE [34]

(LATE WRITE and READ-MODIFY-WRITE cycles)



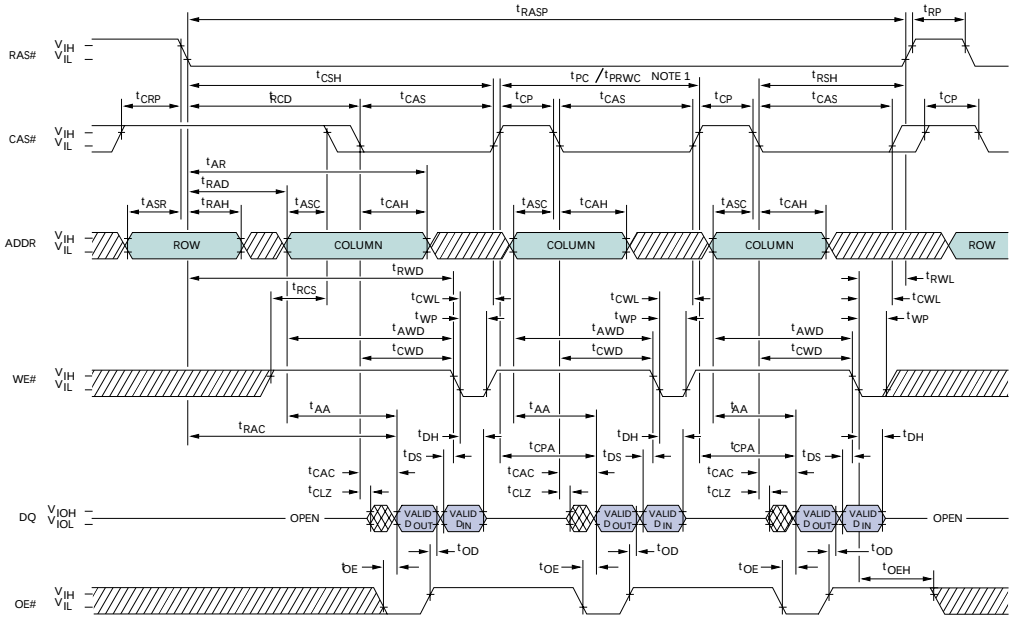
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH (EDO)	12		15		ns
tAR (FPM)	40		45		ns
tAR (EDO)	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD (FPM)	48		55		ns
tAWD (EDO)	42		49		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS (FPM)	13	10,000	15	10,000	ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCLZ (FPM)	3		3		ns
tCLZ (EDO)	0		0		ns
tCRP	5		5		ns
tCSH (FPM)	50		60		ns
tCSH (EDO)	38		45		ns
tCWD (FPM)	36		40		ns
tCWD (EDO)	28		35		ns
tCWL (FPM)	13		15		ns
tCWL (EDO)	8		10		ns
tDH	8		10		ns
tDS	0		0		ns
tOD (FPM)	3	13	3	15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOD (EDO)	0	12	0	15	ns
tOE (FPM)		13		15	ns
tOE (EDO)		12		15	ns
tOEH (FPM)	13		15		ns
tOEH (EDO)	8		10		ns
tRAC		50		60	ns
tRAD (FPM)	13		15		ns
tRAD (EDO)	9		12		ns
tRAH (FPM)	8		10		ns
tRAH (EDO)	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRCD (FPM)	18		20		ns
tRCD (EDO)	11		14		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWC (FPM)	131		155		ns
tRWC (EDO)	116		140		ns
tRWD (FPM)	73		85		ns
tRWD (EDO)	67		79		ns
tRWL	13		15		ns
tWP (FPM)	8		10		ns
tWP (EDO)	5		5		ns

FAST/EDO-PAGE-MODE READ-WRITE CYCLE [34]

(LATE WRITE and READ-MODIFY-WRITE cycles)



FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

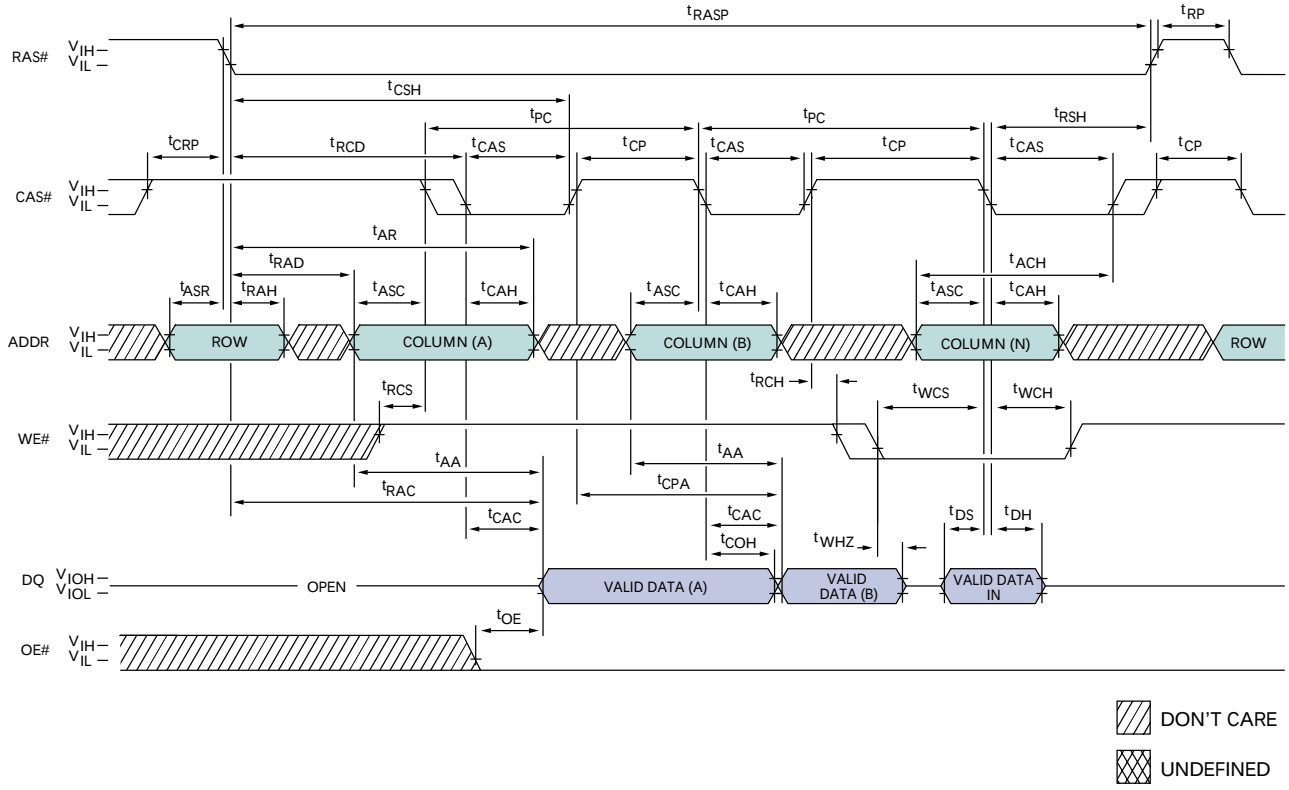
SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR (FPM)	40		45		ns
tAR (EDO)	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD (FPM)	48		55		ns
tAWD (EDO)	42		49		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS (FPM)	13	10,000	15	10,000	ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCLZ (FPM)	3		3		ns
tCLZ (EDO)	0		0		ns
tCP	8		10		ns
tCPA (FPM)		30		35	ns
tCPA (EDO)		28		35	ns
tCRP	5		5		ns
tCSH (FPM)	50		60		ns
tCSH (EDO)	38		45		ns
tCWD (FPM)	36		40		ns
tCWD (EDO)	28		35		ns
tCWL (FPM)	13		15		ns
tCWL (EDO)	8		10		ns
tDH	8		10		ns
tDS	0		0		ns
tOD (FPM)	3	13	3	15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOD (EDO)	0	12	0	15	ns
tOE (FPM)		13		15	ns
tOE (EDO)		12		15	ns
tOEH (FPM)	13		15		ns
tOEH (EDO)	8		10		ns
tPC (FPM)	30		35		ns
tPC (EDO)	20		25		ns
tPRWC (FPM)	76		85		ns
tPRWC (EDO)	47		56		ns
tRAC		50		60	ns
tRAD (FPM)	13		15		ns
tRAD (EDO)	9		12		ns
tRAH (FPM)	8		10		ns
tRAH (EDO)	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD (FPM)	18		20		ns
tRCD (EDO)	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWD (FPM)	73		85		ns
tRWD (EDO)	67		79		ns
tRWL	13		15		ns
tWP (FPM)	8		10		ns
tWP (EDO)	5		5		ns

NOTE: 1. tPC is for LATE WRITE cycles only.

EDO-PAGE-MODE READ EARLY WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



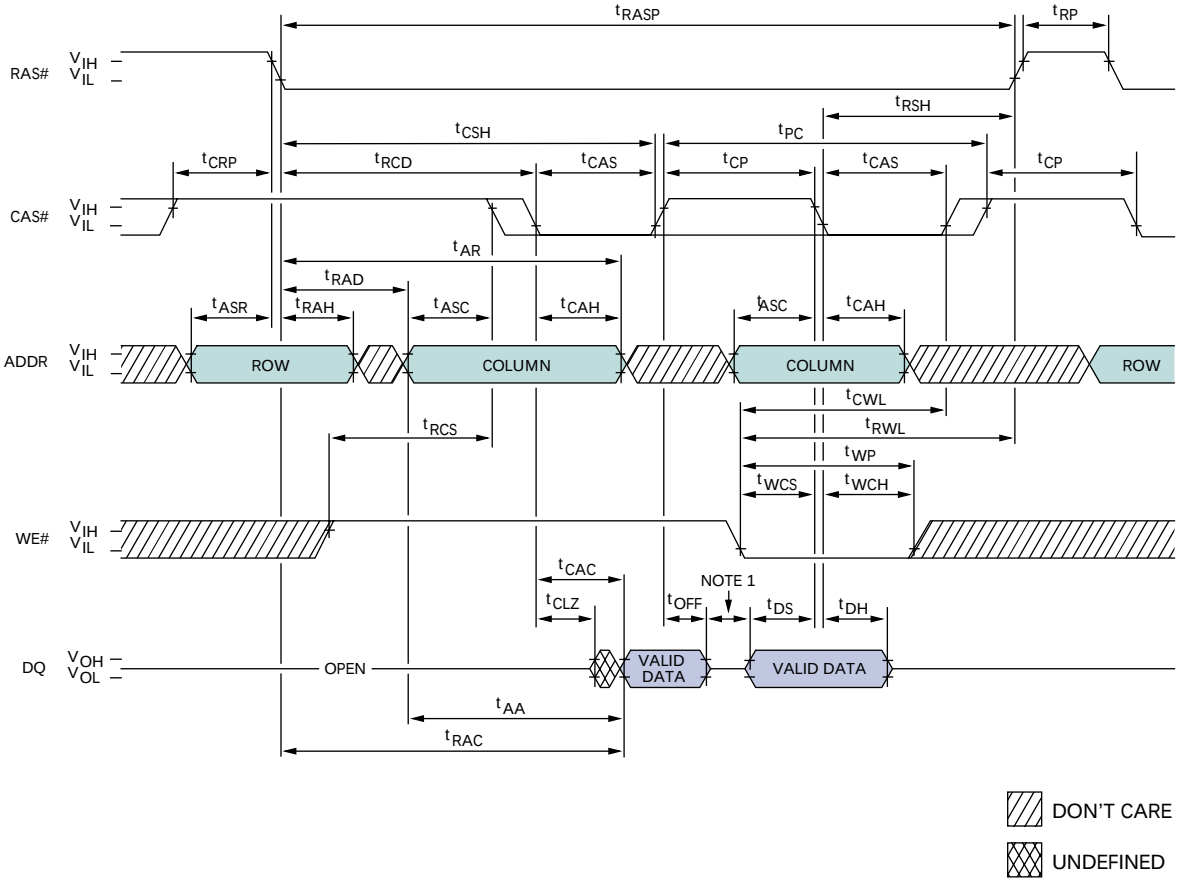
EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE		12		15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tWCH	8		10		ns
tWCS	0		0		ns
tWHZ		12		15	ns

FAST-PAGE-MODE READ EARLY WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



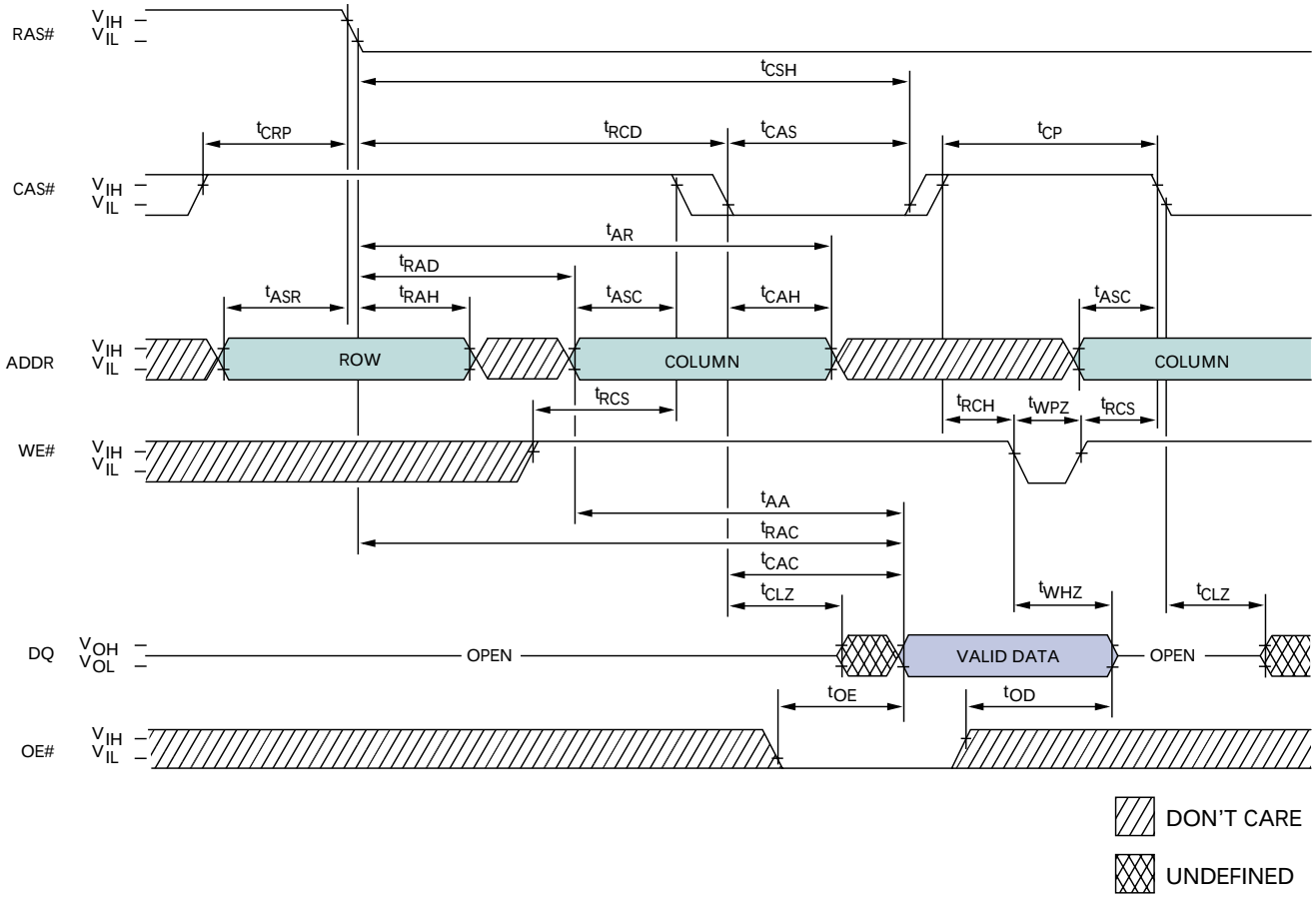
FAST PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	40		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	13	10,000	15	10,000	ns
tCLZ	3		3		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSH	50		60		ns
tCWL	13		15		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOFF	3	13	3	15	ns
tPC	30		35		ns
tRAC		50		60	ns
tRAD	13		15		ns
tRAH	8		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	18		20		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCS	0		0		ns
tWP	8		10		ns

NOTE: 1. Do not drive data prior to tristate.

EDO READ CYCLE
(with WE#-controlled disable)

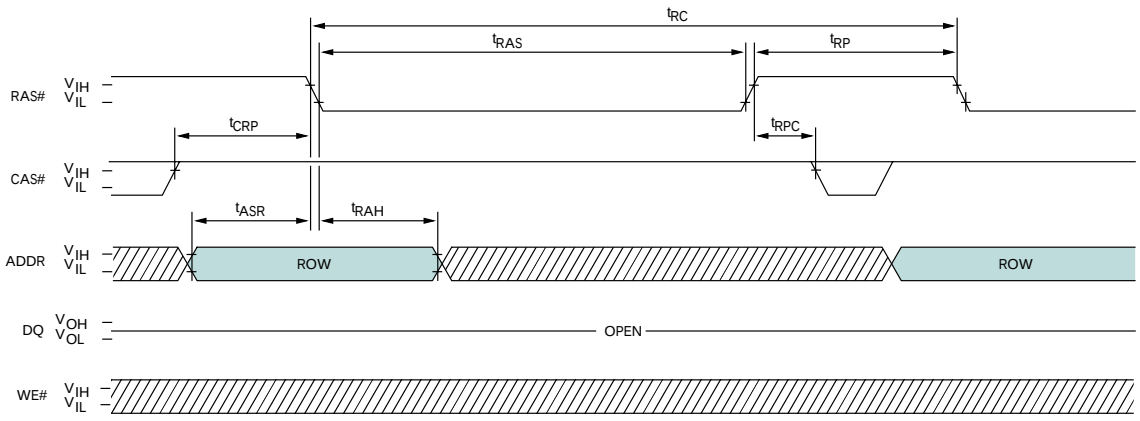


EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSH	38		45		ns

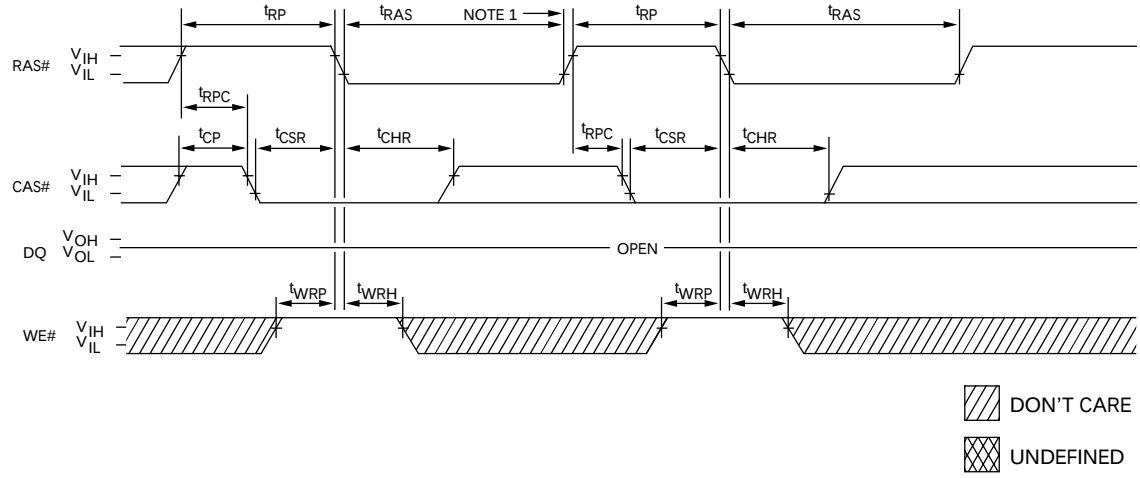
SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOD	0	12	0	15	ns
tOE		12		15	ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tWHZ		12		15	ns
tWPZ	10		10		ns

RAS#-ONLY REFRESH CYCLE [34]



CBR REFRESH CYCLE [34]

(Addresses, OE# = DON'T CARE)



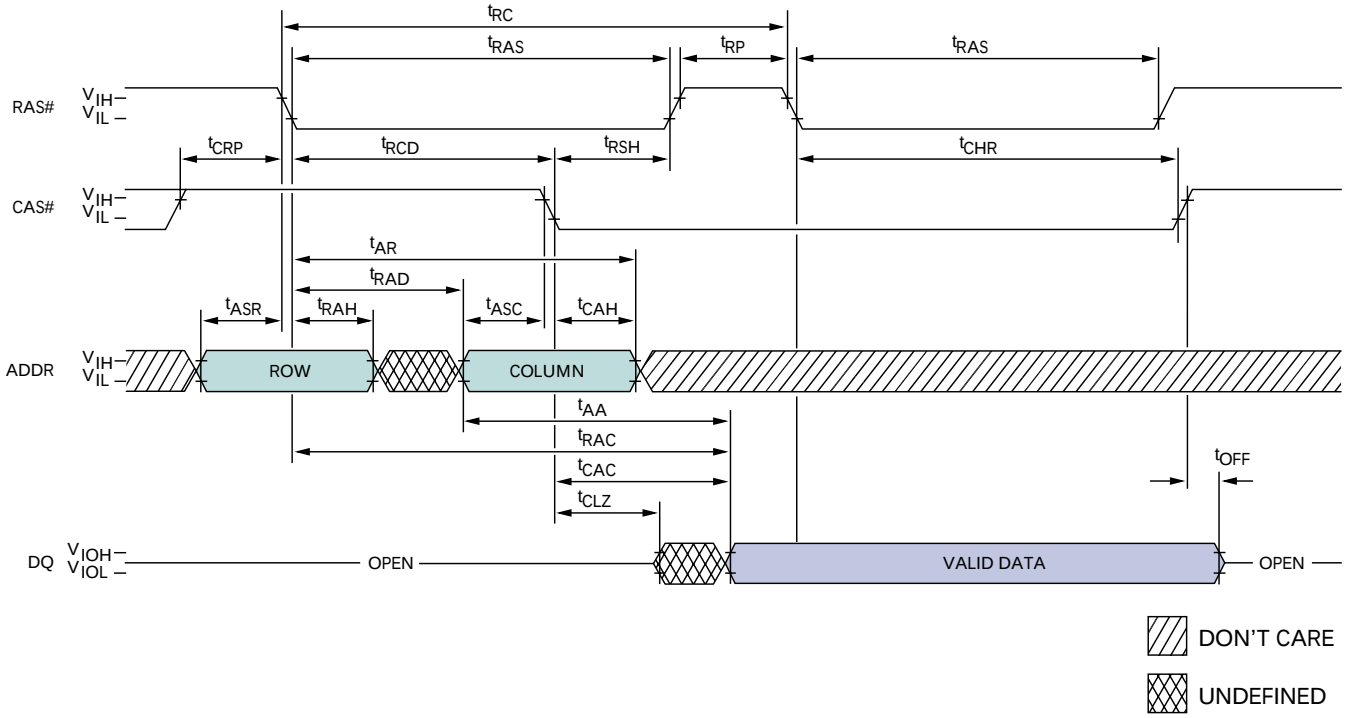
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tASR	0		0		ns
tCHR (FPM)	15		15		ns
tCHR (EDO)	8		10		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSR	5		5		ns
tRAH (FPM)	8		10		ns
tRAH (EDO)	9		10		ns
tRAS	50	10,000	60	10,000	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRC (FPM)	90		110		ns
tRC (EDO)	84		104		ns
tRP	30		40		ns
tRPC (FPM)	0		0		ns
tRPC (EDO)	5		5		ns
tWRH (FPM)	10		10		ns
tWRH (EDO)	8		10		ns
tWRP (FPM)	10		10		ns
tWRP (EDO)	8		10		ns

HIDDEN REFRESH CYCLE [20, 34]

(WE# = HIGH; OE# = LOW)



FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

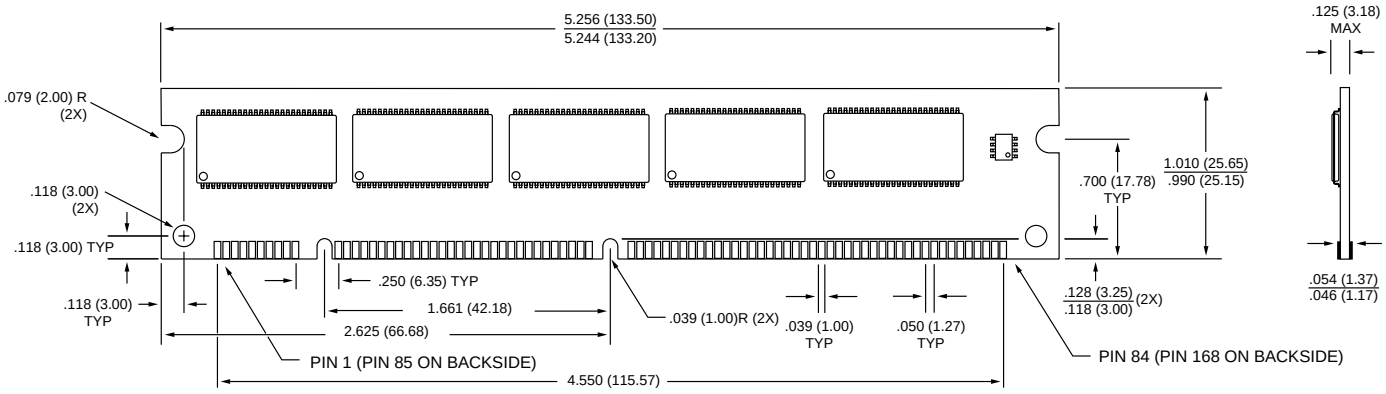
SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR (FPM)	40		45		ns
tAR (EDO)	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCHR (FPM)	15		15		ns
tCHR (EDO)	8		10		ns
tCLZ (FPM)	3		3		ns
tCLZ (EDO)	0		0		ns
tCRP	5		5		ns
tOD (FPM)	3	13	3	15	ns
tOD (EDO)	0	12	0	15	ns
tOE (FPM)		13		15	ns
tOE (EDO)		12		15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOFF (FPM)	3	13	3	15	ns
tOFF (EDO)	0	12	0	15	ns
tORD	0		0		ns
tRAC		50		60	ns
tRAD (FPM)	13		15		ns
tRAD (EDO)	9		12		ns
tRAH (FPM)	8		10		ns
tRAH (EDO)	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRC (FPM)	90		110		ns
tRC (EDO)	84		104		ns
tRCD (FPM)	18		20		ns
tRCD (EDO)	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns

168-PIN DIMM

(32MB)

FRONT VIEW



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
E-mail: prodmktg@micron.com, Internet: http://www.micron.com, Customer Comment Line: 800-932-4992