Replacement of
TL074C

Quad Low-Noise J-FET Operational Amplifier

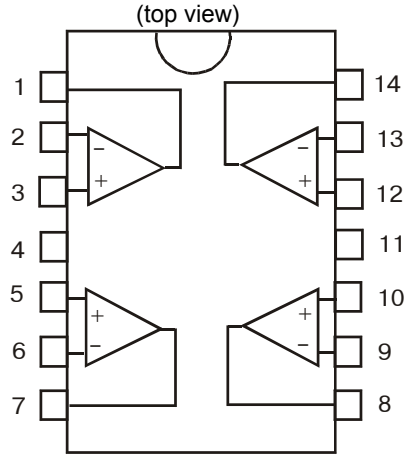
MIK074C

January 2002 - revised June 2002

Features

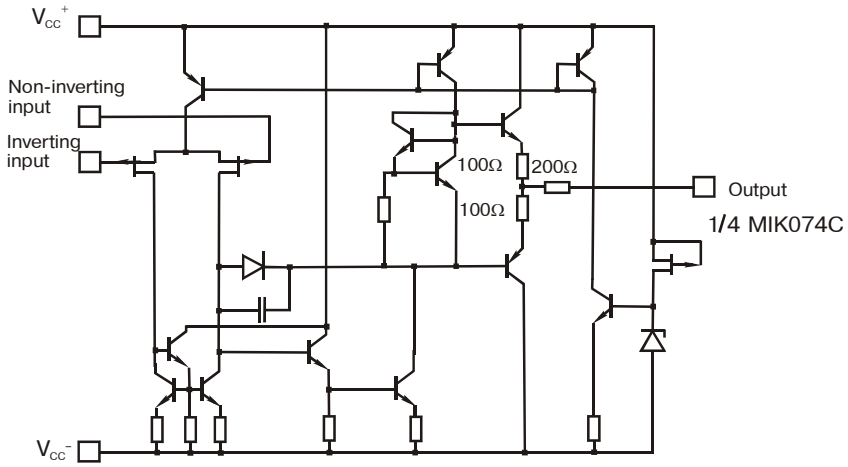
- Low power consumption
- Wide common-mode and differential voltage range
- Low input bias and offset currents
- Low noise e_n=18nV/√Hz(typ)
- Output short-circuit protection
- High input impedance J-FET input stage
- Low harmonic distortion: 0.01% (typ)
- Internal frequency compensation
- Latch up free operation
- High slew rate: 13 V/μs (typ)

Pin Connections



Pad N	Pad Name
1	Output 1
2	Inverting input 1
3	Non-inverting input 1
4	V_{CC} +
5	Non-inverting input 2
6	Inverting input 2
7	Output 2
8	Output 3
9	Inverting input 3
10	Non-inverting input 3
11	V_{CC} -
12	Non-inverting input 4
13	Inverting input 4
14	Output 4

Schematic Diagram



Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage – (Note 1)	±18	V
V_i	Input Voltage – (Note 3)	±15	V
V_{id}	Differential Input Voltage – (Note 2)	±30	V
	Output Short-circuit Duration (Note 4)	Infinite	
T_{oper}	Operating Free-Air Temperature Range MIK074C	0 to 70	^{0}C

Note 1: All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
Note 2: Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
Note 3: The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
Note 4: The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

Electrical Characteristics

V_{CC} = ± 15V, T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameters	Min	Typ	Max	Units
V_{IO}	Input Offset Voltage (R_S = 50Ω, V_0=0) T_{amb} =25°C $T_{min.} \le T_{amb.} \le T_{max.}$		3	10 13	mV
DV_{IO}	Input Offset Voltage Drift		18		µV/°C
I_{IO}	Input Offset Current* T_{amb} =25°C $T_{min.} \le T_{amb.} \le T_{max.}$		5	100 10	pA nA
I_{IB}	Input Bias Current* T_{amb} =25°C $T_{min.} \le T_{amb.} \le T_{max.}$		65	200 20	pA nA
A_{VD}	Large Signal Voltage Gain (R_L = 2kΩ, V_O =± 10V) T_{amb} =25°C $T_{min.} \le T_{amb.} \le T_{max.}$	25 15	200		V/mV
SVR	Supply Voltage Rejection Ratio (R_S = 50Ω, V_0=0) T_{amb} =25°C $T_{min.} \le T_{amb.} \le T_{max.}$	70 70	86		dB
I_{CC}	Supply Current (Per Amplifier) T_{amb} =25°C $T_{min.} \le T_{amb.} \le T_{max}$		1.4	2.5 2.5	mA
V_{ICM}	Input Common Mode Voltage Range	±11	+15 -12		V
CMR	Common Mode Rejection Ratio (R_S = 50Ω, V_0=0) T_{amb} =25°C	70	86		dB
$\pm V_{OPP}$	Output Voltage Swing T_{amb} =25°C R_L=10kΩ $T_{min.} \le T_{amb.} \le T_{max.}$ R_L=2kΩ R_L=10kΩ	12 10 12	13.5		V
SR	Slew Rate (V_i = 10V, R_L= 2kΩ, C_L = 100pF, T_{amb} =25°C, unity gain)	8	13		V/µs
t_r	Rise Time (V_i = 20mV, R_L= 2kΩ, C_L =100pF, T_{amb} =25°C, unity gain)		0.1		µs
K_{OV}	Overshoot (V_i = 20mV, R_L= 2kΩ, C_L =100pF, T_{amb} =25°C, unity gain)		20		%
GBP	Gain Bandwidth Product		3		MHz
R_I	Input Resistance		10^{12}		Ω
THD	Total Harmonic Distortion (f=1kHz, R_L= 2kΩ, T_{amb} =25°C)		0.01		%
e_n	Equivalent input Noise Voltage (R_S = 100Ω, f = 1KHz)		18		$\frac{nV}{\sqrt{Hz}}$
V_{O1}/V_{O2}	Channel Separation (A_V =100)		120		dB

* The Input bias currents are junction leakage currents which approximately double for every 10^0C increase in the junction temperature.

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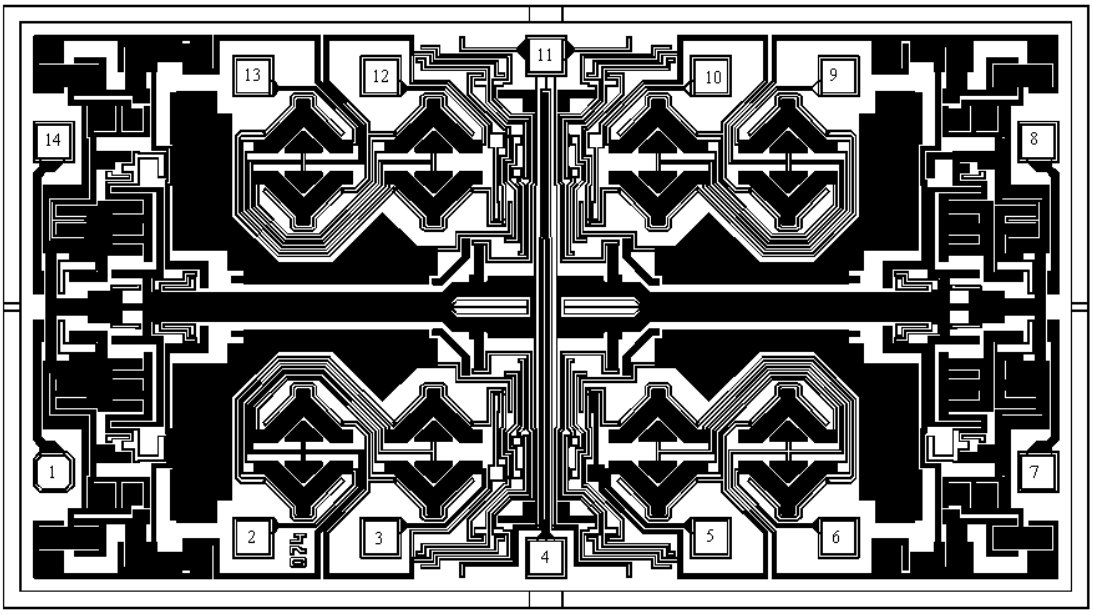
Pad location MIK074C



Ship size 3.25 x 1.8 mm

Pad Location Coordinates

Pad	Pad Name	Coordinates µm	
		X	Y
1	Output 1	150	406
2	Inverting input 1	748	210
3	Non-inverting input 1	1131	210
4	V_{CC} +	1625	150
5	Non-inverting input 2	2119	210
6	Inverting input 2	2502	210
7	Output 2	3100	406
8	Output 3	3100	1394
9	Inverting input 3	2502	1590
10	Non-inverting input 3	2119	1590
11	V_{CC} -	1625	1650
12	Non-inverting input 4	1131	1590
13	Inverting input 4	748	1590
14	Output 4	150	1394

Note: Contact Pad#1 has chamfered corners.