VP520S

PAL/NTSC to CIF/QCIF Converter

Advance Information

Supersedes version in June 1995 Digital Video & DSP IC Handbook, HB3923-2 DS3504 - 3.2 October 1996

FEATURES

- Lower Power, pin compatible replacement for VP520
- Converts CCIR601 luminance and chrominance to CIF or QCIF resolution, and vice versa, using a 27MHz system clock.
- Luminance and chrominance channels have their own sets of horizontal and vertical filters with on chip line stores
- Each filter set may be configured to either decimate or interpolate.
- NTSC line insertion or removal mode
- Produces / expects CIF/QCIF data in macroblock format.
- 120 Pin QFP Package

ASSOCIATED PRODUCTS

- VP510 Colour Space Converter
- VP2611 H261 Encoder
- VP2615 H261 Decoder
- VP2612 Video Multiplexer
- VP2614 Video Demultiplexer

DESCRIPTION

The VP520S is designed to convert 16 bit multiplexed luminance and chrominance data between CCIR601 and CIF/QCIF resolutions. Vertical and horizontal FIR filters are provided, with the vertical filters supported by on chip line stores. The coefficients used by the filters are user definable, and are down loaded from an independent host data bus. An internal address generator supports an external DRAM frame store, and also provides line to macroblock conversion.

When producing CIF or QCIF video the horizontal filters precede the vertical filters, and are provided with between 8 and 16 taps. The vertical filters are provided with four CIF line delays which allow a 5 tap filter to be implemented. When producing QCIF the available RAM is used to provide six line delays, which thus allows 7 tap filters to be used.

When the device is producing CCIR601 video, the incoming data must be in macroblock format, and the vertical filters precede the horizontal filters The inputs are firstly written to a external CIF sized frame store, and are read out in line format. The VP520S will support two complete frame stores, and allows the CIF/QCIF data to be read out twice in order to produce two interlaced fields of video.

The VP520S supports the conversion between CIF/QCIF and NTSC video. An extra line is produced for every five lines when producing CIF data, and one line in six is removed when producing NTSC video. Poly phase filters are used to provide the correct decimation and interpolation ratios.

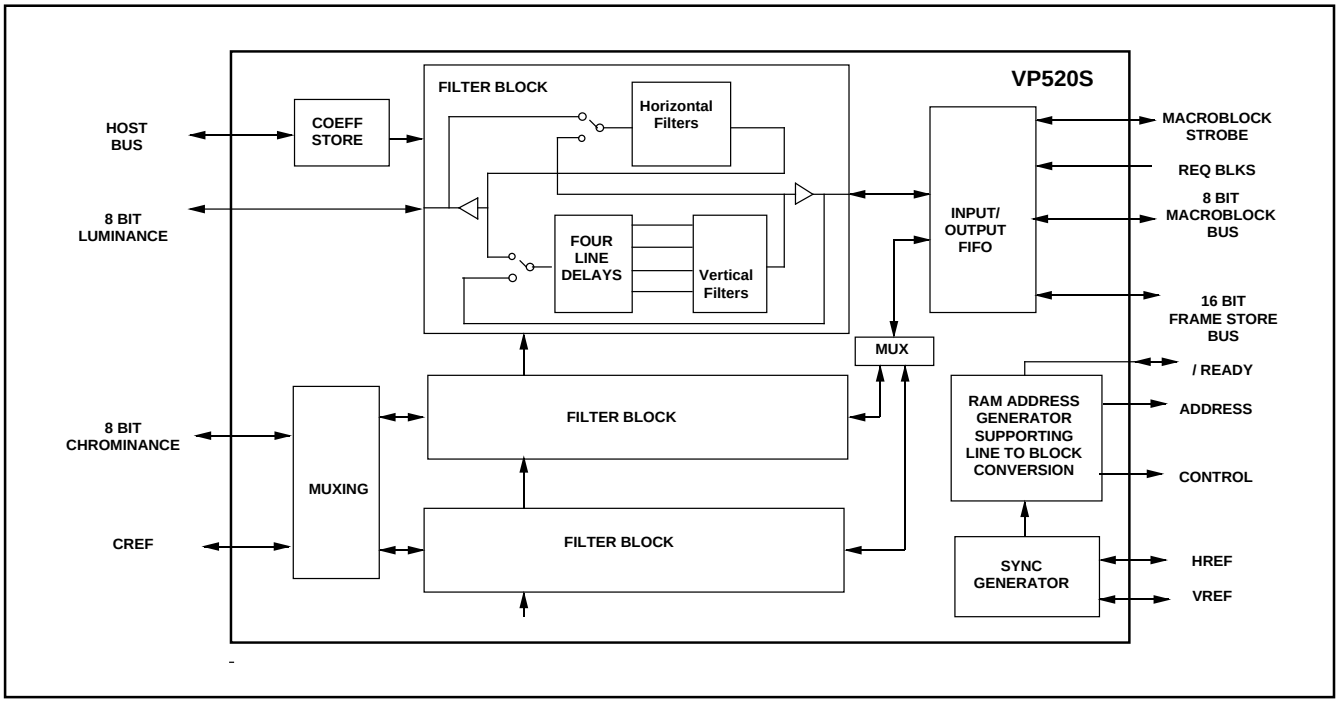


Fig 1 : Simplified Block Diagram

PIN DESCRIPTION

NAME	TYPE	FUNCTION
Y7:0	I/O	Luminance input or output bus
C7:0	I/O	Chrominance input or output bus
M7:0	I/O	Macroblock input or output bus
D15:0	I/O	16 bit data bus for DRAM frame store
A7:0	O	Multiplexed address bus to the DRAM
A8	O	Most sig address bit or second CAS
$\overline{RAS}$	O	Row strobe for the DRAM's
$\overline{CAS}$	O	Column strobe for the DRAM's
R/$\overline{W}$	O	Read/ write signal to the DRAM's
HREF	I/O	Horiz. reference in or horiz. sync out
VREF	I/O	Vertical reference in or vertical sync out
CREF	I/O	CREF in or CREF out
FREF	I/O	Field Indicator in or out
$\overline{HBLNK}$	O	Horizontal Blanking output
$\overline{CSYNC}$	O	Composite sync output in free run mode
CLMP	O	Defines a black level clamping period for A/D converters
VRST		Frame start identifier. If FRST is low then a low going edge will reset the internal sync generator.
FRST		Field identifier
REQYUV	I	Request macroblocks from encoder
MCLK	I/O	Macroblock I/O strobe
FSIG	I/O	Frame start/ ready signal
SCLK	I	System Clock. 27MHz in PAL/NTSC systems
HD7:0	I/O	Host data bus
HA3:0	I	Host controller address bits
$\overline{RD}$	I	An active low host read strobe
$\overline{WR}$	I	An active low host write strobe
$\overline{CEN}$	I	An active low enable for the strobes
$\overline{RST}$	I	Power on reset
TDI	I	JTAG I/P data
TDO	O	JTAG O/P data
TMS	I	Test mode select
TCK	I	JTAG clock
$\overline{TRST}$	I	JTAG reset
TOE	I	When high all O/P's are high impedance

NOTE:
"Barred" active low signals do not appear with a bar in the main body of the text.

VIDEO COMPRESS MODE (DECIMATE)

This mode is used when CCIR601 video is to be converted to CIF or QCIF spatial resolution prior to compression. Incoming luminance and chrominance data does not need any prior buffering, but must meet the timing requirements given in Figure 2. A bit in Control register 1 allows the Cb component to precede the Cr component if necessary. This data is passed through vertical and horizontal decimating filters before it is stored in an external frame store. When a complete field has been decimated it is read out in macroblock format and transferred to the next system component.

In this mode HREF, VREF, and FREF are normally inputs which are used to reference active video with respect to video synchronization pulses. The active going edges are used internally, and these must meet the set up time with respect to the system clock as given in Figure 2. Stable inputs are needed with no jitter due to asynchronous pixel clocks, but when this is not possible an external FIFO can be used plus two extra signals as described later. The reference inputs need only stay active for one system clock period. Note that the active going edges for HREF and VREF can individually be defined to be high going or low going, through two bits in Control Register 0. Also note that CREF is always an input and is used as a qualifier for SCLK. The actual edges of CREF are not used.

The internal sync generator can still be used in this mode, if there is a need to supply sync to the video source. The HREF and VREF pins are then used to output HSYNC and VSYNC. Composite sync is supplied on the CSYNC pin.

In addition the CLMP pin provides a pulse [13 SCLK's wide] which can be used to DC restore the black level in an A/D converter. It is active high during the back porch.

The horizontal blanking output (HBLANK) defines when the device expects the first pixel in a line to be supplied, and is derived from the user supplied HREF input. The delay between HREF and HBLANK is user definable in multiples of CREF periods. If the defined value is zero then the HREF input must be horizontal blanking with the minimum set time specified. The HBLANK output is then not defined.

All data changes are referenced to the system clock. The edge actually used is indicated by the CREF input signal, which has a period of double the clock period. The VP520S will strobe in data on the rising edge of the system clock which occurs whilst CREF is high.

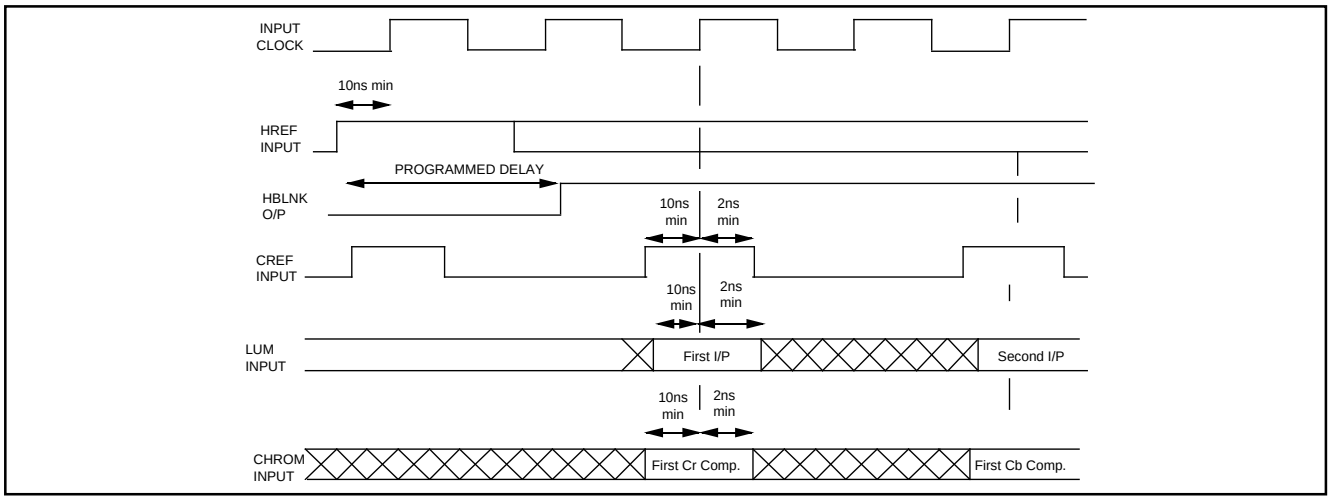


Fig 2 : Luminance and chrominance inputs in the decimate mode.

The first video line to be filtered and stored will be derived from the vertical reference input (VREF). The user can choose the number of transitions of the HREF input which must occur, after VREF has gone active, before starting the filter operation. Data is then not written to the DRAM until after the pipeline delay through the filters.

The VP520S only expects to use one field of CCIR601 video, which can be selected by the FREF input or internal logic. A bit in Control Register 1 (Internal / External Field Detect) determines which option is to be used. An additional Field Select Bit determines whether the field selected should correspond to FREF being high or low. When the Field Select Bit and the input are at the same logical level then that field is used. Note that FREF transitions must be coincident with active going VREF transitions.

Internal logic is provided which determines the field (Field 1) in which VREF goes active in less than half a line period after the HREF input last went active.The half line period is determined by VREF going active between 1 and 432 CREF qualified SCLK edges after HREF went active (1-429 in NTSC mode). Note that coincident VREF and HREF edges will indicate this field on the first CREF qualified SCLK edge.

This logic is used, rather than the FREF input, when the Internal / External Field Detect Bit is low. Field 1 is selected when the Field Select in Control register 1 is low, and Field 2 is used when the bit is high.

In the Split Screen mode this logic is overridden, and both fields are actually used. External logic is assumed to switch between two sources of video, one for each field. The internal DRAM address generator is modified such that half area pictures from the centre of each source are actually stored as CIF/QCIF data. The first line used in each field will be 72 line delays in addition to the number which has been defined by the user. The split screen option is not supported in the QCIF mode of operation, and a reset is needed after a mode change in CIF.

The VP520S will insert zero's into the line delays during vertical blanking. This ensures that all the filter accumulators are cleared and the edges of the picture are correctly processed. The horizontal filters always give the required results since four decimated values are ignored at either side of the picture.

Incoming luminance data could have a black level of 16, which will be shifted if the filter coefficients are not chosen to exactly give a gain of unity. A Control Bit is thus provided, which when set causes 16 to be subtracted from incoming luminance. A black level of zero will then stay as zero throughout the filter operation. At the output of the filters 16 is always added to the results, regardless of the state of the Control Bit. Saturation logic ensures that these addition / subtraction operations do not produce negative results or values greater than 254.

A Control Bit is also provided which selects between colour difference inputs and true Cr Cb chrominance values. Cr Cb values are 8 bit positive only numbers, with black levels of 128. These must be converted to two's complement signed numbers by subtracting 128, thus giving a black level of zero through the filters. The outputs of the filters are always converted to positive only Cr Cb values by adding 128 to the results, regardless of the state of the Control Bit.

COPING WITH SYNC JITTER

When input syncs to the VP520S have jitter, due to the use of a composite video decoder which does not produce a line locked clock, it is necessary to use an external FIFO line buffer. For this reason the VP520S supports a system in which external line buffer writes are controlled by the video source and line reads are controlled by the VP520S. The VP520S in the decode loop is assumed to be supplying sync to the VP520S in the encode loop, but the sync generator must be reset at the start of a frame to be in step with the video source. Two pins have been supplied to support this situation, namely: VRST - pin 34, and FRST - pin 36. The falling edge of VRST (frame start identifier) when FRST (field identifier) is low identifies the start of the frame. These two inputs can typically be supplied by the Brooktree Bt812 Composite Video Decoder. Note that Host Address 3 must be programmed with the value 02 Hex to enable the reset operation.

CIF/QCIF MACROBLOCK OUTPUTS

When producing decimated CIF/QCIF data in macroblock format, the device raises a flag when a frame of data is ready for reading from the frame store (FSIG). The FSIG pin is automatically configured as an output in the decimate mode, but will only stay active (high) for the time given in Figure 3. If a Request Macroblock response (REQYUV) is not obtained during this period, then FSIG will be taken low and the frame of data presently available will be ignored. It will go high again when a new frame of data is available.

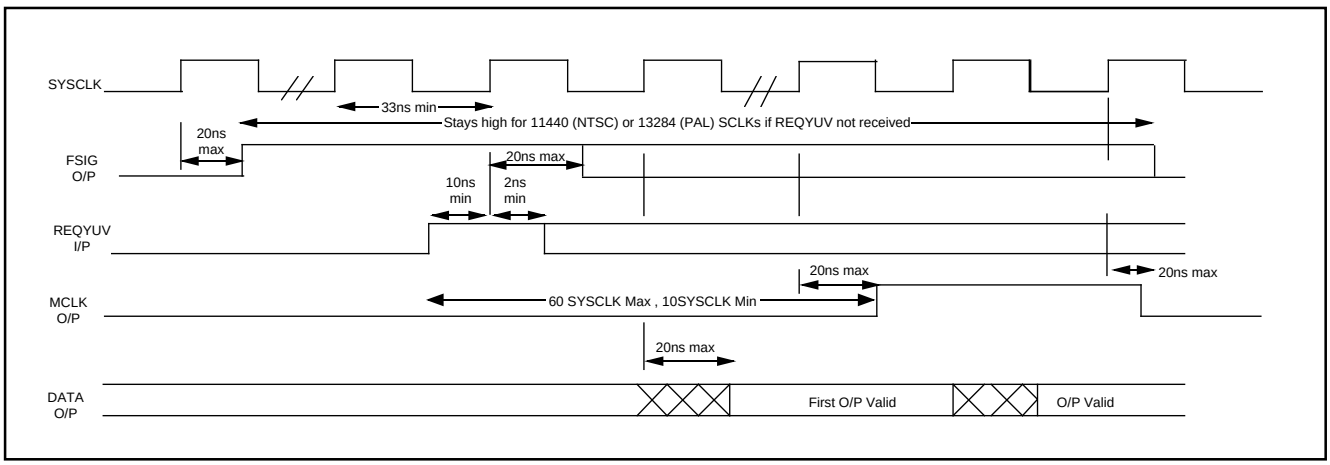


Fig 3 : Macroblock Output Timing

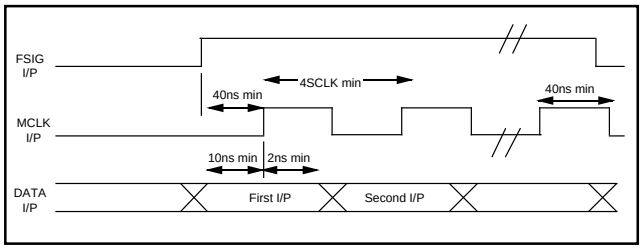


Fig 4 : Macroblock Input Timing

When it receives a REQYUV response from the next system component, it starts to output a macroblock by using an output strobe derived by dividing down the clock input. Detailed timing is given in Figure 3. This strobe only occurs when data is available at the output pins and at a rate of SYSCLK/4. The 'Request Macroblock' flag must go inactive and then active again before a further macroblock is made available.

The Frame Ready flag is only available on the output pin if the Frame Enable Bit is set in Control Register 1. Through this control bit a host controller is able to determine whether a new frame is to be compressed and transmitted. In an alternative arrangement the control bit can be permanently set, and the Frame Ready Flag is then used as an interrupt to the host controller. It then generates a signal which is used as the Frame Ready signal for the next device.

The following sections describe this interface as it applies to the VP2611 H261 Video Encoder.

TRANSFERING MACROBLOCKS TO THE VP2611

When the VP520S has stored a complete field of decimated video in the DRAM, it raises a Frame Ready Flag (FSIG). If the bit in Control Register 1 does not inhibit the output, this flag becomes the FRMIN input on the VP2611. This responds to the FRMIN input by generating a Request for Macroblock Data (REQYUV). The VP2611 MUST then receive a complete macroblock (384 bytes) within 1870 cycles of the system clock. When the VP520S is producing decimated CIF/QCIF data, writing line data to the DRAM has priority, and only four macroblock read operations are possible in every 32 clock cycles i.e. one read takes eight cycles. These, however, are 16 bit word operations and it thus requires 384 x 8/2 = 1536 cycles to output the data. In addition there is a maximum delay of 60 clock periods from receiving REQYUV to producing the first output strobe (MCLK). This is still well within the time available.

The four 16 bit words are stored in the VP520S and transmitted to the VP2611 as eight bytes using a strobe (MCLK) derived from the system clock. This is only present when valid data is available, and it drives the PCLK input on the VP2611.

It takes the VP2611 almost exactly all the available time at 30 Hz frame rates to process all the macroblocks. After a field time (half an interlaced frame) the VP520S will start to write new data to the DRAM, and data could be overwritten during the last macroblocks. Since there is available space in the DRAM, a small address offset is used between video fields to avoid this problem.

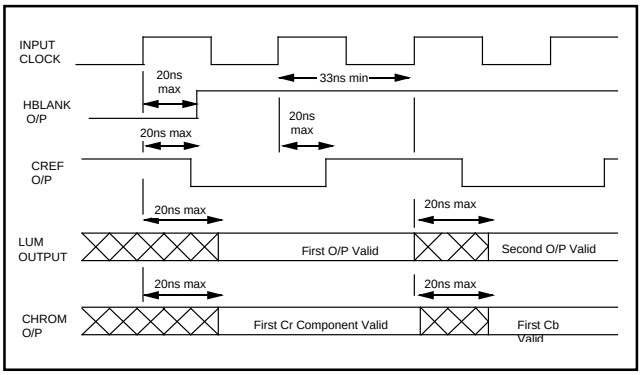


Fig 5 : Luminance and Chrominance Output Timing

INTERPOLATE MODE

In this mode the VP520S expects to receive CIF/QCIF data in macroblock format, which it then writes to an external frame store. This is then read back in line format and passed through vertical and horizontal interpolating filters to produce two fields of CCIR601 video. Detailed input timing is given in Figure 4.

FSIG automatically becomes an input which is used to identify the start of a frame and to reset the internal address counter. FSIG must stay high until a complete CIF/QCIF frame has been received (internal logic counts macroblocks). If FSIG goes low early then the complete frame will be ignored, and the previously received frame will continue to be displayed.

An input strobe, derived by dividing the system clock by four, must also be provided in order to input data. This must only be present when valid data is available on the input pins. Incoming macroblocks are byte wide, and these are internally buffered to allow four 16 bit words to be written to the DRAM every 32 system clock cycles. This is equivalent to a byte input rate of SCLK/4 which must not be exceeded.

The CIF frame store is double buffered such that a new frame can be received whilst the previous one is being displayed. In fact the use of 256K x 16 DRAM's gives sufficient capacity for more than three complete CIF frames, and the internal address generator will simply roll around to make full use of the available space.

Once a complete CIF/QCIF frame has been received, it will normally be used to generate two interlaced PAL or NTSC fields. These fields continue to be re-generated until a complete new CIF frame has been received. The rate of receiving frames depends on the transmission bandwidth, but the maximum rate is 30 Hz. The changeover to the newly received frame will occur when the VP520S has finished generating any one of the pair of interlaced fields for display, it does not

SYMBOL	PARAMETER	MINIMUM	MAXIMUM
t RAC	Access time from RAS	-	105ns or under
t CAC	Access time from CAS	-	25ns or under
t RP	RAS precharge time	50ns or under	-
t CP	CAS precharge time	12ns or under	-
t RAS	RAS pulse width	80ns or under	-
t CAS	CAS pulse width	50ns or under	-
t REF	Time between complete refreshes	-	4 ms or over (8 ms with 256k x n)

N.B. All times are quoted assuming 27MHz operation. For lower clock frequencies increase the above values proportionately.

Table 1. External DRAM Timing Requirements

necessarily have to have generated two interlaced fields from the received frame. If the VP520S is receiving frames at the full CIF 30 Hz frame rate but only displaying PAL frames at 25 Hz, then periodically one of the PAL frames (comprising two interlaced fields at 50 Hz) will be generated from two received CIF/QCIF frames. An incoming CIF/QCIF frame will always be used since the interlaced field rate is always greater than 30 Hz in either PAL or NTSC.

The data is read from the frame store such that interpolated data becomes available after programmed delays referenced to the VREF and HREF signals. Six bits are available to define the line delay, and ten are provided to define the delay from HREF in CREF periods. The actual delays are greater than the programmed values because of the internal pipeline delays, which are also mode dependent.

HREF and VREF can either be user supplied inputs, or are generated internally from a PAL/NTSC timing generator. A bit in Control Register 0 determines this option, and when the internal generator is specified the HREF pin becomes an output which supplies horizontal sync and the VREF pin supplies vertical sync. A composite sync output is also provided for system level use. In this mode the VREF and HREF signals used internally are effectively vertical and horizontal sync, and the programmed delays should be chosen to reflect this condition.

The signals provided from the internal timing generator allow the VP520S to drive the VP510 Colour Space Converter and an RGB monitor. Detailed output timing is given in Figure 5. Note that the chrominance order can be changed. Alternatively they can be used to drive off the shelf composite video encoders.

External chrominance data can have a zero colour difference value of either 0 or 128. This is defined using the Chrominance Control Bit. Where 128 is the zero colour difference value, 128 will be subtracted from incoming chrominance data and 128 will be added to output chrominace data. Output values will be limited to lie in the range 16 to 240.

External luminace data can have a black luminace level of either 0 or 16. This is defined using the Luminace Control Bit. Where 16 is the black value, 16 will be subtracted from incoming luminace data and 16 will be added to output luminace data. Output values will be limited to lie in the range 16 to 235.

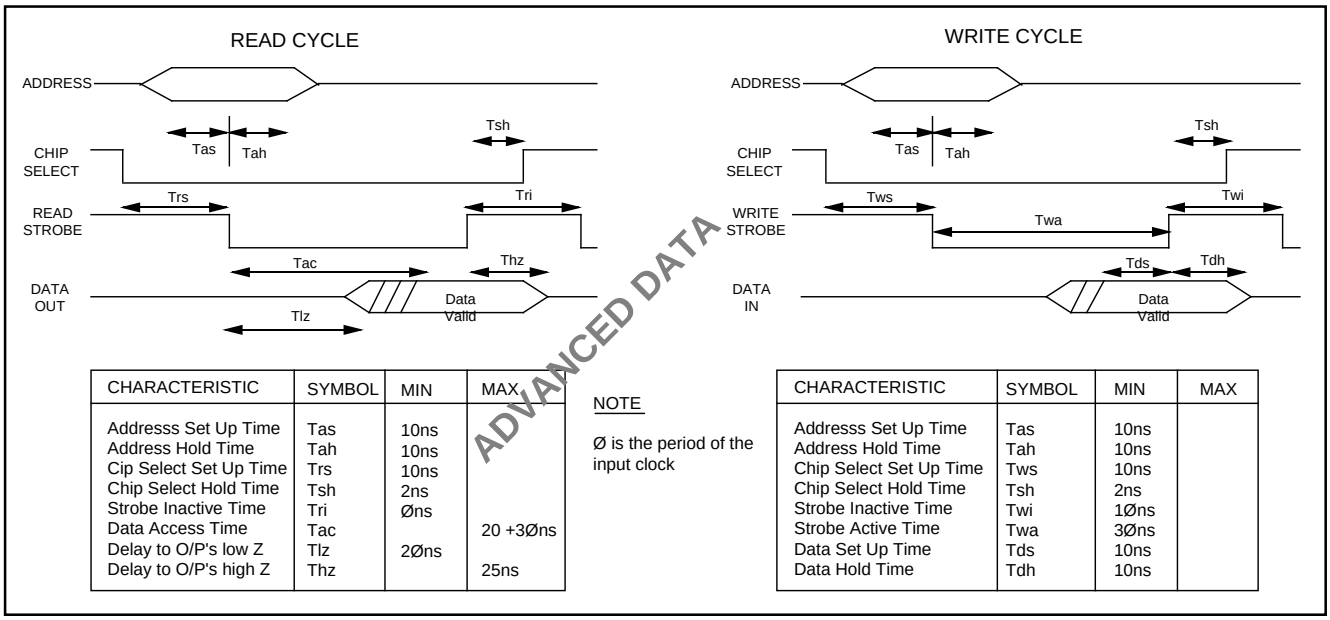
The data stored in the CIF frame store will not contain the black levels normally present during horizontal and vertical flyback. This is inserted by the VP520S at the appropriate times in order to ensure that the correct filter operation occurs at the edges of the picture. In addition to these black levels during flyback, a bit in Control Register 1 allows all active video to be replaced by a fixed colour. This colour is user definable through YUV values in three registers.

FRAME STORE INTERFACE

All read and write operations to the external DRAM frame stores are based on the use of fast page mode with 13.5 MHz CAS cycles. Internally a 54 MHz clock is produced from the 27MHz System clock, and this determines the minimum time interval which can be used in the generation of pulses and defining precharge times. Any DRAM used must meet the timing constraints given in Table 1.

Reading and writing rates dictate the need for a 16 bit data interface, and line data is re-organized to allow a 16 bit word to consist of either two luminance values or two chrominance values. This gives compatibility with the macroblock requirements since a sub block is either all chrominance or all luminance data. Reading or writing macroblock data requires jumps between pages, but four words can always be read or written using fast page mode.

Read and write operations must be timeshared to meet the requirements of the system. This time-sharing is based on the use of 16 cycles of the 13.5 MHz clock. When reading or writing line data to the store, 10 cycles are used for eight words, and six cycles are left free for four exchanges with the encoder or decoder. The additional cycles are needed when



CHARACTERISTIC	SYMBOL	MIN	MAX
Addresss Set Up Time	Tas	10ns	
Address Hold Time	Tah	10ns	
Cip Select Set Up Time	Trs	10ns	
Chip Select Hold Time	Tsh	2ns	
Strobe Inactive Time	Tri	Øns	
Data Access Time	Tac		20 +3Øns
Delay to O/P's low Z	Tlz	2Øns	
Delay to O/P's high Z	Thz		25ns

NOTE

Ø is the period of the input clock

CHARACTERISTIC	SYMBOL	MIN	MAX
Addresss Set Up Time	Tas	10ns	
Address Hold Time	Tah	10ns	
Chip Select Set Up Time	Tws	10ns	
Chip Select Hold Time	Tsh	2ns	
Strobe Inactive Time	Twi	1Øns	
Strobe Active Time	Twa	3Øns	
Data Set Up Time	Tds	10ns	
Data Hold Time	Tdh	10ns	

Fig 6 : Host Interface Timing

using fast page mode in order to guarantee RAS precharge times and RAS to CAS delays.

The above time partitioning gives a line rate of 6.75 MHz, which meets real time CIF requirements. The exchange rate with the encoder or decoder is only half of this, but is adequate for CIF data at 30 Hz frame rates. In the decode mode the VP520S produces two fields at 60 Hz rates from every 30 Hz received frame, thus writing need only be half the rate of reading. In the decimate mode the VP520S produces a CIF frame using line rates which could have supported two 60Hz fields, but only one is used. Thus reading rates need only be half writing rates since the spare field time is available.

In the interpolate mode two complete CIF frame stores are required, which dictates the use of 256K word DRAM's. The A8 pin then provides the ninth address bit needed for such devices. In the decimate mode only one CIF frame store is required, and a Control Register Bit allows the user to select either 256K word DRAM's, or 64K x 16 devices. In the latter case two such devices are needed, and the A8 pin now supplies a second CAS strobe to enable the second device. Refresh cycles generate CAS before RAS sequences.

HOST INTERFACE

The VP520S employs a conventional memory mapped host interface using a data bus and an address bus. To minimize on pin count the VP520S only uses four address lines, and all internal RAM is addressed through counters. All data is validated with a read or write strobe, and an active low enabling signal. These strobes can be asynchronous to the 27 MHz clock, but the latter must be present to move the data through several pipeline delays. Strobes must thus be valid for several clock periods. Timing is shown in Figure 5.

In the worst case mode (QCIF to NTSC video), the device must store 40 horizontal coefficients and 210 vertical coefficients. Internal storage must thus be provided for a total of 250 eight bit coefficients, and this is split into four blocks. These consist of storage for 24 horizontal luminance coefficients; storage for 16 horizontal chrominance coefficients; storage for 70 vertical luminance coefficients; and finally 140 vertical chrominance coefficients. Each block of RAM has its own internal address counter, and all counters are simultaneously reset with a write to address F hex. Each RAM area has an associated address as listed below, and a read or write using that address will increment the relevant counter. Attempts to use more addresses than are applicable to a particular area will cause undefined behaviour.

Address allocations are given below;

Addr	Function
0	Reserved
1	R/W horizontal luminance coefficients. Max 24
2	R/W horizontal chrominance coefficients. Max 16.
3	Normally 00 Hex. When 02 Hex the sync generator can be reset with the FRST and VRST pins.
4	Reserved for internal use
5	R/W vertical luminance coefficients. Max 70.
6	R/W vertical chrominance coefficients. Max 140.
7	Set to the normal operating value of 01 Hex by RESET. When loaded with 21 Hex an encoding plus a decoding VP520S can be connected 'back to back' for test purposes or coefficient investigations. No other values must be used.
8	Control Register 0. See below.
9	Control Register 1. See below
A	Line delay from VREF to first active line. 6MSBs only
A/B	Pixel delay from HREF to first active pixel 2 Bits from A plus 8 from B to give a 10 Bit value. Bit A1 is the MSB
C	Blanked screen Y value
D	Blanked screen U value
E	Blanked screen V value
F	Clear all address counters

The bits in control registers 0 and 1 are used individually, and are defined below. Where necessary the action caused when changing a control bit is delayed until the start of a new field.

REGISTER 0 (Address 8)

BIT	FUNCTION
0	Interpolate if high, decimate if low
1	PAL if low, NTSC if high
2	QCIF if high, CIF if low
3	If low subtract 16 from Y, add 16 back after filtering
4	If low subtract 128 from chrominance I/Ps, add 128 to O/Ps
5	If low generate sync, if high lock to HREF and VREF
6	If low then active edge of VREF is low going.
7	If low then active edge of HREF is low going.

REGISTER 1 (Address 9)

BIT	FUNCTION
0	If low then U inputs precede V inputs and outputs
1	If low use the internal field detect logic
2	Field Select. See text.
3	If low use 64Kx16 DRAM (encoder only)
4	When high specifies Split Screen mode (encoder only)
5	When low the Frame Ready Flag is enabled
6	When high the screen is blanked (colour defined in addresses C, D, E)
7	When high DRAM writes are disabled

USE OF ADDRESS 7

By loading Hex 21 into host address 7 it is possible to connect the encoding and decoding filters into a back to back configuration. This is useful for test purposes or for evaluating the filter coefficient values, and it avoids the need for a 'Frame Start' signal into the filter in the decode path. In normal operation address 7 should contain 01 which is the default after a reset operation.

LOADING COEFFICIENTS

The following tables show the coefficient storage locations for different modes. The filter sections below describe the use of coefficient sets. Within a set, coefficients are stored in ascending order, ie. C0, C1, C2 etc. Note that some locations are shown as not used. However, since each store is loaded sequentially, the data stream used to load the coefficient stores must contain padding values corresponding to the unused addresses. Note also that only the address range shown in the tables have to be loaded with data.

A: Horizontal Luminance Store

This is a 24 byte RAM and coefficients will be stored as follows. The full sequence is obtained by writing to Address 1, twenty four times and supplying the required data.

Mode	Addresses	Coefficient Set
CCIR -> CIF	0-7	1
CCIR -> QCIF	0-15	1
CIF -> CCIR	0-5	1
	6-11	2
QCIF -> CCIR	0-5	1
	6-11	2
	12-17	3
	18-23	4

B: Horizontal Chrominance Store

This is a 16 byte RAM and coefficients will be stored as follows, by writing to Address 2 the required number of times.

Mode	Addresses	Coefficient Set
CCIR -> CIF	0-7	1
CCIR -> QCIF	0-15	1
CIF -> CCIR	0-3	1
	4-7	2
QCIF -> CCIR	0-3	1
	4-7	2
	8-11	3
	12-15	4

C: Vertical Luminance Store

This is a 70 byte RAM and coefficients will be stored by writing to Address 5 the required number of times.

Mode	Addresses	Coefficient Set
625 line -> CIF	0-4	1
525 line -> CIF	0-4	1
	5-9	2
	10-14	3
	15-19	4
	20-24	5
	25-29	6
625 -> QCIF	0-6	1
525 -> QCIF	0-6	1
	7-13	2
	14-20	3
	21-27	4
	28-34	5
	35-41	6
CIF -> 625 line	0-4	1, even field
	5-9	1, odd field
CIF -> 525 line	0-4	1, even field
	5-9	2, even field
	10-14	3, even field
	15-19	4, even field
	20-24	5, even field
	25-29	not used
	30-34	1, odd field
	35-39	not used
	40-44	2, odd field
	45-49	3, odd field
	50-54	4, odd field
	55-59	5, odd field
QCIF -> 625 line	0-6	1, even field
	7-13	2, even field
	14-20	1, odd field
	21-27	2, odd field
OCIF -> 525 line	0-6	1, even field
	7-13	2, even field
	14-20	3, even field
	21-27	4, even field
	28-34	5, even field
	35-41	1, odd field
	42-48	2, odd field
	49-55	3, odd field
	56-62	4, odd field
	63-69	5, odd field

D: Vertical Chrominance Store

This is a 140 byte RAM and coefficients will be stored by writing to Address 6 the required number of times.

Mode	Addresses	Coefficient Set
625 line -> CIF	0-4	1
525 line -> CIF	0-4	1
	5-9	2
	10-14	3
625 line -> QCIF	0-6	1
525 line -> QCIF	0-6	1
	7-13	2
	14-20	3
CIF -> 625 line	0-4	1, even field
	5-9	2, even field
	10-14	1, odd field
	15-19	2, odd field
CIF -> 525 line	0-4	1, even field
	5-9	2, even field
	10-14	3, even field
	15-19	4, even field
	20-24	5, even field
	25-29	not used
	30-34	1, odd used
	35-39	not used
	40-44	2, odd field
	45-49	3, odd field
	50-54	4, odd field
	55-59	5, odd field
QCIF -> 525 line	0-6	1, even field
	7-13	2, even field
	14-20	3, even field
	21-27	4, even field
	28-34	5, even field
	35-41	6, even field
	42-48	7, even field
	49-55	8, even field
	56-62	9, even field
	63-69	10, even field
	70-76	1, odd field
	77-83	2, odd field
	84-90	3, odd field
	91-97	4, odd field
	98-104	5, odd field
	105-111	6, odd field

	112-118	7, odd field
	119-125	8, odd field
	126-132	9, odd field
	133-139	10, odd field
QCIF -> 625 line	0-6	1, even field
	7-13	2, even field
	14-20	3, even field
	21-27	4, even field
	28-34	1, odd field
	35-41	2, odd field
	42-48	3, odd field
	49-55	4, odd field

HORIZONTAL FILTERS

Chrominance data is assumed to have already been decimated down to half the horizontal sampling rate of the luminance data, before it is applied to the VP520S. When producing CIF data both luminance and chrominance are then both decimated by two, when producing QCIF data they are both decimated by four.

Simulations with actual video have shown that 8 tap CIF filters and 16 tap QCIF filters give more than adequate performance in the decimation mode. In the interpolation mode these same simulations have shown the need for longer filters in the luminance channel. The hardware thus supports a 12 tap filter when interpolating luminance from CIF inputs, but only 8 taps are provided for each chrominance channel. Even longer filters are needed when QCIF data must be interpolated, and the luminance channel is provided with 24 taps, and each chrominance channel with 16 taps.

Note that when interpolating by two the output rate is double the input rate, but every other input will be conceptually zero. Similarly when interpolating by four there are three zero's between every data point, even though the output rate is four times the input rate. Thus during any clock period only one half or one quarter of the coefficients are actually in use, and the computational burden is no greater than when doing the equivalent decimation.

Since all the coefficients are not in use during any clock cycle, it is convenient to refer to two smaller sets of coefficients. Thus the 12 tap CIF luminance filter, for example, can be considered to have two sets of 6 coefficients, and the 24 tap QCIF luminance filter to have four sets of 6 coefficients. The addressing in the coefficient RAMs uses this concept of sets.

VERTICAL FILTERS

The vertical filters are designed to produce CIF with the spatial relationship shown in Figure 7, and QCIF with the spatial relationship shown in Figure 8. Original PAL or NTSC video contains lines of coincident luminance and chrominance, but the CIF specification requires that the decimated chrominance information is shifted such that it lies mid way between two luminance lines. This is achieved by choosing the centre outputs from the filter which best fit the requirements. The filter outputs actually used by the device are shown by the arrows in Figures 7 and 8, and are optimal when the even field provides the original video.

It is assumed that one of the interlaced fields has been discarded prior to the VP520S, and thus no further decimation occurs when producing CIF luminance from PAL (NTSC in

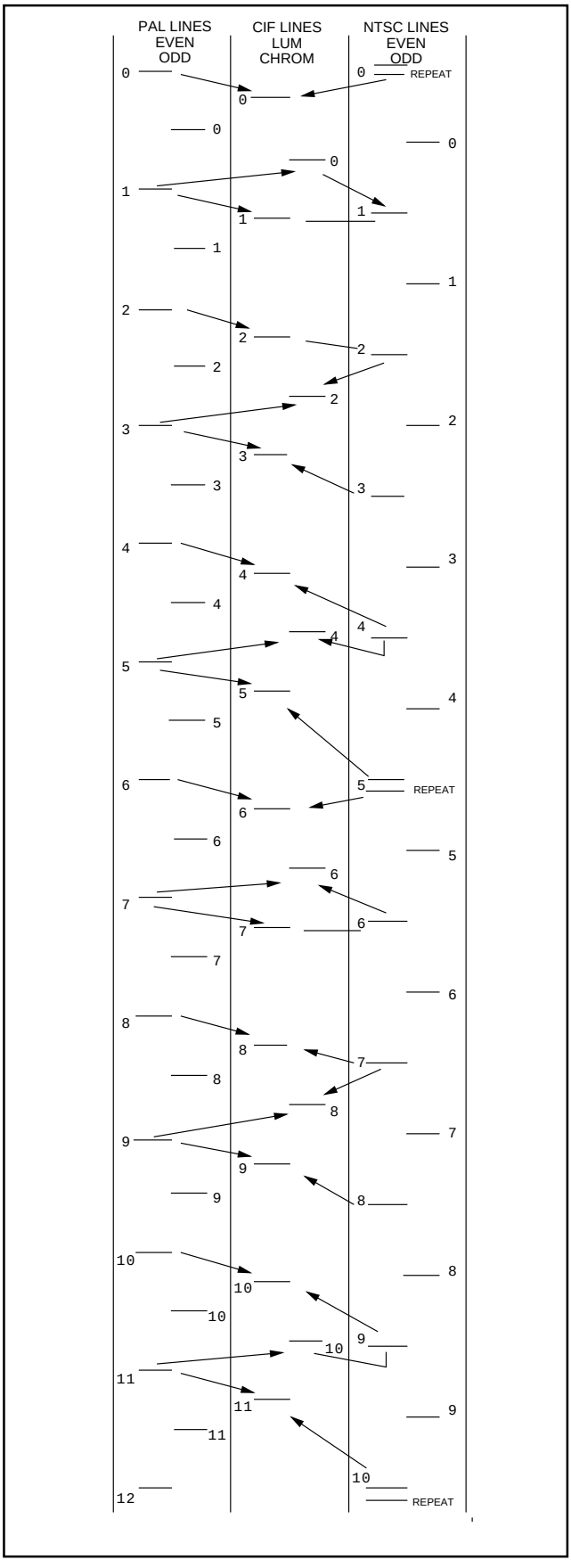


Fig 7 : CIF Spatial Relationships

fact needs some interpolation - see the relevant section). Chrominance, however, is decimated by two. When producing QCIF data the luminance channel is decimated by two, and the chrominance by four.

When the VP520S is used to derive interlaced CCIR601 video, the internal address generator will read the CIF/QCIF frame store twice in order to produce the two fields. Each field has its own set of coefficients.

Internal RAM is provided which will support four CIF line delays for both chrominance and luminance. Five tap filters are thus possible for CIF conversions. With a QCIF system the internal RAM could theoretically be used to provide eight QCIF line delays. In practice, however, little benefit is obtained by using vertical filters with more than seven taps, and thus only six line delays are used.

Polyphase filters are used to support the spatial conversions. PAL conversion is relatively simple and only requires a set of coefficients for each mode. NTSC conversion requires several sets of coefficients since the 240 lines in a field must be converted to 288 lines of CIF. One line is repeated in every five to produce six lines which are then filtered with their own coefficients.

The generation of interpolated outputs requires CIF / QCIF data to be repeatedly read from the frame store at various line intervals. This is all handled by the internal address generator, and is transparent to the user. The device then produces coincident luminance and chrominance data which has been interpolated from data in the frame store. The first line will be produced to match the delay from the VREF input which has been pre-defined. This delay must be greater than the internal pipeline delay, which itself is mode dependent (delay yet to be determined).

The device introduces black lines at the top and bottom of the fields. Thus the first and last lines in the interpolated field will be filtered with varying amounts of black information.

PAL VERTICAL FILTERING

When producing CIF data the five tap filters provide outputs for every line at the 6.75 MHz decimated line rate. Every filtered luminance line is used but every other filtered chrominance line will be discarded. Filter outputs corresponding to odd numbered PAL chrominance lines in any field being at the centre are used to provide the CIF chrominance lines. This is shown by the arrows in Figure 7.

When decimating down to QCIF seven tap filters are used, which provide outputs for every line at the 3.375 MHz line rate. Only every other filtered luminance line, and every fourth chrominance line are actually stored in the frame store. Different PAL lines are used to produce the offset luminance and chrominance lines as indicated by the arrows in Figure 7.

When interpolating from CIF the luminance channel conceptually uses a 10 tap filter, with every other input line containing only zero's. Thus only five coefficients are actually used when producing interpolated lines for the even field, and five different coefficients are used when producing the odd field. The device thus stores two sets of five coefficients; one set for each field produced by reading the CIF frame store twice.

The chrominance filter is conceptually a 20 tap filter with three lines of zero's for every actual input. Thus each chrominance channel needs four sets of five coefficients; two sets are needed to produce one field, and two sets are needed for the other field. The same chrominance data is read twice for a given pair of luminance lines, in order to provide inputs for the filter. Thus the internal line delays contain the same set of chrominance data on two consecutive lines supplying data to the filters.

When interpolating from QCIF, seven coefficients can be

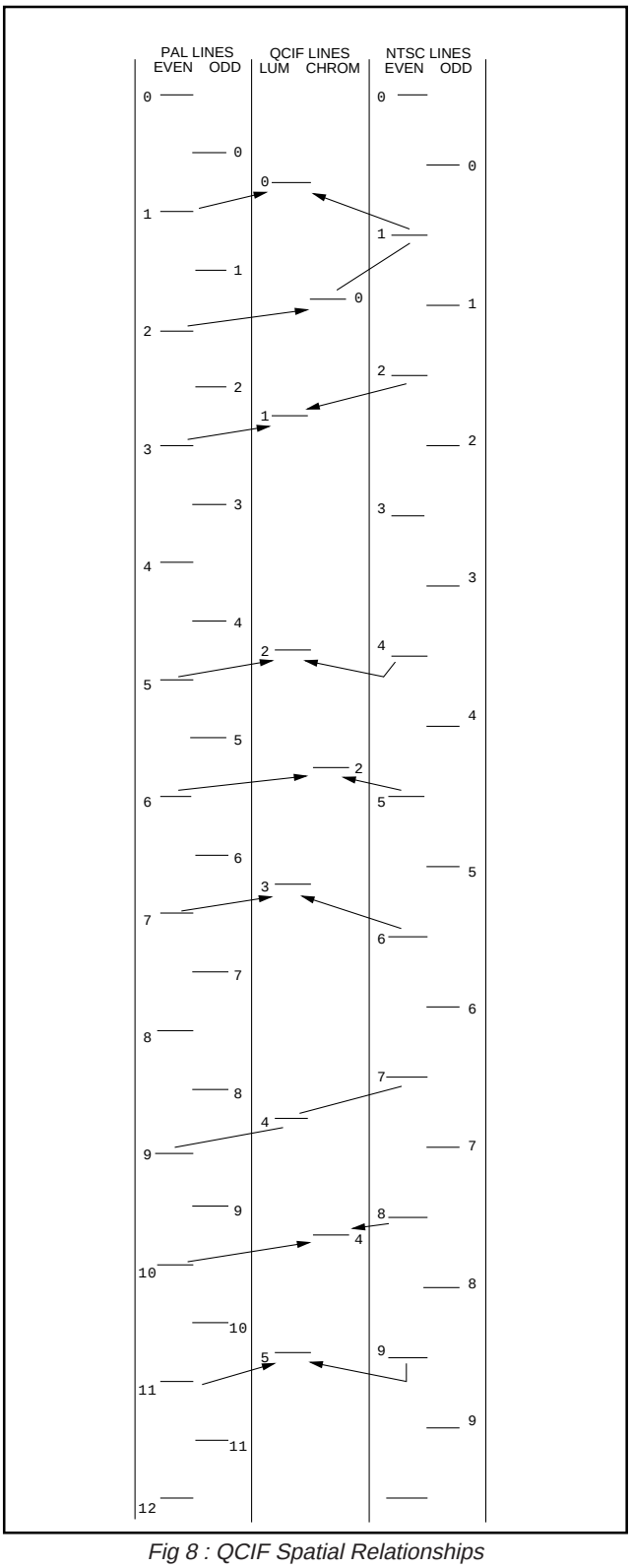


Fig 8 : QCIF Spatial Relationships

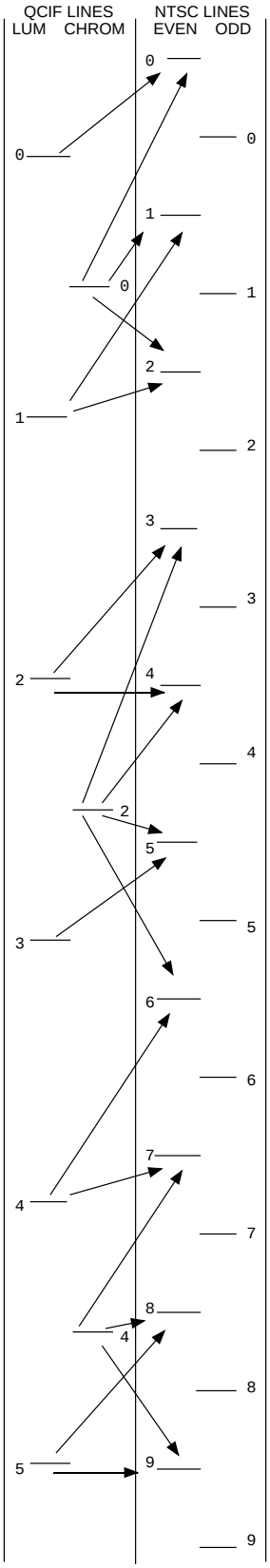


Fig 9 : Interpolating from QCIF to NTSC

used in each set since six line delays are provided. The luminance filter conceptually contains 28 taps (four sets of seven coefficients with two sets used to produce each field). Similarly the chrominance filter consists of 56 taps arranged as eight sets of seven coefficients with four sets needed for each field. In order to provide data for the filters each luminance line is read twice, and each chrominance line is read four times to produce each field.

NTSC VERTICAL FILTERING

One field of NTSC video consists of 240 chrominance and luminance lines, which must be converted to 288 lines of CIF luminance and 144 lines of CIF chrominance. The luminance increase is mechanized by repeating the first line in every five to produce six lines, which are then applied to the vertical filters. A different set of coefficients is used for each line, requiring a total of 30 to be stored within the device. The line repeat causes one set of line data to be used twice, but each time different coefficients are used by the filter. This technique is equivalent to interpolating the data by six, and then decimating by five. The required coefficients for each of the six sets can be derived by conceptually using this approach.

The line repeat requires an additional FIFO line delay before the four delays used by the filters. By reducing the horizontal blanking time it is possible to read six lines (one is repeated) from the FIFO in the time taken to acquire five lines of video with blanking.

Chrominance data also passes through the input FIFO and one line in every five is repeated. This is done in order to avoid differential delays with the luminance data. Three chrominance lines are only needed, however, for every five original lines. They are produced by using three sets of five coefficients and discarding two filtered lines in every five. The three selected filter outputs are chosen such that the centre line of the filter is closest to the CIF line number needed. The centre lines which are actually used are shown in Figure 8, and result in a sequence of two chosen outputs then a gap followed by one output then a gap. Simply using every other output would not give the best fit.

A simplified approach is used when decimating down to QCIF resolution, and the input FIFO is not used. Six luminance lines are derived from ten NTSC lines by choosing the six outputs produced when the centre line in the filter is closest to the QCIF line that is needed. Overall this results in a luminance sequence consisting of two outputs then a gap, followed by one output then a gap and is shown in Figure 8.

Three chrominance lines are derived from the same inputs by using three sets of seven coefficients. The chrominance sequence is also shown in Figure 7, and consists of an output then three gaps, followed by an output and two gaps.

When interpolating from CIF up to NTSC resolutions, it is necessary to read lines of data from the CIF frame store with reduced blanking periods. The timing is calculated such that six lines are read in the time that five lines would have been read if they had the correct blanking period. These fast lines are continuously filtered using all the available information, and the results are written to an output FIFO. This FIFO is then read with the correct blanking period inserted in order to provide NTSC data at the output pins. Thus five lines are read out in the time taken to load six lines (one of which need not actually be written since it is never used)

Five sets of coefficients are used to produce the five lines which are actually stored, but the coefficients are different for the even and odd field generation. Thus a total of ten sets of five coefficients are internally stored. In effect we have interpolated by five and then decimated by three in order to produce the complete NTSC frame.

Each CIF chrominance line is used to produce two filtered NTSC chrominance lines, and one filtered line in every six is then ignored. This is mechanized by reading each CIF chrominance line twice for every pair of luminance lines. The same filtering and discard technique as used in the luminance channel is then applied, using five sets of coefficients for each field. Ten sets are thus needed to produce two NTSC fields. We have effectively interpolated by ten and then decimated by three to produce 480 chrominance lines for the complete frame.

When interpolating from QCIF to NTSC the additional output buffering is not used. Instead a sequence is used which will generate 10 NTSC lines in any field from six QCIF luminance lines and three chrominance lines. Figure 9 illustrates how the first and fourth lines are used once and the second, third, fifth, and sixth used twice to produce QCIF luminance. Since this 1 - 2 - 2 sequence is used twice in every ten lines, only five rather than ten sets of coefficients are actually needed for each field (ten sets in total).

The first and third chrominance lines are used three times, and the second line is used four times. Thus ten sets of coefficients are needed for each field (twenty sets in total). Each luminance and chrominance set consists of seven coefficients, since six line delays are provided for the filters.

JTAG Test Interface

The VP520S includes a test interface consisting of a boundary scan loop of test registers placed between the pads and the core of the chip. The control of this loop is fully JTAG/ IEEE 1149-1 1990 compatible. Please refer to this document for a full description of the standard.

The interface has five dedicated pins: TMS, TDI, TDO, TCK and TRST. The TRST pin is an independent reset for the interface controller and should be pulsed low, soon after power up; if the JTAG interface is not to be used it can be tied low permanently. The TDI pin is the input for shifting in serial instruction and test data; TDO the output for test data. The TCK pin is the independent clock for the test interface and registers, and TMS the mode select signal.

TDI and TMS are clocked in on the rising edge of TCK, and all output transitions on TDO happen on its falling edge.

Instructions are clocked into the 3 bit instruction register (no parity bit) and the following instructions are available.

Instruction Register (MSB first)	**Name**
111	BYPASS
000	EXTEST (Inversion except for VREF, HREF, CSYNC and CLMP)
010	SAMPLE/PRELOAD

The TAP controller used in this device does not support a separate INTEST instruction but allows EXTEST to drive the internals of the device as well as to drive the output pins. Output enables are thus present in the chain which are not connected to pins but which allow EXTEST to be used to control the impedance of all the outputs. The TOE pin, which can separately be used to control the impedance of all the outputs, can be monitored as an input through the scan chain but cannot be used to control the outputs through the TAP controller. The signals controlled by the various enables are listed below:

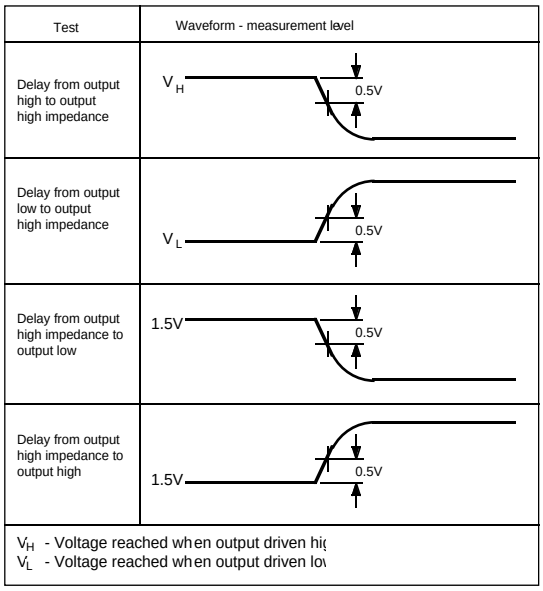
PAD NAME	SIGNALS CONTROLLED
dram_oeb	A8:0, RAS, CAS, R/W
refs_oeb	FREF, VREF, HREF
csync_oeb	CLMP, CSYNC, HBLNK
cgtout_oeb	Test function only
d_oeb	D15:0
m_oeb	M7:0, MCLK, FSIG
c_dec_b	CREF
yuv_oeb	Y7:0, C7:0
cdata_oeb	HD7:0

ABSOLUTE MAXIMUM RATINGS [See Notes]

Supply voltage V_{DD}	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to V_{DD} + 0.5V
Output voltage V_{OUT}	-0.5V to V_{DD} + 0.5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HMB)	500V
Storage temperature T_S	-65°C to 150°C
Ambient temperature with power applied T_{AMB}	0°C to 70°C
Junction temperature	150°C
Package power dissipation	5000mW

NOTES ON MAXIMUM RATINGS

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as negative into the device.



STATIC ELECTRICAL CHARACTERISTICS

Operating Conditions (unless otherwise stated)
Tamb = 0 C to +70°C V_{DD} = 5.0v ± 5%

Characteristic	Symbol	Value Min.	Value Typ.	Value Max.	Units	Conditions
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -4mA
Input high voltage	V_{IH}	2.0		-	V	V_{DD} - 1V for SYSCLK and MCLK
Input low voltage	V_{IL}	-		0.8	V	
Input leakage current	I_{IN}	-10		+10	µA	GND < V_{IN} < V_{DD}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-50		+50	µA	GND < V_{OUT} < V_{DD}
Output S/C current	I_{SC}	10		300	mA	

ORDERING INFORMATION

VP520S/CG/GH1R (Commercial - Plastic QFP package)

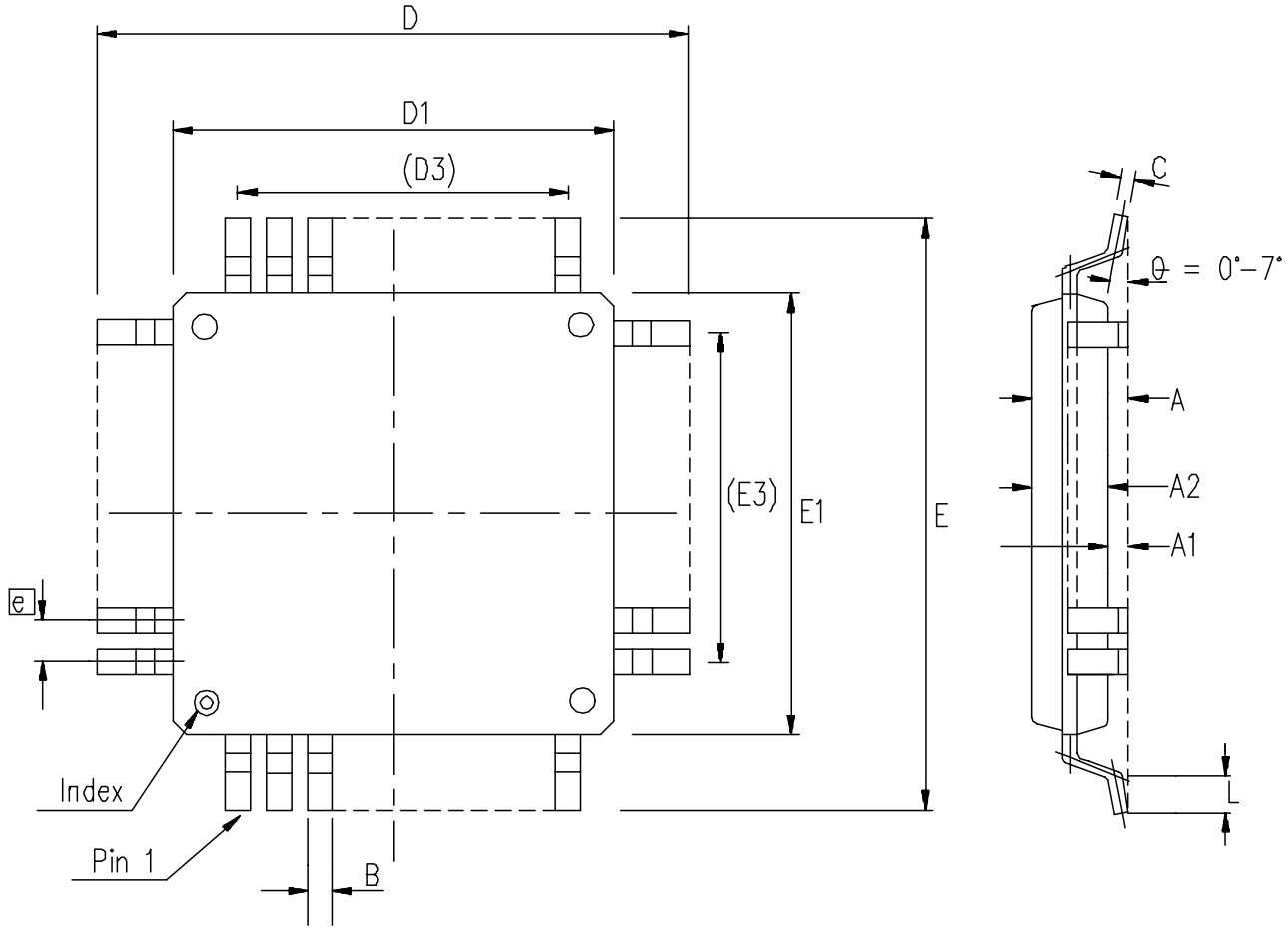
PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	GND	25	M3	49	CREF	73	VDD	97	D14
2	A8	26	M2	50	GND	74	SCLK	98	D13
3	A7	27	M1	51	CSYNC	75	GND	99	D12
4	A6	28	M0	52	Y0	76	VDD	100	GND
5	A5	29	MCLK	53	Y1	77	HA0	101	VDD
6	VDD	30	VDD	54	Y2	78	HA1	102	D11
7	GND	31	GND	55	Y3	79	HA2	103	D10
8	A4	32	REQYUV	56	Y4	80	HA3	104	D9
9	A3	33	GND	57	Y5	81	WR	105	D8
10	A2	34	VRST	58	Y6	82	RD	106	GND
11	A1	35	FSIG	59	Y7	83	CEN	107	VDD
12	A0	36	FRST	60	VDD	84	HD0	108	D0
13	VDD	37	VDD	61	GND	85	HD1	109	D1
14	GND	38	RST	62	HBLNK	86	HD2	110	D2
15	RW	39	TCK	63	C0	87	HD3	111	D3
16	VDD	40	TMS	64	C1	88	HD4	112	GND
17	GND	41	TRST	65	C2	89	HD5	113	VDD
18	RAS	42	TDI	66	C3	90	VDD	114	D4
19	VDD	43	TDO	67	C4	91	GND	115	D5
20	GND	44	TOE	68	C5	92	HD6	116	D6
21	M7	45	VDD	69	C6	93	HD7	117	D7
22	M6	46	VREF	70	C7	94	CLMP	118	CAS
23	M5	47	FREF	71	N/C	95	VDD	119	GND
24	M4	48	HREF	72	GND	96	D15	120	VDD

Table 2: 120 Pin QFP Pin Assignment

Signal	Direction	JTAG Bit Number	Signal	Direction	JTAG Bit Number	Signal	Direction	JTAG Bit Number
A8	OUT	145	Y2	OUT	93	HD5	OUT	43
A7	OUT	144	Y2	IN	92	HD5	IN	42
A6	OUT	143	Y3	OUT	91	HD6	OUT	41
A5	OUT	142	Y3	IN	90	HD6	IN	40
A4	OUT	141	Y4	OUT	89	HD7	OUT	39
A3	OUT	140	Y4	IN	88	HD7	IN	38
A2	OUT	139	Y5	OUT	87	cdata_oeb*	OUT	37
A1	OUT	138	Y5	IN	86	CLMP	OUT	36
A0	OUT	137	Y6	OUT	85	D15	OUT	35
RW	OUT	136	Y6	IN	84	D15	IN	34
RAS	OUT	135	Y7	OUT	83	D14	OUT	33
dram_oeb	OUT	134	Y7	IN	82	D14	IN	32
M7	OUT	133	HBLNK	OUT	81	D13	OUT	31
M7	IN	132	C0	OUT	80	D13	IN	30
M6	OUT	131	C0	IN	79	D12	OUT	29
M6	IN	130	C1	OUT	78	D12	IN	28
M5	OUT	129	C1	IN	77	D11	OUT	27
M5	IN	128	C2	OUT	76	D11	IN	26
M4	OUT	127	C2	IN	75	D10	OUT	25
M4	IN	126	C3	OUT	74	D10	IN	24
M3	OUT	125	C3	IN	73	D9	OUT	23
M3	IN	124	C4	OUT	72	D9	IN	22
M2	OUT	123	C4	IN	71	D8	OUT	21
M2	IN	122	C5	OUT	70	D8	IN	20
M1	OUT	121	C5	IN	69	D0	OUT	19
M1	IN	120	C6	OUT	68	D0	IN	18
M0	OUT	119	C6	IN	67	D1	OUT	17
M0	IN	118	C7	OUT	66	D1	IN	16
MCLK	OUT	117	C7	IN	65	D2	OUT	15
MCLK	IN	116	yuv_oeb	OUT	64	D2	IN	14
m_oeb	OUT	115	CGTOUT (N/C)	OUT	63	D3	OUT	13
REQYUV	IN	114	cgtout_oeb	OUT	62	D3	IN	12
FSIG	OUT	113	SCLK	IN	61	D4	OUT	11
FSIG	IN	112	HA0	IN	60	D4	IN	10
RST	IN	111	HA1	IN	59	D5	OUT	9
TOE	IN	110	HA2	IN	58	D5	IN	8
VREF	OUT	109	HA3	IN	57	D6	OUT	7
VREF	IN	108	WR	IN	56	D6	IN	6
FREF	OUT	107	RD	IN	55	D7	OUT	5
FREF	IN	106	CEN	IN	54	D7	IN	4
HREF	OUT	105	HD0	OUT	53	d-oeb*	OUT	3
HREF	IN	104	HD0	IN	52	CAS	OUT	2
CREF	OUT	103	HD1	OUT	51	VRST	IN	1
CREF	IN	102	HD1	IN	50	FRST	IN	0
refs_oeb	OUT	101	HD2	OUT	49			
c_dec_b		100	HD2	IN	48			
CSYNC	OUT	99	HD3	OUT	47			
csync_oeb	OUT	98	HD3	IN	46			
Y0	OUT	97	HD4	OUT	45			
Y0	IN	96	HD4	IN	44			
Y1	OUT	95						
Y1	IN	94						

Table 3: JTAG Register Allocation

CGTOUT (N/C) This pin is only used for GPS test purposes and should not be used for system purposes.



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	---	3.91		---	0.154
A1	0.25	---		0.010	---
A2	3.17	3.67		0.125	0.144
D	31.65	32.15		1.246	1.266
D1	27.90	28.10		1.098	1.106
D3	23.20 REF			0.913 REF	
E	31.65	32.15		1.246	1.266
E1	27.90	28.10		1.098	1.106
E3	23.20 REF			0.913 REF	
L	0.65	0.95		0.026	0.037
e	0.80 BSC			0.0315 BSC	
B	0.22	0.38		0.009	0.015
C	0.13	0.23		0.005	0.009
	Pin features				
N	120				
ND	30				
NE	30				
NOTE	SQUARE				

NOTES:–
1. CONTROLLING DIMENSIONS ARE IN MM.
2. This document supersedes 418/ED/51699/002 issue 1

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