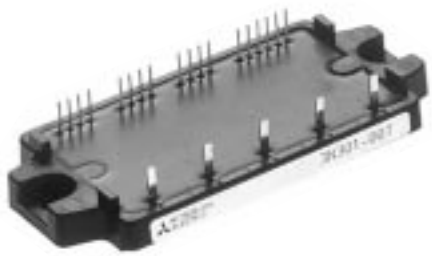
PM15CNJ060

FLAT-BASE TYPE
INSULATED PACKAGE

PM15CNJ060

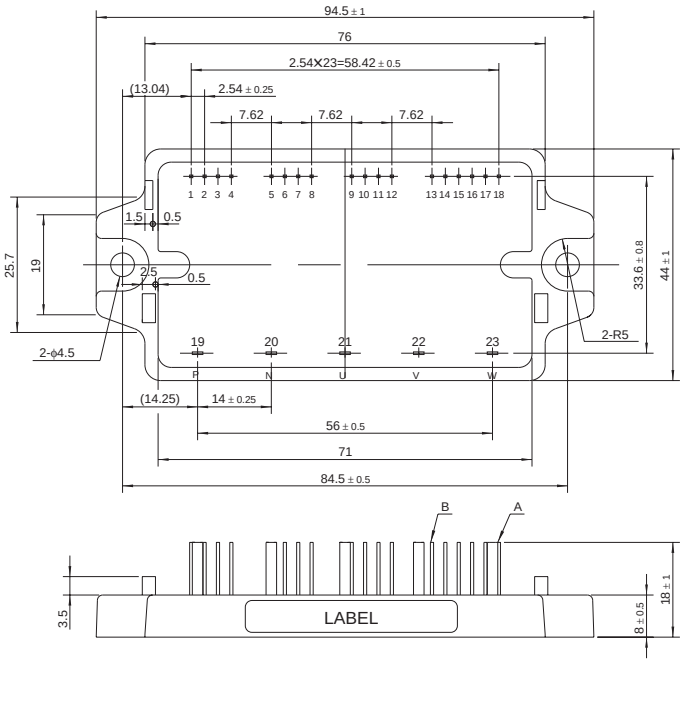


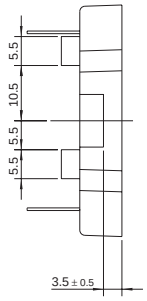
- 3 phase IGBT (15A/600V) inverter output
- Monolithic gate drive & protection logic circuit
- Protection logic
  - Over circuit (OC)
  - Short circuit (SC)
  - Over temperature (OT)
  - Under voltage lock-out (UV)
- UL Recognized File No. E80271
  Yellow Card No. E80276

APPLICATION

General purpose inverter, servo drives and other motor controlers

PACKAGE OUTLINES **Dimensions in mm**

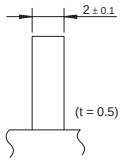




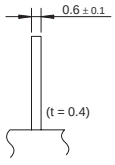
Terminal code

1.	V_{UPC}	13.	V_{NC}
2.	NC	14.	V_{N1}
3.	U_P	15.	U_N
4.	V_{UP1}	16.	V_N
5.	V_{VPC}	17.	W_N
6.	NC	18.	FO
7.	V_P	19.	P
8.	V_{VP1}	20.	N
9.	V_{WPC}	21.	U
10.	NC	22.	V
11.	W_P	23.	W
12.	V_{WP1}		

NC : No Connect



A:Detail



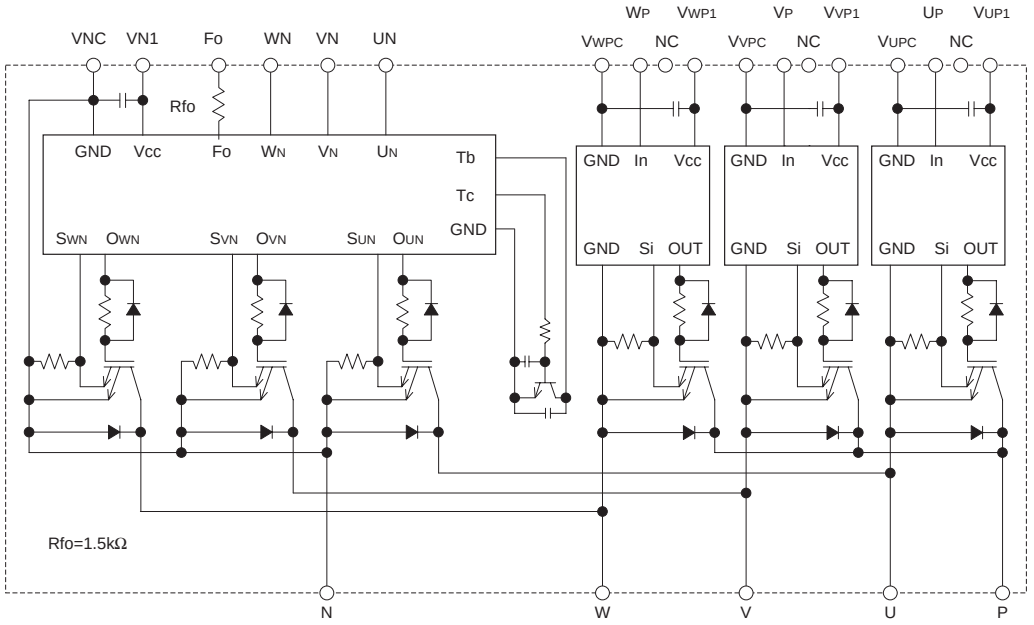
B:Detail

MITSUBISHI ELECTRIC

PM15CNJ060

FLAT-BASE TYPE
INSULATED PACKAGE

INTERNAL FUNCTIONS BLOCK DIAGRAM



MAXIMUM RATINGS (Tj = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{CES}	Collector-Emitter Voltage	V_D = 15V, V_{CIN} = 15V	600	V
±I_C	Collector Current	T_C = 25°C	15	A
±I_{CP}	Collector Current (Peak)	T_C = 25°C	30	A
P_C	Collector Dissipation	T_C = 25°C	43	W
T_j	Junction Temperature		–20 ~ +125*	°C

*The item defines the maximum junction temperature for the power elements (IGBT/Diode) of the IPM to ensure safe operation. However, these power elements can endure junction temperature as high as 150°C instantaneously. To make use of this additional temperature allowance, a detailed study of the exact application conditions is required and, accordingly, necessary information is requested to be provided before use.

CONTROL PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Supply Voltage	Applied between : V_{UP1}-V_{UPC}, V_{VP1}-V_{VPC}, V_{WP1}-V_{WPC}, V_{N1}-V_{NC}	20	V
V_{CIN}	Input Voltage	Applied between : U_P-V_{UPC}, V_P-V_{VPC}, W_P-V_{WPC}, U_N • V_N • W_N-V_{NC}	20	V
V_{FO}	Fault Output Supply Voltage	Applied between : F_O-V_{NC}	20	V
I_{FO}	Fault Output Current	Sink current at F_O terminals	20	mA

MITSUBISHI ELECTRIC

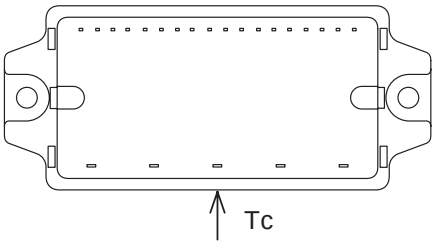
PM15CNJ060

FLAT-BASE TYPE
INSULATED PACKAGE

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(PROT)}$	Supply Voltage Protected by SC	V_D = 13.5 ~ 16.5V, Inverter Part, T_j = 125°C Start	400	V
$V_{CC(surge)}$	Supply Voltage	Applied between : P-N, Surge value	500	V
T_C	Module Case Operating Temperature	(Note-1)	–20 ~ +100	°C
T_{stg}	Storage Temperature		–40 ~ +125	°C
V_{iso}	Isolation Voltage	60Hz, Sinusoidal Charged part to Base, AC 1 min.	2500	V_{rms}

(Note-1) Tc measurement point



ELECTRICAL CHARACTERISTICS (Tj = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Test Condition		Limits			Unit
				Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	V_D = 15V, I_C = 15A, V_{CIN} = 0V, Pulsed (Fig. 1)	T_j = 25°C	—	1.8	2.5	V
			T_j = 125°C	—	1.9	2.6	
V_{EC}	FWDi Forward Voltage	–I_C = 15A, V_D = 15V, V_{CIN} = 15V (Fig. 2)		—	2.0	3.0	V
t_{on}	Switching Time	V_D = 15V, V_{CIN} = 0V↔15V, V_{CC} = 300V, I_C = 15A, T_j = 125°C, Inductive Load (Upper-Lower Arm) (Fig. 3)		0.3	0.7	1.6	µs
t_{rr}				—	0.15	0.5	µs
$t_{c(on)}$				—	0.35	1.0	µs
t_{off}				—	1.5	2.3	µs
$t_{c(off)}$				—	0.4	1.2	µs
I_{CES}	Collector-Emitter Cutoff Current	V_{CE} = V_{CES}, V_D = 15V (Fig. 4)	T_j = 25°C	—	—	1	mA
			T_j = 125°C	—	—	10	

MITSUBISHI ELECTRIC

CONTROL PART

Symbol	Parameter	Test Condition		Limits			Unit
				Min.	Typ.	Max.	
I_D	Circuit Current	V_D = 15V, V_{CIN} = 15V	V_{N1}-V_{NC}	—	18	25	mA
			V_{XP1}-V_{XPC}	—	7	10	
$V_{th(ON)}$	Input ON Voltage	Applied between : U_P-V_{UPC}, V_P-V_{VPC}, W_P-V_{WPC}		1.2	1.5	1.8	V
$V_{th(OFF)}$	Input OFF Voltage	U_N • V_N • W_N-V_{NC}		1.7	2.0	2.3	V
OC	Over Current Trip Level	–20 ≤ T_j ≤ 125°C, V_D = 15V (Fig. 5,6)		18	26	—	A
SC	Short Circuit Trip Level	–20 ≤ T_j ≤ 125°C, V_D = 15V (Fig. 5,6)		—	39	—	A
$t_{off(OC)}$	Over Current Delay Time	V_D = 15V (Fig. 5,6)		—	10	—	µs
OT	Over Temperature protection	V_D = 15V	Trip level	100	110	120	°C
OT_r			Reset level	—	90	—	°C
UV	Supply Circuit Under-Voltage Protection	–20 ≤ T_j ≤ 125°C	Trip level	11.5	12.0	12.5	V
UV_r			Reset level	—	12.5	—	V
$I_{FO(H)}$	Fault Output Current	V_D = 15V, V_{CIN} = 15V (Note-2)		—	—	0.01	mA
$I_{FO(L)}$				—	10	15	mA
t_{FO}	Minimum Fault Output Pulse Width	V_D = 15V (Note-2)		1.0	1.8	—	ms

(Note-2) Fault output is given only when the internal SC, OT & UV protections schemes of either upper or lower arm device operate to protect it.

THERMAL RESISTANCES

Symbol	Parameter	Test Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case Thermal Resistances	Inverter IGBT part (per 1/6 module)	—	—	2.9	°C/W
$R_{th(j-c)F}$		Inverter FWDi part (per 1/6 module)	—	—	4.5	°C/W
$R_{th(c-f)}$	Contact Thermal Resistance	Case to fin, (per 1 module) Thermal grease applied	—	—	0.5	°C/W

MECHANICAL RATINGS AND CHARACTERISTICS

Symbol	Parameter	Test Condition	Limits			Unit
			Min.	Typ.	Max.	
—	Mounting torque	Mounting part screw : M4	0.98	1.18	1.47	N • m
			10	12	15	kg•cm
—	Weight	—	—	60	—	g

RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Test Condition	Recommended value	Unit
V_{CC}	Supply Voltage	Applied across P-N terminals (Fig. 3)	≤ 400	V
V_D	Control Supply Voltage	Applied between : U_{P1}-V_{UPC}, V_{VP1}-V_{VPC} W_{P1}-V_{WPC}, V_{N1}-V_{NC} (Note-3)	15 ± 1.5	V
$V_{CIN(ON)}$	Input ON Voltage	Applied between : U_P-V_{UPC}, V_P-V_{VPC}, W_P-V_{WPC}	≤ 0.8	V
$V_{CIN(OFF)}$	Input OFF Voltage	U_N • V_N • W_N-V_{NC}	≥ 4.0	
f_{PWM}	PWM Input Frequency	Using Application Circuit of Fig. 8	≤ 15	kHz
t_{dead}	Arm Shoot-through Blocking Time	For IPM's each input signals (Fig. 7)	≥ 2	µs

(Note-3) With ripple satisfying the following conditions
dv/dt swing ≤ ±5V/µs, Variation ≤ 2V peak to peak

PRECAUTIONS FOR TESTING

1. Before appling any control supply voltage (V_D), the input signals should be low level.
   After this, each input signal should be set to the specified ON and OFF level.
2. When performing “SC” tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above $V_{CC(surge)}$ rating of the device.
   (These test should not be done by using a curve tracer or its equivalent.)

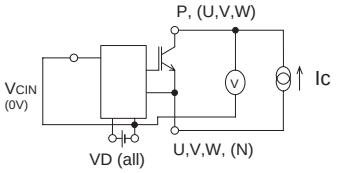


Fig. 1 $V_{CE(sat)}$ Test

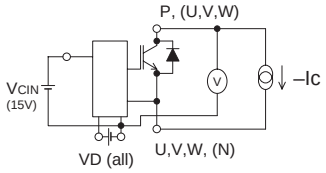


Fig. 2 V_{EC} Test

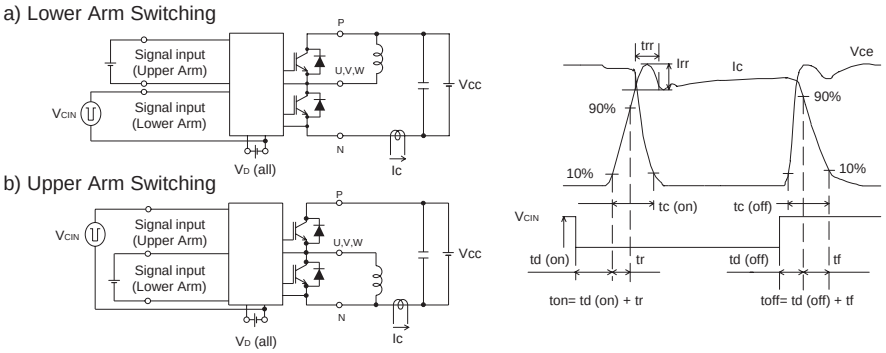


Fig. 3 Switching time Test circuit and waveform

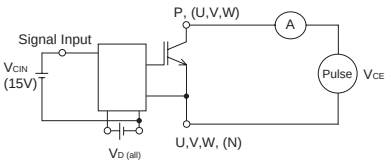


Fig. 4 I_{CES} Test

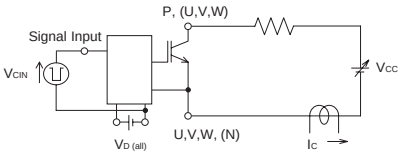


Fig. 5 OC and SC Test

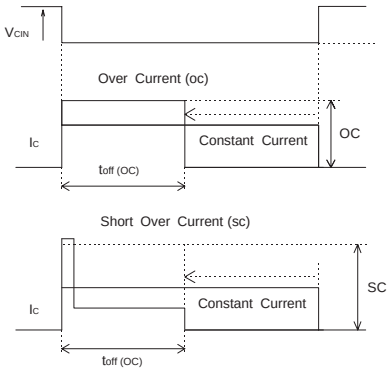


Fig. 6 OC and SC Test waveform

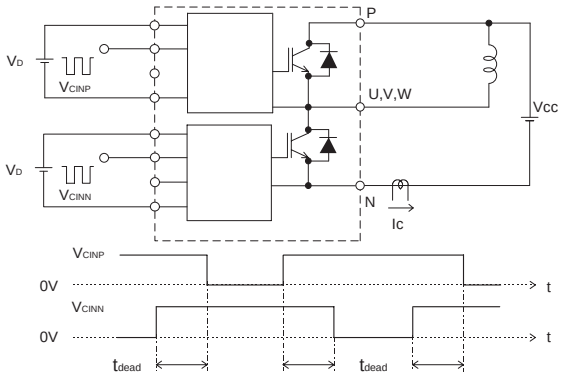


Fig. 7 Dead time measurement point example

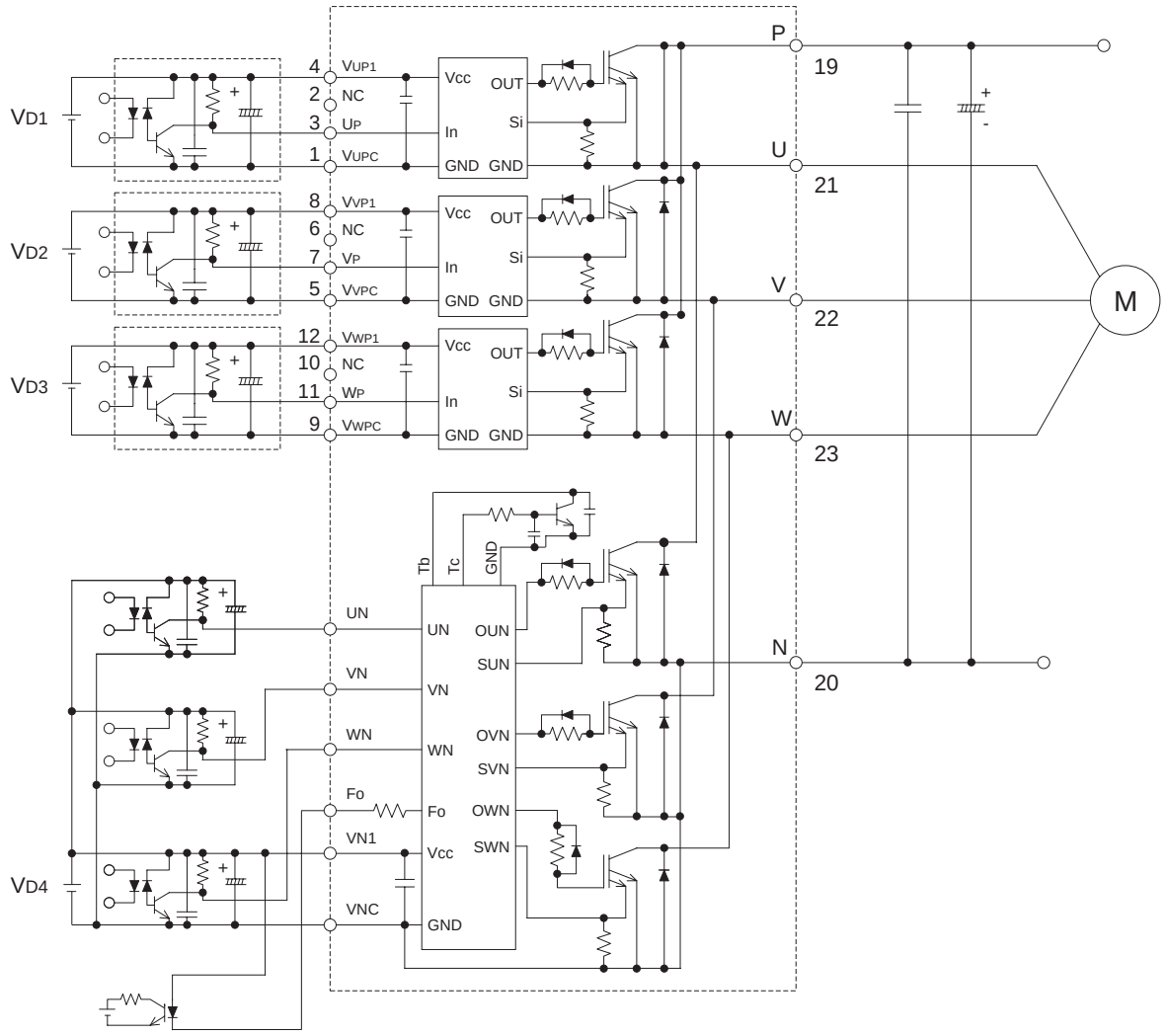


Fig. 8 Application Example Circuit

NOTES FOR STABLE AND SAFE OPERATION ;

- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers : t_{PLH}, $t_{PHL} \leq 0.8\mu s$, Use High CMR type.
- Slow switching opto-coupler : CTR > 100%
- Use 4 isolated control power supplies (V_D). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.