V53C365165A
3.3 VOLT 4M X 16 EDO PAGE MODE CMOS DYNAMIC RAM

V53C365165A	40	50	60
Max. $\overline{RAS}$ Access Time, (t_{RAC})	40 ns	50 ns	60 ns
Max. Column Address Access Time, (t_{CAA})	20 ns	25 ns	30 ns
Min. Extended Data Out Page Mode Cycle Time, (t_{PC})	16 ns	20 ns	25 ns
Min. Read/Write Cycle Time, (t_{RC})	69 ns	84 ns	104 ns

Features

- 4M x 16-bit organization
- EDO Page Mode for a sustained data rate of 63 MHz
- $\overline{RAS}$ access time: 40, 50, 60 ns
- Dual $\overline{CAS}$ Inputs
- Low power dissipation
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh, Hidden Refresh
- Refresh Interval: 4096 cycles/64 ms
- Self refresh (L-version only)
- Available in 50-pin 400 mil TSOP-II
- Single +3.3 V ±0.3 V Power Supply
- LVTTL Interface

Description

The V53C365165A is a 4,194,304 x 16 bit high-performance CMOS dynamic random access memory. The V53C365165A offers Page mode operation with Extended Data Output. The V53C365165A has an symmetric address, 12-bit row and 10-bit column.

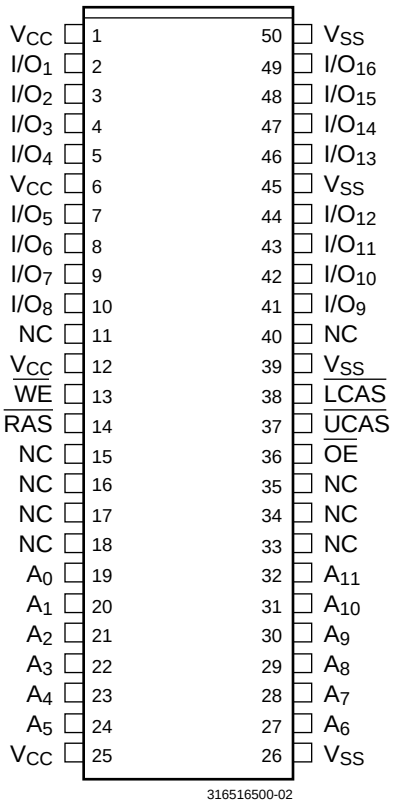
All inputs are TTL compatible. EDO Page Mode operation allows random access up to 1024 x 16 bits, within a page, with cycle times as short as 16 ns.

These features make the V53C365165A ideally suited for a wide variety of high performance computer systems and peripheral applications.

Device Usage Chart

Operating Temperature Range	Package Outline	Access Time (ns)			Power		Temperature Mark
	T	40	50	60	Std.	L	
0°C to 70°C	•	•	•	•	•	•	Blank

50 Pin Plastic TSOP-II PIN CONFIGURATION Top View



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Pin Names

A_0–A_{11}	Row, Column Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe/Upper Byte Control
$\overline{LCAS}$	Column Address Strobe/Lower Byte Control
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_1–I/O_{16}	Data Input, Output
V_{CC}	+3.3V Supply
V_{SS}	0V Supply
NC	No Connect

Description	Pkg.	Pin Count
TSOP-II	T	50

Absolute Maximum Ratings*

Operating temperature range .....0 to 70 °C
Storage temperature range ..... -55 to 150 °C
Soldering temperature .....260 °C
Soldering time.....10 s
Input/output voltage .... -0.5 to min (V_{CC}+0.5, 4.6) V
Power supply voltage .....-0.5V to 4.6 V
Power dissipation ..... 1.0 W
Data out current (short circuit) ..... 50 mA

*__Note:__ Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

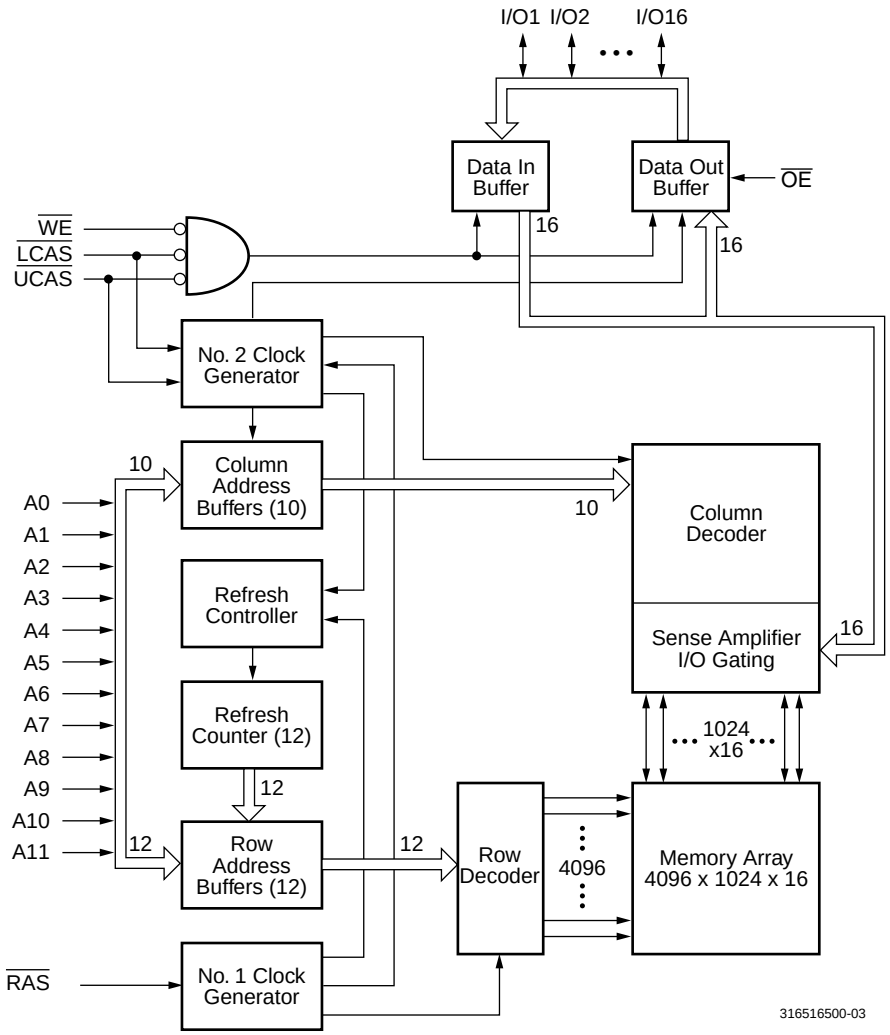
T_A = 25°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V, f = 1 Mhz

Symbol	Parameter	Min.	Max.	Unit
C_{IN1}	Address Input	—	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$	—	7	pF
C_{OUT}	Data Input/Output	—	7	pF

*__Note:__ Capacitance is sampled and not 100% tested.

Block Diagram

4M x 16



DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C365165A			Unit	Test Conditions	Notes
			Min.	Typ.	Max.			
I_{LI}	Input Leakage Current (any input pin)		–2		2	µA	$V_{SS} \le V_{IN} \le V_{CC}$	
I_{LO}	Output Leakage Current (for High-Z State)		–2		2	µA	$V_{SS} \le V_{OUT} \le V_{CC}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{CC1}	V_{CC} Supply Current, Operating	40			170	mA	$t_{RC} = t_{RC}$ (min.)	2, 3, 4
		50			140			
		60			115			
I_{CC2}	V_{CC} Supply Current, TTL Standby				1	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-Only Refresh	40			170	mA	$t_{RC} = t_{RC}$ (min.)	2, 4
		50			140			
		60			115			
I_{CC4}	V_{CC} Supply Current, EDO Page Mode Operation	40			140	mA	Minimum Cycle	2, 3, 4
		50			105			
		60			85			
I_{CC5}	V_{CC} Supply Current, CMOS Standby				500	µA	$\overline{RAS} \ge V_{CC} - 0.2$ V, $\overline{CAS} \ge V_{CC} - 0.2$ V	
I_{CC5}	V_{CC} Supply Current, CMOS Standby (L-Version)				120	µA	$\overline{RAS} \ge V_{CC} - 0.2$ V, $\overline{CAS} \ge V_{CC} - 0.2$ V	
I_{CC6}	Average Self Refresh Current CBR cycle with $t_{RAS} > t_{RASS}$ min., (L-version only) $\overline{CAS}$ held low, $\overline{WE} = V_{CC} - 0.2V$, Address and $D_{IN} = V_{CC} - 0.2V$ or 0.2V				400	µA		
I_{CC7}	V_{CC} Supply Current, during $\overline{CAS}$-before-$\overline{RAS}$ Refresh	40			170	mA		2, 4
		50			140			
		60			115			
V_{IL}	Input Low Voltage		–0.3		0.8	V		1
V_{IH}	Input High Voltage		2.0		V_{CC}+0.3	V		1
V_{OL}	Output Low Voltage (LVTTL)				0.4	V	I_{OL} = 2 mA	1
V_{OL}	Output Low Voltage (LVCMOS)				0.2	V	I_{OL} = 100 µA	1
V_{OH}	Output High Voltage (LVTTL)		2.4			V	I_{OH} = –2 mA	
V_{OH}	Output High Voltage (LVCMOS)		V_{CC}–0.2			V	I_{OH} = –100 µA	

Truth Table

Function		$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	Row Addr	Col Addr	I/O_1–I/O_{16}
Standby		H	H→X	H→X	X	X	X	X	High Impedance
Read: Word		L	L	H	H	L	ROW	COL	Data Out
Read: Lower Byte		L	L	H	H	L	ROW	COL	Lower Byte: Data Out Upper Byte: High-Z
Read: Upper Byte		L	H	L	H	L	ROW	COL	Lower Byte: High-Z Upper Byte: Data Out
Write: Word (Early Write)		L	L	L	L	X	ROW	COL	Data In
Write: Lower Byte (Early Write)		L	L	H	L	X	ROW	COL	Lower Byte: Data Out Upper Byte: High-Z
Write: Upper Byte (Early Write)		L	H	L	L	X	ROW	COL	Lower Byte: High-Z Upper Byte: Data Out
Read-Modify-Write		L	L	L	H→L	L→H	ROW	COL	Data Out, Data In
EDO Page Mode Read	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data Out
	2nd Cycle	L	H→L	H→L	H	L	N/A	COL	Data Out
EDO Page Mode Early Write (Word)	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data In
	2nd Cycle	L	H→L	H→L	L	X	N/A	COL	Data In
EDO Page Mode RMW	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data Out, Data In
	2nd Cycle	L	H→L	H→L	H→L	L→H	N/A	COL	Data Out, Data In
$\overline{RAS}$ only refresh		L	H	H	X	X	ROW	N/A	High Impedance
$\overline{CAS}$-before-$\overline{RAS}$ refresh		H→L	L	L	H	X	X	N/A	High Impedance
Test Mode Entry		H→L	L	L	L	X	X	N/A	High Impedance
Hidden Refresh (Read)		L→H→L	L	L	H	L	ROW	COL	Data Out
Hidden Refresh (Write)		L→H→L	L	L	L	X	ROW	COL	Data In
Self Refresh (L-Version)		H→L	L	H	X	X	X	X	High Impedance

AC Characteristics (5,6)

T_A = 0 to 70°C,V_{CC} = 3.3 V ±0.3V , t_T = 2 ns

#	Symbol	Parameter	-40		- 50		- 60		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
Common Parameters										
1	t_{RC}	Random read or write cycle time	69	—	84	—	104	—	ns	
2	t_{RAS}	$\overline{RAS}$ pulse width	40	100K	50	100K	60	100K	ns	
3	t_{CAS}	$\overline{CAS}$ pulse width	6	100K	8	100K	10	100K	ns	
4	t_{RP}	$\overline{RAS}$ precharge time	25	—	30	—	40	—	ns	
5	t_{CP}	$\overline{CAS}$ precharge time	6	—	8	—	10	—	ns	
6	t_{ASR}	Row address setup time	0	—	0	—	0	—	ns	
7	t_{RAH}	Row address hold time	5	—	7	—	10	—	ns	
8	t_{ASC}	Column address setup time	0	—	0	—	0	—	ns	
9	t_{CAH}	Column address hold time	5	—	7	—	10	—	ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	9	30	11	37	14	45	ns	
11	t_{RAD}	$\overline{RAS}$ to column address delay time	7	20	9	25	12	30	ns	
12	t_{RSH}	$\overline{RAS}$ hold time	6	—	8	—	10	—	ns	
13	t_{CSH}	$\overline{CAS}$ hold time	32	—	40	—	48	—	ns	
14	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	5	—	5	—	5	—	ns	
15	t_T	Transition time (rise and fall)	1	50	1	50	1	50	ns	7
16	t_{REF}	Refresh period for 4k-refresh version	—	64	—	64	—	64	ms	
17	t_{REF}	Refresh period for L-versions	—	256	—	256	—	256	ms	
Read Cycle										
18	t_{RAC}	Access time from $\overline{RAS}$	—	40	—	50	—	60	ns	8, 9
19	t_{CAC}	Access time from $\overline{CAS}$	—	10	—	13	—	15	ns	8, 9
20	t_{CAA}	Access time from column address	—	20	—	25	—	30	ns	8,10
21	t_{OEA}	$\overline{OE}$ access time	—	10	—	13	—	15	ns	
22	t_{RAL}	Column address to $\overline{RAS}$ lead time	20	—	25	—	30	—	ns	
23	t_{RCS}	Read command setup time	0	—	0	—	0	—	ns	
24	t_{RCH}	Read command hold time	0	—	0	—	0	—	ns	11
25	t_{RRH}	Read command hold time referenced to $\overline{RAS}$	0	—	0	—	0	—	ns	11
26	t_{CLZ}	$\overline{CAS}$ to output in low-Z	0	—	0	—	0	—	ns	8
27	t_{OFF}	Output buffer turn-off delay	0	10	0	13	0	15	ns	12
28	t_{OEZ}	Output buffer turn-off delay from $\overline{OE}$	0	10	0	13	0	15	ns	12
29	t_{DZC}	Data to $\overline{CAS}$ low delay	0	—	0	—	0	—	ns	13
30	t_{DZO}	Data to $\overline{OE}$ low delay	0	—	0	—	0	—	ns	13

AC Characteristics (5,6) (Cont'd)

T_A = 0 to 70°C,V_{CC} = 3.3 V ±0.3V , t_T = 2 ns

#	Symbol	Parameter	-40		- 50		- 60		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
31	t_{CDD}	$\overline{CAS}$ high to data delay	10	—	13	—	15	—	ns	14
32	t_{ODD}	***$\overline{OE}$*** high to data delay	10	—	13	—	15	—	ns	14
Write Cycle										
33	t_{WCH}	Write command hold time	5	—	7	—	10	—	ns	
34	t_{WP}	Write command pulse width	5	—	7	—	10	—	ns	
35	t_{WCS}	Write command setup time	0	—	0	—	0	—	ns	15
36	t_{RWL}	Write command to $\overline{RAS}$ lead time	6	—	8	—	10	—	ns	
37	t_{CWL}	Write command to $\overline{CAS}$ lead time	6	—	8	—	10	—	ns	
38	t_{DS}	Data setup time	0	—	0	—	0	—	ns	16
39	t_{DH}	Data hold time	5	—	7	—	10	—	ns	16
Read-Modify-Write Cycle										
40	t_{RWC}	Read-write cycle time	89	—	109	—	133	—	ns	
41	t_{RWD}	$\overline{RAS}$ to WE delay time	52	—	65	—	77	—	ns	15
42	t_{CWD}	$\overline{CAS}$ to ***$\overline{WE}$*** delay time	22	—	28	—	32	—	ns	15
43	t_{AWD}	Column address to $\overline{WE}$ delay time	32	—	40	—	47	—	ns	15
44	t_{OEH}	$\overline{OE}$ command hold time	5	—	7	—	10	—	ns	
EDO Page Mode Cycle										
45	t_{PC}	EDO Page Mode cycle time	16	—	20	—	24	—	ns	
46	t_{CPA}	Access time from $\overline{CAS}$ precharge	—	22	—	27	—	32	ns	7
47	t_{COH}	Output data hold time	3	—	5	—	5	—	ns	
48	t_{RAS}	$\overline{RAS}$ pulse width in EDO page mode	40	200K	50	200K	60	200K	ns	
49	t_{RHPC}	$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	22	—	27	—	32	—	ns	
50	t_{OEP}	$\overline{OE}$ pulse width	5	—	5	—	5	—	ns	
51	t_{OEHC}	$\overline{OE}$ hold time from $\overline{CAS}$ high	5	—	5	—	5	—	ns	
52	t_{WEZ}	Output buffer turn-off delay from $\overline{WE}$	0	10	0	13	0	15	ns	
53	tOES	OE setup time prior to CAS	5	—	5	—	5	—	ns	
EDO Page Mode Read-Modify-Write Cycle										
54	t_{PRWC}	EDO page mode read-write cycle time	44	—	54	—	63	—	ns	
55	t_{CPWD}	$\overline{CAS}$ precharge to $\overline{WE}$	34	—	42	—	49	—	ns	

AC Characteristics (5,6) (Cont'd)

T_A = 0 to 70°C,V_{CC} = 3.3 V ±0.3V , t_T = 2 ns

#	Symbol	Parameter	-40		- 50		- 60		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle										
56	t_{CSR}	$\overline{CAS}$ setup time	5	—	5	—	5	—	ns	
57	t_{CHR}	$\overline{CAS}$ hold time	5	—	5	—	10	—	ns	
58	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time	5	—	5	—	5	—	ns	
59	t_{WRP}	Write to $\overline{RAS}$ precharge time	5	—	5	—	10	—	ns	
60	t_{WRH}	Write hold time referenced to $\overline{RAS}$	5	—	5	—	10	—	ns	
Self Refresh Cycle (L-Version)										
61	t_{RASS}	$\overline{RAS}$ pulse width	100K	—	100K	—	100K	—	ns	17
62	t_{RPS}	$\overline{RAS}$ precharge time	69	—	84	—	104	—	ns	17
63	t_{CHS}	$\overline{CAS}$ hold time	50	—	50	—	50	—	ns	17

Notes:

1. All voltages are referenced to V_{SS}.
   V_{IH} may overshoot to V_{CC} + 0.2V for pulse widths of < 4ns with 3.3V. V_{IL} may undershoot to -2.0V for pulse width < 4.0 ns with 3.3V. Pulse width measured at 50% points with amplitude measured peak to DC reference.
2. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} and I_{CC7} depend on cycle rate.
3. I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
4. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4} it can be changed once or less during a hyper page mode cycle (t_{PC}).
5. An initial pause of 100 µs is required after power-up followed by 8 $\overline{RAS}$-only-refresh cycles, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T = 2 ns.
7. $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with the specified current load and 100 pF at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
9. Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.
10. Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{CAA}.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
13. Either t_{DZC} or t_{DZO} must be satisfied.
14. Either t_{CDD} or t_{ODD} must be satisfied.

15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$, $t_{AWD} > t_{AWD\ (min.)}$ and $t_{CPWD} > t_{CPWD\ (min.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.

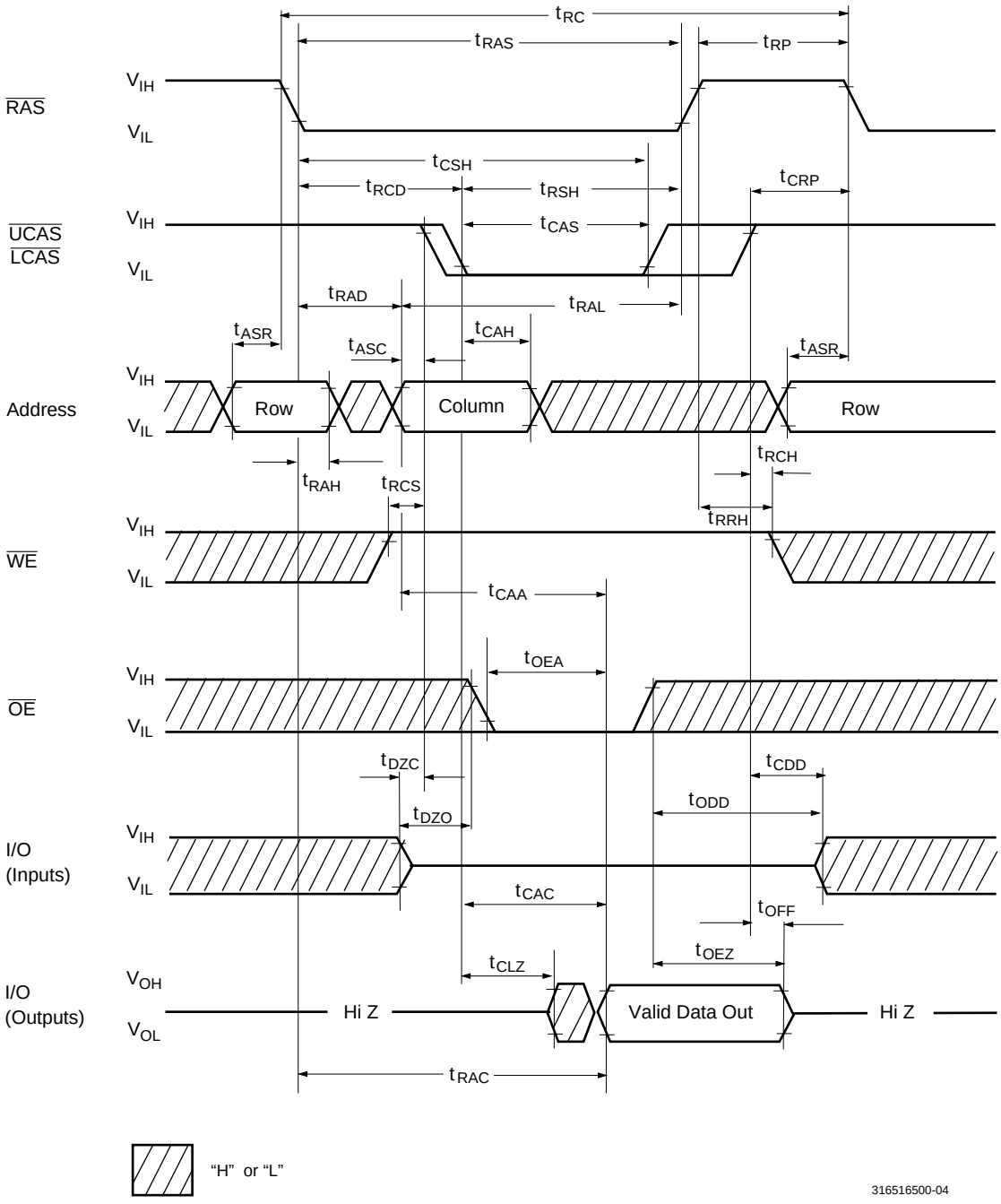
16. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

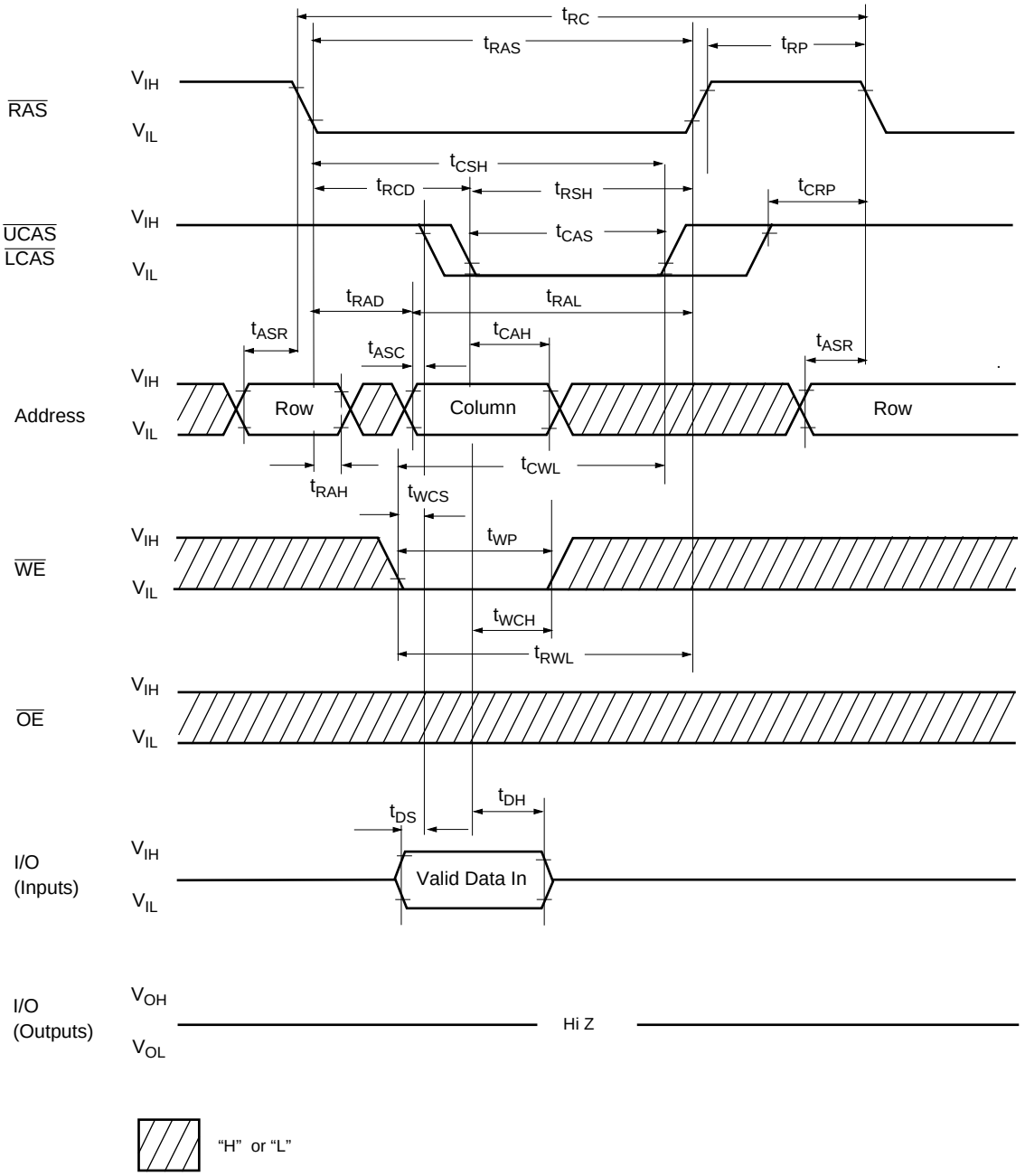
    If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

    If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.

Waveforms of Read Cycle



Waveforms of Write Cycle (Early Write)



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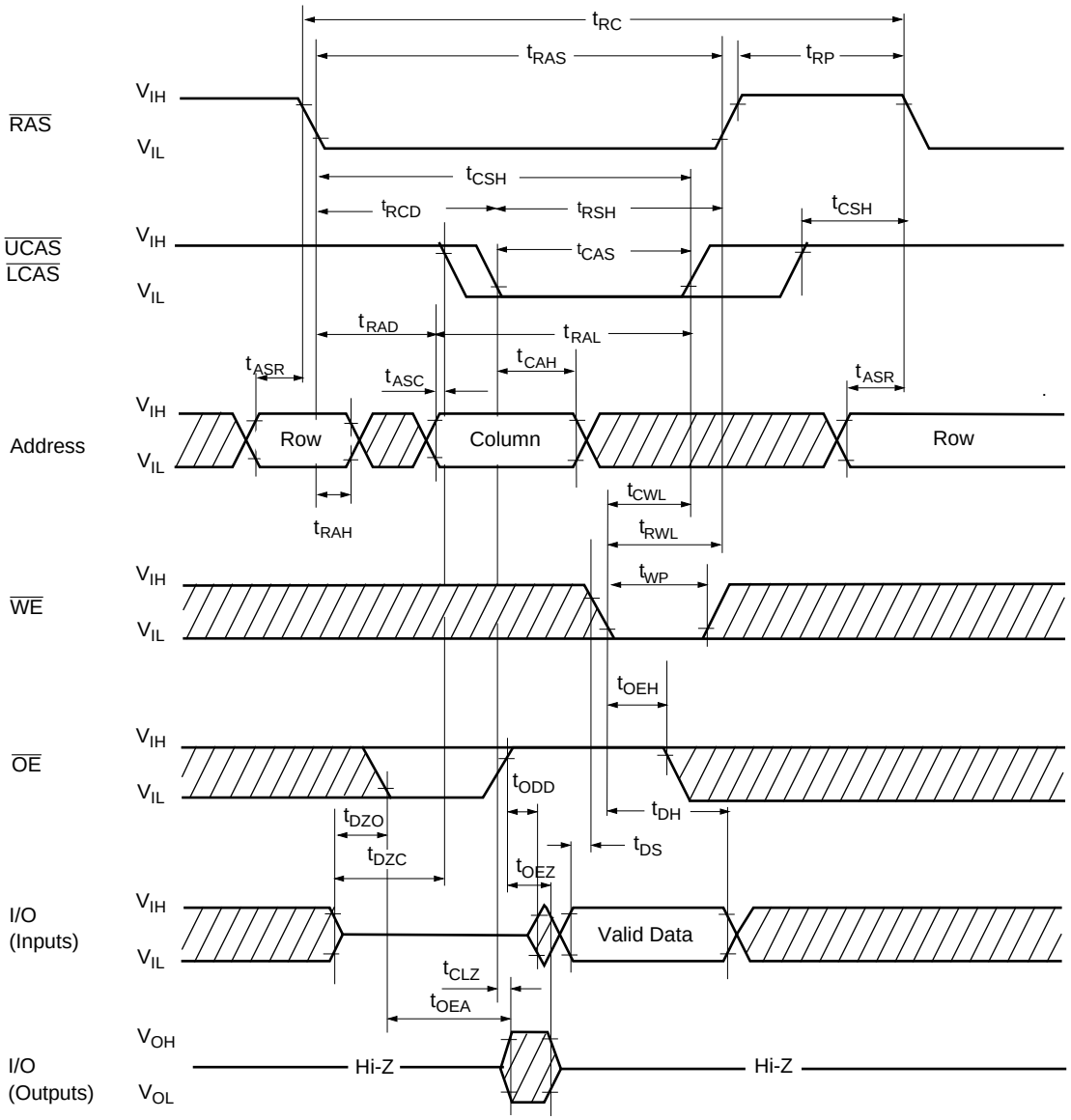
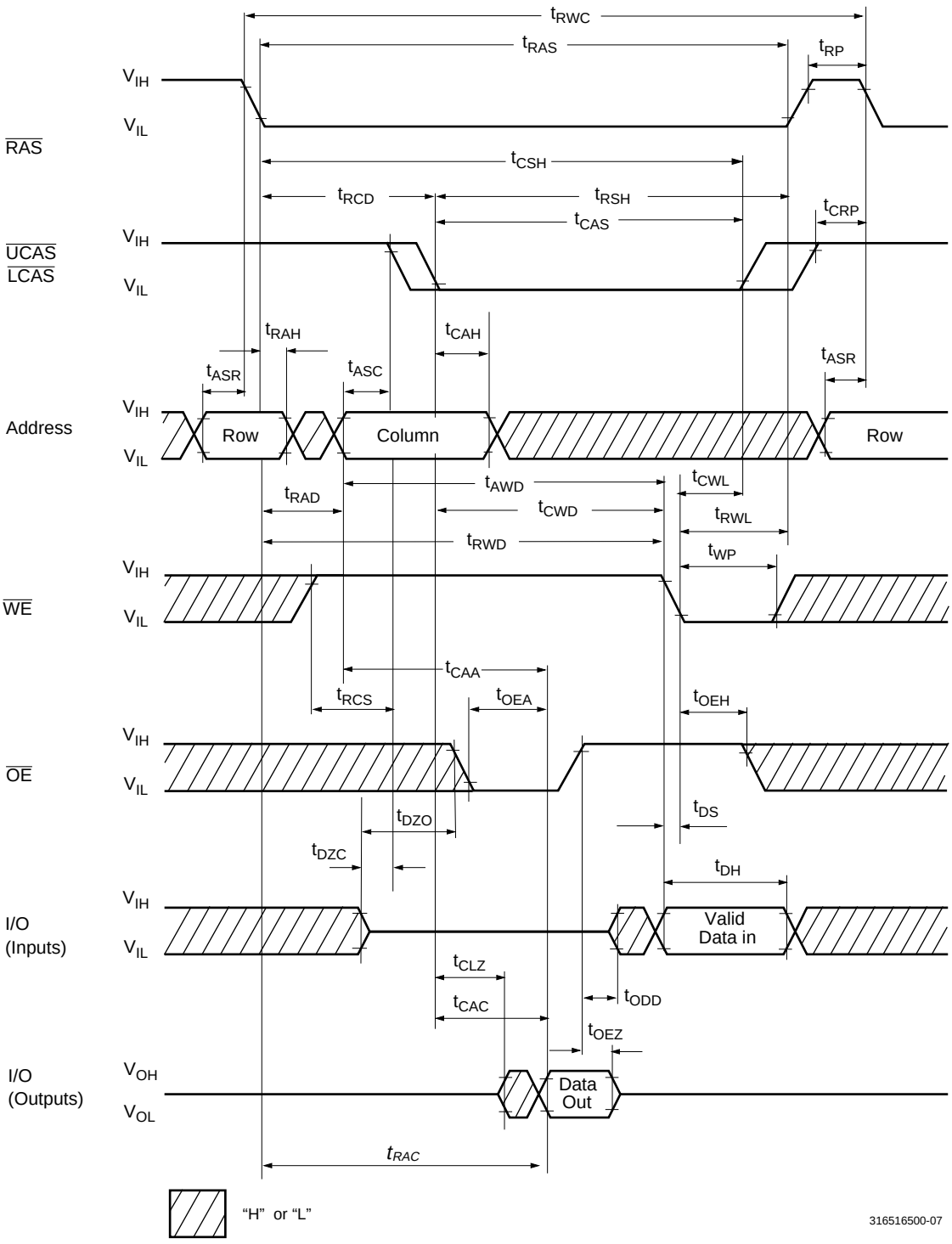
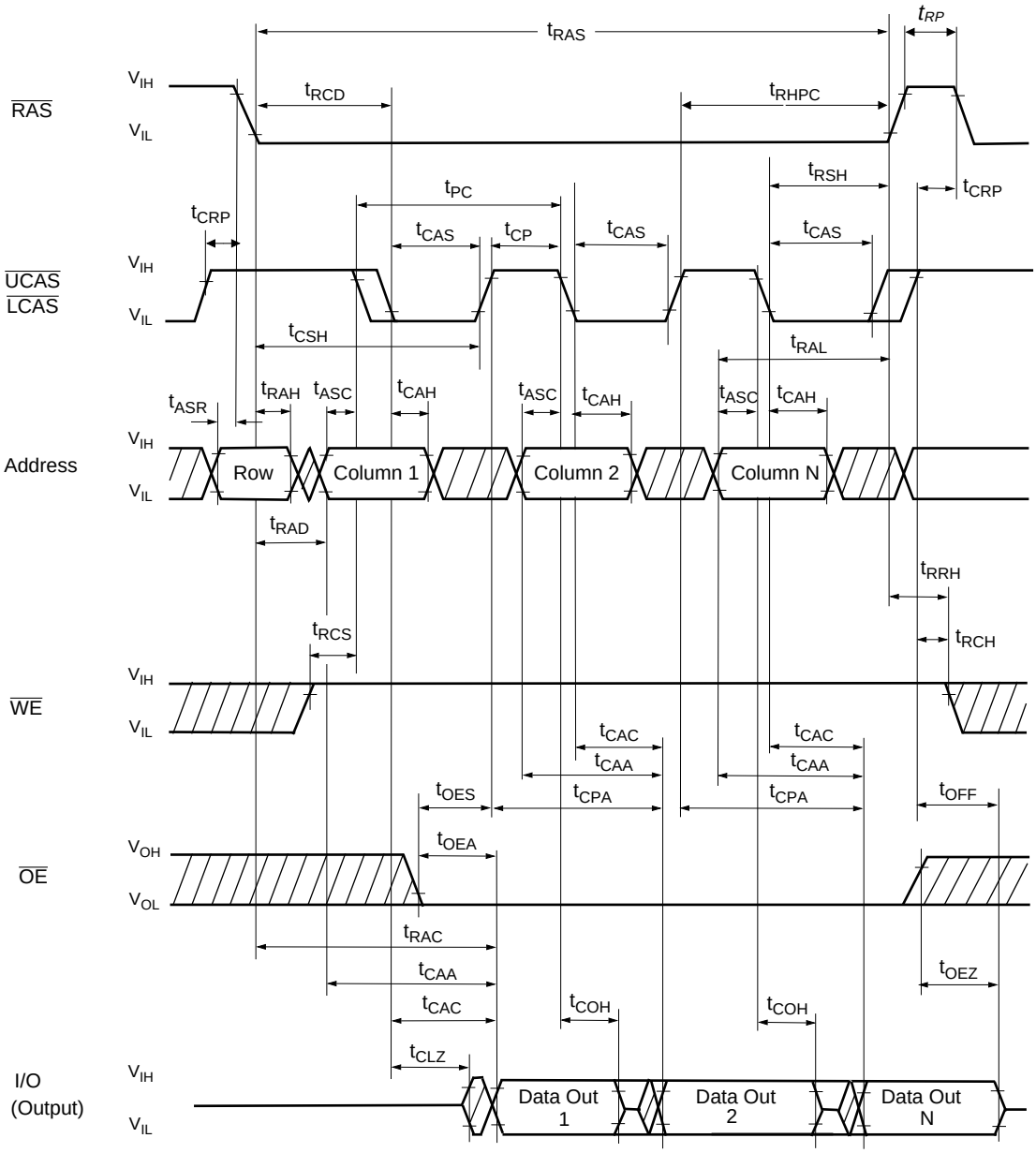
Waveforms of Write Cycle ($\overline{OE}$ Controlled Write)



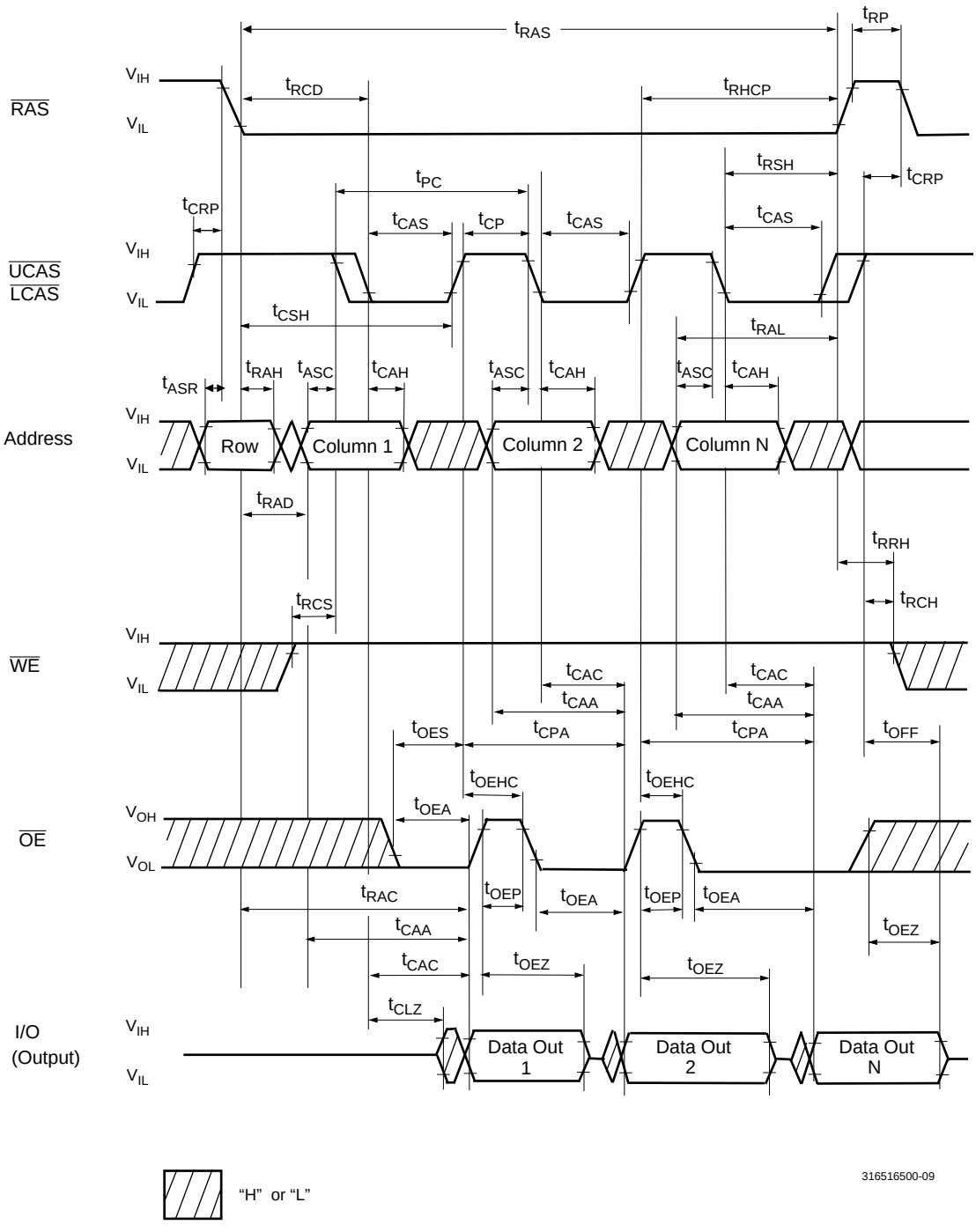
Waveforms of Read-Write (Read-Modify-Write) Cycle



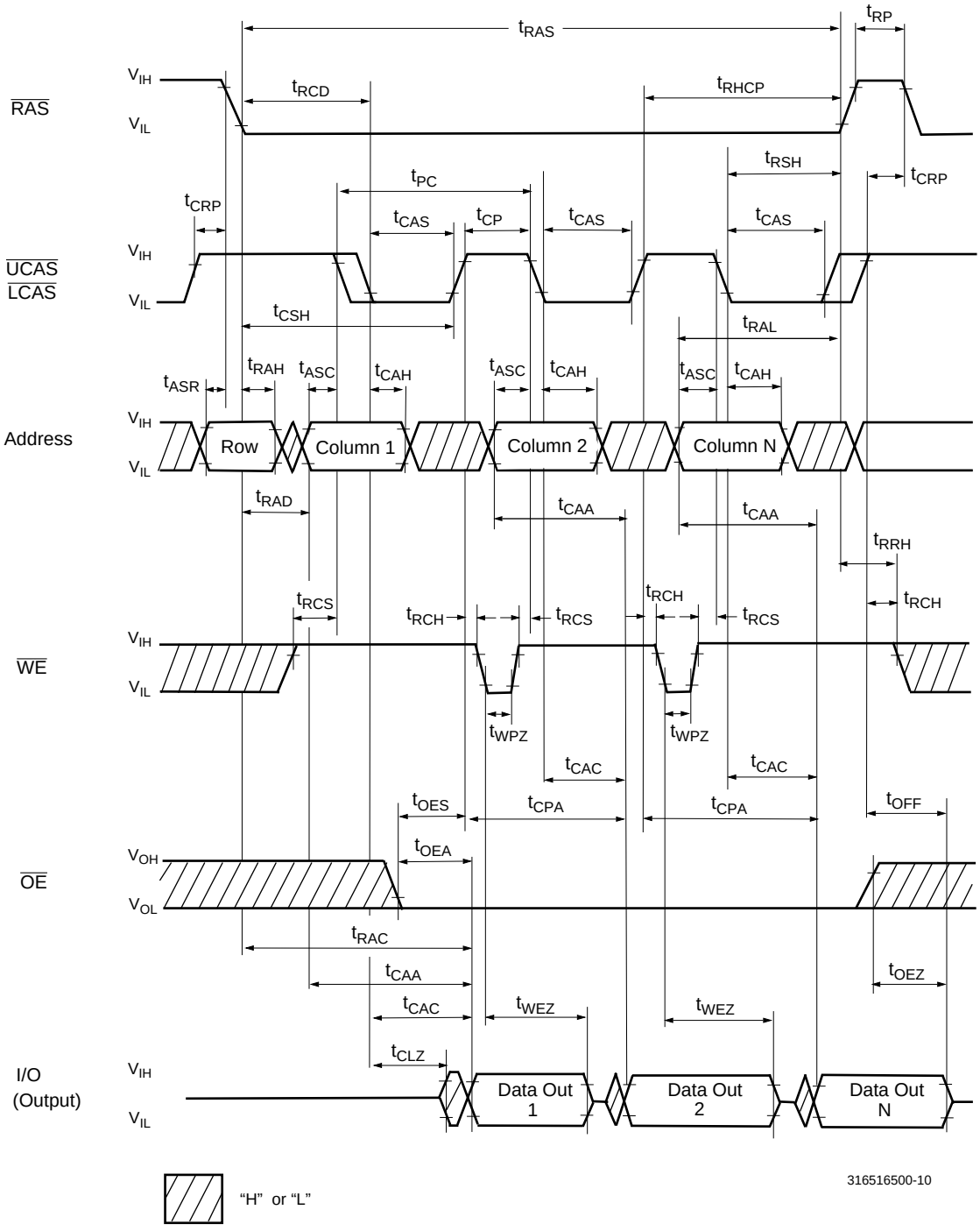
Waveforms of EDO Page Mode Read Cycle



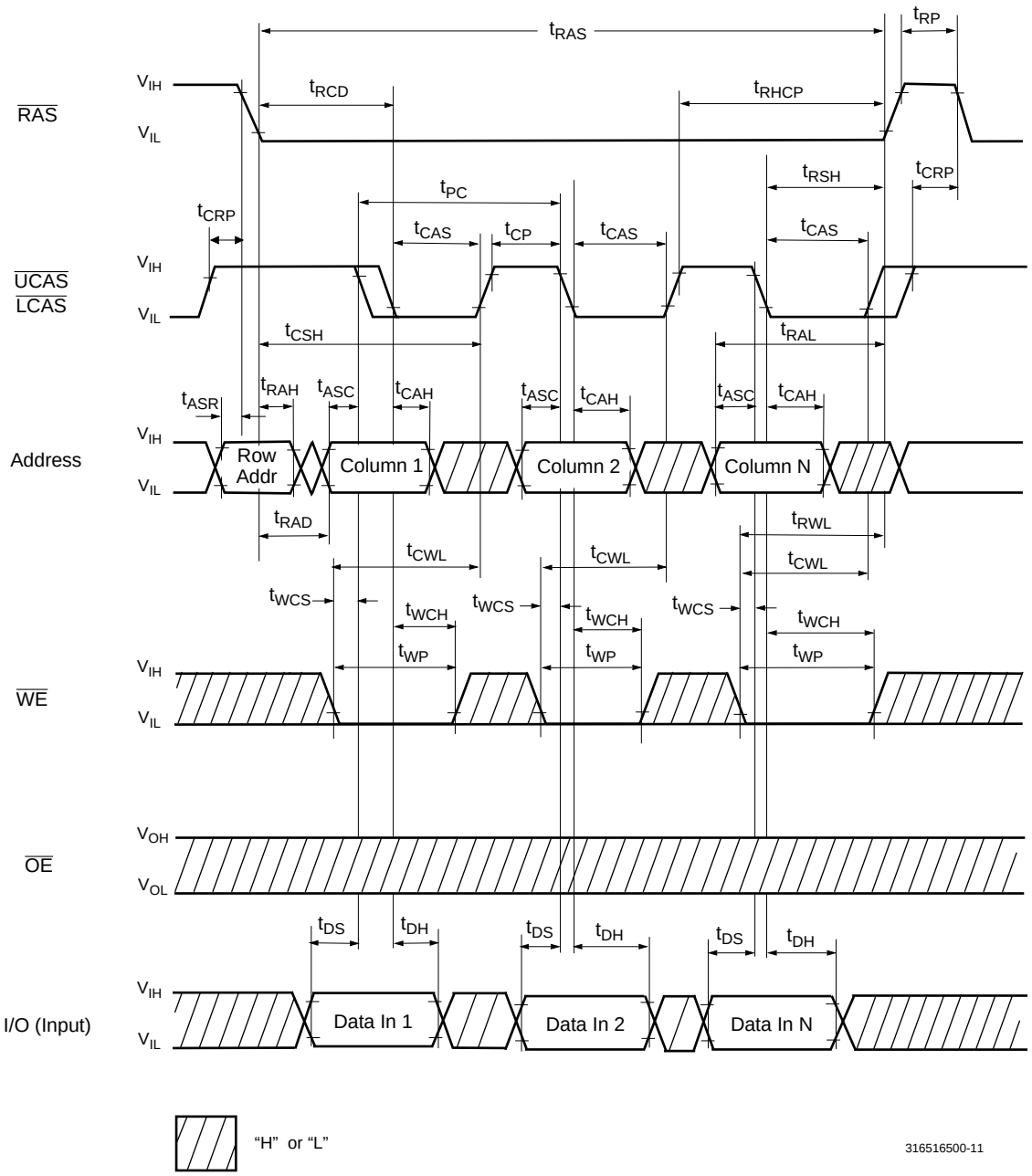
Waveforms of EDO Page Mode Read Cycle ($\overline{OE}$ Control)



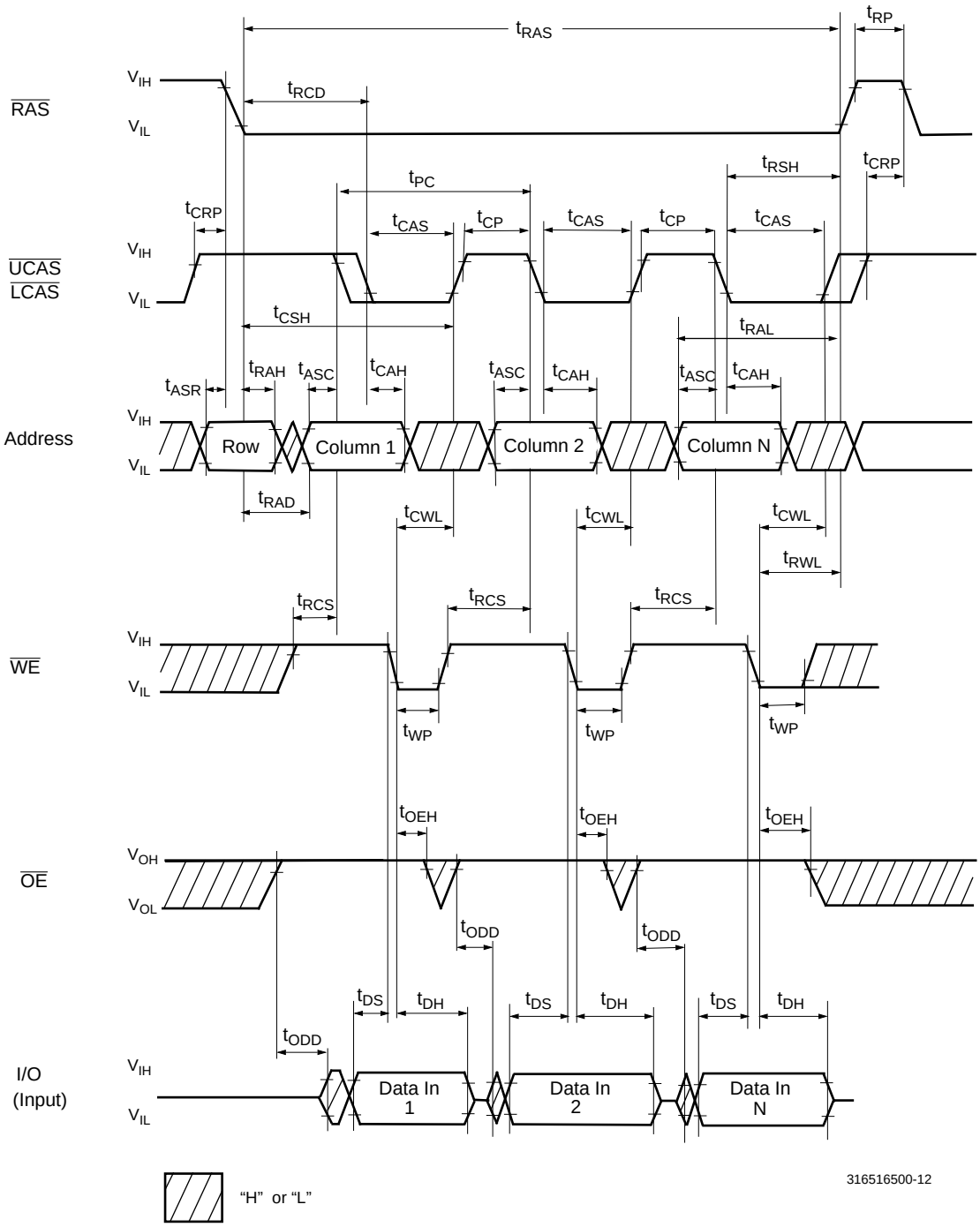
Waveforms of EDO Page Mode Read Cycle ($\overline{WE}$ Control)



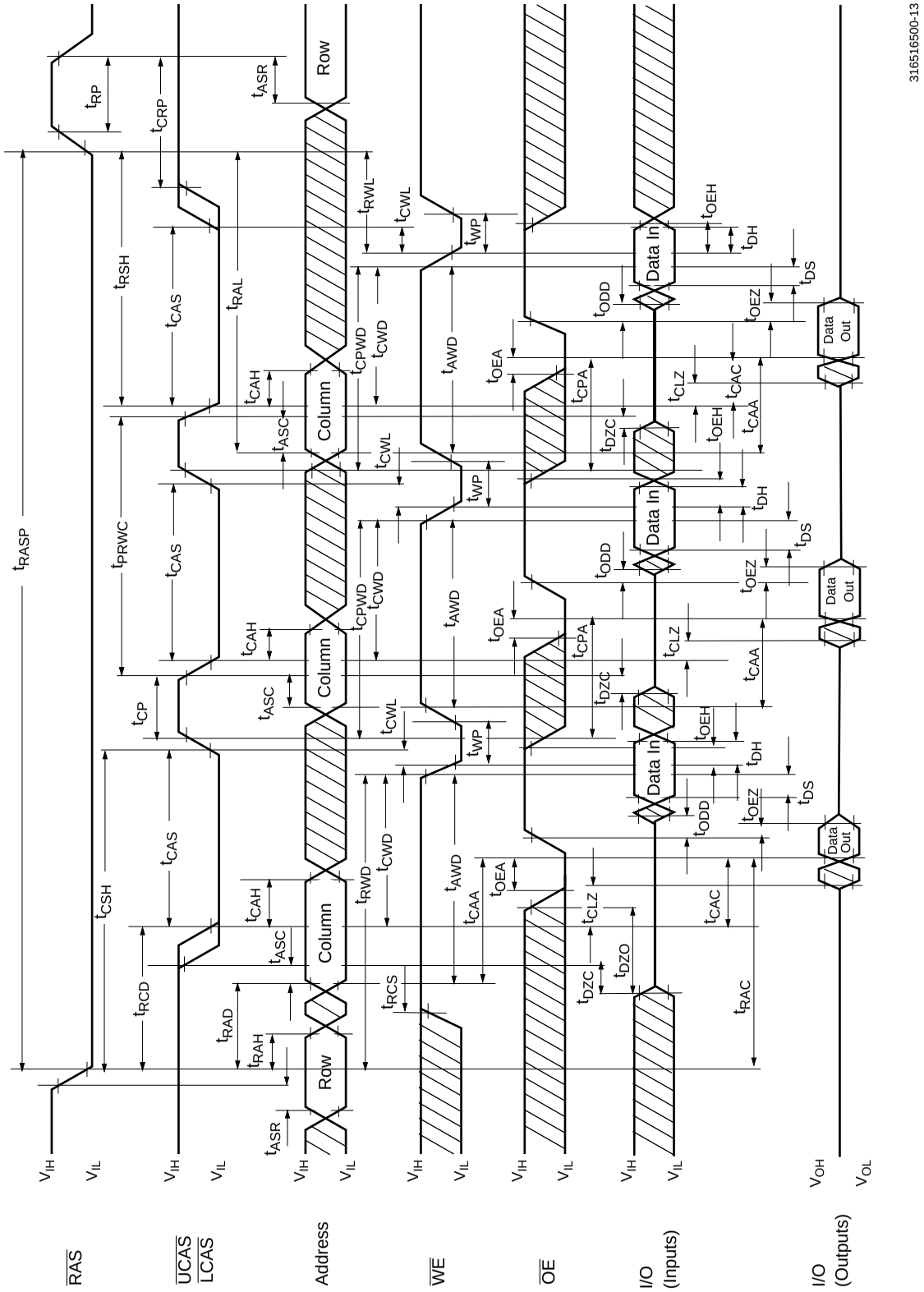
Waveforms of EDO Page Mode Early Write Cycle



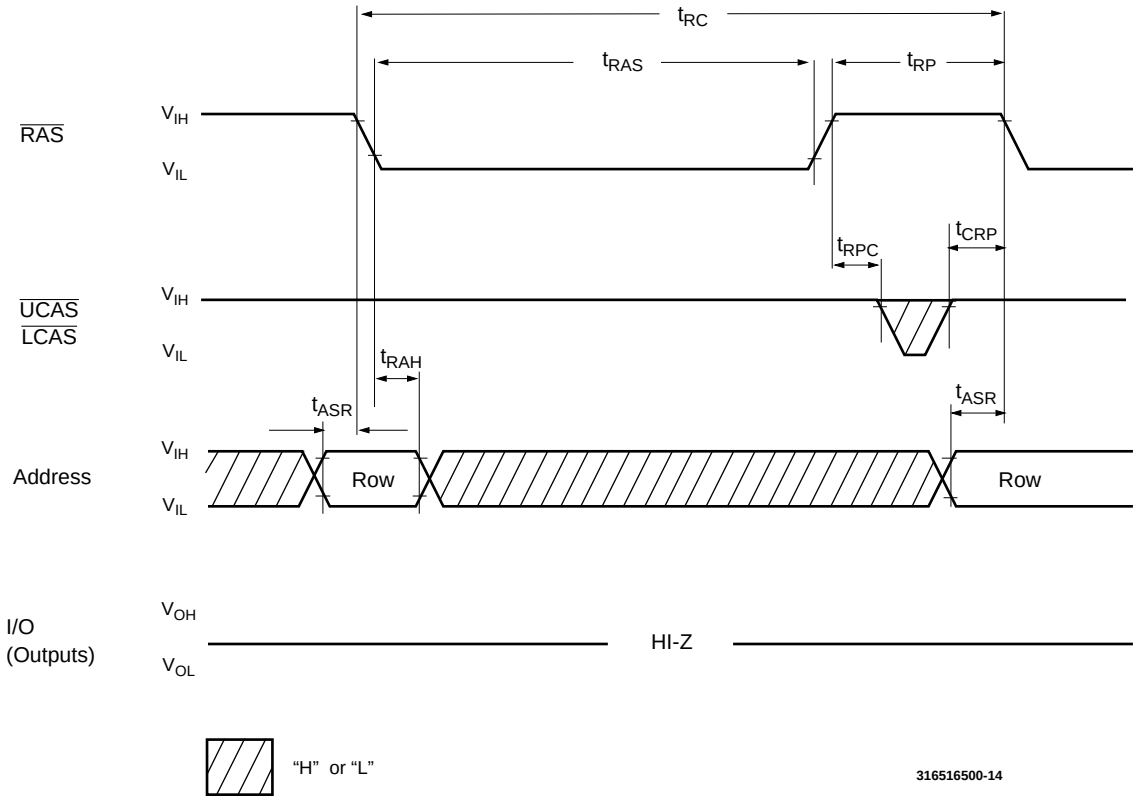
Waveforms of EDO Page Mode Late Write Cycle



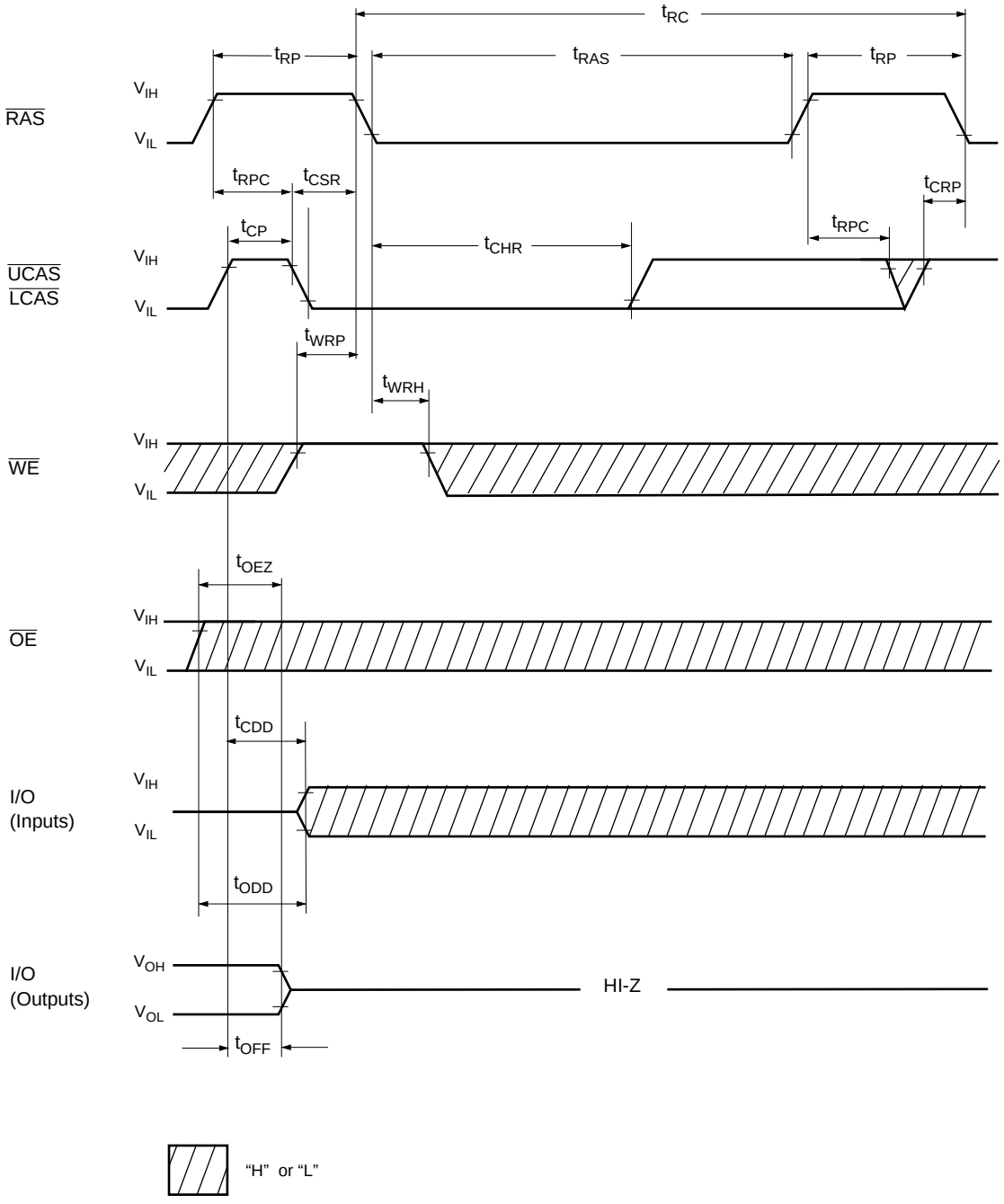
Waveforms of EDO Page Mode Read-Modify-Write Cycle



Waveforms of $\overline{RAS}$ Only Refresh Cycle



Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



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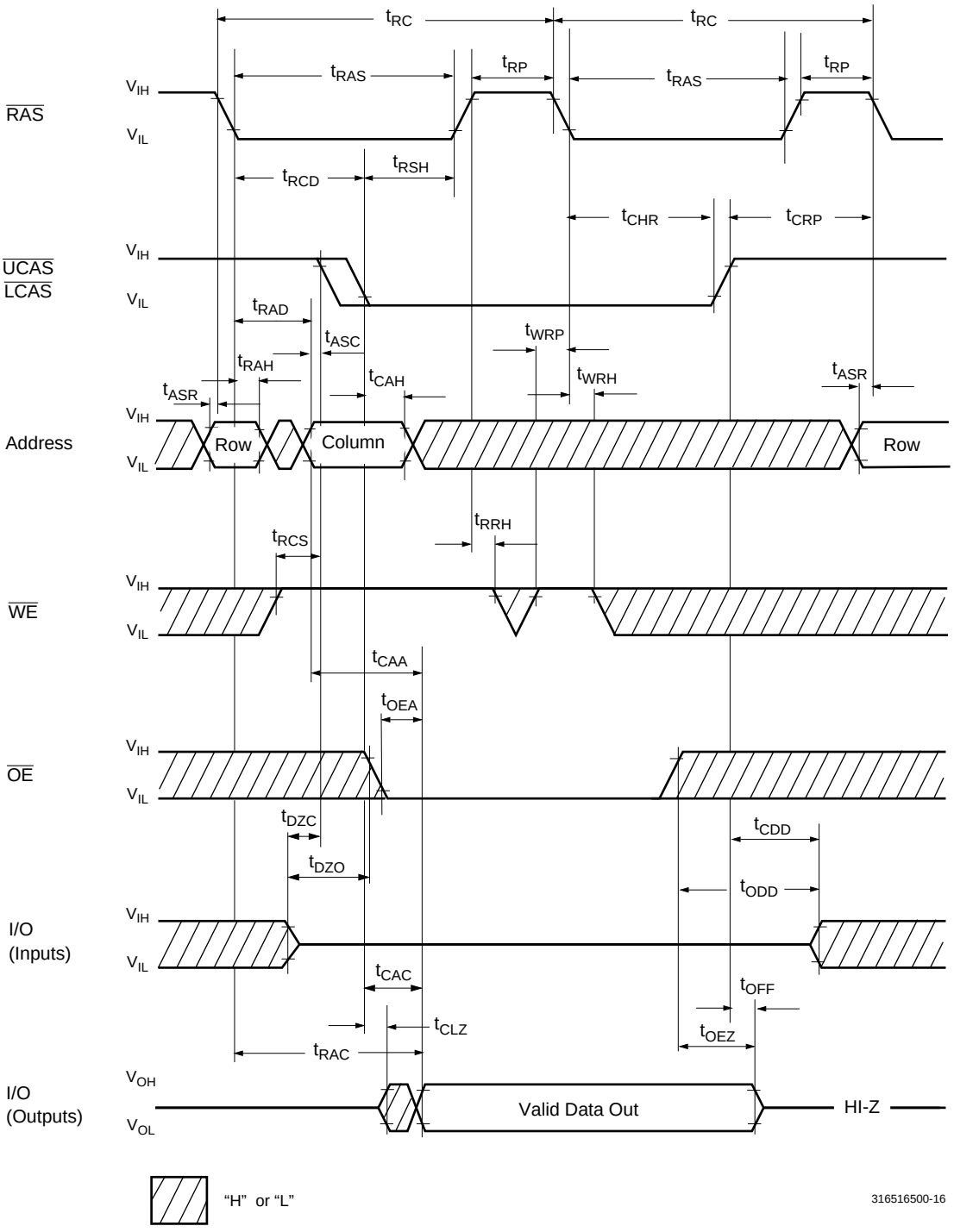
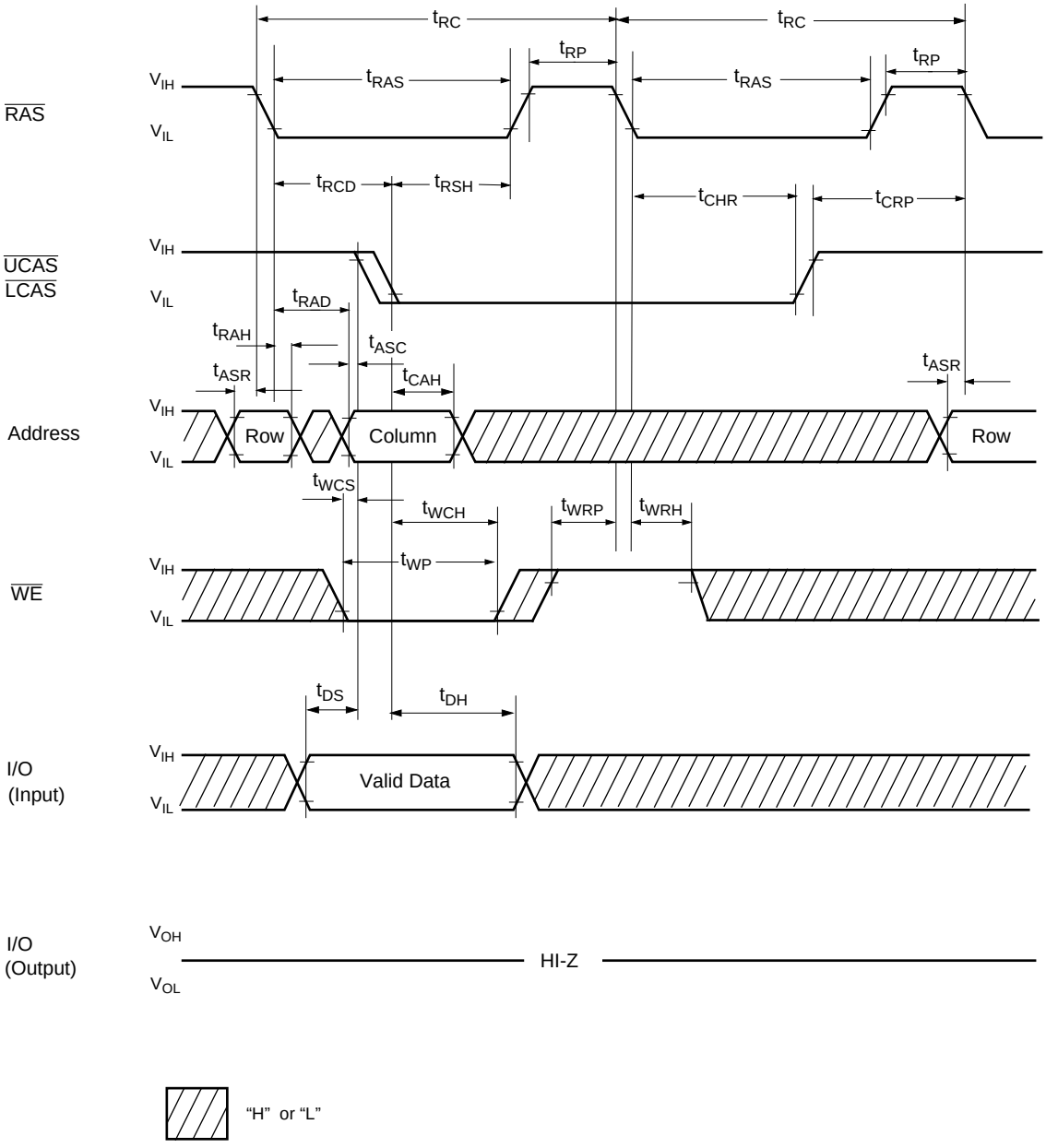
Waveforms of Hidden Refresh Read Cycle

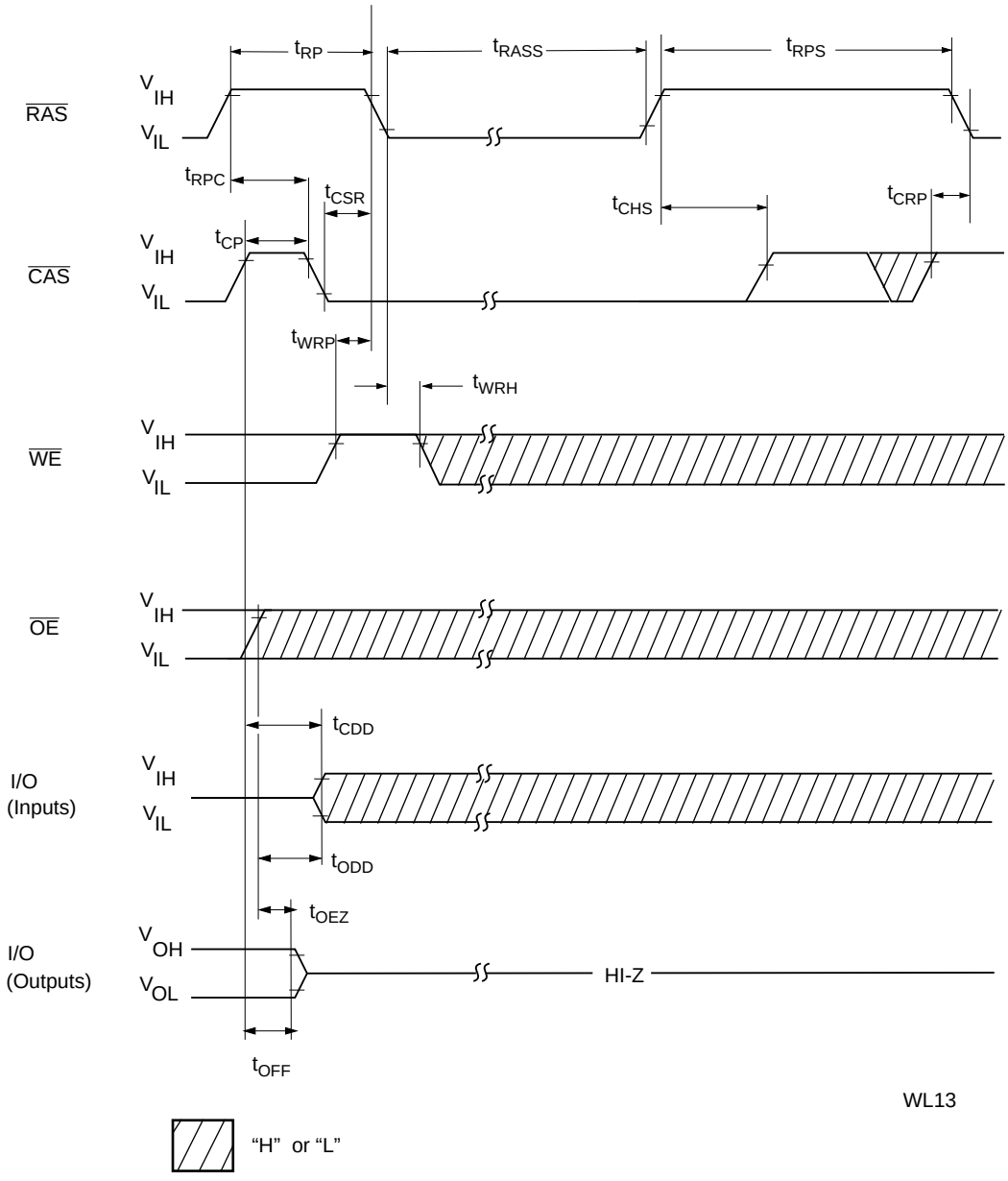


Waveforms of Hidden Refresh Early Write Cycle



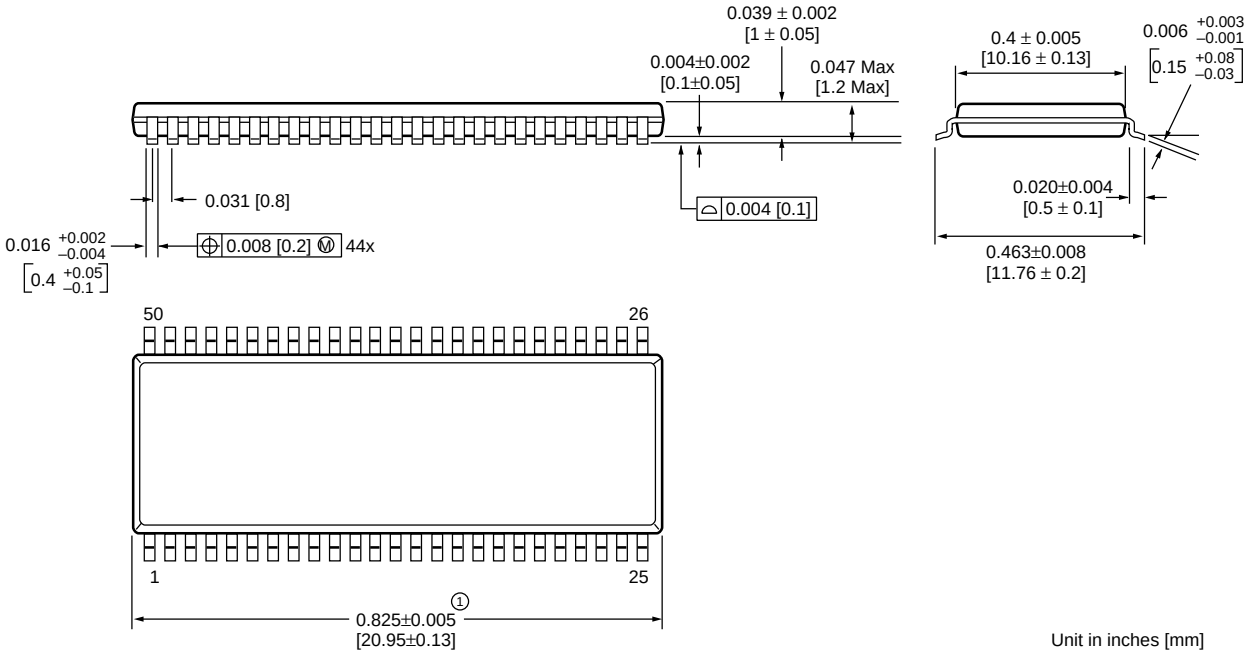
316516500-17

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Self Refresh Cycle



Package Diagrams

50-Pin 400 mil TSOP-II



Unit in inches [mm]

① Does not include plastic or metal protrusion of 0.010 [0.25] max. per side

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