

V53C517400A	50	60
Max. $\overline{\text{RAS}}$ Access Time, (t_{RAC})	50 ns	60 ns
Max. Column Address Access Time, (t_{CAA})	25 ns	30 ns
Min. Page Mode Cycle Time, (t_{PC})	35 ns	40 ns
Min. Read/Write Cycle Time, (t_{RC})	84 ns	104 ns

Features

- 4M x 4-bit organization
- Fast Page Mode for a sustained data rate of 50 MHz
- $\overline{\text{RAS}}$ access time: 50, 60 ns
- Low power dissipation
- Read-Modify-Write, $\overline{\text{RAS}}$ -Only Refresh, $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh, Hidden Refresh and Self-Refresh
- Refresh Interval: 2048 cycles/32 ms
- Available in 24/26-pin 300 mil SOJ, and 24/26-pin 300 mil TSOP-II
- Single +5V $\pm 10\%$ Power Supply
- TTL Interface

Description

The V53C517400A is a 4,194,304 x 4 bit high-performance CMOS dynamic random access memory. The V53C517400A offers Page mode operation. The V53C517400A has symmetric address, 11-bit row and 11-bit column, 2K refresh.

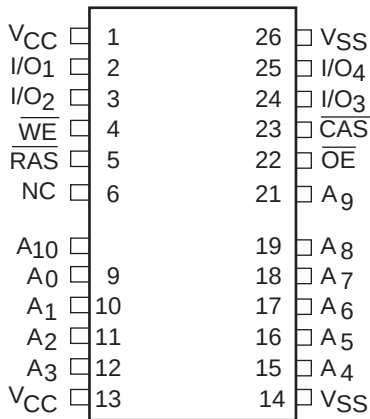
All inputs are TTL compatible. Fast Page Mode operation allows random access up to 2048 x 4 bits, within a page, with cycle times as short as 35ns.

These features make the V53C517400A ideally suited for a wide variety of high performance computer systems and peripheral applications.

Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)		Power	Temperature Mark
	K	T	50	60	Std.	
0°C to 70°C	•	•	•	•	•	Blank

**24/26-Pin Plastic SOJ/TSOP-II
PIN CONFIGURATION
Top View**



311740002-02

Pin Names

A ₀ –A ₁₀	Row, Column Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
I/O ₁ –I/O ₄	Data Input, Output
V _{CC}	5V Supply
V _{SS}	0V Supply
NC	No Connect

Description	Pkg.	Pin Count
SOJ	K	26/24
TSOP-II	T	26/24

Absolute Maximum Ratings*

Operating temperature range 0 to 70 °C
 Storage temperature range -55 to 150 °C
 Input/output voltage -0.5 to min ($V_{CC}+0.5$, 7.0) V
 Power supply voltage -1.0 to 7.0 V
 Power dissipation 1.0 W
 Data out current (short circuit) 50 mA

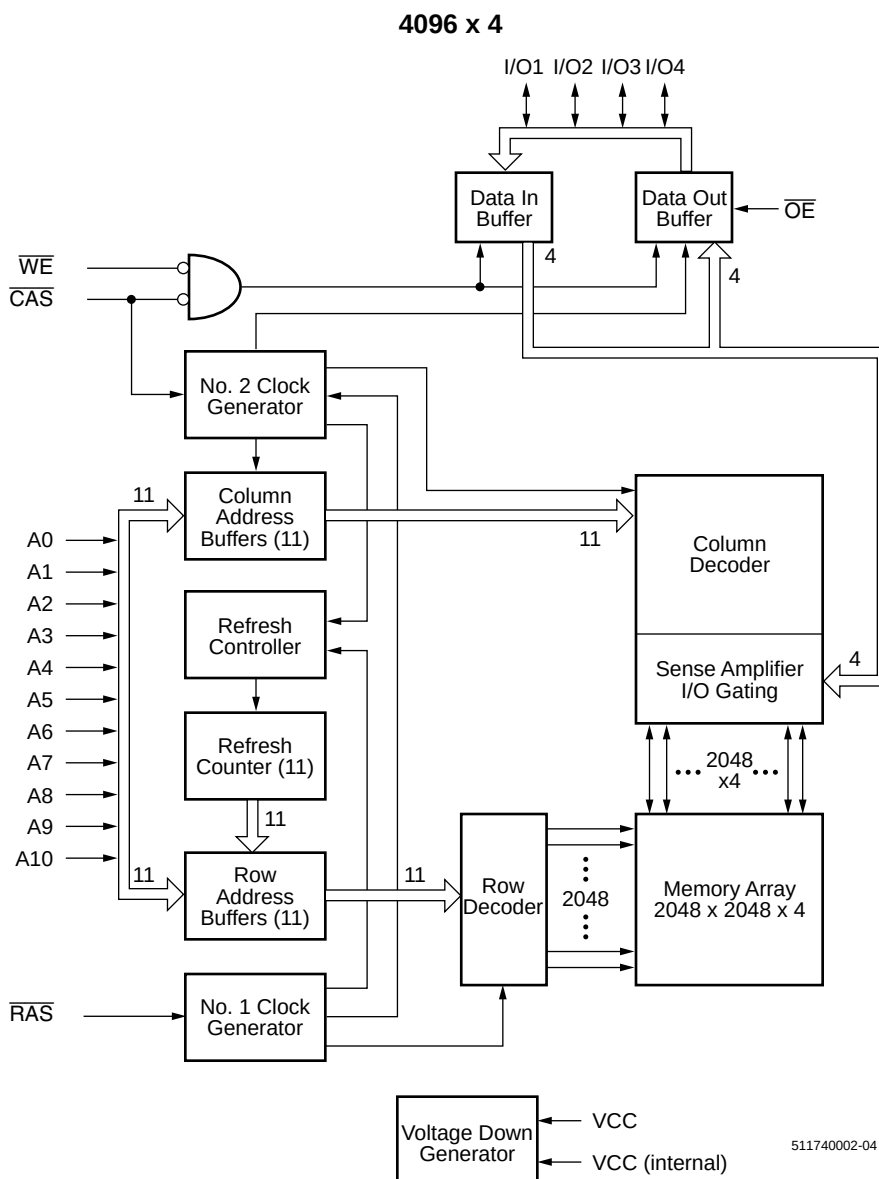
*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

$T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address Input	—	5	pF
C_{IN2}	$\overline{\text{RAS}}$, CAS , $\overline{\text{WE}}$, $\overline{\text{OE}}$	—	7	pF
C_{OUT}	Data Input/Output	—	7	pF

*Note: Capacitance is sampled and not 100% tested.

Block Diagram

DC and Operating Characteristics (1-2)

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise specified.

Symbol	Parameter	Access Time	V53C517400A			Unit	Test Conditions	Notes
			Min.	Typ.	Max.			
I_{LI}	Input Leakage Current (any input pin)		-10		10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$	1
I_{LO}	Output Leakage Current (for High-Z State)		-10		10	μA	$V_{SS} \leq V_{OUT} \leq V_{CC}$ RAS, $\overline{\text{CAS}}$ at V_{IH}	1
I_{CC1}	V_{CC} Supply Current, Operating	50			120	mA	$t_{RC} = t_{RC}(\text{min.})$	2, 3, 4
		60			110			
I_{CC2}	V_{CC} Supply Current, TTL Standby				2	mA	RAS, $\overline{\text{CAS}}$ at V_{IH} other inputs $\geq V_{SS}$	
I_{CC3}	V_{CC} Supply Current, RAS-Only Refresh	50			120	mA	$t_{RC} = t_{RC}(\text{min.})$	2, 4
		60			110			
I_{CC4}	V_{CC} Supply Current, Fast Page Mode Operation	50			40	mA	Minimum Cycle	2, 3, 4
		60			35			
I_{CC5}	V_{CC} Supply Current, during $\overline{\text{CAS}}$ -before-RAS Refresh	50			120	mA		2, 4
		60			110			
I_{CC6}	V_{CC} Supply Current, CMOS Standby				1.0	mA	RAS $\geq V_{CC} - 0.2\text{V}$, CAS $\geq V_{CC} - 0.2\text{V}$ other input $\geq V_{SS}$	1
I_{CC7}	Average Self Refresh Current (CBR cycle with $t_{RAS} > t_{RASSmin.}$, $\overline{\text{CAS}}$ held low, $\overline{\text{WE}} = V_{CC} - 0.2\text{V}$, Address and Din = $V_{CC} - 0.2\text{V}$ or 0.2V)				1.0	mA		
V_{CC}	Power Supply Voltage		4.5	5.0	5.5	V		
V_{IL}	Input Low Voltage		-0.5		0.8	V		1
V_{IH}	Input High Voltage		2.4		$V_{CC} + 0.5$	V		1
V_{OL}	Output Low Voltage				0.4	V	$I_{OUT} = 4.2\text{mA}$	1
V_{OH}	Output High Voltage		2.4		0.4	V	$I_{OUT} = -5\text{mA}$	

AC Characteristics^(5,6) $T_A = 0 \text{ to } 70^\circ\text{C}, V_{CC} = 5V \pm 10\%, t_T = 2 \text{ ns}$

#	Symbol	Parameter	-50		-60		Unit	Note
			min.	max.	min.	max.		
Common Parameters								
1	t _{RC}	Random read or write cycle time	90	–	110	–	ns	
2	t _{RP}	$\overline{\text{RAS}}$ precharge time	30	–	40	–	ns	
3	t _{RAS}	$\overline{\text{RAS}}$ pulse width	50	10k	60	10k	ns	
4	t _{CAS}	$\overline{\text{CAS}}$ pulse width	13	10k	15	10k	ns	
5	t _{ASR}	Row address setup time	0	–	0	–	ns	
6	t _{RAH}	Row address hold time	8	–	10	–	ns	
7	t _{ASC}	Column address setup time	0	–	0	–	ns	
8	t _{CAH}	Column address hold time	10	–	15	–	ns	
9	t _{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	18	37	20	45	ns	
10	t _{RAD}	$\overline{\text{RAS}}$ to column address delay	13	25	15	30	ns	
11	t _{RSH}	$\overline{\text{RAS}}$ hold time	13		15	–	ns	
12	t _{CSH}	$\overline{\text{CAS}}$ hold time	50		60	–	ns	
13	t _{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	5	–	5	–	ns	
14	t _T	Transition time (rise and fall)	3	50	3	50	ns	7
15	t _{REF}	Refresh period	–	32	–	32	ms	
Read Cycle								
16	t _{RAC}	Access time from $\overline{\text{RAS}}$	–	50	–	60	ns	8, 9
17	t _{CAC}	Access time from $\overline{\text{CAS}}$	–	13	–	15	ns	8, 9
18	t _{CAA}	Access time from column address	–	25	–	30	ns	8,10
19	t _{OEA}	$\overline{\text{OE}}$ access time	–	13	–	15	ns	
20	t _{RAL}	Column address to $\overline{\text{RAS}}$ lead time	25	–	30	–	ns	
21	t _{RCS}	Read command setup time	0	–	0	–	ns	
22	t _{RCH}	Read command hold time	0	–	0	–	ns	11
23	t _{RRH}	Read command hold time referenced to $\overline{\text{RAS}}$	0	–	0	–	ns	11
24	t _{CLZ}	$\overline{\text{CAS}}$ to output in low-Z	0	–	0	–	ns	8
25	t _{OFF}	Output buffer turn-off delay	0	13	0	15	ns	12
26	t _{OEZ}	Output turn-off delay from $\overline{\text{OE}}$	0	13	0	15	ns	12
27	t _{DZC}	Data to $\overline{\text{CAS}}$ low delay	0	–	0	–	ns	13
28	t _{DZO}	Data to $\overline{\text{OE}}$ low delay	0	–	0	–	ns	13
29	t _{CDD}	$\overline{\text{CAS}}$ high to data delay	13	–	15	–	ns	14
30	t _{ODD}	$\overline{\text{OE}}$ high to data delay	13	–	15	–	ns	14

AC Characteristics^(5,6) $T_A = 0 \text{ to } 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $t_T = 2 \text{ ns}$

#	Symbol	Parameter	-50		-60		Unit	Note
			min.	max.	min.	max.		
Write Cycle								
31	t _{WCH}	Write command hold time	8	–	10	–	ns	
32	t _{WP}	Write command pulse width	8	–	10	–	ns	
33	t _{WCS}	Write command setup time	0	–	0	–	ns	15
34	t _{RWL}	Write command to $\overline{\text{RAS}}$ lead time	13	–	15	–	ns	
35	t _{CWL}	Write command to $\overline{\text{CAS}}$ lead time	13	–	15	–	ns	
36	t _{DS}	Data setup time	0	–	0	–	ns	16
37	t _{DH}	Data hold time	8	–	10	–	ns	16
Read-modify-Write Cycle								
38	t _{RWC}	Read-write cycle time	126	–	150	–	ns	
39	t _{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	68	–	80	–	ns	15
40	t _{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	31	–	35	–	ns	15
41	t _{AWD}	Column address to $\overline{\text{WE}}$ delay time	43	–	50	–	ns	15
42	t _{OEH}	$\overline{\text{OE}}$ command hold time	13	–	15	–	ns	
Fast Page Mode Cycle								
43	t _{PC}	Fast Page mode cycle time	35	–	40	–	ns	
44	t _{CP}	$\overline{\text{CAS}}$ precharge time	10	–	10	–	ns	
45	t _{CPA}	Access time from $\overline{\text{CAS}}$ precharge	–	30	–	35	ns	7
46	t _{RASP}	$\overline{\text{RAS}}$ pulse width in Fast mode	50	200k	60	200k	ns	
47	t _{RHPC}	$\overline{\text{CAS}}$ precharge to $\overline{\text{RAS}}$ Delay	30	–	35	–	ns	
Fast Page Mode Read-modify-Write Cycle								
48	t _{PRWC}	Fast Page mode read-write cycle time	71	–	80	–	ns	
49	t _{CPWD}	$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$	48	–	55	–	ns	
CAS-before-RAS Refresh Cycle								
50	t _{CSR}	$\overline{\text{CAS}}$ setup time	10	–	10	–	ns	
51	t _{CHR}	$\overline{\text{CAS}}$ hold time	10	–	10	–	ns	
52	t _{RPC}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	5	–	5	–	ns	
53	t _{WRP}	Write to $\overline{\text{RAS}}$ precharge time	10	–	10	–	ns	
54	t _{WRH}	Write hold time referenced to $\overline{\text{RAS}}$	10	–	10	–	ns	
CAS-before-RAS Counter Test Cycle								
55	t _{CPT}	$\overline{\text{CAS}}$ precharge time	35	–	40	–	ns	

AC Characteristics^(5,6)

$T_A = 0 \text{ to } 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $t_T = 2 \text{ ns}$

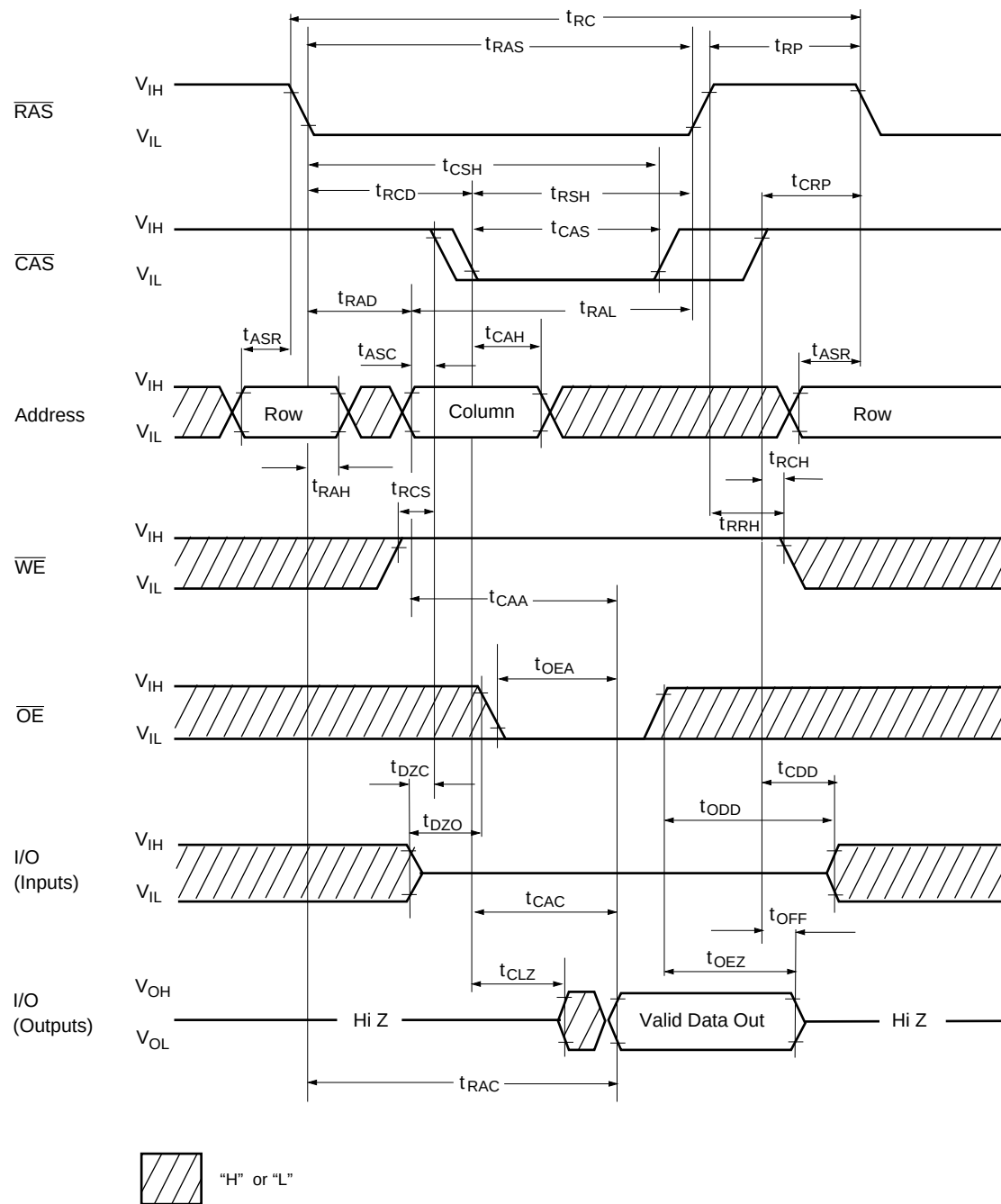
#	Symbol	Parameter	-50		-60		Unit	Note
			min.	max.	min.	max.		
Test Mode								
56	t _{WTS}	Write command setup time	10	–	10	–	ns	
57	t _{WTH}	Write command hold time	10	–	10	–	ns	
58	t _{CHRT}	$\overline{\text{CAS}}$ hold time	30	–	30	–	ns	
59	t _{RAHT}	$\overline{\text{RAS}}$ hold time in test mode	30	–	30	–	ns	
Self Refresh Cycle								
60	t _{RASS}	$\overline{\text{RAS}}$ pulse width	100k	–	100k	–	ns	17
61	t _{RPS}	$\overline{\text{RAS}}$ precharge time	95	–	110	–	ns	17
62	t _{CHS}	$\overline{\text{CAS}}$ hold time	-50	–	-50	–	ns	17

Notes:

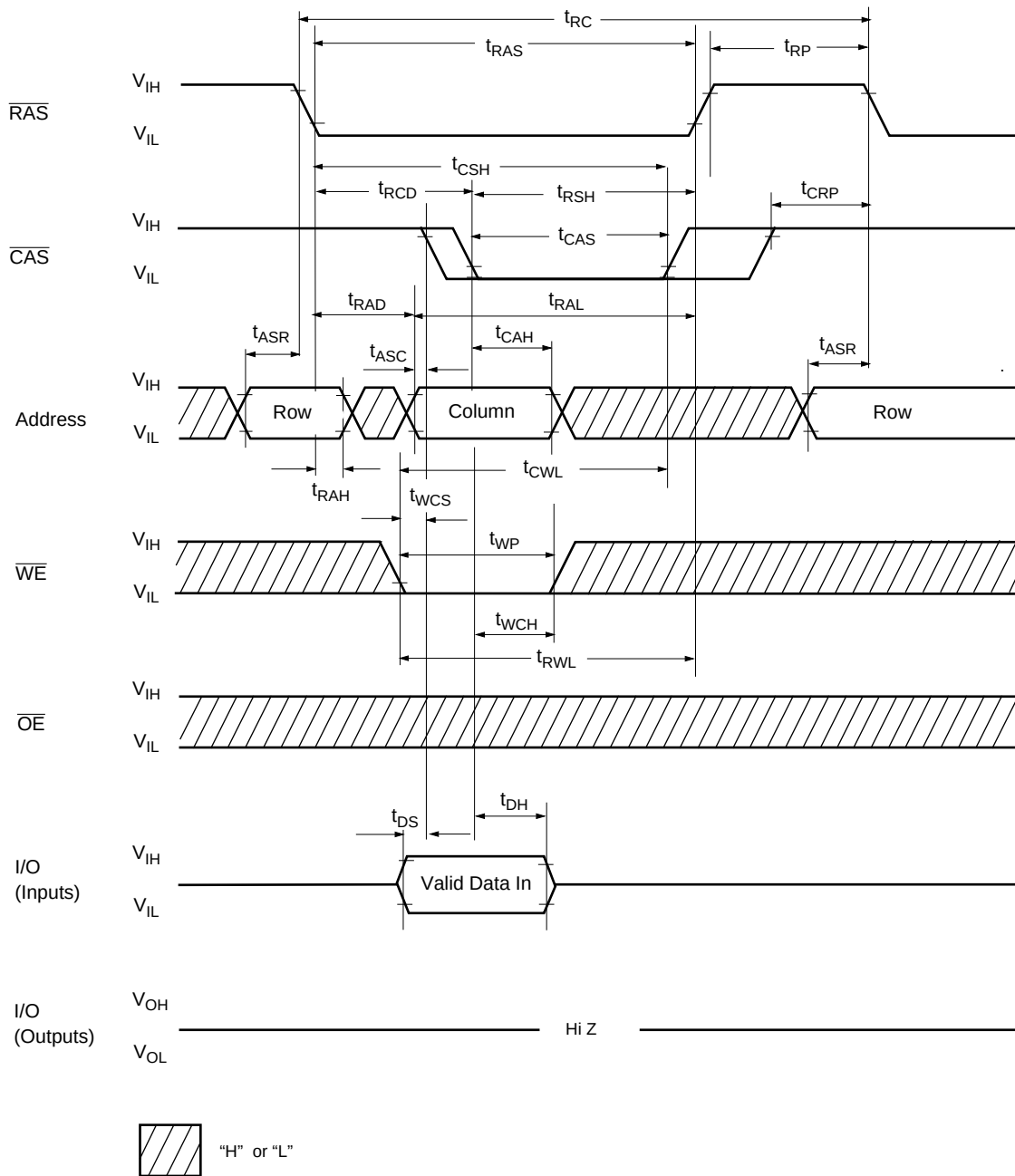
- 1) All voltages are referenced to V_{SS} .
- 2) I_{CC1} , I_{CC3} , I_{CC4} and I_{CC5} depend on cycle rate.
- 3) I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
- 4) Address can be changed once or less while $\overline{RAS} = V_{IL}$. In case of I_{CC4} it can be changed once or less during a Fast Page mode cycle
- 5) An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{CAS}$ -before- $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
- 6) AC measurements assume $t_T = 2$ ns.
- 7) $V_{IH (min.)}$ and $V_{IL (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL} .
- 8) Measured with the specified current load and 100 pF at $V_{OL} = 0.8$ V and $V_{OH} = 2.0$ V. Access time is determined by the latter of t_{RAC} , t_{CAC} , t_{CAA} , t_{CPA} , t_{OEA} . t_{CAC} is measured from tristate.
- 9) Operation within the $t_{RCD (max.)}$ limit ensures that $t_{RAC (max.)}$ can be met. $t_{RCD (max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD (max.)}$ limit, then access time is controlled by t_{CAC} .
- 10) Operation within the $t_{RAD (max.)}$ limit ensures that $t_{RAC (max.)}$ can be met. $t_{RAD (max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD (max.)}$ limit, then access time is controlled by t_{CAA} .
- 11) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- 12) $t_{OFF (max.)}$, $t_{OEZ (max.)}$ define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels. t_{OFF} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.
- 13) Either t_{DZC} or t_{DZO} must be satisfied.
- 14) Either t_{CDD} or t_{ODD} must be satisfied.
- 15) t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS (min.)}$, the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD (min.)}$, $t_{CWD} > t_{CWD (min.)}$ and $t_{AWD} > t_{AWD (min.)}$, the cycle is a read-write cycle and I/O will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.
- 16) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
- 17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

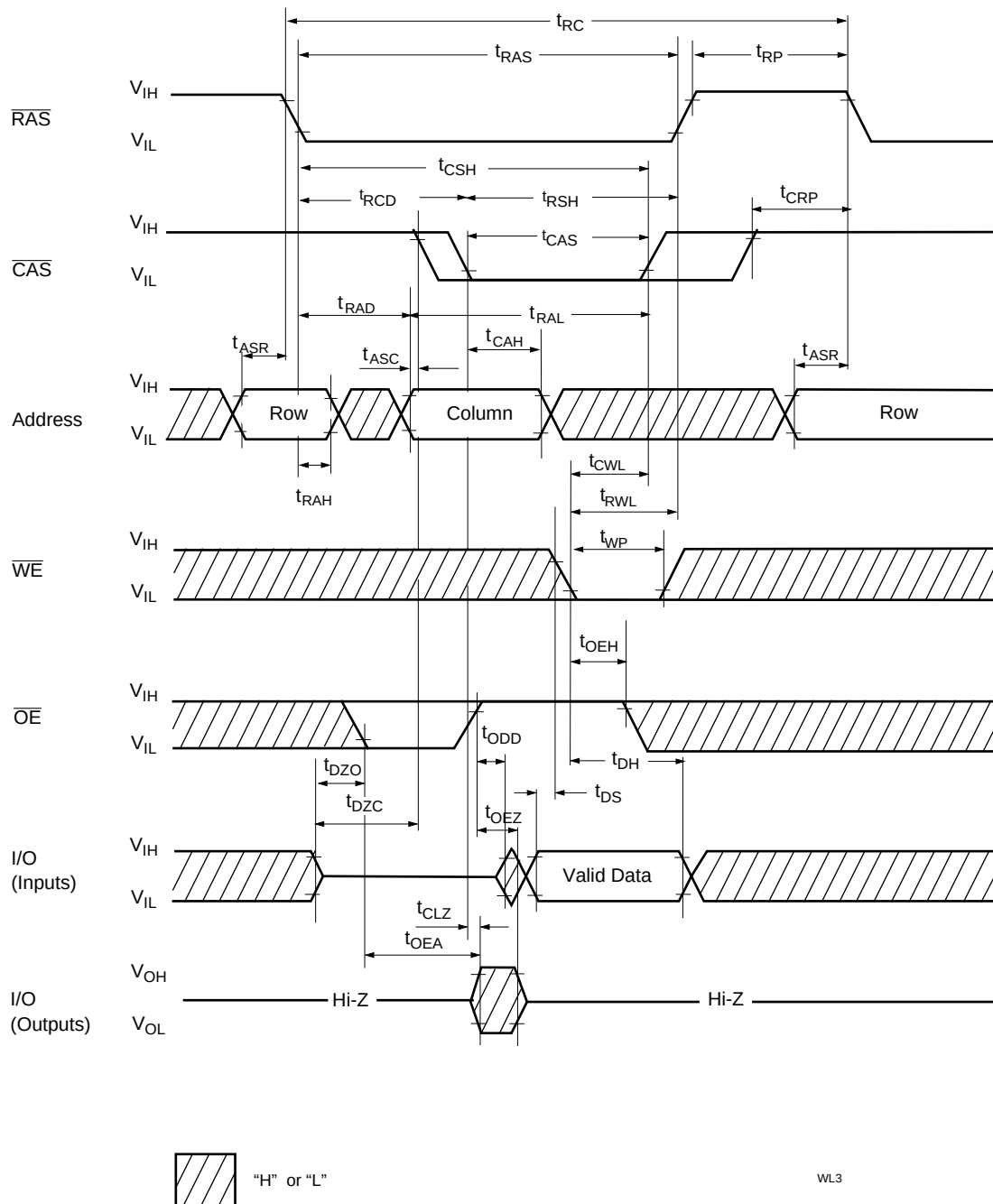
If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.

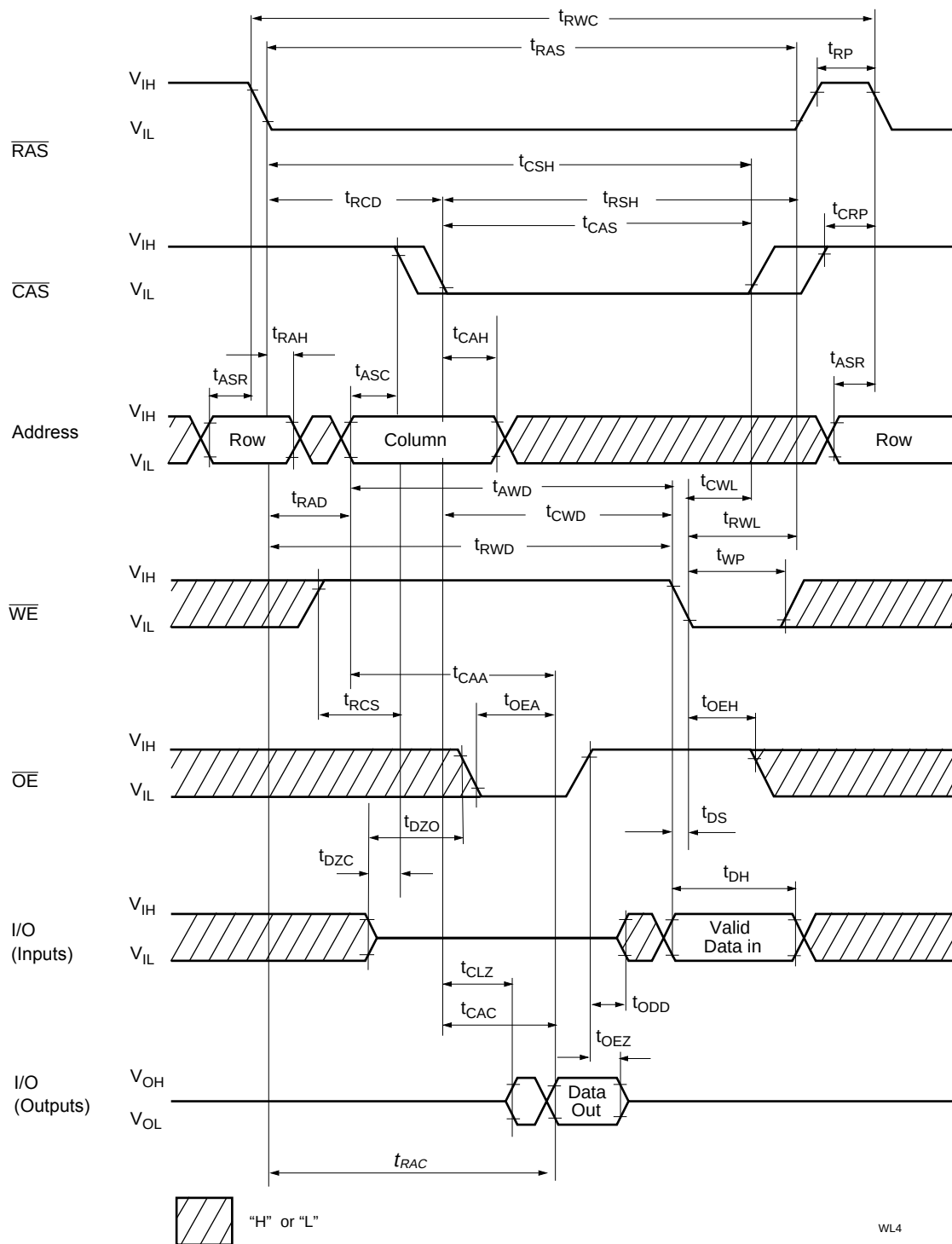
Waveforms of Read Cycle

WL1

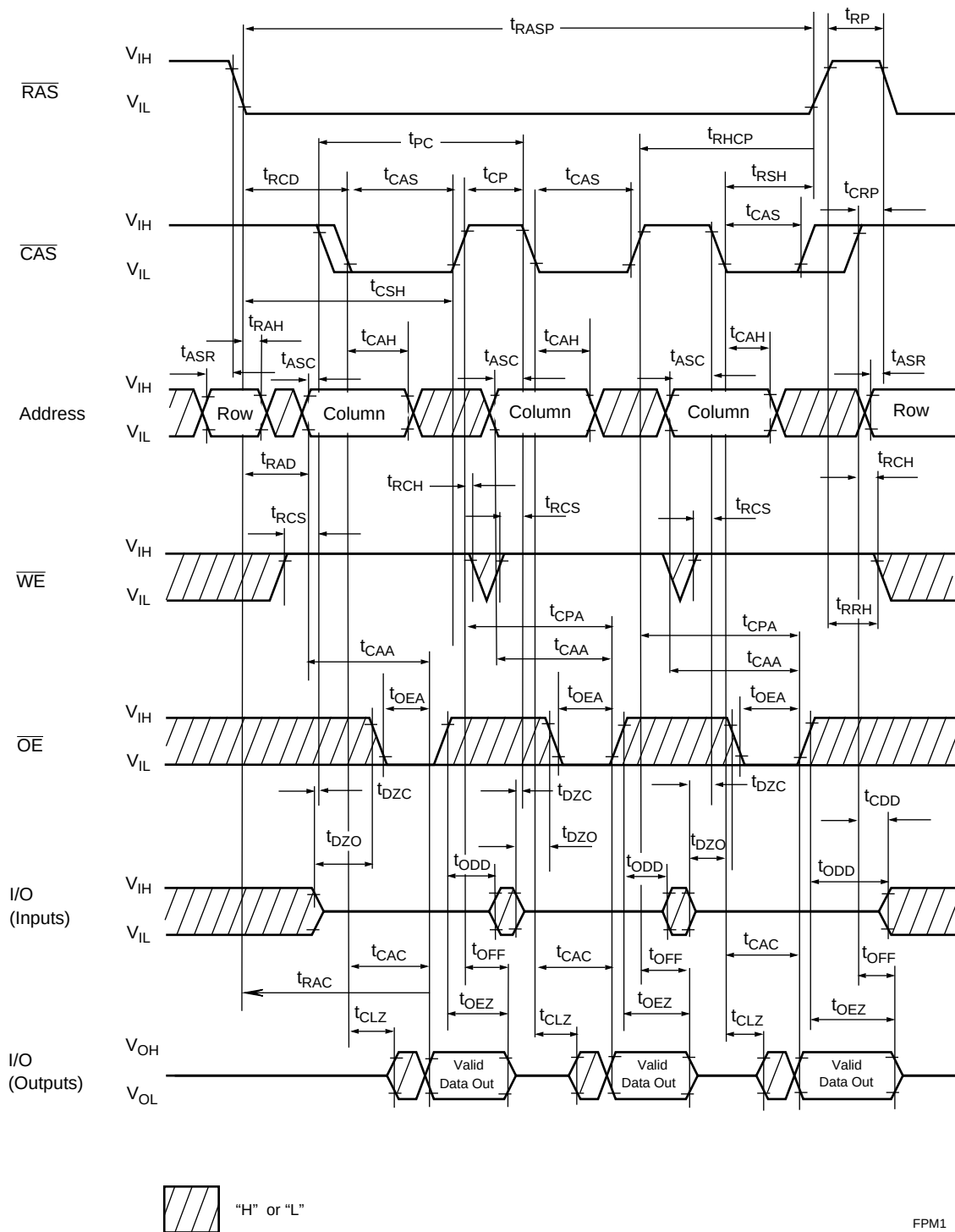
Waveforms of Write Cycle (Early Write)

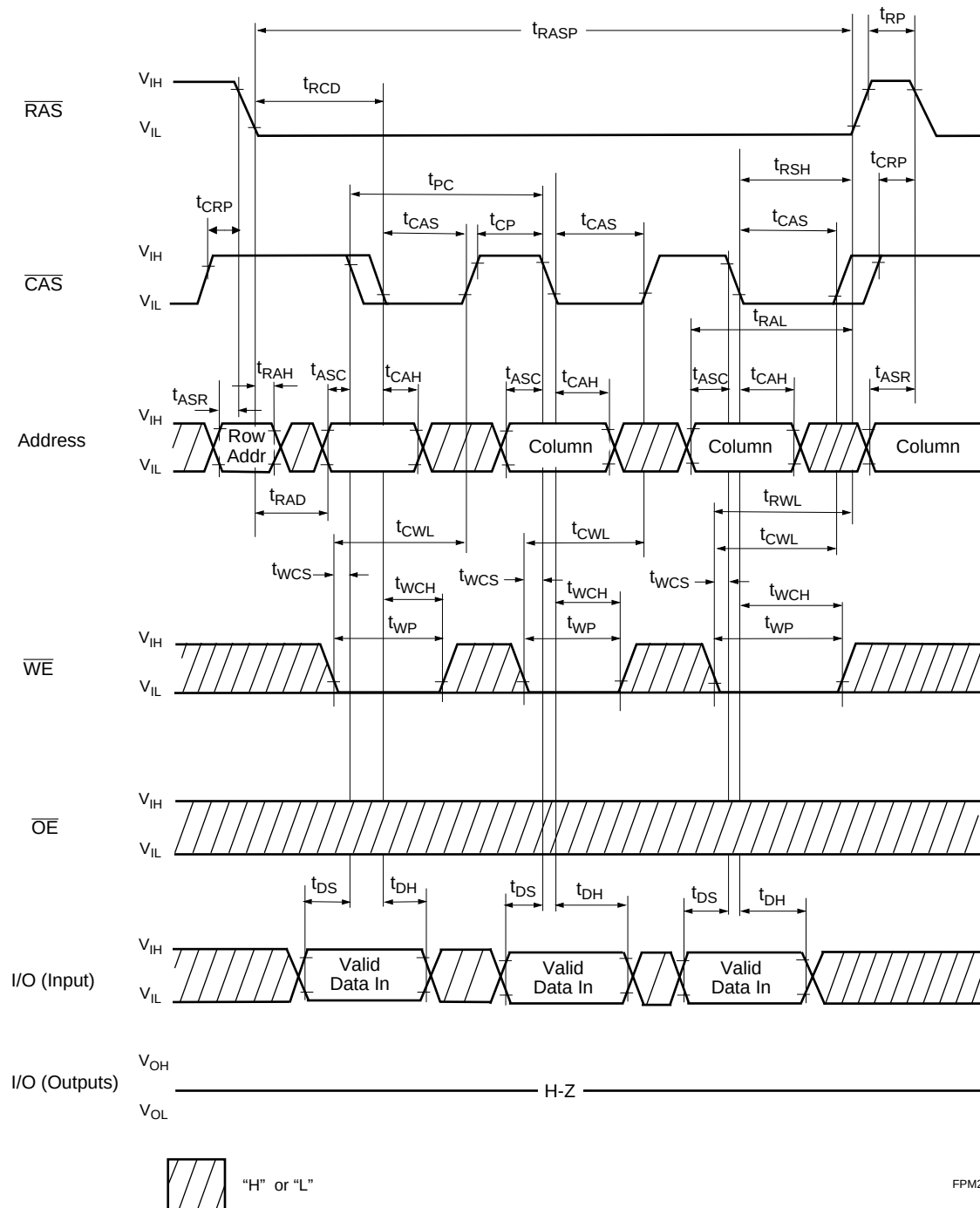
WL2

Waveforms of Write Cycle ($\overline{\text{OE}}$ Controlled Write)

Waveforms of Read-Write (Read-Modify-Write) Cycle

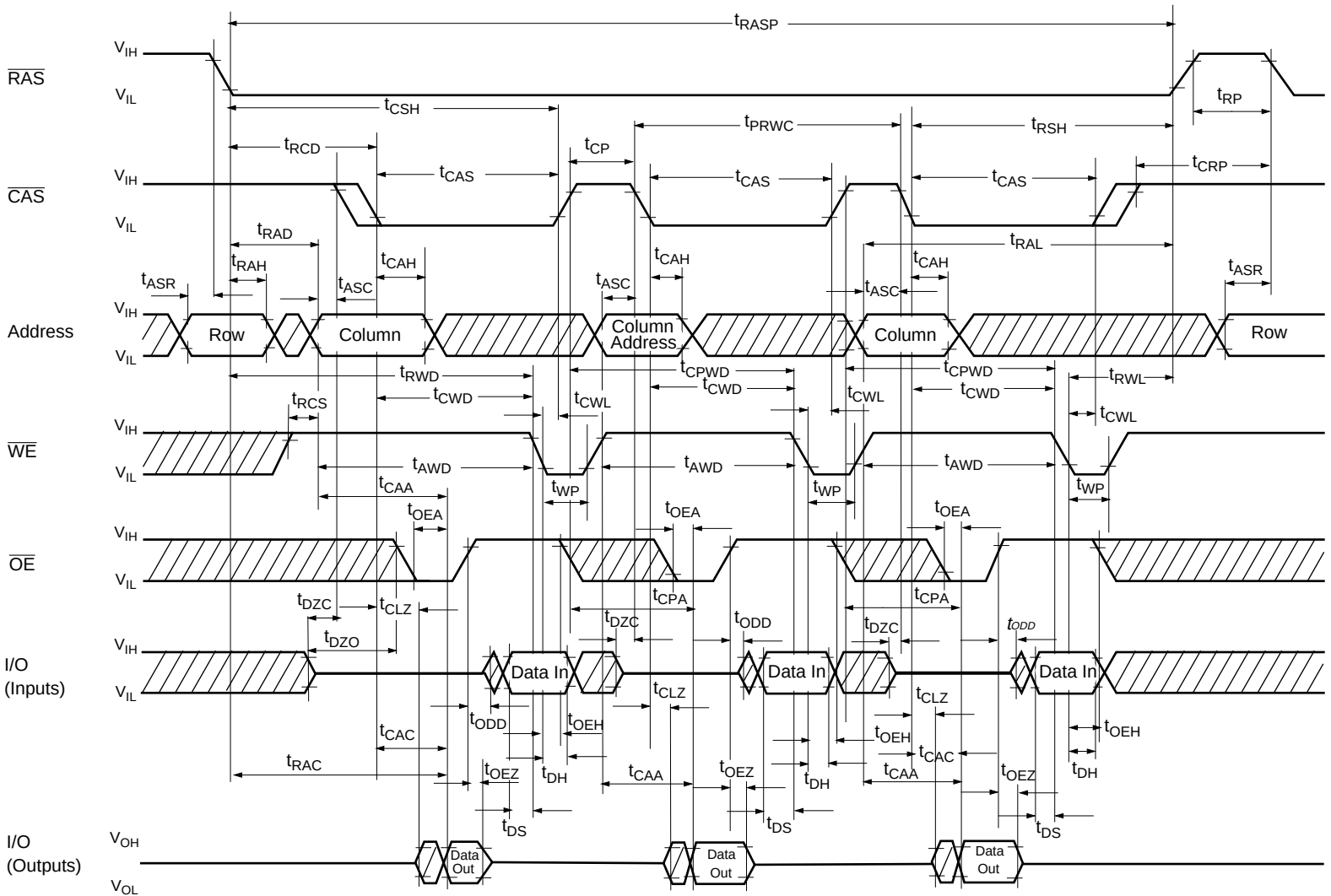
WL4

Waveforms of Fast Page Mode Read Cycle

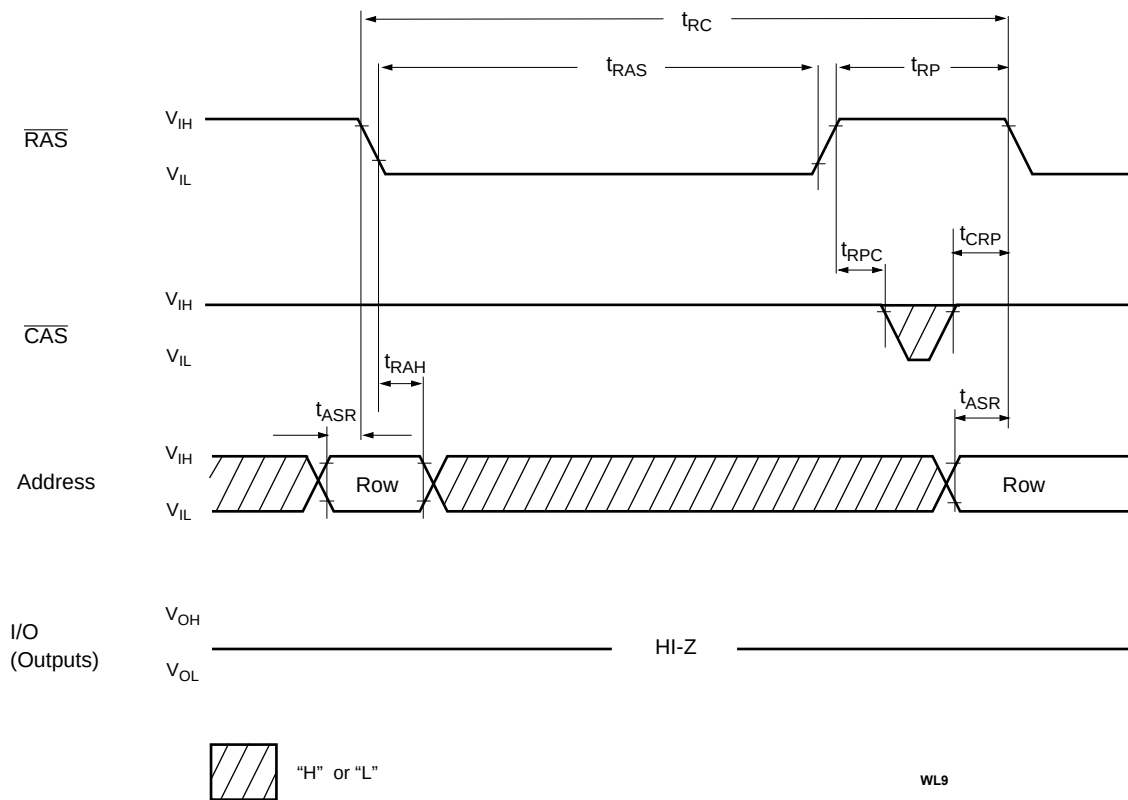
Waveforms of Fast Page Mode Early Write Cycle

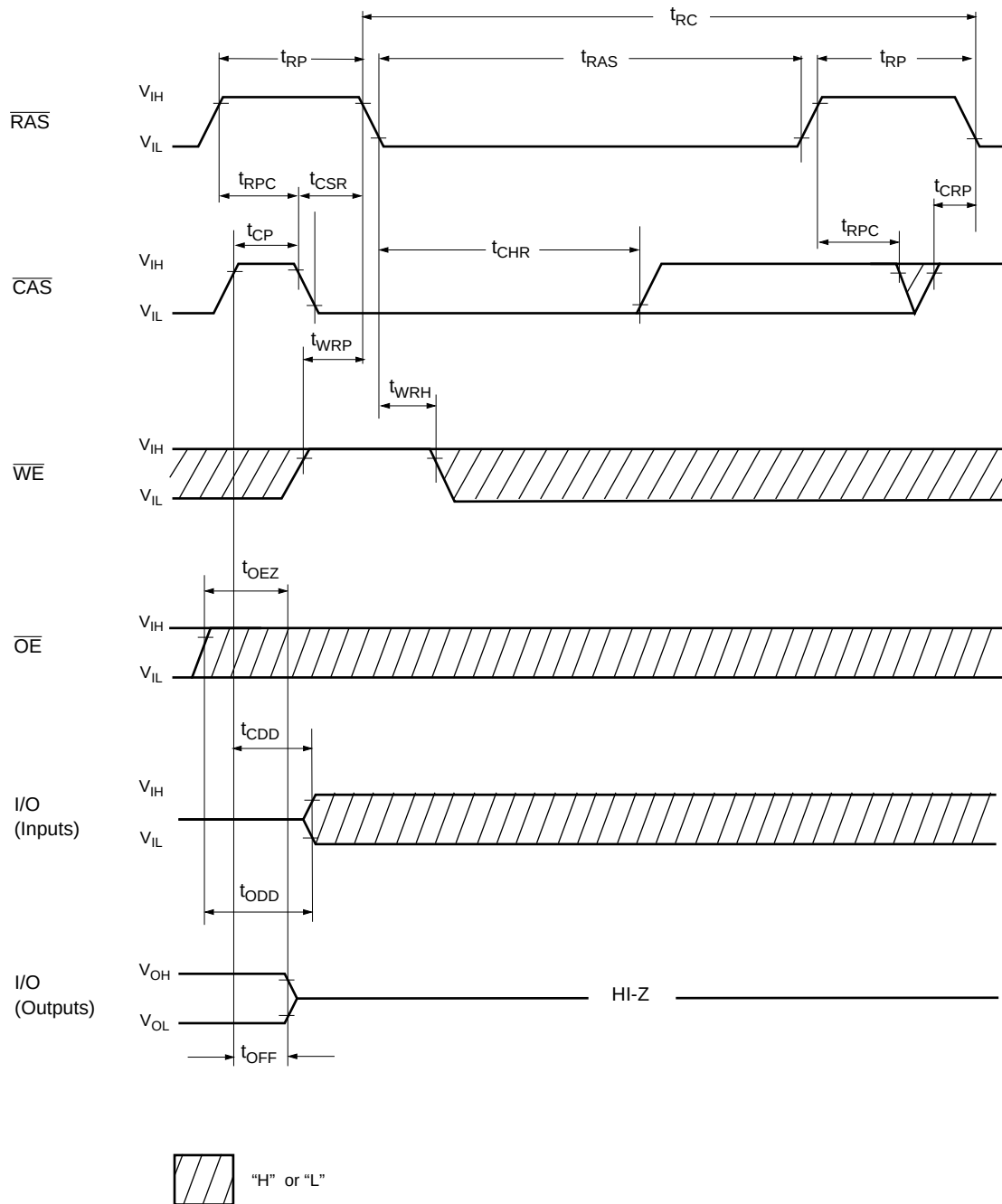
FPM2

Waveforms of Fast Page Mode Late Write and Read-Modify-Write Cycle

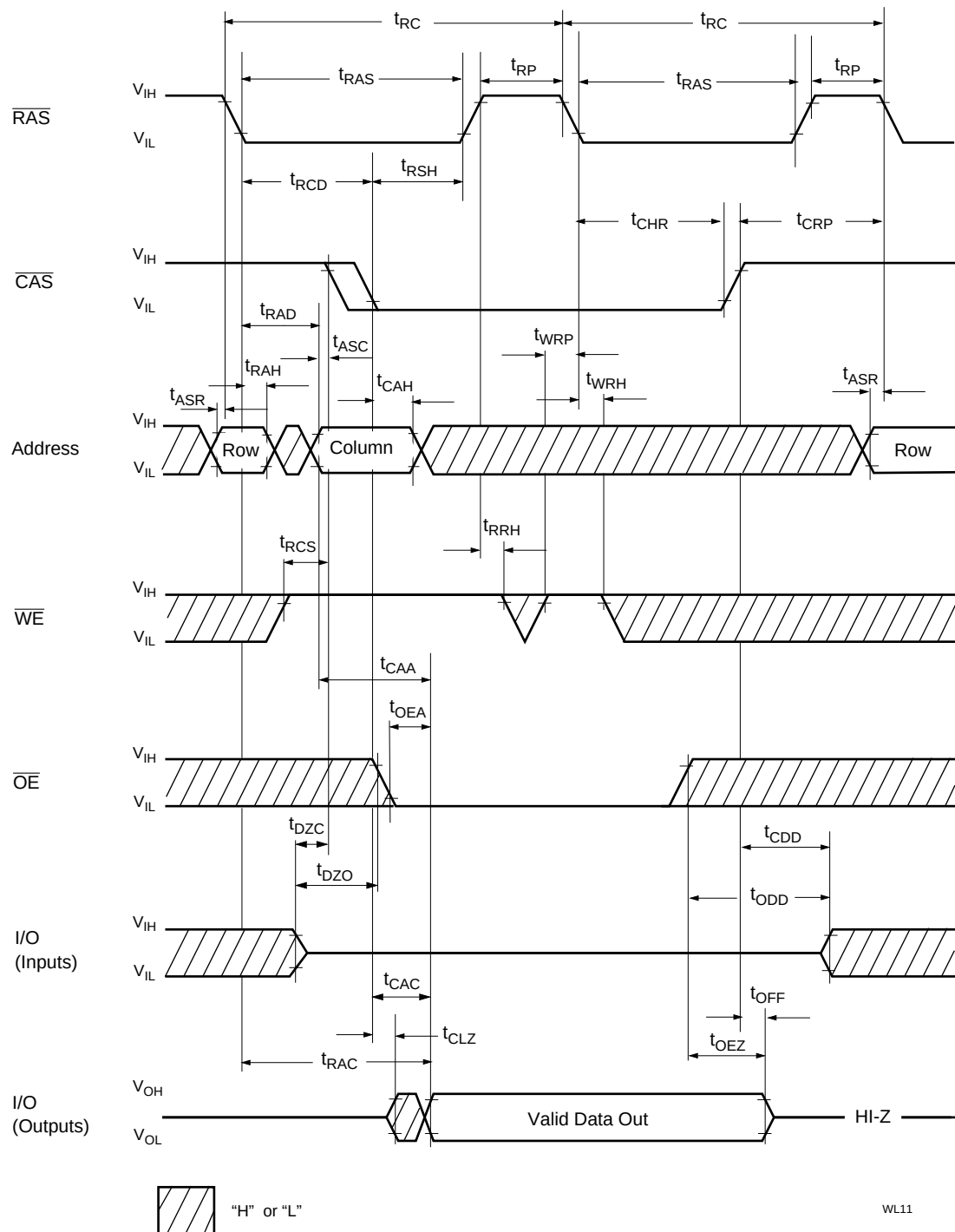


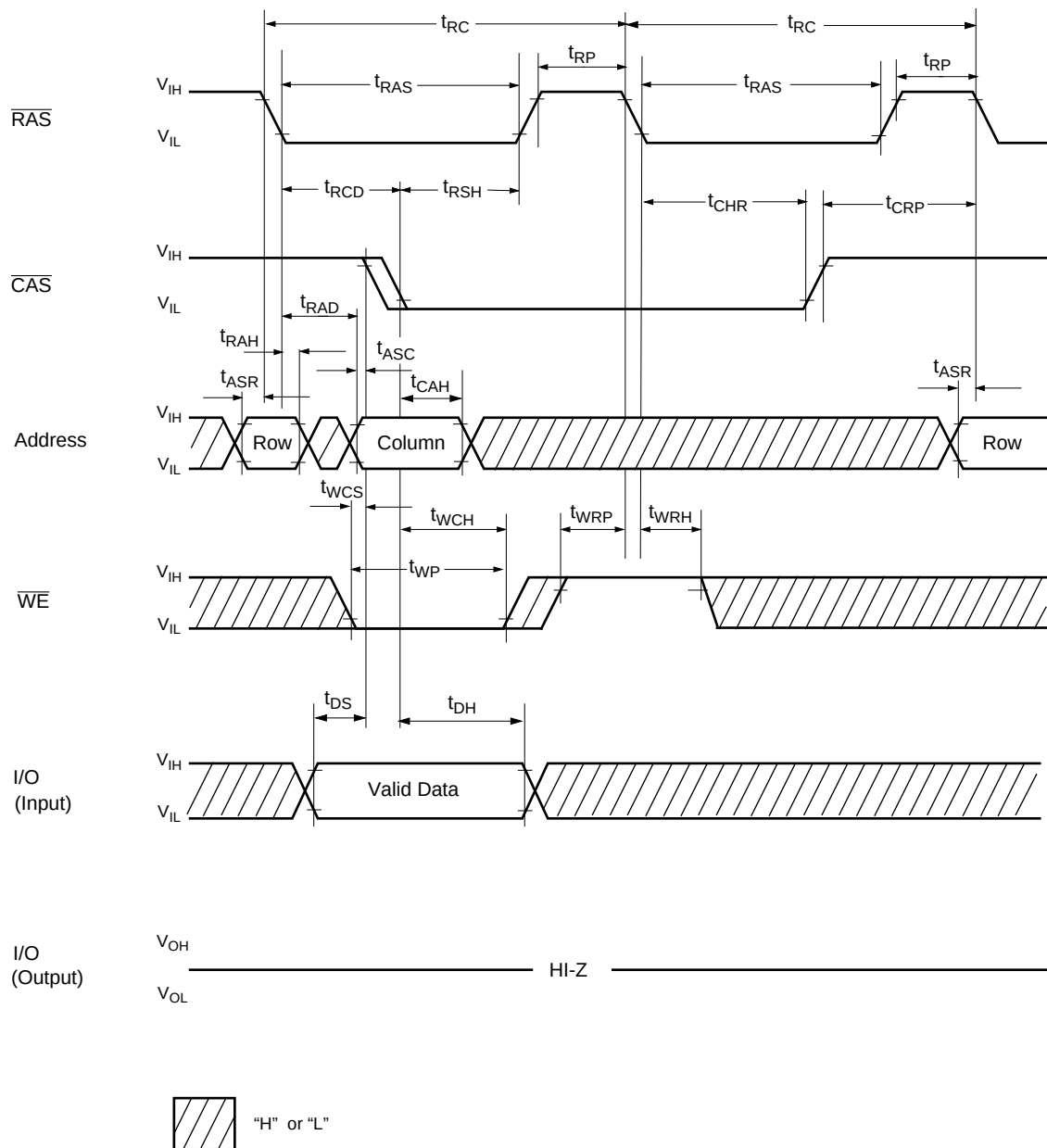
WL17

Waveforms of $\overline{\text{RAS}}$ Only Refresh Cycle

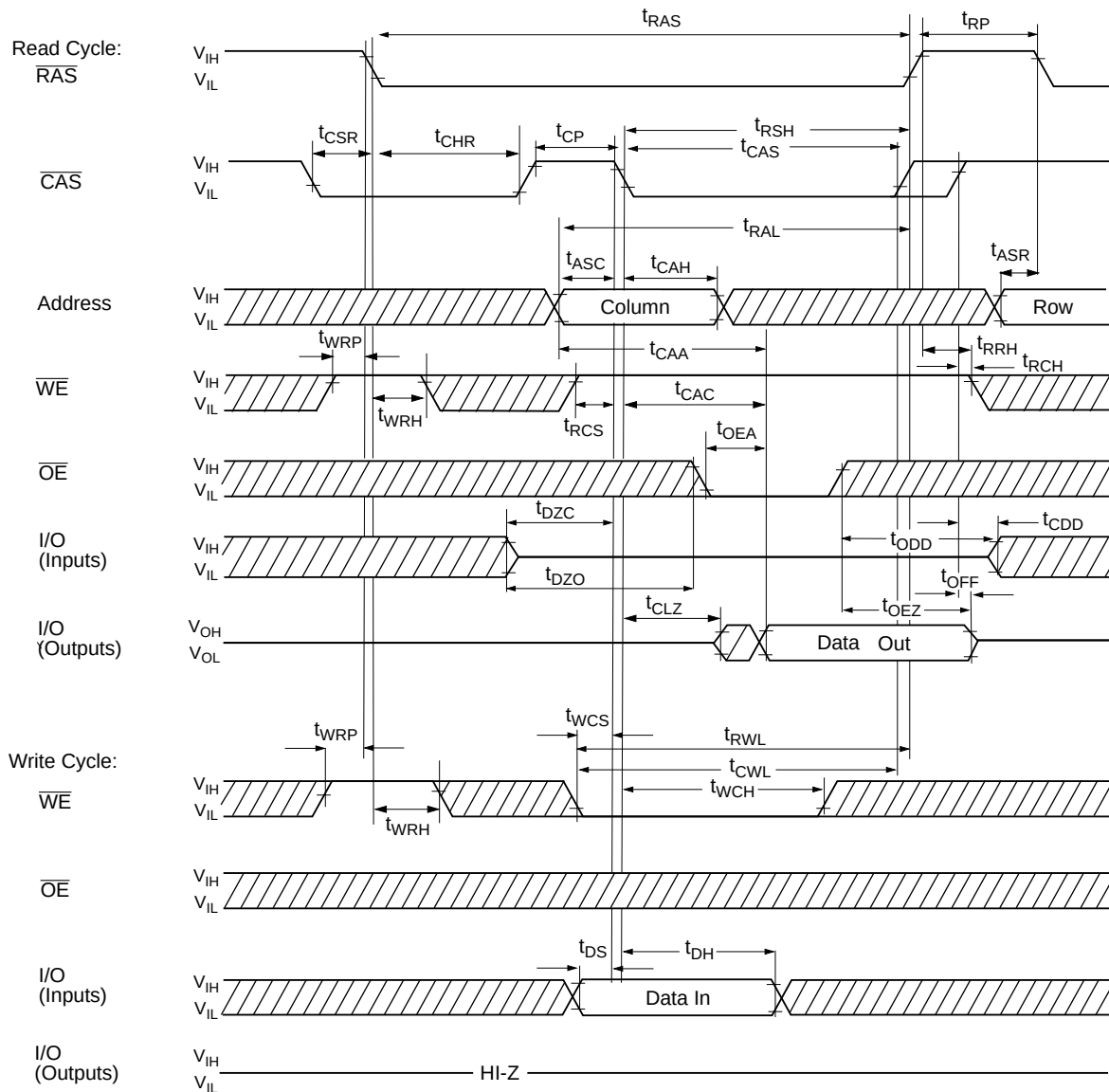
Waveforms of $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle

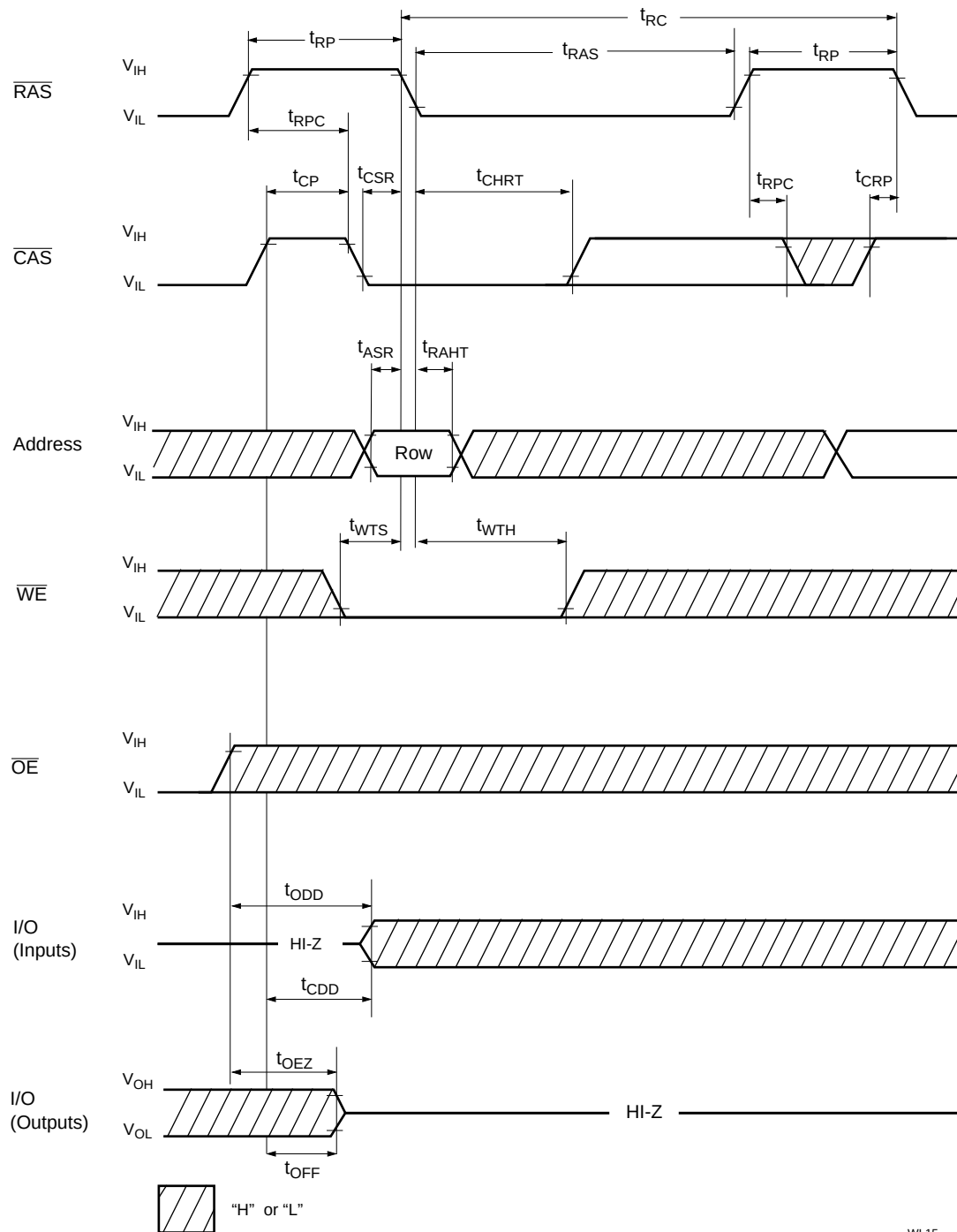
WL10

Waveforms of Hidden Refresh Read Cycle

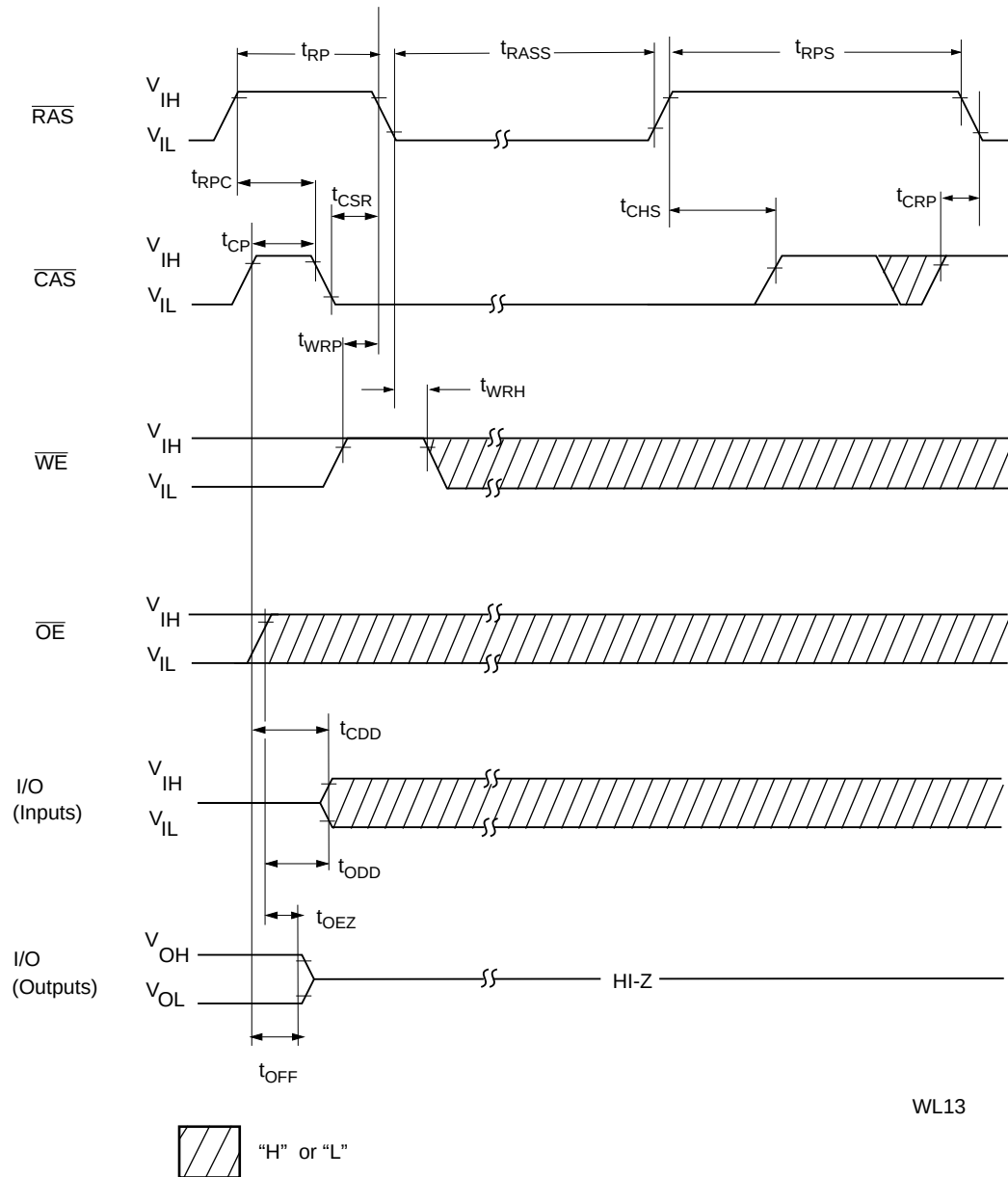
Waveforms of Hidden Refresh Early Write Cycle

WL12

Waveforms of $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Counter Test Cycle

Waveforms of Test Mode Entry

WL15

Waveforms of CAS-before-RAS Self Refresh Cycle

WL13

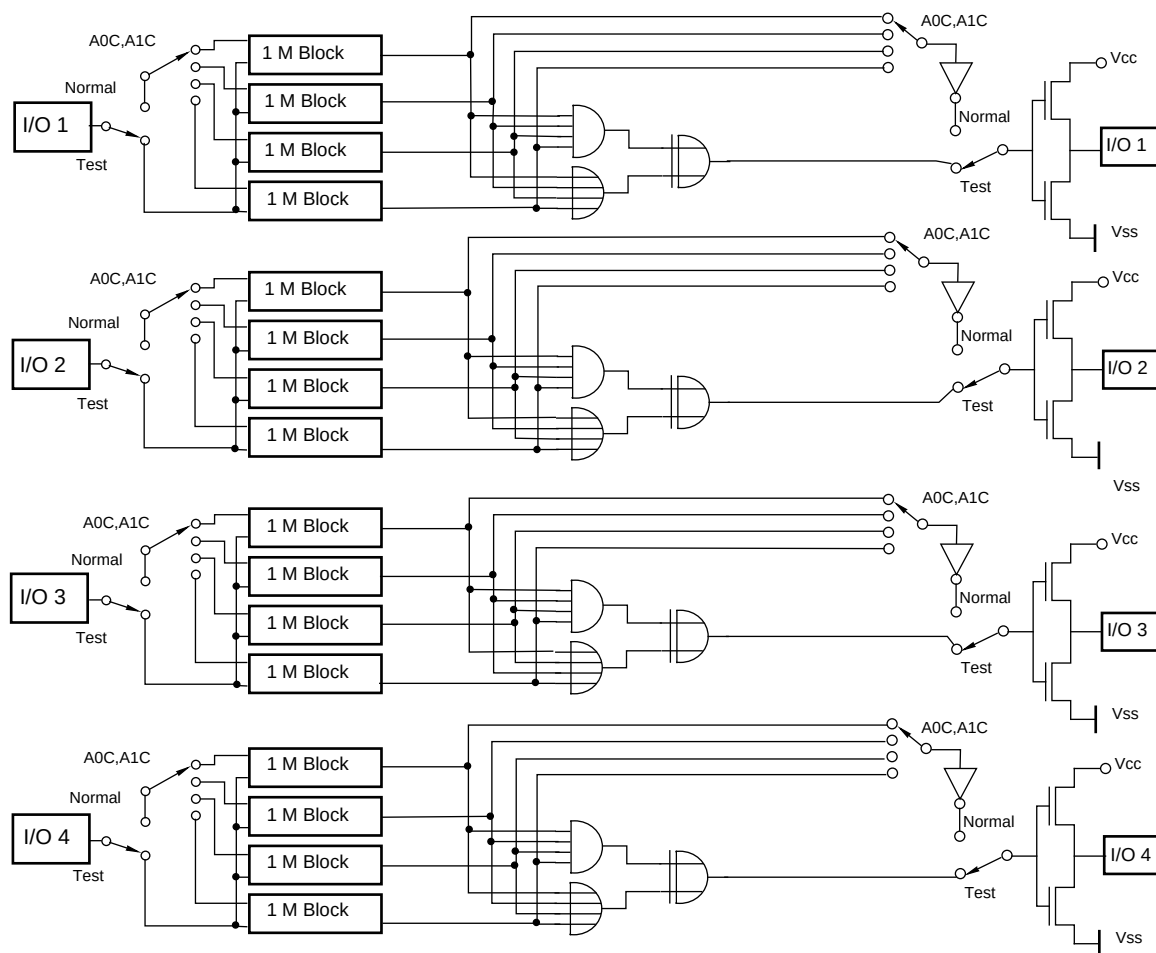
Test Mode

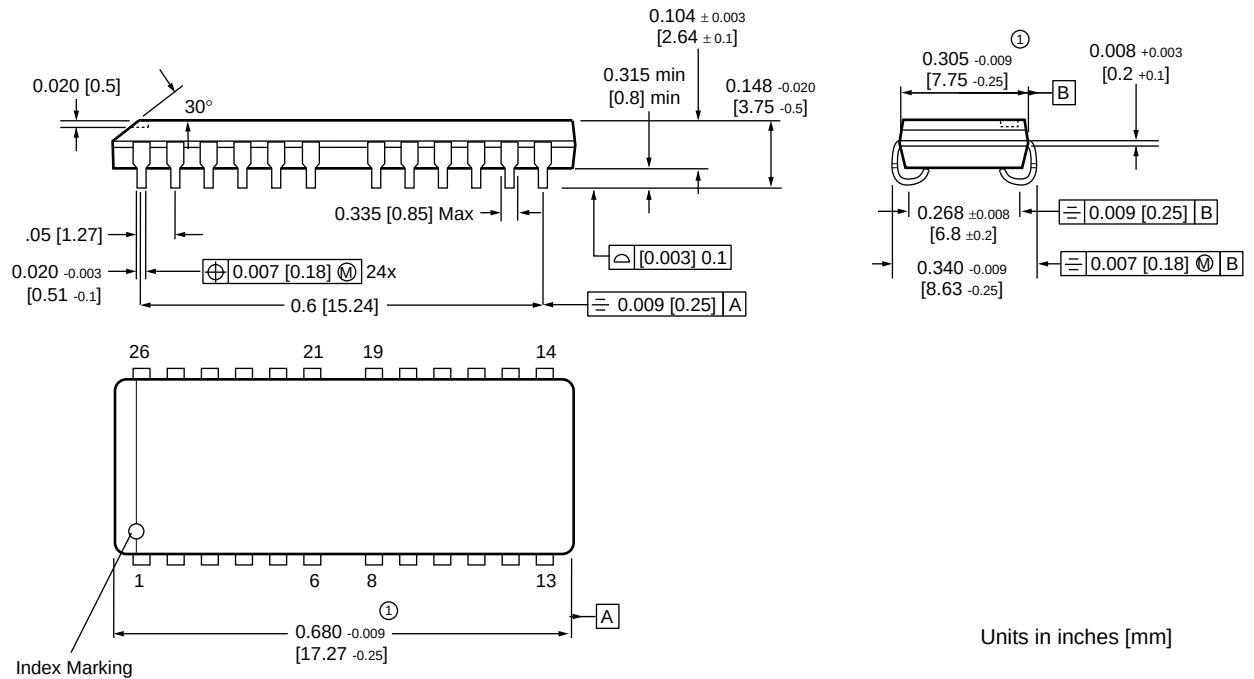
As the V53C517400A is organized internally as 1M x 16-bits, a test mode cycle using 4:1 compression can be used to improve test time. Note that in the 4M x 4 version the test time is reduced by 1/4 for a N test pattern.

In a test mode "write" the data from each I/O pin is written into four 1M blocks simultaneously (all "1" s or all "0" s). In test mode "read" each I/O output is used for indicating the test mode result. If the internal four bits are equal, the I/O would indicate a "1". If

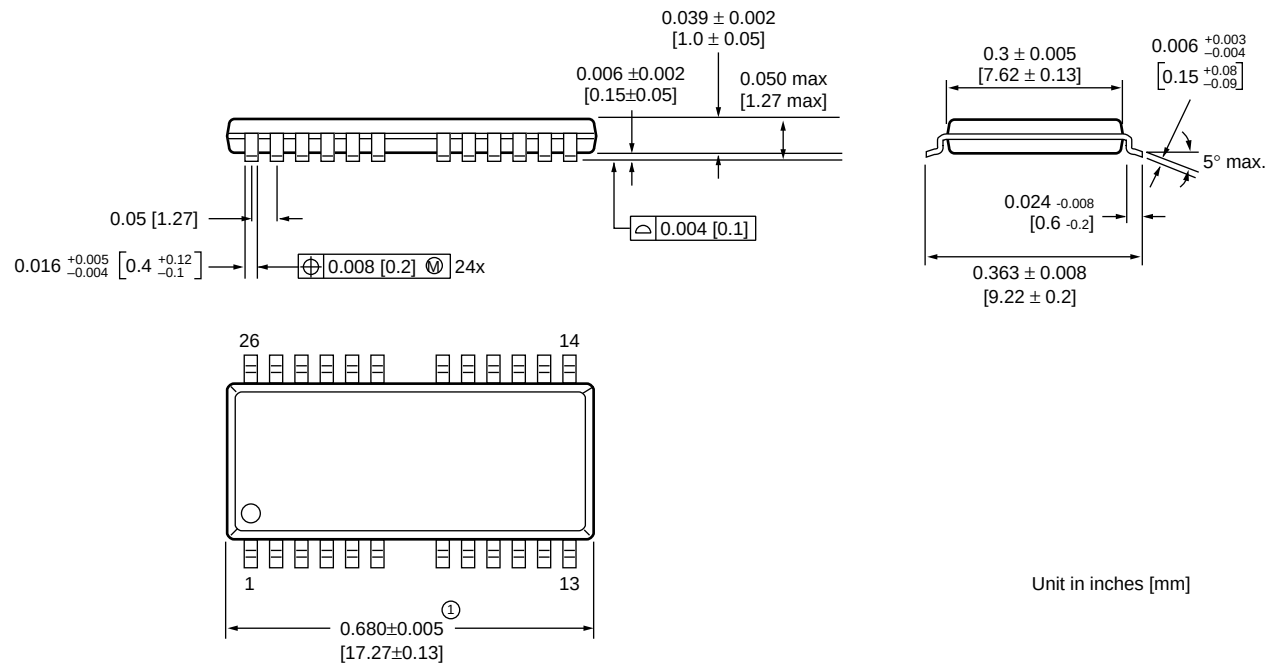
they were not equal, the I/O would indicate a "0". The WCBR cycle (WE, CAS before RAS) puts the device into test mode. To exit from test mode, a "CAS before RAS refresh", "RAS only refresh" or "Hidden refresh" can be used. Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles.

Row addresses A0 through A9 have to be kept high to perform a testmode entry cycle. All other addresses are don't care.

Block Diagram in Test Mode

Package Diagrams**24/26-pin 300 mil SOJ**

① Does not include plastic or metal protrusion of 0.15 max. per side

24/26-pin 300 mil TSOP-II

① Does not include plastic or metal protrusion of 0.15 max. per side

Notes

Notes

Notes

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