

**512K X 16 FAST PAGE MODE  
CMOS DYNAMIC RAM**

<b>HIGH PERFORMANCE</b>	<b>40</b>	<b>45</b>	<b>50</b>	<b>60</b>
Max. $\overline{\text{RAS}}$ Access Time, ( $t_{\text{RAC}}$ )	40 ns	45 ns	50 ns	60 ns
Max. Column Address Access Time, ( $t_{\text{CAA}}$ )	20 ns	22 ns	24 ns	30 ns
Min. Fast Page Mode Cycle Time, ( $t_{\text{PC}}$ )	23 ns	25 ns	28 ns	35 ns
Min. Read/Write Cycle Time, ( $t_{\text{RC}}$ )	75 ns	80 ns	90 ns	110 ns

**Features**

- 512K x 16-bit organization
- $\overline{\text{RAS}}$  access time: 40, 45, 50, 60 ns
- Fast Page Mode for a sustained data rate of 43 MHz
- Dual  $\overline{\text{CAS}}$  Inputs
- Pin-to-Pin compatible with 256Kx16
- Low power dissipation
- Read-Modify-Write,  $\overline{\text{RAS}}$ -Only Refresh,  $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$  Refresh
- Refresh Interval: 512 cycles/8 ms
- Available in 40-pin 400 mil SOJ
- Single +5V Power Supply
- TTL Interface

**Description**

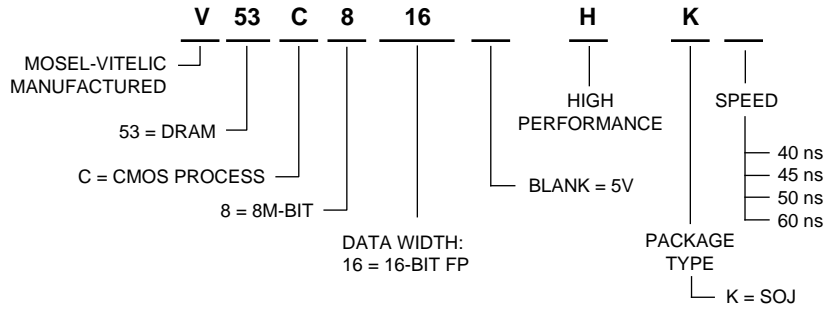
The V53C816H is a 524,288 x 16 bit high-performance CMOS dynamic random access memory. The V53C816H offers Fast Page mode with dual  $\overline{\text{CAS}}$  inputs. An address,  $\overline{\text{CAS}}$  and  $\overline{\text{RAS}}$  input capacitances are reduced to one half when the 256Kx16 DRAM is used to construct the same memory density. The V53C816H has asymmetric address, 10-bit row and 9-bit column.

All inputs are TTL compatible. Fast Page Mode operation allows random access up to 512K x 16 bits, within a page, with cycle times as short as 23ns.

The V53C816H is best suited for graphics, and buffer memory applications.

**Device Usage Chart**

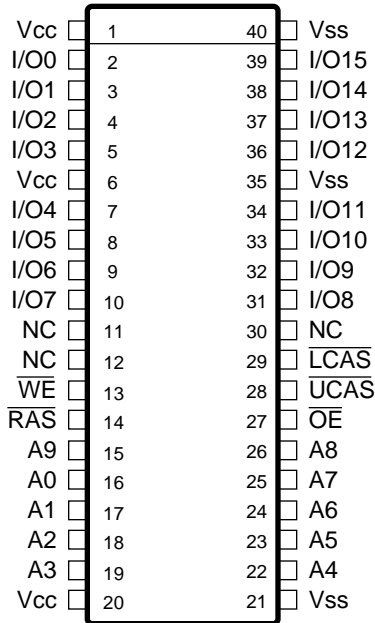
Operating Temperature Range	Package Outline	Access Time (ns)				Power	Temperature Mark
	K	40	45	50	60	Std.	
0°C to 70 °C	•	•	•	•	•	•	Blank



Description	Pkg.	Pin Count
SOJ	K	40

816H-01

**40-Pin SOJ  
PIN CONFIGURATION  
Top View**



816H-02

**Pin Names**

A <sub>0</sub> -A <sub>9</sub>	Address Inputs, A <sub>9</sub> is effective with $\overline{\text{RAS}}$
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{UCAS}}$	Column Address Strobe Upper Byte Control
$\overline{\text{LCAS}}$	Column Address Strobe Lower Byte Control
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
I/O <sub>0</sub> -I/O <sub>15</sub>	Data Input, Output
V <sub>CC</sub>	+5V Supply
V <sub>SS</sub>	0V Supply
NC	No Connect

**Absolute Maximum Ratings\***

Ambient Temperature  
 Under Bias ..... -10°C to +80°C  
 Storage Temperature (plastic)..... -55°C to +125°C  
 Voltage Relative to V<sub>SS</sub> ..... -1.0 V to +7.0 V  
 Data Output Current ..... 50 mA  
 Power Dissipation..... 1.4 W

\*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

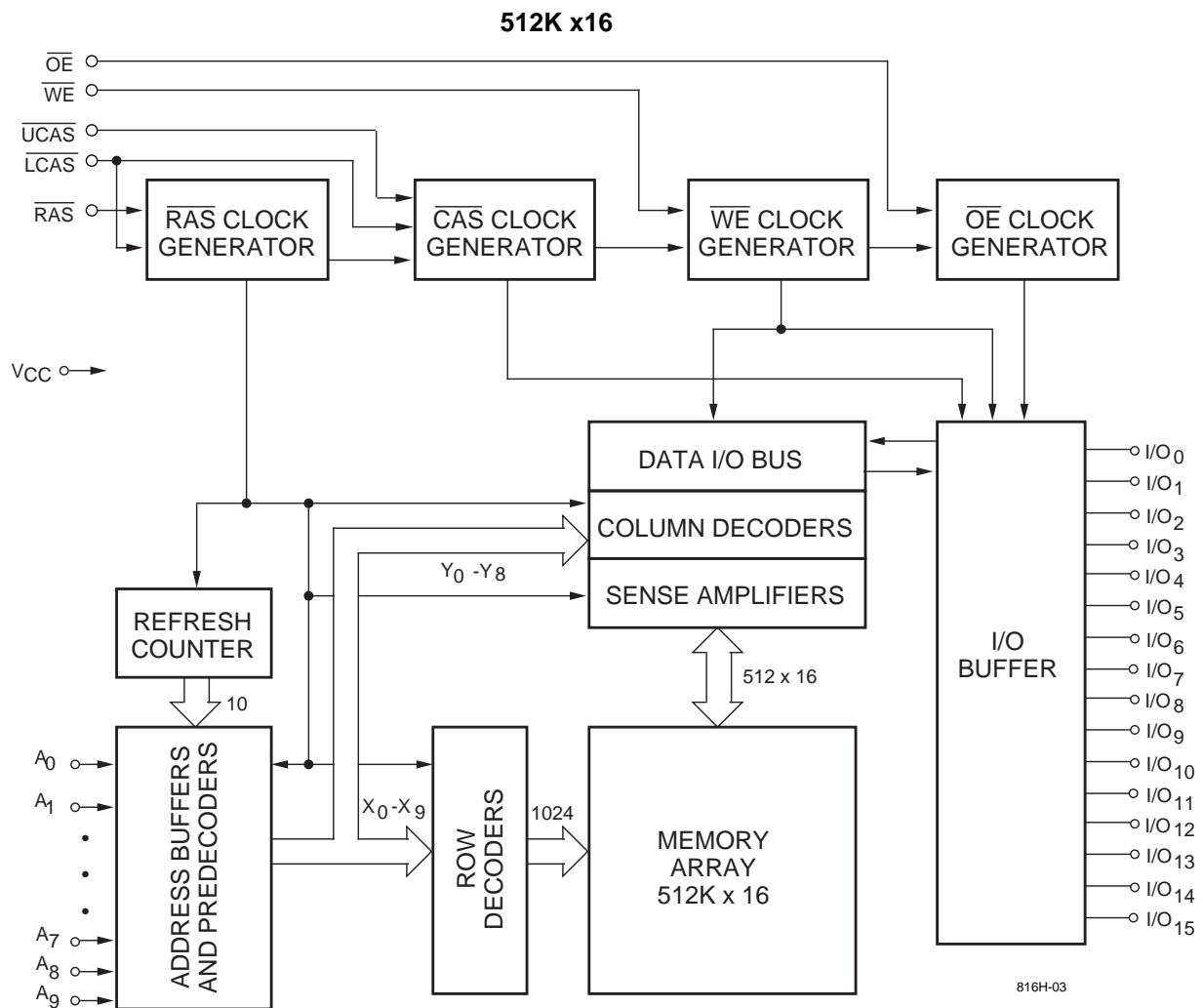
**Capacitance\***

T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5 V ± 10%, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Unit
C <sub>IN1</sub>	Address Input	3	4	pF
C <sub>IN2</sub>	RAS, CAS, WE, OE	4	5	pF
C <sub>OUT</sub>	Data Input/Output	5	7	pF

\* Note: Capacitance is sampled and not 100% tested

**Block Diagram**



**DC and Operating Characteristics (1-2)**

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 5\%$ ,  $V_{SS} = 0\text{ V}$ , unless otherwise specified.

Symbol	Parameter	Access Time	V53C816H			Unit	Test Conditions	Notes
			Min.	Typ.	Max.			
$I_{LI}$	Input Leakage Current (any input pin)		-10		10	$\mu\text{A}$	$V_{SS} \leq V_{IN} \leq V_{CC}$	
$I_{LO}$	Output Leakage Current (for High-Z State)		-10		10	$\mu\text{A}$	$V_{SS} \leq V_{OUT} \leq V_{CC}$ $\overline{\text{RAS}}, \overline{\text{CAS}}$ at $V_{IH}$	
$I_{CC1}$	$V_{CC}$ Supply Current, Operating	40			220	mA	$t_{RC} = t_{RC}(\text{min.})$	1, 2
		45			210			
		50			200			
		60			190			
$I_{CC2}$	$V_{CC}$ Supply Current, TTL Standby				4	mA	$\overline{\text{RAS}}, \overline{\text{CAS}}$ at $V_{IH}$ other inputs $\geq V_{SS}$	
$I_{CC3}$	$V_{CC}$ Supply Current, RAS-Only Refresh	40			220	mA	$t_{RC} = t_{RC}(\text{min.})$	2
		45			210			
		50			200			
		60			190			
$I_{CC4}$	$V_{CC}$ Supply Current, Fast Page Mode Operation	40			210	mA	Minimum Cycle	1, 2
		45			200			
		50			190			
		60			180			
$I_{CC5}$	$V_{CC}$ Supply Current, Standby, Output Enabled other inputs $\geq V_{SS}$				2.0	mA	$\overline{\text{RAS}} = V_{IH}, \overline{\text{CAS}} = V_{IL}$	1
$I_{CC6}$	$V_{CC}$ Supply Current, CMOS Standby				2.0	mA	$\overline{\text{RAS}} \geq V_{CC} - 0.2\text{ V},$ $\overline{\text{CAS}} \geq V_{CC} - 0.2\text{ V},$ All other inputs $\geq V_{SS}$	
$V_{CC}$	Supply Voltage		4.5	5.0	5.5	V		
$V_{IL}$	Input Low Voltage		-1		0.8	V		3
$V_{IH}$	Input High Voltage		2.4		$V_{CC} + 1$	V		3
$V_{OL}$	Output Low Voltage				0.4	V	$I_{OL} = 2.0\text{ mA}$	
$V_{OH}$	Output High Voltage		2.4			V	$I_{OH} = -2.0\text{ mA}$	

**AC Characteristics**

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$  unless otherwise noted

AC Test conditions, input pulse levels 0 to 3V

#	Symbol	Parameter	40		45		50		60		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	$t_{RAS}$	$\overline{RAS}$ Pulse Width	40	75	45	75K	50	75K	60	75K	ns	
2	$t_{RC}$	Read or Write Cycle Time	75		80		90		110		ns	
3	$t_{RP}$	$\overline{RAS}$ Precharge Time	25		25		30		40		ns	
4	$t_{CSH}$	$\overline{CAS}$ Hold Time	40		45		50		60		ns	
5	$t_{CAS}$	$\overline{CAS}$ Pulse Width	12		13		14		15		ns	
6	$t_{RCD}$	$\overline{RAS}$ to $\overline{CAS}$ Delay	17	28	18	32	19	36	20	45	ns	4
7	$t_{RCS}$	Read Command Setup Time	0		0		0		0		ns	
8	$t_{ASR}$	Row Address Setup Time	0		0		0		0		ns	
9	$t_{RAH}$	Row Address Hold Time	7		8		9		10		ns	
10	$t_{ASC}$	Column Address Setup Time	0		0		0		0		ns	
11	$t_{CAH}$	Column Address Hold Time	5		6		7		10		ns	
12	$t_{RSH (R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	12		13		14		15		ns	
13	$t_{CRP}$	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		5		ns	
14	$t_{RCH}$	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		0		ns	5
15	$t_{RRH}$	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		0		ns	5
16	$t_{ROH}$	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	8		9		10		10		ns	
17	$t_{OAC}$	Access Time from $\overline{OE}$		12		13		14		15	ns	
18	$t_{CAC}$	Access Time from $\overline{CAS}$		12		13		14		15	ns	6, 7
19	$t_{RAC}$	Access Time from $\overline{RAS}$		40		45		50		60	ns	6, 8, 9
20	$t_{CAA}$	Access Time from Column Address		20		22		24		30	ns	6, 7, 10
21	$t_{LZ}$	$\overline{OE}$ or $\overline{CAS}$ to Low-Z Output	0		0		0		0		ns	16
22	$t_{HZ}$	$\overline{OE}$ or $\overline{CAS}$ to High-Z Output	0	6	0	7	0	8	0	10	ns	16
23	$t_{AR}$	Column Address Hold Time from $\overline{RAS}$	30		35		40		50		ns	
24	$t_{RAD}$	$\overline{RAS}$ to Column Address Delay Time	12	20	13	23	14	26	15	30	ns	11
25	$t_{RSH (W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	12		13		14		15		ns	
26	$t_{CWL}$	Write Command to $\overline{CAS}$ Lead Time	12		13		14		15		ns	
27	$t_{WCS}$	Write Command Setup Time	0		0		0		0		ns	12, 13
28	$t_{WCH}$	Write Command Hold Time	5		6		7		10		ns	
29	$t_{WP}$	Write Pulse Width	5		6		7		10		ns	
30	$t_{WCR}$	Write Command Hold Time from $\overline{RAS}$	30		35		40		50		ns	
31	$t_{RWL}$	Write Command to $\overline{RAS}$ Lead Time	12		13		14		15		ns	

**AC Characteristics** (Cont'd)

#	Symbol	Parameter	40		45		50		60		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
32	$t_{DS}$	Data in Setup Time	0		0		0		0		ns	14
33	$t_{DH}$	Data in Hold Time	5		6		7		10		ns	14
34	$t_{WOH}$	Write to $\overline{OE}$ Hold Time	6		7		8		10		ns	14
35	$t_{OED}$	$\overline{OE}$ to Data Delay Time	6		7		8		10		ns	14
36	$t_{RWC}$	Read-Modify-Write Cycle Time	110		115		130		155		ns	
37	$t_{RRW}$	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	75		80		87		105		ns	
38	$t_{CWD}$	$\overline{CAS}$ to $\overline{WE}$ Delay	30		32		34		40		ns	12
39	$t_{RWD}$	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	58		62		68		85		ns	12
40	$t_{CRW}$	$\overline{CAS}$ Pulse Width (RMW)	48		50		52		65		ns	
41	$t_{AWD}$	Col. Address to $\overline{WE}$ Delay	38		41		42		58		ns	12
42	$t_{PC}$	Fast Page Mode Read or Write Cycle Time	23		25		28		35		ns	
43	$t_{CP}$	$\overline{CAS}$ Precharge Time	5		6		7		10		ns	
44	$t_{CAR}$	Column Address to $\overline{RAS}$ Setup Time	20		22		24		30		ns	
45	$t_{CAP}$	Access Time from Column Precharge		22		24		27		34	ns	7
46	$t_{DHR}$	Data in Hold Time Referenced to $\overline{RAS}$	30		35		40		50		ns	
47	$t_{CSR}$	$\overline{CAS}$ Setup Time $\overline{CAS}$ -before- $\overline{RAS}$ Refresh	10		10		10		10		ns	
48	$t_{RPC}$	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		0		ns	
49	$t_{CHR}$	$\overline{CAS}$ Hold Time $\overline{CAS}$ -before- $\overline{RAS}$ Refresh	8		10		12		15		ns	
50	$t_{PCM}$	Fast Page Mode Read-Modify-Write Cycle Time	60		65		70		85		ns	
51	$t_T$	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	15
52	$t_{REF}$	Refresh Interval (512 Cycles)	8		8		8		16		8	17

**Notes:**

1.  $I_{CC}$  is dependent on output loading when the device output is selected. Specified  $I_{CC}$  (max.) is measured with the output open.
2.  $I_{CC}$  is dependent upon the number of address transitions. Specified  $I_{CC}$  (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified  $V_{IL}$  (min.) is steady state operating. During transitions,  $V_{IL}$  (min.) may undershoot to  $-1.0$  V for a period not to exceed 20 ns. All AC parameters are measured with  $V_{IL}$  (min.)  $\geq V_{SS}$  and  $V_{IH}$  (max.)  $\leq V_{CC}$ .
4.  $t_{RCD}$  (max.) is specified for reference only. Operation within  $t_{RCD}$  (max.) limits insures that  $t_{RAC}$  (max.) and  $t_{CAA}$  (max.) can be met. If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max.), the access time is controlled by  $t_{CAA}$  and  $t_{CAC}$ .
5. Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a Read Cycle to occur.
6. Measured with a load equivalent to one TTL input and 50 pF.
7. Access time is determined by the longest of  $t_{CAA}$ ,  $t_{CAC}$  and  $t_{CAP}$ .
8. Assumes that  $t_{RAD} \leq t_{RAD}$  (max.). If  $t_{RAD}$  is greater than  $t_{RAD}$  (max.),  $t_{RAC}$  will increase by the amount that  $t_{RAD}$  exceeds  $t_{RAD}$  (max.).
9. Assumes that  $t_{RCD} \leq t_{RCD}$  (max.). If  $t_{RCD}$  is greater than  $t_{RCD}$  (max.),  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds  $t_{RCD}$  (max.).
10. Assumes that  $t_{RAD} \geq t_{RAD}$  (max.).
11. Operation within the  $t_{RAD}$  (max.) limit ensures that  $t_{RAC}$  (max.) can be met.  $t_{RAD}$  (max.) is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (max.) limit, the access time is controlled by  $t_{CAA}$  and  $t_{CAC}$ .
12.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CWD}$  are not restrictive operating parameters.
13.  $t_{WCS}$  (min.) must be satisfied in an Early Write Cycle.
14.  $t_{DS}$  and  $t_{DH}$  are referenced to the latter occurrence of  $\overline{CAS}$  or  $\overline{WE}$ .
15.  $t_T$  is measured between  $V_{IH}$  (min.) and  $V_{IL}$  (max.). AC-measurements assume  $t_T = 3$  ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200  $\mu$ s pause and 8  $\overline{RAS}$ -containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

**Truth Table**

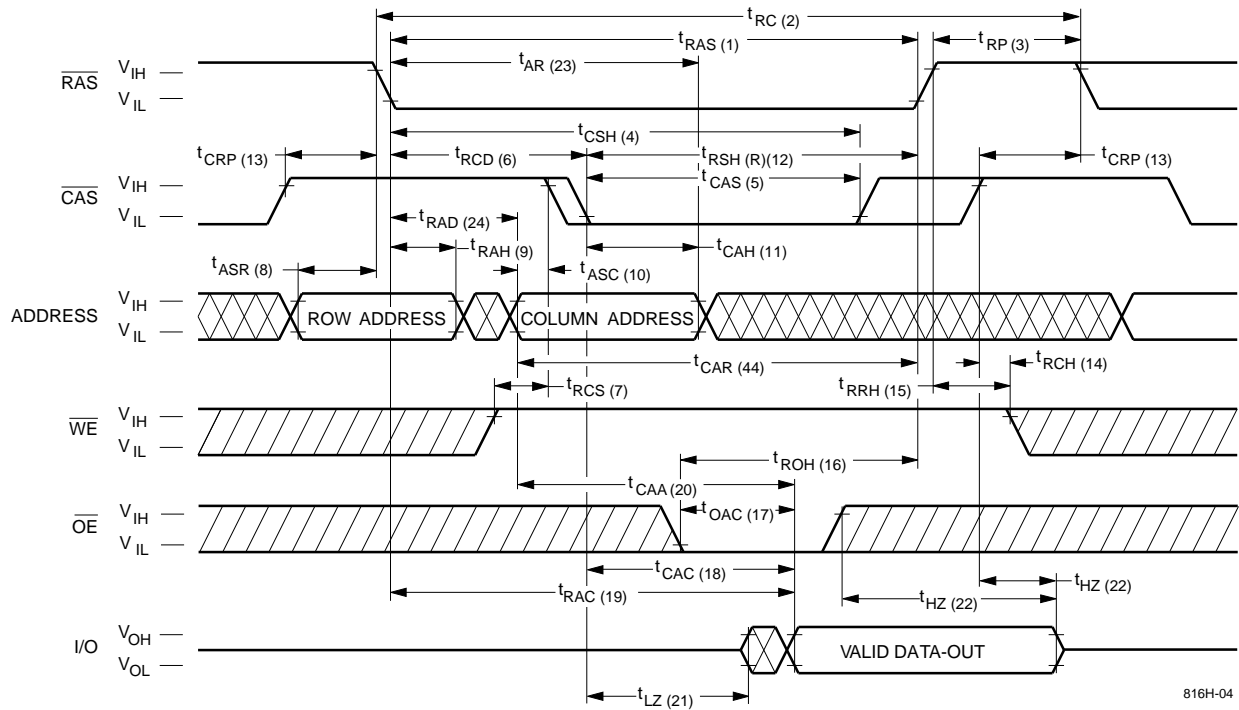
Function	$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	ADDRESS	I/O	Notes
Standby	H	H	H	X	X		High-Z	
Read: Word	L	L	L	H	L	ROW/COL	Data Out	
Read: Lower Byte	L	L	H	H	L	ROW/COL	Lower Byte, Data-Out Upper Byte, High-Z	
Read: Upper Byte	L	H	L	H	L	ROW/COL	Lower Byte, High-Z Upper Byte, Data-Out	
Write: Word (Early-Write)	L	L	L	L	X	ROW/COL	Data-In	
Write: Lower Byte (Early)	L	L	H	L	X	ROW/COL	Lower Byte, Data-In Upper Byte, High-Z	
Read: Upper Byte (Early)	L	H	L	L	X	ROW/COL	Lower Byte, High-Z Upper Byte, Data-In	
Read-Write	L	L	L	H→L	L→H	ROW/COL	Data-Out, Data-In	1, 2
Fast Page-Mode Read	L	H→L	H→L	H	L	COL	Data-Out	2
Fast Page-Mode Write	L	H→L	H→L	L	X	COL	Data-In	2
Fast Page-Mode Read-Write	L	H→L	H→L	H→L	L→H	COL	Data-Out, Data-In	1, 2
Hidden Refresh Read	L→H→L	L	L	H	L	ROW/COL	Data-Out	2
$\overline{\text{RAS}}$ -Only Refresh	L	H	H	X	X	ROW	High-Z	
CBR Refresh	H→L	L	L	X	X		High-Z	3

**Notes:**

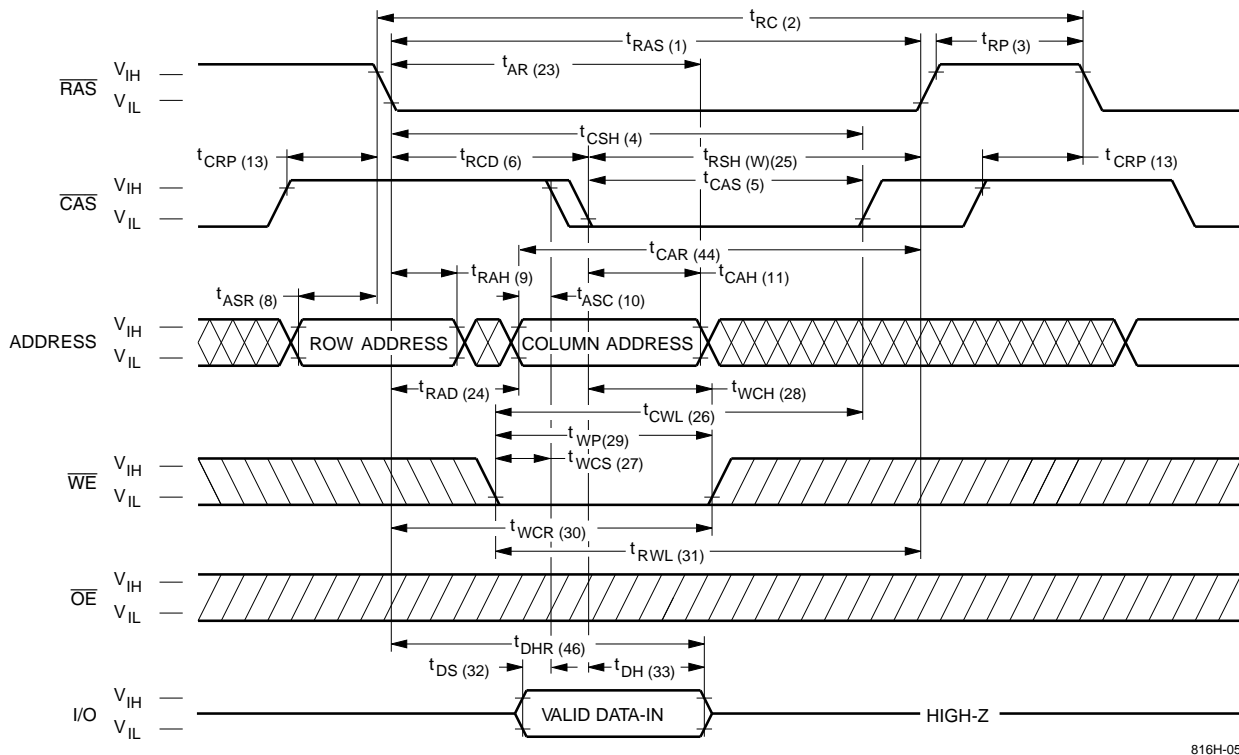
1. Byte write cycles  $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$  active.
2. Byte Read cycles  $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$  active.
3. Only one of the two  $\overline{\text{CAS}}$  must be active ( $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$ ).



Waveforms of Read Cycle

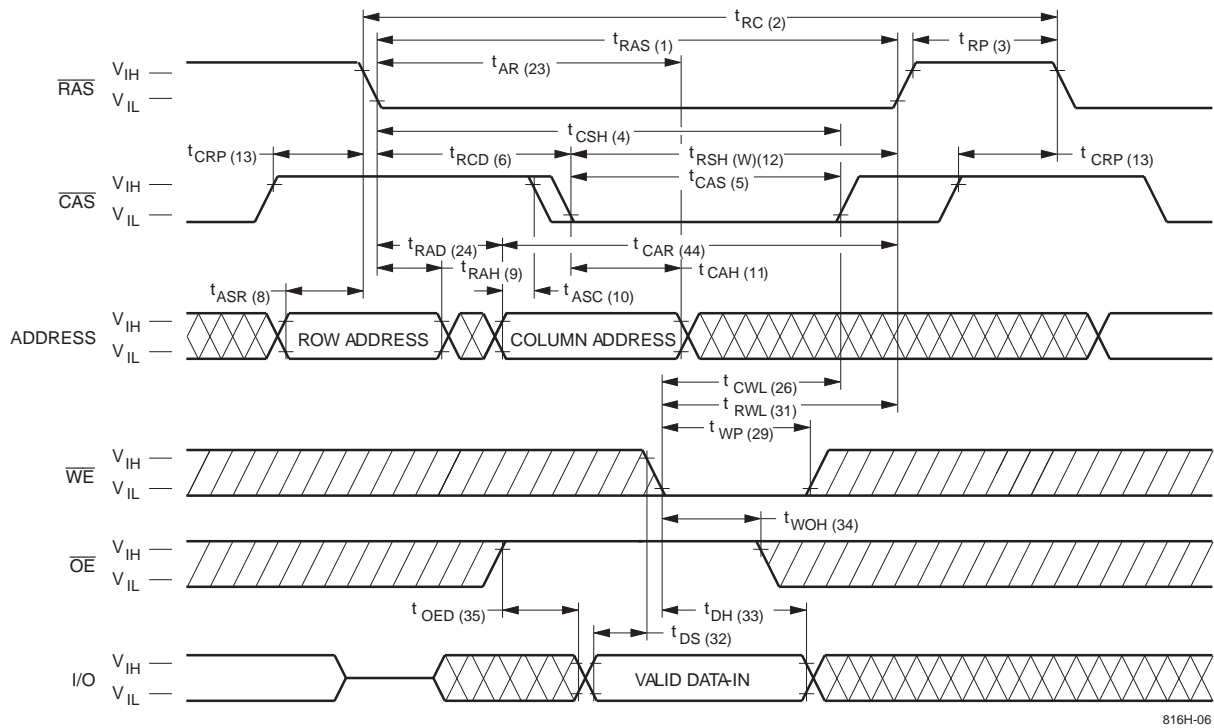


Waveforms of Early Write Cycle



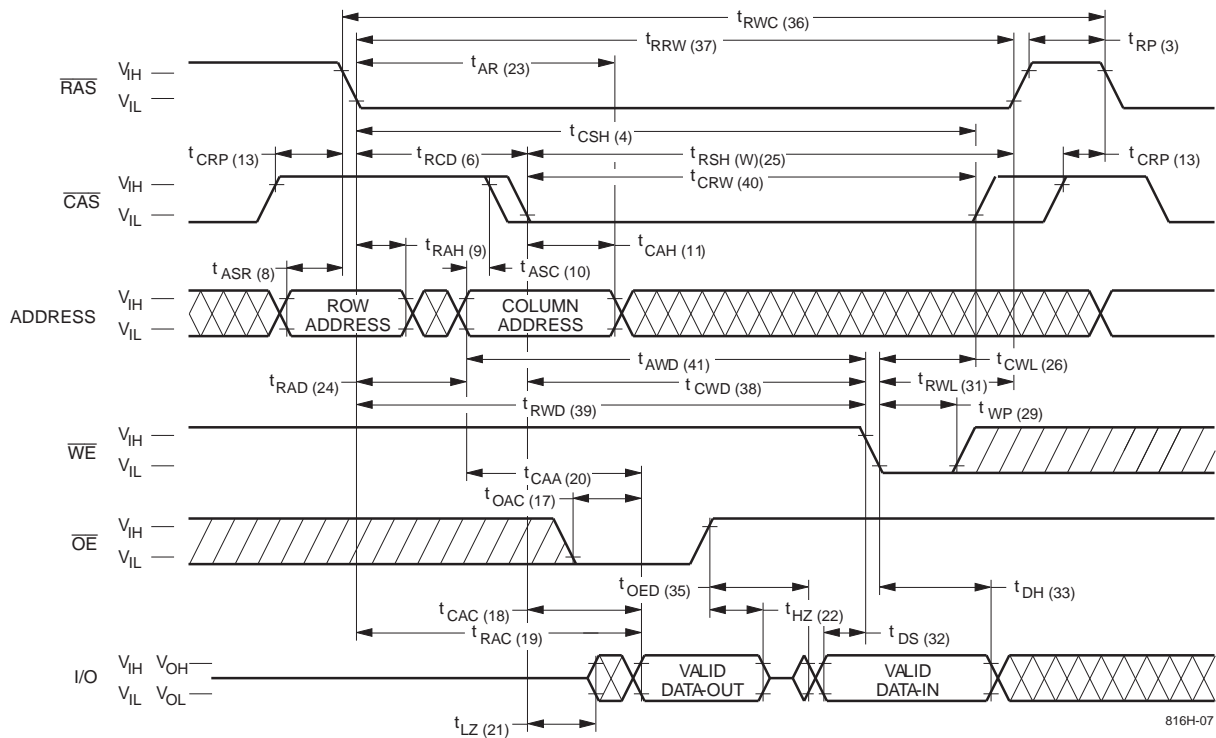
 Don't Care  Undefined

Waveforms of  $\overline{OE}$ -Controlled Write Cycle



816H-06

Waveforms of Read-Modify-Write Cycle

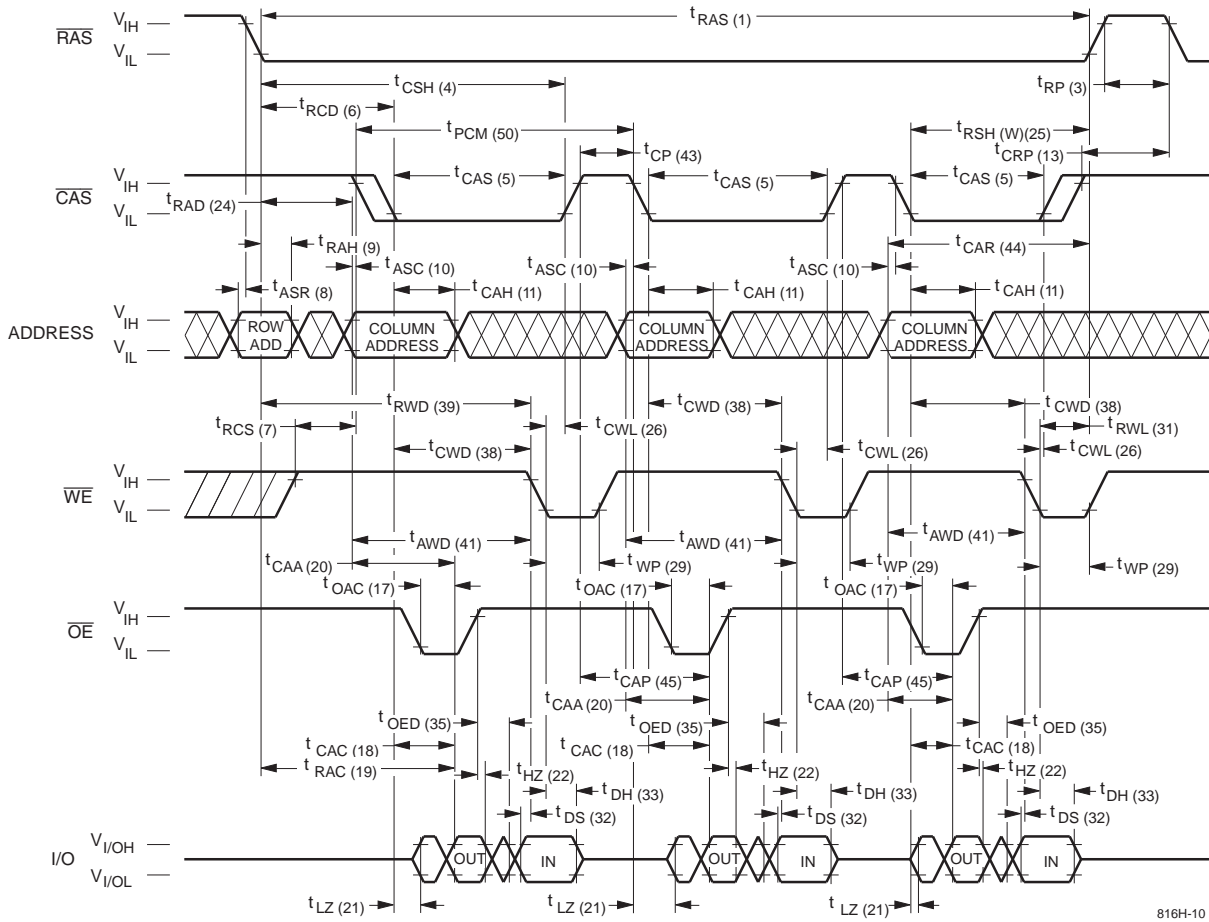


816H-07

Don't Care Undefined

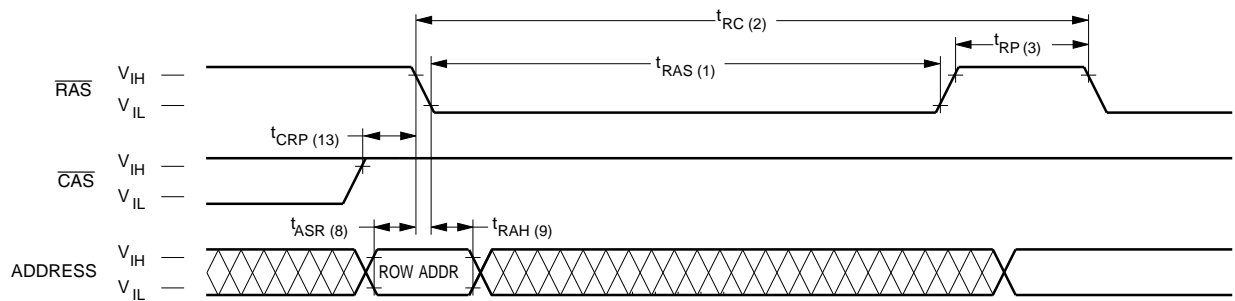


**Waveforms of Fast Page Mode Read-Write Cycle**



816H-10

**Waveforms of RAS-Only Refresh Cycle**

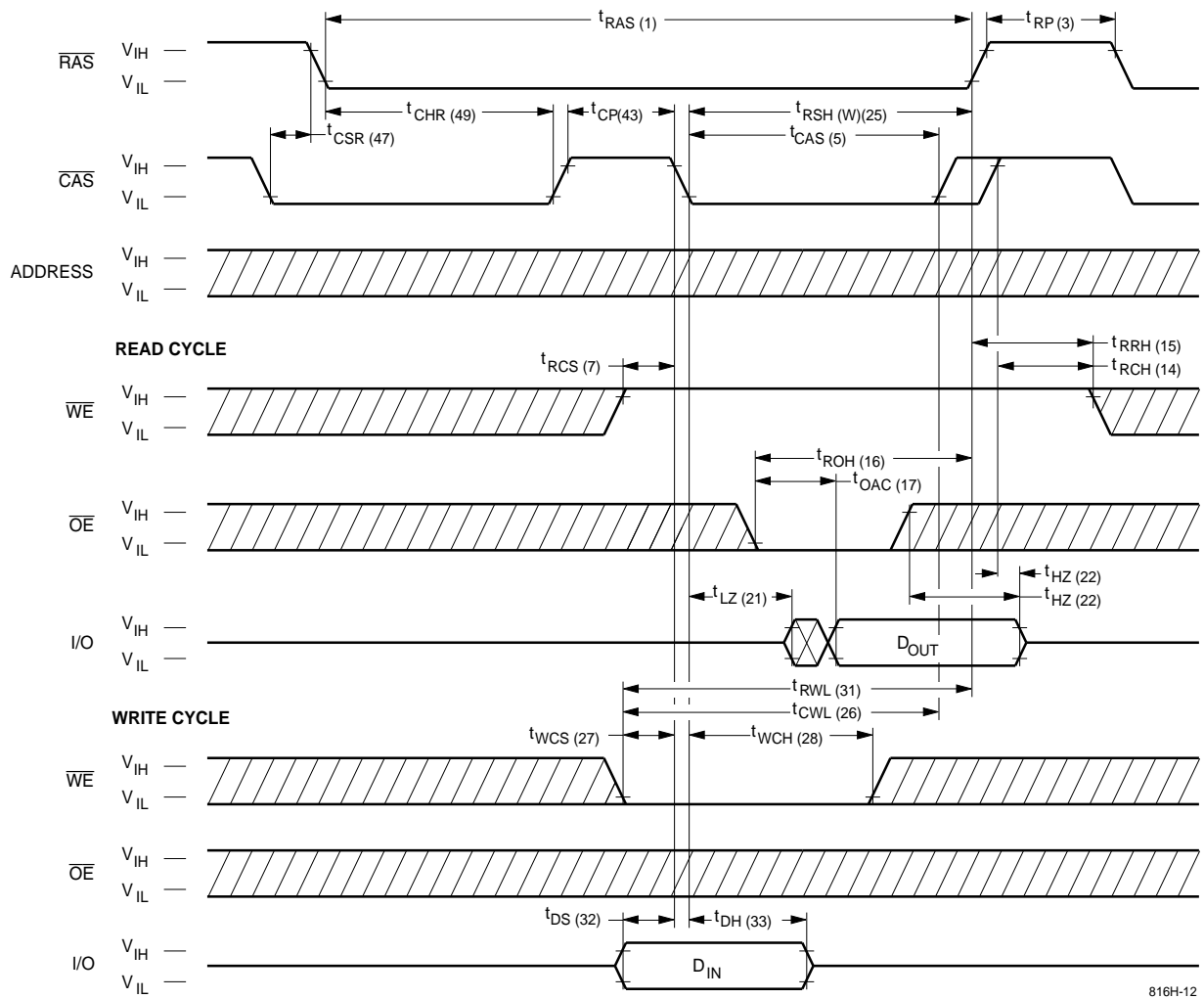


816H-11

NOTE:  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$  = Don't care

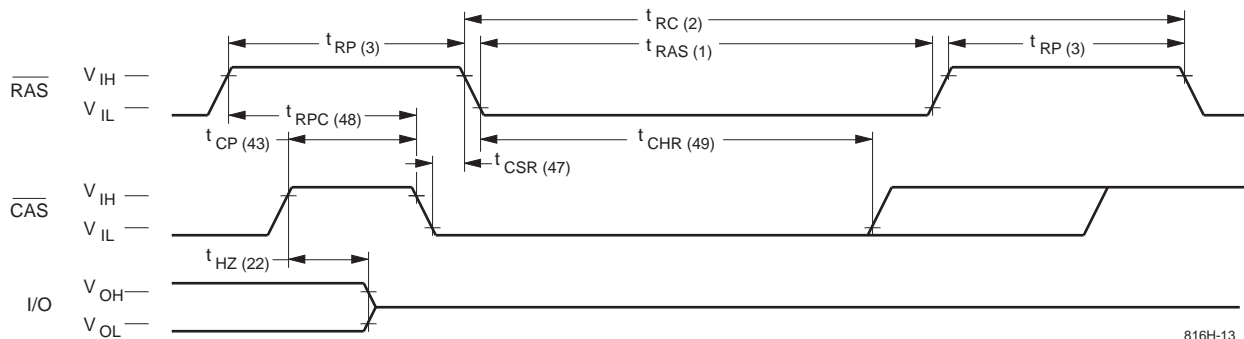


**Waveforms of  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Refresh Counter Test Cycle**



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**Waveforms of  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Refresh Cycle**

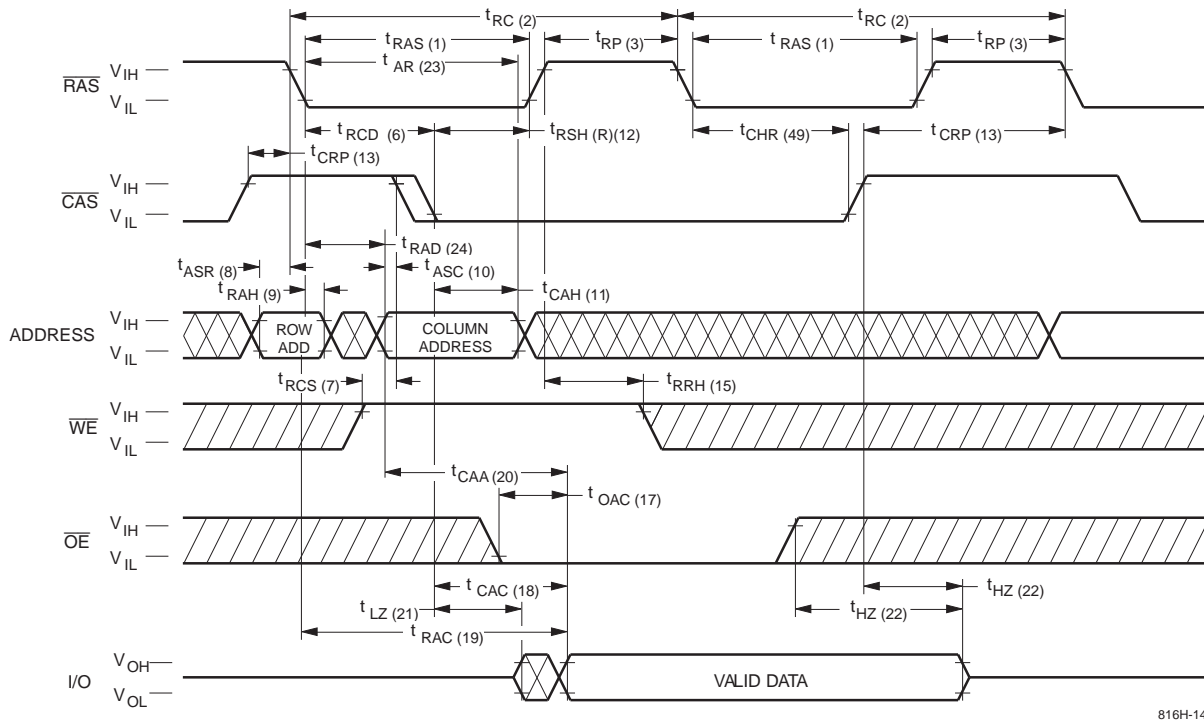


816H-13

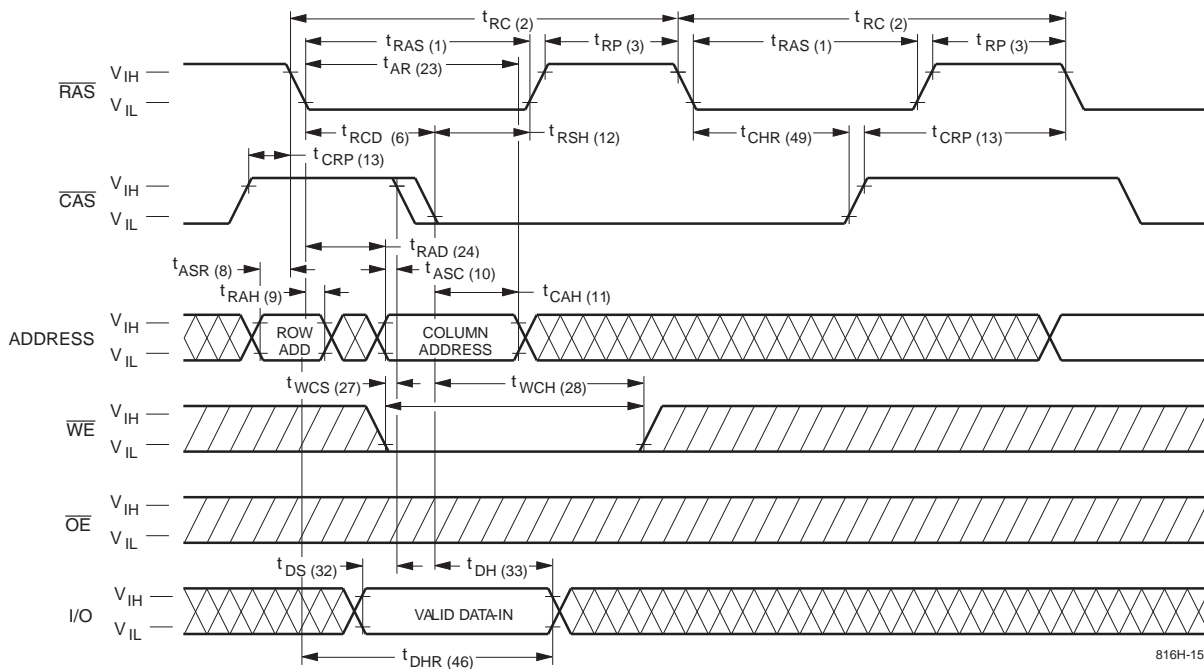
NOTE:  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ ,  $A_0$ - $A_8$  = Don't care

Don't Care Undefined

**Waveforms of Hidden Refresh Cycle (Read)**



**Waveforms of Hidden Refresh Cycle (Write)**



 Don't Care  Undefined

### Functional Description

The V53C816H is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C816H reads and writes data by multiplexing an 19-bit address into a 10-bit row and a 9-bit column address. The row address is latched by the Row Address Strobe ( $\overline{RAS}$ ). The column address “flows through” an internal address buffer and is latched by the Column Address Strobe ( $\overline{CAS}$ ). Because access time is primarily dependent on a valid column address rather than the precise time that the  $\overline{CAS}$  edge occurs, the delay time from  $\overline{RAS}$  to  $\overline{CAS}$  has little effect on the access time.

### Memory Cycle

A memory cycle is initiated by bringing  $\overline{RAS}$  low. Any memory cycle, once initiated, must not be ended or aborted before the minimum  $t_{RAS}$  time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time  $t_{RP}/t_{CP}$  has elapsed.

### Read Cycle

A Read cycle is performed by holding the Write Enable ( $\overline{WE}$ ) signal High during a  $\overline{RAS}/\overline{CAS}$  operation. The column address must be held for a minimum specified by  $t_{AR}$ . Data Out becomes valid only when  $t_{OAC}$ ,  $t_{RAC}$ ,  $t_{CAA}$  and  $t_{CAC}$  are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by  $t_{CAA}$  when  $t_{RAC}$ ,  $t_{CAC}$  and  $t_{OAC}$  are all satisfied.

### Write Cycle

A Write Cycle is performed by taking  $\overline{WE}$  and  $\overline{CAS}$  low during a  $\overline{RAS}$  operation. The column address is latched by  $\overline{CAS}$ . The Write Cycle can be  $\overline{WE}$  controlled or  $\overline{CAS}$  controlled depending on whether  $\overline{WE}$  or  $\overline{CAS}$  falls later. Consequently, the input data must be valid at or before the falling edge of  $\overline{WE}$  or  $\overline{CAS}$ , whichever occurs last. In the  $\overline{CAS}$ -controlled Write Cycle, when the leading edge of  $\overline{WE}$  occurs prior to the  $\overline{CAS}$  low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with  $\overline{RAS}$  or  $\overline{CAS}$  will maintain the output in the High-Z state.

In the  $\overline{WE}$  controlled Write Cycle,  $\overline{OE}$  must be in the high state and  $t_{OED}$  must be satisfied.

### Fast Page Mode Operation

Fast Page Mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining  $\overline{RAS}$  low while performing successive  $\overline{CAS}$  cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while  $\overline{CAS}$  is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of  $\overline{CAS}$ , eliminating  $t_{ASC}$  and  $t_T$  from the critical timing path.  $\overline{CAS}$  latches the address into the column address buffer and acts as an output enable. During Fast Page Mode operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is  $t_{CAA}$  or  $t_{CAP}$  controlled. If the column address is valid prior to the rising edge of  $\overline{CAS}$ , the access time is referenced to the  $\overline{CAS}$  rising edge and is specified by  $t_{CAP}$ . If the column address is valid after the rising  $\overline{CAS}$  edge, access is timed from the occurrence of a valid address and is specified by  $t_{CAA}$ . In both cases, the falling edge of  $\overline{CAS}$  latches the address and enables the output.

Fast Page Mode provides a sustained data rate of 43 MHz for applications that require high data rates such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{512}{t_{RC} + 511 \times t_{PC}}$$

### Data Output Operation

The V53C816H Input/Output is controlled by  $\overline{OE}$ ,  $\overline{CAS}$ ,  $\overline{WE}$  and  $\overline{RAS}$ . A  $\overline{RAS}$  low transition enables the transfer of data to and from the selected row address in the Memory Array. A  $\overline{RAS}$  high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a  $\overline{RAS}$  low transition, a  $\overline{CAS}$  low transition or  $\overline{CAS}$  low level enables the internal I/O path. A  $\overline{CAS}$  high transition or a  $\overline{CAS}$  high level disables the I/O path and the output driver if it is enabled. A  $\overline{CAS}$  low transition while  $\overline{RAS}$  is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding  $\overline{OE}$  high. The  $\overline{OE}$  signal has no effect on

any data stored in the output latches. A  $\overline{WE}$  low level can also disable the output drivers when  $\overline{CAS}$  is low. During a Write cycle, if  $\overline{WE}$  goes low at a time in relationship to  $\overline{CAS}$  that would normally cause the outputs to be active, it is necessary to use  $\overline{OE}$  to disable the output drivers prior to the  $\overline{WE}$  low transition to allow Data In Setup Time ( $t_{DS}$ ) to be satisfied.

### Power-On

After application of the  $V_{CC}$  supply, an initial pause of 200  $\mu s$  is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a RAS clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During Power-On, the  $V_{CC}$  current requirement of the V53C816H is dependent on the input levels of RAS and CAS. If RAS is low during Power-On, the device will go into an active cycle and  $I_{CC}$  will exhibit current transients. It is recommended that RAS and CAS track with  $V_{CC}$  or be held at a valid  $V_{IH}$  during Power-On to avoid current surges.

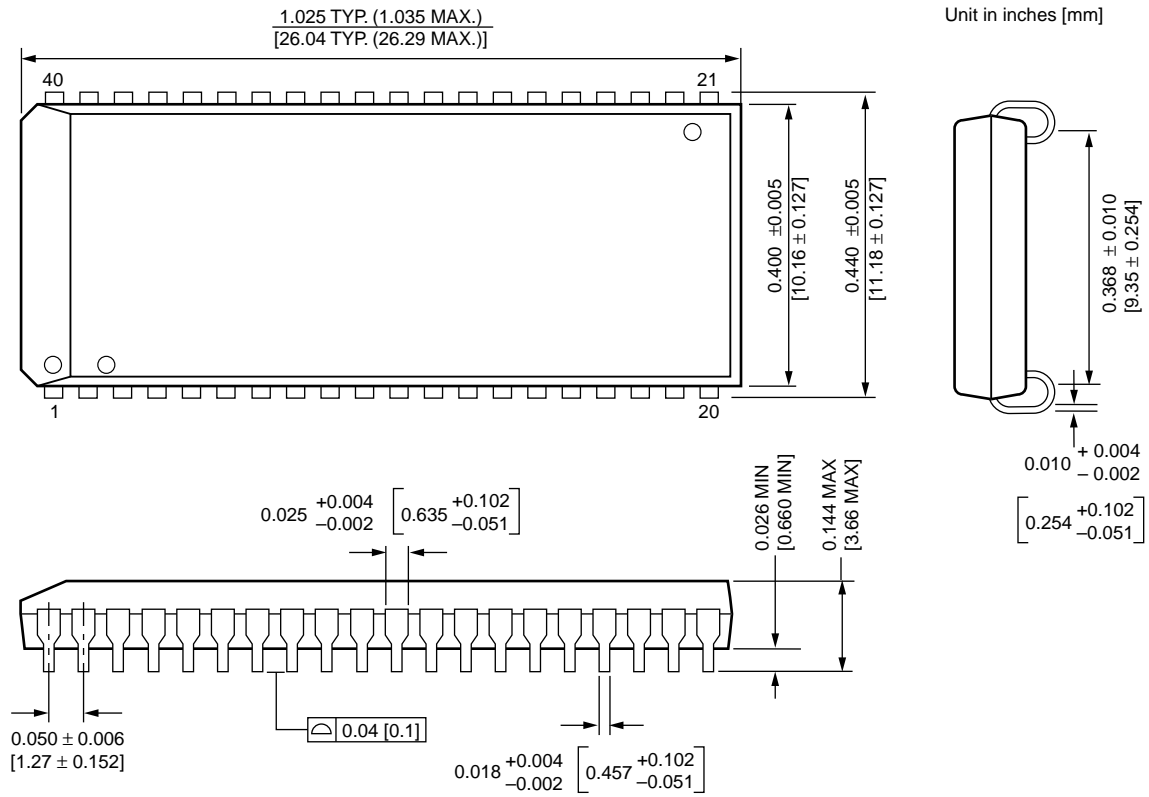
**Table 1. V53C816H Data Output Operation for Various Cycle Types**

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$ -Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$ -Controlled Write Cycle (Late Write)	$\overline{OE}$ Controlled. High $\overline{OE} = \text{High-Z I/Os}$
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$ -only Refresh	High-Z
$\overline{CAS}$ -before- $\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$ -only Cycles	High-Z



**Package Diagram**

**40-Pin Plastic SOJ**



**U.S.A.**

3910 NORTH FIRST STREET  
SAN JOSE, CA 95134  
PHONE: 408-433-6000  
FAX: 408-433-0952

**HONG KONG**

19 DAI FU STREET  
TAIPO INDUSTRIAL ESTATE  
TAIPO, NT, HONG KONG  
PHONE: 852-2665-4883  
FAX: 852-2664-7535

**TAIWAN**

7F, NO. 102  
MIN-CHUAN E. ROAD, SEC. 3  
TAIPEI  
PHONE: 886-2-2545-1213  
FAX: 886-2-2545-1209

1 CREATION ROAD I  
SCIENCE BASED IND. PARK  
HSIN CHU, TAIWAN, R.O.C.  
PHONE: 886-3-578-3344  
FAX: 886-3-579-2838

**SINGAPORE**

10 ANSON ROAD #23-13  
INTERNATIONAL PLAZA  
SINGAPORE 079903  
PHONE: 65-3231801  
FAX: 65-3237013

**JAPAN**

WBG MARINE WEST 25F  
6, NAKASE 2-CHOME  
MIHAMA-KU, CHIBA-SHI  
CHIBA 261-71  
PHONE: 81-43-299-6000  
FAX: 81-43-299-6555

**IRELAND & UK**

BLOCK A UNIT 2  
BROOMFIELD BUSINESS PARK  
MALAHIDE  
CO. DUBLIN, IRELAND  
PHONE: +353 1 8038020  
FAX: +353 1 8038049

**GERMANY  
(CONTINENTAL  
EUROPE & ISRAEL )**

71083 HERRENBERG  
BENZSTR. 32  
GERMANY  
PHONE: +49 7032 2796-0  
FAX: +49 7032 2796 22

**U.S. SALES OFFICES****NORTHWESTERN**

3910 NORTH FIRST STREET  
SAN JOSE, CA 95134  
PHONE: 408-433-6000  
FAX: 408-433-0952

**NORTHEASTERN**

SUITE 436  
20 TRAFALGAR SQUARE  
NASHUA, NH 03063  
PHONE: 603-889-4393  
FAX: 603-889-9347

**NORTHEASTERN**

SUITE 436  
20 TRAFALGAR SQUARE  
NASHUA, NH 03063  
PHONE: 603-889-4393  
FAX: 603-889-9347

**SOUTHWESTERN**

SUITE 200  
5150 E. PACIFIC COAST HWY.  
LONG BEACH, CA 90804  
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RICHARDSON, TX 75081  
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