MAC8S SERIES

Advance Information

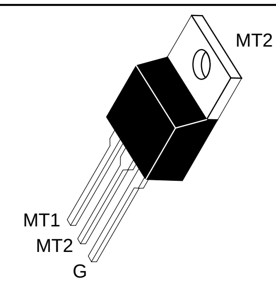
TRIACS

Silicon Bidirectional Thyristors

Designed for industrial and consumer applications for full wave control of ac loads such as appliance controls, heater controls, motor controls, and other power switching applications.

- Sensitive Gate Allows Triggering by Microcontrollers and other Logic Circuits
- High Immunity to dv/dt — 25 V/µs Minimum at 110°C
- High Commutating di/dt — 8.0 A/ms Minimum at 110°C
- Minimum and Maximum Values of I_{GT}, V_{GT} and I_H Specified for ease of Design
- On-State Current Rating of 8 Amperes RMS at 70°C
- High Surge Current Capability — 70 Amperes
- Blocking Voltage to 800 Volts
- Rugged, Economical TO220AB Package

TRIACS
8 AMPERES RMS
400 THRU 800
VOLTS



CASE 221A–06
(TO-220AB)
STYLE 4

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Peak Repetitive Off-State Voltage (1) (T_J = –40 to 110°C, Sine Wave, 50 to 60Hz, Gate Open)	 MAC8SD MAC8SM MAC8SN	V_{DRM}	 400 600 800	Volts
On-State RMS Current (Full Cycle Sine Wave, 60Hz, T_J = 70°C)		$I_{T(RMS)}$	8	A
Peak Non-repetitive Surge Current (One Half Cycle, 60Hz, T_J = 110°C)		I_{TSM}	70	A
Circuit Fusing Consideration (t = 8.3 ms)		I^2t	20	A^2sec
Peak Gate Power (Pulse Width ≤ 1.0µs, T_C = 70°C)		P_{GM}	16	Watts
Average Gate Power (t = 8.3ms, T_C = 70°C)		$P_{G(AV)}$	0.35	Watts
Operating Junction Temperature Range		T_J	–40 to +110	°C
Storage Temperature Range		T_{stg}	–40 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 2.2 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 5 Seconds	T_L	260	°C

(1) V_{DRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

REV 0

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Peak Repetitive Blocking Current (V_D = Rated V_{DRM}, Gate Open) T_J = 25°C	I_{DRM}	—	—	0.01	mA
T_J = 110°C		—	—	2.0	
ON CHARACTERISTICS					
Peak On-State Voltage* (I_{TM} = ±11A)	V_{TM}	—	—	1.85	Volts
Continuous Gate Trigger Current (V_D = 12 V, R_L = 100Ω)	I_{GT}				mA
MT2(+), G(+)		.8	2.0	5.0	
MT2(+), G(–)		.8	3.0	5.0	
MT2(–), G(–)		.8	3.0	5.0	
Hold Current (V_D = 12V, Gate Open, Initiating Current = ±150mA)	I_H	1.0	3.0	10	mA
Latching Current (V_D = 24V, I_G = 5mA)	I_L				mA
MT2(+), G(+)		2.0	5.0	15	
MT2(–), G(–)		2.0	10	20	
MT2(+), G(–)		2.0	5.0	15	
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100Ω)	V_{GT}				Volts
MT2(+), G(+)		0.45	0.62	1.5	
MT2(+), G(–)		0.45	0.60	1.5	
MT2(–), G(–)		0.45	0.65	1.5	
DYNAMIC CHARACTERISTICS					
Critical Rate of Rise of Off–State Voltage (V_D = 400V, I_{TM} = 3.5A, Commutating dv/dt = 10Vμ/sec, Gate Open, T_J = 110°C, f= 500 Hz, Snubber: C_S = 0.01 μF, R_S = 15Ω, see Figure 16.)	(dv/dt)c	8.0	10	—	A/ms
Critical Rate of Rise of Off-State Voltage (V_D = Rate V_{DRM}, Exponential Waveform, R_{GK} = 510Ω, T_J = 110°C)	dv/dt	25	75	—	V/μs

* Indicates Pulse Test: Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2%.

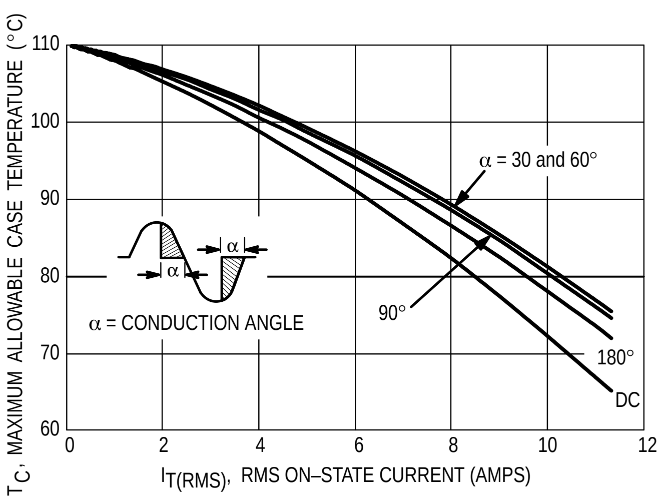


Figure 1.0 RMS Current Derating

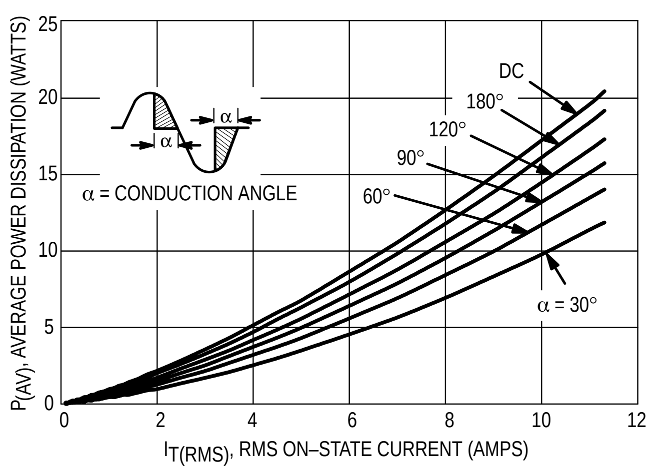


Figure 2.0 Maximum On–State Power Dissipation

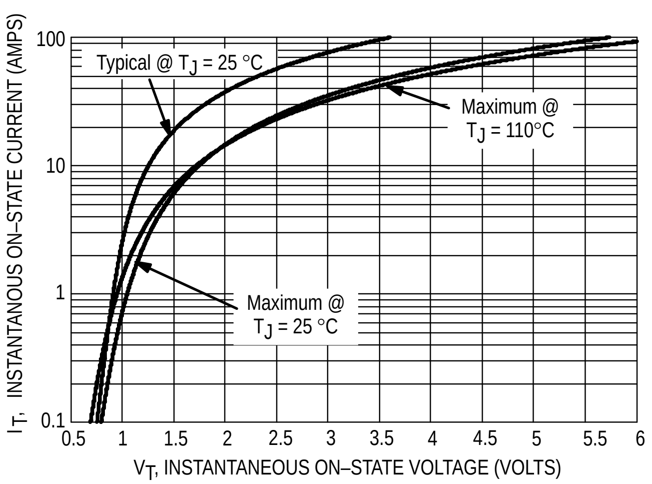


Figure 3.0 On–State Characteristics

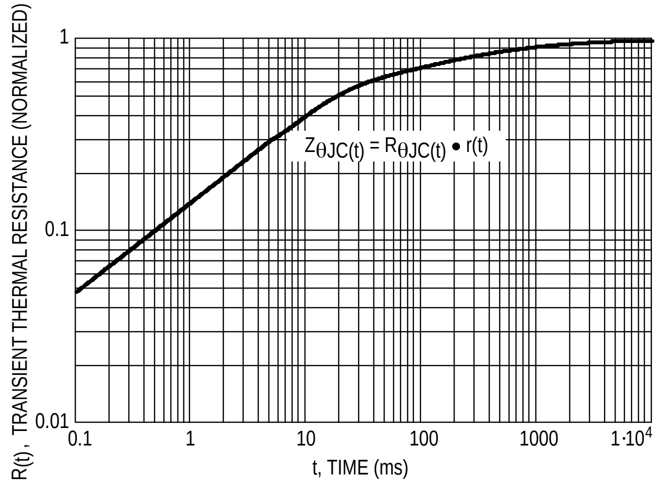


Figure 4.0 Transient Thermal Response

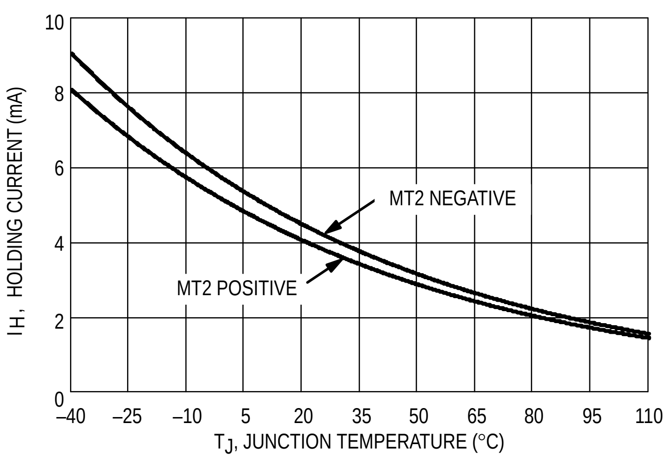


Figure 5.0 Typical Holding Current Versus Junction Temperature

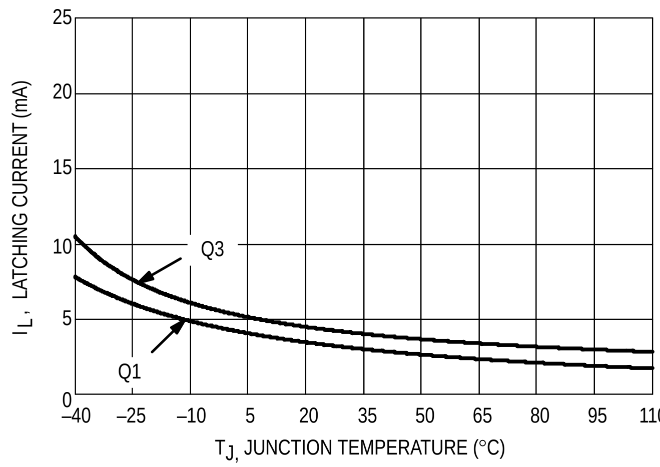


Figure 6.0 Typical Latching Current Versus Junction Temperature

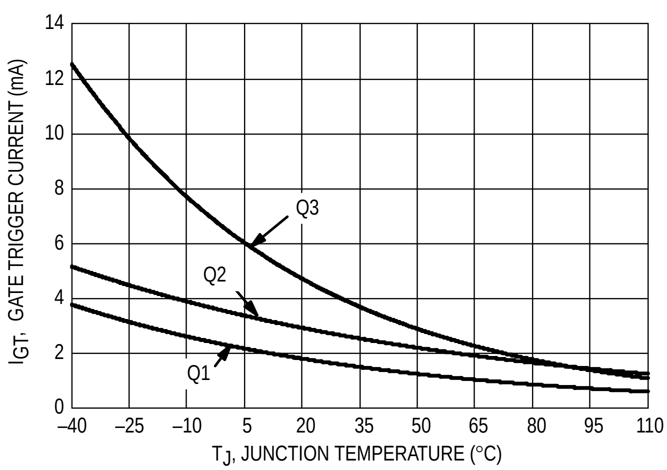


Figure 7.0 Typical Gate Trigger Current Versus Junction Temperature

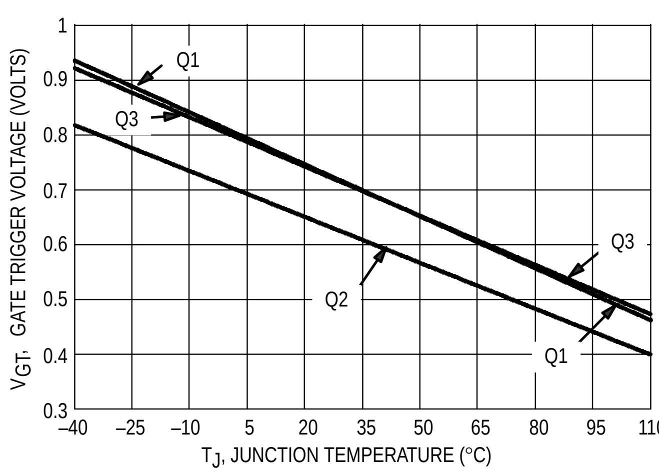


Figure 8.0 Typical Gate Trigger Voltage Versus Junction Temperature

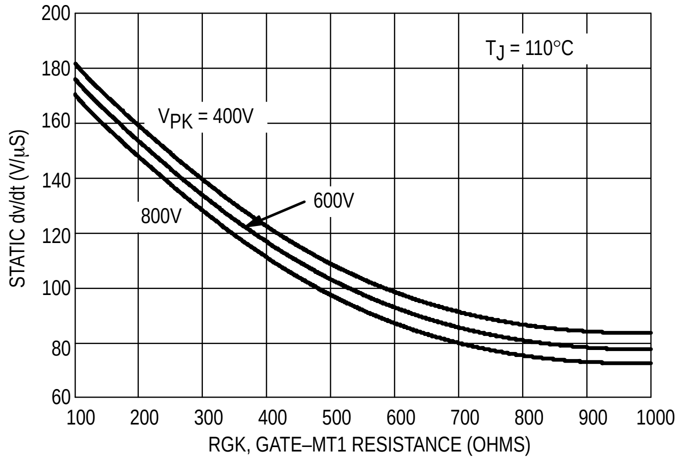


Figure 9.0 Typical Exponential Static dv/dt Versus Gate–MT1 Resistance, MT2(+)

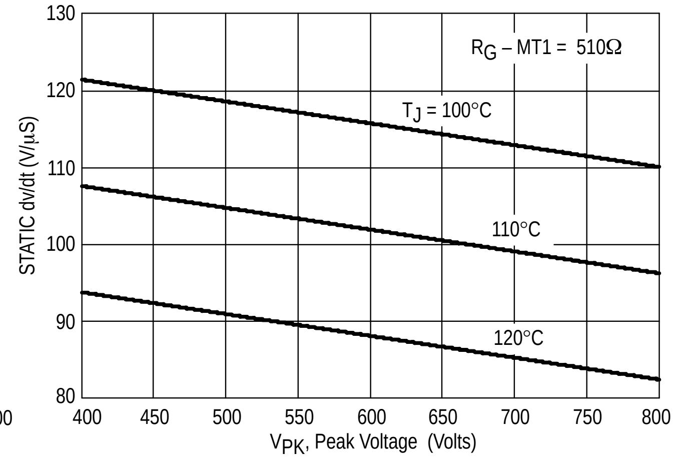


Figure 10.0 Typical Exponential Static dv/dt Versus Peak Voltage, MT2(+)

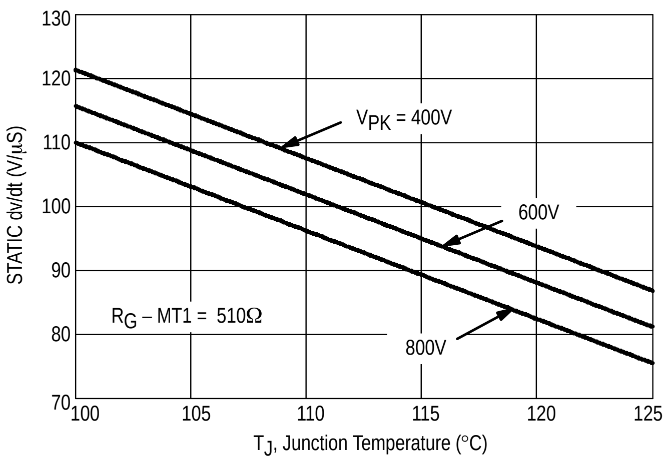


Figure 11.0 Typical Exponential Static dv/dt Versus Junction Temperature, MT2(+)

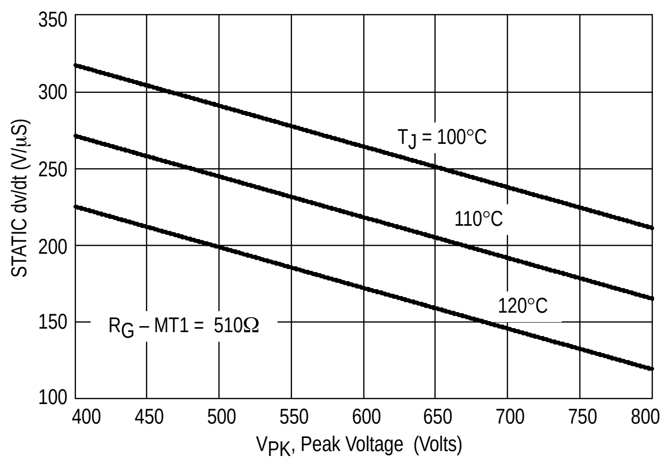


Figure 12.0 Typical Exponential Static dv/dt Versus Peak Voltage, MT2(–)

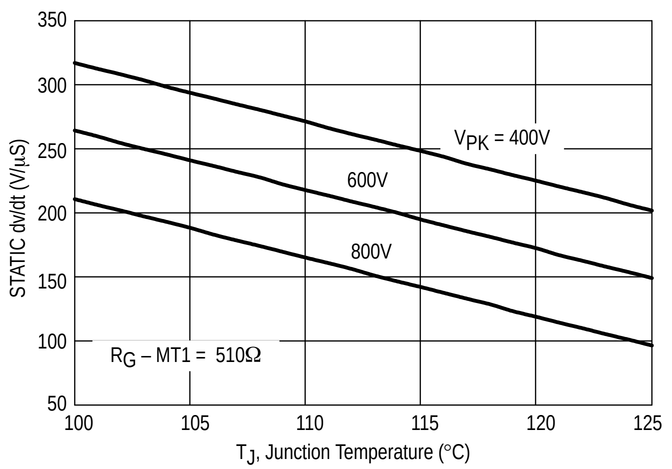


Figure 13.0 Typical Exponential Static dv/dt Versus Junction Temperature, MT2(–)

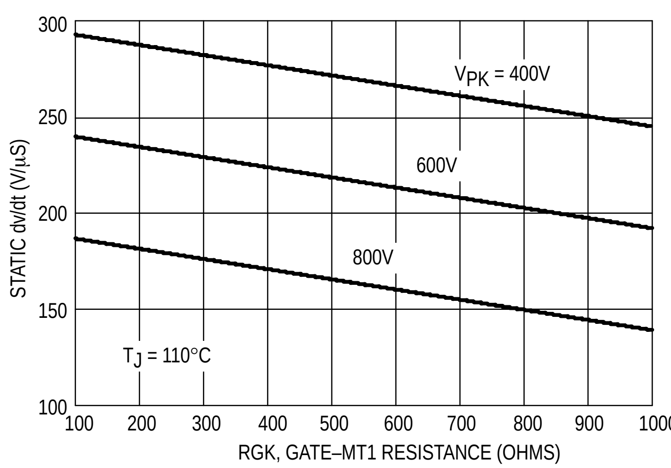


Figure 14.0 Typical Exponential Static dv/dt Versus Gate–MT1 Resistance, MT2(–)

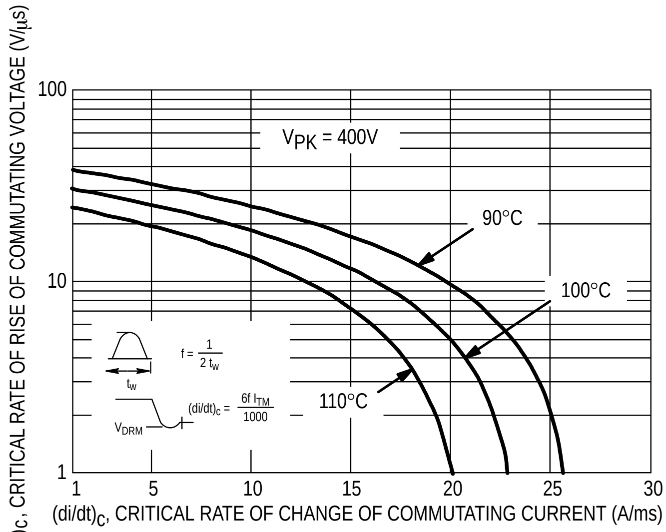
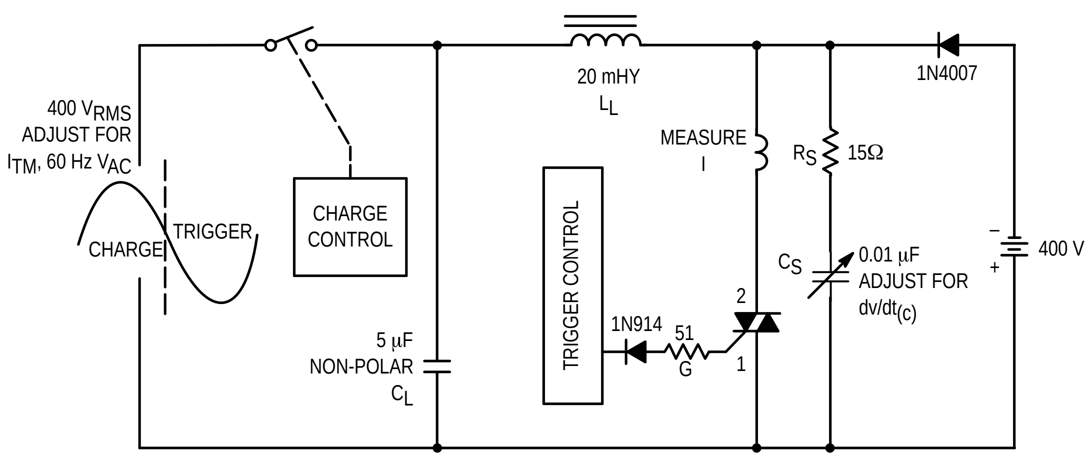


Figure 15.0 Critical Rate of Rise of Commutating Voltage



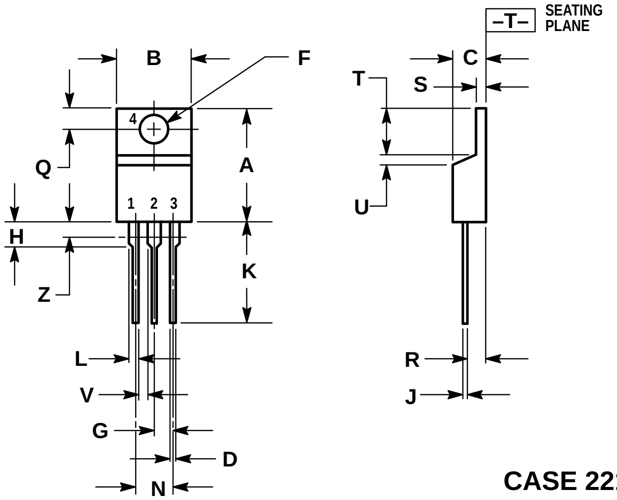
Note: Component values are for verification of rated $(dv/dt)_c$. See AN1048 for additional information.

Figure 16.0 Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Voltage

NOTES

NOTES

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

CASE 221A–06
(TO-220AB)

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