Product Preview

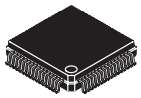
Low-Voltage 1:22 Differential PECL/HSTL Clock Driver

MC100EP223

LOW–VOLTAGE 1:22 DIFFERENTIAL PECL/HSTL CLOCK DRIVER

The MC100EP223 is a low skew 1–to–22 differential driver, designed with clock distribution in mind. It accepts two clock sources into an input multiplexer. The selected signal is fanned out to 22 identical differential outputs.

- 200ps Part–to–Part Skew
- 50ps Output–to–Output Skew
- Differential Design
- Open Emitter HSTL Compatible Outputs
- 3.3V V_{CC}
- Both PECL and HSTL Inputs
- 75kΩ Input Pulldown Resistors
- Thermally Enhanced 64 lead Exposed Pad LQFP



TC SUFFIX
64–LEAD LQFP PACKAGE
CASE 840K–01

The EP223 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate–to–gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

The EP223 HSTL outputs are not realized in the conventional manner. To minimize part–to–part and output–to–output skew, the HSTL compatible output levels are generated with an open emitter architecture. The outputs are pulled down with 50Ω to ground, rather than the typical 50Ω to V_{DDQ} pullup of a “standard” HSTL output. Because the HSTL outputs are pulled to ground, the EP223 does not utilize the V_{DDQ} supply of the HSTL standard. The output levels are derived from V_{CC}.

In the case of an asynchronous control, there is a chance of generating a ‘runt’ clock pulse when the device is enabled/disabled. To avoid this, the output enable (OE) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all 22 differential pairs will be used and therefore terminated. In the case where fewer than 22 pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

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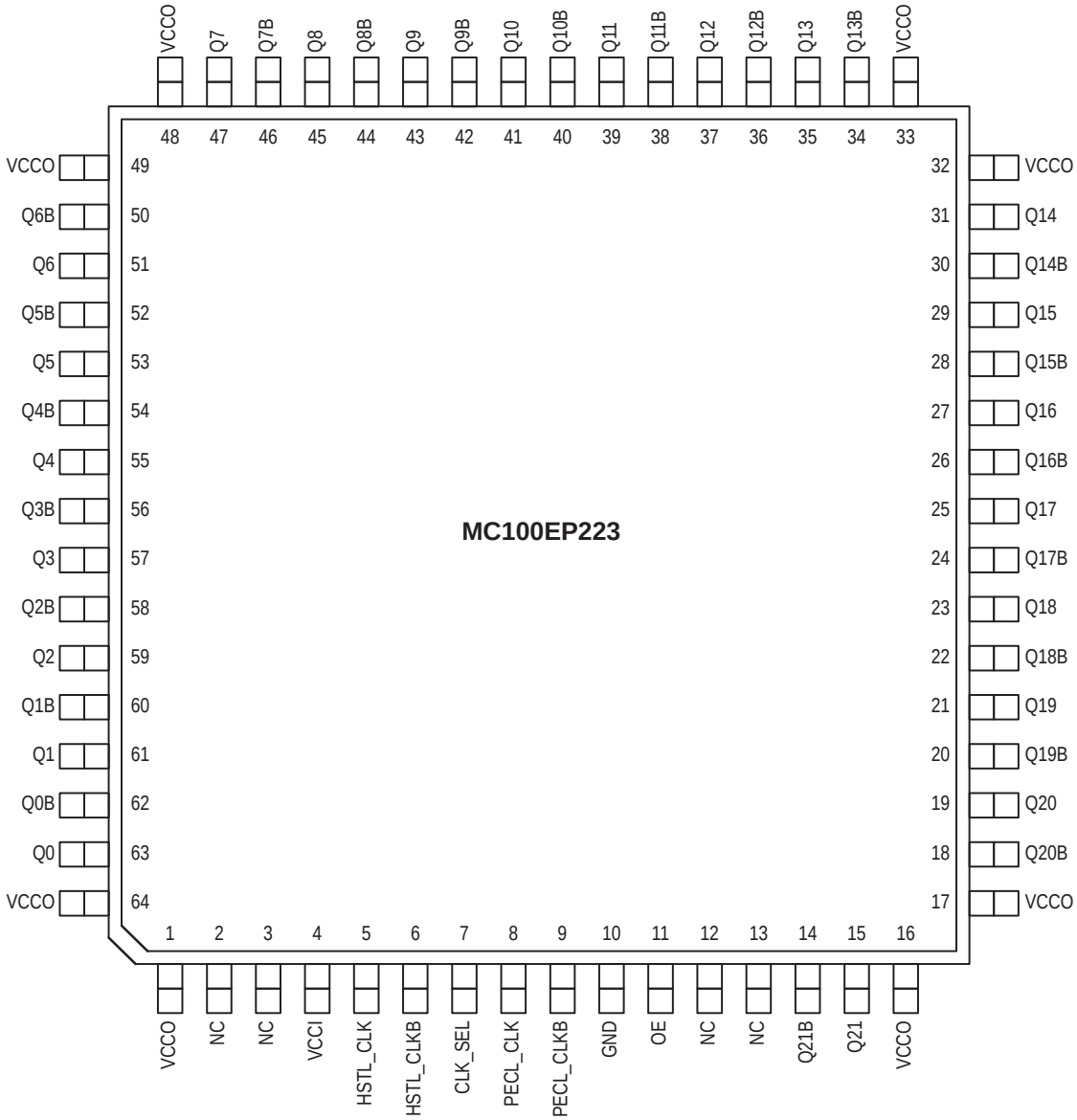


Figure 1. 64–Lead Pinout (Top View)

PIN NAMES

Pins	Function
HSTL_CLK, HSTL_CLKB	Differential HSTL Inputs
PECL_CLK, PECL_CLKB	Differential PECL Inputs
Q0:21, Q0B:21B	Differential HSTL Outputs
CLK_SEL	Active Clock Select Input
OE	Output Enable
GND	Ground
VCCI	Core VCC
VCCO	I/O VCC

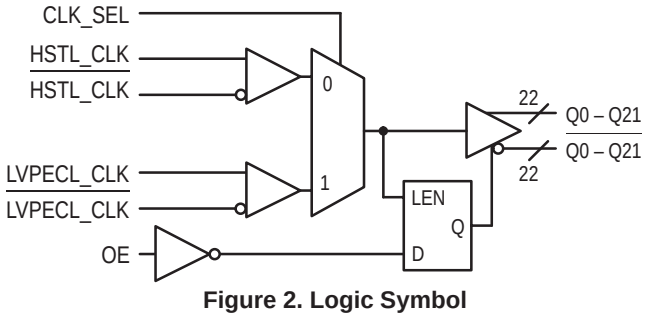


Figure 2. Logic Symbol

FUNCTION

OE	CLK_SEL	Q0:21, Q0B:21B
0	0	Q = Low, QB = High
0	1	Q = Low, QB = High
1	0	HSTL_CLK, HSTL_CLKB
1	1	PECL_CLK, PECL_CLKB

SIGNAL GROUPS

Level	Direction	Signal
HSTL	Input	HSTL_CLK, HSTL_CLKB
HSTL	Output	Q0:21, Q0B:21B
LVPECL	Input	PECL_CLK, PECL_CLKB
LVCMOS/LVTTL	Input	CLK_SEL, OE

HSTL DC CHARACTERISTICS

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage				1.0						V
V_{OL}	Output LOW Voltage						0.4				V
V_{IH}	Input HIGH Voltage				$V_{\mathfrak{X}}$+0.1		1.6				V
V_{IL}	Input LOW Voltage				–0.3		$V_{\mathfrak{X}}$–0.1				V
$V_{\mathfrak{X}}$	Input Crossover Voltage				0.68		0.9				V

PECL DC CHARACTERISTICS

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage (Note 1.)	2.135		2.420	2.135		2.420	2.135		2.420	V
V_{IL}	Input LOW Voltage (Note 1.)	1.490		1.825	1.490		1.825	1.490		1.825	V
I_{IH}	Input HIGH Current			150			150			150	µA

1. These values are for V_{CC} = 3.3V. Level specifications vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{EE} = GND, V_{CC} =$V_{CC(min)}$ to $V_{CC(max)}$)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delay to Output IN (Differential)		1.0			1.0			1.0		ns
t_{skew}	Within–Device Skew Part–to–Part Skew (Diff)			50 200			50 200			50 200	ps
f_{max}	Maximum Input Frequency			250			250			250	MHz
V_{PP}	Minimum Input Swing PECL_CLK		600			600			600		mV
V_{CMR}	Common Mode Range PECL_CLK										V
t_r, t_f	Output Rise/Fall Time (20–80%)	300		600	300		600	300		600	ps

Power Supply Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
V_{CCI}	Core V_{CC}	3.0	3.3	3.6	V
V_{CCO}	I/O V_{CC}	1.6	1.8	2.0	V
I_{CC}	Power Supply Current				mA
I_{EE}	Power Supply Current				mA

APPLICATIONS INFORMATION

Using the thermally enhanced package of the MC100EP223

The MC100EP223 uses a thermally enhanced 64 lead LQFP package. This package provides the low thermal impedance that supports the power consumption of the MC100EP223 high-speed bipolar integrated circuit and eases the power management task for the system design. An exposed pad at the bottom of the package establishes thermal conductivity from the package to the printed circuit board. In order to take advantage of the enhanced thermal capabilitites of this package, it is recommended to solder the exposed pad of the package to the printed circuit board. The attachment process for exposed pad package is the same as for any standard surface mount package. Vias are recommended from the pad on the board down to an appropriate plane in the board that is capable of distributing the heat. In order to supply enough solder paste to fill those vias and not starve the solder joints, it may be required to stencil print solder paste onto the printed circuit pad. This pad should match the dimensions of the exposed pad. The dimensions of the exposed pad are shown on the package outline in this specification. For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

Thermal Resistance

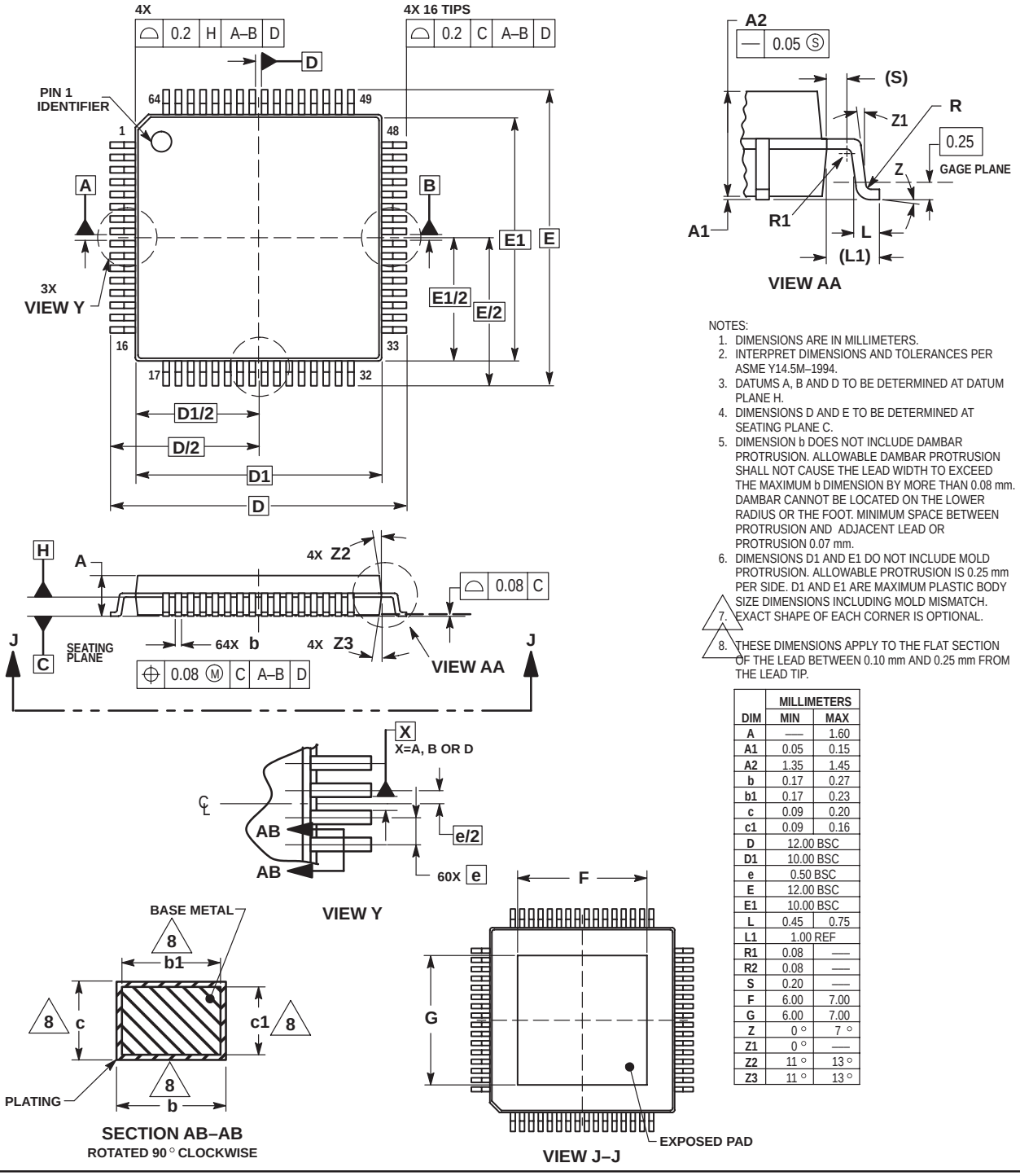
Convection LFPM	R_{THJA}[a] °C/W	R_{THJA}[b] °C/W	R_{THJC}[c] °C/W	R_{THJB}[d] °C/W
Natural	57.1	24.9	15.8	9.7
100	50.0	21.3		
200	46.9	20.0		
400	43.4	18.7		
800	38.6	16.9		

a. Junction to ambient, single layer test board, per JESD51-6
b. Junction to ambient, four conductor layer test board (2S2P), per JES51-6
c. Junction to case, per MIL-SPEC 883E, method 1012.1
d. Junction to board, four conductor layer test board (2S2P) per JESD 51-8

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100EP223 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals.

OUTLINE DIMENSIONS

TC SUFFIX
PLASTIC LQFP PACKAGE, EXPOSED PAD
CASE 840K–01
ISSUE O



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 mm.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	—	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
D	12.00 BSC	
D1	10.00 BSC	
e	0.50 BSC	
E	12.00 BSC	
E1	10.00 BSC	
L	0.45	0.75
L1	1.00 REF	
R1	0.08	—
R2	0.08	—
S	0.20	—
F	6.00	7.00
G	6.00	7.00
Z	0 °	7 °
Z1	0 °	—
Z2	11 °	13 °
Z3	11 °	13 °

NOTES

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