# 512KB and 1MB BurstRAM™ Secondary Cache Modules for PowerPC™ PReP/CHRP Platforms

**MPC2105A**
**MPC2106A**
**MPC2105B**
**MPC2106B**

The MPC2105A/B and the MPC2106A/B are designed to provide burstable, high performance L2 cache for the PowerPC 60x microprocessor family in conformance with the PowerPC Reference Platform (PReP) and the PowerPC Common Hardware Reference Platform (CHRP) specifications.

The MPC2105A/B and MPC2106A/B utilize synchronous BurstRAMs. The modules are configured as 64K x 72, and 128K x 72 bits in a 178 (89 x 2) pin DIMM format. The MPC2105A/B uses four of the 3 V 64K x 18; the MPC2106A/B uses eight of the 3 V 64K x 18. For tag bits, a 5 V cache tag RAM configured as 16K x 12 for tag field plus 16K x 2 for valid and dirty status bits is used.

Bursts can be initiated with the ADS signal. Subsequent burst addresses are generated internal to the BurstRAM by the CNTEN signal.

Write cycles are internally self timed and are initiated by the rising edge of the clock (CLKx) inputs. Eight write enables are provided for byte write control.

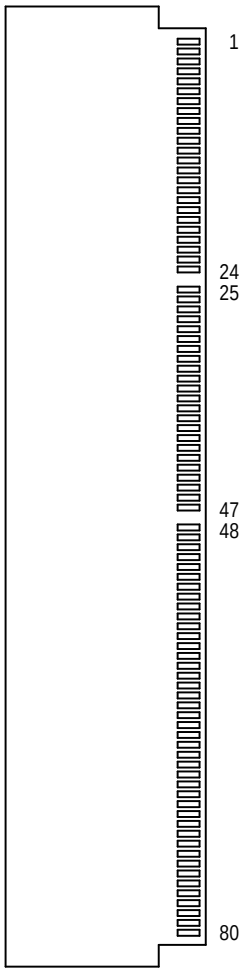
Presence detect pins are available for auto configuration of the cache control.

The module family pinout will support 5 V and 3.3 V components for a clear path to lower voltage and power savings. Both power supplies must be connected.

All of these cache modules are plug and pin compatible with each other.

- PowerPC–style Burst Counter on Chip
- Flow–Through Data I/O
- Plug and Pin Compatibility
- Multiple Clock Pins for Reduced Loading
- 20 Ω Series Resistors on DL and DH Pins for Noise Reduction (MPC2105A/6A)
- All Cache Data and Tag I/Os are LVTTL (3.3 V) Compatible
- Three State Outputs
- Byte Write Capability
- Fast Module Clock Rates: Up to 66 MHz
- Fast SRAM Access Times: 10 ns for Tag RAM Match
  9 ns for Data RAM
- Decoupling Capacitors for Each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- 178 Pin Card Edge Module
- Burndy Connector, Part Number: ELF178KSC–3Z50

**178–LEAD CARD EDGE**
**TOP VIEW**
**MPC2105A/B CASE 1132A–01**
**MPC2106A/B CASE 1132–01**

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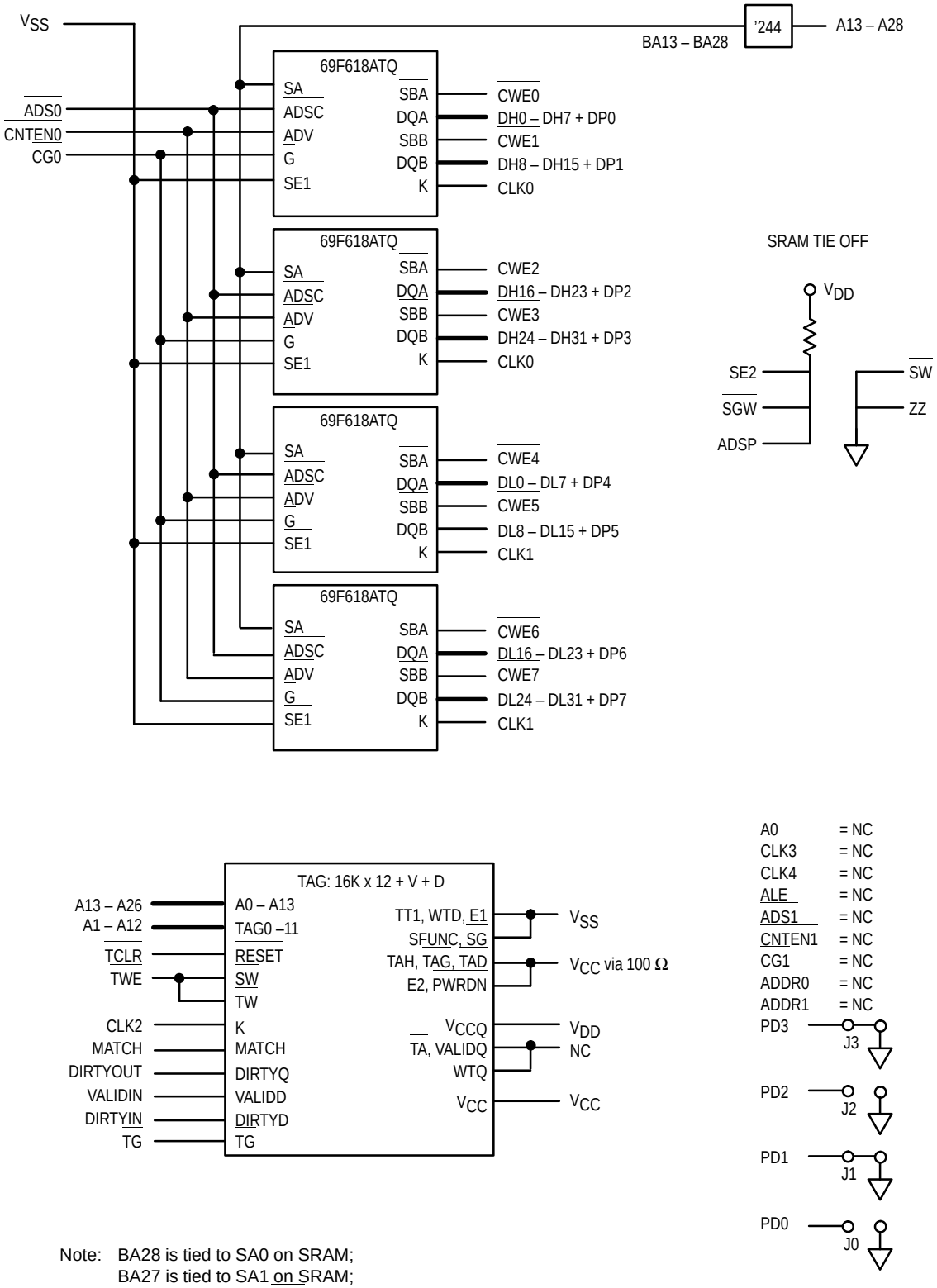
The PowerPC name is a trademark of IBM Corp., used under license therefrom.

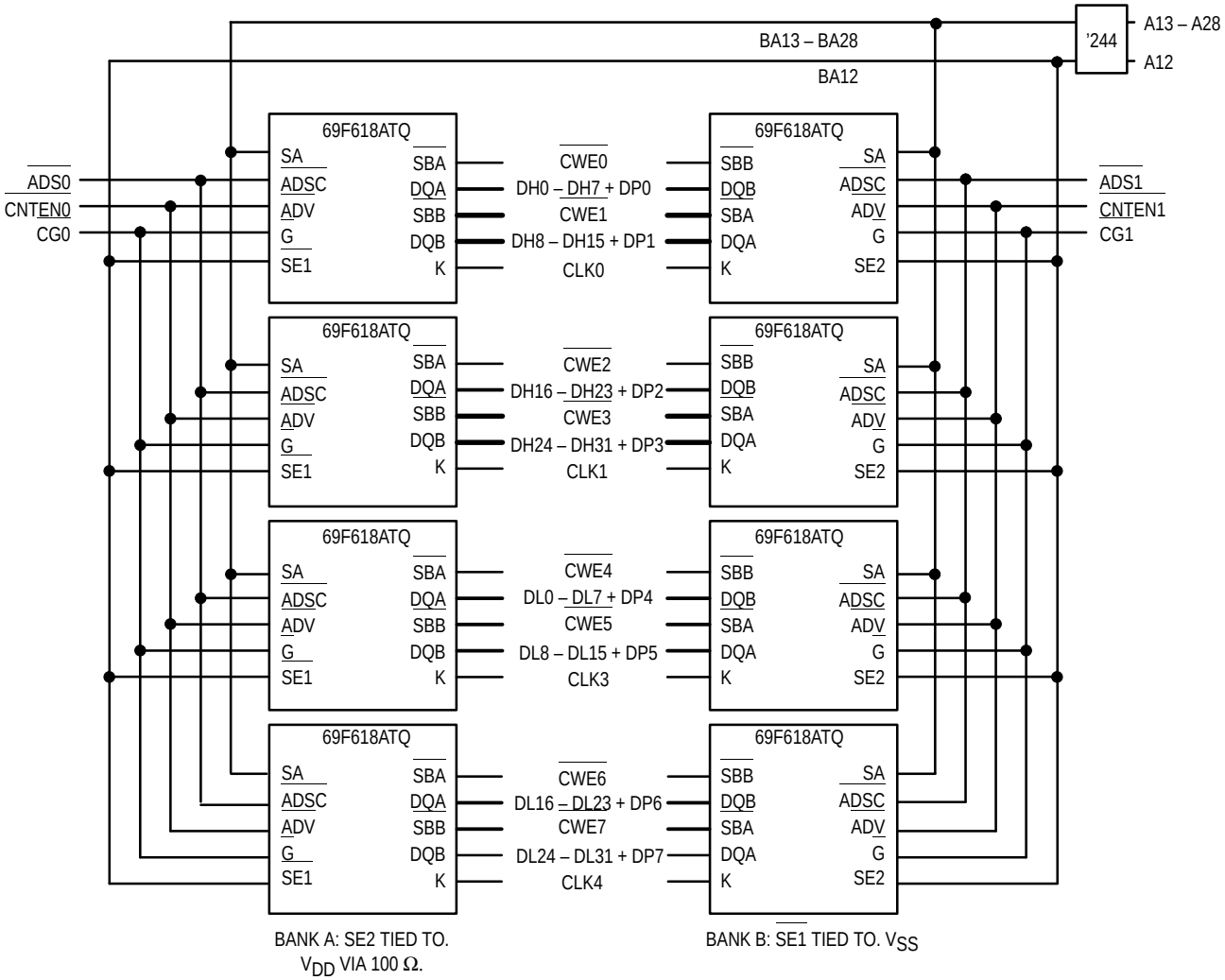
**REV 1**
**12/19/96**

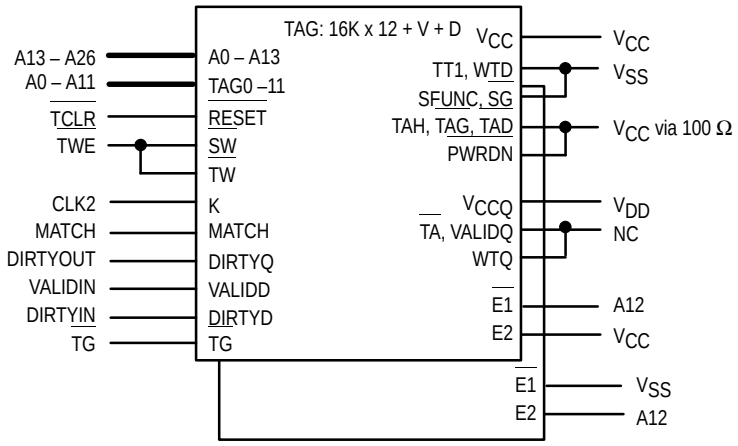
## MPC2105A/B BLOCK DIAGRAM




Note: BA28 is tied to SA0 on SRAM;
BA27 is tied to SA1 on SRAM;
STANDBY is tied to SE3 on SRAM.

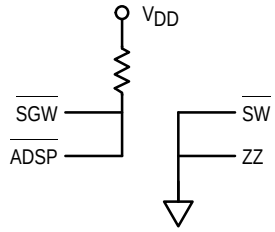
## MPC2106A/B BLOCK DIAGRAM



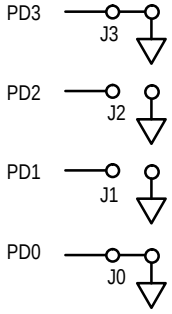




Note: BA28 is tied to SA0 on SRAM;
BA27 is tied to SA1 on SRAM;
STANDBY is tied to SE3 on SRAM.

SRAM TIE OFF




ALE = NC
ADDR0 = NC
ADDR1 = NC

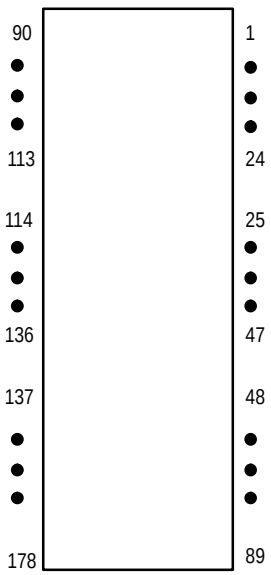


**PIN ASSIGNMENT 178–LEAD DIMM**

| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $V_{SS}$ | 27 | DH0 | 53 | DL1 | 79 | $V_{SS}$ | 105 | DH14 | 131 | DL17 | 157 | A22 |
| 2 | PD0/IDSCLK | 28 | DP0 | 54 | DL0 | 80 | A7 | 106 | DH13 | 132 | CWE6 | 158 | A20 |
| 3 | PD2 | 29 | $V_{SS}$ | 55 | $V_{SS}$ | 81 | A5 | 107 | $V_{CC}$ | 133 | DL15 | 159 | $V_{SS}$ |
| 4 | DH30 | 30 | CLK1 | 56 | CLK2 | 82 | A3 | 108 | DH10 | 134 | DL13 | 160 | A18 |
| 5 | DH28 | 31 | $V_{SS}$ | 57 | $V_{SS}$ | 83 | A0 | 109 | DH8 | 135 | $V_{SS}$ | 161 | A16 |
| 6 | DH26 | 32 | DL28 | 58 | DP4 | 84 | $V_{CC}$ | 110 | CWE1 | 136 | DL10 | 162 | A15 |
| 7 | DH24 | 33 | DL26 | 59 | $\overline{CG0}$ | 85 | TCLR | 111 | DH6 | 137 | DL8 | 163 | A14 |
| 8 | $V_{DD}$ | 34 | DL24 | 60 | $\overline{CG1}$ | 86 | MATCH | 112 | $V_{DD}$ | 138 | $\overline{CWE5}$ | 164 | $V_{DD}$ |
| 9 | DP3 | 35 | DP7 | 61 | $V_{DD}$ | 87 | $\overline{TG}$ | 113 | DH4 | 139 | DL6 | 165 | A10 |
| 10 | DH22 | 36 | $V_{CC}$ | 62 | ADDR0 | 88 | DIRTYIN | 114 | $V_{SS}$ | 140 | $V_{DD}$ | 166 | A8 |
| 11 | DH20 | 37 | DL22 | 63 | RESERVED | 89 | $V_{SS}$ | 115 | CLK0 | 141 | DL5 | 167 | A6 |
| 12 | DH19 | 38 | DL20 | 64 | ADS0 | 90 | $V_{SS}$ | 116 | $V_{SS}$ | 142 | DL2 | 168 | $V_{SS}$ |
| 13 | $V_{SS}$ | 39 | DL18 | 65 | ADS1 | 91 | PD1/IDSDATA | 117 | DH1 | 143 | $V_{SS}$ | 169 | A4 |
| 14 | DH17 | 40 | DL16 | 66 | A28 | 92 | PD3 | 118 | CWE0 | 144 | CLK3 | 170 | A2 |
| 15 | DP2 | 41 | $V_{SS}$ | 67 | A26 | 93 | DH31 | 119 | DL31 | 145 | $V_{SS}$ | 171 | A1 |
| 16 | DH15 | 42 | DP6 | 68 | A25 | 94 | DH29 | 120 | DL30 | 146 | CLK4 | 172 | BURSTMODE |
| 17 | DH12 | 43 | DL14 | 69 | A23 | 95 | DH27 | 121 | $V_{SS}$ | 147 | $V_{SS}$ | 173 | $V_{CC}$ |
| 18 | $V_{CC}$ | 44 | DL12 | 70 | $V_{SS}$ | 96 | DH25 | 122 | DL29 | 148 | CWE4 | 174 | VALIDIN |
| 19 | DH11 | 45 | DL11 | 71 | A21 | 97 | $V_{DD}$ | 123 | DL27 | 149 | ALE | 175 | $\overline{TWE}$ |
| 20 | DH9 | 46 | $V_{SS}$ | 72 | A19 | 98 | $\overline{CWE3}$ | 124 | DL25 | 150 | $V_{DD}$ | 176 | STANDBY |
| 21 | DP1 | 47 | DL9 | 73 | A17 | 99 | DH23 | 125 | $V_{CC}$ | 151 | ADDR1 | 177 | DIRTYOUT |
| 22 | DH7 | 48 | DP5 | 74 | A13 | 100 | DH21 | 126 | $\overline{CWE7}$ | 152 | RESERVED | 178 | $V_{SS}$ |
| 23 | $V_{DD}$ | 49 | DL7 | 75 | $V_{DD}$ | 101 | DH18 | 127 | DL23 | 153 | $\overline{CNTEN0}$ | | |
| 24 | DH5 | 50 | DL4 | 76 | A12 | 102 | $V_{SS}$ | 128 | DL21 | 154 | $\overline{CNTEN1}$ | | |
| 25 | DH3 | 51 | $V_{DD}$ | 77 | A11 | 103 | DH16 | 129 | DL19 | 155 | A27 | | |
| 26 | DH2 | 52 | DL3 | 78 | A9 | 104 | $\overline{CWE2}$ | 130 | $V_{SS}$ | 156 | A24 | | |

NOTE: $V_{CC}$ and $V_{DD}$ must be connected on all modules.

**TOP VIEW**



## PIN DESCRIPTIONS

| Pin Locations | Symbol | Type | Description |
|---|---|---|---|
| 66, 67, 68, 69, 71, 72, 73, 74, 76, 77, 78, 80, 81, 82, 83, 155, 156, 157, 158, 160, 161, 162, 163, 165, 166, 167, 169, 170, 171 | A0 – A28 | Input | Address Inputs – (MSB:0, LSB:28). |
| 62 | ADDR0 | Input | Least significant address bit when asynchronous Data RAMs are used. |
| 151 | ADDR1 | Input | Next to least significant address bit when asynchronous Data RAMs are used. |
| 64, 65 | $\overline{\text{ADS0}}$, $\overline{\text{ADS1}}$ | Input | Data RAM Address Strobe – For MPC2105A/B use $\overline{\text{ADS0}}$ only. For MPC2106A/B use $\overline{\text{ADS0}}$, $\overline{\text{ADS1}}$. |
| 149 | ALE | Input | Data RAM Address Latch Enable – Use for asynchronous Data RAM only. |
| 172 | BURSTMODE | Input | Burstmode. 0 = Linear, 1 = Interleaved. |
| 59, 60 | $\overline{\text{CG0}}$, CG1 | Input | Data RAM Output Enables – For MPC2105A/B use $\overline{\text{CG0}}$ only. For MPC2106A/B use $\overline{\text{CG0}}$, CG1. |
| 30, 56, 115, 144, 146 | CLK0 – CLK4 | Input | Clock Inputs – CLK2 is for Tag RAM, CLK0, 1, 3, and 4 are for Data RAMs only. For MPC2106A/B use all the clocks. For MPC2105A/B use CLK0 – CLK2 only. |
| 153, 154 | $\overline{\text{CNTEN0}}$, CNTEN1 | Input | Data RAM Count Enables – For MPC2105A/B use $\overline{\text{CNTEN0}}$ only. For MPC2106A/B use $\overline{\text{CNTEN0}}$, CNTEN1. |
| 98, 104, 110, 118, 126, 132, 138, 148 | CWE0 – CWE7 | Input | Data RAM Write Enables – (MSB:0, LSB:7). |
| 4, 5, 6, 7, 10, 11, 12, 14, 16, 17, 19, 20, 22, 24, 25, 26, 27, 93, 94, 95, 96, 99, 100, 101, 103, 105, 106, 108, 109, 111, 113, 117 | DH0 – DH31 | I/O | High Data Bus – (MSB:0, LSB:31). |
| 88 | DIRTYIN | Input | Dirty input bit. |
| 177 | DIRTYOUT | Output | Dirty output bit. |
| 32, 33, 34, 37, 38, 39, 40, 43, 44, 45, 47, 49, 50, 52, 53, 54, 119, 120, 122, 123, 124, 127, 128, 129, 131, 133, 134, 136, 137, 139, 141, 142 | DL0 – DL31 | I/O | Low Data Bus – (MSB:0, LSB:31). |
| 9, 15, 21, 28, 35, 42, 48, 58 | DP0 – DP7 | I/O | Data Parity Bits – (MSB:0, LSB:7) |
| 86 | MATCH | Output | Tag RAM active high match indication. |
| 2 | PD0/IDSCLK | Input | Presence detect bit 0/EEPROM serial clock. (EEPROM option only). |
| 91 | PD1/IDSDATA | I/O | Presence detect bit 1/EEPROM serial data. (EEPROM option only). |
| 3, 92 | PD2, PD3 | Output | Presence detect bits. |
| 63, 152 | RESERVED | | Reserved pin. |
| 176 | STANDBY | Input | Standby pin. Reduces standby power consumption. |
| 85 | $\overline{\text{TCLR}}$ | Input | Tag RAM clear. |
| 87 | $\overline{\text{TG}}$ | Input | Tag RAM output enable. |
| 175 | $\overline{\text{TWE}}$ | Input | Tag RAM write enable. |
| 174 | VALIDIN | Input | Tag RAM valid bit. |
| 18, 36, 84, 107, 125, 173 | $V_{CC}$ | Input | + 5 V power supply. Must be connected. |
| 8, 23, 51, 61, 75, 97, 112, 140, 150, 164 | $V_{DD}$ | Input | + 3.3 V power supply. Must be connected. |
| 1, 13, 29, 31, 41, 46, 55, 57, 70, 79, 89, 90, 102, 114, 116, 121, 130, 135, 143, 145, 147, 159, 168, 178 | $V_{SS}$ | Input | Ground. |

**DATA RAM MCM69F618A SYNCHRONOUS TRUTH TABLE** (See Notes 1, 2, and 3)

| STANDBY | ADSx | CNTENx | CWEx | CLKx | Address Used | Operation |
|---|---|---|---|---|---|---|
| H | L | X | X | L–H | N/A | Deselected |
| L | L | X | L | L–H | External Address | Write Cycle, Begin Burst |
| L | L | X | H | L–H | External Address | Read Cycle, Begin Burst |
| X | H | L | L | L–H | Next Address | Write Cycle, Continue Burst |
| X | H | L | H | L–H | Next Address | Read Cycle, Continue Burst |
| X | H | H | L | L–H | Current Address | Write Cycle, Suspend Burst |
| X | H | H | H | L–H | Current Address | Read Cycle, Suspend Burst |

NOTES:
1. X means Don't Care.
2. All inputs except CG must meet set–up and hold times for the low–to–high transition of clock (CLK0 – CLK4).
3. Wait states are inserted by suspending burst.

**ASYNCHRONOUS TRUTH TABLE** (See Notes 1 and 2)

| Operation | CG | I/O Status |
|---|---|---|
| Read | L | Data Out (DQ0 – DQ8) |
| Read | H | High–Z |
| Write | X | High–Z — Data In |
| Deselected | X | High–Z |

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{CG}$ must be high before the input data required set–up time and held high through the input data hold time.

**ABSOLUTE MAXIMUM RATINGS** (Voltages Referenced to $V_{SS}$ = 0 V)

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Power Supply Voltage | | $V_{CC}$ | – 0.5 to + 7.0 | V |
| Voltage Relative to $V_{SS}$ | | $V_{in}$, $V_{out}$ | – 0.5 to $V_{CC}$ + 0.5 | V |
| Output Current (per I/O) | Data RAM<br>Tag | $I_{out}$ | ± 30<br>± 20 | mA |
| Power Dissipation | MPC2105A/B<br>MPC2106A/B | $P_D$ | 4.6<br>9.2 | W |
| Temperature Under Bias | | $T_{bias}$ | – 10 to + 85 | °C |
| Operating Temperature | | $T_A$ | 0 to +70 | °C |
| Storage Temperature | | $T_{stg}$ | – 55 to + 125 | °C |

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}$ = 5.0 V ± 5%, $V_{DD}$ = 3.3 V ± 10%, $T_A$ = 0 to + 70°C, Unless Otherwise Noted)

**RECOMMENDED OPERATING CONDITIONS** (Voltages referenced to $V_{SS}$ = 0 V)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage (Operating Voltage Range) | $V_{CC}$<br>$V_{DD}$ | 4.75<br>3.00 | 5.25<br>3.60 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | $V_{DD}$ + 0.3** | V |
| Input Low Voltage | $V_{IL}$ | – 0.5* | 0.8 | V |

* $V_{IL}$ (min) = – 0.5 V dc; $V_{IL}$ (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** $V_{IH}$ (max) = $V_{DD}$ + 0.3 V dc; $V_{IH}$ (max) = $V_{DD}$ + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

**DC CHARACTERISTICS**

| Parameter | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input Leakage Current (All Inputs, $V_{in}$ = 0 to $V_{DD}$) | Data RAM<br>Tag | $I_{lkg(I)}$ | — | ± 1.0<br>± 5.0 | µA |
| Output Leakage Current (CG = $V_{IH}$, $V_{out}$ = 0 to $V_{DD}$) | Data RAM<br>Tag | $I_{lkg(O)}$ | — | ± 1.0<br>± 5.0 | µA |
| TTL Output Low Voltage ($I_{OL}$ = + 8.0 mA) | | $V_{OL}$ | — | 0.4 | V |
| TTL Output High Voltage ($I_{OH}$ = – 4.0 mA) | | $V_{OH}$ | 2.4 | — | V |

**POWER SUPPLY CURRENTS**

| Parameter | | Symbol | Max | Unit |
|---|---|---|---|---|
| AC Supply Current (CG = $V_{IH}$, E = $V_{IL}$, $I_{out}$ = 0 mA, All Inputs = $V_{IL}$ and $V_{IH}$, $V_{IL}$ = 0.0 V and $V_{IH}$ ≥ 3.0 V, Cycle Time ≥ 20 ns) | MPC2105A/B<br>MPC2106A/B | $I_{DDA}$ | 900<br>1800 | mA |
| | MPC2105A/B<br>MPC2106A/B | $I_{CCA}$ | 320<br>640 | mA |
| AC Standby Current (E = $V_{IH}$, $I_{out}$ = 0 mA, All Inputs = $V_{IL}$ or $V_{IH}$ $V_{IL}$ = 0.0 V and $V_{IH}$ ≥ 3.0 V, Cycle Time ≥ 20 ns) | MPC2105A/B<br>MPC2106A/B | $I_{SB1}(V_{DD})$ | 440<br>880 | mA |
| | MPC2105A/B<br>MPC2106A/B | $I_{SB1}(V_{CC})$ | 320<br>640 | mA |

**CAPACITANCE** (f = 1.0 MHz, dV = 3.0 V, $T_A$ = 25°C, Periodically Sampled Rather Than 100% Tested)

| Parameter | | Symbol | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Capacitance | (A13 – A28)<br>(Data RAM Control Pins)<br>(CLK0 – CLK4)<br>(Tag Control Pins) | $C_{in}$ | —<br>16<br>8<br>— | 15<br>20<br>10<br>5 | pF |
| Tag Output Capacitance | (MATCH, DIRTYOUT) | $C_{out}$ | — | 7 | pF |
| Data RAM Input/Output Capacitance | (DH0 – DH31, DL0 – DL31) | $C_{I/O}$ | 6 | 8 | pF |
| Tag Input/Output Capacitance | (A0 – A11) | $C_{I/O}$ | — | 7 | pF |

## DATA RAMs AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}$ = 5.0 V ± 5%, $V_{DD}$ = 3.3 V ± 10% $T_A$ = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

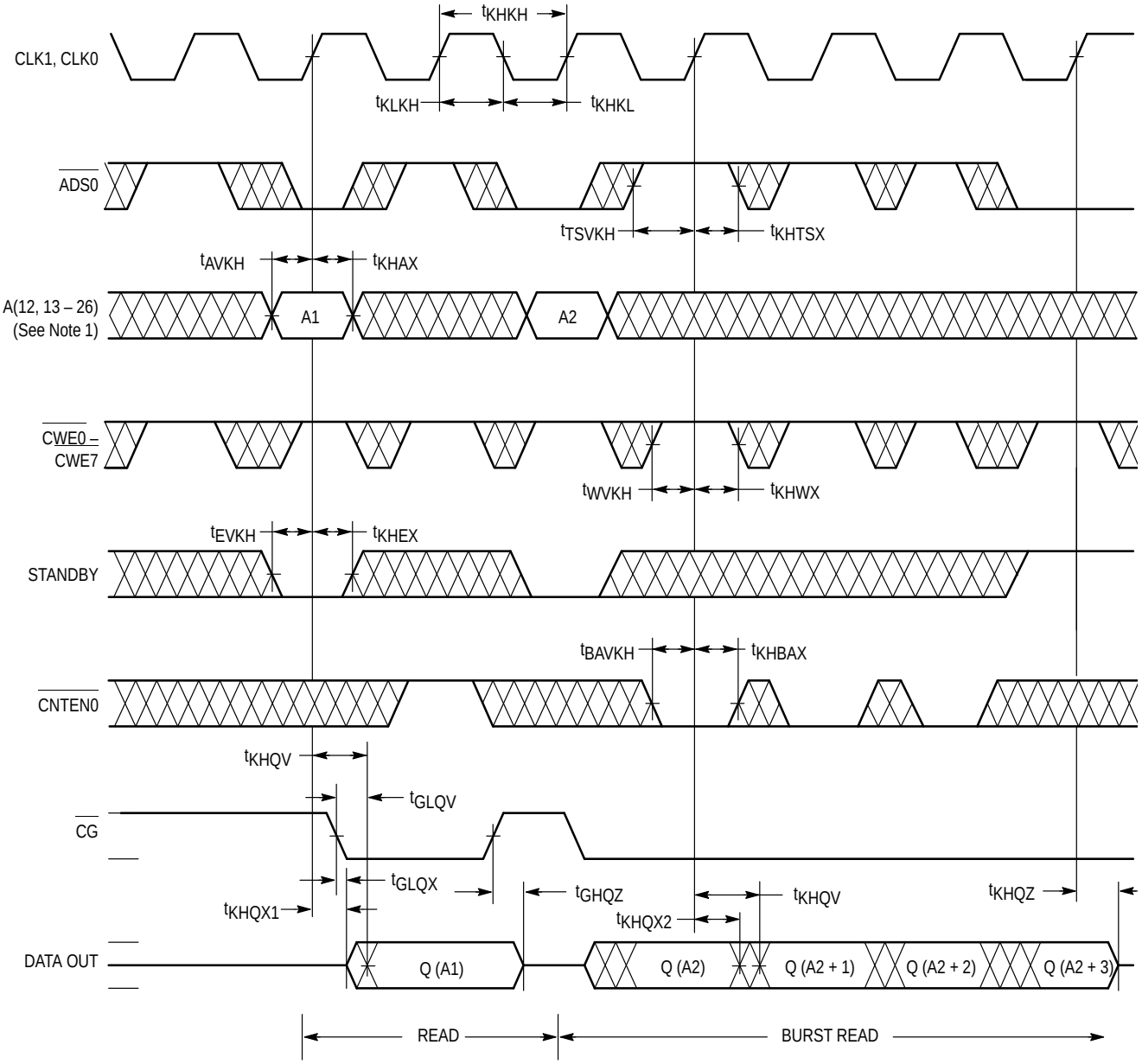
Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1a Unless Otherwise Noted

**SYNCHRONOUS DATA RAMs READ/WRITE CYCLE TIMING** (See Notes 1, 2, and 3)

| Parameter | Symbol | MPC2105A/B MPC2106A/B | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Cycle Time | $t_{KHKH}$ | 15 | — | ns | |
| Clock Access Time | $t_{KHQV}$ | — | 9 | ns | 4 |
| Output Enable to Output Valid | $t_{GLQV}$ | — | 5 | ns | |
| Clock High to Output Active | $t_{KHQX1}$ | 6 | — | ns | |
| Clock High to Output Change | $t_{KHQX2}$ | 3 | — | ns | |
| Output Enable to Output Active | $t_{GLQX}$ | 0 | — | ns | |
| Output Disable to Q High–Z | $t_{GHQZ}$ | 2 | 6 | ns | |
| Clock High to Q High–Z | $t_{KHQZ}$ | — | 6 | ns | |
| Clock High Pulse Width | $t_{KHKL}$ | 5 | — | ns | |
| Clock Low Pulse Width | $t_{KLKH}$ | 5 | — | ns | |
| Setup Time — Address | $t_{AVKH}$ | 7.5 | — | ns | 5, 6 |
| Setup Times: — Address Status<br>Data In<br>Write<br>Address Advance<br>Chip Enable | $t_{SVKH}$<br>$t_{DVKH}$<br>$t_{WVKH}$<br>$t_{BAVVKH}$<br>$t_{EVKH}$ | 2.5 | — | ns | 5 |
| Hold Times: — Address<br>Address Status<br>Data In<br>Write<br>Address Advance<br>Chip Enable | $t_{KHAX}$<br>$t_{KHTSX}$<br>$t_{KHDX}$<br>$t_{KHWX}$<br>$t_{KHBAX}$<br>$t_{KHEX}$ | 0.5 | — | ns | 5 |

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. All read and write cycle timings are referenced from CLK or CG.
3. CG is a don't care when UW or LW is sampled low.
4. Maximum access times are guaranteed for all possible PowerPC external bus cycles.
5. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of CLK whenever $\overline{TSP}$ or TSC is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of CLK when the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when TSP or TSC is low) to remain enabled.
6. 5 ns of setup delay is incurred in address buffers.

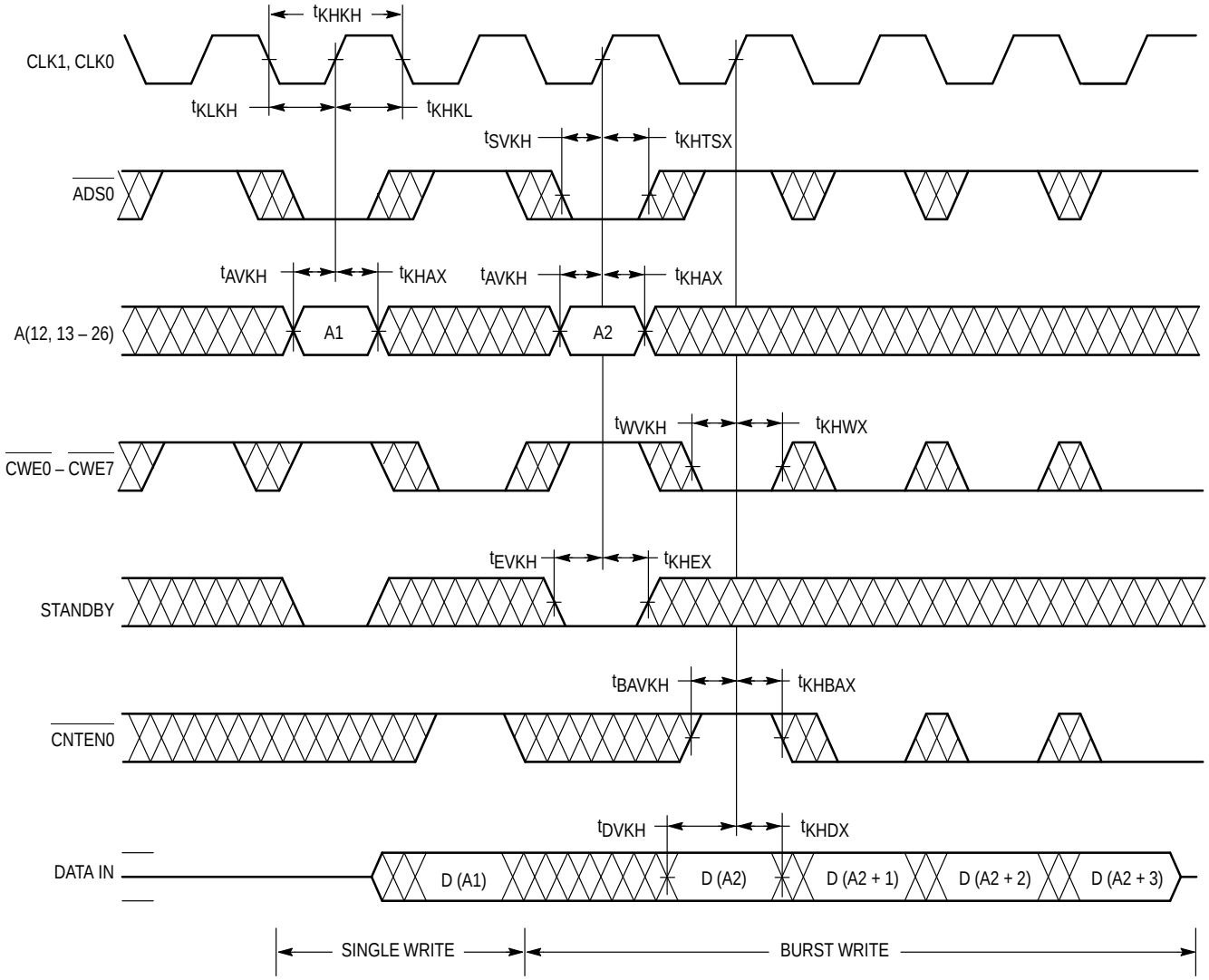
## SYNCHRONOUS DATA RAM READ CYCLE




NOTES:

1. Cache addresses used are: 13 – 26 for MPC2105A/B; and 12 – 26 for MPC2106A/B.
2. Q1 (A2) represents the first ouput from the external address A2; Q2 (A2) represents the next output data in the burst sequence with A2 as the base address.

## SYNCHRONOUS DATA RAM WRITE CYCLE




NOTES:
1. Cache addresses used are: 13 – 26 for MPC2105A/B; and 12 – 26 for MPC2106A/B.
2. CG0 = $V_{IH}$

**RESET FUNCTION TRUTH TABLE** (See Notes 1 and 2)

| TCLR | CLK | TWE | TAG0 – TAG11 | DIRTYOUT | MATCH | Operation | POWER |
|---|---|---|---|---|---|---|---|
| L | L – H | H | High–Z | L(3) | L(3) | Reset Status | Active |
| L | L – H | L | — | — | — | Not Allowed | — |

NOTES:
1. H = $V_{IH}$, L = $V_{IL}$, X = don't care, — = undefined.
2. TG is X for this table.
3. These are output states.

**READ FUNCTION TRUTH TABLE** (See Notes 1, 2, and 3)

| TG | TWE | CLK | TAG0 – TAG11 | VALIDIN | DIRTYIN | DIRTYOUT | MATCH | Operation |
|---|---|---|---|---|---|---|---|---|
| L | H | X | $D_{out}$ | — | — | $D_{out}$ | $D_{out}$ | Read Tag I/O |
| H | X | X | High–Z | — | — | — | — | Tag I/O Disable |

**WRITE FUNCTION TRUTH TABLE** (See Notes 1 and 2)

| TG | TWE | CLK | TAG0 – TAG11 | VALIDIN | DIRTYIN | DIRTYOUT | MATCH | Operation |
|---|---|---|---|---|---|---|---|---|
| H | L | L – H | $D_{in}$ | — | — | — | L | Write Tag I/O |
| L | L | L – H | — | — | — | — | — | Not Allowed |

NOTES:
1. H = $V_{IH}$, L = $V_{IL}$, X = don't care, — = undefined.
2. This table applies when RESET and PWRDN are high.
3. $D_{out}$ in this case is the same as $D_{in}$. The input data is written through to the outputs during the write operation.

**MATCH FUNCTION TRUTH TABLE** (See Notes 1 through 4)

| TG | TWE | TAG0 – TAG11 | VALIDIN(4) | DIRTYIN(4) | MATCH | Operation |
|---|---|---|---|---|---|---|
| X | X | — | — | — | $D_{out}$ | Selected |
| L | H | $D_{out}$ | — | — | L | Read Tag I/O |
| H | L | $D_{in}$ | $D_{in}$ | $D_{in}$ | L | Write Tag I/O, Status Bits |
| H | H | $TAG_{in}$ | L | — | L | Invalid Data – Dedicated Status Bits |
| H | H | $TAG_{in}$ | H | — | H | Match – Dedicated Status Bits |

NOTES:
1. H = $V_{IH}$, L = $V_{IL}$, X = don't care, — = undefined.
2. M = high if $TAG_{in}$ equals the memory contents at the address; M = low if $TAG_{in}$ does not equal the contents at that address.
3. PWRDN and RESET are high for this table. GS and CLK are X.
4. This column represents the stored memory cell data for the given status bit at the selected address.

## TAG RAM AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}$ = 5.0 V ± 5%, $T_A$ = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1a Unless Otherwise Noted

**TAG RAM READ CYCLE** (See Notes 1 through 4)

| Parameter | Symbol | Tag RAM | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Clock Access Time | $t_{KHQV}$ | — | 10 | ns |
| Output Enable to Output Valid | $t_{GLQV}$ | — | 8 | ns |
| Output Enable to Output Active | $t_{GLQX}$ | 0 | — | ns |
| Output Disable to Q High–Z | $t_{GHQZ}$ | 1 | 6 | ns |
| Status Bit Hold from Address Change | $t_{AXSX}$ | 3 | — | ns |
| Address Access Time Status Bits | $t_{AVSV}$ | — | 10 | ns |
| Tag Bit Hold from Address Change | $t_{AVQX}$ | 3 | — | ns |
| Address Access Time Tag Bits | $t_{AVQV}$ | — | 12 | ns |

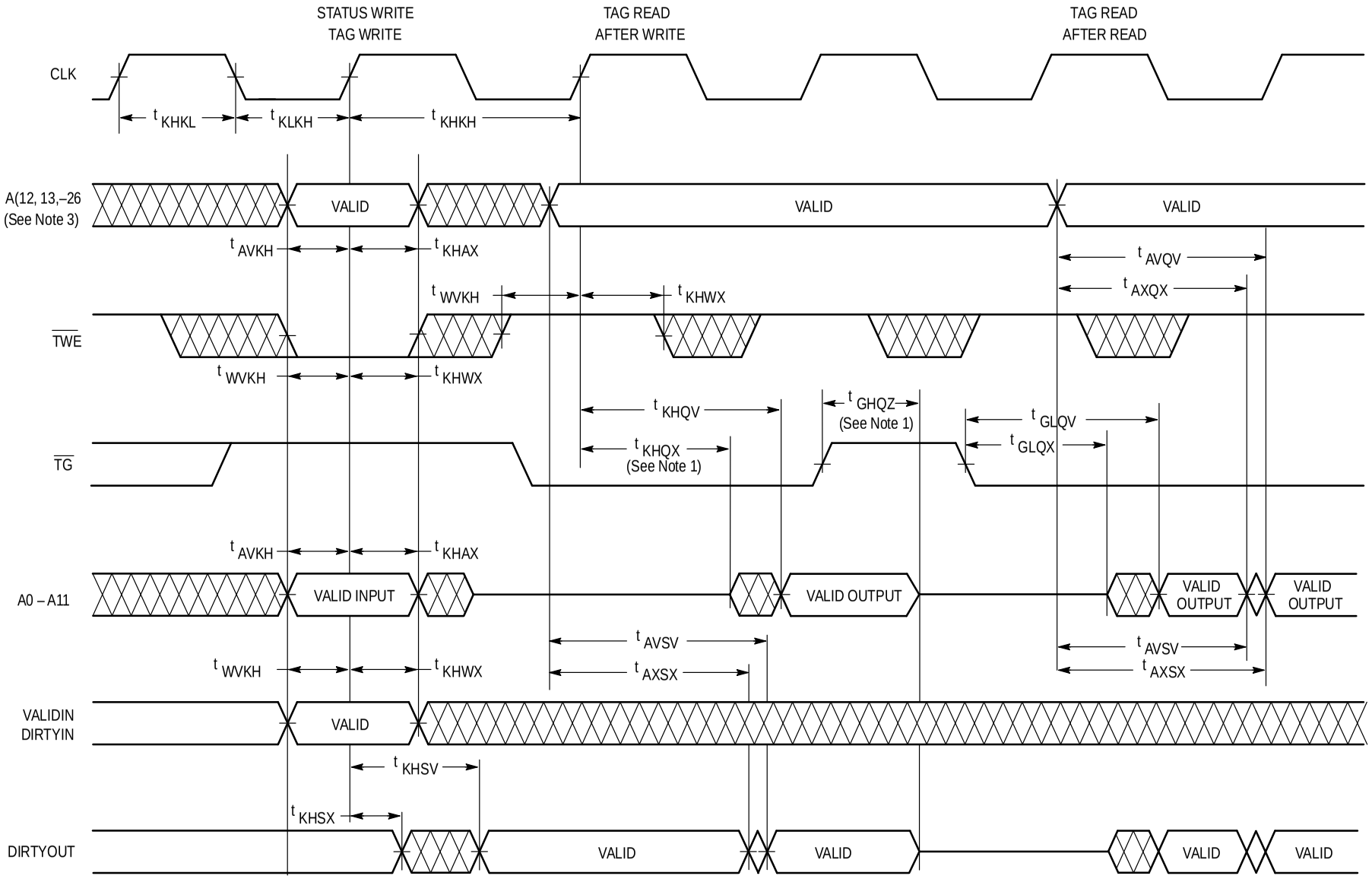
NOTES:
1. Setup and hold times, W (write) refers to $\overline{TWE}$.
2. A read cycle is defined by TWE high. A write cycle is defined by $\overline{TWE}$ low.
3. Maximum access times are guaranteed for all possible MC68040 and PowerPC external bus cycles.
4. Tag reads are asynchronous.

**TAG RAM WRITE CYCLE** (See Notes 1 through 4)

| Parameter | Symbol | Tag RAM | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Cycle Time | $t_{KHKH}$ | 15 | — | ns |
| Clock High Pulse Width | $t_{KHKL}$ | 4.5 | — | ns |
| Clock Low Pulse Width | $t_{KLKH}$ | 4.5 | — | ns |
| Clock High to Output Active | $t_{KHQX}$ | 1.5 | — | ns |
| Setup Times Address<br>Write | $t_{AVKH}$<br>$t_{WVKH}$ | 3 | — | ns |
| Hold Times Address<br>Write | $t_{KHAX}$<br>$t_{KHWX}$ | 1.5 | — | ns |
| Status Output Hold | $t_{KHSX}$ | 0 | — | ns |
| Clock High to Status Bits Valid | $t_{KHSV}$ | — | 9 | ns |

NOTES:
1. Setup and hold times, W (write) refers to $\overline{TWE}$.
2. A read cycle is defined by TWE high. A write cycle is defined by $\overline{TWE}$ low.
3. Maximum access times are guaranteed for all possible MC68040 and PowerPC external bus cycles.
4. Tag writes are synchronous.

## TAG RAM WRITE AND READ CYCLES (See Note 2)




NOTES:

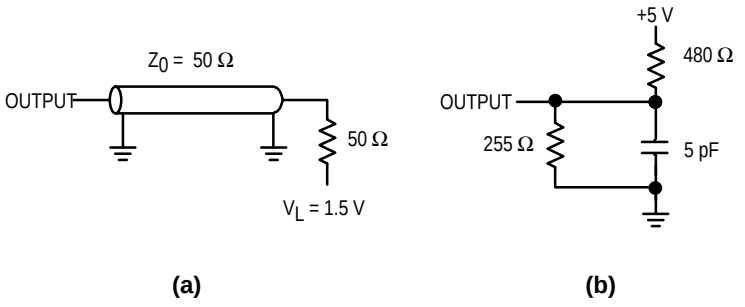
1. Transition is measured plus or minus 200 mV from steady state.
2. $\overline{TCLR}$ = High.
3. Cache addresses used are: A13 – 26 for MPC2105A, A12 – 26 for MPC2106A.

**TAG RAM MATCH CYCLE**

| Parameter | Symbol | Tag RAM | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Clock High Write to MATCH Invalid | $t_{KHML}$ | — | 7 | ns |
| Clock High Read to MATCH Valid | $t_{KHMV}$ | — | 10 | ns |
| Address Valid to MATCH Valid | $t_{AVMV}$ | — | 10 | ns |
| MATCH Valid Hold from Address Change | $t_{AXMX}$ | 2 | — | ns |
| TG Low to MATCH Invalid | $t_{GLML}$ | — | 7 | ns |
| TG High to MATCH Valid | $t_{GHMX}$ | — | 8 | ns |

**TAG RAM RESET ($\overline{\text{TCLR}}$) CYCLE**

| Parameter | Symbol | Tag RAM | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| TCLR Setup Time | $t_{STC}$ | 4 | — | ns |
| TCLR Hold Time | $t_{HTC}$ | 1 | — | ns |
| Status Bit Reset Time | $t_{SRST}$ | — | 60 | ns |
| Status Bit Hold from TCLR Low | $t_{SHRS}$ | 2 | — | ns |
| TCLR Low to MATCH Invalid | $t_{RSML}$ | — | 10 | ns |
| TCLR High to MATCH Valid | $t_{RSMV}$ | — | 100 | ns |
| TCLR Low to TAG High–Z | $t_{RSQZ}$ | — | 10 | ns |
| TCLR High to TAG Active | $t_{RSQX}$ | — | 100 | ns |
| STANDBY Setup to TCLR Low | $t_{PDSR}$ | 30 | — | ns |
| TCLR High to TWE Low | $t_{RHWX}$ | 80 | — | ns |



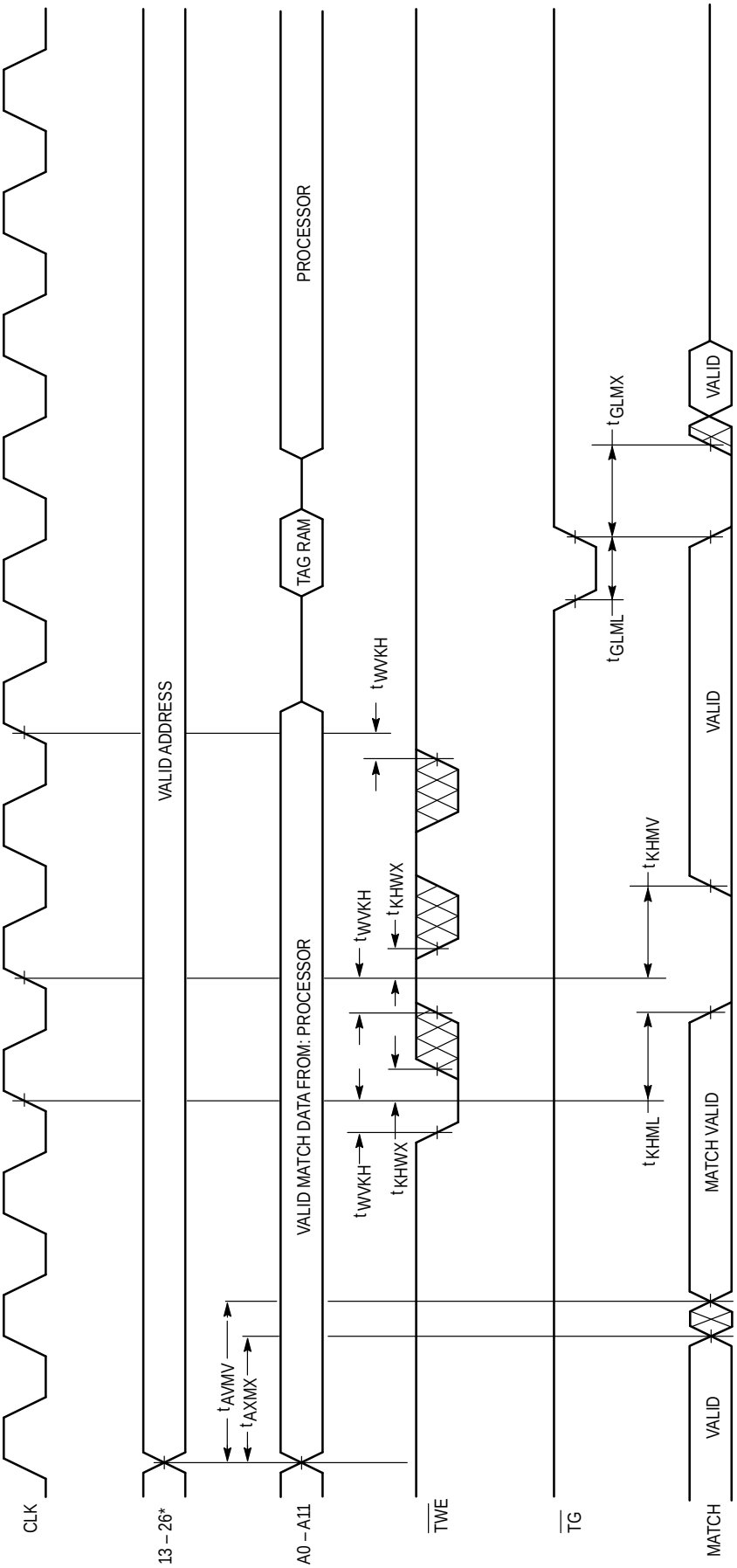

**(a)** **(b)**

**Figure 1. Test Loads**

## TIMING LIMITS

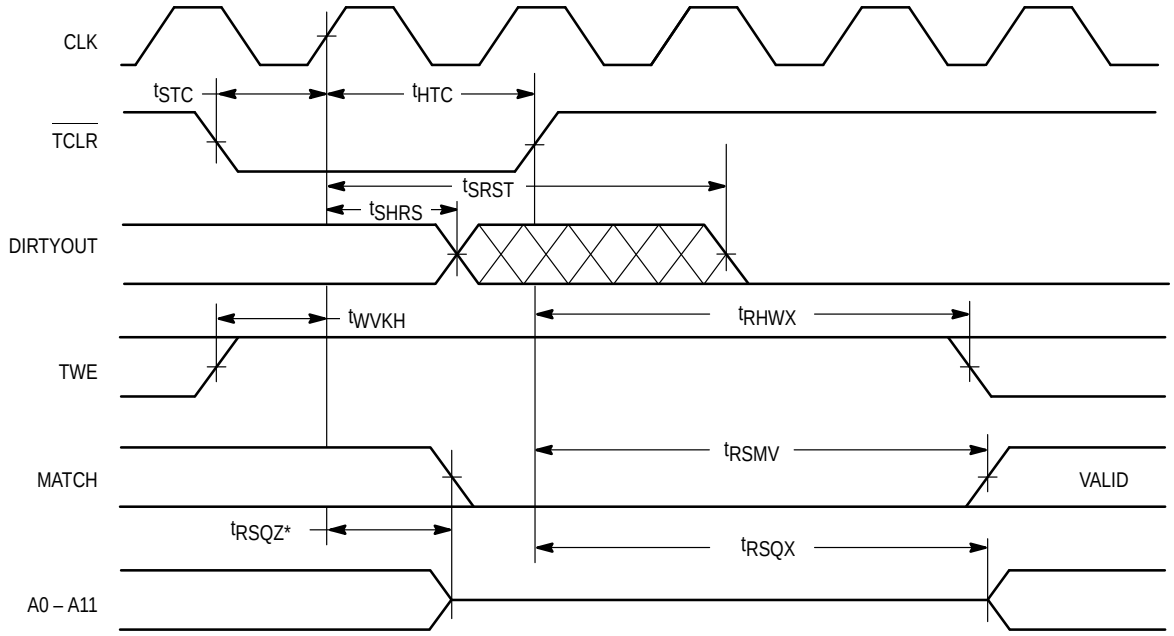
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

**TAG RAM MATCH CYCLE**



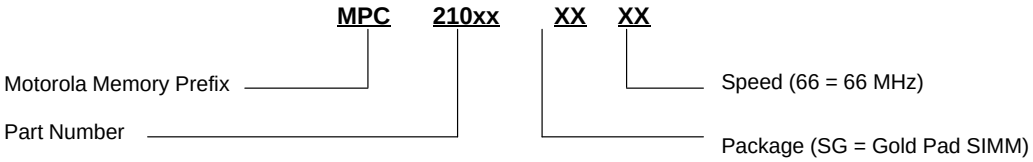

* Cache addresses used are: A13 –26 for MPC2105A, A12 – 26 for MPC2106A.

## TAG RAM $\overline{\text{TCLR}}$ FUNCTION




* Transition is measured plus or minus 200 mV from steady state.

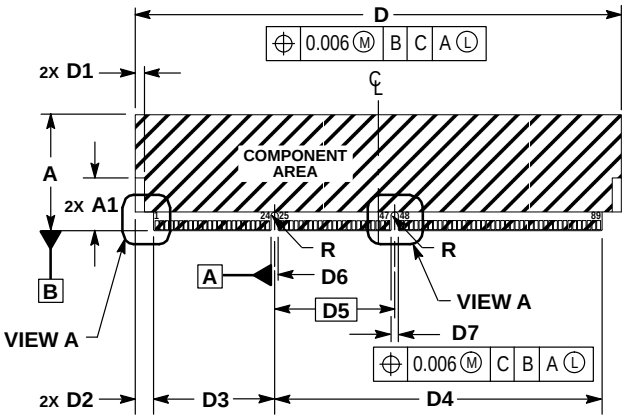
## ORDERING INFORMATION
**(Order by Full Part Number)**



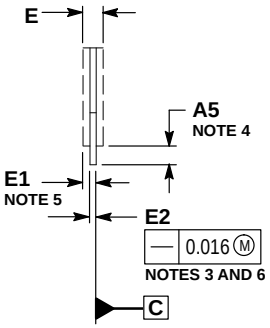

| | | |
|---|---|---|
| Full Part Numbers — | MPC2105ASG66 | MPC2105A = 512KB, synchronous, series resistors |
| | MPC2106ASG66 | MPC2106A = 1MB, synchronous, series resistors |
| | MPC2105BSG66 | MPC2105B = 512KB, synchronous |
| | MPC2106BSG66 | MPC2106B = 1MB, synchronous |

## PACKAGE DIMENSIONS

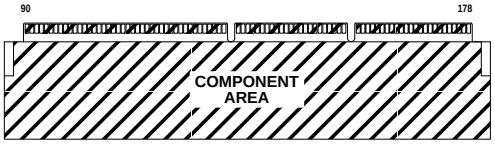
**178 LEAD CARD EDGE**
**MPC2105A/B**
**CASE 1132A–01**



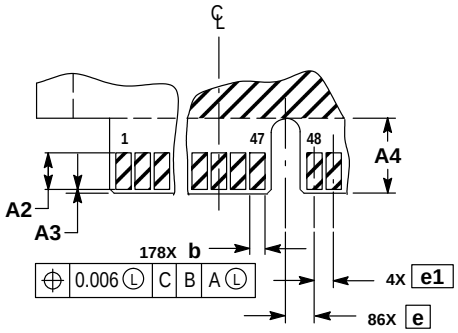

FRONT VIEW




SIDE VIEW




BACK VIEW

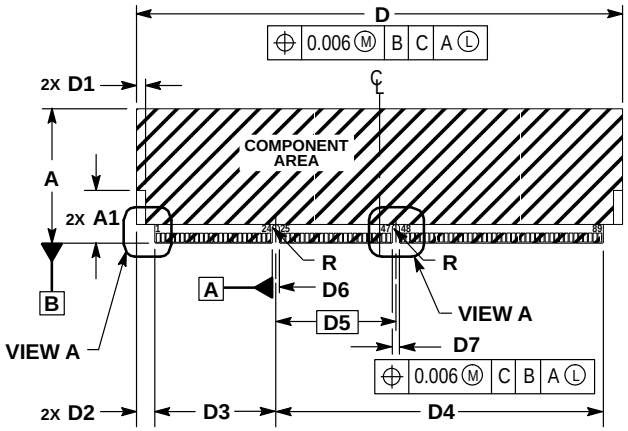



VIEW A

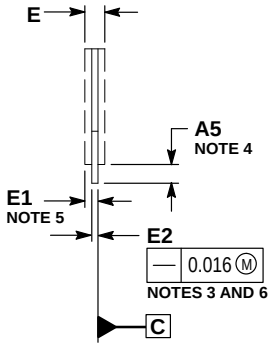
NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN INCHES.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.
4. DIMENSIONS E AND A5 DEFINE A DOUBLE–SIDED MODULE.
5. DIMENSION E1 DEFINES OPTIONAL SINGLE–SIDED MODULE.
6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.

| | INCHES | |
|---|---|---|
| DIM | MIN | MAX |
| A | 1.190 | 1.210 |
| A1 | 0.545 | — |
| A2 | 0.095 | — |
| A3 | — | 0.010 |
| A4 | 0.195 | — |
| A5 | 0.195 | — |
| b | 0.039 | 0.043 |
| D | 5.055 | 5.065 |
| D1 | 0.100 | — |
| D2 | 0.190 | — |
| D3 | 1.255 | 1.265 |
| D4 | 3.405 | 3.410 |
| D5 | 1.250 BSC | |
| D6 | 0.072 | 0.076 |
| D7 | 0.075 | 0.081 |
| e | 0.050 BSC | |
| e1 | 0.075 BSC | |
| E | — | 0.210 |
| E1 | — | 0.140 |
| E2 | 0.055 | 0.070 |

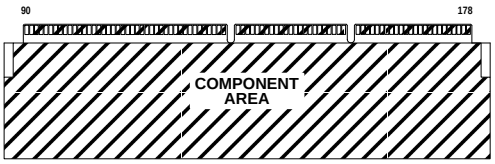
**178 LEAD CARD EDGE**
**MPC2106A/B**
**CASE 1132–01**



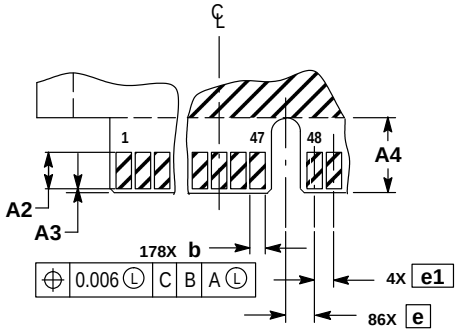

FRONT VIEW




SIDE VIEW




BACK VIEW




VIEW A

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6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.

| | INCHES | |
|---|---|---|
| DIM | MIN | MAX |
| A | 1.390 | 1.410 |
| A1 | 0.545 | — |
| A2 | 0.095 | — |
| A3 | — | 0.010 |
| A4 | 0.195 | — |
| A5 | 0.195 | — |
| b | 0.039 | 0.043 |
| D | 5.055 | 5.065 |
| D1 | 0.100 | — |
| D2 | 0.190 | — |
| D3 | 1.255 | 1.265 |
| D4 | 3.405 | 3.410 |
| D5 | 1.250 BSC | |
| D6 | 0.072 | 0.076 |
| D7 | 0.075 | 0.081 |
| e | 0.050 BSC | |
| e1 | 0.075 BSC | |
| E | — | 0.210 |
| E1 | — | 0.140 |
| E2 | 0.055 | 0.070 |

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