Advance Information

MPC7410EC/D
Rev. 1, 1/2002

MPC7410 RISC
Microprocessor
Hardware Specifications

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The MPC7410 is a reduced instruction set computing (RISC) microprocessor that implements the PowerPC instruction set architecture. This document describes pertinent electrical and physical characteristics of the MPC7410. For functional characteristics of the processor, refer to the *MPC7410 RISC Microprocessor User's Manual*.

This document contains the following topics:

To locate updates for this document, refer to the website at http://www.motorola.com/semiconductors.

1.1 Overview

The MPC7410 is the second implementation of the fourth generation (G4) microprocessors from Motorola. The MPC7410 implements the full PowerPC 32-bit architecture and is targeted at both computing and embedded systems applications.

Some comments on the MPC7410 with respect to MPC750:

- The MPC7410 adds an implementation of the new AltiVec™ technology instruction set
- The MPC7410 includes significant improvements in memory subsystem (MSS) bandwidth and offers an optional, high-bandwidth MPX bus interface
- The MPC7410 adds full hardware-based multiprocessing capability, including a five-state cache coherency protocol (four MESI states plus a fifth state for shared intervention)

- The MPC7410 is implemented in a next generation process technology for core frequency improvement
- The MPC7410 floating-point unit has been improved to make latency equal for -precision and single-precision operations involving multiplication
- The completion queue has been extended to eight slots
- There are no other significant changes to scalar pipelines, decode/dispatch/completion mechanisms, or the branch unit. The MPC750 four-stage pipeline model is unchanged (fetch, decode/dispatch, execute, complete/writeback)

Some comments on the MPC7410 with respect to MPC7400:

- The MPC7410 adds configurable direct mapped SRAM capability to the L2 cache interface
- The MPC7410 adds 32-bit interface support to the L2 cache interface. The MPC7410 implements a 19^{th} L2 address pin (L2ASPARE on the MPC7400) in order to support additional address range.
- The MPC7410 removes support for 3.3 V I/O on the L2 cache interface

Figure 1 shows a block diagram of the MPC7410.

1.2 Features

This section summarizes features of the MPC7410 implementation of the PowerPC architecture. Major features of the MPC7410 are as follows:

- Branch processing unit
  - — Four instructions fetched per clock
  - — One branch processed per cycle (plus resolving two speculations)
  - — Up to one speculative stream in execution, one additional speculative stream in fetch
  - — 512-entry branch history table (BHT) for dynamic prediction
  - — 64-entry, four-way set-associative branch target instruction cache (BTIC) for eliminating branch delay slots
- Dispatch unit
  - — Full hardware detection of dependencies (resolved in the execution units)
  - — Dispatch two instructions to eight independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, floating-point, AltiVec permute, AltiVec ALU)
  - — Serialization control (predispatch, postdispatch, execution serialization)
- Decode
  - — Register file access
  - — Forwarding control
  - — Partial instruction decode

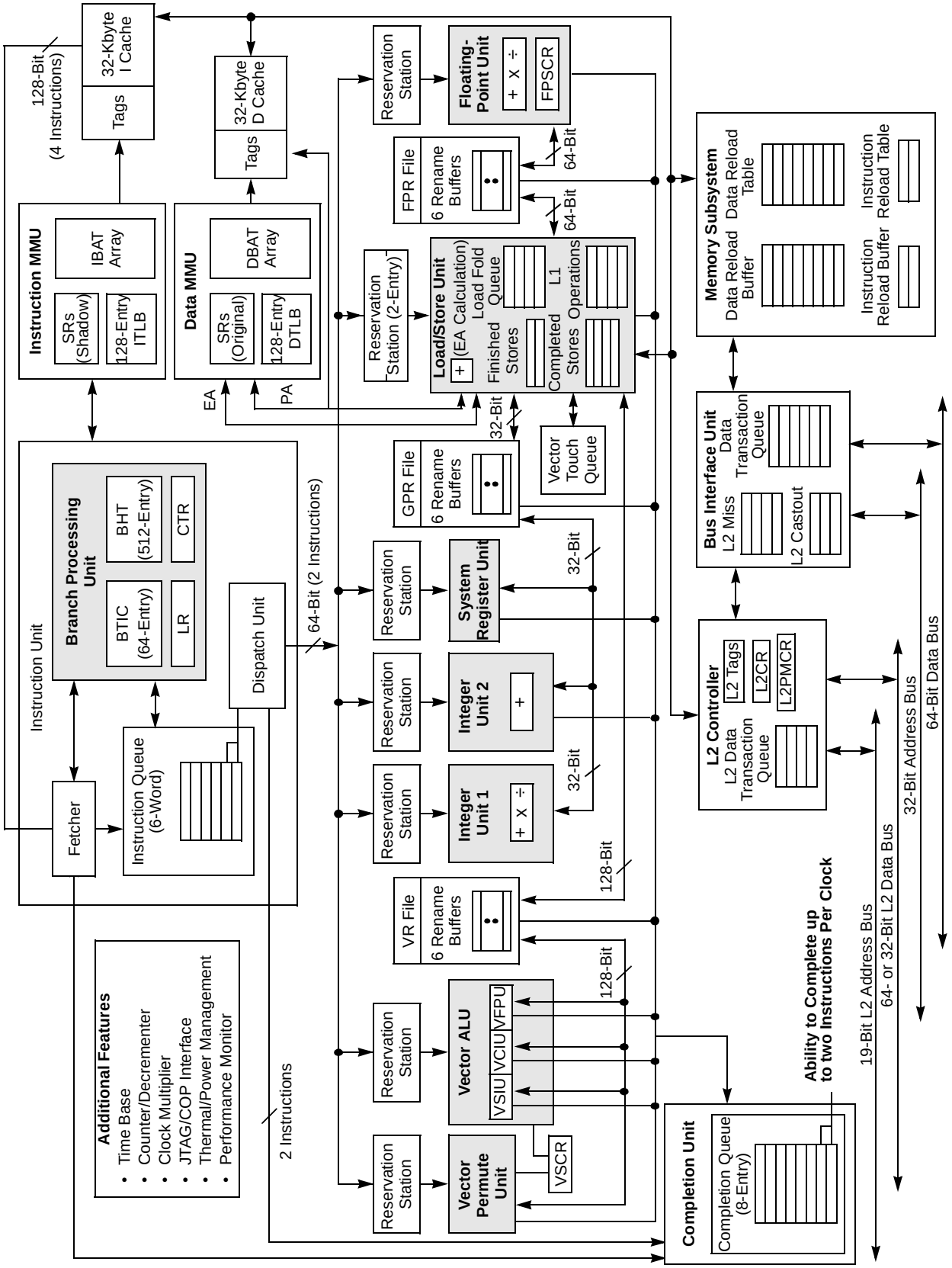


Figure 1. MPC7410 Block Diagram

- Completion
  - Eight-entry completion buffer
  - Instruction tracking and peak completion of two instructions per cycle
  - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization, and all instruction flow changes
- Fixed point units (FXUs) that share 32 GPRs for integer operands
  - Fixed point unit 1 (FXU1)—multiply, divide, shift, rotate, arithmetic, logical
  - Fixed point unit 2 (FXU2)—shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shifts, rotates, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
- Three-stage floating-point unit and a 32-entry FPR file
  - Support for IEEE-754 standard single- and double-precision floating-point arithmetic
  - Three-cycle latency, one-cycle throughput (single- or double-precision)
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Time deterministic non-IEEE mode
- System unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions
- AltiVec unit
  - Full 128-bit data paths
  - Two dispatchable units: vector permute unit and vector ALU unit.
  - Contains its own 32-entry 128-bit vector register file (VRF) with 6 renames
  - The vector ALU unit is further subdivided into the vector simple integer unit (VSIU), the vector complex integer unit (VCIU), and the vector floating-point unit (VFPU).
  - Fully pipelined
- Load/store unit
  - 1-cycle load or store cache access (byte, half word, word, double word)
  - 2-cycle load latency with 1-cycle throughput
  - Effective address generation
  - Hits under misses (multiple outstanding misses)
  - Single-cycle unaligned access within double-word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating-point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations
  - Store gathering
  - Executes the cache and TLB instructions

  - Big- and little-endian byte addressing supported
  - Misaligned little-endian supported
  - Supports FXU, FPU, and AltiVec load/store traffic
  - Complete support for all four architecture AltiVec DST streams
- Level 1 (L1) cache structure
  - 32K, 32-byte line, eight-way set-associative instruction cache (iL1)
  - 32K, 32-byte line, eight-way set-associative data cache (dL1)
  - Single-cycle cache access
  - Pseudo least-recently-used (LRU) replacement
  - Data cache supports AltiVec LRU and transient instructions algorithm
  - Copy-back or write-through data cache (on a page-per-page basis)
  - Supports all PowerPC memory coherency modes
  - Nonblocking instruction and data cache
  - Separate copy of data cache tags for efficient snooping
  - No snooping of instruction cache except for ICBI instruction
- Level 2 (L2) cache interface
  - Internal L2 cache controller and tags; external data SRAMs
  - 512-K, 1-M, and 2-Mbyte two-way set-associative L2 cache support
  - Copy-back or write-through data cache (on a page basis, or for all L2)
  - 32-byte (512-K), 64-byte (1-M), or 128-byte (2-M) sectored line size
  - Supports pipelined (register-register) synchronous BurstRAMs and pipelined (register-register) late write synchronous BurstRAMs
  - Supports direct-mapped mode for 256-K, 512-K, 1-M, or 2-Mbyte of SRAM (either all, half, or none of L2 SRAM must be configured as direct-mapped)
  - Core-to-L2 frequency divisors of ÷1, ÷1.5, ÷2, ÷2.5, ÷3, ÷3.5, and ÷4 supported
  - 64-bit data bus which also supports 32-bit bus mode
  - Selectable interface voltages of 1.8 V and 2.5 V
- Memory management unit
  - 128-entry, two-way set-associative instruction TLB
  - 128-entry, two-way set-associative data TLB
  - Hardware reload for TLBs
  - Four instruction BATs and four data BATs
  - Virtual memory support for up to 4 exabytes (2^{52}) of virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
  - Snooped and invalidated for TLBI instructions
- Efficient data flow
  - All data buses between VRF, load/store unit, dL1, iL1, L2, and the bus are 128 bits wide
  - dL1 is fully pipelined to provide 128 bits/cycle to/from the VRF

  - L2 is fully pipelined to provide 128 bits per L2 clock cycle to the L1s
  - Up to eight outstanding, out-of-order, cache misses between dL1 and L2/bus
  - Up to seven outstanding, out-of-order transactions on the bus
  - Load folding to fold new dL1 misses into older, outstanding load and store misses to the same line
  - Store miss merging for multiple store misses to the same line. Only coherency action taken (i.e., address only) for store misses merged to all 32 bytes of a cache line (no data tenure needed).
  - Two-entry finished store queue and four-entry completed store queue between load/store unit and dL1
  - Separate additional queues for efficient buffering of outbound data (castouts, write throughs, etc.) from dL1 and L2
- Bus interface
  - MPX bus extension to 60x processor interface
  - Mode-compatible with 60x processor interface
  - 32-bit address bus
  - 64-bit data bus
  - Bus-to-core frequency multipliers of 2x, 2.5x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 9x supported
  - Selectable interface voltages of 1.8 V, 2.5 V, and 3.3 V
- Power management
  - Low-power design with thermal requirements very similar to MPC740 and MPC750
  - Low voltage processor core
  - Selectable interface voltages of 1.8 V can reduce power in output buffers
  - Three static power saving modes: doze, nap, and sleep
  - Dynamic power management
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
  - Array built-in self test (ABIST)—factory test only
  - Redundancy on L1 data arrays and L2 tag arrays
- Reliability and serviceability
  - Parity checking on 60x and L2 cache buses

1.3 General Parameters

The following list provides a summary of the general parameters of the MPC7410:

Technology	0.18 µm CMOS, six-layer metal
Die size	6.32 mm × 8.26 mm (52 mm^2)
Transistor count	10.5 million

Logic design	Fully static
Packages	Surface mount 360 ceramic ball grid array (CBGA)
Core power supply	1.8 V ± 100 mV DC (nominal; see Table 3 for recommended operating conditions)
I/O power supply	1.8 V ± 100 mV DC or 2.5 V ± 100 mV 3.3 V ± 165 mV (processor bus only) (input thresholds are configuration pin selectable)

1.4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC7410.

1.4.1 DC Electrical Characteristics

The tables in this section describe the MPC7410 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Maximum Value	Unit	Note
Core supply voltage		V_{DD}	–0.3 to 2.1	V	4
PLL supply voltage		AV_{DD}	–0.3 to 2.1	V	4
L2 DLL supply voltage		$L2AV_{DD}$	–0.3 to 2.1	V	4
Processor bus supply voltage		OV_{DD}	–0.3 to 3.465	V	3,6
L2 bus supply voltage		$L2OV_{DD}$	–0.3 to 2.6	V	3
Input voltage	Processor bus	V_{in}	–0.3 to OV_{DD} + 0.2 V	V	2, 5
	L2 bus	V_{in}	–0.3 to $L2OV_{DD}$ + 0.2 V	V	2, 5
	JTAG signals	V_{in}	–0.3 to OV_{DD} + 0.2 V	V	
Storage temperature range		T_{stg}	–55 to 150	°C	
Rework temperature		T_{rwk}	260	°C	

Notes:
1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution**: V_{in} must not exceed OV_{DD} or $L2OV_{DD}$ by more than 0.2 V at any time including during power-on reset.
3. **Caution**: $L2OV_{DD}/OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 2.0 V at any time including during power-on reset; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution**: $V_{DD}/AV_{DD}/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4 V at any time including during power-on reset; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. V_{in} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. MPC7410RXnnnLE (Rev 1.4) and later only. Previous revisions do not support 3.3 V OV_{DD} and have a maximum value OV_{DD} of –0.3 to 2.6 V.

Figure 2 shows the allowable undershoot and overshoot voltage for the MPC7410.

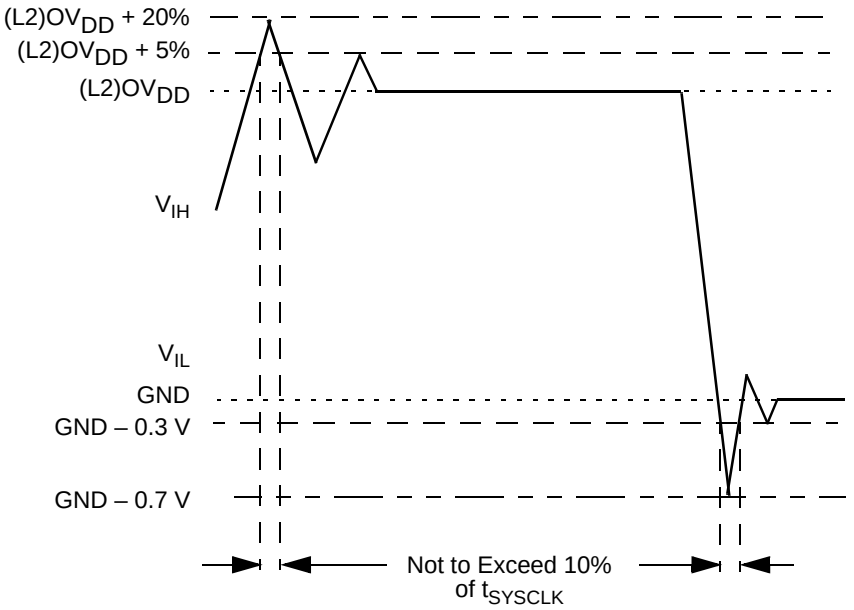


Figure 2. Overshoot/Undershoot Voltage

The MPC7410 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7410 core voltage must always be provided at nominal voltage (see Table 3 for actual recommended core voltage). Voltage to the L2 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 2. Voltage must be provided to the $L2OV_{DD}$ power pins even if the interface is not used. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins BVSEL and L2VSEL at the negation of the signal $\overline{\text{HRESET}}$. These signals must remain stable during part operation and cannot change. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or $L2OV_{DD}$ power pins.

Table 2. Input Threshold Voltage Setting

BVSEL Signal [3]	Processor Bus Input Threshold is Relative to:	L2VSEL Signal [3]	L2 Bus Input Threshold is Relative to:	Note
0	1.8 V	0	1.8 V	1
$\overline{\text{HRESET}}$	2.5 V	$\overline{\text{HRESET}}$	2.5 V	1, 2
1	3.3 V	1	2.5 V	1, 4, 5
HRESET	3.3 V	HRESET	Not Supported	6

Notes:
1. **Caution:** The input threshold selection must agree with the OV_{DD}/$L2OV_{DD}$ voltages supplied.
2. To select the 2.5-V threshold option, BVSEL and/or L2VSEL should be tied to $\overline{\text{HRESET}}$ so that the two signals change state together. This is the preferred method for selecting this mode of operation.
3. To overcome the internal pull-up resistance, a pull-down resistance less than 250 Ω should be used.
4. Default voltage setting if left unconnected (internal pulled-up). MPC7410RXnnnLE (Rev 1.4) and later only. Previous revisions do not support 3.3 V OV_{DD}, the default voltage setting if left unconnected is 2.5 V.
5. MPC7410RXnnnLE (Rev 1.4) and later only. Previous revisions do not support 3.3 V OV_{DD}, having BVSEL = 1 selects the 2.5 V threshold.
6. MPC7410RXnnnLE (Rev 1.4) and later only. Previous revisions do not support BVSEL = HRESET.

Table 3 provides the recommended operating conditions for the MPC7410.

Table 3. Recommended Operating Conditions[1]

Characteristic		Symbol	Recommended Value	Unit	Notes
Core supply voltage		V_{DD}	1.8 V ± 100 mV	V	
PLL supply voltage		AV_{DD}	1.8 V ± 100 mV	V	
L2 DLL supply voltage		$L2AV_{DD}$	1.8 V ± 100 mV	V	
Processor bus supply voltage	BVSEL = 0	OV_{DD}	1.8 V ± 100 mV	V	
	BVSEL = $\overline{\text{HRESET}}$	OV_{DD}	2.5 V ± 100 mV	V	
	BVSEL = HRESET or BVSEL = 1	OV_{DD}	3.3 V ± 165 mV	V	2, 3
L2 bus supply voltage	L2VSEL = 0	$L2OV_{DD}$	1.8 V ± 100 mV	V	
	L2VSEL = $\overline{\text{HRESET}}$ or L2VSEL = 1	$L2OV_{DD}$	2.5 V ± 100 mV	V	
Input voltage	Processor bus and JTAG signals	V_{in}	GND to OV_{DD}	V	
	L2 bus	V_{in}	GND to $L2OV_{DD}$	V	
Die-junction temperature		T_j	0 to 105	°C	

Notes:
1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. MPC7410RXnnnLE (Rev 1.4) and later only. Previous revisions do not support 3.3 V OV_{DD} and have a recommended OV_{DD} value of 2.5 V ±100 mV for BVSEL = 1.
3. MPC7410RXnnnLE (Rev 1.4) and later only. Previous revisions do not support BVSEL = HRESET.

Table 4 provides the package thermal characteristics for the MPC7410.

Table 4. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit	Notes
		MPC7410 CBGA		
Junction-to-ambient thermal resistance, natural convection, single-layer (1s) board	$R_{\theta JA}$	24	°C/W	1, 2
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JMA}$	17	°C/W	1, 3
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	$R_{\theta JMA}$	18	°C/W	1, 3
Junction-to-ambient thermal resistance, 400 ft/min airflow, single-layer (1s) board	$R_{\theta JMA}$	16		
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	$R_{\theta JMA}$	14	°C/W	1, 3

Table 4. Package Thermal Characteristics (continued)

Characteristic	Symbol	Value	Unit	Notes
		MPC7410 CBGA		
Junction-to-ambient thermal resistance, 400 ft/min airflow, four-layer (2s2p) board	$R_{\theta JMA}$	13		
Junction-to-board thermal resistance	$R_{\theta JB}$	8	°C/W	4
Junction-to-case thermal resistance	$R_{\theta JC}$	< 0.1	°C/W	5

Note:
1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.

Refer to Section 1.8.8, “Thermal Management Information,” for more details about thermal management.

Table 5 provides the DC electrical characteristics for the MPC7410.

Table 5. DC Electrical Specifications

At recommended operating conditions (see Table 3)

Characteristic	Nominal Bus Voltage[1]	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs except SYSCLK)	1.8	V_{IH}	$0.65 \times (L2)OV_{DD}$	$(L2)OV_{DD} + 0.2$	V	2, 3, 8
	2.5	V_{IH}	1.7	$(L2)OV_{DD} + 0.2$		
	3.3	V_{IH}	2.0	$OV_{DD} + 0.3$		
Input low voltage (all inputs except SYSCLK)	1.8	V_{IL}	–0.3	$0.35 \times (L2)OV_{DD}$	V	8
	2.5	V_{IL}	–0.3	$0.2 \times (L2)OV_{DD}$		
	3.3	V_{IL}	–0.3	0.8		
SYSCLK input high voltage	1.8	CV_{IH}	1.5	$OV_{DD} + 0.2$	V	2, 8
	2.5	CV_{IH}	2.0	$OV_{DD} + 0.2$		
	3.3	CV_{IH}	2.4	$OV_{DD} + 0.3$		
SYSCLK input low voltage	1.8	CV_{IL}	–0.3	0.2	V	8
	2.5	CV_{IL}	–0.3	0.4		
	3.3	CV_{IL}	–0.3	0.4		

Table 5. DC Electrical Specifications (continued)

At recommended operating conditions (see Table 3)

Characteristic	Nominal Bus Voltage[1]	Symbol	Min	Max	Unit	Notes
Input leakage current, V_{in} = $L2OV_{DD}/OV_{DD}$	1.8	I_{in}	—	20	µA	2, 3, 6, 7
	2.5	I_{in}	—	35		
	3.3	I_{in}	—	70		
High-Z (off-state) leakage current, V_{in} = $L2OV_{DD}/OV_{DD}$	1.8	I_{TSI}	—	20	µA	2, 3, 5, 7
	2.5	I_{TSI}	—	35		
	3.3	I_{TSI}	—	70		
Output high voltage, I_{OH} = –6 mA	1.8	V_{OH}	$(L2)OV_{DD}$ – 0.45	—	V	8
	2.5	V_{OH}	1.7	—		
	3.3	V_{OH}	2.4	—		
Output low voltage, I_{OL} = 6 mA	1.8	V_{OL}	—	0.45	V	8
	2.5	V_{OL}	—	0.4		
	3.3	V_{OL}	—	0.4		
Capacitance, V_{in} = 0 V, f = 1 MHz		C_{in}	—	6.0	pF	3, 4, 7

Notes:
1. Nominal voltages; see Table 3 for recommended operating conditions.
2. For processor bus signals, the reference is OV_{DD} while $L2OV_{DD}$ is the reference for the L2 bus signals.
3. Excludes factory test signals.
4. Capacitance is periodically sampled rather than 100% tested.
5. The leakage is measured for nominal OV_{DD} and $L2OV_{DD}$, or both OV_{DD} and $L2OV_{DD}$ must vary in the same direction (for example, both OV_{DD} and $L2OV_{DD}$ vary by either +5% or –5%).
6. Measured at max $OV_{DD}/L2OV_{DD}$.
7. Excludes IEEE 1149.1 boundary scan (JTAG) signals.
8. For JTAG support: all signals controlled by BVSEL and L2VSEL will see $V_{IL}/V_{IH}/V_{OL}/V_{OH}/CV_{IH}/CV_{IL}$ DC limits of 1.8 V mode while either the EXTEST or CLAMP instruction is loaded into the IEEE 1149.1 instruction register by the UpdateIR TAP state until a different instruction is loaded into the instruction register by either another UpdateIR or a Test-Logic-Reset TAP state. If only $\overline{\text{TSRT}}$ is asserted to the part, and then a SAMPLE instruction is executed, there is no way to control or predict what the DC voltage limits are. If $\overline{\text{HRESET}}$ is asserted before executing a SAMPLE instruction, the DC voltage limits will be controlled by the BVSEL/L2VSEL settings during $\overline{\text{HRESET}}$. Anytime $\overline{\text{HRESET}}$ is not asserted (i.e., just asserting $\overline{\text{TRST}}$), the voltage mode is not known until either EXTEST or CLAMP is executed, at which time the voltage level will be at the DC limits of 1.8 V.

Table 6 provides the power consumption for the MPC7410.

Table 6. Power Consumption for MPC7410

	Processor (CPU) Frequency			Unit	Notes
	400 MHz	450 MHz	500 MHz		
Full-On Mode					
Typical	4.2	4.7	5.3	W	1, 3
Maximum	9.5	10.7	11.9	W	1, 2
Doze Mode					
Maximum	4.3	4.8	5.3	W	1
Nap Mode					
Maximum	1.35	1.5	1.65	W	1
Sleep Mode					
Maximum	1.3	1.45	1.6	W	1
Sleep Mode—PLL and DLL Disabled					
Typical	600	600	600	mW	1
Maximum	1.1	1.1	1.1	W	1

Notes:
1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O supply power (OV_{DD} and $L2OV_{DD}$) or PLL/DLL supply power (AV_{DD} and $L2AV_{DD}$). OV_{DD} and $L2OV_{DD}$ power is system dependent, but is typically <10% of V_{DD} power. Worst case power consumption for AV_{DD} = 15 mW and $L2AV_{DD}$ = 15 mW.
2. Maximum power is measured at 105°C and V_{DD} = 1.8 V while running an entirely cache-resident, contrived sequence of instructions which keep the execution units, including AltiVec, maximally busy.
3. Typical power is an average value measured at 65°C and V_{DD} = 1.8 V in a system while running typical benchmarks.

1.4.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC7410. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Section 1.4.2.1, “Clock AC Specifications,” and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:3] signals. Parts are sold by maximum processor core frequency; see Section 1.10, “Ordering Information.”

1.4.2.1 Clock AC Specifications

Table 7 provides the clock AC timing specifications as defined in Figure 3.

Table 7. Clock AC Timing Specifications

At recommended operating conditions (see Table 3)

Characteristic	Symbol	Maximum Processor Core Frequency						Unit	Notes
		400 MHz		450 MHz		500 MHz			
		Min	Max	Min	Max	Min	Max		
Processor frequency	f_{core}	350	400	350	450	350	500	MHz	1
VCO frequency	f_{VCO}	700	800	700	900	700	1000	MHz	1
SYSCLK frequency	f_{SYSCLK}	33	133	33	133	33	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	30	7.5	30	7.5	30	ns	
SYSCLK rise and fall time	t_{KR} and t_{KF}	—	0.5	—	0.5	—	0.5	ns/V	2
SYSCLK duty cycle measured at $OV_{DD}/2$	t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	%	3
SYSCLK jitter		—	±150	—	±150	—	±150	ps	4
Internal PLL relock time		—	100	—	100	—	100	µs	5

Notes:

1. **Caution**: The SYSCLK frequency and PLL_CFG[0:3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:3] signal description in Section 1.8.1, “PLL Configuration,” for valid PLL_CFG[0:3] settings.
2. Rise and fall times measurement are determined by the slew rates of the bus interface, rather than by time. As a result, the 0.5 ns rise/fall time spec of the 1.8- and 2.5-V bus interfaces is equivalent to the 1 ns rise/fall time of the 3.3-V bus interface. Both interfaces required a 2 V/ns slew rate. The slew rate is measured as a 1-V change (from 0.2 to 1.2 V) in 0.5 ns for the 1.8- and 2.5-V bus interfaces, whereas the 3.3-V bus interface required a 2-V change (from 0.4 to 2.4 V) in 1 ns.
3. Timing is guaranteed by design and characterization.
4. This represents total input jitter—short term and long term combined—and is guaranteed by design.
5. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 3 provides the SYSCLK input timing diagram.

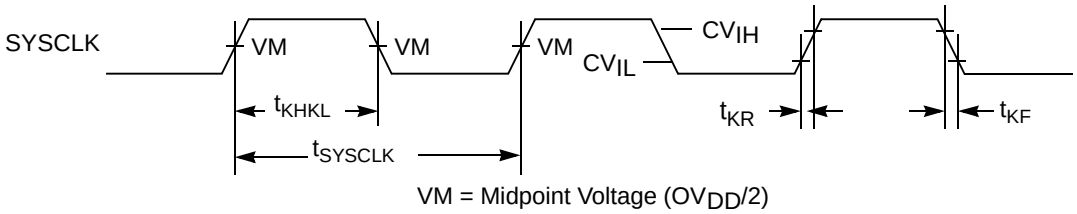


Figure 3. SYSCLK Input Timing Diagram

1.4.2.2 Processor Bus AC Specifications

Table 8 provides the processor bus AC timing specifications for the MPC7410 as defined in Figure 4 and Figure 5. Timing specifications for the L2 bus are provided in Section 1.4.2.3, "L2 Clock AC Specifications."

Table 8. Processor Bus AC Timing Specifications[1]

At recommended operating conditions (see Table 3)

Parameter	Symbol[2]	400, 450, 500 MHz		Unit	Notes
		Min	Max		
Mode Select Input Setup to $\overline{\text{HRESET}}$	t_{MVRH}	8	—	t_{sysclk}	3, 4, 5, 6
$\overline{\text{HRESET}}$ to Mode Select Input Hold	t_{MXRH}	0	—	ns	2, 3, 5
Input Setup	t_{IVKH}	1.0	—	ns	
Input Hold	t_{IXKH}	0	—	ns	
Output Valid Times: $\overline{\text{TS}}$ $\overline{\text{ARTRY}}$, $\overline{\text{SHD0}}$, $\overline{\text{SHD1}}$ All Other Outputs	 t_{KHTSV} t_{KHARV} t_{KHOV}	 — — —	 3.0 2.3 3.0	ns	7, 8
Output Hold Times: $\overline{\text{TS}}$ $\overline{\text{ARTRY}}$, $\overline{\text{SHD0}}$, $\overline{\text{SHD1}}$ All Other Outputs	 t_{KHTSX} t_{KHARX} t_{KHOX}	 0.5 0.5 0.5	 — — —	ns	7, 12
SYSCLK to Output Enable	t_{KHOE}	0.5	—	ns	11
SYSCLK to Output High Impedance (all except $\overline{\text{ABB}}$/$\overline{\text{AMON}}$(0), $\overline{\text{ARTRY}}$/$\overline{\text{SHD}}$, $\overline{\text{DBB}}$/$\overline{\text{DMON}}$(0), $\overline{\text{SHD0}}$, $\overline{\text{SHD1}}$)	t_{KHOZ}	—	3.5	ns	
SYSCLK to $\overline{\text{ABB}}$/$\overline{\text{AMON}}$(0), $\overline{\text{DBB}}$/$\overline{\text{DMON}}$(0) High Impedance After Precharge	t_{KHABPZ}	—	1	t_{sysclk}	5, 9, 11
Maximum Delay to $\overline{\text{ARTRY}}$, $\overline{\text{SHD0}}$, $\overline{\text{SHD1}}$ Precharge	t_{KHARP}	—	1	t_{sysclk}	5, 10, 11

Table 8. Processor Bus AC Timing Specifications[1] (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol[2]	400, 450, 500 MHz		Unit	Notes
		Min	Max		
SYSCLK to $\overline{\text{ARTRY}}$, $\overline{\text{SHD0}}$, $\overline{\text{SHD1}}$ High Impedance After Precharge	t_{KHARPZ}	—	2	t_{sysclk}	5, 10, 11

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH)—note the position of the reference and its state for inputs—and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 5).
4. This specification is for configuration mode select only. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time during the power-on reset sequence.
5. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
6. Mode select signals are BVSEL, EMODE, L2VSEL, PLL_CFG[0:3].
7. All other output signals are composed of the following— A[0:31], AP[0:3], TT[0:4], TS, $\overline{\text{TBST}}$, TSIZ[0:2], $\overline{\text{GBL}}$, $\overline{\text{WT}}$, $\overline{\text{CI}}$, DH[0:31], DL[0:31], DP[0:7], $\overline{\text{BR}}$, $\overline{\text{CKSTP\_OUT}}$, $\overline{\text{DRDY}}$, $\overline{\text{HIT}}$, $\overline{\text{QREQ}}$, $\overline{\text{RSRV}}$.
8. Output valid time is measured from 2.4 V to 0.8 V which may be longer than the time required to discharge from V_{DD} to 0.8 V.
9. According to the 60x bus protocol, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ are driven only by the currently active bus master. They are asserted low then precharged high before returning to high-Z as shown in Figure 6. The nominal precharge width for $\overline{\text{ABB}}$ or $\overline{\text{DBB}}$ is $0.5 \times t_{SYSCLK}$, i.e., less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-Z behavior is guaranteed by design.
10. According to the 60x bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue since any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following $\overline{\text{AACK}}$ will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{sysclk}; i.e., it should be high-Z as shown in Figure 6 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing are tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
11. Guaranteed by design and not tested.
12. Output hold time characteristics can be altered by the use of the L2_TSTCLK pin during system reset, similar to L2 output hold being altered by the use of bits [14-15] in the L2CR register. Information on the operation of the L2_TSTCLK will be included in future revisions of this specification.

Figure 4 provides the AC test load for the MPC7410.

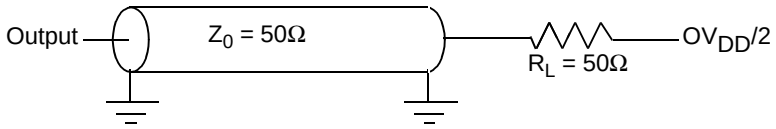


Figure 4. AC Test Load

Figure 5 provides the mode select input timing diagram for the MPC7410.

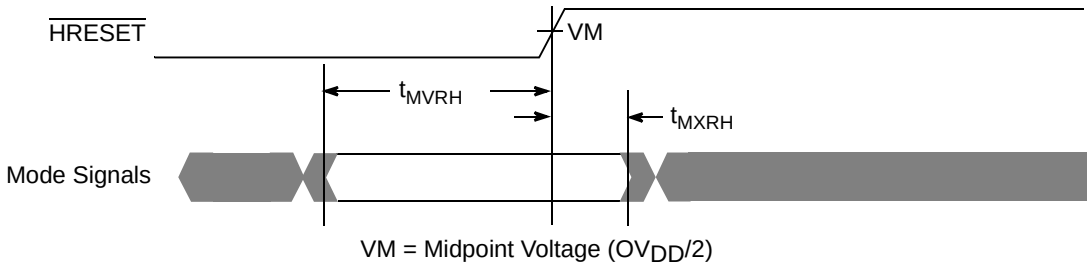


Figure 5. Mode Input Timing Diagram

Figure 6 provides the input/output timing diagram for the MPC7410.

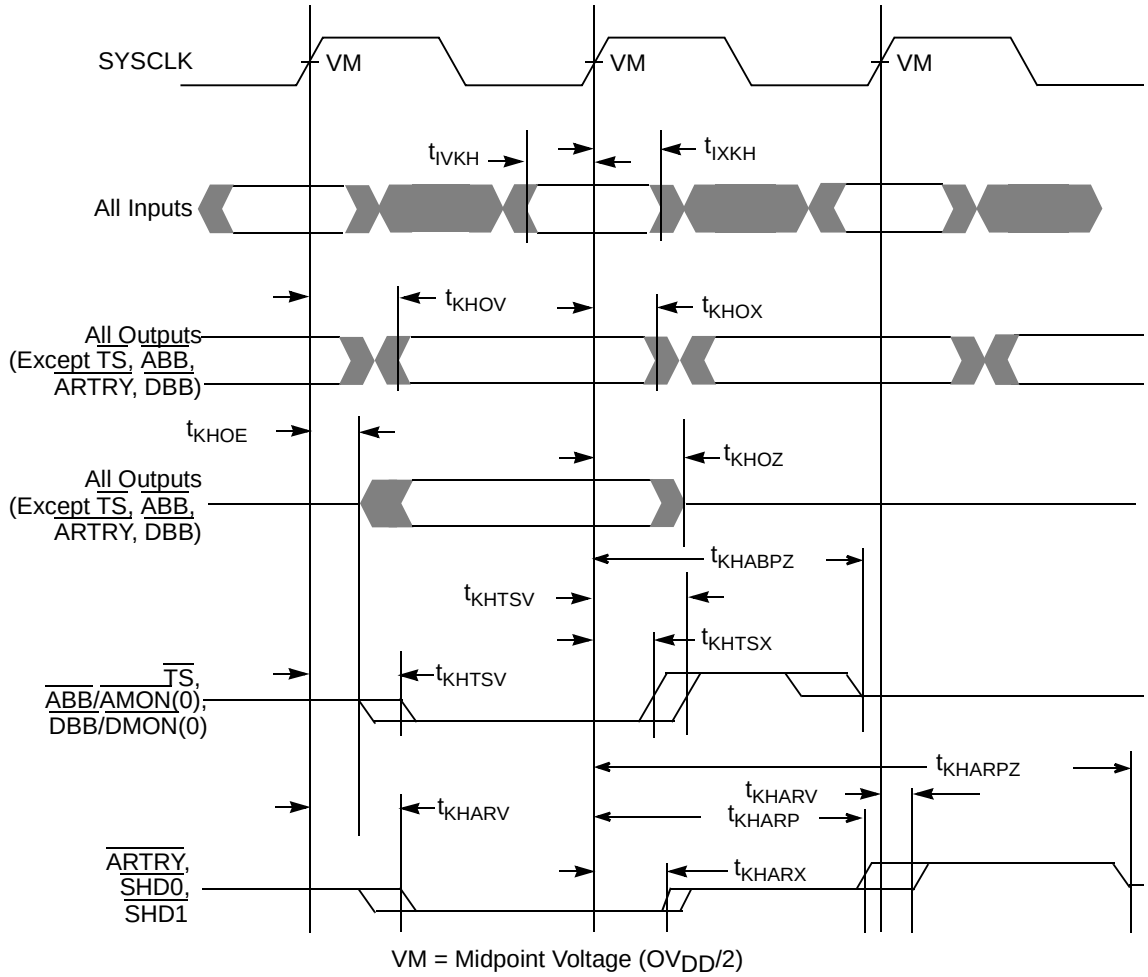


Figure 6. Input/Output Timing Diagram

1.4.2.3 L2 Clock AC Specifications

The L2CLK frequency is programmed by the L2 Configuration Register (L2CR[4:6]) core-to-L2 divisor ratio. See Table 14 for example core and L2 frequencies at various divisors. Table 9 provides the potential range of L2CLK output AC timing specifications as defined in Figure 7.

The L2SYNC_OUT signal is intended to be routed halfway out to the SRAMs and then returned to the L2SYNC_IN input of the MPC7410 to synchronize L2CLKOUT at the SRAM with the processor's internal clock. L2CLKOUT at the SRAM can be offset forward or backward in time by shortening or lengthening the routing of L2SYNC_OUT to L2SYNC_IN. See Motorola Application Note AN1794/D, *Backside L2 Timing Analysis for the PCB Design Engineer.*

The minimum L2CLK frequency in Table 9 is specified by the maximum delay of the internal DLL. The variable-tap DLL introduces up to a full clock period delay in the L2CLKOUTA, L2CLKOUTB, and L2SYNC_OUT signals so that the returning L2SYNC_IN signal is phase-aligned with the next core clock (divided by the L2 divisor ratio). Do not choose a core-to-L2 divisor which results in an L2 frequency below this minimum, or the L2CLKOUT signals provided for SRAM clocking will not be phase-aligned with the MPC7410 core clock at the SRAMs.

The maximum L2CLK frequency shown in Table 9 is the core frequency divided by one. Very few L2 SRAM designs will be able to operate in this mode. Most designs will select a greater core-to-L2 divisor to provide a longer L2CLK period for read and write access to the L2 SRAMs. The maximum L2CLK frequency for any application of the MPC7410 will be a function of the AC timings of the MPC7410, the AC timings for the SRAM, bus loading, and printed circuit board trace length.

Motorola is similarly limited by system constraints and cannot perform tests of the L2 interface on a socketed part on a functional tester at the maximum frequencies in Table 9. Therefore, functional operation and AC timing information are tested at core-to-L2 divisors of two or greater.

L2 input and output signals are latched or enabled, respectively, by the internal L2CLK (which is SYSCLK multiplied up to the core frequency and divided down to the L2CLK frequency). In other words, the AC timings in Table 10 are entirely independent of L2SYNC_IN. In a closed loop system, where L2SYNC_IN is driven through the board trace by L2SYNC_OUT, L2SYNC_IN only controls the output phase of L2CLKOUTA and L2CLKOUTB which are used to latch or enable data at the SRAMs. However, since in a closed loop system L2SYNC_IN is held in phase-alignment with the internal L2CLK, the signals in Table 10 are referenced to this signal rather than the not-externally-visible internal L2CLK. During manufacturing test, these times are actually measured relative to SYSCLK.

Table 9. L2CLK Output AC Timing Specifications

At recommended operating conditions (see Table 3)

Parameter	Symbol	400 MHz		450 MHz		500 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
L2CLK frequency	f_{L2CLK}	133	400	133	400	133	400	MHz	1, 4
L2CLK cycle time	t_{L2CLK}	2.5	7.5	2.5	7.5	2.5	7.5	ns	
L2CLK duty cycle	t_{CHCL}/t_{L2CLK}	50		50		50		%	2
Internal DLL-relock time		640	—	640	—	640	—	L2CLK	3
DLL capture window		0	10	0	10	0	10	ns	5
L2CLKOUT output-to-output skew	t_{L2CSKW}	—	50	—	50	—	50	ps	6

Table 9. L2CLK Output AC Timing Specifications (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol	400 MHz		450 MHz		500 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
L2CLKOUT output jitter		—	±150	—	±150	—	±150	ps	6

Notes:
1. L2CLK outputs are L2CLK_OUTA, L2CLK_OUTB, and L2SYNC_OUT pins. The L2CLK frequency to core frequency settings must be chosen such that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. The maximum L2CLK frequency will be system dependent. L2CLK_OUTA and L2CLK_OUTB must have equal loading.
2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.
3. The DLL-relock time is specified in terms of L2CLKs. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in ns. Relock timing is guaranteed by design and characterization.
4. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 150 MHz. This adds more delay to each tap of the DLL.
5. Allowable skew between L2SYNC_OUT and L2SYNC_IN.
6. Guaranteed by design and not tested. This output jitter number represents the maximum delay of one tap forward or one tap back from the current DLL tap as the phase comparator seeks to minimize the phase difference between L2SYNC_IN and the internal L2CLK. This number must be comprehended in the L2 timing analysis. The input jitter on SYSCLK affects L2CLKOUT and the L2 address/data/control signals equally and, therefore, is already comprehended in the AC timing and does not have to be considered in the L2 timing analysis.

The L2CLK_OUT timing diagram is shown in Figure 7.

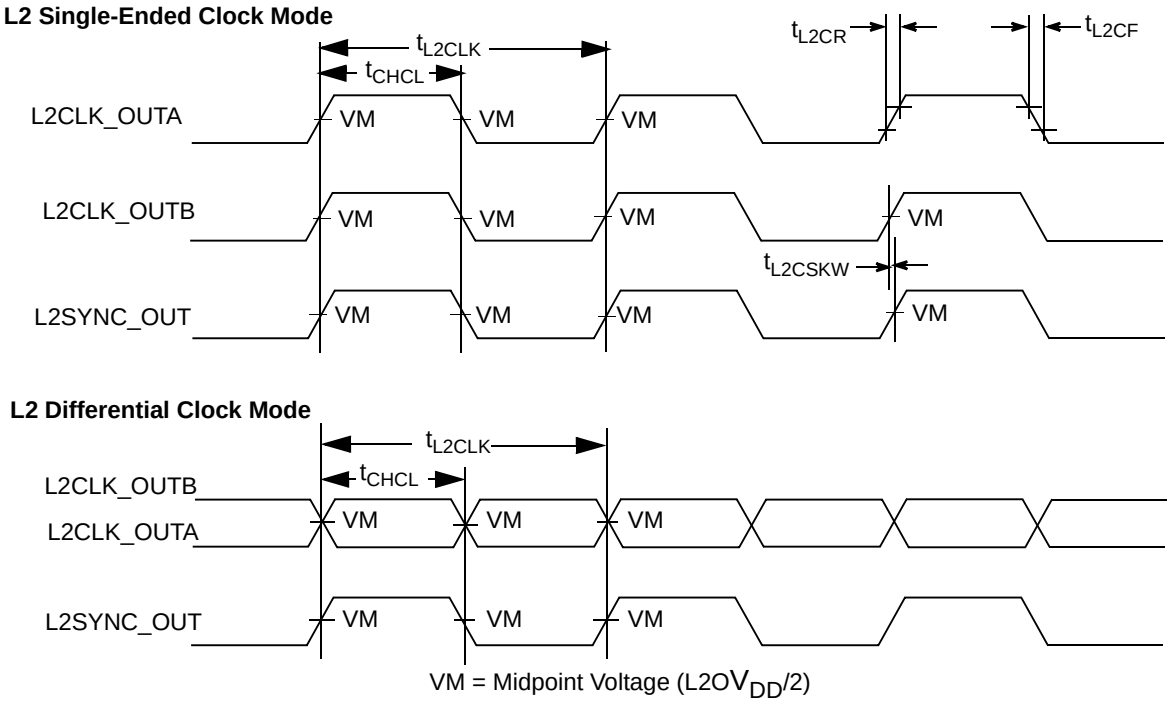


Figure 7. L2CLK_OUT Output Timing Diagram

1.4.2.4 L2 Bus AC Specifications

Table 10 provides the L2 bus interface AC timing specifications for the MPC7410 as defined in Figure 8 and Figure 9 for the loading conditions described in Figure 10.

Table 10. L2 Bus Interface AC Timing Specifications

At recommended operating conditions (see Table 3)

Parameter	Symbol	400, 450, 500 MHz		Unit	Notes
		Min	Max		
L2SYNC_IN rise and fall time	t_{L2CR} and t_{L2CF}	—	1.0	ns	1
Setup Times: Data and parity	t_{DVL2CH}	1.5	—	ns	2
Input Hold Times: Data and parity	t_{DXL2CH}	—	0.0	ns	2
Valid Times:	t_{L2CHOV}			ns	3, 4
All outputs when L2CR[14-15] = 00		—	2.5		
All outputs when L2CR[14-15] = 01		—	2.5		
All outputs when L2CR[14-15] = 10		—	2.9		
All outputs when L2CR[14-15] = 11		—	3.5		
Output Hold Times	t_{L2CHOX}			ns	3
All outputs when L2CR[14-15] = 00		0.4	—		
All outputs when L2CR[14-15] = 01		0.8	—		
All outputs when L2CR[14-15] = 10		1.2	—		
All outputs when L2CR[14-15] = 11		1.6	—		
L2SYNC_IN to high impedance:	t_{L2CHOZ}			ns	
All outputs when L2CR[14-15] = 00		—	2.0		
All outputs when L2CR[14-15] = 01		—	2.5		
All outputs when L2CR[14-15] = 10		—	3.0		
All outputs when L2CR[14-15] = 11		—	3.5		

Notes:
1. Rise and fall times for the L2SYNC_IN input are measured from 20% to 80% of $L2OV_{DD}$.
2. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L2SYNC_IN (see Figure 8). Input timings are measured at the pins.
3. All output specifications are measured from the midpoint voltage of the rising edge of L2SYNC_IN to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 10).
4. The outputs are valid for both single-ended and differential L2CLK modes. For pipelined registered synchronous BurstRAMs, L2CR[14–15] = 00 is recommended. For pipelined late write synchronous BurstRAMs, L2CR[14–15] = 10 is recommended.

Figure 8 shows the L2 bus input timing diagrams for the MPC7410.

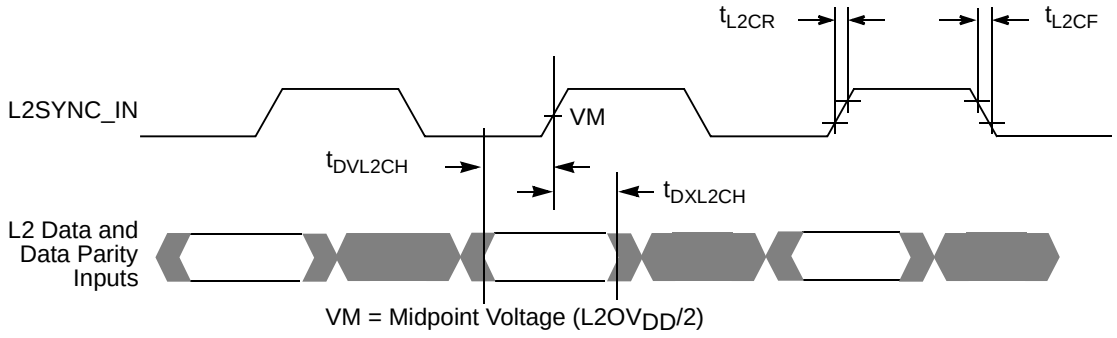


Figure 8. L2 Bus Input Timing Diagrams

Figure 9 shows the L2 bus output timing diagrams for the MPC7410.

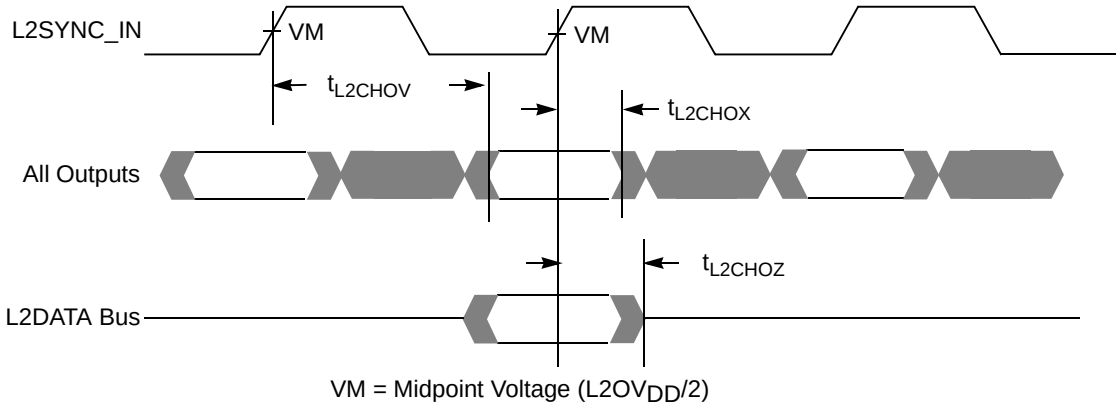


Figure 9. L2 Bus Output Timing Diagrams

Figure 10 provides the AC test load for L2 interface of the MPC7410.

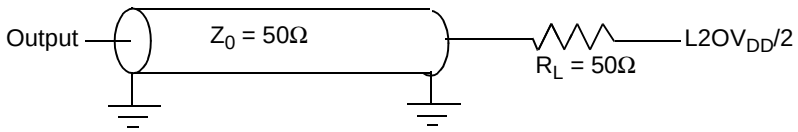


Figure 10. AC Test Load for the L2 Interface

1.4.2.5 IEEE 1149.1 AC Timing Specifications

Table 11 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 12, Figure 13, Figure 14, and Figure 15.

Table 11. JTAG AC Timing Specifications (Independent of SYSCLK)[1]

At recommended operating conditions (see Table 3)

Parameter	Symbol	Min	Max	Unit	Notes
TCK Frequency of Operation	f_{TCLK}	0	33.3	MHz	
TCK Cycle Time	t_{TCLK}	30	—	ns	
TCK Clock Pulse Width Measured at OV_{DD}/2	t_{JHJL}	15	—	ns	

Table 11. JTAG AC Timing Specifications (Independent of SYSCLK)[1] (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol	Min	Max	Unit	Notes
TCK Rise and Fall Times	t_{JR} and t_{JF}	0	2	ns	
$\overline{\text{TRST}}$ Assert Time	t_{TRST}	25	—	ns	2
Input Setup Times: Boundary-scan data TMS, TDI	 t_{DVJH} t_{IVJH}	 4 0	 — —	ns	 3
Input Hold Times: Boundary-scan data TMS, TDI	 t_{DXJH} t_{IXJH}	 20 25	 — —	ns	 3
Valid Times: Boundary-scan data TDO	 t_{JLDV} t_{JLOV}	 4 4	 20 25	ns	 4
TCK to Output High Impedance: Boundary-scan data TDO	 t_{JLDZ} t_{JLOZ}	 3 3	 19 9	ns	 4, 5 5

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 11). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 11 provides the AC test load for TDO and the boundary-scan outputs of the MPC7410.

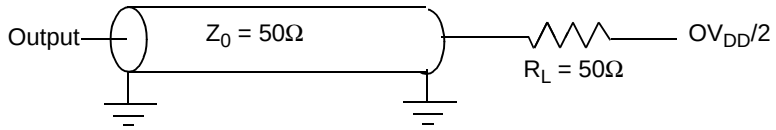


Figure 11. Alternate AC Test Load for the JTAG Interface

Figure 12 provides the JTAG clock input timing diagram.

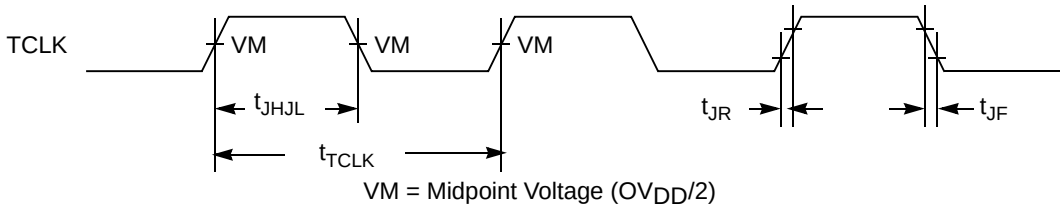


Figure 12. JTAG Clock Input Timing Diagram

Figure 13 provides the $\overline{\text{TRST}}$ timing diagram.

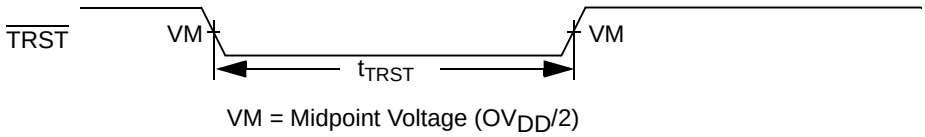


Figure 13. $\overline{\text{TRST}}$ Timing Diagram

Figure 14 provides the boundary-scan timing diagram.

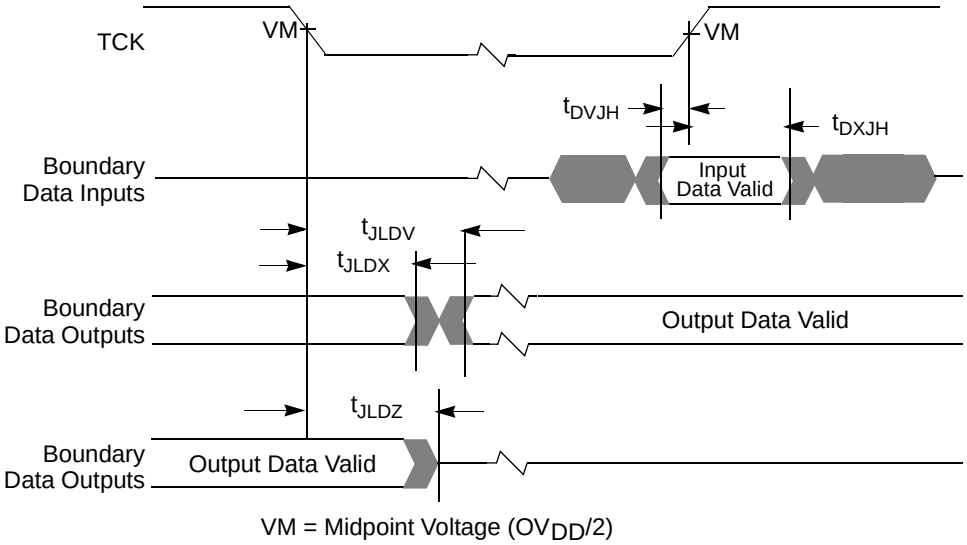


Figure 14. Boundary-Scan Timing Diagram

Figure 15 provides the test access port timing diagram.

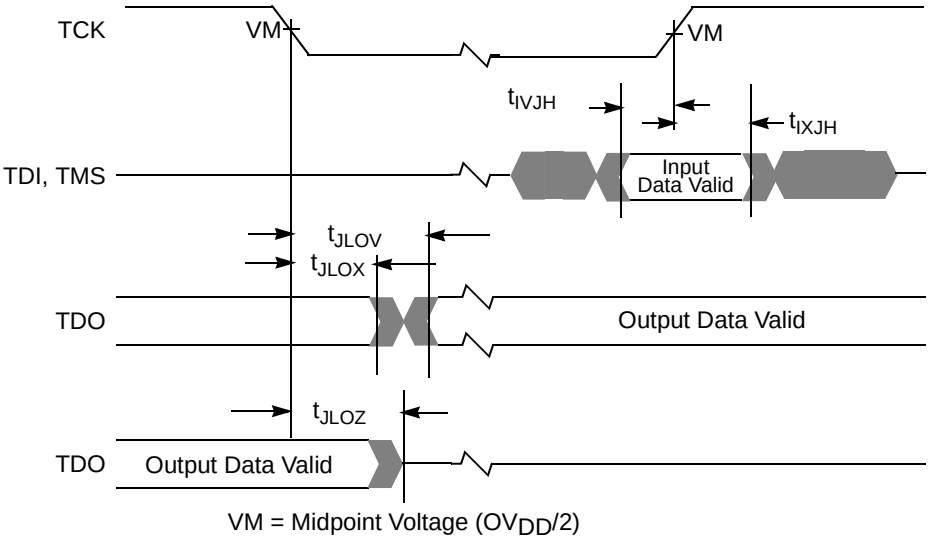


Figure 15. Test Access Port Timing Diagram

1.5 Pin Assignments

Figure 16 (in part A) shows the pinout of the MPC7410, 360 CBGA package as viewed from the top surface. Part B shows the side profile of the CBGA package to indicate the direction of the top surface view.

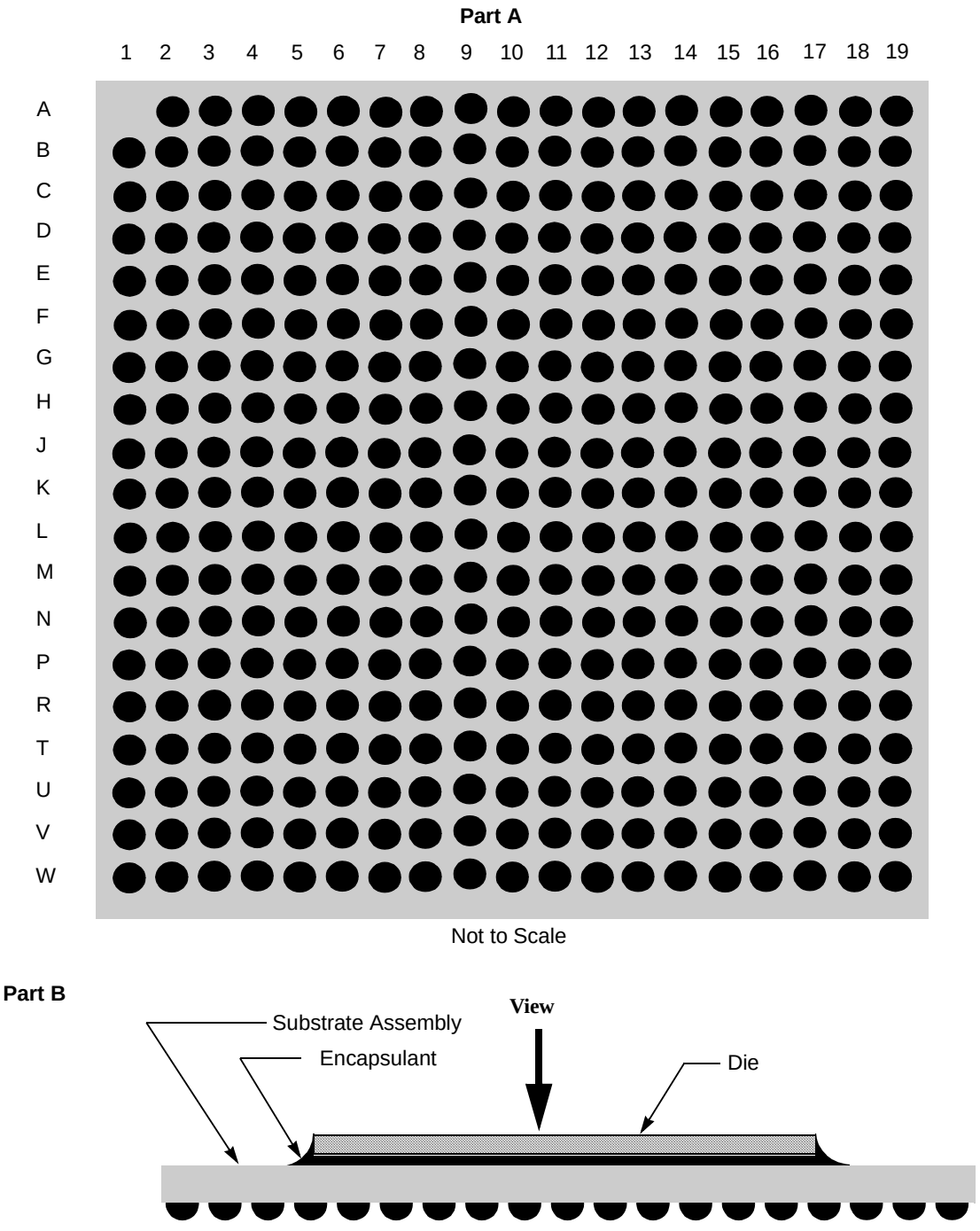


Figure 16. Pinout of the MPC7410, 360 CBGA Package as Viewed from the Top Surface

1.6 Pinout Listings

Table 12 provides the pinout listing for the MPC7410, 360 CBGA package.

Table 12. Pinout Listing for the MPC7410, 360 CBGA Package

Signal Name	Pin Number	Active	I/O	I/F Select[1]	Notes
A[0:31]	A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2	High	I/O	BVSEL	
$\overline{\text{AACK}}$	N3	Low	Input	BVSEL	
$\overline{\text{ABB}}$	L7	Low	Output	BVSEL	12
AP[0:3]	C4, C5, C6, C7	High	I/O	BVSEL	
$\overline{\text{ARTRY}}$	L6	Low	I/O	BVSEL	
AV_{DD}	A8	—	Input	V_{DD}	
$\overline{\text{BG}}$	H1	Low	Input	BVSEL	
$\overline{\text{BR}}$	E7	Low	Output	BVSEL	
BVSEL	W1	High	Input	N/A	1, 3, 8, 9, 14
$\overline{\text{CHK}}$	K11	Low	Input	BVSEL	4, 8, 9
$\overline{\text{CI}}$	C2	Low	I/O	BVSEL	
$\overline{\text{CKSTP\_IN}}$	B8	Low	Input	BVSEL	
$\overline{\text{CKSTP\_OUT}}$	D7	Low	Output	BVSEL	
CLK_OUT	E3	High	Output	BVSEL	
$\overline{\text{DBB}}$	K5	Low	Output	BVSEL	12
$\overline{\text{DBG}}$	K1	Low	Input	BVSEL	
DH[0:31]	W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5	High	I/O	BVSEL	
DL[0:31]	M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2	High	I/O	BVSEL	
DP[0:7]	L1, P2, M2, V2, M1, N2, T3, R1	High	I/O	BVSEL	
$\overline{\text{DRDY}}$	K9	Low	Output	BVSEL	6, 8, 13
$\overline{\text{DBWO}}$ DTI[0]	D1	Low	Input	BVSEL	
DTI[1:2]	H6, G1	High	Input	BVSEL	10, 13
$\overline{\text{EMODE}}$	A3	Low	Input	BVSEL	7, 10
$\overline{\text{GBL}}$	B1	Low	I/O	BVSEL	

Table 12. Pinout Listing for the MPC7410, 360 CBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select[1]	Notes
GND	D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16	—	—	N/A	
$\overline{\text{HIT}}$	B5	Low	Output	BVSEL	6, 8
$\overline{\text{HRESET}}$	B6	Low	Input	BVSEL	15
$\overline{\text{INT}}$	C11	Low	Input	BVSEL	
L1_TSTCLK	F8	High	Input	BVSEL	2
L2ADDR[0:16]	L17, L18, L19, M19, K18, K17, K15, J19, J18, J17, J16, H18, H17, J14, J13, H19, G18	High	Output	L2VSEL	
L2ADDR[17:18]	K19,W19	High	Output	L2VSEL	8
$L2AV_{DD}$	L13	—	Input	V_{DD}	
$\overline{\text{L2CE}}$	P17	Low	Output	L2VSEL	
L2CLK_OUTA	N15	High	Output	L2VSEL	
L2CLK_OUTB	L16	High	Output	L2VSEL	
L2DATA[0:63]	U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13	High	I/O	L2VSEL	
L2DP[0:7]	V14, U16, T19, N18, H14, F17, C19, B15	High	I/O	L2VSEL	
$L2OV_{DD}$	D15, E14, E16, H16, J15, L15, M16, K13, P15, R14, R16, T15, F15	—	—	N/A	11
L2SYNC_IN	L14	High	Input	L2VSEL	
L2SYNC_OUT	M14	High	Output	L2VSEL	
L2_TSTCLK	F7	High	Input	BVSEL	2
L2VSEL	A19	High	Input	N/A	1, 3, 8, 9, 14
$\overline{\text{L2WE}}$	N16	Low	Output	L2VSEL	
L2ZZ	G17	High	Output	L2VSEL	
$\overline{\text{LSSD\_MODE}}$	F9	Low	Input	BVSEL	2
$\overline{\text{MCP}}$	B11	Low	Input	BVSEL	15
OV_{DD}	D5, D8, D12, E4, E6, E9, E11, F5, H4, J5, L5, M4, P5, R4, R6, R9, R11, T5, T8, T12	—	—	N/A	
PLL_CFG[0:3]	A4, A5, A6, A7	High	Input	BVSEL	

Table 12. Pinout Listing for the MPC7410, 360 CBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select[1]	Notes
$\overline{\text{QACK}}$	B2	Low	Input	BVSEL	
$\overline{\text{QREQ}}$	J3	Low	Output	BVSEL	
$\overline{\text{RSRV}}$	D3	Low	Output	BVSEL	
$\overline{\text{SHD0}}$	B3	Low	I/O	BVSEL	8
$\overline{\text{SHD1}}$	B4	Low	I/O	BVSEL	5, 8
$\overline{\text{SMI}}$	A12	Low	Input	BVSEL	
$\overline{\text{SRESET}}$	E10	Low	Input	BVSEL	
SYSCLK	H9	—	Input	BVSEL	
$\overline{\text{TA}}$	F1	Low	Input	BVSEL	
TBEN	A2	High	Input	BVSEL	
$\overline{\text{TBST}}$	A11	Low	Output	BVSEL	
TCK	B10	High	Input	BVSEL	
TDI	B7	High	Input	BVSEL	9
TDO	D9	High	Output	BVSEL	
$\overline{\text{TEA}}$	J1	Low	Input	BVSEL	
TMS	C8	High	Input	BVSEL	9
$\overline{\text{TRST}}$	A10	Low	Input	BVSEL	9, 14
$\overline{\text{TS}}$	K7	Low	I/O	BVSEL	
TSIZ[0:2]	A9, B9, C9	High	Output	BVSEL	
TT[0:4]	C10, D11, B12, C12, F11	High	I/O	BVSEL	
$\overline{\text{WT}}$	C3	Low	I/O	BVSEL	

Table 12. Pinout Listing for the MPC7410, 360 CBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select[1]	Notes
V_{DD}	G8, G10, G12, J8, J10, J12, L8, L10, L12, N8, N10, N12	—	—	N/A	

Notes:
1. $\overline{OV_{DD}}$ supplies power to the processor bus, JTAG, and all control signals except the L2 cache controls ($\overline{L2CE}$, $\overline{L2WE}$, and L2ZZ); $L2OV_{DD}$ supplies power to the L2 cache interface (L2ADDR[0:18], L2DATA[0:63], L2DP[0:7], and L2SYNC_OUT) and the L2 control signals; and V_{DD} supplies power to the processor core and the PLL and DLL (after filtering to become AV_{DD} and $L2AV_{DD}$, respectively). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL/L2VSEL pin configurations of Table 2 and the voltage supplied. For actual recommended value of V_{in} or supply voltages, see Table 3.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. To allow for future I/O voltage changes, provide the option to connect BVSEL and L2VSEL independently to either OV_{DD}, GND, HRESET or $\overline{HRESET}$. For the MPC7410 the L2 bus only supports 2.5 V and 1.8 V options. The default selection, if L2VSEL is left unconnected, is 2.5 V operation. For the MPC7410 the processor bus supports 3.3 V, 2.5 V, and 1.8 V options. The default selection, if BVSEL is left unconnected, is 3.3 V operation. Refer to Table 2 for supported BVSEL and L2VSEL settings.
4. Connect to $\overline{HRESET}$ to trigger post power-on-reset (por) internal memory test.
5. Ignored input in 60x bus mode.
6. Unused output in 60x bus mode. Signal is three-stated in 60x mode.
7. Deasserted (pulled high) at $\overline{HRESET}$ for 60x bus mode.
8. Uses one of nine existing no-connects in MPC750 360 BGA package.
9. Internal pull up on die. Pulled-up signals are V_{DD} based.
10. Reuses MPC750 $\overline{DRTRY}$, $\overline{DBDIS}$, and TLBISYNC pins (DTI1, DTI2, and $\overline{EMODE}$, respectively).
11. The VOLTDET pin position on the MPC750 360 CBGA package is now an $L2OV_{DD}$ pin on the MPC7410 360 CBGA package.
12. Output only for MPC7410, was I/O for MPC750.
13. Enhanced mode only.
14. To overcome the internal pull-up resistance and ensure this input will recognize a low signal, a pull-down resistance less than 250 Ω should be used.
15 $\overline{MCP}$ minimum pulse width: asynchronous, falling-edge input needs to be held asserted for a minimum of 2 cycles to guarantee that it is latched by the processor.

1.7 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC7410, 360 CBGA package.

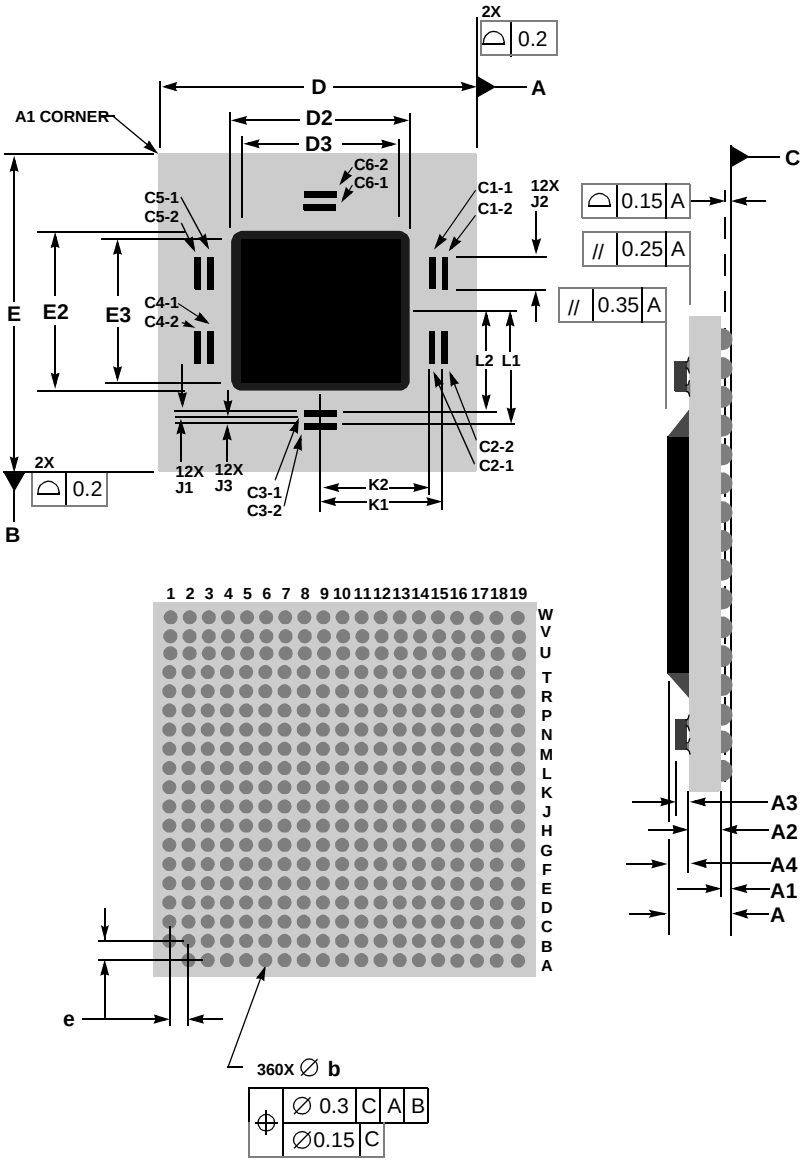
1.7.1 Package Parameters for the MPC7410

The package parameters are as provided in the following list. The package type is 25×25 mm, 360-lead ceramic ball grid array (CBGA).

Package outline	25×25 mm
Interconnects	360 (19×19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.65 mm
Maximum module height	3.20 mm
Ball diameter	0.89 mm (35 mil)

1.7.2 Mechanical Dimensions for the MPC7410, 360 CBGA

Figure 17 provides the mechanical dimensions and bottom surface nomenclature of the MPC7410, 360 CBGA package.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE A1 CORNER IS DESIGNATED WITH A BALL MISSING FROM THE ARRAY.

	Millimeters	
DIM	MIN	MAX
A	2.72	3.20
A1	0.80	1.00
A2	1.10	1.30
A3	—	0.60
A4	0.82	0.90
b	0.82	0.93
C1-1	$L2OV_{DD}$	
C1-2	GND	
C2-1	$L2OV_{DD}$	
C2-2	GND	
C3-1	V_{DD}	
C3-2	GND	
C4-1	OV_{DD}	
C4-2	GND	
C5-1	OV_{DD}	
C5-2	GND	
C6-1	V_{DD}	
C6-2	GND	
D	25.00 BSC	
D2	10.0 typ.	
D3	6.32	
e	1.27 BSC	
E	25.00 BSC	
E2	12.6 typ.	
E3	8.26	
J1	0.89 BSC	
J2	3.2 BSC	
J3	0.68 BSC	
K1	6.56	
K2	8.13	
L1	8.61	
L2	7.04	

Figure 17. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7410, 360 CBGA

1.8 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC7410.

1.8.1 PLL Configuration

The MPC7410 PLL is configured by the PLL_CFG[0–3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MPC7410 is shown in Table 13 for example frequencies. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with the minimum and maximum core frequencies listed in Table 8.

Table 13. MPC7410 Microprocessor PLL Configuration

PLL_CFG [0:3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 33.3 MHz	Bus 50 MHz	Bus 66.6 MHz	Bus 75 MHz	Bus 83.3 MHz	Bus 100 MHz	Bus 133 MHz
0100	2x	2x							
0110	2.5x	2x							
1000	3x	2x							400 (800)
1110	3.5x	2x						350 (700)	465 (930)
1010	4x	2x						400 (800)	
0111	4.5x	2x					375 (750)	450 (900)	
1011	5x	2x				375 (750)	416 (833)	500 (1000)	
1001	5.5x	2x			366 (733)	412 (825)	458 (916)		
1101	6x	2x			400 (800)	450 (900)	500 (1000)		
0101	6.5x	2x			433 (866)	488 (967)			
0010	7x	2x		350 (700)	466 (933)				
0001	7.5x	2x		375 (750)	500 (1000)				
1100	8x	2x		400 (800)					
0000	9x	2x		450 (900)					

Table 13. MPC7410 Microprocessor PLL Configuration (continued)

PLL_CFG [0:3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 33.3 MHz	Bus 50 MHz	Bus 66.6 MHz	Bus 75 MHz	Bus 83.3 MHz	Bus 100 MHz	Bus 133 MHz
0011	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied						
1111	PLL off		PLL off, no core clocking occurs						

Notes:
1. PLL_CFG[0:3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the MPC7410; see Section 1.4.2.1, “Clock AC Specifications,” for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use and third- party emulator tool development only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the MPC7410 regardless of the SYSCLK input.
5. PLL-off mode should not be used during chip power-up sequencing.

The MPC7410 generates the clock for the external L2 synchronous data SRAMs by dividing the core clock frequency of the MPC7410. The divided-down clock is then phase-adjusted by an on-chip delay-lock-loop (DLL) circuit and should be routed from the MPC7410 to the external RAMs. A separate clock output, L2SYNC_OUT is sent out half the distance to the SRAMs and then returned as an input to the DLL on pin L2SYNC_IN so that the rising-edge of the clock as seen at the external RAMs can be aligned to the clocking of the internal latches in the L2 bus interface.

The core-to-L2 frequency divisor for the L2 PLL is selected through the L2CLK bits of the L2CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the MPC7410 core, and the phase adjustment range that the L2 DLL supports. Table 14 shows various example L2 clock frequencies that can be obtained for a given set of core frequencies. The minimum L2 frequency target is 133 MHz. Sample core-to-L2 frequencies for the MPC7410 is shown in Table 14. In this example, shaded cells represent settings that, for a given core frequency, result in L2 frequencies that do not comply with the minimum and maximum L2 frequencies listed in Table 10.

Table 14. Sample Core-to-L2 Frequencies

Core Frequency (MHz)	÷1	÷1.5	÷2	÷2.5	÷3	÷3.5	÷4
350	350	233	175	140	—	—	—
366	366	244	183	147	—	—	—
400	400	266	200	160	133	—	—
433	—	288	216	173	144	—	—
450	—	300	225	180	150	—	—
466	—	311	233	186	155	133	—

Table 14. Sample Core-to-L2 Frequencies (continued)

Core Frequency (MHz)	÷1	÷1.5	÷2	÷2.5	÷3	÷3.5	÷4
500	—	333	250	200	166	143	—

Note: The core and L2 frequencies are for reference only. Some examples may represent core or L2 frequencies which are not useful, not supported, or not tested for by the MPC7410; see Section 1.4.2.3, “L2 Clock AC Specifications,” for valid L2CLK frequencies. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 150 MHz.

1.8.2 PLL Power Supply Filtering

The AV_{DD} and $L2AV_{DD}$ power signals are provided on the MPC7410 to provide power to the clock generation PLL and L2 cache DLL, respectively. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500 kHz to 10 MHz resonant frequency range of the PLL. A circuit similar to the one shown in Figure 18 using surface mount capacitors with minimum Effective Series Inductance (ESL) is recommended. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. An identical but separate circuit should be placed as close as possible to the $L2AV_{DD}$ pin. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360 CBGA footprint, without the inductance of vias. The $L2AV_{DD}$ pin may be more difficult to route but is proportionately less critical.

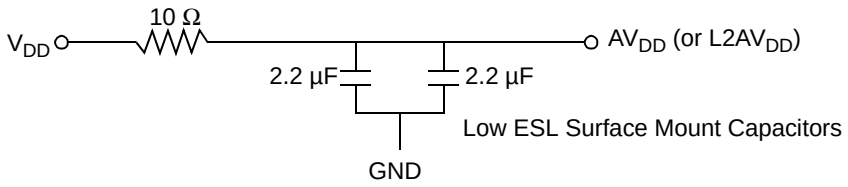


Figure 18. PLL Power Supply Filter Circuit

1.8.3 Decoupling Recommendations

Due to the MPC7410 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7410 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7410 system, and the MPC7410 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and $L2OV_{DD}$ pin of the MPC7410. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, $(L2)OV_{DD}$, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should have a value of 0.01 µF or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603 orientations where connections are made along the length of the part.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, $L2OV_{DD}$, and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

1.8.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level through a resistor. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, $L2OV_{DD}$, and GND pins of the MPC7410. Note that power must be supplied to $L2OV_{DD}$ even if the L2 interface of the MPC7410 will not be used.

1.8.5 Output Buffer DC Impedance

The MPC7410 60x and L2 I/O drivers are characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 19).

The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When Data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When Data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

Figure 19 describes the driver impedance measurement circuit described above.

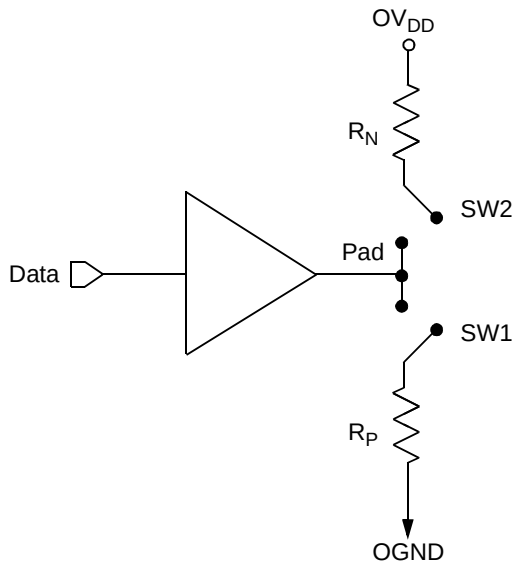


Figure 19. Driver Impedance Measurement Circuit

Alternately, the following is another method to determine the output impedance of the MPC7410. A voltage source, V_{force}, is connected to the output of the MPC7410, as in Figure 20. Data is held low, the voltage source is set to a value that is equal to (L2)OV_{DD}/2, and the current sourced by V_{force} is measured. The voltage drop across the pull-down device, which is equal to (L2)OV_{DD}/2, is divided by the measured current to determine the output impedance of the pull-down device, R_N. Similarly, the impedance of the pull-up device is determined by dividing the voltage drop of the pull-up, (L2)OV_{DD}/2, by the current sank by the pull-up when the data is high and V_{force} is equal to (L2)OV_{DD}/2. This method can be employed with either empirical data from a test setup or with data from simulation models, such as IBIS.

R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$. Figure 20 describes the alternate driver impedance measurement circuit.

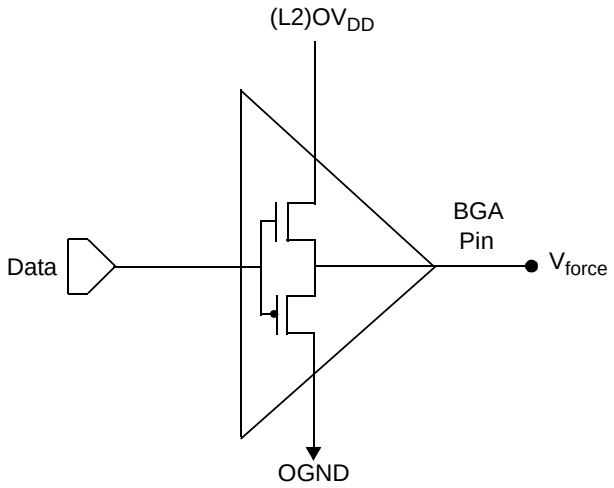


Figure 20. Alternate Driver Impedance Measurement Circuit

Table 15 summarizes the signal impedance results. The driver impedance values were characterized at 0°, 65°, and 105°C. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 15. Impedance Characteristics

V_{DD} = 1.8 V, OV_{DD} = 2.5 V, T_j = 0° – 105°C

Impedance	Processor Bus	L2 Bus	Symbol	Unit
R_N	41.5–54.3	42.7–54.1	Z_0	Ω
R_P	37.3–55.3	39.3–50.0	Z_0	Ω

1.8.6 Pull-Up Resistor Requirements

The MPC7410 requires pull-up resistors (1 kΩ–5 kΩ) on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7410 or other bus masters. These pins are: $\overline{TS}$, $\overline{AACK}$, $\overline{ARTRY}$, $\overline{SHDO}$, $\overline{SHD1}$, $\overline{TEA}$, and $\overline{TA}$.

Three test pins also require pull-up resistors (100 Ω–1 kΩ). These pins are L1_TSTCLK, L2_TSTCLK, and $\overline{LSSD\_MODE}$. These signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.

In addition, $\overline{CKSTP\_OUT}$ is an open-drain style output that requires a pull-up resistor (1 kΩ–5 kΩ) if it is used by the system.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Since the MPC7410 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the MPC7410 or by other receivers in the system. It is recommended that these signals be pulled up through weak (10 kΩ) pull-up resistors by the system, or that they may be otherwise driven by the system during inactive periods of the bus. The snooped address and transfer attribute inputs are: A[0:31], AP[0:3], TT[0:4], $\overline{\text{TBST}}$, $\overline{\text{CI}}$, $\overline{\text{WT}}$, and $\overline{\text{GBL}}$.

In systems where $\overline{\text{GBL}}$ is not connected and other devices may be asserting $\overline{\text{TS}}$ for a snoopable transaction while not driving $\overline{\text{GBL}}$ to the processor, we recommend that a strong (1 kΩ) pull-up resistor be used on $\overline{\text{GBL}}$.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: DH[0:31], DL[0:31], and DP[0:7].

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If parity checking is disabled through HID0, and parity generation is not required by the MPC7410 (note the MPC7410 always generates parity), then all parity pins may be left unconnected by the system.

The L2 interface does not normally require pull-up resistors.

1.8.7 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

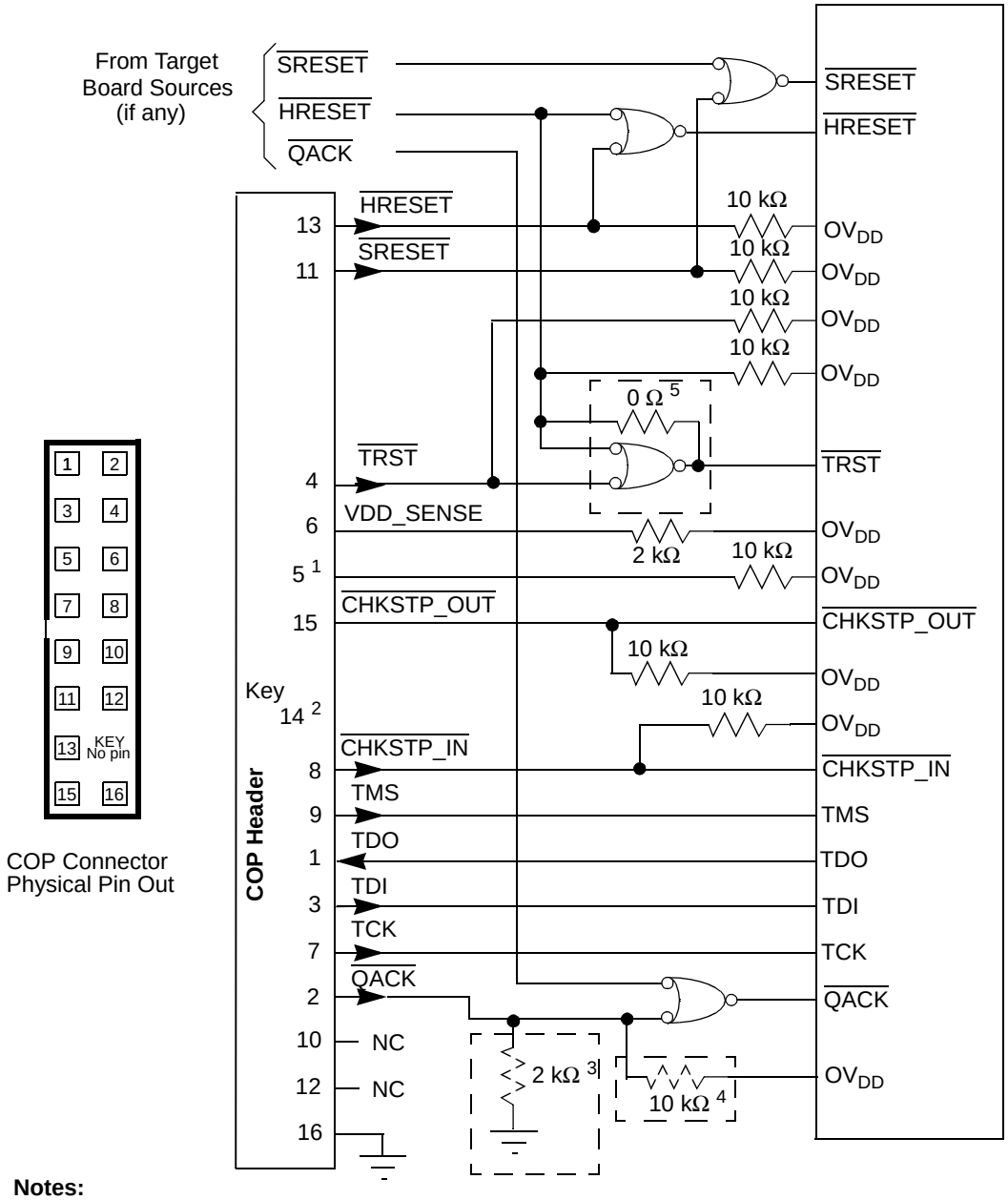
The arrangement shown in Figure 21 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted ensuring that the JTAG scan chain is initialized during power-on. While Motorola recommends that the COP header be designed into the system as shown in Figure 21, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP header shown in Figure 21 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 21; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 21 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 21 is usually connected to the PCI bridge chip in a system and is an input to the MPC7410 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC7410 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is deasserted when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged via logic so that it also can be driven by the PCI bridge.



Notes:

1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the MPC7410. Connect pin 5 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.
4. Populate only if debug tool uses an open-drain type output and does not actively deassert $\overline{\text{QACK}}$.
5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0-Ω isolation reisistor.

Figure 21. COP Connector Diagram

1.8.8 Thermal Management Information

This section provides thermal management information for the ceramic ball grid array (CBGA) package for

air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—adhesive, spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly; see Figure 22. This spring force should not exceed 5.5 pounds of force. Note that care should be taken to avoid focused forces being applied to die corners and/or edges when mounting heatsinks.

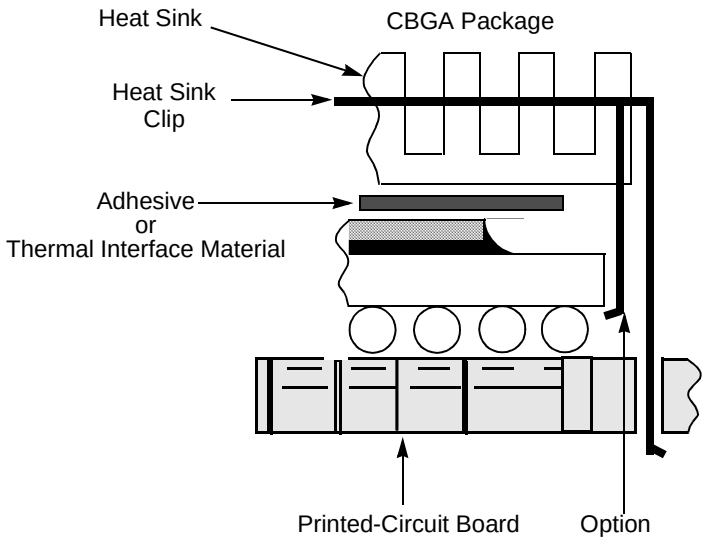


Figure 22. Package Exploded Cross-Sectional View with Several Heat Sink Options

The board designer can choose between several types of heat sinks to place on the MPC7410. There are several commercially-available heat sinks for the MPC7410 provided by the following vendors:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #15
Santa Clara, CA 95054
Internet: www.alphanovatech.com

The Bergquist Company 800-347-4572
18930 West 78th St.
Chanhassen, MN 55317
Internet: www.bergquistcompany.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Tyco Electronics 800-522-6752
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering 603-635-5201
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

1.8.8.1 Internal Package Conduction Resistance

For the exposed-die packaging technology, shown in Table 3, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case (or top-of-die for exposed silicon) thermal resistance
- The die junction-to-ball thermal resistance

Figure 23 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms.

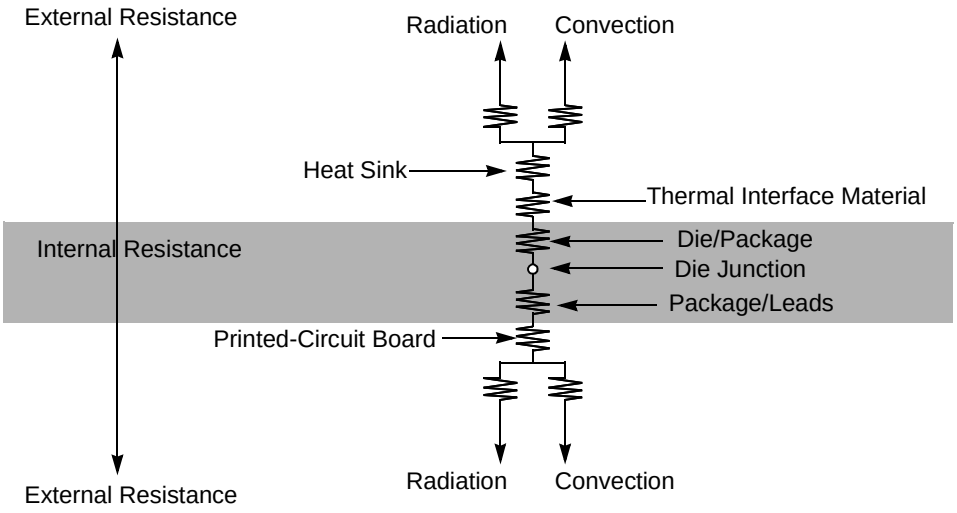


Figure 23. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

1.8.8.2 Adhesives and Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 24 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure.

The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 22). This spring force should not exceed 5.5 pounds of force. Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, etc.

Figure 24 describes the thermal performance of selected thermal interface materials.

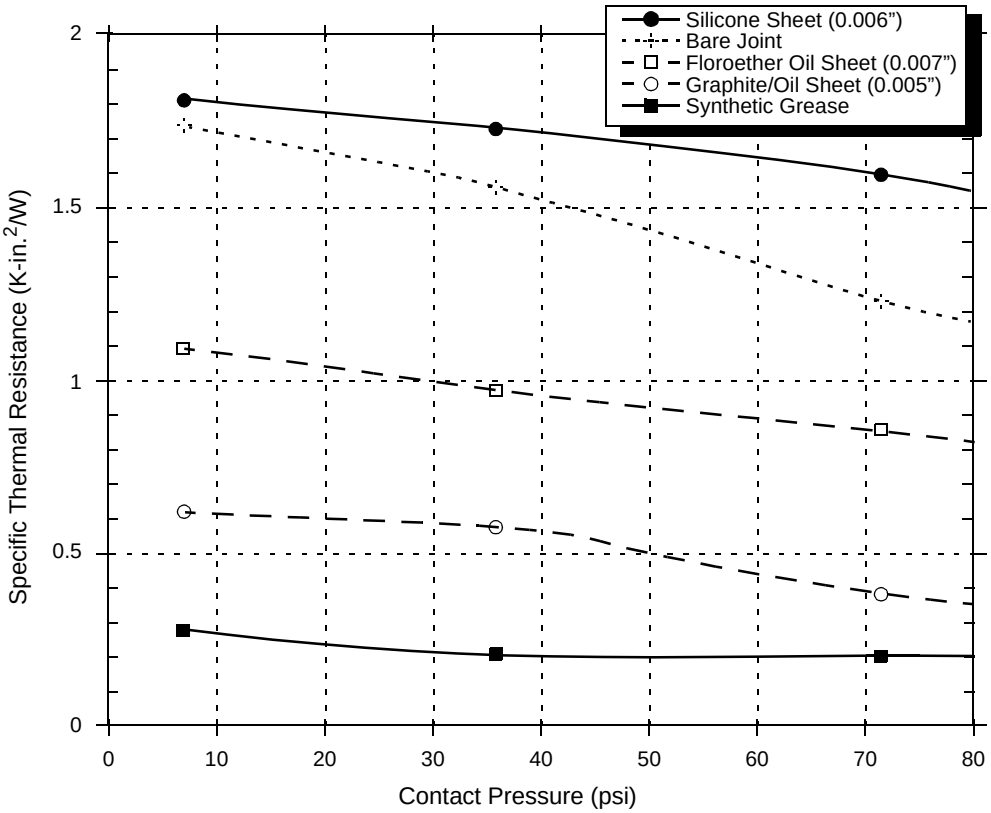


Figure 24. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially-available thermal interfaces and adhesive materials provided by the following vendors:

Chomerics, Inc. 781-935-4850
77 Dragon Court
Woburn, MA 01888-4014
Internet: www.chomerics.com

Dow-Corning Corporation 800-248-2481
Dow-Corning Electronic Materials
2200 W. Salzburg Rd.
Midland, MI 48686-0997
Internet: www.dow.com

Shin-Etsu MicroSi, Inc 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
Thermagon Inc. 4707 Detroit Ave. Cleveland, OH 44102 Internet: www.thermagon.com	888-246-9050

1.8.8.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) \times P_d$$

where:

T_j is the die-junction temperature

T_a is the inlet cabinet ambient temperature

T_r is the air temperature rise within the computer cabinet

θ_{jc} is the junction-to-case thermal resistance

θ_{int} is the adhesive or interface material thermal resistance

θ_{sa} is the heat sink base-to-ambient thermal resistance

P_d is the power dissipated by the device

During operation the die-junction temperatures (T_j) should be maintained less than the value specified in Table 3. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material (θ_{int}) is typically about 1°C/W. Assuming a T_a of 30°C, a T_r of 5°C, a CBGA package θ_{jc} = 0.03, and a power consumption (P_d) of 5.0 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.03°C/W + 1.0°C/W + \theta_{sa}) \times 5.0\ W$

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (θ_{sa}) versus airflow velocity is shown in Figure 25.

Assuming an air velocity of 0.5 m/s, we have an effective R_{sa} of 7°C/W, thus

$$T_j = 30°C + 5°C + (0.03°C/W + 1.0°C/W + 7°C/W) \times 5.0\ W,$$

resulting in a die-junction temperature of approximately 75°C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, The Bergquist Company, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need airflow.

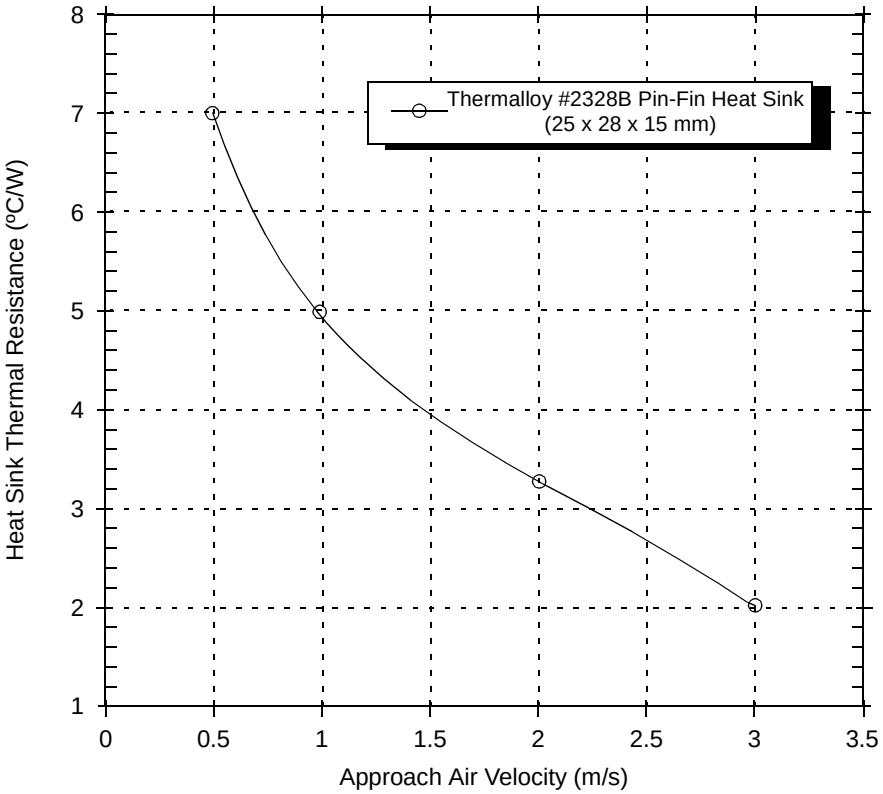


Figure 25. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs.

1.9 Document Revision History

Table 16 provides a revision history for this hardware specification.

Table 16. Document Revision History

Rev. No.	Substantive Change(s)
0	Initial release.
0.1	Minor updates.
0.2	Corrected Section 1.3 General Parameters - Technology from 0.13 µm to 0.18 µm.
	Updated Table 7 - adds power consumption numbers; adds note on estimated decrease w/o AltiVec.
	Updated Table 8 - adds minimun values for Processor frequency and VCO frequency.
	Updated Table 9: Input Setup, Output Valid Times, Output Hold Times, SYSCLK to Output High Impedance.
	Updated Table 11: L2SYNC_IN to high impedance.
	Updated Figure 17 - Mechanical Dimensions, adds capacitor pad dimensions.
0.3	Added 3.3 V support on the processor bus (BVSEL).
	Table 7 - update Typical and Maximum power numbers for Full-On Mode in. Removed note 4. Reworded notes 2 and 3.
	Table 9, Note 2 - removed reference to application note.
	Figure 17 - corrected side view datum A to now be datum C.
	Section 1.8.7 - added $\overline{CI}$ and $\overline{WT}$ to transfer attribute signals requiring pull-ups.
	Section 1.8.7 - added 1 kΩ pull-up recommendation to $\overline{GBL}$ when $\overline{GBL}$ is not connected.
	Table 2 - added pull-down resistance necessary for internally pulled-up voltage select pins. Added 3.3 V support for BVSEL.
	Table 13 - added note 14 for BVSEL, L2VSEL, and $\overline{TRST}$ pins to address pull-down resistance necessary for these internally pulled-up pins to recognize a low signal.
	Table 6 - lowered 2.5 V CV_{IH} from 2.2 V to 2.0 V to be compatible with V_{OH} of the MPC107. Added support for 3.3 V processor bus.
	Table 15 - modified note 1, use L2CR[L2SL] for L2CLK freq. less than 150 MHz.
	Table 8 - revised note 2 discussing for 3.3V bus voltage support.
	Table 14 - added note 5, do not use PLL-off during power-up sequence.
	Table 11 - update Output Hold Times (t_{L2CHOX})

Table 16. Document Revision History (continued)

Rev. No.	Substantive Change(s)
Rev 1.0	Section 1.3 and Table 3 - revised OV_{DD} from 3.3 V ± 100 mV to 3.3 V ± 165 mV.
	Table 13 - removed unsupported PLL configurations.
	Table 13 - added note 15 for minimum $\overline{MCP}$ pulse width, correct note 3 for 3.3 V processor bus support.
	Table 13 - revised note 3 to include emulator tool development.
	Table 14 - removed unsupported Core-to-L2 example frequencies.
	Section 1.8.8 - updated heat sink vendors list.
	Section 1.8.8.2 - updated interface vendors list.
	Table 1 - Updated voltage sequencing requirements notes 3 and 4.
	Table 4 - Updated/added thermal characteristics.
	Table 5 - Removed table and TAU related information, TAU is no longer supported.
	Table 6 - Updated I_{in} and I_{TSI} leakage current specs.
	Section 1.8.3 - “Power Supply Voltage Sequencing” section REMOVED.
	Section 1.10 - Reformatted section.
	Section 1.8.6 - Changed recommended pull-up resistor value to 1 kΩ–5 kΩ. Added $\overline{AACK}$, $\overline{TEA}$, and $\overline{TS}$ to control signals needing pull-ups.
	Section 1.8.7 - Revised text regarding connection of $\overline{TRST}$. Combined Figure 22, Figure 23, and Table 17, into Figure 21.
	Table 7 - Corrected min VCO frequencies from 450 to 700 MHz to match min Processor frequency of 350 MHz.
	Table 2- Added notes 3 to clarify BVSEL for revisions prior to Rev E which do not support 3.3 V OV_{DD}.
	Table 3 - Added notes 5 and 6 to clarify BVSEL for revisions prior to Rev E which do not support 3.3 V OV_{DD}.
	Table 5 - Added note 8 regarding DC voltage limits for JTAG signals.

1.10 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 1.10.1, “Part Numbers Addressed by This Specification.” Section 1.10.2, “Part Numbers Not Fully Addressed by This Document,” lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a part number specification.

1.10.1 Part Numbers Addressed by This Specification

Table 17 provides the Motorola part numbering nomenclature for the MPC7410 Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Motorola sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 17. Part Numbering Nomenclature

MPC	***xxxx***	***xx***	***nnn***	***x***	***x***
Product Code	**Part Identifier**	**Package [1]**	**Processor Frequency [2]**	**Application Modifier**	**Revision Level**
MPC	7410	RX = CBGA	400 450 500	L: 1.8 V ± 100 mV 0 to 105°C	C: 1.2; PVR = 800C 1102 D: 1.3; PVR = 800C 1103 E: 1.4; PVR = 800C 1104

Notes:
1. See Section 1.7, “Package Description” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

1.10.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate part number specifications which supplement and supersede this document; see Table 18.

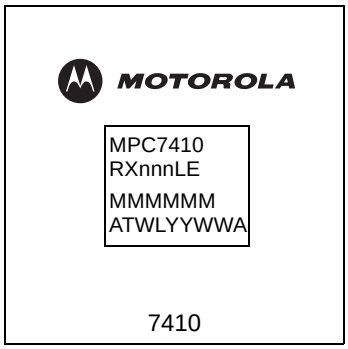
Table 18. Part Numbers with Separate Documentation

Part Number Series	Operating Conditions	Document Order Number of Applicable Specification
MPC7410RX*nnn*PC	2.0 V ± 50 mV, 0° to 65°C	XPC7410PCPNS/D
MPC7410RX*nnn*PD	2.0 V ± 50 mV, 0° to 65°C	XPC7410PDPNS/D
MPC7410RX*nnn*PE	2.0 V ± 50 mV, 0° to 65°C	XPC7410PEPNS/D
MPC7410RX*nnn*NE	1.5 V ± 50 mV, 0° to 105°C	XPC7410NEPNS/D
MPC7410RX*nnn*TE	1.8 V ± 50 mV, -40° to 105°C	MPC7410TEPNS/D

Note: For other differences, see applicable specifications.

1.10.3 Part Marking

Parts are marked as the example shown in Figure 26.



BGA

Notes:

nnn is the speed grade of the part.
MMMMMM is the 6-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 26. Part Marking for BGA Device

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