

Data Book

ADVANCED CLOCK DRIVERS DEVICE DATA BOOK

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*timing
solutions*



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Advanced Clock Drivers Device Data

FOREWORD

This publication includes technical information for the several product families that comprise Motorola Advanced Clock Drivers products. Motorola's broad portfolio of devices support voltage levels from 2.5 V to 5.0 V in both CMOS I/O and various differential I/O technologies. Advanced Clock Drivers are developed by the Motorola Timing Solutions Operations organization.

All devices are listed in alphanumeric order in the *Device Index* of this book. Just turn to the appropriate page for technical details of the known device.

A *Selector Guide* by product family is provided at the beginning of the book to aid you in identifying devices that meet your application and functional

performance requirements.

Complete device specifications are provided in the form of *Data Sheets* which are categorized into the six product types: Clock Generators, Failover / Redundant Clocks, Clock Synthesizers, Zero-Delay Buffers, LVCMOS Fanout Buffers, and Differential Fanout Buffers.

Chapters on *Packaging Information* and *Application Notes* include additional information to aid you in the design process.

The information in this book has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies.

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Advanced Clock Drivers Device Data

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Chapter One

Advanced Clock Drivers Selector Guide

The Advanced Clock Drivers products in this Selector Guide are divided into six categories: Clock Generators, Failover/Redundant Clocks, Clock Synthesizers, Zero-Delay Buffers, LVCMOS Fanout Buffers, and Differential Fanout Buffers. Clock Characteristic Diagrams are also provided.

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Call your local Motorola sales office or distributor to determine Motorola's closest replacement device.

Access Data On-Line

Use the Motorola SPS Internet to access Motorola Semiconductor Product data at www.motorola.com/semiconductors. The SPS Internet provides you with instant access to data sheets, selector guide information, package outlines, on-line technical support and much more.

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Applications Assistance

Applications assistance is available from your nearest Motorola semiconductor sales office or by calling 1-800-521-6274.

Clock Generator Reference Table

1

Introduction

This classification of product uses PLL technology to generate output clocks that are synchronous, and in most cases phase aligned, to an input reference clock. Limited frequency synthesis and zero delay performance is provided.

Device	Processor and application	Temp. Range (°C) (T _A)	VCC (V)	Package	Output frequency range (MHz)	Max output skew (ps)	Max period jitter (ps)	Input	No. of outputs	Status
MPC9315	Telecom/Networking Applications	–40 to 85	3.3/ 2.5	32 LQFP	18 to 200	120	±8 (rms)	2 select-able LVCMOS	8 LVCMOS	P
MPC9330	Pentium or PowerPC603/740/750 Class Processor Designs (on-board crystal oscillator)	0 to 70	3.3	32 LQFP	16 to 200	150	TBD	XTAL or LVCMOS	6 LVCMOS	P
MPC9331	Pentium or PowerPC603/740/750 Class Processor Designs (faster VCO than 930)	0 to 70	3.3	32 LQFP	16 to 200	150	TBD	LVCMOS or LVPECL	6 LVCMOS	P
MPC9350	Networking and Telecommunications Ideal for PowerQUICC II and PowerPC MPC74XX applications	–40 to 85	3.3/ 2.5	32 LQFP	25 to 200	200	—	XTAL or LVCMOS	9 LVCMOS	P
MPC9351	Networking and Telecommunications Ideal for PowerQUICC II and PowerPC MPC74XX applications	–40 to 85	3.3/ 2.5	32 LQFP	25 to 200	100	—	LVCMOS or LVPECL	9 LVCMOS	P
MPC9352	General Purpose or RISC/CSIC Class Processor Designs	–40 to 85	3.3/ 2.5	32 LQFP	16 to 200	150	TBD	LVCMOS	11 LVCMOS	P
MPC93R51	Networking and Telecommunications Ideal for PowerQUICC II and PowerPC MPC74XX applications	0 to 70	3.3	32 LQFP	240	150	15 rms	LVCMOS or LVPECL	9 LVCMOS	P
MPC93R52	General Purpose or RISC/CSIC Class Processor Designs	0 to 70	3.3	32 LQFP	240	200	—	LVCMOS	11 LVCMOS	P
MPC9600	General purpose 2.5 V, high fanout zero delay buffer	–40 to 85	3.3/ 2.5	48 LQFP	25 to 200	150	50	LVCMOS or LVPECL	21 LVCMOS	P
MPC9772	General Purpose or RISC/CSIC Class Designs (independent output enable/disable “lo-power” scheme)	0 to 70	3.3	52 LQFP	25 to 240	300	TBD	XTAL or LVCMOS	12 LVCMOS	P
MPC9773	Pentium or PowerPC603/740/750 Class Designs (output enable/disable “lo-power” scheme)	0 to 70	3.3	52 LQFP	25 to 240	300	TBD	LVCMOS or LVPECL	12 LVCMOS	P
MPC9774	Fault Tolerant (redundant Clock Source needed) Pentium/PowerPC603/740/750/RISC Class Processor Design	0 to 70	3.3	52 LQFP	25 to 125	300	TBD	LVCMOS	15 LVCMOS	P
MPC9850	Designed for PowerQUICC and PowerPC applications. Includes RapidIO clock generation.	–40 to 85	3.3V w/3.3 or 2.5 I/O	100 PBGA	16 to 200	TBD	TBD	LVCMOS or LVPECL	8 LVCMOS 2 LVDS	IN
MPC9893	Systems with clock redundancy needs (high-end computing and telecomm), FAILOVER Clock	–40 to 85	3.3/ 2.5	48 LQFP	25 – 200	TBD	TBD	LVCMOS	9 LVCMOS	S
MPC9992	Pentium or PowerPC603/740/750 Class Designs (output enable/disable “lo-power” scheme)	–40 to 85	3.3/ 2.5	32 LQFP	20 – 400	150	TBD	LVPECL or XTAL	7 Differential Pairs	S
MPC9993	Systems with clock redundancy needs (high-end computing and telecomm) Differential LVPECL 50 MHz to 90 MHz input frequency	–40 to 85	3.3/ 2.5	32 LQFP	50 – 200	150	TBD	LVPECL	5 Differential Pairs	S

Legend:

IN = In Development (TARGET specifications) P = Production (FINAL specifications) S = Sampling (PRELIM specifications)

Clock Generator Reference Table (continued)

1

Device	Processor and application	Temp. Range (°C) (T _A)	VCC (V)	Package	Output frequency range (MHz)	Max output skew (ps)	Max period jitter (ps)	Input	No. of outputs	Status
MC88915FN55	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	0 to 70	5.0	28 PLCC	5 – 55	500	—	CMOS	8 LVCMOS	P
MC88915FN70	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	0 to 70	5.0	28 PLCC	5 – 70	500	—	CMOS	8 LVCMOS	P
MC88915TFN55	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	–40 to 85	5.0	28 PLCC	55	500	—	CMOS	8 LVCMOS	P
MC88915TFN70	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	–40 to 85	5.0	28 PLCC	5 – 70	500	—	CMOS	8 LVCMOS	P
MC88915TFN100	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	–40 to 85	5.0	28 PLCC	5 – 100	500	—	CMOS	8 LVCMOS	P
MC88915TFN133	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	–40 to 85	5.0	28 PLCC	5 – 133	500	—	CMOS	8 LVCMOS	P
MC88915TFN160	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	0 to 70	5.0	28 PLCC	5 – 160	500	—	CMOS	8 LVCMOS	P
MC88LV915TFN	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	0 to 70	3.3	28 PLCC	5 – 100	500	—	CMOS	8 LVCMOS	P
MC88LV926DW	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	0 to 70	3.3	20 SOIC 300 Mil	5 – 133	500	—	CMOS	6 LVCMOS	P
MC88916DW70/80	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	–40 to 85	5.0	20 SOIC 300 Mil	5 – 80	500	—	CMOS	6 LVCMOS	P
MC88920DW	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	–40 to 85	5.0	20 SOIC 300 Mil	5 – 50	500	—	CMOS	6 LVCMOS	P

Legend:

IN = In Development (TARGET specifications) P = Production (FINAL specifications) S = Sampling (PRELIM specifications)

Failover or Redundant Clock Reference Table

Introduction

1

Redundant or Failover Clock Applications are required for high reliability telecommunications, networking and other applications where the loss of a clock source would cause system failure. Clock sources for these applications may be generated by master system clocks and distributed over a backplane to various modules in a pc board, chassis or electronics cabinet.

Device	Processor and application	Temp. Range (°C) (T _A)	VCC (V)	Package	Output frequency range (MHz)	Max output skew (ps)	Max period jitter (ps)	Input	No. of Outputs	Status
MPC9892	Systems with clock redundancy needs (high-end computing and telecomm) Differential LVPECL 50 MHz to 90 MHz input frequency	-40 to 85	3.3	32 LQFP	50 – 200	150	TBD	LVPECL	5 Differential Pairs	S
MPC9893	Systems with clock redundancy needs (high-end computing and telecomm), FAILOVER Clock	-40 to 85	3.3	48 LQFP	25 – 200	TBD	TBD	LVC MOS	9 LVC MOS	S
MPC9894	4 input redundant clock with I2C configuration interface	-40 to 105 (T _J)	3.3/ 2.5	100 PBGA	21.25 to 340	TBD	TBD	LVPECL	8 LVPECL	IN
MPC9895	Systems with clock redundancy needs (high-end computing and telecomm), FAILOVER Clock with restore function	-40 to 85	3.3	100 PBGA	25 – 200	TBD	TBD	LVC MOS	9 LVC MOS	S
MPC9993	Systems with clock redundancy needs (high-end computing and telecomm) Differential LVPECL 50 MHz to 90 MHz input frequency	-40 to 85	3.3	32 LQFP	50 – 200	150	TBD	LVPECL	5 Differential Pairs	S

Legend:

IN = In Development (TARGET specifications) P = Production (FINAL specifications) S = Sampling (PRELIM specifications)

Clock Synthesizer Reference Table

Introduction

This classification of products uses PLL technology to synthesize high frequency clocks from low cost crystal sources. Programmable frequency steps are typically 1 MHz or less with output frequencies as high as 800 MHz.

1

Device	Processor and application	Temp. Range (°C) (T _A)	VCC (V)	Package	Output frequency range (MHz)	Max period jitter (ps)	Input	Outputs	Status
MPC926508	Clock synthesizer for networking applications (Pin compatible with ICS650-08)	-40 to 85	3.3	20 TSSOP	100/133	TBD	XTAL or LVCMOS	LVCMOS	IN
MPC9229	Clock source for 25 MHz to 450 MHz processor designs (serial and/or parallel) 1 MHz steps	0 to 70	3.3	28 PLCC 32 LQFP	400	25	XTAL	LVPECL	P
MPC9230	Clock source for 50 MHz to 900 MHz processor designs (serial and/or parallel) 1 MHz steps	0 to 70	3.3	28 PLCC 32 LQFP	800	25	XTAL or LVCMOS	LVPECL	P
MPC9239	Clock source for 50 MHz to 900 MHz processor designs (serial and/or parallel) 16.66 MHz steps	0 to 70	3.3	28 PLCC 32 LQFP	900	25	XTAL or LVCMOS	LVPECL	P
MPC9259	Clock source for 50 MHz to 900 MHz processor designs (serial or parallel) 16.66 MHz steps	0 to 70	3.3	32 LQFP	900	25	XTAL or LVCMOS	LVDS	S

Legend:

IN = In Development (TARGET specifications) P = Production (FINAL specifications) S = Sampling (PRELIM specifications)

Zero-Delay Buffer Reference Table

Introduction

1

This classification of products uses PLL technology to reproduce exact copies, in frequency and phase, of the input reference clock. These specialized products provide superior AC performance to clock generators, but lack any frequency synthesis capabilities.

Device	Processor and application	Temp. Range (°C) (T _A)	VCC (V)	Package	Output frequency range (MHz)	Max output skew (ps)	Max period jitter (ps)	Input	Outputs	Status
MPC962305	General Purpose Zero-delay applications. (Pin compatible with CY2305/CY23S05)	0 to 70 or -40 to 85	3.3	8 SOIC 8 TSSOP 16 SOIC 16 TSSOP	133	250	200	LVC MOS	8 LVC MOS	IN
MPC962308	General Purpose Zero-delay applications. (Pin compatible with CY2308/CY23S08)	0 to 70 or -40 to 85	3.3	16 SOIC 16 TSSOP	133	200	200	LVC MOS	4 + feed-back LVC MOS	IN
MPC962309	General Purpose Zero-delay applications. (Pin compatible with CY2309/CY23S09)	0 to 70 or -40 to 85	3.3	8 SOIC 8 TSSOP 16 SOIC 16 TSSOP	133	250	200	LVC MOS	8 + feed-back LVC MOS	IN
MPC9608	General Purpose Zero-delay applications, Companion to Power-QUICK and PPC designs, DRAM applications	-40 to 85	3.3/ 2.5	32 LQFP	12.5 to 200	150	10 (RMS)	LVC MOS	10 LVC MOS	IN
MPC9653	High Performance Clock Tree Design, PC100SDRAM	-40 to 85	3.3/ 2.5	32 LQFP	200	150	TBD	LVPECL Ref LVC MOS fdbk	8 + feed-back LVC MOS	P
MPC9658	Very High Performance Clock Tree Design up to 200 MHz, PC100SDRAM	-40 to 85	3.3/ 2.5	32 LQFP	200	150	TBD	LVPECL Ref LVC MOS fdbk	10 + feed-back LVC MOS	P
MPC961C	General Purpose also Power-QUICC: Zero-delay applications (CMOS clock signal retiming without insertion delay) DRAM driver	-40 to 85	3.3/ 2.5	32 LQFP	50 to 200	150	10 (RMS)	LVC MOS Ref LVC MOS fdbk	17 + feed-back LVC MOS	P
MPC961P	Zero-delay applications (PECL clock signal retiming without insertion delay)	-40 to 85	3.3/ 2.5	32 LQFP	50 to 200	150	10 (RMS)	LVPECL Ref LVC MOS fdbk	17 + feed-back LVC MOS	P

Legend:

IN = In Development (TARGET specifications) P = Production (FINAL specifications) S = Sampling (PRELIM specifications)

LVC MOS Fanout Buffer Reference Table

Introduction

This classification of product uses digital circuitry to produce multiple copies of its input clock. In some cases the output frequencies will be divided down versions of the input clock.

1

Device	Processor and application	Temp. Range (°C) (Ambient)	VCC (V)	Package	Max output frequency (MHz)	Max output skew (ps)	Max part-part skew (ns)	Input	Outputs	Status
MPC905	Pentium PCI Processor Bus Clock or PCI Bus Hi-Speed Transmission Line Driver	0 to 70	3.3	16 SOIC	100	500	—	XTAL or external LVC MOS	6	P
MPC940L	General Purpose or RISC/CSIC PCI Clock Distribution to Synchronous Memory (better performance than MPC9109)	0 to 70	3.3/2.5	32 QFP/LQFP	250	150	1.7	LVPECL or LVC MOS	18	P
MPC941	General Purpose or RISC/CSIC PCI Clock Distribution to Synchronous Memory (more outputs than MPC940)	−40 to 85	3.3/2.5	48 QFP	250	250	1.2	LVPECL or LVC MOS	27	P
MPC942C	Pentium II and other high performance synchronous designs (CMOS inputs)	0 to 70	3.3/2.5	32 LQFP	250	250	1	LVTTTL or LVC MOS	18	P
MPC942P	Pentium II and other high performance synchronous designs (PECL inputs)	0 to 70	3.3/2.5	32 LQFP	250	250	1	LVPECL	18	P
MPC9443	Low Voltage High-performance Telecom, Networking and computing Applications	−40 to 85	3.3/2.5 †	48 LQFP	250	200	—	LVPECL or LVC MOS	16	P
MPC9446	Low Voltage Mid-range and High-performance Telecom, Networking and Computing Applications	−40 to 85	3.3/2.5 †	32 LQFP	250	200	—	LVC MOS	10	P
MPC9447	General Purpose or RISC/CSIC Class Processor Clock Fanout for L2 Cache	−40 to 85	3.3/2.5	32 LQFP	275	150	TBD	LVTTTL	9	P
MPC9448	General Purpose or RISC/CSIC Class Processor Clock Fanout for L2 Cache (faster & more outputs than the MPC947)	−40 to 85	3.3/2.5	32 LQFP	275	150	TBD	LVPECL or LVC MOS	12	P
MPC9449	General Purpose or RISC/CSIC Class Processor PCI Clock Distribution to Synch Memory (5 more outputs than the MPC946)	−40 to 85	3.3/2.5	52 LQFP	200	200	TBD	LVPECL or LVC MOS	15	P
MPC9456	Low Voltage Mid-range and High-performance Telecom, Networking and Computing Applications	−40 to 85	3.3/2.5 †	32 LQFP	250	250	—	LVPECL	10	P

† Supports single and mixed mode power supply

Legend:

IN = In Development (TARGET specifications) P = Production (FINAL specifications) S = Sampling (PRELIM specifications)

Differential Fanout Buffer Reference Table

1

Introduction

This classification of product uses digital circuitry to produce multiple copies of its input clock. In some cases the output frequencies will be divided down versions of the input clock.

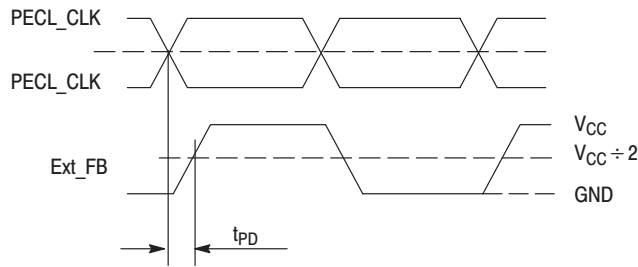
Device	Processor and application	Temp. Range (°C) (T _J)	VCC (V)	Package	Max part-part skew	Max output Skew (ps)	Output technology	Input	Outputs	Status
MC100ES6011	ECL 1:2 Differential Fanout Buffer	–40 to 85 (T _A)	3.3/2.5	8 SOIC 8 TSSOP	TBD	TBD	LVPECL	ECL	1:2	IN
MC100ES6014	1:5 Differential ECL/PECL/HSTL Clock Driver	–40 to 85 (T _A)	3.3/2.5	20 TSSOP	TBD	TBD	LVPECL	ECL/ PECL or HSTL	1:5	IN
MC100ES6056	ECL Dual Differential 2:1 Multiplexer	–40 to 85 (T _A)	3.3	20 SOIC 20 TSSOP	TBD	TBD	LVPECL	ECL	Dual 2:1	IN
MC100ES6111	Clock distribution schemes requiring “very low” part-to-part and output-to-output skews	0 to 110	3.3/2.5	32 LQFP	TBD	35	3 GHz LVPECL	ECL/ LVPECL or HSTL	1:10	P
MC100ES6139	ECL ÷ 2/4, ÷ 4/5/6 Clock Generation Chip	–40 to 85 (T _A)	3.3	20 SOIC 20 TSSOP	TBD	TBD	LVPECL	ECL	1:6	IN
MC100ES6210	Clock distribution schemes requiring “very low” part-to-part and output-to-output skews	0 to 110	3.3/2.5	32 LQFP	TBD	35	3 GHz LVPECL	ECL/ LVPECL	Dual 1:5	P
MC100ES6220	LV/PECL Designs needing low skew. Telecom Back-Bone Equipment, Semi Test Equipment	0 to 110	3.3/2.5	52 LQFP exposed pad	TBD	50	3 GHz LVPECL	ECL/ LVPECL	Dual 1:10 DIFF	P
MC100ES6221	LV/PECL Designs needing low skew. Telecom Back-Bone Equipment, Semi Test Equipment	0 to 110	3.3/2.5	52 LQFP exposed pad	TBD	50	3 GHz LVPECL	ECL/ LVPECL	1:20 DIFF	P
MC100ES6222	LV/PECL Designs needing low skew. Telecom Back-Bone Equipment, Semi Test Equipment	0 to 110	3.3/2.5	52 LQFP exposed pad	TBD	50	3 GHz LVPECL	ECL/ LVPECL	1:15 DIFF	P
MC100ES6226	Clock distribution schemes requiring “extremely low” part-to-part and output-to-output skews	0 to 110	3/2.5	32 LQFP	TBD	35	3 GHz LVPECL	LVPECL	1:9	P
MC100ES6254	Differential 2x2 clock switch and Fanout Buffer	0 to 110	3/2.5	32 LQFP	TBD	35	3 GHz LVPECL	LVPECL	Single 1:6 or Double 1:3	P
MC100ES7111	Clock distribution schemes requiring very low part-to-part and output-to-output skews	–40 to 110	3.3	32 LQFP	TBD	TBD	LVDS	LVPECL HSTL LVDS	1:10	IN
MC100ES8111	Clock distribution schemes requiring “extremely low” part-to-part and output-to-output skews	0 to 110	3.3	32 LQFP	200	50	HSTL	HSTL or LVPECL	1:10	S

Legend:

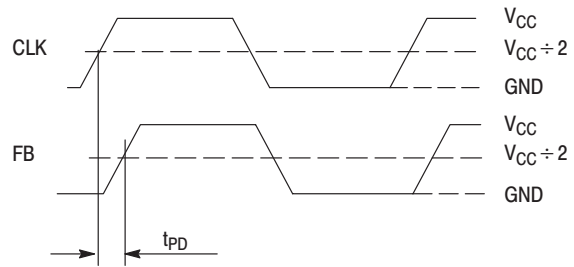
IN = In Development (TARGET specifications) P = Production (FINAL specifications) S = Sampling (PRELIM specifications)

Clock Characteristic Diagrams

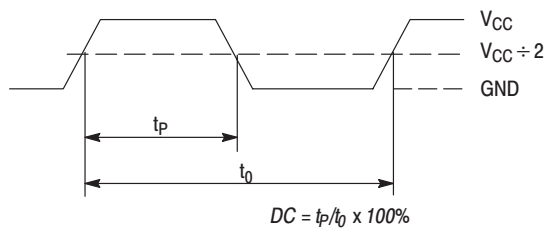
1



Propagation delay (t_{PD} , static phase offset) test reference (PECL)

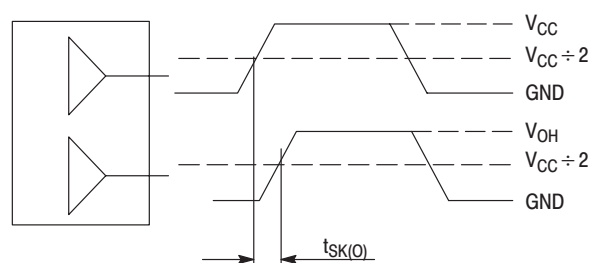


Propagation delay (t_{PD} , static phase offset) test reference (CMOS)



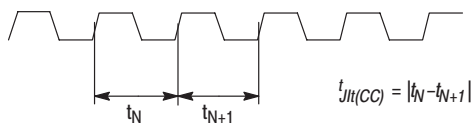
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Output Duty Cycle (DC)



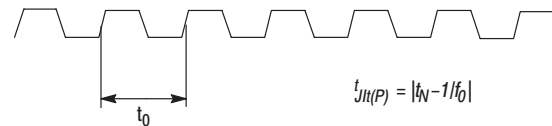
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Output-to-output Skew $t_{SK(O)}$



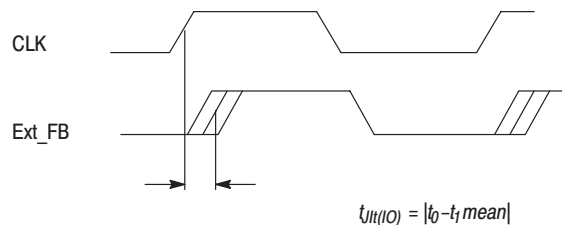
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Cycle-to-cycle Jitter



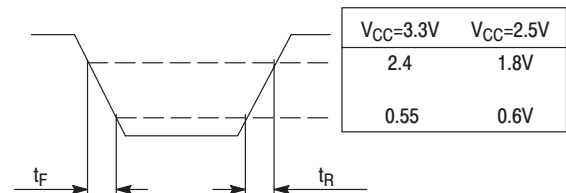
The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Period Jitter



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

I/O (Phase) Jitter



Transition Time Test Reference

Chapter Two

Clock Generator Data Sheets

Clock Generator Device Index

Device Number	Page	Device Number	Page
MC88915T	12	MPC952	168
MC88LV915T	31	MPC9600	174
MC88LV926	40	MPC972	186
MPC930	49	MPC973	198
MPC931	49	MPC974	210
MPC9315	61	MPC9772	216
MPC932	72	MPC9773	230
MPC9330	78	MPC9774	245
MPC9331	88	MPC9850	255
MPC9350	98	MPC990	263
MPC9351	107	MPC991	270
MPC9352	117	MPC992	276
MPC93R51	130	MPC9952	282
MPC93R52	139	MPC9990	287
MPC950	150	MPC9992	297
MPC951	160		

Low Skew CMOS PLL Clock Drivers, 3-State 55, 70, 100, 133 and 160MHz Versions

The MC88915T Clock Driver utilizes phase-locked loop technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for high performance PC's and workstations. For a 3.3V version, see the MC88LV915T data sheet.

The PLL allows the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple components on a board. The PLL also allows the MC88915T to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency. Multiple 88915's can lock onto a single reference clock, which is ideal for applications when a central system clock must be distributed synchronously to multiple boards (see Figure 7).

Five "Q" outputs (Q0–Q4) are provided with less than 500 ps skew between their rising edges. The $\overline{Q5}$ output is inverted (180° phase shift) from the "Q" outputs. The 2X_Q output runs at twice the "Q" output frequency, while the Q/2 runs at 1/2 the "Q" frequency.

The VCO is designed to run optimally between 20 MHz and the 2X_Q F_{max} specification. The wiring diagrams in Figure 5 detail the different feedback configurations which create specific input/output frequency relationships. Possible frequency ratios of the "Q" outputs to the SYNC input are 2:1, 1:1, and 1:2.

The FREQ_SEL pin provides one bit programmable divide-by in the feedback path of the PLL. It selects between divide-by-1 and divide-by-2 of the VCO before its signal reaches the internal clock distribution section of the chip (see the block diagram on page 2). In most applications FREQ_SEL should be held high (+1). If a low frequency reference clock input is used, holding FREQ_SEL low (+2) will allow the VCO to run in its optimal range (>20MHz and >40MHz for the TFN133 version).

In normal phase-locked operation the PLL_EN pin is held high. Pulling the PLL_EN pin low disables the VCO and puts the 88915 in a static "test mode". In this mode there is no frequency limitation on the input clock, which is necessary for a low frequency board test environment. The second SYNC input can be used as a test clock input to further simplify board-level testing (see detailed description on page 11).

Pulling the $\overline{OE/RST}$ pin low puts the clock outputs 2X_Q, Q0–Q4, $\overline{Q5}$ and Q/2 into a high impedance state (3-state). After the $\overline{OE/RST}$ pin goes back high Q0–Q4, $\overline{Q5}$ and Q/2 will be reset in the low state, with 2X_Q being the inverse of the selected SYNC input. Assuming PLL_EN is low, the outputs will remain reset until the 88915 sees a SYNC input pulse.

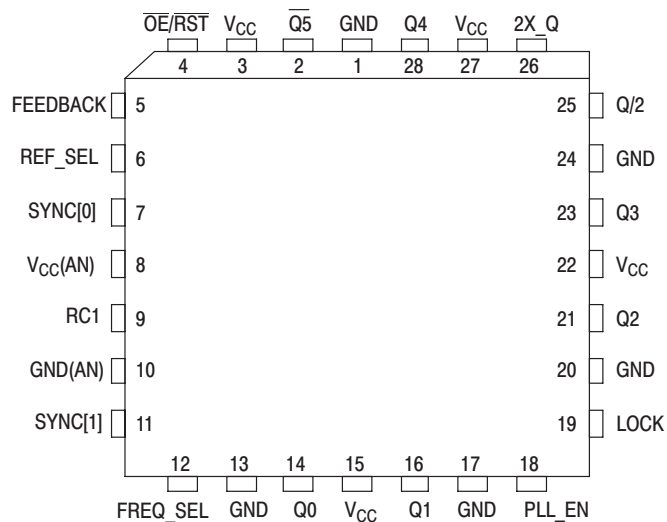
A lock indicator output (LOCK) will go high when the loop is in steady-state phase and frequency lock. The LOCK output will go low if phase-lock is lost or when the PLL_EN pin is low. The LOCK output will go high no later than 10ms after the 88915 sees a SYNC signal and full 5V V_{CC} .

Features

- Five Outputs (Q0–Q4) with Output–Output Skew < 500 ps each being phase and frequency locked to the SYNC input
- The phase variation from part-to-part between the SYNC and FEEDBACK inputs is less than 550 ps (derived from the t_{PD} specification, which defines the part-to-part skew)
- Input/Output phase-locked frequency ratios of 1:2, 1:1, and 2:1 are available
- Input frequency range from 5MHz – 2X_Q F_{MAX} spec. (10MHz – 2X_Q F_{MAX} for the TFN133 version)
- Additional outputs available at 2X and +2 the system "Q" frequency. Also a $\overline{Q}$ (180° phase shift) output available
- All outputs have ± 36 mA drive (equal high and low) at CMOS levels, and can drive either CMOS or TTL inputs. All inputs are TTL-level compatible. ± 88 mA I_{OL}/I_{OH} specifications guarantee 50 Ω transmission line switching on the incident edge
- Test Mode pin (PLL_EN) provided for low frequency testing. Two selectable CLOCK inputs for test or redundancy purposes. All outputs can go into high impedance (3-state) for board test purposes
- Lock Indicator (LOCK) accuracy indicates a phase-locked state

MC88915TFN55
MC88915TFN70
MC88915TFN100
MC88915TFN133
MC88915TFN160

**LOW SKEW CMOS
PLL CLOCK DRIVER**

Pinout: 28-Lead PLCC (Top View)

FN SUFFIX
 PLASTIC PLCC
 CASE 776-02

PIN SUMMARY

Pin Name	Num	I/O	Function
SYNC[0]	1	Input	Reference clock input
SYNC[1]	1	Input	Reference clock input
REF_SEL	1	Input	Chooses reference between sync[0] & Sync[1]
FREQ_SEL	1	Input	Doubles VCO Internal Frequency (low)
FEEDBACK	1	Input	Feedback input to phase detector
RC1	1	Input	Input for external RC network
Q(0-4)	5	Output	Clock output (locked to sync)
$\overline{Q5}$	1	Output	Inverse of clock output
2x_Q	1	Output	2 x clock output (Q) frequency (synchronous)
Q/2	1	Output	Clock output(Q) frequency $\div 2$ (synchronous)
LOCK	1	Output	Indicates phase lock has been achieved (high when locked)
$\overline{OE/RST}$	1	Input	Output Enable/Asynchronous reset (active low)
PLL_EN	1	Input	Disables phase-lock for low freq. testing
V _{CC} , GND	11		Power and ground pins (note pins 8, 10 are "analog" supply pins for internal PLL only)

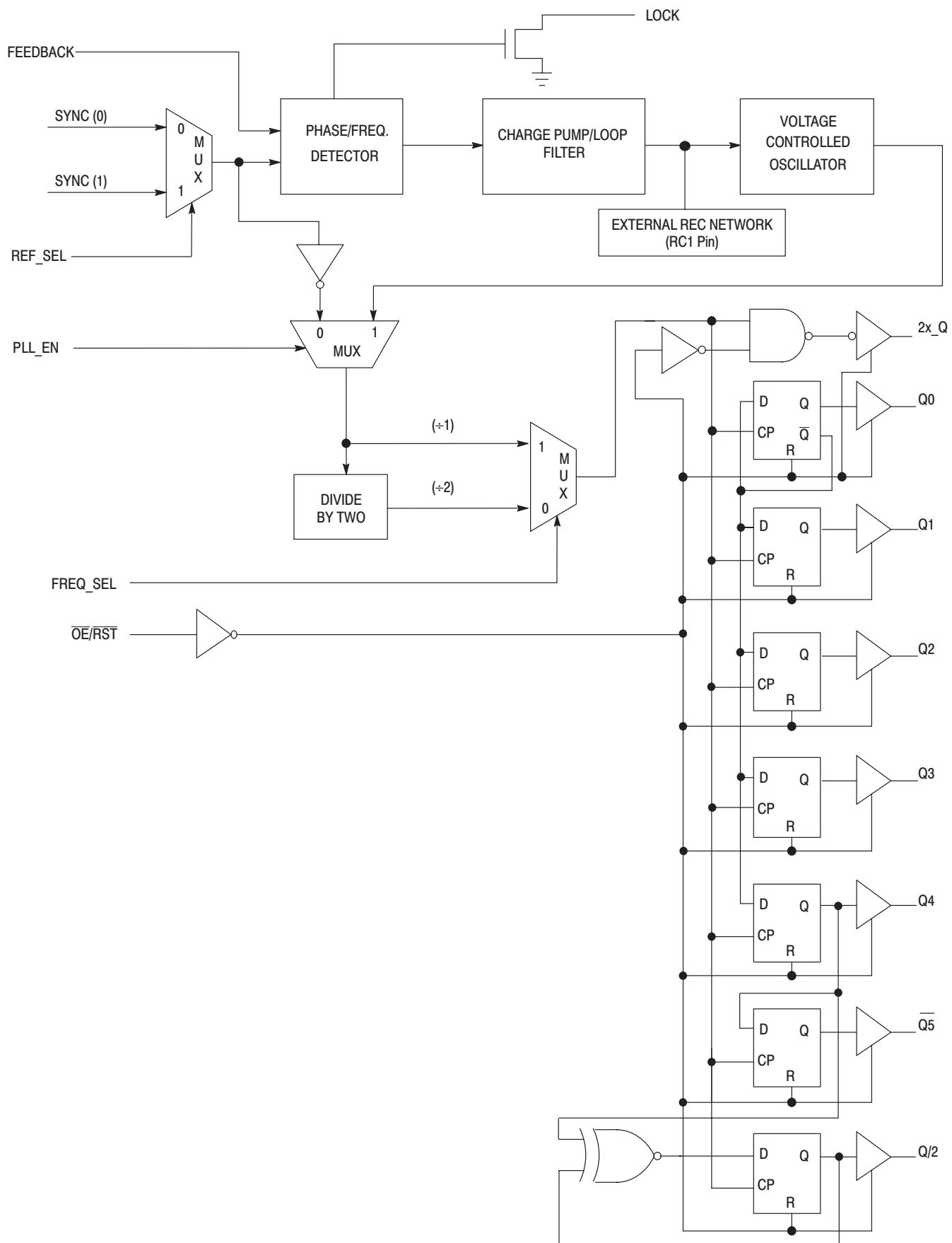


Figure 1. MC88915T Block Diagram (All Versions)

MC88915TFN55 and MC88915TFN70

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum		Maximum	Unit
		TFN70	TFN55		
$t_{RISE/FALL, SYNC}$ Inputs	Rise/Fall Time, SYNC Inputs From 0.8 to 2.0V	—	—	3.0	ns
t_{CYCLE} , SYNC Inputs	Input Clock Period SYNC Inputs	28.5 ¹	36.0 ¹	200 ²	ns
Duty Cycle SYNC Inputs	Input Duty Cycle SYNC Inputs	50% $\pm$ 25%			

1. These t_{CYCLE} minimum values are valid when 'Q' output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 5b.
2. Information in Table 1 and in Note 3 of the AC specification notes describe this specification and its limits depending on what output is fed back, and if FREQ_SEL is high or low.

DC ELECTRICAL CHARACTERISTICS

(Voltages Referenced to GND) $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ for 55MHz Version; $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ for 70MHz Version; $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions	V_{CC} V	Target Limit	Unit
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$	4.75 5.25	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$	4.75 5.25	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $I_{OH} = -36\text{mA}$ ¹	4.75 5.25	4.01 4.51	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $I_{OL} = 36\text{mA}$ ¹	4.75 5.25	0.44 0.44	V
I_{in}	Maximum Input Leakage Current	$V_I = V_{CC}$ or GND	5.25	± 1.0	μA
I_{CCT}	Maximum I_{CC} /Input	$V_I = V_{CC} - 2.1\text{V}$	5.25	2.0 ²	mA
I_{OLD}	Minimum Dynamic Output Current ³	$V_{OLD} = 1.0\text{V}$ Max	5.25	88	mA
I_{OHD}		$V_{OHD} = 3.85\text{V}$ Min	5.25	-88	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_I = V_{CC}$ or GND	5.25	1.0	mA
I_{OZ}	Maximum 3-State Leakage Current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND	5.25	± 50 ⁴	μA

1. I_{OL} and I_{OH} are 12mA and -12mA respectively for the LOCK output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration is 2.0ms, one output loaded at a time.
4. Specification value for I_{OZ} is preliminary, will be finalized upon 'MC' status.

CAPACITANCE AND POWER SPECIFICATIONS

Symbol	Parameter	Typical Values	Unit	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0\text{V}$
C_{PD}	Power Dissipation Capacitance	40	pF	$V_{CC} = 5.0\text{V}$
PD_1	Power Dissipation @ 50MHz with 50 Ω Thevenin Termination	23mW/Output 184mW/Device	mW	$V_{CC} = 5.0\text{V}$ $T = 25^\circ\text{C}$
PD_2	Power Dissipation @ 50MHz with 50 Ω Parallel Termination to GND	57mW/Output 456mW/Device	mW	$V_{CC} = 5.0\text{V}$ $T = 25^\circ\text{C}$

NOTE: PD_1 and PD_2 mW/Output numbers are for a 'Q' output.

MC88915TFN55 and MC88915TFN70 (continued)

FREQUENCY SPECIFICATIONS ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$)

Symbol	Parameter	Guaranteed Minimum		Unit
		TFN70	TFN55	
$f_{\max}^1$	Maximum Operating Frequency (2X_Q Output)	70	55	MHz
	Maximum Operating Frequency (Q0–Q4, Q5 Output)	35	27.5	MHz

1. Maximum Operating Frequency is guaranteed with the part in a phase-locked condition, and all outputs loaded with 50Ω terminated to $V_{CC}/2$.

AC CHARACTERISTICS ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$, Load = 50Ω Terminated to $V_{CC}/2$)

Symbol	Parameter	Min	Max	Unit	Condition
t _{RISE/FALL} Outputs	Rise/Fall Time, All Outputs (Between 0.2V _{CC} and 0.8V _{CC})	1.0	2.5	ns	Into a 50Ω Load Terminated to V _{CC} /2
t _{RISE/FALL} ¹ 2X_Q Output	Rise/Fall Time Into a 20pF Load, With Termination Specified in Note ²	0.5	1.6	ns	t _{RISE} : 0.8V – 2.0V t _{FALL} : 2.0V – 0.8V
t _{PULSE WIDTH} ¹ (Q0–Q4, Q ₅ , Q/2)	Output Pulse Width: Q0, Q1, Q2, Q3, Q4, Q ₅ , Q/2 @ V _{CC} /2	0.5t _{CYCLE} – 0.5 ²	0.5t _{CYCLE} + 0.5 ²	ns	Into a 50Ω Load Terminated to V _{CC} /2
t _{PULSE WIDTH} ¹ (2X_Q Output)	Output Pulse Width: 2X_Q @ 1.5V 66MHZ 50MHZ 40MHZ	0.5t _{CYCLE} – 0.5 ² 0.5t _{CYCLE} – 1.0 0.5t _{CYCLE} – 1.5	0.5t _{CYCLE} + 0.5 ² 0.5t _{CYCLE} + 1.0 0.5t _{CYCLE} + 1.5	ns	Must Use Termination Specified in Note ²
t _{PULSE WIDTH} ¹ (2X_Q Output)	Output Pulse Width: 2X_Q @ V _{CC} /2 50–65MHZ 40–49MHZ 66–70MHZ	0.5t _{CYCLE} – 1.0 ² 0.5t _{CYCLE} – 1.5 0.5t _{CYCLE} – 0.5	0.5t _{CYCLE} + 1.0 ² 0.5t _{CYCLE} + 1.5 0.5t _{CYCLE} + 0.5	ns	Into a 50Ω Load Terminated to V _{CC} /2
t _{PD} ^{1,3} SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)	(With 1MΩ from RC1 to An V _{CC})		ns	See Note ⁴ and Figure 2 for Detailed Explanation
		–1.05	–0.40		
		(With 1MΩ from RC1 to An GND)			
		+1.25	+3.25		
t _{SKEW_r} ^{1,4} (Rising) See Note ⁵	Output-to-Output Skew Between Out- puts Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to V _{CC} /2
t _{SKEW_f} ^{1,4} (Falling)	Output-to-Output Skew Between Out- puts Q0–Q4 (Falling Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to V _{CC} /2
t _{SKEW_{all}} ^{1,4}	Output-to-Output Skew 2X_Q, Q/2, Q0–Q4 Rising, Q ₅ Falling	—	750	ps	All Outputs Into a Matched 50Ω Load Terminated to V _{CC} /2
t _{LOCK} ⁵	Time Required to Acquire Phase-Lock From Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
t _{PZL} ⁶	Output Enable Time $\overline{\text{OE}}/\text{RST}$ to 2X_Q, Q0–Q4, Q ₅ , and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low
t _{PHZ} , t _{PLZ} ⁶	Output Disable Time $\overline{\text{OE}}/\text{RST}$ to 2X_Q, Q0–Q4, Q ₅ , and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low

1. These specifications are not tested, they are guaranteed by statistical characterization. See AC specification Note 1.

2. t_{CYCLE} in this spec is $1/\text{Frequency}$ at which the particular output is running.

3. The t_{PD} specification's min/max values may shift closer to zero if a larger pullup resistor is used.

4. Under equally loaded conditions and at a fixed temperature and voltage.

5. With V_{CC} fully powered-on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with $C1 = 0.1\mu\text{F}$, t_{LOCK} minimum is with $C1 = 0.01\mu\text{F}$.

6. The t_{PZL} , t_{PHZ} , t_{PLZ} minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

MC88915TFN100

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL, SYNC}$ Inputs	Rise/Fall Time, SYNC Inputs From 0.8 to 2.0V	—	3.0	ns
$t_{CYCLE, SYNC}$ Inputs	Input Clock Period SYNC Inputs	20.0 ¹	200 ²	ns
Duty Cycle SYNC Inputs	Input Duty Cycle SYNC Inputs	50% $\pm$ 25%		

- These t_{CYCLE} minimum values are valid when 'Q' output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 5b.
- Information in Table 1 and in Note 3 of the AC specification notes describe this specification and its limits depending on what output is fed back, and if FREQ_SEL is high or low.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND) $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions	V_{CC} V	Target Limit	Unit
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$	4.75 5.25	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$	4.75 5.25	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $I_{OH} = -36\text{mA}$ ¹	4.75 5.25	4.01 4.51	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $I_{OL} = 36\text{mA}$ ¹	4.75 5.25	0.44 0.44	V
I_{in}	Maximum Input Leakage Current	$V_I = V_{CC}$ or GND	5.25	± 1.0	μA
I_{CCT}	Maximum I_{CC} /Input	$V_I = V_{CC} - 2.1\text{V}$	5.25	2.0 ²	mA
I_{OLD}	Minimum Dynamic Output Current ³	$V_{OLD} = 1.0\text{V}$ Max	5.25	88	mA
I_{OHD}		$V_{OHD} = 3.85\text{V}$ Min	5.25	-88	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_I = V_{CC}$ or GND	5.25	1.0	mA
I_{OZ}	Maximum 3-State Leakage Current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND	5.25	± 50 ⁴	μA

- I_{OL} and I_{OH} are 12mA and -12mA respectively for the LOCK output.
- The PLL_EN input pin is not guaranteed to meet this specification.
- Maximum test duration is 2.0ms, one output loaded at a time.
- Specification value for I_{OZ} is preliminary, will be finalized upon 'MC' status.

CAPACITANCE AND POWER SPECIFICATIONS

Symbol	Parameter	Typical Values	Unit	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0\text{V}$
C_{PD}	Power Dissipation Capacitance	40	pF	$V_{CC} = 5.0\text{V}$
PD_1	Power Dissipation @ 50MHz with 50 Ω Thevenin Termination	23mW/Output 184mW/Device	mW	$V_{CC} = 5.0\text{V}$ $T = 25^\circ\text{C}$
PD_2	Power Dissipation @ 50MHz with 50 Ω Parallel Termination to GND	57mW/Output 456mW/Device	mW	$V_{CC} = 5.0\text{V}$ $T = 25^\circ\text{C}$

NOTE: PD_1 and PD_2 mW/Output numbers are for a 'Q' output.

FREQUENCY SPECIFICATIONS ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$)

Symbol	Parameter	Guaranteed Minimum	Unit
		TFN100	
f _{max} ¹	Maximum Operating Frequency (2X_Q Output)	100	MHz
	Maximum Operating Frequency (Q0–Q4, $\overline{Q5}$ Output)	50	MHz

- Maximum Operating Frequency is guaranteed with the part in a phase-locked condition, and all outputs loaded with 50 Ω terminated to $V_{CC}/2$.

MC88915TFN100 (continued)

AC CHARACTERISTICS ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$, Load = 50Ω Terminated to $V_{CC}/2$)

Symbol	Parameter	Min	Max	Unit	Condition
t _{RISE/FALL} Outputs	Rise/Fall Time, All Outputs (Between 0.2V _{CC} and 0.8V _{CC})	1.0	2.5	ns	Into a 50Ω Load Terminated to V _{CC} /2
t _{RISE/FALL} ¹ 2X_Q Output	Rise/Fall Time Into a 20pF Load, With Termination Specified in Note ²	0.5	1.6	ns	t _{RISE} : 0.8V – 2.0V t _{FALL} : 2.0V – 0.8V
t _{PULSE WIDTH} ¹ (Q0–Q4, Q̅5, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q3, Q4, Q̅5, Q/2 @ V _{CC} /2	0.5t _{CYCLE} – 0.5 ²	0.5t _{CYCLE} + 0.5 ²	ns	Into a 50Ω Load Terminated to V _{CC} /2
t _{PULSE WIDTH} ¹ (2X_Q Output)	Output Pulse Width: 2X_Q @ 1.5V	0.5t _{CYCLE} – 0.5 ²	0.5t _{CYCLE} + 0.5 ²	ns	Must Use Termination Specified in Note ²
t _{PULSE WIDTH} ¹ (2X_Q Output)	Output Pulse Width: 40–49MHz 50–65MHz 66–100MHz	0.5t _{CYCLE} – 1.5 ² 0.5t _{CYCLE} – 1.0 0.5t _{CYCLE} – 0.5	0.5t _{CYCLE} + 1.5 ² 0.5t _{CYCLE} + 1.0 0.5t _{CYCLE} + 0.5	ns	Into a 50Ω Load Terminated to V _{CC} /2
t _{PD} ^{1,3} SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)	(With 1MΩ from RC1 to An V _{CC})		ns	See Note ⁴ and Figure 2 for Detailed Explanation
		–1.05	–0.30		
		(With 1MΩ from RC1 to An GND)			
		+1.25	+3.25		
t _{SKEW_r} ^{1,4} (Rising) See Note ⁵	Output–to–Output Skew Between Out- puts Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to V _{CC} /2
t _{SKEW_f} ^{1,4} (Falling)	Output–to–Output Skew Between Out- puts Q0–Q4 (Falling Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to V _{CC} /2
t _{SKEW_{all}} ^{1,4}	Output–to–Output Skew 2X_Q, Q/2, Q0–Q4 Rising, Q̅5 Falling	—	750	ps	All Outputs Into a Matched 50Ω Load Terminated to V _{CC} /2
t _{LOCK} ⁵	Time Required to Acquire Phase–Lock From Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
t _{PZL} ⁶	Output Enable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0–Q4, Q̅5, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low
t _{PHZ} , t _{PLZ} ⁶	Output Disable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0–Q4, Q̅5, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low

1. These specifications are not tested, they are guaranteed by statistical characterization. See AC specification Note 1.

2. T_{CYCLE} in this spec is $1/\text{Frequency}$ at which the particular output is running.

3. The T_{PD} specification's min/max values may shift closer to zero if a larger pullup resistor is used.

4. Under equally loaded conditions and at a fixed temperature and voltage.

5. With V_{CC} fully powered-on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with $C1 = 0.1\mu\text{F}$, t_{LOCK} minimum is with $C1 = 0.01\mu\text{F}$.

6. The t_{PZL} , t_{PHZ} , t_{PLZ} minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

MC88915TFN133

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL, SYNC}$ Inputs	Rise/Fall Time, SYNC Inputs From 0.8 to 2.0V	—	3.0	ns
$t_{CYCLE, SYNC}$ Inputs	Input Clock Period SYNC Inputs	15.0 ¹	100 ²	ns
Duty Cycle SYNC Inputs	Input Duty Cycle SYNC Inputs	50% $\pm$ 25%		

- These t_{CYCLE} minimum values are valid when 'Q' output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 5b.
- Information in Table 1 and in Note 3 of the AC specification notes describe this specification and its limits depending on what output is fed back, and if FREQ_SEL is high or low.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND) $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions	V_{CC} V	Target Limit	Unit
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$	4.75 5.25	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$	4.75 5.25	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $I_{OH} = -36\text{mA}$ ¹	4.75 5.25	4.01 4.51	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $I_{OL} = 36\text{mA}$ ¹	4.75 5.25	0.44 0.44	V
I_{in}	Maximum Input Leakage Current	$V_I = V_{CC}$ or GND	5.25	± 1.0	μA
I_{CCT}	Maximum I_{CC} /Input	$V_I = V_{CC} - 2.1\text{V}$	5.25	2.0 ²	mA
I_{OLD}	Minimum Dynamic Output Current ³	$V_{OLD} = 1.0\text{V}$ Max	5.25	88	mA
I_{OHD}		$V_{OHD} = 3.85\text{V}$ Min	5.25	-88	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_I = V_{CC}$ or GND	5.25	1.0	mA
I_{OZ}	Maximum 3-State Leakage Current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND	5.25	± 50 ⁴	μA

- I_{OL} and I_{OH} are 12mA and -12mA respectively for the LOCK output.
- The PLL_EN input pin is not guaranteed to meet this specification.
- Maximum test duration is 2.0ms, one output loaded at a time.
- Specification value for I_{OZ} is preliminary, will be finalized upon 'MC' status.

CAPACITANCE AND POWER SPECIFICATIONS

Symbol	Parameter	Typical Values	Unit	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0\text{V}$
C_{PD}	Power Dissipation Capacitance	40	pF	$V_{CC} = 5.0\text{V}$
PD_1	Power Dissipation @ 50MHz with 50 Ω Thevenin Termination	23mW/Output 184mW/Device	mW	$V_{CC} = 5.0\text{V}$ $T = 25^\circ\text{C}$
PD_2	Power Dissipation @ 50MHz with 50 Ω Parallel Termination to GND	57mW/Output 456mW/Device	mW	$V_{CC} = 5.0\text{V}$ $T = 25^\circ\text{C}$

NOTE: PD_1 and PD_2 mW/Output numbers are for a 'Q' output.

FREQUENCY SPECIFICATIONS ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$)

Symbol	Parameter	Guaranteed Minimum	Unit
		TFN133	
f _{max} ¹	Maximum Operating Frequency (2X_Q Output)	133	MHz
	Maximum Operating Frequency (Q0–Q4, Q ₅ Output)	66	MHz

- Maximum Operating Frequency is guaranteed with the part in a phase-locked condition, and all outputs loaded with 50 Ω terminated to $V_{CC}/2$.

MC88915TFN133 (continued)

AC CHARACTERISTICS ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$, Load = 50Ω Terminated to $V_{CC}/2$)

Symbol	Parameter	Min	Max	Unit	Condition
t _{RISE/FALL} Outputs	Rise/Fall Time, All Outputs (Between 0.2V _{CC} and 0.8V _{CC})	1.0	2.5	ns	Into a 50Ω Load Terminated to V _{CC} /2
t _{RISE/FALL} ¹ 2X_Q Output	Rise/Fall Time Into a 20pF Load, With Termination Specified in Note ²	0.5	1.6	ns	t _{RISE} : 0.8V – 2.0V t _{FALL} : 2.0V – 0.8V
t _{PULSE WIDTH} ¹ (Q0–Q4, Q ₅ , Q/2)	Output Pulse Width: Q0, Q1, Q2, Q3, Q4, Q ₅ , Q/2 @ V _{CC} /2	0.5t _{CYCLE} – 0.5 ²	0.5t _{CYCLE} + 0.5 ²	ns	Into a 50Ω Load Terminated to V _{CC} /2
t _{PULSE WIDTH} ¹ (2X_Q Output)	Output Pulse Width: 66–133MHz 2X_Q @ 1.5V 40–65MHz	0.5t _{CYCLE} – 0.5 ² 0.5t _{CYCLE} – 0.9	0.5t _{CYCLE} + 0.5 ² 0.5t _{CYCLE} + 0.9	ns	Must Use Termination Specified in Note 2
t _{PULSE WIDTH} ¹ (2X_Q Output)	Output Pulse Width: 66–133MHz 2X_Q @ V _{CC} /2 40–65MHz	0.5t _{CYCLE} – 0.5 ² 0.5t _{CYCLE} – 0.9	0.5t _{CYCLE} + 0.5 ² 0.5t _{CYCLE} + 0.9	ns	Into a 50Ω Load Terminated to V _{CC} /2
t _{PD} ^{1,3} SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)	(With 1MΩ from RC1 to An V _{CC})		ns	See Note 4 and Figure 2 for Detailed Explanation
		–1.05	–0.25		
		(With 1MΩ from RC1 to An GND)			
		+1.25	+3.25		
t _{SKEW_r} ^{1,4} (Rising) See Note ⁵	Output-to-Output Skew Between Out- puts Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to V _{CC} /2
t _{SKEW_f} ^{1,4} (Falling)	Output-to-Output Skew Between Out- puts Q0–Q4 (Falling Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to V _{CC} /2
t _{SKEW_{all}} ^{1,4}	Output-to-Output Skew 2X_Q, Q/2, Q0–Q4 Rising, Q ₅ Falling	—	750	ps	All Outputs Into a Matched 50Ω Load Terminated to V _{CC} /2
t _{LOCK} ⁵	Time Required to Acquire Phase-Lock From Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
t _{PZL} ⁶	Output Enable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0–Q4, Q ₅ , and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low
t _{PHZ} , t _{PLZ} ⁶	Output Disable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0–Q4, Q ₅ , and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low

1. These specifications are not tested, they are guaranteed by statistical characterization. See AC specification Note 1.

2. T_{CYCLE} in this spec is $1/\text{Frequency}$ at which the particular output is running.

3. The T_{PD} specification's min/max values may shift closer to zero if a larger pullup resistor is used.

4. Under equally loaded conditions and at a fixed temperature and voltage.

5. With V_{CC} fully powered-on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with $C1 = 0.1\mu\text{F}$, t_{LOCK} minimum is with $C1 = 0.01\mu\text{F}$.

6. The t_{PZL} , t_{PHZ} , t_{PLZ} minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

MC88915TFN160

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL, SYNC}$ Inputs	Rise/Fall Time, SYNC Inputs From 0.8 to 2.0V	—	3.0	ns
$t_{CYCLE, SYNC}$ Inputs	Input Clock Period SYNC Inputs	12.5	100	ns
Duty Cycle SYNC Inputs	Input Duty Cycle SYNC Inputs	50% $\pm$ 25%		

- These t_{CYCLE} minimum values are valid when 'Q' output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 5b.
- Information in Table 1 and in Note 3 of the AC specification notes describe this specification and its limits depending on what output is fed back, and if FREQ_SEL is high or low.

2

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND) $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions	V_{CC} V	Target Limit	Unit
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$	4.75 5.25	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$	4.75 5.25	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $I_{OH} = -36\text{mA}$ ¹	4.75 5.25	4.01 4.51	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $I_{OL} = 36\text{mA}$ ¹	4.75 5.25	0.44 0.44	V
I_{in}	Maximum Input Leakage Current	$V_I = V_{CC}$ or GND	5.25	± 1.0	μA
I_{CCT}	Maximum I_{CC} /Input	$V_I = V_{CC} - 2.1\text{V}$	5.25	2.0 ²	mA
I_{OLD}	Minimum Dynamic Output Current ³	$V_{OLD} = 1.0\text{V}$ Max	5.25	88	mA
I_{OHD}		$V_{OHD} = 3.85\text{V}$ Min	5.25	-88	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_I = V_{CC}$ or GND	5.25	1.0	mA
I_{OZ}	Maximum 3-State Leakage Current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND	5.25	± 50 ⁴	μA

- I_{OL} and I_{OH} are 12mA and -12mA respectively for the LOCK output.
- The PLL_EN input pin is not guaranteed to meet this specification.
- Maximum test duration is 2.0ms, one output loaded at a time.
- Specification value for I_{OZ} is preliminary, will be finalized upon 'MC' status.

CAPACITANCE AND POWER SPECIFICATIONS

Symbol	Parameter	Typical Values	Unit	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0\text{V}$
C_{PD}	Power Dissipation Capacitance	40	pF	$V_{CC} = 5.0\text{V}$
PD_1	Power Dissipation @ 50MHz with 50 Ω Thevenin Termination	15mW/Output 120mW/Device	mW	$V_{CC} = 5.0\text{V}$ $T = 25^\circ\text{C}$
PD_2	Power Dissipation @ 50MHz with 50 Ω Parallel Termination to GND	57mW/Output 456mW/Device	mW	$V_{CC} = 5.0\text{V}$ $T = 25^\circ\text{C}$

NOTE: PD_1 and PD_2 mW/Output numbers are for a 'Q' output.

FREQUENCY SPECIFICATIONS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$)

Symbol	Parameter	Guaranteed Minimum	Unit
		TFN160	
f _{max} ¹	Maximum Operating Frequency (2X_Q Output)	160	MHz
	Maximum Operating Frequency (Q0–Q4, $\overline{Q5}$ Output)	80	MHz

- Maximum Operating Frequency is guaranteed with the part in a phase-locked condition, and all outputs loaded with 50 Ω terminated to $V_{CC}/2$.

MC88915TFN160 (continued)

AC CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$, Load = 50Ω Terminated to $V_{CC}/2$)

Symbol	Parameter	Min	Max	Unit	Condition
$t_{RISE/FALL}$ Outputs	Rise/Fall Time, All Outputs (Between $0.2V_{CC}$ and $0.8V_{CC}$)	1.0	2.5	ns	Into a 50Ω Load Terminated to $V_{CC}/2$
$t_{RISE/FALL}$ 2X_Q Output	Rise/Fall Time	0.5	1.6	ns	t_{RISE} : $0.8\text{V} - 2.0\text{V}$ t_{FALL} : $2.0\text{V} - 0.8\text{V}$
$t_{PULSE\ WIDTH}$ (Q0–Q4, $\overline{Q5}$, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q3, Q4, $\overline{Q5}$, Q/2 @ $V_{CC}/2$	$0.5t_{CYCLE} - 0.5^2$	$0.5t_{CYCLE} + 0.5^2$	ns	Into a 50Ω Load Terminated to $V_{CC}/2$
$t_{PULSE\ WIDTH}$ (2X_Q Output)	Output Pulse Width: 80MHz 100MHz 133MHz 160MHz 2X_Q @ V_{CC}	$0.5t_{CYCLE} - 0.7$ $0.5t_{CYCLE} - 0.5$ $0.5t_{CYCLE} - 0.5$ TBD	$0.5t_{CYCLE} + 0.7$ $0.5t_{CYCLE} + 0.5$ $0.5t_{CYCLE} + 0.5$ TBD	ns	
t_{PD}^1 SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)	(With $1\text{M}\Omega$ from RC1 to An V_{CC})		ns	See Note 2 and Figure 2 for Detailed Explanation
		133MHz 160MHz	-1.05 -0.9		
t_{CYCLE} (2x_Q Output)	Cycle-to-Cycle Variation 133MHz 160MHz	$t_{CYCLE} - 300\text{ps}$ $t_{CYCLE} - 300\text{ps}$	$t_{CYCLE} + 300\text{ps}$ $t_{CYCLE} + 300\text{ps}$		
t_{SKEW}^3 (Rising) See Note 4	Output-to-Output Skew Between Out- puts Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}/2$
t_{SKEW}^3 (Falling)	Output-to-Output Skew Between Out- puts Q0–Q4 (Falling Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}/2$
t_{SKEW}^3	Output-to-Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling	—	750	ps	All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}/2$
t_{LOCK}^4	Time Required to Acquire Phase-Lock From Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
t_{PZL}^5	Output Enable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low
t_{PHZ}, t_{PLZ}^5	Output Disable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low

1. T_{CYCLE} in this spec is $1/\text{Frequency}$ at which the particular output is running.

2. The T_{PD} specification's min/max values may shift closer to zero if a larger pullup resistor is used.

3. Under equally loaded conditions and at a fixed temperature and voltage.

4. With V_{CC} fully powered-on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with $C1 = 0.1\mu\text{F}$, t_{LOCK} minimum is with $C1 = 0.01\mu\text{F}$.

5. The t_{PZL} , t_{PHZ} , t_{PLZ} minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

Applications Information for All Versions

General AC Specification Notes

- Several specifications can only be measured when the MC88915TFN55, 70 and 100 are in phase-locked operation. It is not possible to have the part in phase-lock on ATE (automated test equipment). Statistical characterization techniques were used to guarantee those specifications which cannot be measured on the ATE. MC88915TFN55, 70 and 100 units were fabricated with key transistor properties intentionally varied to create a 14 cell designed experimental matrix. IC performance was characterized over a range of transistor properties (represented by the 14 cells) in excess of the expected process variation of the wafer fabrication area, to set performance limits of ATE testable specifications within those which are to be guaranteed by statistical characterization. In this way all units passing the ATE test will meet or exceed the non-tested specifications limits.
- These two specs ($t_{RISE/FALL}$ and t_{PULSE} Width 2X_Q output) guarantee that the MC88915T meets the 40MHz and 33MHz MC68040 P-Clock input specification (at 80MHz and 66MHz, respectively). For these two specs to be guaranteed by Motorola, the termination scheme shown below in Figure 1 must be used.
- The wiring Diagrams and explanations in Figure 5 demonstrate the input and output frequency relationships for three possible feedback configurations. The allowable SYNC input range for each case is also indicated. There are two allowable SYNC frequency ranges, depending whether $FREQ\_SEL$ is high or low. Although not shown, it is possible to feed back the $\overline{Q5}$ output, thus creating a 180° phase shift between the SYNC input and the "Q" outputs. Table 1 below summarizes the allowable SYNC frequency range for each possible configuration.

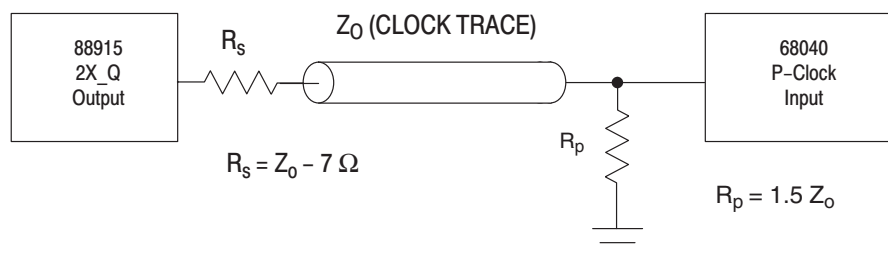


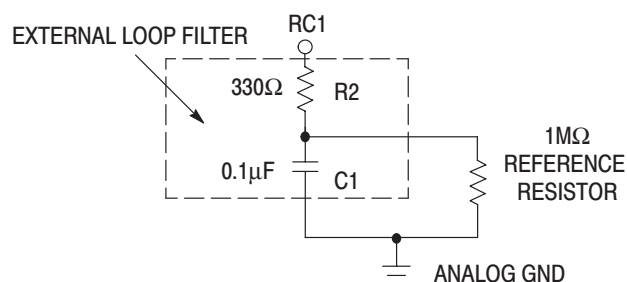
Figure 1. MC68040 P-Clock Input Termination Scheme

Table 1. Allowable SYNC Input Frequency Ranges for Different Feedback Configurations.

FREQ_SEL Level	Feedback Output	Allowable SYNC Input Frequency Range (MHZ)	Corresponding VCO Frequency Range	Phase Relationships of the "Q" Outputs to Rising SYNC Edge
HIGH	Q/2	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAX Spec)	0°
HIGH	Any "Q" (Q0–Q4)	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAX Spec)	0°
HIGH	$\overline{Q5}$	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAX Spec)	180°
HIGH	2X_Q	20 to (2X_Q FMAX Spec)	20 to (2X_Q FMAX Spec)	0°
LOW	Q/2	2.5 to (2X_Q FMAX Spec)/8	20 to (2X_Q FMAX Spec)	0°
LOW	Any "Q" (Q0–Q4)	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAX Spec)	0°
LOW	$\overline{Q5}$	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAX Spec)	180°
LOW	2X_Q	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAX Spec)	0°

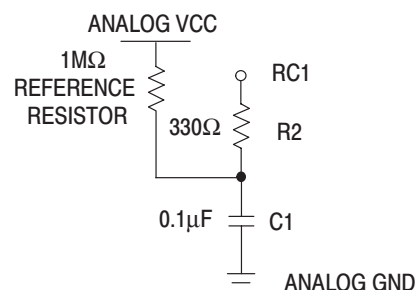
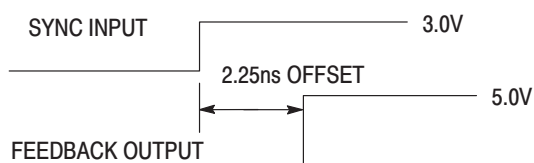
- A 1MΩ resistor tied to either Analog V_{CC} or Analog GND as shown in Figure 2 is required to ensure no jitter is present on the MC88915T outputs. This technique causes a phase offset between the SYNC input and the output connected to the FEEDBACK input, measured at the input pins. The t_{PD} spec describes how this offset varies with process, temperature, and voltage. The specs were arrived at by

measuring the phase relationship for the 14 lots described in note 1 while the part was in phase-locked operation. The actual measurements were made with a 10MHz SYNC input (1.0ns edge rate from 0.8V – 2.0V) with the Q/2 output fed back. The phase measurements were made at 1.5V. The Q/2 output was terminated at the FEEDBACK input with 100Ω to V_{CC} and 100Ω to ground.



With the 1MΩ resistor tied in this fashion, the t_{PD} specification measured at the input pins is:

$$t_{PD} = 2.25\text{ns} \pm 1.0\text{ns}$$



With the 1MΩ resistor tied in this fashion, the t_{PD} specification measured at the input pins is:

$$t_{PD} = -0.775\text{ns} \pm 0.275\text{ns}$$

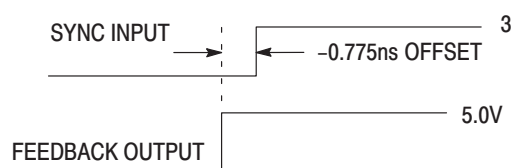


Figure 2. Depiction of the Fixed SYNC to Feedback Offset (t_{PD}) Which is Present When a 1MΩ Resistor is Tied to V_{CC} or Ground

5. The t_{SKEW_r} specification guarantees that the rising edges of outputs Q/2, Q0, Q1, Q2, Q3, and Q4 will always fall within a 500ps window within one part. However, if the relative position of each output within this window is not specified, the 500 ps window must be added to each side of the t_{PD} specification limits to calculate the total part-to-part skew.

For this reason the absolute distribution of these outputs are provided in table 2. When taking the skew data, Q0 was used as a reference, so all measurements are relative to this output. The information in Table 2 is derived from measurements taken from the 14 process lots described in Note 1, over the temperature and voltage range.

Table 2. Relative Positions of Outputs Q/2, Q0–Q4, 2X_Q, Within the 500ps t_{SKEW_r} Spec Window

Output	– (ps)	+ (ps)
Q0	0	0
Q1	–72	40
Q2	–44	276
Q3	–40	255
Q4	–274	–34
Q/2	–16	250
2X_Q	–633	–35

6. Calculation of Total Output-to-Skew between multiple parts (Part-to-Part skew)

By combining the t_{PD} specification and the information in Note 5, the worst case output-to-output skew between multiple 88915's connected in parallel can be calculated. This calculation assumes that all parts have a common SYNC input clock with equal delay of that input signal to each part. This skew value is valid at the 88915 output pins only (equally loaded), it does not include PCB trace delays due to varying loads.

With a 1 M Ω resistor tied to analog V_{CC} as shown in note 4, the t_{PD} spec. limits between SYNC and the Q/2 output (connected to the FEEDBACK pin) are -1.05ns and -0.5ns . To calculate the skew of any given output between two or more parts, the absolute value of the distribution of that output given in table 2 must be subtracted and added to the lower and upper t_{PD} spec limits respectively. For output Q2, $[276 - (-44)] = 320\text{ps}$ is the absolute value of the

distribution. Therefore $[-1.05\text{ns} - 0.32\text{ns}] = -1.37\text{ns}$ is the lower t_{PD} limit, and $[-0.5\text{ns} + 0.32\text{ns}] = -0.18\text{ns}$ is the upper limit. Therefore the worst case skew of output Q2 between any number of parts is $|(-1.37) - (-0.18)| = 1.19\text{ns}$. Q2 has the worst case skew distribution of any output, so 1.2ns is the absolute worst case output-to-output skew between multiple parts.

7. Note 4 explains that the t_{PD} specification was measured and is guaranteed for the configuration of the Q/2 output connected to the FEEDBACK pin and the SYNC input running at 10MHz. The fixed offset (t_{PD}) as described above has some dependence on the input frequency and at what frequency the VCO is running. The graphs of Figure 3 demonstrate this dependence.

The data presented in Figure 3 is from devices representing process extremes, and the measurements were also taken at the voltage extremes ($V_{CC} = 5.25\text{V}$ and 4.75V). Therefore the data in Figure 3 is a realistic representation of the variation of t_{PD} .

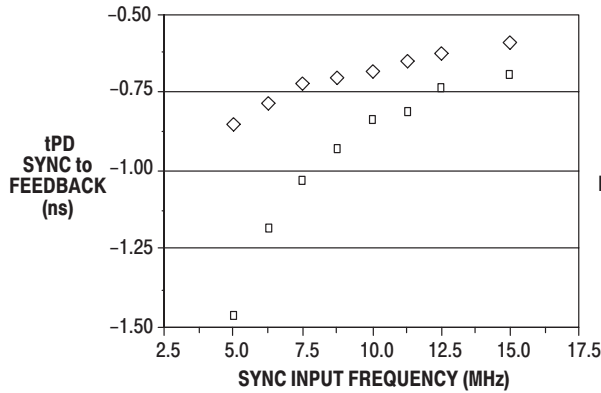


Figure 3a.

t_{PD} versus Frequency Variation for Q/2 Output Fed Back, Including Process and Voltage Variation @ 25°C (With 1M Ω Resistor Tied to Analog V_{CC})

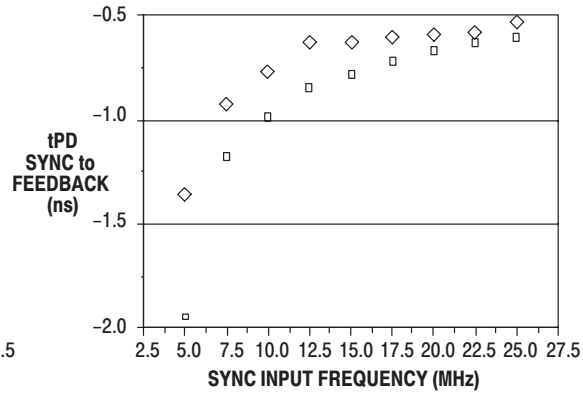


Figure 3b.

t_{PD} versus Frequency Variation for Q4 Output Fed Back, Including Process and Voltage Variation @ 25°C (With 1M Ω Resistor Tied to Analog V_{CC})

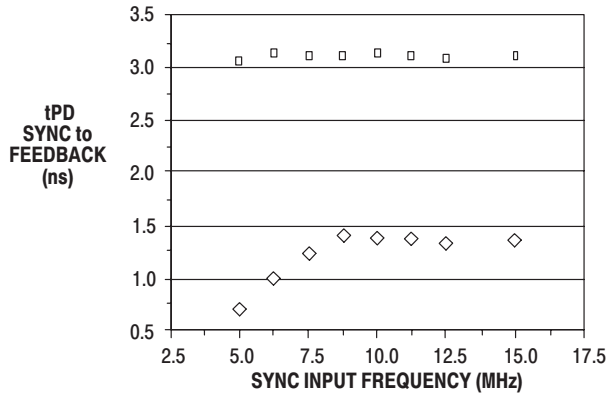


Figure 3c.

t_{PD} versus Frequency Variation for Q/2 Output Fed Back, Including Process and Voltage Variation @ 25°C (With 1M Ω Resistor Tied to Analog GND)

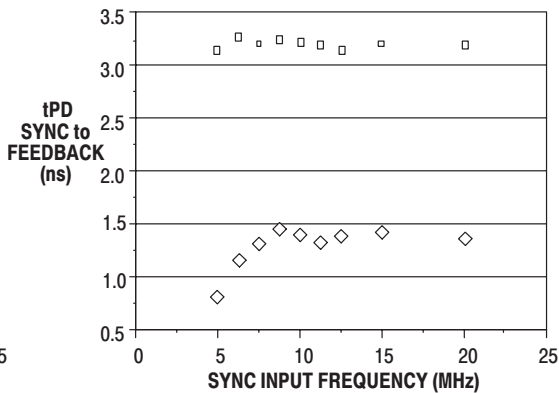


Figure 3d.

t_{PD} versus Frequency Variation for Q4 Output Fed Back, Including Process and Voltage Variation @ 25°C (With 1M Ω Resistor Tied to Analog GND)

8. The lock indicator pin (LOCK) will reliably indicate a phase-locked condition at SYNC input frequencies down to 10MHz. At frequencies below 10MHz, the frequency of correction pulses going into the phase detector from the SYNC and FEEDBACK pins may not be sufficient to allow the lock indicator circuitry to accurately predict a phase-locked condition. The MC88915T is guaranteed to

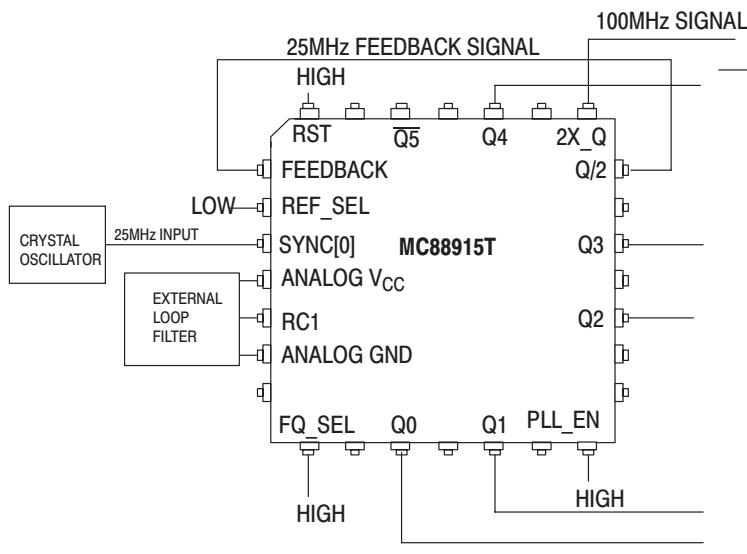
provide stable phase-locked operation down to the appropriate minimum input frequency given in Table 1, even though the LOCK pin may be LOW at frequencies below 10MHz. The exact minimum frequency where the lock indicator functionality can be guaranteed will be available when the MC88915T reaches 'MC' status.



2

2

- 2



1:2 Input to “Q” Output Frequency Relationship

In this application, the Q/2 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q/2 and SYNC, thus the Q/2 frequency will equal the SYNC frequency. The “Q” outputs (Q0–Q4, Q5) will always run at 2X the Q/2 frequency, and the 2X_Q output will run at 4X the Q/2 frequency.

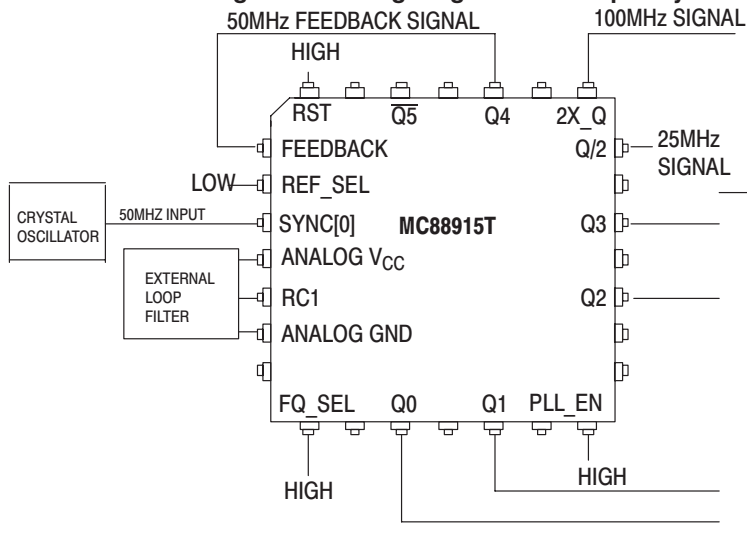
50MHz
“Q”
CLOCK
OUTPUTS

Allowable Input Frequency Range:

5MHz to $(2X\_Q \text{ FMAX Spec})/4$ (for FREQ_SEL HIGH)
2.5MHz to $(2X\_Q \text{ FMAX Spec})/8$ (for FREQ_SEL LOW)

Note: If the $\overline{OE}/\overline{RST}$ input is active, a pull-up or pull-down resistor isn't necessary at the FEEDBACK pin so it won't when the fed back output goes into 3-state.

Figure 5a. Wiring Diagram and Frequency Relationships With Q/2 Output Feed Back



1:1 Input to “Q” Output Frequency Relationship

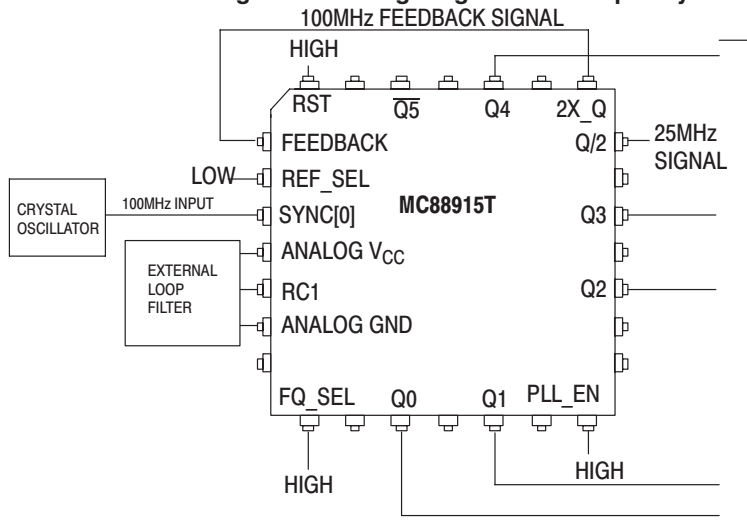
In this application, the Q4 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q4 and SYNC, thus the Q4 frequency (and the rest of the “Q” outputs) will equal the SYNC frequency. The Q/2 output will always run at 1/2 the “Q” frequency, and the 2X_Q output will run at 2X the “Q” frequency.

50MHz
“Q”
CLOCK
OUTPUTS

Allowable Input Frequency Range:

10MHz to $(2X\_Q \text{ FMAX Spec})/2$ (for FREQ_SEL HIGH)
5MHz to $(2X\_Q \text{ FMAX Spec})/4$ (for FREQ_SEL LOW)

Figure 5b. Wiring Diagram and Frequency Relationships With Q4 Output Feed Back



2:1 Input to “Q” Output Frequency Relationship

In this application, the 2X_Q output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of 2X_Q and SYNC, thus the 2X_Q frequency will equal the SYNC frequency. The Q/2 output will always run at 1/4 the 2X_Q frequency, and the “Q” outputs will run at 1/2 the 2X_Q frequency.

50MHz
“Q”
CLOCK
OUTPUTS

Allowable Input Frequency Range:

20MHz to $(2X\_Q \text{ FMAX Spec})$ (for FREQ_SEL HIGH)
10MHz to $(2X\_Q \text{ FMAX Spec})/2$ (for FREQ_SEL LOW)

Figure 5c. Wiring Diagram and Frequency Relationships with 2X_Q Output Feed Back

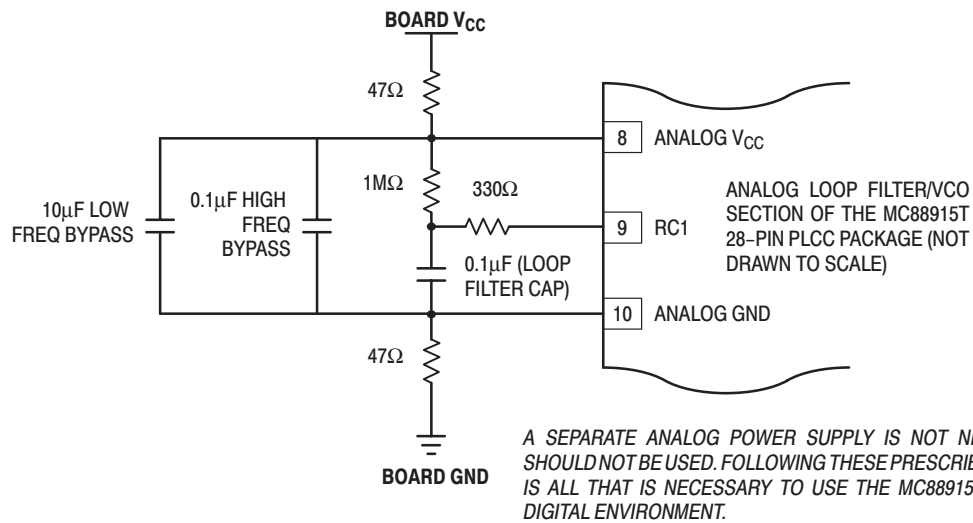


Figure 6. Recommended Loop Filter and Analog Isolation Scheme for the MC88915T

Notes Concerning Loop Filter and Board Layout Issues

1. Figure 6 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter-free operation:

1a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.

1b. The 47Ω resistors, the 10μF low frequency bypass capacitor, and the 0.1μF high frequency bypass capacitor form a wide bandwidth filter that will minimize the 88915T's sensitivity to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital V_{CC} supply will cause no more than a 100pS phase deviation on the 88915T outputs. A 250mV step deviation on V_{CC} using the recommended filter values should cause no more than a 250pS phase deviation; if a 25μF bypass capacitor is used (instead of 10μF) a 250mV V_{CC} step should cause no more than a 100pS phase deviation.

If good bypass techniques are used on a board design near components which may cause digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the 88915T's digital V_{CC} supply. The purpose of the bypass filtering scheme shown in Figure 6 is to give the

88915T additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

1c. There are no special requirements set forth for the loop filter resistors (1MΩ and 330Ω). The loop filter capacitor (0.1μF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.

1d. The 1M reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead-band. If the VCO (2X_Q output) is running above 40MHz, the 1MΩ resistor provides the correct amount of current injection into the charge pump (2–3μA). For the TFN55, 70 or 100, if the VCO is running below 40MHz, a 1.5MΩ reference resistor should be used (instead of 1MΩ).

2. In addition to the bypass capacitors used in the analog filter of Figure 6, there should be a 0.1μF bypass capacitor between each of the other (digital) four V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the 88915T outputs, in addition to reducing potential for noise in the 'analog' section of the chip. These bypass capacitors should also be tied as close to the 88915T package as possible.

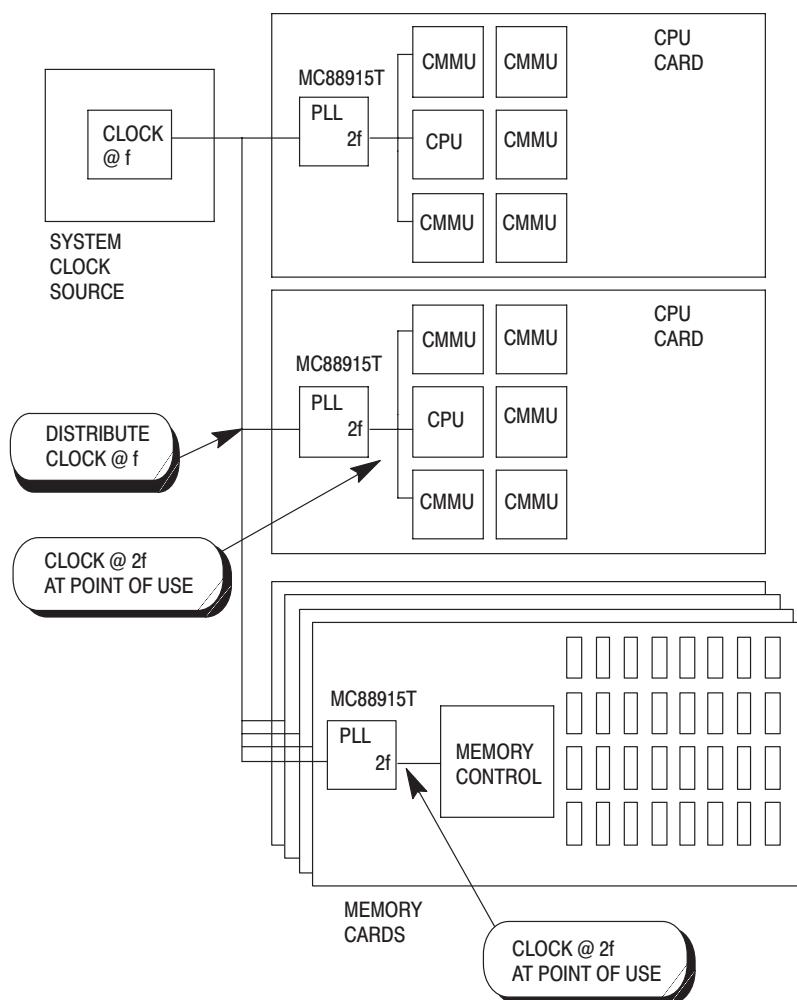


Figure 7. Representation of a Potential Multi-Processing Application Utilizing the MC88915T for Frequency Multiplication and Low Board-to-Board Skew

MC88915T System Level Testing Functionality

3-state functionality has been added to the 100MHz version of the MC88915T to ease system board testing. Bringing the $\overline{OE}/RST$ pin low will put all outputs (except for LOCK) into the high impedance state. As long as the PLL_EN pin is low, the Q0-Q4, Q5, and the Q/2 outputs will remain reset in the low state after the $\overline{OE}/RST$ until a falling SYNC edge is seen. The 2X_Q output will be the inverse of the SYNC signal in this mode. If the 3-state functionality will be used, a pull-up or pull-down resistor must be tied to the FEEDBACK input pin to prevent it from floating when the feedback output goes into high impedance.

With the PLL_EN pin low the selected SYNC signal is gated directly into the internal clock distribution network, bypassing and disabling the VCO. In this mode the outputs are directly driven by the SYNC input (per the block diagram). This mode can also be used for low frequency board testing.

Note: If the outputs are put into 3-state during normal PLL operation, the loop will be broken and phase-lock will be lost. It will take a maximum of 10mS (tLOCK spec) to regain phase-lock after the $\overline{OE}/RST$ pin goes back high.

Low Voltage Low Skew CMOS PLL Clock Driver, 3-State

MC88LV915T

2

**LOW SKEW CMOS
PLL CLOCK DRIVER**

The MC88LV915T Clock Driver utilizes phase-locked loop technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for high performance PC's and workstations.

The PLL allows the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple components on a board. The PLL also allows the MC88LV915T to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency. Multiple 88LV915's can lock onto a single reference clock, which is ideal for applications when a central system clock must be distributed synchronously to multiple boards (see Figure 4 on Page 39).

Five "Q" outputs (Q0–Q4) are provided with less than 500 ps skew between their rising edges. The $\overline{Q5}$ output is inverted (180° phase shift) from the "Q" outputs. The 2X_Q output runs at twice the "Q" output frequency, while the Q/2 runs at 1/2 the "Q" frequency.

The VCO is designed to run optimally between 20 MHz and the 2X_Q F_{max} specification. The wiring diagrams in Figure 2 detail the different feedback configurations which create specific input/output frequency relationships. Possible frequency ratios of the "Q" outputs to the SYNC input are 2:1, 1:1, and 1:2.

The FREQ_SEL pin provides one bit programmable divide-by in the feedback path of the PLL. It selects between divide-by-1 and divide-by-2 of the VCO before its signal reaches the internal clock distribution section of the chip (see the block diagram on page 2). In most applications FREQ_SEL should be held high (+1). If a low frequency reference clock input is used, holding FREQ_SEL low (+2) will allow the VCO to run in its optimal range (>20MHz).

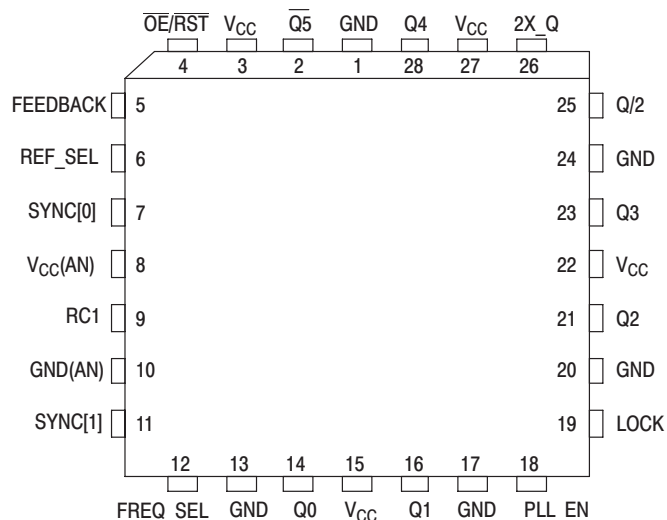
In normal phase-locked operation the PLL_EN pin is held high. Pulling the PLL_EN pin low disables the VCO and puts the 88LV915T in a static "test mode". In this mode there is no frequency limitation on the input clock, which is necessary for a low frequency board test environment. The second SYNC input can be used as a test clock input to further simplify board-level testing (see detailed description on page 11).

Pulling the $\overline{OE/RST}$ pin low puts the clock outputs 2X_Q, Q0–Q4, $\overline{Q5}$ and Q/2 into a high impedance state (3-state). After the $\overline{OE/RST}$ pin goes back high Q0–Q4, $\overline{Q5}$ and Q/2 will be reset in the low state, with 2X_Q being the inverse of the selected SYNC input. Assuming PLL_EN is low, the outputs will remain reset until the 88LV915 sees a SYNC input pulse.

A lock indicator output (LOCK) will go high when the loop is in steady-state phase and frequency lock. The LOCK output will go low if phase-lock is lost or when the PLL_EN pin is low. The LOCK output will go high no later than 10ms after the 88LV915 sees a SYNC signal and full 5V V_{CC} .

Features

- Five Outputs (Q0–Q4) with Output–Output Skew < 500 ps each being phase and frequency locked to the SYNC input
- The phase variation from part-to-part between the SYNC and FEEDBACK inputs is less than 550 ps (derived from the t_{PD} specification, which defines the part-to-part skew)
- Input/Output phase-locked frequency ratios of 1:2, 1:1, and 2:1 are available
- Input frequency range from 5MHz – 2X_Q F_{MAX} spec.
- Additional outputs available at 2X and +2 the system "Q" frequency. Also a $\overline{Q}$ (180° phase shift) output available
- All outputs have ± 36 mA drive (equal high and low) at CMOS levels, and can drive either CMOS or TTL inputs. All inputs are TTL-level compatible. ± 88 mA I_{OL}/I_{OH} specifications guarantee 50 Ω transmission line switching on the incident edge
- Test Mode pin (PLL_EN) provided for low frequency testing. Two selectable CLOCK inputs for test or redundancy purposes. All outputs can go into high impedance (3-state) for board test purposes
- Lock Indicator (LOCK) accuracy indicates a phase-locked state

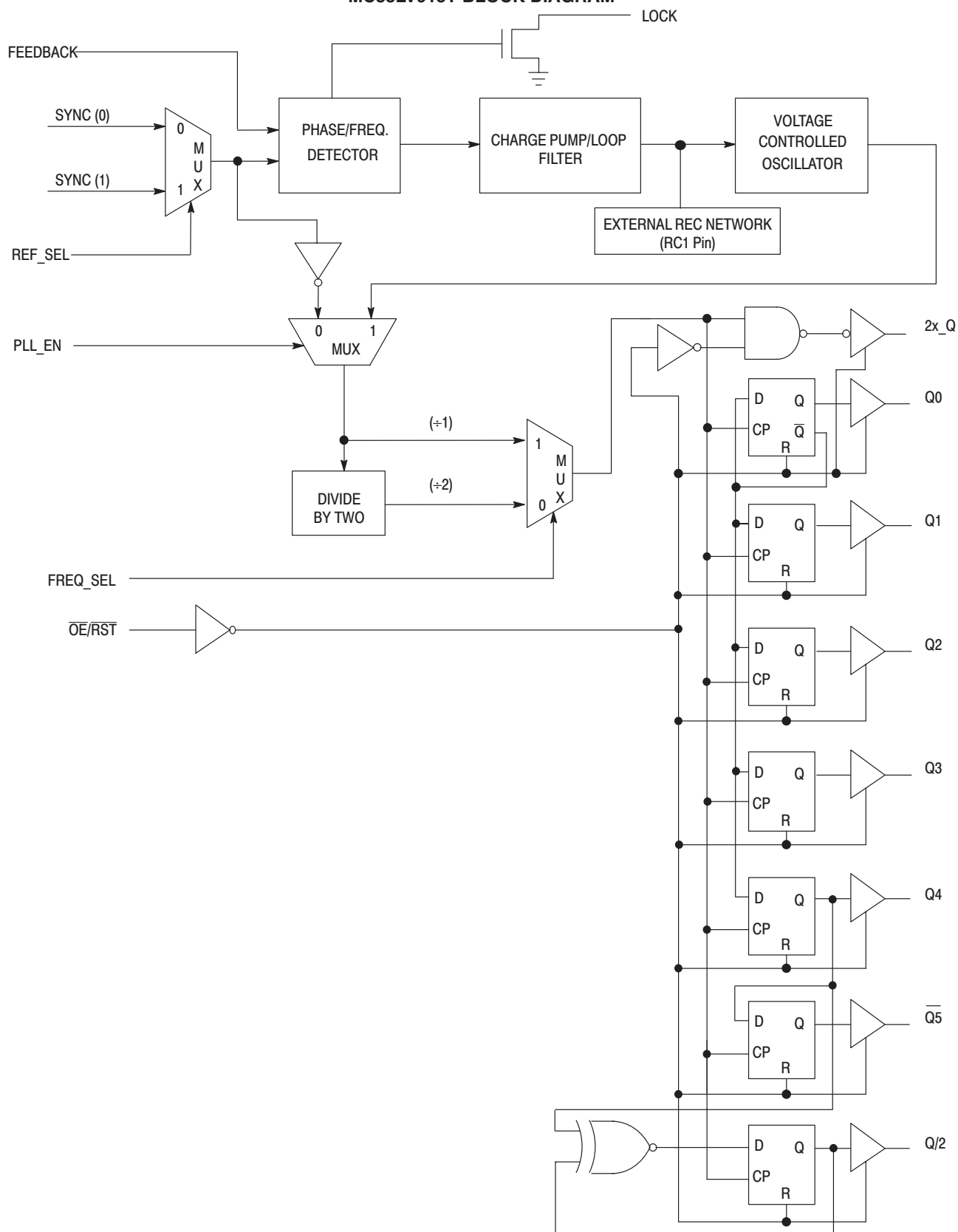
Pinout: 28-Lead PLCC (Top View)

FN SUFFIX
 PLASTIC PLCC
 CASE 776-02

PIN SUMMARY

Pin Name	Num	I/O	Function
SYNC[0]	1	Input	Reference clock input
SYNC[1]	1	Input	Reference clock input
REF_SEL	1	Input	Chooses reference between sync[0] & Sync[1]
FREQ_SEL	1	Input	Doubles VCO Internal Frequency (low)
FEEDBACK	1	Input	Feedback input to phase detector
RC1	1	Input	Input for external RC network
Q(0-4)	5	Output	Clock output (locked to sync)
$\overline{Q5}$	1	Output	Inverse of clock output
2x_Q	1	Output	2 x clock output (Q) frequency (synchronous)
Q/2	1	Output	Clock output(Q) frequency $\div 2$ (synchronous)
LOCK	1	Output	Indicates phase lock has been achieved (high when locked)
$\overline{OE/RST}$	1	Input	Output Enable/Asynchronous reset (active low)
PLL_EN	1	Input	Disables phase-lock for low freq. testing
V_{CC}, GND	11		Power and ground pins (note pins 8, 10 are "analog" supply pins for internal PLL only)

MC88LV915T BLOCK DIAGRAM



MAXIMUM RATINGS*

Symbol	Parameter	Limits	Unit
V_{CC}, AV_{CC}	DC Supply Voltage Referenced to GND	-0.5 to 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, Per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, Per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current Per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits	Unit
V_{CC}	Supply Voltage	3.3 ± 0.3	V
V_{in}	DC Input Voltage	0 to V_{CC}	V
V_{out}	DC Output Voltage	0 to V_{CC}	V
T_A	Ambient Operating Temperature	0 to 70	°C
ESD	Static Discharge Voltage	> 1000	V

DC CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C ; $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$)

Symbol	Parameter	V_{CC}	Guaranteed Limits	Unit	Condition
V_{IH}	Minimum High Level Input Voltage	3.0 3.3	2.0 2.0	V	$V_{OUT} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$
V_{IL}	Minimum Low Level Input Voltage	3.0 3.3	0.8 0.8	V	$V_{OUT} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$
V_{OH}	Minimum High Level Output Voltage	3.0 3.3	2.4 2.7	V	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -24\text{mA}$
V_{OL}	Minimum Low Level Output Voltage	3.0 3.3	0.44 0.44	V	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = 24\text{mA}$
I_{IN}	Maximum Input Leakage Current	3.6	± 1.0	μA	$V_I = V_{CC}, \text{GND}$
I_{CCT}	Maximum I_{CC} /Input	3.6	2.0	mA	$V_I = V_{CC} - 2.1\text{V}$
I_{OLD}	Minimum Dynamic ³ Output Current	3.6	+50	mA	$V_{OLD} = 1.25\text{V}$
I_{OHD}		3.6	-50	mA	$V_{OHD} = 2.35\text{V}$
I_{CC}	Maximum Quiescent Supply Current	3.6	TBD	μA	$V_I = V_{CC}, \text{GND}$

- I_{OL} is +12mA for the $\overline{\text{RST\_OUT}}$ output.
- The PLL_EN input pin is not guaranteed to meet this specification.
- Maximum test duration 2.0ms, one output loaded at a time.

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL}$ SYNC Input	Rise/Fall Time, SYNC Input From 0.8V to 2.0V	—	5.0	ns
t_{CYCLE} SYNC Input	Input Clock Period SYNC Input	$\frac{1}{f_{2X\_Q/4}}$	100	ns
Duty Cycle	Duty Cycle, SYNC Input	50% $\pm$ 25%		

FREQUENCY SPECIFICATIONS ($T_A = 0^\circ\text{C}$ to 70°C ; $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$)

Symbol	Parameter	Guaranteed Minimum	Unit
F _{max} (2X_Q)	Maximum Operating Frequency, 2X_Q Output	100	MHz
F _{max} ('Q')	Maximum Operating Frequency, Q0–Q3 Outputs	50	MHz

NOTE: Maximum Operating Frequency is guaranteed with the 88LV926 in a phase-locked condition.

AC CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Load = 50Ω Terminated to $V_{CC}/2$)

Symbol	Parameter	Min	Max	Unit	Condition
t _{RISE/FALL} Outputs	Rise/Fall Time, All Outputs (Between 0.8 to 2.0V)	0.5	2.0	ns	Into a 50Ω Load Terminated to V _{CC} /2
t _{PULSE WIDTH} (Q0–Q4, $\overline{Q5}$, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q3, Q4, $\overline{Q5}$, Q/2 @ V _{CC} /2	0.5t _{CYCLE} – 0.5 ¹	0.5t _{CYCLE} + 0.5 ¹	ns	Into a 50Ω Load Terminated to V _{CC} /2
t _{PULSE WIDTH} (2X_Q Output)	Output Pulse Width: 2X_Q @ 1.5V 40MHz 66MHz 80MHz 100MHz	0.5t _{CYCLE} – 1.5 0.5t _{CYCLE} – 1.0 0.5t _{CYCLE} – 1.0 0.5t _{CYCLE} – 1.0	0.5t _{CYCLE} + 0.5 0.5t _{CYCLE} + 0.5 0.5t _{CYCLE} + 0.5 0.5t _{CYCLE} + 0.5	ns	Into a 50Ω Load Terminated to V _{CC} /2
t _{CYCLE} (2x_Q Output)	Cycle-to-Cycle Variation 2x_Q @ V _{CC} /2 40MHz 66MHz 80MHz 100MHz	t _{CYCLE} – 600ps t _{CYCLE} – 300ps t _{CYCLE} – 300ps t _{CYCLE} – 400ps	t _{CYCLE} + 600ps t _{CYCLE} + 300ps t _{CYCLE} + 300ps t _{CYCLE} + 400ps		
t _{PD} ² SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins) 66MHz 80MHz 100MHz	(With 1MΩ from RC1 to An V _{CC})		ns	
		–1.65 –1.45 –1.25	–1.05 –0.85 –0.65		
t _{SKEW} ³ (Rising) See Note 4	Output-to-Output Skew Between Out- puts Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to V _{CC} /2
t _{SKEW} ³ (Falling)	Output-to-Output Skew Between Out- puts Q0–Q4 (Falling Edges Only)	—	750	ps	All Outputs Into a Matched 50Ω Load Terminated to V _{CC} /2
t _{SKEW} ³ all	Output-to-Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling	—	750	ps	All Outputs Into a Matched 50Ω Load Terminated to V _{CC} /2
t _{LOCK} ⁴	Time Required to Acquire Phase-Lock From Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
t _{PZL} ⁵	Output Enable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low
t _{PHZ} , t _{PLZ} ⁵	Output Disable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low

1. T_{CYCLE} in this spec is 1/Frequency at which the particular output is running.

2. The T_{PD} specification's min/max values may shift closer to zero if a larger pullup resistor is used.

3. Under equally loaded conditions and at a fixed temperature and voltage.

4. With V_{CC} fully powered-on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with $C1 = 0.1\mu\text{F}$, t_{LOCK} minimum is with $C1 = 0.01\mu\text{F}$.

5. The t_{PZL} , t_{PHZ} , t_{PLZ} minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

Applications Information for All Versions

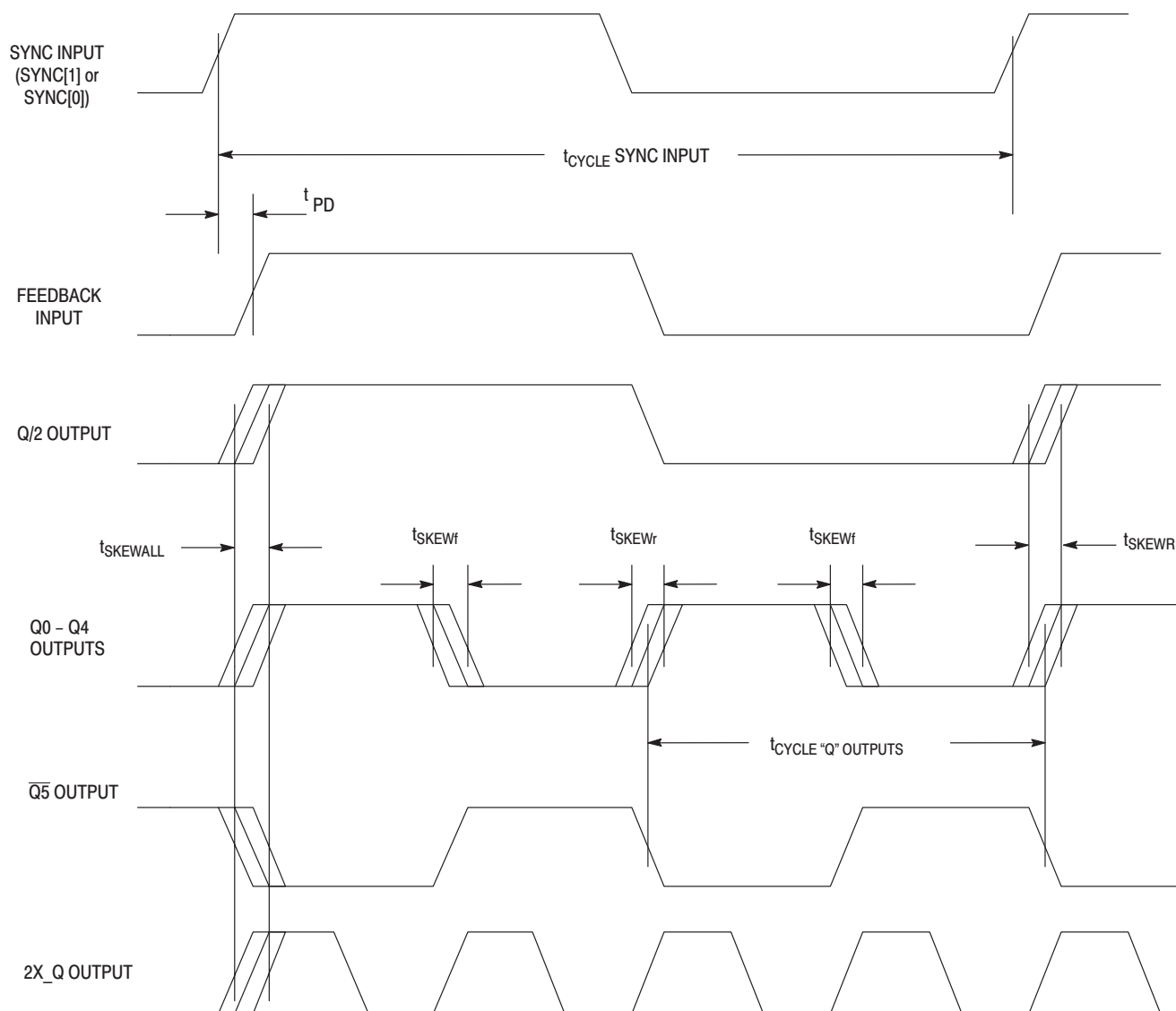
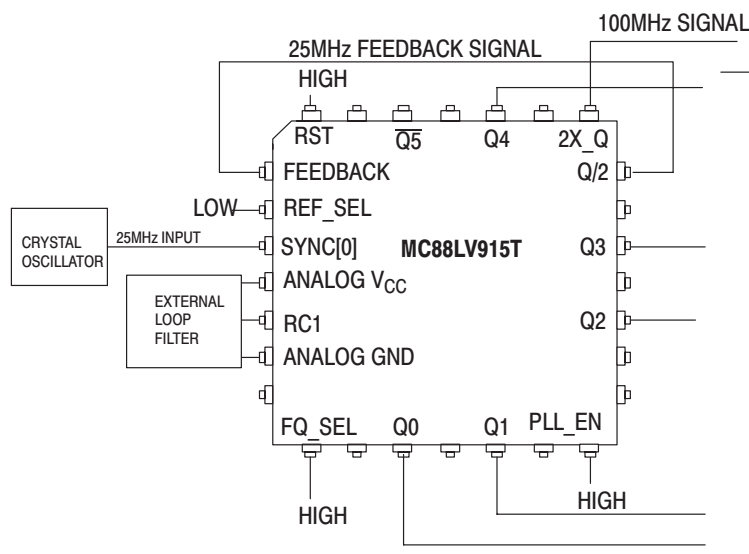


Figure 1. Output/Input Switching Waveforms and Timing Diagrams

(These waveforms represent the hook-up configuration of Figure 2a on page 37)

Timing Notes:

- The MC88LV915T aligns rising edges of the FEEDBACK input and SYNC input, therefore the SYNC input does not require a 50% duty cycle.
- All skew specs are measured between the $V_{CC}/2$ crossing point of the appropriate output edges. All skews are specified as 'windows', not as a $\pm$ deviation around a center point.
- If a "Q" output is connected to the FEEDBACK input (this situation is not shown), the "Q" output frequency would match the SYNC input frequency, the 2X_Q output would run at twice the SYNC frequency, and the Q/2 output would run at half the SYNC frequency.



1:2 Input to “Q” Output Frequency Relationship

In this application, the Q/2 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q/2 and SYNC, thus the Q/2 frequency will equal the SYNC frequency. The “Q” outputs (Q0–Q4, $\overline{Q5}$) will always run at 2X the Q/2 frequency, and the 2X_Q output will run at 4X the Q/2 frequency.

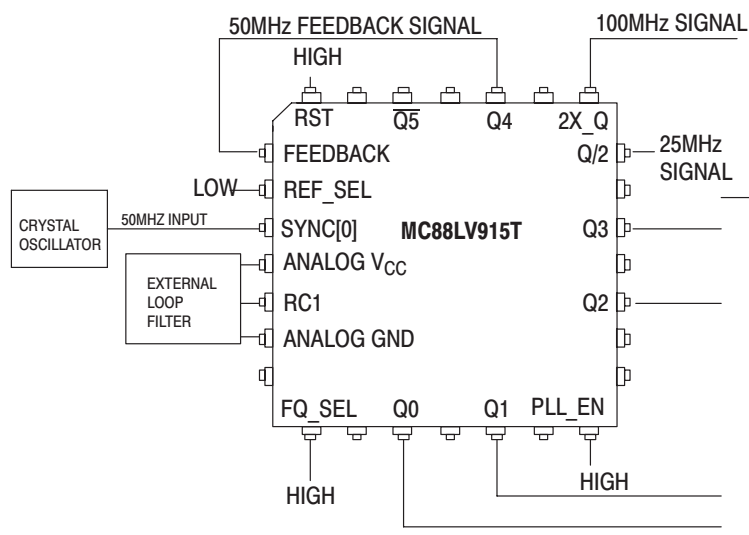
50MHz
“Q”
CLOCK
OUTPUTS

Allowable Input Frequency Range:

5MHz to $(2X\_Q \text{ FMAX Spec})/4$ (for FREQ_SEL HIGH)
2.5MHz to $(2X\_Q \text{ FMAX Spec})/8$ (for FREQ_SEL LOW)

Note: If the $\overline{OE}/\text{RST}$ input is active, a pull-up or pull-down resistor isn't necessary at the FEEDBACK pin so it won't when the feedback output goes into 3-state.

Figure 2a. Wiring Diagram and Frequency Relationships With Q/2 Output Feed Back



1:1 Input to “Q” Output Frequency Relationship

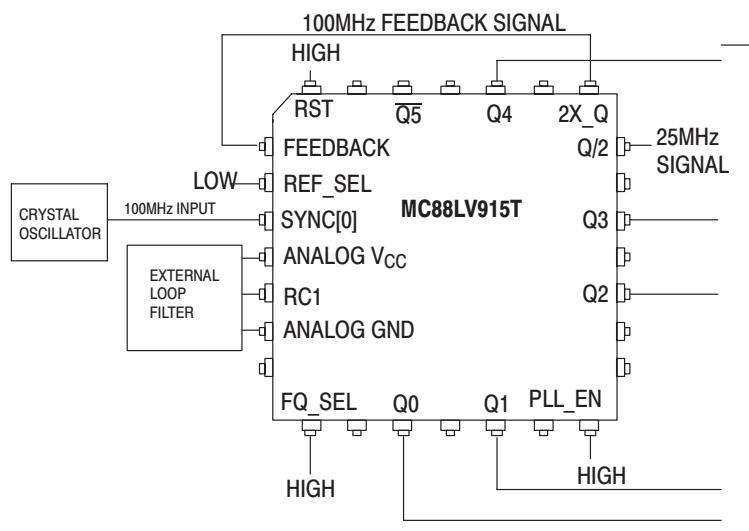
In this application, the Q4 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q4 and SYNC, thus the Q4 frequency (and the rest of the “Q” outputs) will equal the SYNC frequency. The Q/2 output will always run at 1/2 the “Q” frequency, and the 2X_Q output will run at 2X the “Q” frequency.

50MHz
“Q”
CLOCK
OUTPUTS

Allowable Input Frequency Range:

10MHz to $(2X\_Q \text{ FMAX Spec})/2$ (for FREQ_SEL HIGH)
5MHz to $(2X\_Q \text{ FMAX Spec})/4$ (for FREQ_SEL LOW)

Figure 2b. Wiring Diagram and Frequency Relationships With Q4 Output Feed Back



2:1 Input to “Q” Output Frequency Relationship

In this application, the 2X_Q output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of 2X_Q and SYNC, thus the 2X_Q frequency will equal the SYNC frequency. The Q/2 output will always run at 1/4 the 2X_Q frequency, and the “Q” outputs will run at 1/2 the 2X_Q frequency.

50MHz
“Q”
CLOCK
OUTPUTS

Allowable Input Frequency Range:

20MHz to $(2X\_Q \text{ FMAX Spec})$ (for FREQ_SEL HIGH)
10MHz to $(2X\_Q \text{ FMAX Spec})/2$ (for FREQ_SEL LOW)

Figure 2c. Wiring Diagram and Frequency Relationships with 2X_Q Output Feed Back

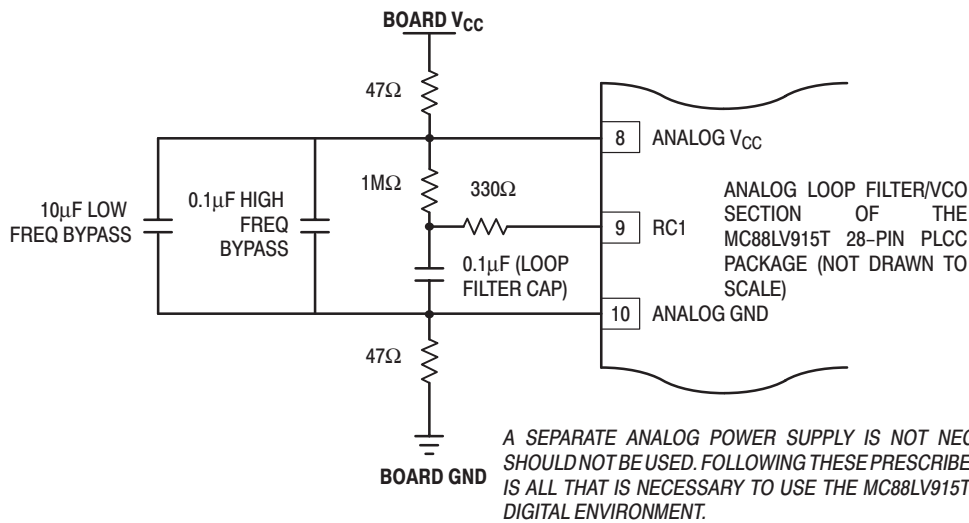


Figure 3. Recommended Loop Filter and Analog Isolation Scheme for the MC88LV915T

Notes Concerning Loop Filter and Board Layout Issues

1. Figure 3 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter-free operation:

1a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.

1b. The 47Ω resistors, the 10µF low frequency bypass capacitor, and the 0.1µF high frequency bypass capacitor form a wide bandwidth filter that will minimize the 88LV915T's sensitivity to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital V_{CC} supply will cause no more than a 100pS phase deviation on the 88LV915T outputs. A 250mV step deviation on V_{CC} using the recommended filter values should cause no more than a 250pS phase deviation; if a 25µF bypass capacitor is used (instead of 10µF) a 250mV V_{CC} step should cause no more than a 100pS phase deviation.

If good bypass techniques are used on a board design near components which may cause digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the 88LV915T's digital V_{CC} supply. The purpose

of the bypass filtering scheme shown in Figure 3 is to give the 88LV915T additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

1c. There are no special requirements set forth for the loop filter resistors (1MΩ and 330Ω). The loop filter capacitor (0.1µF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.

1d. The 1M reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead-band. If the VCO (2X_Q output) is running above 40MHz, the 1MΩ resistor provides the correct amount of current injection into the charge pump (2–3µA). For the TFN55, 70 or 100, if the VCO is running below 40MHz, a 1.5MΩ reference resistor should be used (instead of 1MΩ).

2. In addition to the bypass capacitors used in the analog filter of Figure 3, there should be a 0.1µF bypass capacitor between each of the other (digital) four V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the 88LV915T outputs, in addition to reducing potential for noise in the 'analog' section of the chip. These bypass capacitors should also be tied as close to the 88LV915T package as possible.

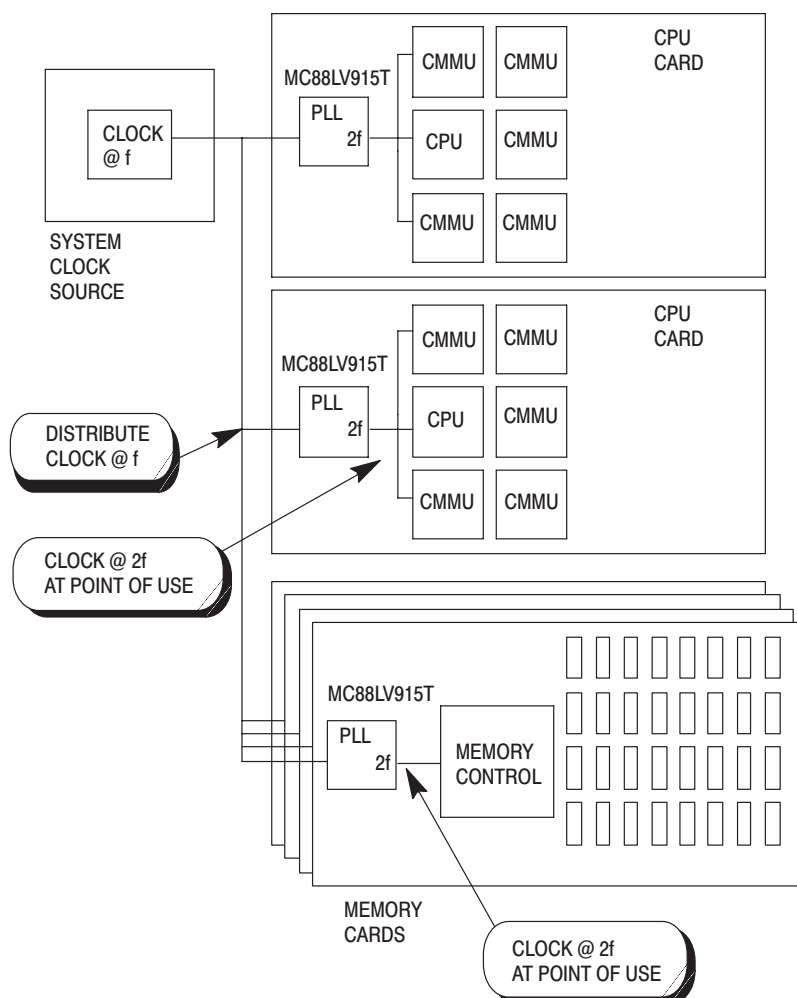


Figure 4. Representation of a Potential Multi-Processing Application Utilizing the MC88LV915T for Frequency Multiplication and Low Board-to-Board Skew

MC88LV915T System Level Testing Functionality

3-state functionality has been added to the 100MHz version of the MC88LV915T to ease system board testing. Bringing the $\overline{OE/RST}$ pin low will put all outputs (except for LOCK) into the high impedance state. As long as the PLL_EN pin is low, the Q0–Q4, Q5, and the Q/2 outputs will remain reset in the low state after the $\overline{OE/RST}$ until a falling SYNC edge is seen. The 2X_Q output will be the inverse of the SYNC signal in this mode. If the 3-state functionality will be used, a pull-up or pull-down resistor must be tied to the FEEDBACK input pin to prevent it from floating when the feedback output goes into high impedance.

With the PLL_EN pin low the selected SYNC signal is gated directly into the internal clock distribution network, bypassing and disabling the VCO. In this mode the outputs are directly driven by the SYNC input (per the block diagram). This mode can also be used for low frequency board testing.

Note: If the outputs are put into 3-state during normal PLL operation, the loop will be broken and phase-lock will be lost. It will take a maximum of 10mS (tLOCK spec) to regain phase-lock after the $\overline{OE/RST}$ pin goes back high.

Low Skew CMOS PLL 68060 Clock Driver

2

The MC88LV926 Clock Driver utilizes phase-locked loop technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for CISC microprocessor or single processor RISC systems. The $\overline{\text{RST\_IN}}/\text{RST\_OUT(LOCK)}$ pins provide a processor reset function designed specifically for the MC68/EC/LC030/040/060 microprocessor family. To support the 68060 processor, the 88LV926 operates from a 3.3V as well as a 5.0V supply.

The PLL allows the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple locations on a board. The PLL also allows the MC88LV926 to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency.

- 2X_Q Output Meets All Requirements of the 50 and 66MHz 68060 Microprocessor PCLK Input Specifications
- Low Voltage 3.3V V_{CC}
- Three Outputs (Q0–Q2) With Output–Output Skew <500ps
- $\overline{\text{CLKEN}}$ Output for Half Speed Bus Applications
- The Phase Variation From Part-to-Part Between SYNC and the 'Q' Outputs Is Less Than 600ps (Derived From the T_{PD} Specification, Which Defines the Part-to-Part Skew)
- SYNC Input Frequency Range From 5MHZ to $2X\_Q F_{Max}/4$
- All Outputs Have $\pm 36\text{mA}$ Drive (Equal High and Low) CMOS Levels
- Can Drive Either CMOS or TTL Inputs. All Inputs Are TTL–Level Compatible with $V_{CC} = 3.3\text{V}$
- Test Mode Pin (PLL_EN) Provided for Low Frequency Testing

Three 'Q' outputs (Q0–Q2) are provided with less than 500ps skew between their rising edges. A 2X_Q output runs at twice the 'Q' output frequency. The 2X_Q output is ideal for 68060 systems which require a 2X processor clock input, and it meets the tight duty cycle spec of the 50 and 66MHz 68060. The QCLKEN output is designed to drive the $\overline{\text{CLKEN}}$ input of the 68060 when the bus logic runs at half of the microprocessor clock rate. The QCLKEN output is skewed relative to the 2X_Q output to ensure that $\overline{\text{CLKEN}}$ setup and hold times of the 68060 are satisfied. A Q/2 frequency is fed back internally, providing a fixed 2X multiplication from the 'Q' outputs to the SYNC input. Since the feedback is done internally (no external feedback pin is provided) the input/output frequency relationships are fixed. The $\overline{\text{Q3}}$ output provides an inverted clock output to allow flexibility in the clock tree design.

In normal phase-locked operation the PLL_EN pin is held high. Pulling the PLL_EN pin low disables the VCO and puts the 88LV926 in a static 'test mode'. In this mode there is no frequency limitation on the input clock, which is necessary for a low frequency board test environment.

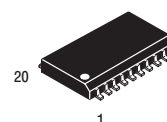
The $\overline{\text{RST\_OUT(LOCK)}}$ pin doubles as a phase-lock indicator. When the $\overline{\text{RST\_IN}}$ pin is held high, the open drain $\overline{\text{RST\_OUT}}$ pin will be pulled actively low until phase-lock is achieved. When phase-lock occurs, the $\overline{\text{RST\_OUT(LOCK)}}$ is released and a pull-up resistor will pull the signal high. To give a processor reset signal, the $\overline{\text{RST\_IN}}$ pin is toggled low, and the $\overline{\text{RST\_OUT(LOCK)}}$ pin will stay low for 1024 cycles of the 'Q' output frequency after the $\overline{\text{RST\_IN}}$ pin is brought back high.

Description of the $\overline{\text{RST\_IN}}/\text{RST\_OUT(LOCK)}$ Functionality

The $\overline{\text{RST\_IN}}$ and $\overline{\text{RST\_OUT(LOCK)}}$ pins provide a 68030/040/060 processor reset function, with the $\overline{\text{RST\_OUT}}$ pin also acting as a lock indicator. If the $\overline{\text{RST\_IN}}$ pin is held high during system power-up, the $\overline{\text{RST\_OUT}}$ pin will be in the low state until steady state phase/frequency lock to the input reference is achieved. 1024 'Q' output cycles after phase-lock is achieved the $\overline{\text{RST\_OUT(LOCK)}}$ pin will go into a high impedance state, allowing it to be pulled high by an external pull-up resistor (see the AC/DC specs for the characteristics of the $\overline{\text{RST\_OUT(LOCK)}}$ pin). If the $\overline{\text{RST\_IN}}$ pin is held low during power-up, the $\overline{\text{RST\_OUT(LOCK)}}$ pin will remain low.

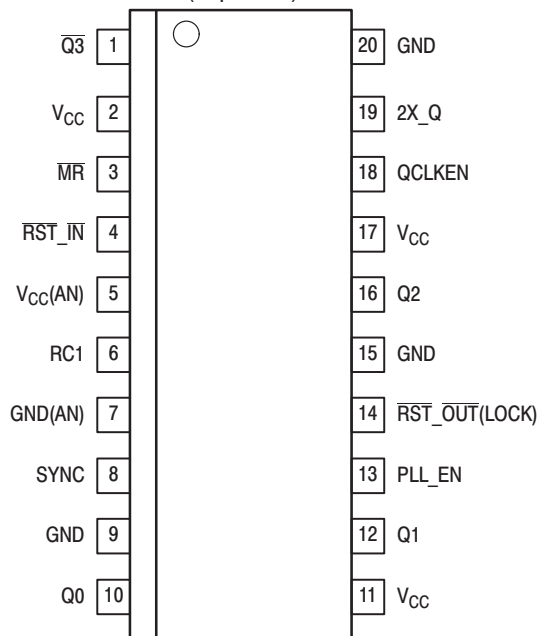
MC88LV926

**LOW SKEW CMOS PLL
68060 CLOCK DRIVER**



DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D

Figure 1. Pinout: 20-Lead Wide SOIC Package
(Top View)



2

Description of the $\overline{\text{RST\_IN}}/\overline{\text{RST\_OUT(LOCK)}}$ Functionality (continued)

After the system start-up is complete and the 88LV926 is phase-locked to the SYNC input signal ($\overline{\text{RST\_OUT}}$ high), the processor reset functionality can be utilized. When the $\overline{\text{RST\_IN}}$ pin is toggled low (min. pulse width=10nS), $\overline{\text{RST\_OUT(LOCK)}}$ will go to the low state and remain there for 1024 cycles of the 'Q' output frequency (512 SYNC cycles). During the time in which the $\overline{\text{RST\_OUT(LOCK)}}$ is actively pulled low, all the 88LV926 clock outputs will continue operating correctly and in a locked condition to the SYNC input (clock signals to the 68030/040/060 family of processors must continue while the processor is in reset). A propagation delay after the 1024th cycle $\overline{\text{RST\_OUT(LOCK)}}$ goes back to the high impedance state to be pulled high by the resistor.

Power Supply Ramp Rate Restriction for Correct 030/040 Processor Reset Operation During System Start-up

Because the $\overline{\text{RST\_OUT(LOCK)}}$ pin is an indicator of phase-lock to the reference source, some constraints must be

placed on the power supply ramp rate to make sure the $\overline{\text{RST\_OUT(LOCK)}}$ signal holds the processor in reset during system start-up (power-up). With the recommended loop filter values (see Figure 5.) the lock time is approximately 10ms. The phase-lock loop will begin attempting to lock to a reference source (if it is present) when VCC reaches 2V. If the VCC ramp rate is significantly slower than 10ms, then the PLL could lock to the reference source, causing $\overline{\text{RST\_OUT(LOCK)}}$ to go high before the 88LV926 and '030/040 processor is fully powered up, violating the processor reset specification. Therefore, if it is necessary for the $\overline{\text{RST\_IN}}$ pin to be held high during power-up, the VCC ramp rate must be less than 10mS for proper 68030/040/060 reset operation.

This ramp rate restriction can be ignored if the $\overline{\text{RST\_IN}}$ pin can be held low during system start-up (which holds $\overline{\text{RST\_OUT}}$ low). The $\overline{\text{RST\_OUT(LOCK)}}$ pin will then be pulled back high 1024 cycles after the $\overline{\text{RST\_IN}}$ pin goes high.

CAPACITANCE AND POWER SPECIFICATIONS

Symbol	Parameter	Value Typ	Unit	Test Conditions
C _{IN}	Input Capacitance	4.5*	pF	V _{CC} = 5.0V
C _{PD}	Power Dissipation Capacitance	40*	pF	V _{CC} = 5.0V
PD ₁	Power Dissipation at 33MHz With 50Ω Thevenin Termination	15mW/Output* 90mW/Device	mW	V _{CC} = 5.0V T = 25°C
PD ₂	Power Dissipation at 33MHz With 50Ω Parallel Termination to GND	37.5mW/Output* 225mW/Device	mW	V _{CC} = 5.0V T = 25°C

* Value at V_{CC} = 3.3V TBD.

MAXIMUM RATINGS*

Symbol	Parameter	Limits	Unit
V_{CC} , AV_{CC}	DC Supply Voltage Referenced to GND	-0.5 to 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, Per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, Per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current Per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits	Unit
V_{CC}	Supply Voltage	3.3 ± 0.3	V
V_{in}	DC Input Voltage	0 to V_{CC}	V
V_{out}	DC Output Voltage	0 to V_{CC}	V
T_A	Ambient Operating Temperature	0 to 70	°C
ESD	Static Discharge Voltage	> 1500	V

DC CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C ; $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$)⁴

Symbol	Parameter	V_{CC}	Guaranteed Limits	Unit	Condition
V_{IH}	Minimum High Level Input Voltage ⁴	3.0 3.3	2.0 2.0	V	$V_{OUT} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$
V_{IL}	Minimum Low Level Input Voltage	3.0 3.3	0.8 0.8	V	$V_{OUT} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$
V_{OH}	Minimum High Level Output Voltage	3.0 3.3	2.2 2.5	V	$V_{IN} = V_{IH}$ or $V_{IL} = -24\text{mA}$ $I_{OH} = -24\text{mA}$
V_{OL}	Minimum Low Level Output Voltage	3.0 3.3	0.55 0.55	V	$V_{IN} = V_{IH}$ or $V_{IL} = +24\text{mA}$ ¹ $I_{OH} = +24\text{mA}$
I_{IN}	Maximum Input Leakage Current	3.3	± 1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC} /Input	3.3	2.0 ²	mA	$V_I = V_{CC} - 2.1\text{V}$
I_{OLD}	Minimum Dynamic ³ Output Current	3.3	50	mA	$V_{OLD} = 1.25\text{V}$ Max
I_{OHD}		3.3	-50	mA	$V_{OHD} = 2.35$ Min
I_{CC}	Maximum Quiescent Supply Current	3.3	750	μA	$V_I = V_{CC}$, GND

1. I_{OL} is +12mA for the RST_OUT output.

2. The PLL_EN input pin is not guaranteed to meet this specification.

3. Maximum test duration 2.0ms, one output loaded at a time.

4. The MC88LV926 can also be operated from a 5.0V supply. V_{OH} output levels will vary 1:1 with V_{CC} , input levels and current specs will be unchanged, except V_{IH} ; when $V_{CC} > 4.0$ volts, V_{IH} minimum level is 2.7 volts.

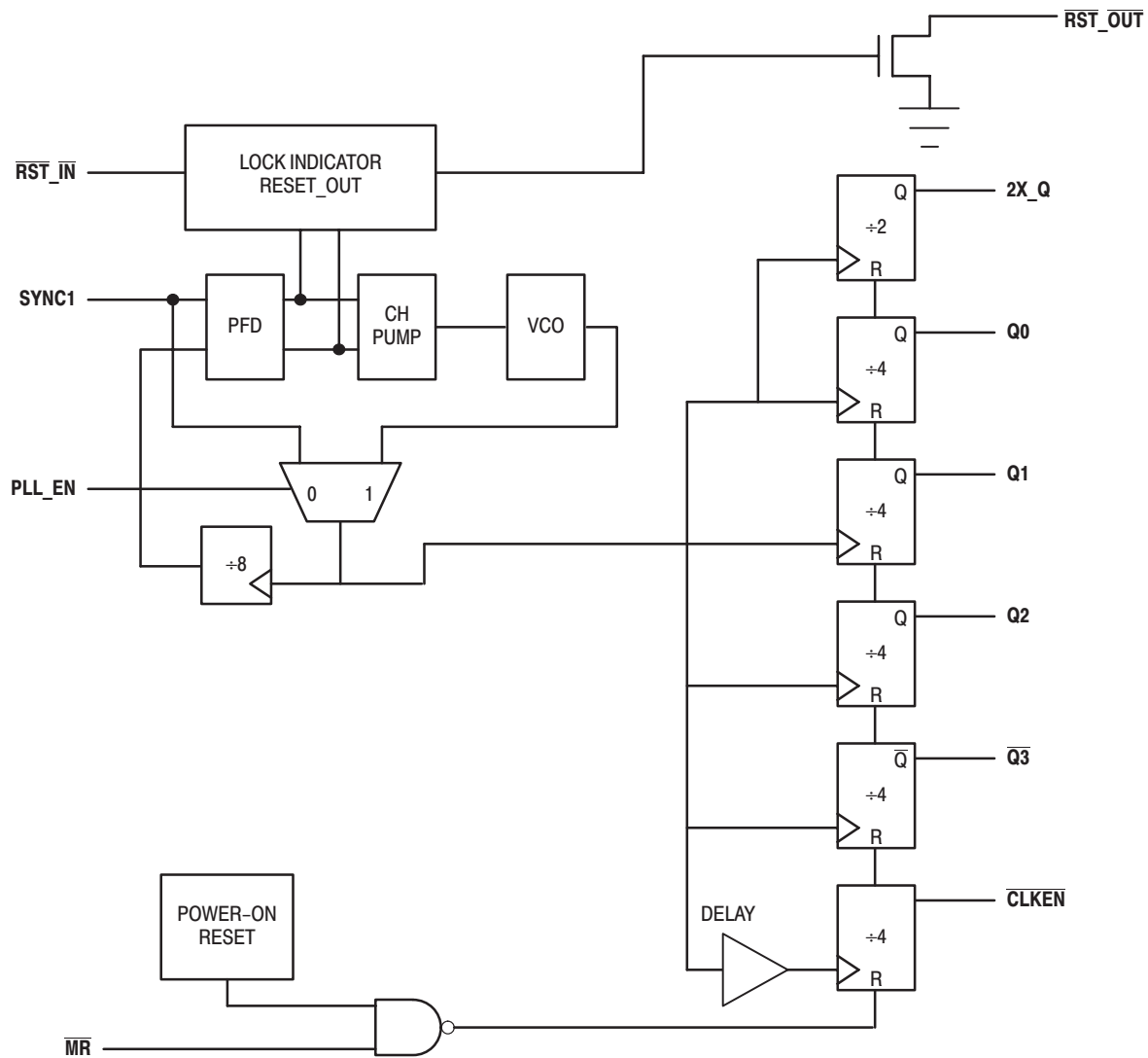


Figure 2. MC88LV926 Logic Block Diagram

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL}$ SYNC Input	Rise/Fall Time, SYNC Input From 0.8V to 2.0V	—	5.0	ns
t_{CYCLE} SYNC Input	Input Clock Period SYNC Input ¹	$\frac{1}{f_{2X\_Q/4}}$	200 ¹	ns
Duty Cycle	Duty Cycle, SYNC Input	50% ± 25%		

1. When $V_{CC} > 4.0$ volts, Maximum SYNC Input Period is 125ns.

FREQUENCY SPECIFICATIONS ($T_A = 0^\circ\text{C}$ to 70°C ; $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ or $5.0\text{V} \pm 5\%$)

Symbol	Parameter	Guaranteed Minimum	Unit
f_{max} (2X_Q)	Maximum Operating Frequency, 2X_Q Output	66	MHz
f_{max} ('Q')	Maximum Operating Frequency, Q0–Q3 Outputs	33	MHz

Maximum Operating Frequency is guaranteed with the 88LV926 in a phase-locked condition.

AC CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C ; $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ or $5.0\text{V} \pm 5\%$)

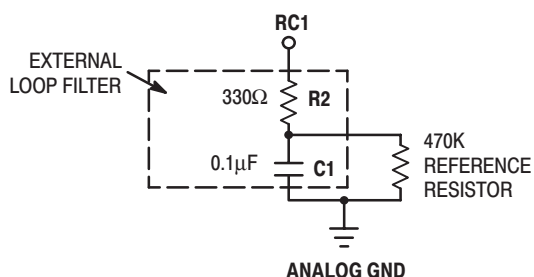
Symbol	Parameter	Minimum	Maximum	Unit	Condition
$t_{\text{RISE/FALL}}$ All Outputs	Rise/Fall Time, into 50Ω Load	0.3	1.6	ns	$t_{\text{RISE}} - 0.8\text{V}$ to 2.0V $t_{\text{FALL}} - 2.0\text{V}$ to 0.8V
$t_{\text{RISE/FALL}}$ 2X_Q Output	Rise/Fall Time into a 50Ω Load	0.5	1.6	ns	$t_{\text{RISE}} - 0.8\text{V}$ to 2.0V $t_{\text{FALL}} - 2.0\text{V}$ to 0.8V
$t_{\text{pulse width(a)}}^1$ (Q0, Q1, Q2, Q3)	Output Pulse Width Q0, Q1, Q2, Q3 at 1.65V	$0.5t_{\text{cycle}} - 0.5$	$0.5t_{\text{cycle}} + 0.5$	ns	50Ω Load Terminated to $V_{CC}/2$ (See Application Note 3)
$t_{\text{pulse width(b)}}^1$ (2X_Q Output)	Output Pulse Width 2X_Q at 1.65V	$0.5t_{\text{cycle}} - 0.5$	$0.5t_{\text{cycle}} + 0.5$	ns	50Ω Load Terminated to $V_{CC}/2$ (See Application Note 3)
$t_{\text{SKEW}_r}^2$ (Rising)	Output-to-Output Skew Between Outputs Q0-Q2 (Rising Edge Only)	—	500	ps	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 4.)
$t_{\text{SKEW}_f}^2$ (Falling)	Output-to-Output Skew Between Outputs Q0-Q2 (Falling Edge Only)	—	1.0	ns	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 4.)
$t_{\text{SKEW}_{\text{all}}}^2$	Output-to-Output Skew 2X_Q, Q0-Q2, Q3	—	750	ps	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 4.)
$t_{\text{SKEW QCLKEN}}^{1,2}$	Output-to-Output Skew QCLKEN to 2X_Q 2X_Q = 50MHz 2X_Q = 66MHz	9.7^6 7.0^6	—	ns	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 4.)
t_{LOCK}^3	Phase-Lock Acquisition Time, All Outputs to SYNC Input	1	10	ms	
$t_{\text{PHL}} \overline{\text{MR}} - \text{Q}^1$	Propagation Delay, $\overline{\text{MR}}$ to Any Output (High-Low)	1.5	13.5	ns	Into a 50Ω Load Terminated to $V_{CC}/2$
$t_{\text{REC}, \overline{\text{MR}}}$ to SYNC ^{5, 1}	Reset Recovery Time rising $\overline{\text{MR}}$ edge to falling SYNC edge	9	—	ns	
$t_{\text{W}, \overline{\text{MR}} \text{ LOW}}^{5, 1}$	Minimum Pulse Width, $\overline{\text{MR}}$ input Low	5	—	ns	
$t_{\text{W}, \text{RST\_IN LOW}}^1$	Minimum Pulse Width, RST_IN Low	10	—	ns	When in Phase-Lock
t_{PZL}^1	Output Enable Time RST_IN Low to RST_OUT Low	1.5	16.5	ns	See Application Note 5
t_{PLZ}^1	Output Enable Time RST_IN High to RST_OUT High Z	1016 'Q' Cycles (508 Q/2 Cycles)	1024 'Q' Cycles (512 Q/2 Cycles)	ns	See Application Note 5

1. These specifications are not tested, they are guaranteed by statistical characterization. See Application Note 1 for a discussion of this methodology.
2. Under equally loaded conditions and at a fixed temperature and voltage.
3. With V_{CC} fully powered-on: t_{LOCK} Max is with $C1 = 0.1\mu\text{F}$; t_{LOCK} Min is with $C1 = 0.01\mu\text{F}$.
4. See Application Note 4 for the distribution in time of each output referenced to SYNC.
5. Specification is valid only when the PLL_EN pin is low.
6. Guaranteed that QCLKEN will meet the setup and hold time requirement of the 68060.

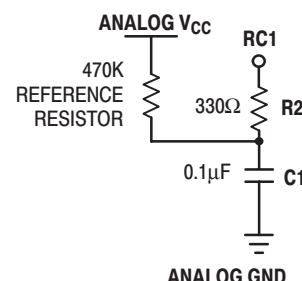
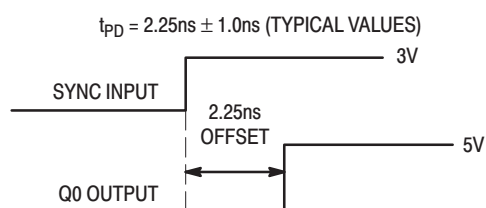
Application Notes

1. Several specifications can only be measured when the MC88LV926 is in phase-locked operation. It is not possible to have the part in phase-lock on ATE (automated test equipment). Statistical characterization techniques were used to guarantee those specifications which cannot be measured on the ATE. MC88LV926 units were fabricated with key transistor properties intentionally varied to create a 14 cell designed experimental matrix. IC performance was characterized over a range of transistor properties (represented by the 14 cells) in excess of the expected process variation of the wafer fabrication area. Response Surface Modeling (RSM) techniques were used to relate IC performance to the CMOS transistor properties over operation voltage and temperature. IC performance to each specification and fab variation were used in conjunction with Yield Surface Modeling™ (YSM™) methodology to set performance limits of ATE testable specifications within those which are to be guaranteed by statistical characterization. In this way, all units passing the ATE test will meet or exceed the non-tested specifications limits.
2. A 470K Ω resistor tied to either Analog V_{CC} or Analog GND, as shown in Figure 1., is required to ensure no jitter is present on the MC88LV926 outputs. This technique causes a phase offset between the SYNC input and the Q0 output, measured at the pins. The t_{PD} spec describes how this offset varies with process, temperature, and voltage. The specs were arrived at by measuring the phase relationship for the 14 lots described in note 1 while the part was in phase-locked operation. The actual measurements were made with a 10MHz SYNC input (1.0ns edge rate from 0.8V to 2.0V). The phase measurements were made at 1.5V. See Figure 1. for a graphical description.
3. Two specs ($t_{RISE/FALL}$ and t_{PULSE} Width 2X_Q output, see AC Specifications) guarantee that the MC88LV926 meets the 33MHz and 66MHz 68060 P-Clock input specification.

2



WITH THE 470K Ω RESISTOR TIED IN THIS FASHION THE T_{PD} SPECIFICATION, MEASURED AT THE INPUT PINS IS:



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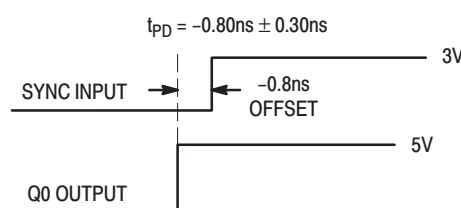


Figure 1. Depiction of the Fixed SYNC to Q0 Offset (t_{PD}) Which Is Present When a 470K Ω Resistor Is Tied to V_{CC} or Ground

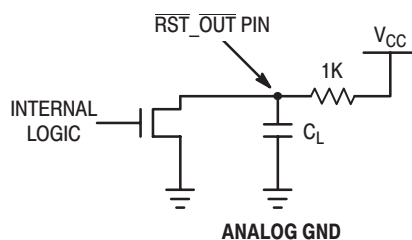


Figure 2. RST_OUT Test Circuit

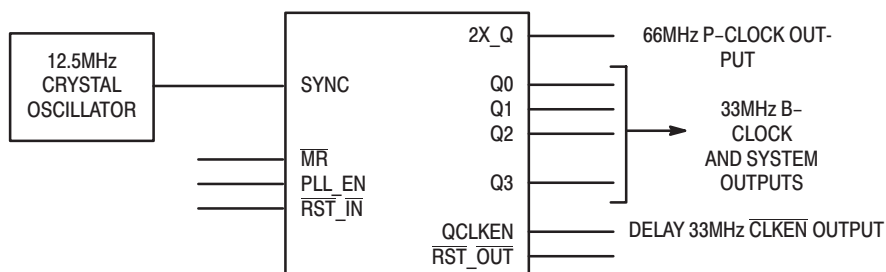


Figure 3. Logical Representation of the MC88LV926 With Input/Output Frequency Relationships

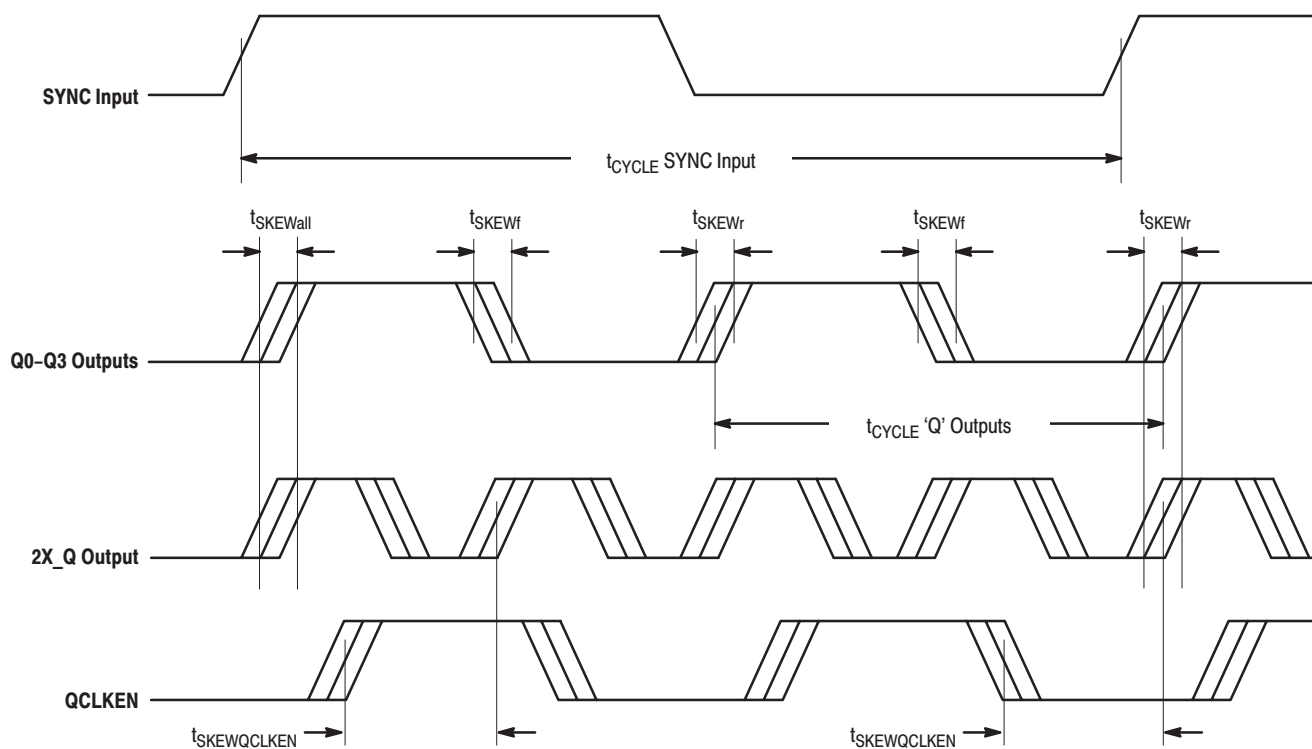


Figure 4. Output/Input Switching Waveforms and Timing Relationships

Timing Notes

1. The MC88LV926 aligns rising edges of the outputs and the SYNC input, therefore the SYNC input does not require a 50% duty cycle.
2. All skew specs are measured between the V_{CC}/2 crossing point of the appropriate output edges. All skews are specified as 'windows', not as a $\pm$ deviation around a center point.

The t_{PD} spec includes the full temperature range from 0°C to 70°C and the full V_{CC} range from 3.0V to 3.3V. If the ΔT and ΔV_{CC} in a given system are less than the specification limits, the t_{PD} spec window will be reduced. The t_{PD} window for a given ΔT and ΔV_{CC} is given by the following regression formula:

TBD

Notes Concerning Loop Filter and Board Layout Issues

1. Figure 5. shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter-free operation:

- 1a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.
- 1b. The 47 Ω resistors, the 10 μ F low frequency bypass capacitor, and the 0.1 μ F high frequency bypass capacitor form a wide bandwidth filter that will make the 88LV926 PLL insensitive to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital V_{CC} supply will cause no more than a 100ps phase deviation on the 88LV926 outputs. A 250mV step deviation on V_{CC} using the recommended filter values will cause no more than a 250ps phase deviation; if a 25 μ F bypass capacitor is used (instead of 10 μ F) a 250mV V_{CC} step will cause no more than a 100ps phase deviation.

If good bypass techniques are used on a board design near components which may cause digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the 88LV926's digital V_{CC} supply. The purpose of the bypass filtering scheme shown in Figure 5. is to give

5. The $\overline{RST\_OUT}$ pin is an open drain N-Channel output. Therefore an external pull-up resistor must be provided to pull up the $\overline{RST\_OUT}$ pin when it goes into the high impedance state (after the MC88LV926 is phase-locked to the reference input with $\overline{RST\_IN}$ held high or 1024 'Q' cycles after the $\overline{RST\_IN}$ pin goes high when the part is locked). In the t_{PLZ} and t_{PZL} specifications, a 1K Ω resistor is used as a pull-up as shown in Figure 2.

the 88LV926 additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

- 1c. There are no special requirements set forth for the loop filter resistors (470K and 330 Ω). The loop filter capacitor (0.1 μ F) can be a ceramic chip capacitor, the same as a standard bypass capacitor.
- 1d. The 470K reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead-band. If the VCO (2X_Q output) is running above 40MHz, the 470K resistor provides the correct amount of current injection into the charge pump (2–3 μ A). If the VCO is running below 40MHz, a 1M Ω reference resistor should be used (instead of 470K).
2. In addition to the bypass capacitors used in the analog filter of Figure 5., there should be a 0.1 μ F bypass capacitor between each of the other (digital) four V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the 88LV926 outputs, in addition to reducing potential for noise in the 'analog' section of the chip. These bypass capacitors should also be tied as close to the 88LV926 package as possible.

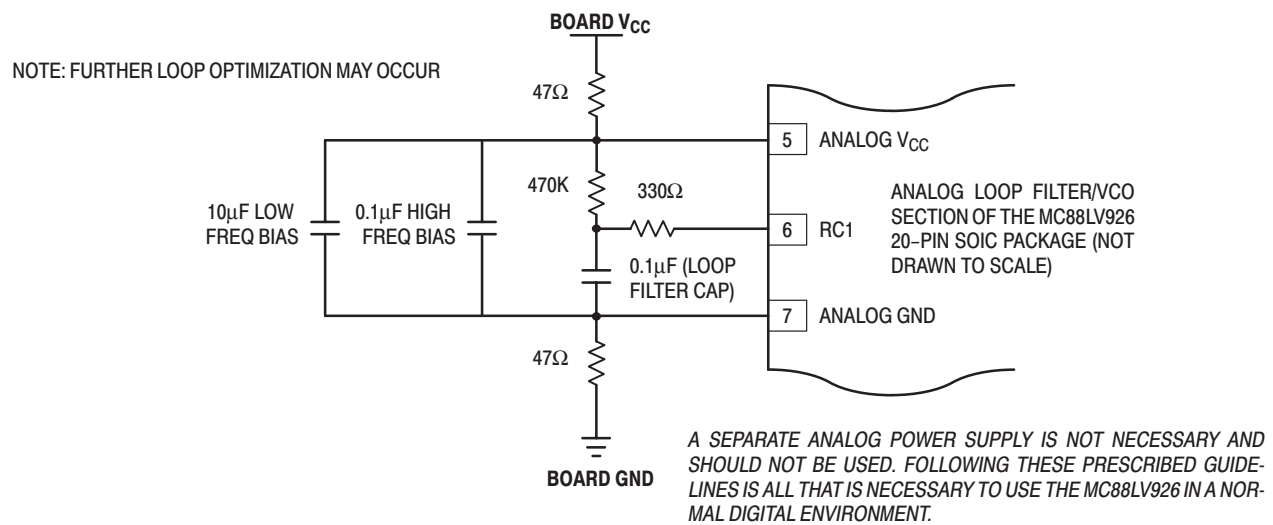


Figure 5. Recommended Loop Filter and Analog Isolation Scheme for the MC88LV926

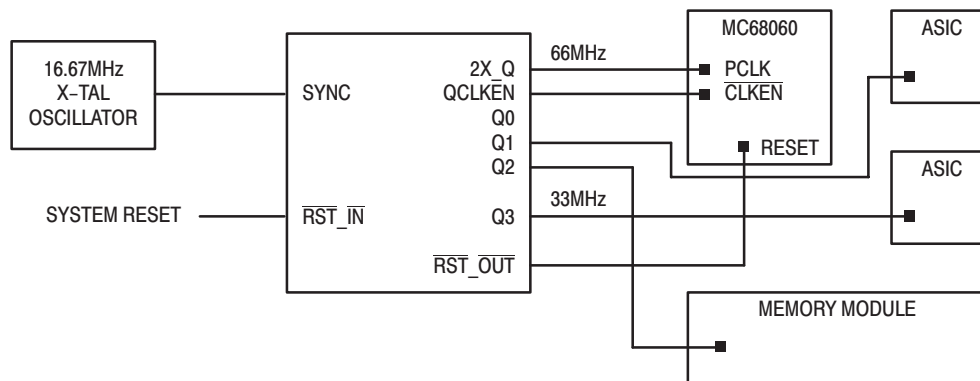


Figure 6. Typical MC88LV926/MC68060 System Configuration

Low Voltage PLL Clock Driver

The MPC930/931 is a 3.3V compatible, PLL based clock driver device targeted for high performance clock applications. With output frequencies of up to 150MHz and output skews of 300ps the MPC930/931 is ideal for the most demanding clock distribution designs. The device employs a fully differential PLL design to minimize cycle to cycle and long term jitter. This parameter is of significant importance when the clock driver is providing the reference clock for PLL's on board today's microprocessors and ASIC's. The device offers 6 low skew outputs, and a choice between internal or external feedback. The feedback option adds to the flexibility of the device, providing numerous input to output frequency relationships.

- On-Board Crystal Oscillator (MPC930)
- Differential LVPECL Reference Input (MPC931)
- Fully Integrated PLL
- Output Shut Down Mode
- Output Frequency up to 150MHz
- Compatible with PowerPC™ and Intel Microprocessors
- 32-Lead TQFP Packaging
- Power Down Mode
- ± 100 ps Typical Cycle-to-Cycle Jitter

The MPC930 and MPC931 are very similar in basic functionality, but there are some minor differences. The MPC931 has been optimized for use as a zero delay buffer. In addition to tighter specification limits on the phase offset of the device, a higher speed VCO has been used on the MPC931. The MPC930, on the other hand, is more optimized for use as a clock generator. When choosing between the 930 and 931, pay special attention to the differences in the AC parameters of each device.

The MPC930/931 offers two power saving features for power conscious portable or "green" designs. The power down pin will seamlessly reduce all of the clock rates by one half so that the system will run at half the potential clock rate to extend battery life. The POWER_DN pin is synchronized internally to the slowest output clock rate. This allows the transition in and out of the power-down mode to be output glitch free. In addition, the shut down control pins will turn off various combinations of clock outputs while leaving a subset active to allow for total processor shut down while maintaining system monitors to "wake up" the system when signaled. During shut down, the PLL will remain locked, if internal feedback is used, so that wake up time will be minimized. The shut down and power down pins can be combined for the ultimate in power savings. The Shut_Dn pins are synchronized to the clock internal to the chip to eliminate the possibility of generating runt pulses.

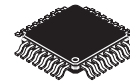
The MPC930/931 devices offer a great deal of flexibility in what is used as the PLL reference. The MPC930 offers an integrated crystal oscillator that allows for an inexpensive crystal to be used as the frequency reference. For more information on the crystal oscillator please refer to the applications section of this data sheet. In those applications where the 930/931 will be used to regenerate clocks from an existing source or as a zero delay buffer, alternative reference clock inputs are provided. Both devices offer an LVCMOS input that can be used as the PLL reference. In addition the MPC931 replaces the crystal oscillator inputs with a differential PECL reference clock input that allows the device to be used in mixed technology clock distribution trees.

An internal feedback divide by 8 of the VCO frequency is compared with the input reference provided by the on-board crystal oscillator when the internal feedback is selected. The on-board crystal oscillator requires no external components other than a series resonant crystal (see Applications Information section for more on crystals). The internal VCO is running at 8x the input reference clock. The outputs can be configured to run at 4x, 2x, 1.25x or 0.66x the input reference frequency. If the external feedback is selected, one of the MPC931's outputs must be connected to the Ext_FB pin. Using the external feedback, numerous input/output frequency relationships can be developed.

The MPC930/931 is fully 3.3V compatible and requires no external loop filter components. All control inputs accept LVCMOS or LVTTTL compatible levels while the outputs provide LVCMOS levels with the capability to drive terminated 50 Ω transmission lines. For series terminated applications, each output can drive two 50 Ω transmission lines, effectively increasing the fanout to 1:12. The device is packaged in a 32-lead TQFP package to provide the optimum combination of board density and cost.

MPC930
MPC931

LOW VOLTAGE
PLL CLOCK DRIVER



FA SUFFIX
32-LEAD TQFP PACKAGE
CASE 873A-02

2

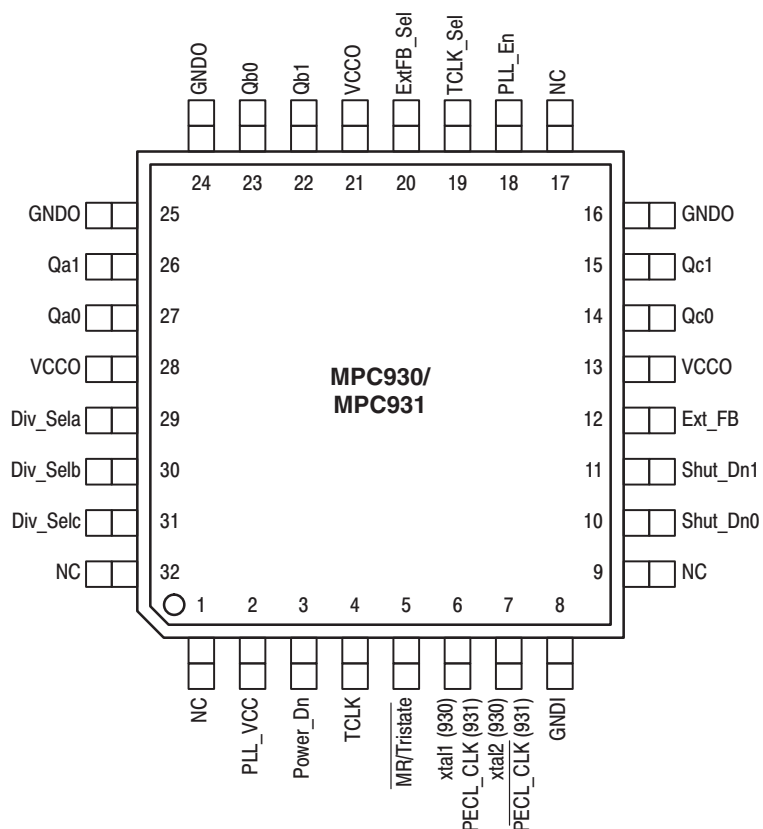


Figure 1. 32-Lead Pinout (Top View)

FUNCTION TABLES

TCLK_Sel	Reference
0	xtal (PECL_CLK)
1	TCLK
PLL_En	PLL Status
0	Test Mode
1	PLL Enabled
ExtFB_Sel	Reference
0	Int. ÷8
1	Ext_FB
Power_Dn	PLL Status
0	VCO/1
1	VCO/2
Div_Sela,b,c	Qa Qb Qc
0	÷2 ÷2 ÷4
1	÷4 ÷4 ÷6
MR/Tristate	PLL Status
0	Disabled
1	Enabled

Shut_Dn1	Shut_Dn0	Div_Seln
0	0	Qb & Qc Low, Qa Toggle
0	1	Qa & Qb Low, Qc Toggle
1	0	Qb Low, Qa & Qc Toggle
1	1	All Toggle

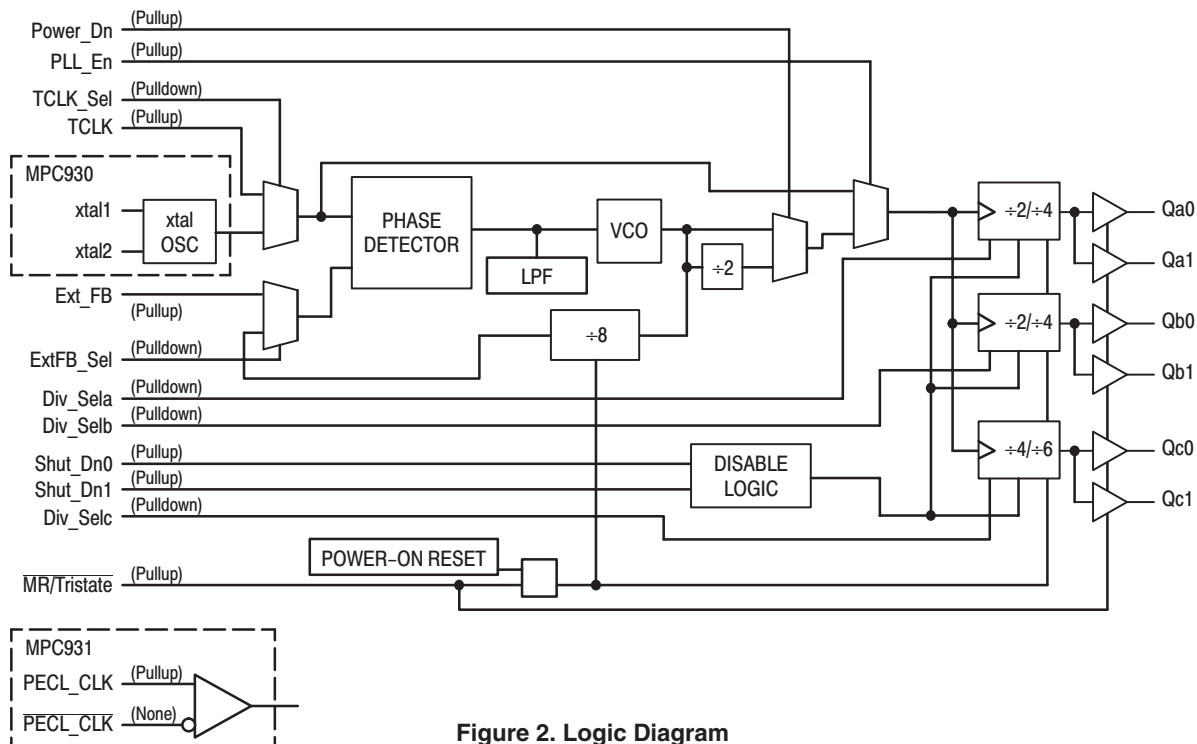


Figure 2. Logic Diagram

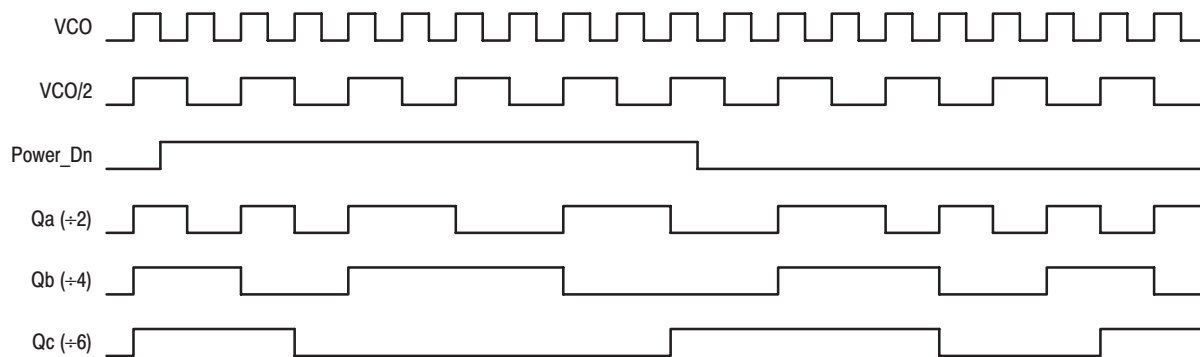


Figure 3. Power_Dn Timing Diagram

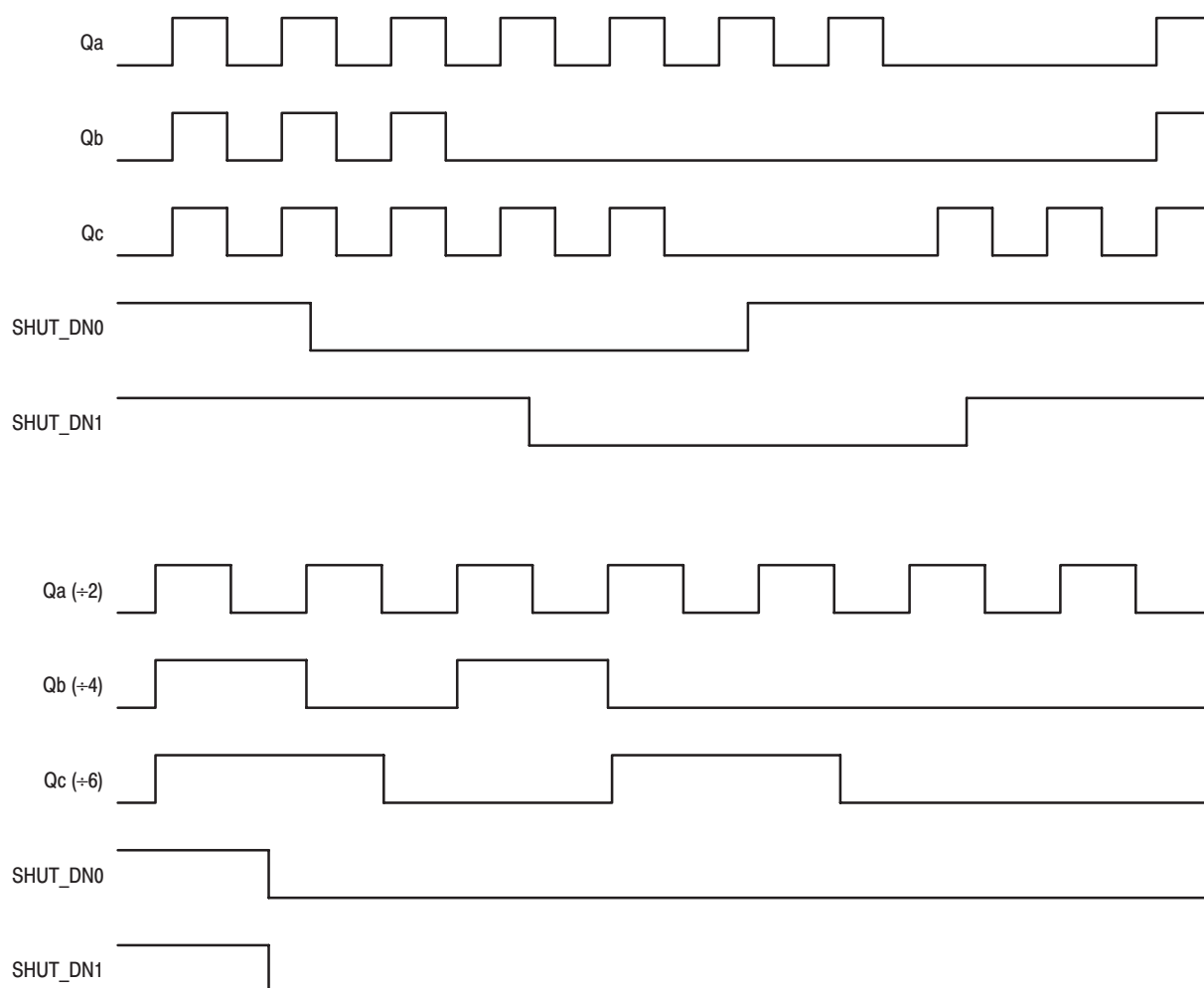


Figure 4. Shut_Dn Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	4.6	V
V_I	Input Voltage	-0.3	$V_{DD} + 0.3$	V
I_{IN}	Input Current		± 20	mA
T_{Stor}	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

PLL INPUT REFERENCE CHARACTERISTICS ($T_A = 0$ to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	10	Note 1.	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

1. Maximum input reference frequency is limited by the VCO lock range and the feedback divider.

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		3.6	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -20\text{mA}$ (Note 2.)
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 20\text{mA}$ (Note 2.)
I_{IN}	Input Current			± 120	μA	Note 3.
I_{CC}	Maximum Core Supply Current		65	85	mA	
I_{CCPLL}	Maximum PLL Supply Current		15	20	mA	
C_{IN}				4	pF	
C_{pd}			25		pF	Per Output

2. The MPC930/931 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}/2$) transmission lines on the incident edge (see Applications Info section).

3. Inputs have pull-up/pull-down resistors which affect input current.

MPC930 AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f_{xtal}	Crystal Oscillator Frequency Range	10		20	MHz	Note 5., Note 7.
f_{ref}	Input Reference Frequency	Note 7.		Note 7.	MHz	Ref = TCLK
t_{os}	Output-to-Output Skew (Note 4.)	Same Frequency Diff Frequency Same Frequency Diff Frequency	200 300 300 450	300 400 400 600	ps	$f_{\text{max}} \leq 100\text{MHz}$ $f_{\text{max}} \leq 100\text{MHz}$ $f_{\text{max}} > 100\text{MHz}$ $f_{\text{max}} > 100\text{MHz}$
f_{VCO}	VCO Lock Range	100		280	MHz	
f_{max}	Maximum Output Frequency	Qa, Qb (+2) Qa, Qb, Qc (+4) Qc (+6)		140 80 47	MHz	Note 4.
t_{pd}	TCLK to EXT_FB Delay	-600	-100	400	ps	$f_{\text{ref}} = 50\text{MHz}$, FB = +4
t_{pw}	Output Duty Cycle (Note 4.)	$t_{\text{CYCLE}}/2$ -750	$t_{\text{CYCLE}}/2$ ± 500	$t_{\text{CYCLE}}/2$ +750	ps	
t_r, t_f	Output Rise/Fall Time (Note 4.)	0.1		1.0	ns	0.8 to 2.0V
$t_{\text{PLZ}}, t_{\text{PHZ}}$	Output Disable Time	2.0		8.0	ns	50Ω to $V_{CC}/2$
t_{PZL}	Output Enable Time	2.0		10	ns	50Ω to $V_{CC}/2$
t_{jitter}	Cycle-to-Cycle Jitter (Peak-to-Peak)		± 100		ps	Note 6.
t_{lock}	Maximum PLL Lock Time			10	ms	

4. Measured with 50Ω to $V_{CC}/2$ termination.

5. See Applications Info section for more Crystal specifications.

6. See Applications Info section for more jitter information.

7. Input reference frequency is bounded by VCO lock range and feedback divide selection.

MPC931 AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f_{ref}	Input Reference Frequency	Note 11.		Note 11.	MHz	
t_{os}	Output-to-Output Skew (Note 8.)	Same Frequency Diff Frequency Same Frequency Diff Frequency	200 300 300 450	300 400 400 600	ps	$f_{\text{max}} \leq 100\text{MHz}$ $f_{\text{max}} \leq 100\text{MHz}$ $f_{\text{max}} > 100\text{MHz}$ $f_{\text{max}} > 100\text{MHz}$
f_{VCO}	VCO Lock Range	200		480	MHz	
f_{max}	Maximum Output Frequency	Qa, Qb (+2) Qa, Qb, Qc (+4) Qc (+6)		150 120 80	MHz	Note 9.
t_{pd}	Reference to EXT_FB Average Delay	TCLK -150 -400	0 -250	+150 -100	ps	$f_{\text{ref}} = 50\text{MHz}$; FB = +8; Note 12.
t_{pw}	Output Duty Cycle (Note 8.)	$t_{\text{CYCLE}}/2$ -750	$t_{\text{CYCLE}}/2$ ± 500	$t_{\text{CYCLE}}/2$ +750	ps	
t_r, t_f	Output Rise/Fall Time (Note 8.)	0.1		1.0	ns	0.8 to 2.0V
$t_{\text{PLZ}}, t_{\text{PHZ}}$	Output Disable Time	2.0		8.0	ns	50Ω to $V_{CC}/2$
t_{PZL}	Output Enable Time	2.0		10	ns	50Ω to $V_{CC}/2$
t_{jitter}	Cycle-to-Cycle Jitter (Peak-to-Peak)		± 100		ps	Note 10.
t_{lock}	Maximum PLL Lock Time			10	ms	

8. Measured with 50Ω to $V_{CC}/2$ termination.9. f_{max} limited by skew spec. Outputs will generate valid CMOS signals up to 180MHz.

10. See Applications Info section for more jitter information.

11. Input reference frequency is bounded by VCO lock range and feedback divide selection.

12. t_{pd} is specified for 50MHz input reference, the window will shrink/grow proportionally from the minimum limit with shorter/longer reference periods. The t_{pd} does not include jitter.

APPLICATIONS INFORMATION

Programming the MPC930/931

The MPC930/931 clock driver outputs can be configured into several frequency relationships, in addition the external feedback option allows for a great deal of flexibility in establishing unique input to output frequency relationships. The output dividers for the three output groups allows the user to configure the outputs into 1:1, 2:1, 3:1, 3:2 and 3:2:1 frequency ratios. The use of even dividers ensures that the output duty cycle is always 50%. Table 1 illustrates the various output configurations, the table describes the outputs using the VCO frequency as a reference. As an example for a 3:2:1 relationship the Qa outputs would be set at VCO/2, the Qb's at VCO/4 and the Qc's at VCO/6. These settings will provide output frequencies with a 3:2:1 relationship.

The division settings establish the output relationship, but one must still ensure that the VCO will be stable given the frequency of the outputs desired. The VCO lock range can be found in the specification tables. The feedback frequency and the Power_Dn pin can be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL is such that for output frequencies between 25 and 180MHz the MPC930/931 can generally be configured into a stable region.

The relationship between the input reference and the output frequency is also very flexible. Table 2 shows the multiplication factors between the inputs and outputs when the internal feedback option is used. For external feedback Table 1 can be used to determine the multiplication factor, there are too many potential combinations to tabularize the external feedback condition. Figure 5 through Figure 10 illustrates several programming possibilities, although not exhaustive it is representative of the potential applications.

Table 1. Programmable Output Frequency Relationships
(Power_Dn = '0')

INPUTS			OUTPUTS		
Div_Sela	Div_Selb	Div_Selc	Qa	Qb	Qc
0	0	0	VCO/2	VCO/2	VCO/4
0	0	1	VCO/2	VCO/2	VCO/6
0	1	0	VCO/2	VCO/4	VCO/4
0	1	1	VCO/2	VCO/4	VCO/6
1	0	0	VCO/4	VCO/2	VCO/4
1	0	1	VCO/4	VCO/2	VCO/6
1	1	0	VCO/4	VCO/4	VCO/4
1	1	1	VCO/4	VCO/4	VCO/6

Table 2. Input Reference/Output Frequency Relationships (Internal Feedback Only)

INPUTS			OUTPUTS					
Div_Sela	Div_Selb	Div_Selc	Qa		Qb		Qc	
			Power_Dn=0	Power_Dn=1	Power_Dn=0	Power_Dn=1	Power_Dn=0	Power_Dn=1
0	0	0	4x	2x	4x	2x	2x	x
0	0	1	4x	2x	4x	2x	4/3x	2/3x
0	1	0	4x	2x	2x	x	2x	x
0	1	1	4x	2x	2x	x	4/3x	2/3x
1	0	0	2x	x	4x	2x	2x	x
1	0	1	2x	x	4x	2x	4/3x	2/3x
1	1	0	2x	x	2x	x	2x	x
1	1	1	2x	x	2x	x	4/3x	2/3x

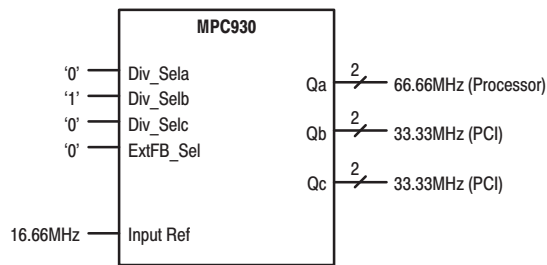


Figure 5. Dual Frequency Configuration

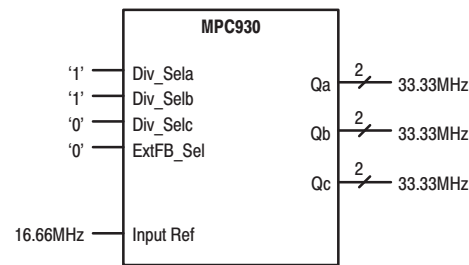


Figure 6. Single Frequency Configuration

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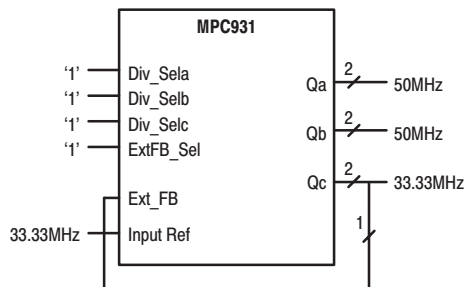


Figure 7. "Zero" Delay Fractional Multiplier

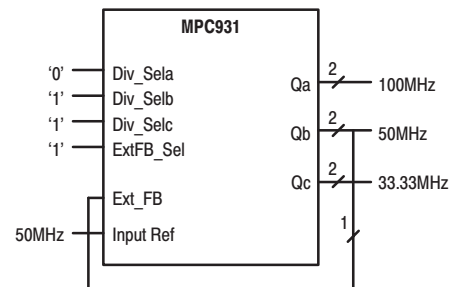


Figure 8. "Zero" Delay Fractional Divider

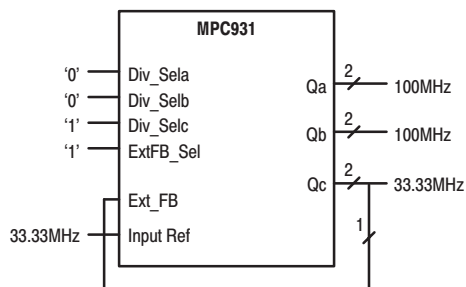


Figure 9. "Zero" Delay Multiply by 3 (50% Duty Cycle)

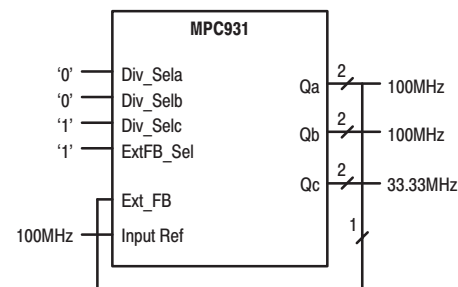


Figure 10. "Zero" Delay Divide by 3 (50% Duty Cycle)

Using the MPC930/931 as a Zero Delay Buffer

The external feedback option of the MPC930/931 clock driver allows for its use as a zero delay buffer. By using one of the outputs as a feedback to the PLL the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The Tpd of the device is specified in the specification tables. For zero delay buffer applications, the MPC931 is recommended over the MPC930. The MPC931 has been optimized and specified specifically for use as a zero delay buffer.

When used as a zero delay buffer the MPC930/931 will likely be in a nested clock tree application. For these applications the MPC931 offers a LVPECL clock input as a PLL reference. This allows the user to use LVPECL as the primary clock dis-

tribution device to take advantage of its far superior skew performance. The MPC931 then can lock onto the LVPECL reference and translate with near zero delay to low skew LVCMOS outputs. Clock trees implemented in this fashion will show significantly tighter skews than trees developed from CMOS fan-out buffers.

To minimize part-to-part skew the external feedback option again should be used. The PLL in the MPC931 decouples the delay of the device from the propagation delay variations of the internal gates. From the specification table one sees a Tpd variation of only ± 150 ps, thus for multiple devices under identical configurations the part-to-part skew will be around 850ps (300ps for Tpd variation plus 300ps output-to-output skew plus 250ps jitter). For devices that are configured differently

the differences between the nominal delays must also be accounted for.

When using the MPC931 as a zero delay buffer there is more information which can help minimize the overall timing uncertainty. To fully minimize the specified uncertainty, it is crucial that the relative position of the outputs be known. It is recommended that if all of the outputs are going to be used that the Qc0 output be used as the feedback reference. The Qc0 output lies in the middle of the other outputs with respect to output skew. Therefore it can be assumed that the output to output skew of the device is $\pm 150\text{ps}$ with respect to output Qc0.

There will be some cases where only a subset of the outputs of the MPC931 are required. There is significantly tighter skew performance between outputs on a common bank (i.e., Qa0 to Qa1). The skews between these common bank outputs are outlined in the table below. In general the skews between outputs on a given bank is about a third of the skew between all banks, reducing the skew to a value of 100ps.

Table 3. Within-Bank Skews

Outputs	Relative Skews
Qa0 $\rightarrow$ Qa1	+35ps, $\pm 50\text{ps}$
Qb0 $\rightarrow$ Qb1	-30ps, $\pm 50\text{ps}$
Qc0 $\rightarrow$ Qc1	20ps, $\pm 50\text{ps}$

Jitter Performance of the MPC930/931

With the clock rates of today's digital systems continuing to increase more emphasis is being placed on clock distribution design and management. Among the issues being addressed is system clock jitter and how that affects the overall system timing budget. The MPC930/931 was designed to minimize clock jitter by employing a differential bipolar PLL as well as incorporating numerous power and ground pins in the design. The following few paragraphs will outline the jitter performance of the MPC930/931, illustrate the measurement limitations and provide guidelines to minimize the jitter of the device.

The most commonly specified jitter parameter is cycle-to-cycle jitter. Unfortunately with today's high performance measurement equipment there is no way to measure this parameter for jitter performance in the class demonstrated by the MPC930/931. As a result different methods are used which approximate cycle-to-cycle jitter. The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak-to-peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. If this is not the case the measurement inaccuracy will add significantly to the measured jitter. The oscilloscope cannot collect adjacent pulses, rather it collects data from a very large sample of pulses. It is safe to assume that collecting pulse information in this mode will produce jitter values somewhat larger than if consecutive cycles were measured, therefore, this measurement will represent an upper bound of cycle-to-cycle jitter. Most likely, this is a conservative estimate of the cycle-to-cycle jitter.

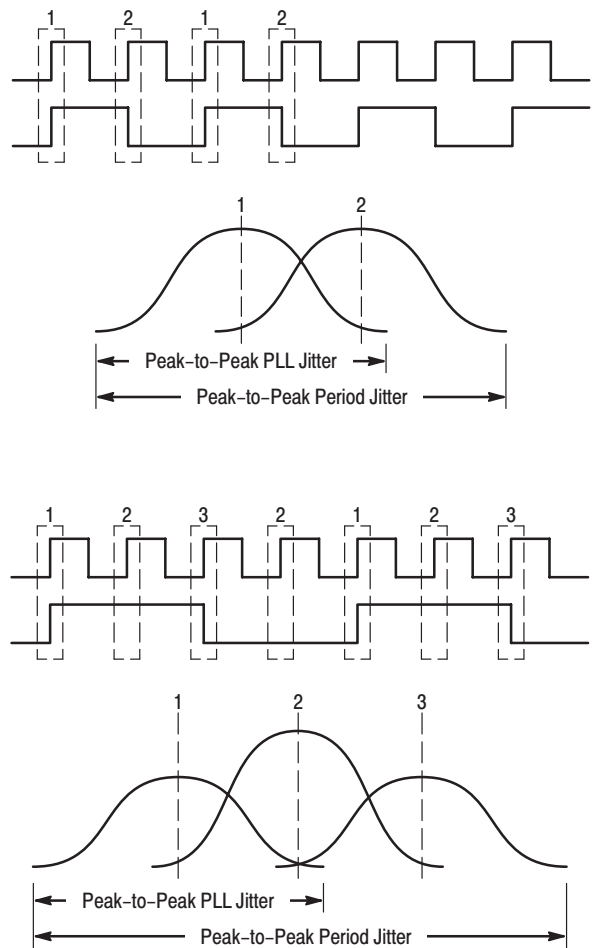


Figure 11. PLL Jitter and Edge Displacement

There are two sources of jitter in a PLL based clock driver, the commonly known random jitter of the PLL and the less intuitive jitter caused by synchronous, different frequency outputs switching. For the case where all of the outputs are switching at the same frequency the total jitter is exactly equal to the PLL jitter. In a device, like the MPC930/931, where a number of the outputs can be switching synchronously but at different frequencies a "multi-modal" jitter distribution can be seen on the highest frequency outputs. Because the output being monitored is affected by the activity on the other outputs it is important to consider what is happening on those other outputs. From Figure 11, one can see for each rising edge on the higher frequency signal the activity on the lower frequency signal is not constant. The activity on the other outputs tends to alter the internal thresholds of the device such that the placement of the edge being monitored is displaced in time. Because the signals are synchronous the relationship is periodic and the resulting jitter is a compilation of the PLL jitter superimposed on the displaced edges. When histograms are plotted the jitter looks like a "multi-modal" distribution as pictured in Figure 11 on page 56. Depending on the size of the PLL jitter and the relative displacement of the edges the "multi-modal" distribution will appear truly "multi-modal" or simply like a "fat" Gaussian distribution. Again note that in the case where all the

outputs are switching at the same frequency there is no edge displacement and the jitter is reduced to that of the PLL.

Figure 12 graphically represents the PLL jitter of the MPC930/931. The data was taken for several different output configurations. Because of the relatively few outputs on the MPC930/931, the multimodal distribution is of a second order affect on the 930/931 and can be ignored. As one can see in the figure the PLL jitter is much less dependent on output configuration than on internal VCO frequency. However, for a given VCO frequency, a lower output frequency produces more jitter.

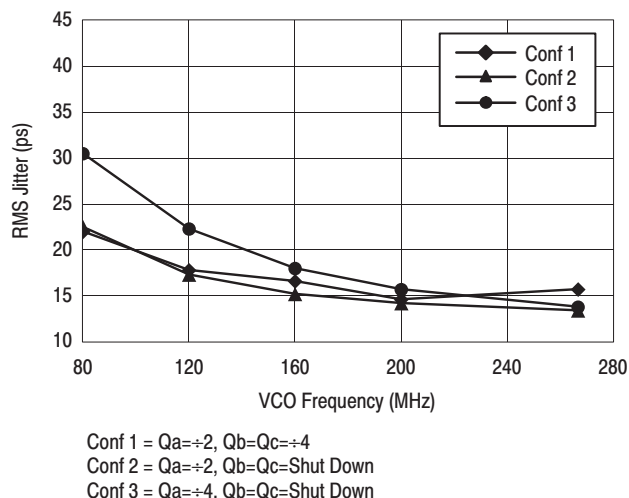


Figure 12. RMS Jitter versus VCO Frequency
(Qa0 Output)

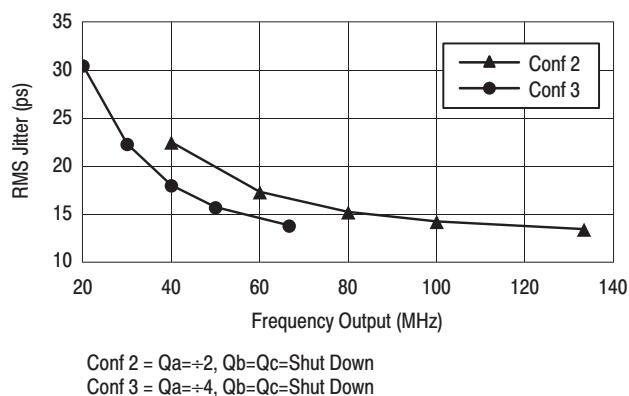


Figure 13. RMS Jitter versus Output Frequency
(Qa0 Output)

Finally from the data there are some general guidelines that, if followed, will minimize the output jitter of the device. First and foremost always configure the device such that the VCO runs as fast as possible. This is by far the most critical parameter in minimizing jitter. Second keep the reference frequency as high as possible. More frequent updates at the phase detector will help to reduce jitter. Note that if there is a tradeoff between higher reference frequencies and higher VCO frequency always chose the higher VCO frequency to minimize jitter. The

third guideline is to try to shut down outputs that are unused. Minimizing the number of switching outputs will minimize output jitter.

Power Supply Filtering

The MPC930/931 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC930/931 provides separate power supplies for the output buffers (V_{CCO}) and the internal PLL (PLL_VCC) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the PLL_VCC pin for the MPC930/931.

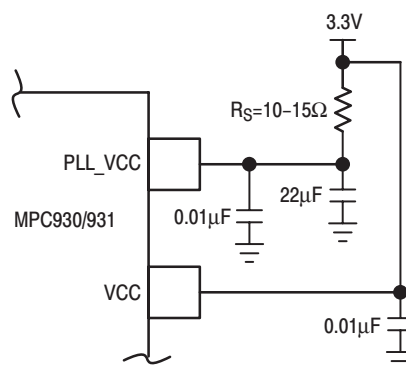


Figure 14. Power Supply Filter

Figure 14 illustrates a typical power supply filter scheme. The MPC930/931 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the PLL_VCC pin of the MPC930/931. From the data sheet the I_{PLL_VCC} current (the current sourced through the PLL_VCC pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the PLL_VCC pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 14 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC930/931 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter

schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the Power Management Features of the MPC930/931

The MPC930/931 clock driver offers two different features that designers can take advantage of for managing power dissipation in their designs. The first feature allows the user to turn off outputs which drive portions of the system which may go idle in a sleep mode. The Shut_Dn pins allow for three different combinations of output shut down schemes. The schemes are summarized in the function tables in the data sheet. The MPC930/931 synchronizes the shut down signals internal to the chip and applies them in a manner which eliminates the possibility of creating runt pulse on the outputs. The device waits for the output to go into the "LOW" state prior to disabling. When the outputs are re-enabled the device waits and re-enables the output such that the transition is synchronous and in the proper phase relationship to the outputs which remained active.

The Power_Dn pin offers another means of implementing power management schemes into a design. To use this feature the device must be set up in its normal operating mode with the Power_Dn pin "LOW", in addition the user must use the internal feedback option. If the external feedback option were used the output frequency reduction would change the feedback frequency and the PLL will lose lock. When the Power_Dn pin is driven "HIGH" the MPC930/931 synchronizes the signal to the internal clock and then seamlessly reduces the frequency of the outputs by one half. The Power_Dn signal is synchronized to the slowest internal VCO clock. It waits until both VCO clocks are in the "LOW" state and then switches from the nominal speed VCO clock to the half speed VCO clock. This will in turn cause the current output pulse to stretch to reflect the reduction in output frequency. When the Power_Dn pin is brought back "LOW" the device will again wait until both of the VCO clocks are "LOW" and then switch to the nominal VCO clock. This will cause the current output pulses, and all successive pulses, to shrink to match the higher output frequency. Both the power up and power down features are illustrated in the timing diagrams of in this data sheet.

Timing diagrams for both of the power management features are shown in Figure 3 and Figure 4 on page 51.

Using the On-Board Crystal Oscillator

The MPC930 features an on-board crystal oscillator to allow for seed clock generation as well as final distribution. The on-board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC930/931 as possible to avoid any board level parasitics. To facilitate co-

location surface mount crystals are recommended, but not required.

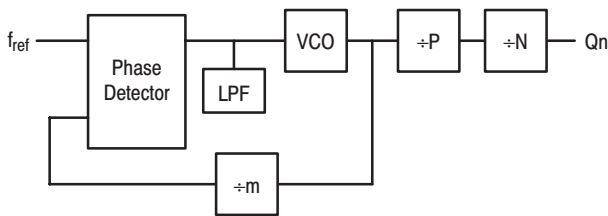
The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on-board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most off the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC930 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

Table 4. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω Max
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

The MPC930 is a clock driver which was designed to generate outputs with programmable frequency relationships and not a synthesizer with a fixed input frequency. As a result the crystal input frequency is a function of the desired output frequency. For a design which utilizes the external feedback to the PLL the selection of the crystal frequency is straight forward; simply chose a crystal which is equal in frequency to the fed back signal. To determine the crystal required to produce the desired output frequency for an application which utilizes internal feedback the block diagram of Figure 15 should be used. The P and the M values for the MPC930/931 are also included in Figure 15. The M values can be found in the configuration tables included in this applications section.



$$f_{ref} = \frac{f_{VCO}}{m}, \quad f_{VCO} = f_{Qn} \cdot N \cdot P$$

$$\therefore f_{ref} = \frac{f_{Qn} \cdot N \cdot P}{m}$$

$$m = 8$$

$$P = 1 \text{ (Power\_Dn='0')}, 2 \text{ (Power\_Dn='1')}$$

Figure 15. PLL Block Diagram

For the MPC930 clock driver, the following will provide an example of how to determine the crystal frequency required for a given design.

Given:

$$Qa = 66.6\text{MHz}$$

$$Qb = 33.3\text{MHz}$$

$$Qc = 22.2\text{MHz}$$

$$\text{Power\_Dn} = '0'$$

$$f_{ref} = \frac{f_{Qn} \cdot N \cdot P}{m}$$

From Table 4

$$f_{Qc} = VCO/6 \text{ then } N = 6$$

From Figure 15

$$m = 8 \text{ and } P = 1$$

$$f_{ref} = \frac{22.22 \cdot 6 \cdot 1}{8} = 16.66\text{MHz}$$

Driving Transmission Lines

The MPC930/931 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current

and thus only a single terminated line can be driven by each output of the MPC930/931 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 16 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC930/931 clock driver is effectively doubled due to its capability to drive multiple lines.

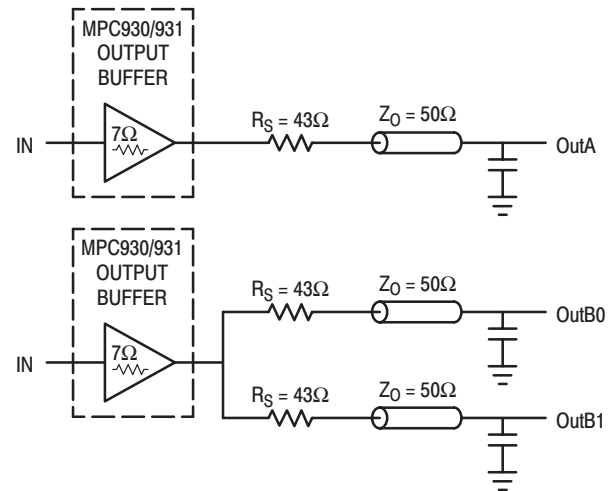


Figure 16. Single versus Dual Transmission Lines

The waveform plots of Figure 17 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC930/931 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC930/931. The output waveform in Figure 17 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S \left(Z_o / (R_s + R_o + Z_o) \right)$$

$$Z_o = 50\Omega \parallel 50\Omega$$

$$R_s = 43\Omega \parallel 43\Omega$$

$$R_o = 7\Omega$$

$$V_L = 3.0 \left(25 / (21.5 + 7 + 25) \right) = 3.0 \left(25 / 53.5 \right) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

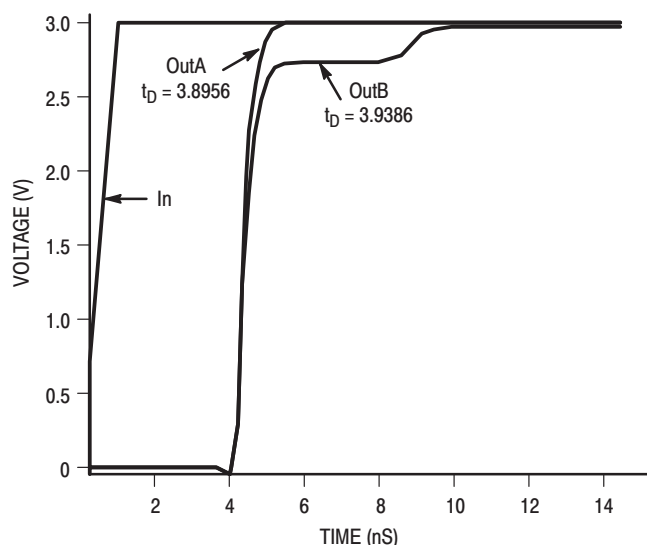


Figure 17. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better

match the impedances when driving multiple lines the situation in Figure 18 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

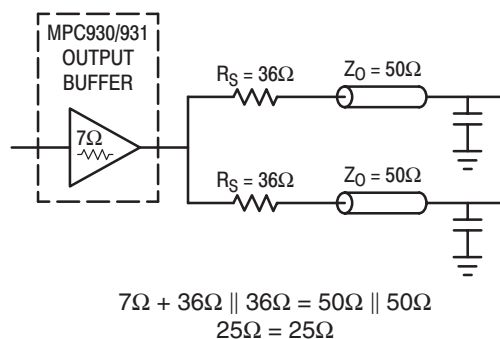


Figure 18. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

2.5V and 3.3V CMOS PLL Clock Generator and Driver

The MPC9315 is a 2.5V and 3.3V compatible, PLL based clock generator designed for low-skew clock distribution in low-voltage mid-range to high-performance telecom, networking and computing applications. The MPC9315 offers 8 low-skew outputs and 2 selectable inputs for clock redundancy. The outputs are configurable and support 1:1, 2:1, 4:1, 1:2 and 1:4 output to input frequency ratios. In addition, a selectable output 180° phase control supports advanced clocking schemes with inverted clock signals. The MPC9315 is specified for the extended temperature range of -40 to +85°C.

Features

- Configurable 8 outputs LVCMOS PLL clock generator
- Compatible to various microprocessor such as PowerQuicc I and II
- Wide range output clock frequency of 18.75 to 160 MHz
- 2.5V and 3.3V CMOS compatible
- Designed for mid-range to high-performance telecom, networking and computer applications
- Fully integrated PLL supports spread spectrum clocking
- Supports applications requiring clock redundancy
- Max. output skew of 120 ps (80 ps within one bank)
- Selectable output configurations (1:1, 2:1, 4:1, 1:2, 1:4 frequency ratios)
- 2 selectable LVCMOS clock inputs
- External PLL feedback path and selectable feedback configuration
- Tristable outputs
- 32 ld LQFP package
- Ambient operating temperature range of -40 to +85°C

Functional Description

The MPC9315 utilizes PLL technology to frequency and phase lock its outputs onto an input reference clock. Normal operation requires a connection of one of the device outputs to the selected feedback (FB0 or FB1) input to close the PLL feedback path. The reference clock frequency and the output divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. With available output dividers of divide-by-1, divide-by-2 and divide-by-4 the internal VCO of the MPC9315 is running at either 1x, 2x or 4x of the reference clock frequency. The frequency of the QA, QB, QC output groups is either the equal, one half or one fourth of the selected VCO frequency and can be configured for each output bank using the FSELA, FSELB and FSELC pins, respectively. The available output to input frequency ratios are 4:1, 2:1, 1:1, 1:2 and 1:4. The REF_SEL pin selects one of the two available LVCMOS compatible reference input (CLK0 and CLK1) supporting clock redundant applications. The selectable feedback input pin allows the user to select different feedback configurations and input to output frequency ratios. The MPC9315 also provides a static test mode when the PLL supply pin (V_{CCA}) is pulled to logic low state (GND). In test mode, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The test mode is intended for system diagnostics, test and debug purpose. This test mode is fully static and the minimum clock frequency specification does not apply. The outputs can be disabled by deasserting the $\overline{OE}$ pin (logic high state). In PLL mode, deasserting $\overline{OE}$ causes the PLL to lose lock due to no feedback signal presence at FB0 or FB1. Asserting $\overline{OE}$ will enable the outputs and close the phase locked loop, also enabling the PLL to recover to normal operation. The MPC9315 is fully 2.5V and 3.3V compatible and requires no external loop filter components. All inputs accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9315 outputs can drive one or two traces giving the devices an effective fanout of 1:18. The device is packaged in a 7x7 mm² 32-lead LQFP package.

The fully integrated PLL of the MPC9315 allows the low skew outputs to lock onto a clock input and distribute it with essentially zero propagation delay to multiple components on the board. In zero-delay buffer mode, the PLL minimizes phase offset between the outputs and the reference signal.

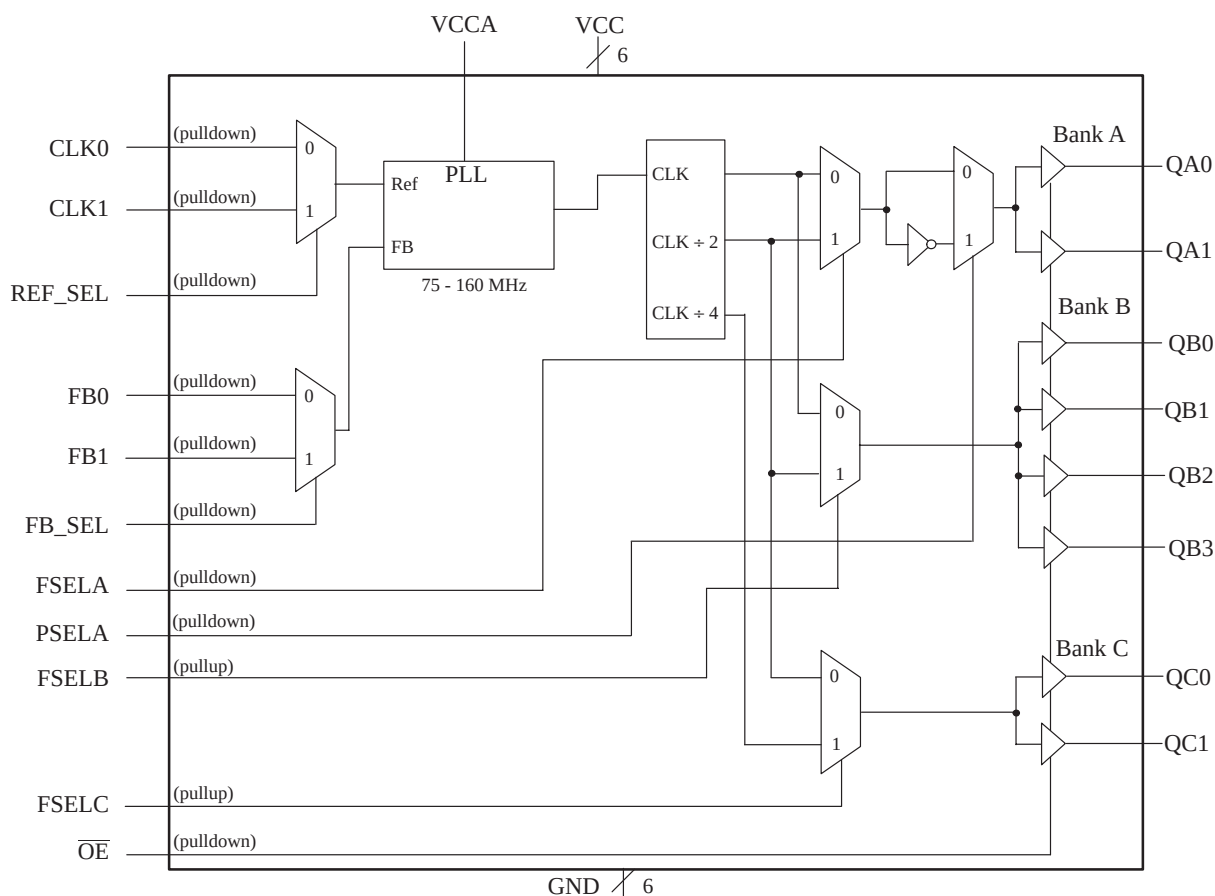
MPC9315

**LOW VOLTAGE
2.5V AND 3.3V PLL
CLOCK GENERATOR**



FA SUFFIX
LQFP PACKAGE
CASE 873A-02

2



The MPC9315 requires an external RC filter for the analog power supply pin VCCA. Please see application section for details.

Figure 1. MPC9315 Logic Diagram

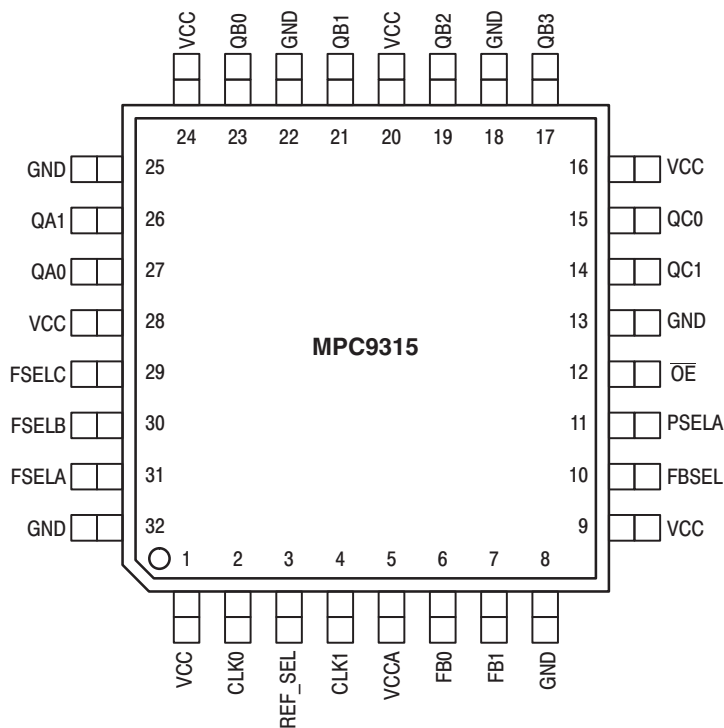


Figure 2. Pinout: 32-Lead Package Pinout (Top View)

PIN CONFIGURATION

Pin	I/O	Type	Function
CLK0	Input	LVC MOS	Reference clock input
CLK1	Input	LVC MOS	Alternative clock input
FB0	Input	LVC MOS	PLL feedback input
FB1	Input	LVC MOS	Alternative feedback input
REF_SEL	Input	LVC MOS	Selects clock input reference clock input, default low (pull-down)
FB_SEL	Input	LVC MOS	Selects PLL feedback clock input, default low (pull-down)
FSELA	Input	LVC MOS	Selects divider ratio of bank A outputs, default low (pull-down)
FSELB	Input	LVC MOS	Selects divider ratio of bank B outputs, default low (pull-up)
FSELC	Input	LVC MOS	Selects divider ratio of bank C outputs, default low (pull-up)
PSELA	Input	LVC MOS	Selects phase of bank A outputs
QA0, QA1	Output	LVC MOS	Bank A outputs
QB0 to QB3	Output	LVC MOS	Bank B outputs
QC0, QC1	Output	LVC MOS	Bank C outputs
$\overline{OE}$	Input	LVC MOS	Output tristate
VCCA		Supply	Analog (PLL) positive supply voltage. Requires external RC filter
VCC		Supply	Digital positive supply voltage
GND		Ground	Digital negative supply voltage (ground)

FUNCTION TABLE

Control	Default	0	1
REF_SEL	0	CLK0	CLK1
FB_SEL	0	FB0	FB1
FSELA	0	QAx = VCO clock frequency	QA0, QA1 = VCO clock frequency $\div$ 2
FSELB	1	QBx = VCO clock frequency	QB0 - QB3 = VCO clock frequency $\div$ 2
FSELC	1	QCx = VCO clock frequency $\div$ 2	QC0, QC1 = VCO clock frequency $\div$ 4
PSELA	0	0° (QA0, QA1 non-inverted)	180° (QA0, QA1 inverted)
VCCA	none	VCCA = GND, PLL off and bypassed for static test and diagnosis	VCCA = 3.3 or 2.5V, PLL enabled
MR	0	Normal operation	Reset (VCO clamped to min. range)
$\overline{OE}$	0	Outputs enabled	Outputs disabled (tristate), open PLL loop

ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	4.6	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} +0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} +0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage temperature	-55	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output Termination Voltage		V _{CC} $\div$ 2		V	
MM	ESD (Machine Model)	200			V	
HBM	ESD (Human Body Model)	2000			V	
LU	Latch-Up	200			mA	
C _{PD}	Power Dissipation Capacitance		10		pF	Per output
C _{IN}			4.0		pF	Inputs

DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input Low Voltage			0.8	V	LVC MOS
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -24 \text{ mA}^a$
V_{OL}	Output Low Voltage			0.55 0.30	V V	$I_{OL} = 24 \text{ mA}^a$ $I_{OL} = 12 \text{ mA}$
Z_{OUT}	Output Impedance		14 - 17		Ω	
I_{IN}	Input Current ^b			± 200	μA	$V_{IN} = V_{CC}$ or GND
I_{CCA}	Maximum PLL Supply Current		3.5	7.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins

- a. The MPC9315 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines.
- b. Inputs have pull-up or pull-down resistors affecting the input current.

AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency			160	MHz	PLL locked
	+1 feedback	100 ^c		80	MHz	PLL locked
	+2 feedback	37.50		40	MHz	PLL locked
	+4 feedback	18.75				PLL locked
	PLL bypass mode	0		TBD	MHz	$V_{CCA} = \text{GND}$
f_{VCO}	VCO Lock Range	75 ^c		160	MHz	
f_{MAX}	Maximum Output Frequency	75		160	MHz	
	+1 output	37.50		80	MHz	
	+2 output	18.75		40	MHz	
	+4 output					
f_{refDC}	Reference Input Duty Cycle	25		75	%	
t_r, t_f	CLK0, CLK1 Input Rise/Fall Time			1.0	ns	0.8 to 2.0V
$t_{(\phi)}$	Propagation Delay CLK0 or CLK1 to FB (Static Phase Offset)	-150		+150	ps	PLL locked
$t_{SK(\phi)}$	Output-to-Output Skew Within one bank			80	ps	
	Any output			120	ps	
DC	Output Duty Cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
BW	PLL closed loop bandwidth				MHz	
	+1 feedback		TBD		MHz	
	+2 feedback		2.0 - 20		MHz	
	+4 feedback		0.6 - 6.0		MHz	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter (1 σ)		10	22	ps	RMS value
$t_{JIT(PER)}$	Period Jitter (1 σ)		8.0	15	ps	RMS value
$t_{JIT(\phi)}$	I/O Phase Jitter (1 σ)		8.0 - 25 ^b	TBD	ps	RMS value
t_{LOCK}	Maximum PLL Lock Time			1.0	ms	

- a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
- b. I/O jitter depends on VCO frequency. Please see application section for I/O jitter versus VCO frequency characteristics.
- c. The VCO range in +1 feedback configuration (e.g. QAx connected to FBx and FSELA = 0) is limited to $100 \leq f_{VCO} \leq 160 \text{ MHz}$. Please see next revision of the MPC9315 for improved VCO frequency range.

DC CHARACTERISTICS ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{IH}	Input High Voltage	1.7		V _{CC} + 0.3	V	LVC MOS
V _{IL}	Input Low Voltage			0.7	V	LVC MOS
V _{OH}	Output High Voltage	1.8			V	I _{OH} = -15 mA ^a
V _{OL}	Output Low Voltage			0.6	V	I _{OL} = 15 mA
Z _{OUT}	Output Impedance		17 - 20		Ω	
I _{IN}	Input Current ^b			±200	μA	V _{IN} = V _{CC} or GND
I _{CCA}	Maximum PLL Supply Current		2.0	5.0	mA	V _{CCA} Pin
I _{CCO}	Maximum Quiescent Supply Current			1.0	mA	All V _{CC} Pins

- a. The MPC9315 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.
- b. Inputs have pull-up or pull-down resistors affecting the input current.

AC CHARACTERISTICS ($V_{GG} = 2.5V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f _{ref}	Input Frequency ^c +2 feedback +4 feedback PLL bypass mode	37.50 18.75 0		80 40 TBD	MHz MHz MHz	PLL locked PLL locked V _{CCA} = GND
f _{VCO}	VCO Lock Range	75 ^c		160 ^c	MHz	
f _{MAX}	Maximum Output Frequency +1 output +2 output +4 output	75 37.50 18.75		160 80 50	MHz MHz MHz	
f _{refDC}	Reference Input Duty Cycle	25		75	%	
t _r , t _f	CLK0, CLK1 Input Rise/Fall Time			1.0	ns	0.7 to 1.7V
t _(∅)	Propagation Delay CLK0 or CLK1 to FB (Static Phase Offset)	−150		+150	ps	PLL locked
t _{SK(∅)}	Output-to-Output Skew Within one bank Any output			80 120	ps ps	
DC	Output Duty Cycle	45	50	55	%	
t _r , t _f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
t _{PLZ} , HZ	Output Disable Time			12	ns	
t _{PZL} , LZ	Output Enable Time			12	ns	
BW	PLL closed loop bandwidth +2 feedback +4 feedback		1.0 – 10 0.4 – 3.0		MHz MHz	
t _{JIT(CC)}	Cycle-to-Cycle Jitter (1σ)		10	22	ps	RMS value
t _{JIT(PER)}	Period Jitter (1σ)		8.0	15	ps	RMS value
t _{JIT(∅)}	I/O Phase Jitter (1σ)		10 – 25 ^b	TBD	ps	RMS value
t _{LOCK}	Maximum PLL Lock Time			1.0	ms	

- a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
- b. I/O jitter depends on VCO frequency. Please see application section for I/O jitter versus VCO frequency characteristics.
- c. ± 1 feedback is not available for $V_{CC} = 2.5V$ operation. Please see next revision of the MPC9315 for the ± 1 feedback option at 2.5V supply.

APPLICATIONS INFORMATION

Programming the MPC9315

The PLL of the MPC9315 supports output clock frequencies from 18.75 to 160 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency range between 75 and 160 MHz for stable and optimal operation. The FSELA, FSELB, FSELC pins select the desired output clock frequencies. Possible frequency ratios of the reference clock

input to the outputs are 1:1, 1:2, 1:4 as well as 2:1 and 4:1, Table 1, Table 2 and Table 3 illustrate the various output configurations and frequency ratios supported by the MPC9315. PSELA controls the output phase of the QA0 and QA1 outputs, allowing the user to generate inverted clock signals synchronous to non-inverted clock signals. See also "Example Configurations for the MPC9315" on page 8 for further reference.

2

Table 1: Output Frequency Relationship for QA0 connected to FB0^a

Inputs			Outputs		
FSELA	FSELB	FSELC	QA0, QA1	QB0-QB3	QC0, QC1
0	0	0	CLK	CLK	CLK ÷ 2
0	0	1	CLK	CLK	CLK ÷ 4
0	1	0	CLK	CLK ÷ 2	CLK ÷ 2
0	1	1	CLK	CLK ÷ 2	CLK ÷ 4
1	0	0	CLK	2 * CLK	CLK
1	0	1	CLK	2 * CLK	CLK ÷ 2
1	1	0	CLK	CLK	CLK
1	1	1	CLK	CLK	CLK ÷ 2

a. Output frequency relationship with respect to input reference frequency CLK.

Table 2: Output Frequency Relationship for QB0 connected to FB0^a

Inputs			Outputs		
FSELA	FSELB	FSELC	QA0, QA1	QB0-QB3	QC0, QC1
0	0	0	CLK	CLK	CLK ÷ 2
0	0	1	CLK	CLK	CLK ÷ 4
0	1	0	2 * CLK	CLK	CLK
0	1	1	2 * CLK	CLK	CLK ÷ 2
1	0	0	CLK ÷ 2	CLK	CLK ÷ 2
1	0	1	CLK ÷ 2	CLK	CLK ÷ 4
1	1	0	CLK	CLK	CLK
1	1	1	CLK	CLK	CLK ÷ 2

a. Output frequency relationship with respect to input reference frequency CLK.

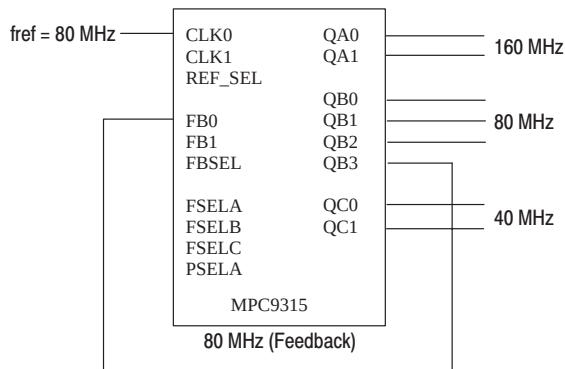
Table 3: Output Frequency Relationship for QC0 connected to FB0^a

Inputs			Outputs		
FSELA	FSELB	FSELC	QA0, QA1	QB0-QB3	QC0, QC1
0	0	0	2 * CLK	2 * CLK	CLK
0	0	1	4 * CLK	4 * CLK	CLK
0	1	0	2 * CLK	CLK	CLK
0	1	1	4 * CLK	2 * CLK	CLK
1	0	0	CLK	2 * CLK	CLK
1	0	1	2 * CLK	4 * CLK	CLK
1	1	0	CLK	CLK	CLK
1	1	1	2 * CLK	2 * CLK	CLK

a. Output frequency relationship with respect to input reference frequency CLK.

Example Configurations for the MPC9315

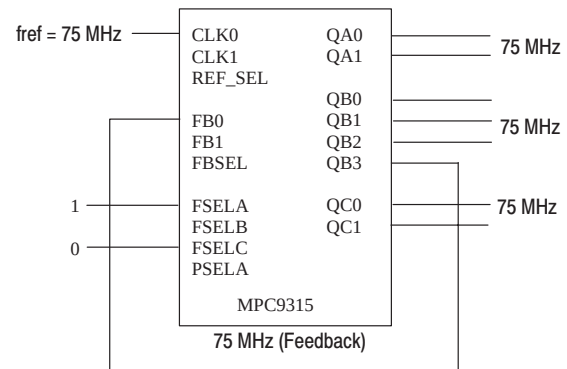
Figure 3. MPC9315 Default Configuration



MPC9315 default configuration (feedback of QB3 = 100 MHz). All control pins are left open.

Frequency range	Min	Max
Input	37.50 MHz	80 MHz
QA outputs	75.00 MHz	160 MHz
QB outputs	37.50 MHz	80 MHz
QC outputs	18.75 MHz	40 MHz

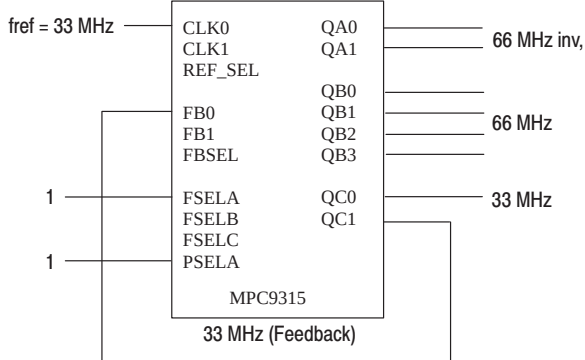
Figure 4. MPC9315 Zero Delay Buffer Configuration



MPC9315 1:1 frequency configuration (feedback of QB3 = 75 MHz). FSELB = H, FSEL = L. All other control pins are left open.

Frequency range	Min	Max
Input	37.50 MHz	80 MHz
QA outputs	37.50 MHz	80 MHz
QB outputs	37.50 MHz	80 MHz
QC outputs	37.50 MHz	80 MHz

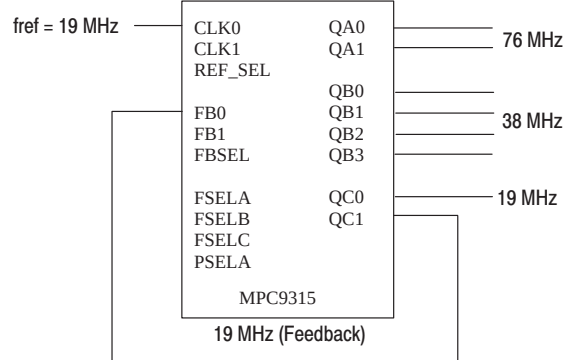
Figure 5. MPC9315 180° Phase Inversion Configuration



MPC9315 1:1 frequency configuration (feedback of QC1 = 33 MHz). FSELB = PSELB = H. All other control pins are left open.

Frequency range	Min	Max
Input	18.75 MHz	40 MHz
QA outputs	37.50 MHz	80 MHz
QB outputs	37.50 MHz	80 MHz
QC outputs	18.75 MHz	40 MHz

Figure 6. MPC9315 x4 Multiplier Configuration



MPC9315 4x, 2x, 1x frequency configuration (feedback of QC1 = 19 MHz). All control pins are left open.

Frequency range	Min	Max
Input	18.75 MHz	40 MHz
QA outputs	75.00 MHz	160 MHz
QB outputs	37.50 MHz	80 MHz
QC outputs	18.75 MHz	40 MHz

Using the MPC9315 in zero-delay applications

The external feedback option of the MPC9315 PLL allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge and virtually eliminates the propagation delay through the device.

The remaining insertion delay (skew error) of the MPC9315 in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset (SPO or t_{ϕ}), I/O jitter ($t_{JIT(\phi)}$), phase or long-term jitter), feedback path delay and the output-to-output skew ($t_{SK(O)}$ relative to the feedback output.

Calculation of part-to-part skew

The MPC9315 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs (TCLK or PCLK) of two or more MPC9315 are connected together, the maximum overall timing uncertainty from the common TCLK input to any output is:

$$t_{SK(PP)} = t_{\phi} + t_{SK(O)} + t_{PD, LINE(FB)} + t_{JIT(\phi)} \cdot CF$$

This maximum timing uncertainty consists of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

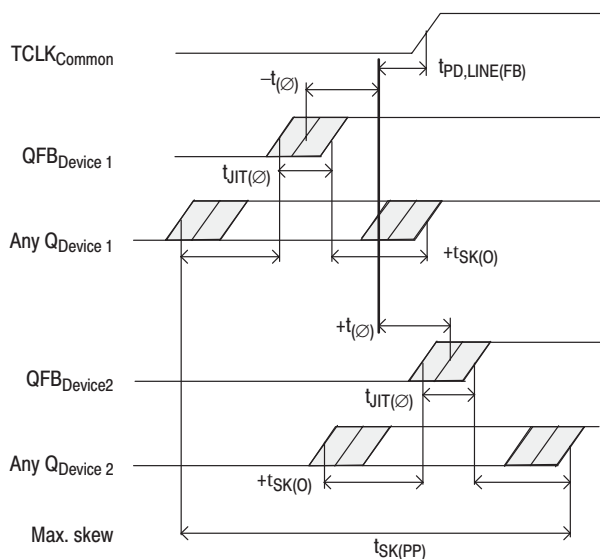


Figure 7. MPC9315 max. device-to-device skew

Due to the statistical nature of I/O jitter, a RMS value (1σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

Table 8: Confidence Factor CF

CF	Probability of clock edge within the distribution
$\pm 1\sigma$	0.68268948
$\pm 2\sigma$	0.95449988
$\pm 3\sigma$	0.99730007
$\pm 4\sigma$	0.99993663
$\pm 5\sigma$	0.99999943
$\pm 6\sigma$	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each

device. In the following example calculation a I/O jitter confidence factor of 99.7% ($\pm 3\sigma$) is assumed, resulting in a worst case timing uncertainty from input to any output of -300 ps to +300 ps relative to TCLK ($V_{CC}=3.3V$ and $f_{VCO} = 160$ MHz):

$$t_{SK(PP)} = [-150ps...150ps] + [-150ps...150ps] + [(10ps \cdot -3)...(10ps \cdot 3)] + t_{PD, LINE(FB)}$$

$$t_{SK(PP)} = [-300ps...300ps] + t_{PD, LINE(FB)}$$

Above equation uses the maximum I/O jitter number shown in the AC characteristic table for $V_{CC}=3.3V$ (10 ps RMS). I/O jitter is frequency dependant with a maximum at the lowest VCO frequency (160 MHz for the MPC9315). Applications using a higher VCO frequency exhibit less I/O jitter than the AC characteristic limit. The I/O jitter characteristics in Figure 8 and Figure 9 can be used to derive a smaller I/O jitter number at the specific VCO frequency, resulting in tighter timing limits in zero-delay mode and for part-to-part skew $t_{SK(PP)}$.

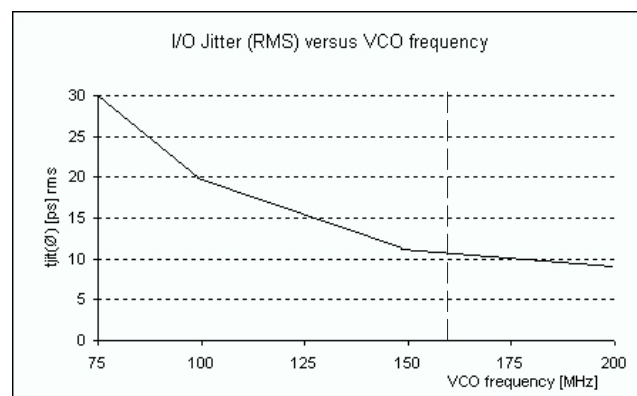


Figure 8. Max. I/O Jitter (RMS) versus frequency for $V_{CC}=2.5V$

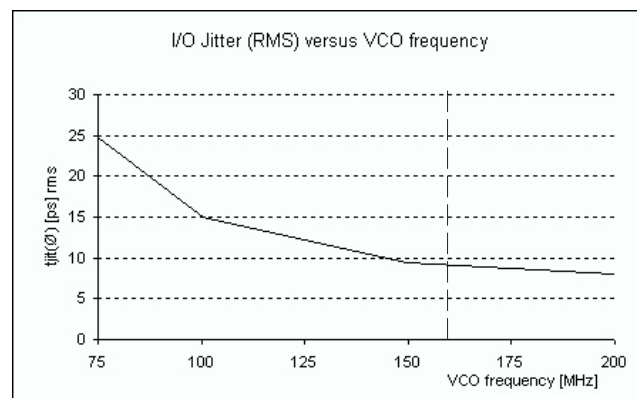


Figure 9. Max. I/O Jitter (RMS) versus frequency for $V_{CC}=3.3V$

Power Supply Filtering

The MPC9315 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9315 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize

noise on the power supplies, a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC9315. Figure 10 illustrates a typical power supply filter scheme. The MPC9315 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F . From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V ($V_{CC}=3.3V$ or $V_{CC}=2.5V$) must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 10 “ V_{CCA} Power Supply Filter” must have a resistance of 270 Ω ($V_{CC}=3.3V$) or 9-10 Ω ($V_{CC}=2.5V$) to meet the voltage drop criteria.

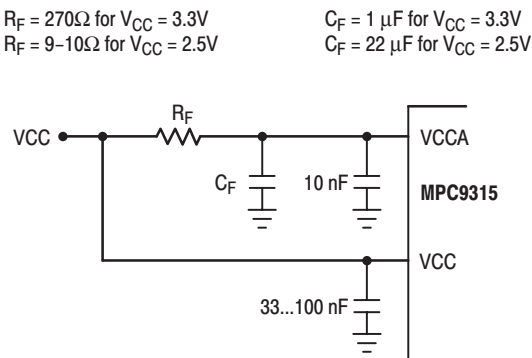


Figure 10. V_{CCA} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 10 “ V_{CCA} Power Supply Filter”, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9315 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC9315 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance

clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC}+2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9315 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 11 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9315 clock driver is effectively doubled due to its capability to drive multiple lines.

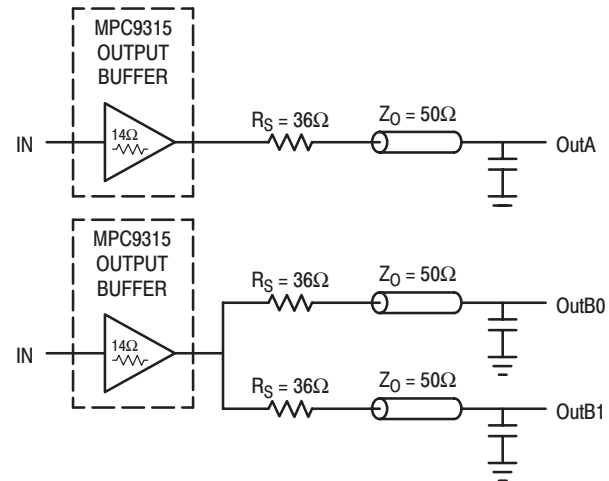


Figure 11. Single versus Dual Transmission Lines

The waveform plots in Figure 12 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9315 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9315. The output waveform in Figure 12 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned} V_L &= V_S (Z_0 \div (R_S + R_0 + Z_0)) \\ Z_0 &= 50\Omega \parallel 50\Omega \\ R_S &= 36\Omega \parallel 36\Omega \\ R_0 &= 14\Omega \\ V_L &= 3.0 (25 \div (18 + 17 + 25)) \\ &= 1.31V \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

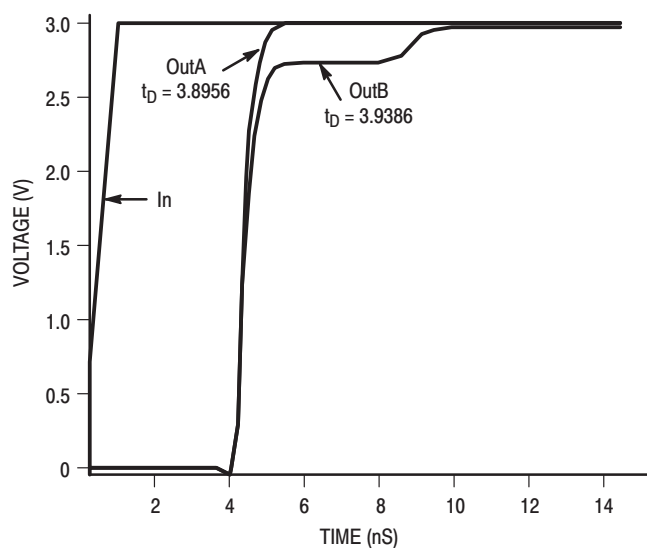


Figure 12. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be

uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 13 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

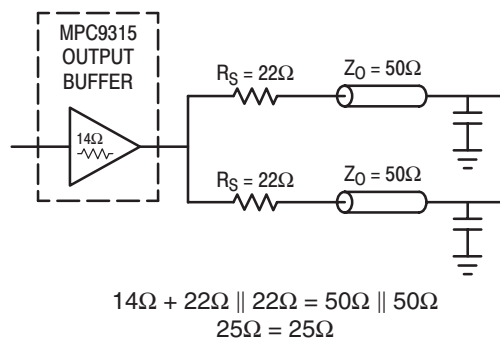


Figure 13. Optimized Dual Line Termination

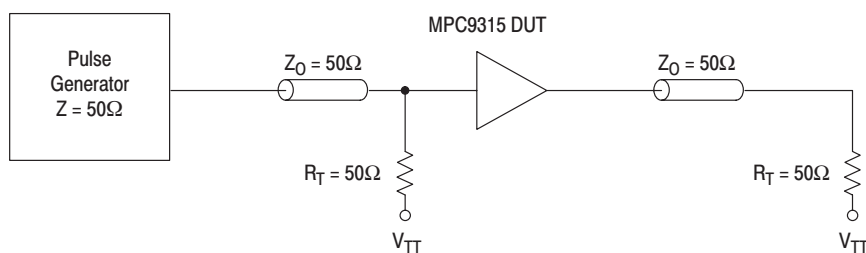


Figure 14. CLK0, CLK1 MPC9315 AC test reference

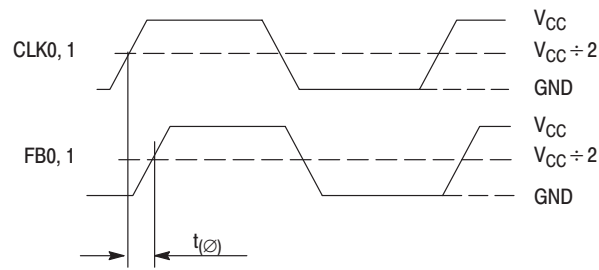
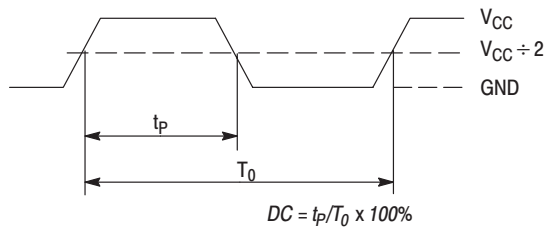
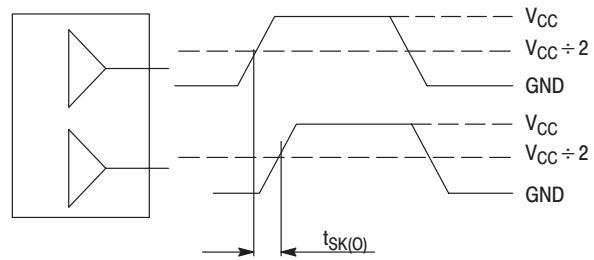


Figure 15. Propagation delay (t_{ϕ}), SPO) test reference



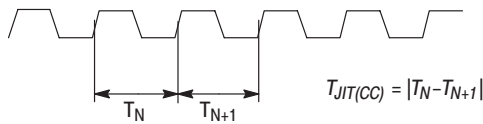
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 16. Output Duty Cycle (DC)



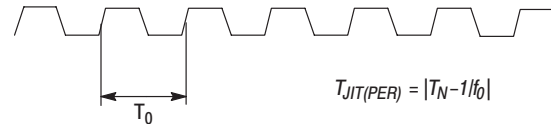
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 17. Output-to-output Skew $t_{SK(O)}$



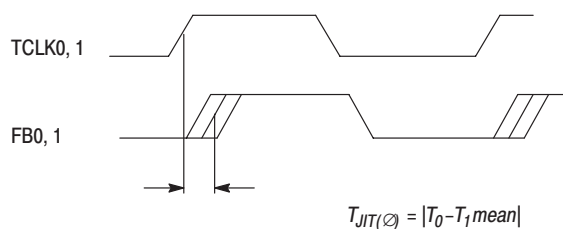
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 18. Cycle-to-cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 19. Period Jitter



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 20. I/O Jitter

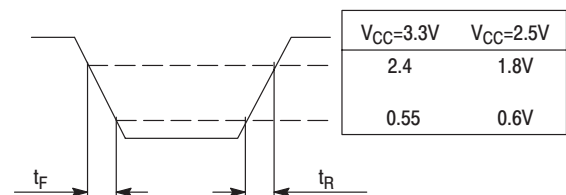


Figure 21. Output Transition Time Test Reference

Low Voltage PLL Clock Driver

The MPC932 is a 3.3 V compatible PLL based clock driver device targeted for zero delay applications. The device provides 6 outputs for driving clock loads plus a single dedicated PLL feedback clock output. The dedicated feedback output gives the user six choices of input multiplication factors: x1, x1.25, x1.5, x2, x2.5 and x3.

- 6 Low Skew Clock Outputs
- 1 Dedicated PLL Feedback Output
- Individual Output Enable Control
- Fully Integrated PLL
- Output Frequency Up to 120MHz
- 32-Lead TQFP Packaging
- 3.3V VCC
- ± 100 ps Cycle-to-Cycle Jitter

The MPC932 provides individual output enable control. The enables are synchronized to the internal clock such that upon assertion the shut down signals will hold the clocks LOW without generating a runt pulse on the outputs. The shut down pins provide a means of powering down certain portions of a system or a means of disabling outputs when the full compliment is not required for a specific design. The shut down pins will disable the outputs when driven LOW. A common shut down pin is provided to disable all of the outputs (except the feedback output) with a single control signal.

Two feedback select pins are provided to select the multiplication factor of the PLL. The MPC932 provides six multiplication factors: x1, x1.25, x1.5, x2, x2.5 and x3. In the x1.25 and x2.5 modes, the QFB output will not provide a 50% duty cycle. The phase detector of the MPC932 only monitors rising edges of its feedback signals, thus for this function a 50% duty cycle is not required. As the QFB signal can also be used to drive other clocks in a system it is important the user understand that the duty cycle will not be 50%. In the x1 and x1.5 modes the QFB output will produce 50% duty cycle signals.

The MPC932 provides two pins for use in system test and debug operations. The $\overline{MR}/OE$ input will force all of the outputs into a high impedance state to allow for back driving the outputs during system test. In addition the PLL_EN pin allows the user to bypass the PLL and drive the outputs directly through the Ref_CLK input. Note the Ref_CLK signal will be routed through the dividers so that it will take several transitions on the Ref_CLK input to create a transition on the outputs.

The MPC932 is fully 3.3 V compatible and requires no external loop filter components. All of the inputs are LVCMOS/LVTTL compatible and the outputs produce rail-to-rail 3.3V swings. For series terminated applications each output can drive two series terminated 50 Ω transmission lines. For parallel terminated lines the device can drive terminations of 50 Ω into VCC/2. The device is packaged in a 32-lead TQFP package to provide the optimum combination of performance, board density and cost.

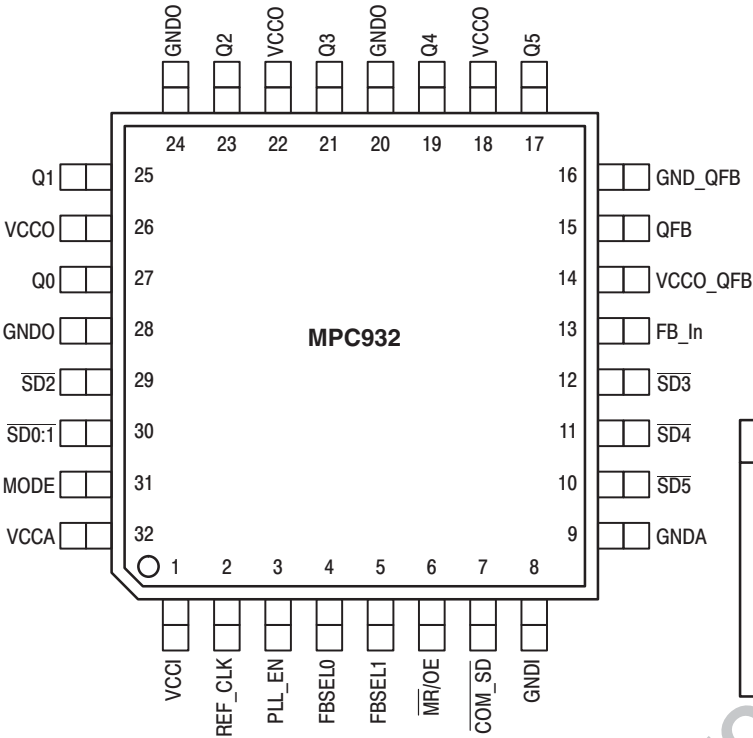
MPC932

**LOW VOLTAGE
PLL CLOCK DRIVER**



FA SUFFIX
TQFP PACKAGE
CASE 873A-02

Pinout: 32-Lead TQFP Package (Top View)

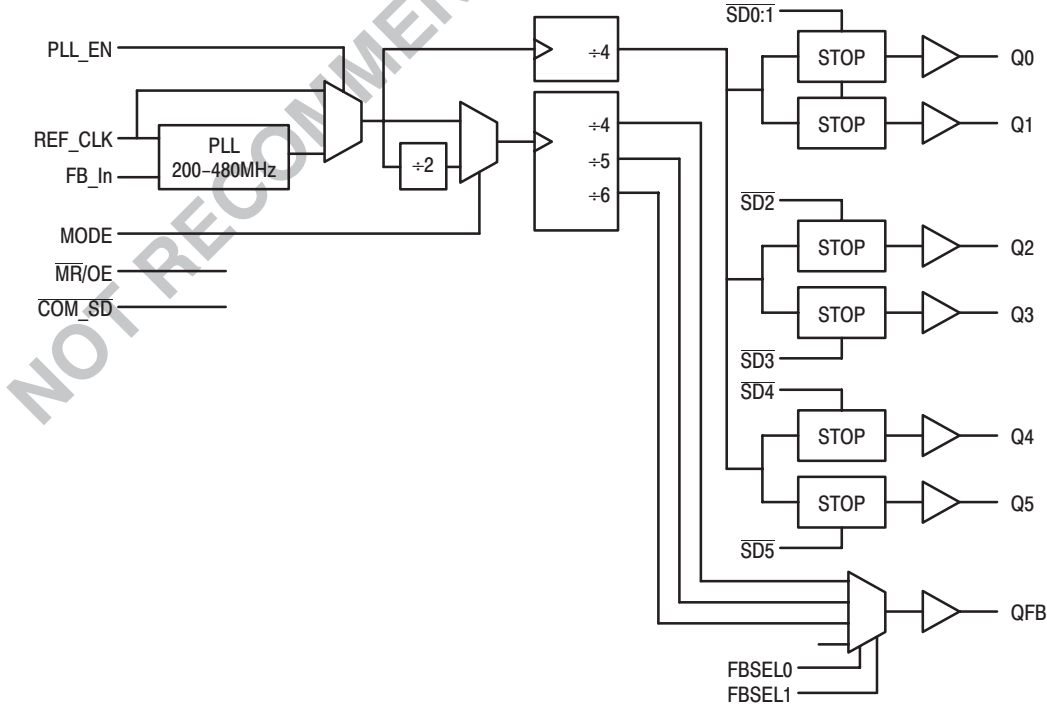


FUNCTION TABLES

SDn, COM_SD	Qn
0	Held LOW
1	Enabled
PLL_En	PLL Status
0	Test Mode
1	PLL Enabled
MR/OE	PLL Status
0	Disabled
1	Enabled

MODE	FBSEL1	FBSEL0	Qn	QFB
0	0	0	VCO/4	VCO/8
0	0	1	VCO/4	VCO/10
0	1	0	VCO/4	VCO/12
0	1	1	NA	NA
1	0	0	VCO/4	VCO/4
1	0	1	VCO/4	VCO/5
1	1	0	VCO/4	VCO/6
1	1	1	NA	NA

LOGIC DIAGRAM



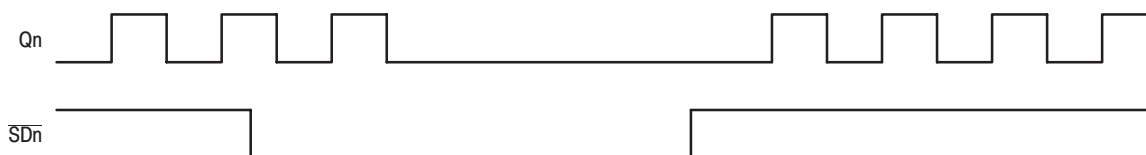


Figure 1. Timing Diagram

2

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	4.6	V
V_I	Input Voltage	-0.3	$V_{DD} + 0.3$	V
I_{IN}	Input Current		± 20	mA
T_{Stor}	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

PLL INPUT REFERENCE CHARACTERISTICS ($T_A = 0$ to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	Note 1.	Note 1.	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

1. Maximum and minimum input reference frequency is limited by the VCO lock range and the feedback divider.

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		3.6	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -20\text{mA}$ (Note 2.)
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 20\text{mA}$ (Note 2.)
I_{IN}	Input Current			± 120	μA	Note 3.
I_{CC}	Maximum Core Supply Current			130	mA	
I_{CCPLL}	Maximum PLL Supply Current		15	20	mA	
C_{IN}				4	pF	
C_{pd}			25		pF	Per Output

2. The MPC932 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}/2$) transmission lines on the incident edge (see Applications Info section).

3. Inputs have pull-up/pull-down resistors which affect input current.

MPC932 AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f_{ref}	Input Reference Frequency	Note 6.		Note 6.	MHz	
t_{os}	Output-to-Output Skew		250	600	ps	Note 4.
f_{VCO}	VCO Lock Range	200		480	MHz	
f_{max}	Maximum Output Frequency (÷4) (÷5) (÷6)			120 96 80	MHz	
t_{pd}	Reference to EXT_FB Average Delay TCLK PECL_CLK	−200	0	200	ps	$f_{\text{ref}} = 50\text{MHz}$; Note 7.
t_{pw}	Output Duty Cycle (Note 4.)	$t_{\text{CYCLE}}/2$ −750	$t_{\text{CYCLE}}/2$ ±500	$t_{\text{CYCLE}}/2$ +750	ps	
t_r, t_f	Output Rise/Fall Time (Note 4.)	0.1		1.0	ns	0.8 to 2.0V
$t_{\text{PLZ}}, t_{\text{PHZ}}$	Output Disable Time	2.0		8.0	ns	$50\ \Omega$ to $V_{CC}/2$
t_{PZL}	Output Enable Time	2.0		10	ns	$50\ \Omega$ to $V_{CC}/2$
t_{jitter}	Cycle-to-Cycle Jitter (Peak-to-Peak)		±100		ps	Note 5.
t_{lock}	Maximum PLL Lock Time			10	ms	

4. Measured with $50\ \Omega$ to $V_{CC}/2$ termination.

5. See Applications Info section for more jitter information.

6. Input reference frequency is bounded by VCO lock range and feedback divide selection.

7. t_{pd} measurement uses the averaging feature of the oscilloscope to remove the jitter component.

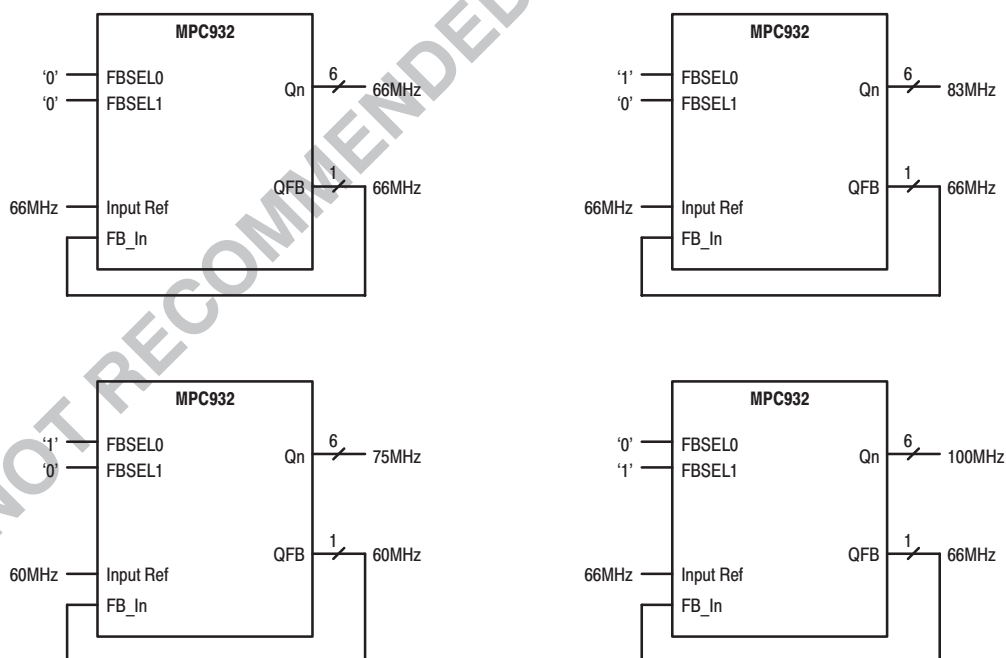
APPLICATIONS INFORMATION

Figure 2. MPC932 Potential Configurations
(Mode = 1)

Power Supply Filtering

The MPC932 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC932 provides separate power supplies for the output buffers (V_{CCO}) and the internal PLL (V_{CCA}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC932.

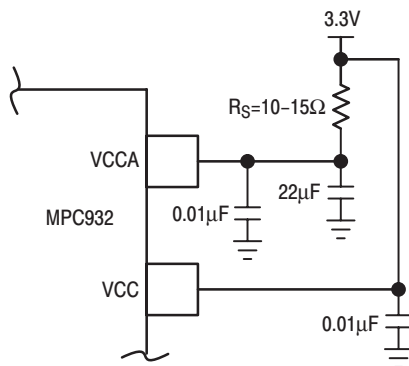


Figure 3. Power Supply Filter

Figure 3 illustrates a typical power supply filter scheme. The MPC932 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the MPC932. From the data sheet the $I_{V_{CCA}}$ current (the current sourced through the V_{CCA} pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the V_{CCA} pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 3 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC932 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter

schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC932 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC932 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fan-out of the MPC932 clock driver is effectively doubled due to its capability to drive multiple lines.

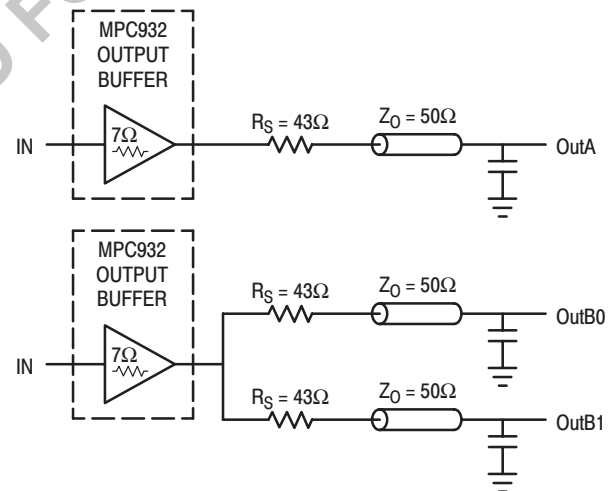


Figure 4. Single versus Dual Transmission Lines

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC932 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC932. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 / (R_S + R_o + Z_0))$$

$$Z_0 = 50\Omega \parallel 50\Omega$$

$$R_S = 43\Omega \parallel 43\Omega$$

$$R_o = 7\Omega$$

$$V_L = 3.0 (25 / (21.5 + 7 + 25)) = 3.0 (25 / 53.5) \\ = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

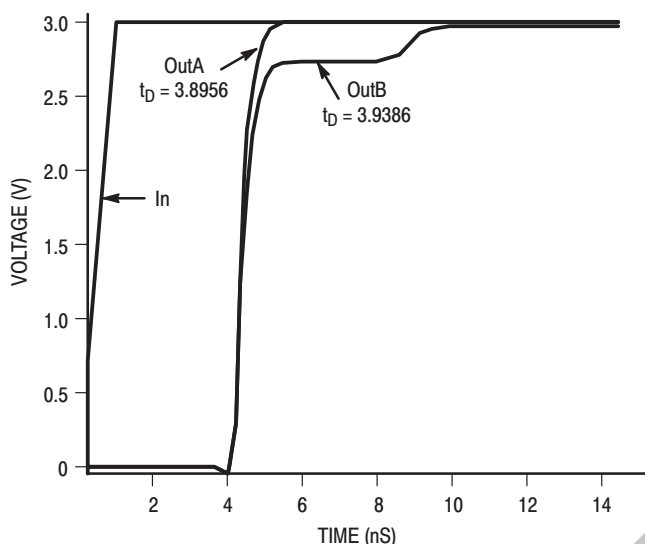


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

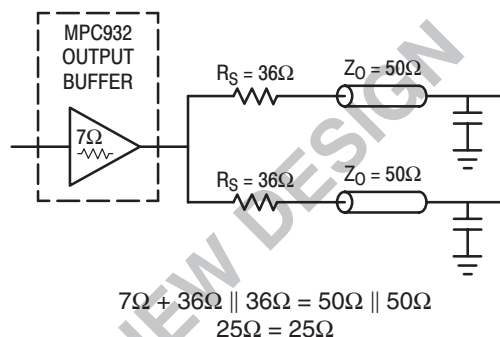


Figure 6. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

2

3.3V 1:6 LVCMOS PLL Clock Generator

The MPC9330 is a 3.3V compatible, 1:6 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance telecomm, networking and computing applications. With output frequencies up to 120 MHz and output skews less than 150ps the device meets the needs of the most demanding clock applications. The MPC9330 is specified for the temperature range of 0°C to +70°C.

Features

- 1:6 PLL based low-voltage clock generator
- 3.3V power supply
- Generates clock signals up to 120 MHz
- Maximum output skew of 150 ps
- On-chip crystal oscillator clock reference
- Alternative LVCMOS PLL reference clock input
- Internal and external PLL feedback
- PLL multiplies the reference clock by 4x, 3x, 2x, 1x, 4/3x, 3/2x, 2/3x, x/2, x/3 or x/4
- Supports zero-delay operation in external feedback mode
- Synchronous output clock stop in logic low eliminates output runt pulses
- Power_down feature reduces output clock frequency
- Drives up to 12 clock lines
- 32 lead LQFP packaging
- Ambient temperature range 0°C to +70°C
- Internal Power-Up Reset
- Pin and function compatible to the MPC930

Functional Description

The MPC9330 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9330 requires either the selection of internal PLL feedback or the connection of one of the device outputs to the feedback input to close the PLL feedback path in external feedback mode. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. In external PLL feedback configuration and with the available post-PLL dividers (divide-by-2, divide-by-4 and divide-by-6), the internal VCO of the MPC9330 is running at either 4x, 8x, 12x, 16x or 24x of the reference clock frequency. In internal feedback configuration (divide-by-16) the internal VCO is running 16x of the reference frequency. The frequency of the QA, QB, QC output banks is a division of the VCO frequency and can be configured independently for each output bank using the FSELA, FSELB and FSELC pins, respectively. The available output to input frequency ratios are 4x, 3x, 2x, 1x, 4/3x, 3/2x, 2/3x, x/2, x/3 or x/4.

The REF_SEL pin selects the internal crystal oscillator or the LVCMOS compatible input as the reference clock signal. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The outputs can be disabled (high-impedance) by deasserting the OE/ $\overline{\text{MR}}$ pin. In the PLL configuration with external feedback selected, deasserting OE/ $\overline{\text{MR}}$ causes the PLL to loose lock due to missing feedback signal presence at FB_IN. Asserting OE/ $\overline{\text{MR}}$ will enable the outputs and close the phase locked loop, enabling the PLL to recover to normal operation. The MPC9330 output clock stop control allows the outputs to start and stop synchronously in the logic low state, without the potential generation of runt pulses.

The MPC9330 is fully 3.3V compatible and requires no external loop filter components. All inputs (except XTAL) accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9330 outputs can drive one or two traces giving the devices an effective fanout of 1:12. The device is packaged in a 7x7 mm² 32-lead LQFP package.

MPC9330

**3.3V 1:6 LVCMOS
PLL CLOCK GENERATOR**



FA SUFFIX
32 LEAD LQFP PACKAGE
CASE 873A

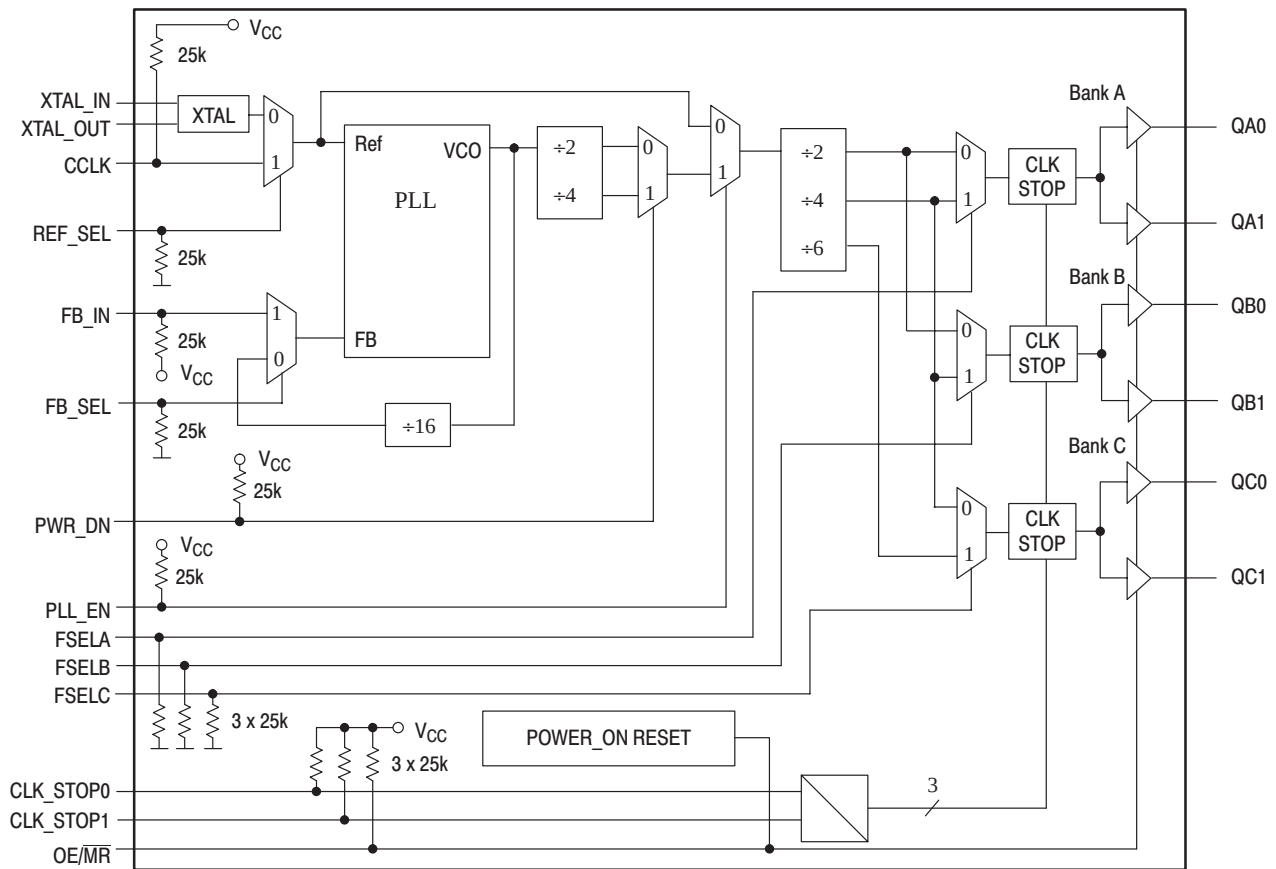
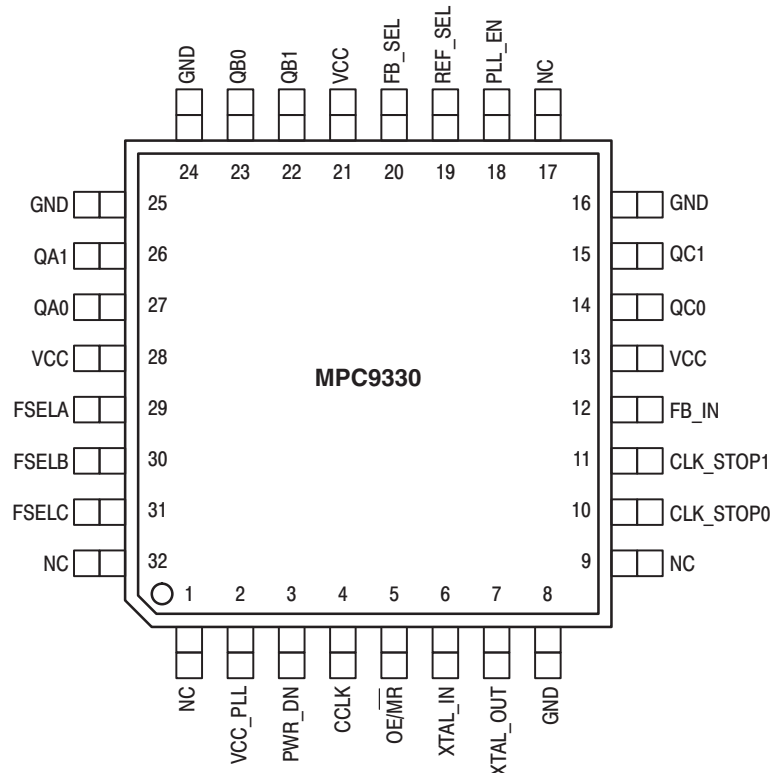


Figure 1. MPC9330 Logic Diagram



It is recommended to use an external RC filter for the analog power supply pin VCC_PLL. Please see application section for details.

Figure 2. MPC9330 32-Lead Package Pinout (Top View)

Table 1: PIN CONFIGURATION

Pin	I/O	Type	Function
CCLK	Input	LVC MOS	PLL reference clock signal
XTAL_IN, XTAL_OUT	Input	Analog	Crystal oscillator interface
FB_IN	Input	LVC MOS	PLL feedback signal input, connect to an output
FB_SEL	Input	LVC MOS	Feedback select
REF_SEL	Input	LVC MOS	Reference clock select
PWR_DN	Input	LVC MOS	Output frequency and power down select
FSELA	Input	LVC MOS	Frequency divider select for bank A outputs
FSELB	Input	LVC MOS	Frequency divider select for bank B outputs
FSELC	Input	LVC MOS	Frequency divider select for bank C outputs
PLL_EN	Input	LVC MOS	PLL enable/disable
CLK_STOP0-1	Input	LVC MOS	Clock output enable/disable
OE/MR	Input	LVC MOS	Output enable/disable (high-impedance tristate) and device reset
QA0-1, QB0-1, QC0-1	Output	LVC MOS	Clock outputs
GND	Supply	Ground	Negative power supply
VCC_PLL	Supply	VCC	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V _{CC_PLL} . Please see applications section for details.
VCC	Supply	VCC	Positive power supply for I/O and core. All VCC pins must be connected to the positive power supply for correct operation

Table 2: FUNCTION TABLE

Control	Default	0	1
REF_SEL	0	The crystal oscillator output is the PLL reference clock	CCLK is the PLL reference clock
FB_SEL	0	Internal PLL feedback of 16. $f_{VCO} = 16 * f_{ref}$	External feedback. Zero-delay operation enabled for CCLK as reference clock
PLL_EN	1	Test mode with PLL disabled. The reference clock is substituted for the internal VCO output. MPC9330 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Normal operation mode with PLL enabled.
PWR_DN	1	VCO ÷ 2 (High output frequency range)	VCO ÷ 4 (Low output frequency range)
FSELA	0	Output divider ÷ 2	Output divider ÷ 4
FSELB	0	Output divider ÷ 2	Output divider ÷ 4
FSELC	0	Output divider ÷ 4	Output divider ÷ 6
CLK_STOP[0:1]	11	See Table 3	
OE/MR	1	Outputs disabled (high-impedance state) and reset of the device. During reset in external feedback configuration, the PLL feedback loop is open. The VCO is tied to its lowest frequency. The MPC9330 requires reset after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLK). Reset does not affect PLL lock in internal feedback configuration.	Outputs enabled (active)
PWR_DN, FSELA, FSELB and FSELC control the operating PLL frequency range and input/output frequency ratios. See Tables 10–12 for supported frequency ranges and output to input frequency ratios.			

Table 3: CLOCK OUTPUT SYNCHRONOUS DISABLE (CLK_STOP) FUNCTION TABLE^a

CLK_STOP0	CLK_STOP1	QA[0:1]	QB[0:1]	QC[0:1]
0	0	Active	Stopped in logic L state	Stopped in logic L state
0	1	Active	Stopped in logic L state	Active
1	0	Stopped in logic L state	Stopped in logic L state	Active
1	1	Active	Active	Active

a. Output operation for OE/M $\overline{R}$ =1 (outputs enabled). OE/M $\overline{R}$ =0 will disable (high-impedance state) all outputs independent on CLK_STOP[0:1]

Table 4: GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output Termination Voltage		V _{CC} ÷ 2		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C _{PD}	Power Dissipation Capacitance		10		pF	Per output
C _{IN}	Input Capacitance		4.0		pF	Inputs

Table 5: ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	3.9	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} +0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} +0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6: DC CHARACTERISTICS (V_{CC} = 3.3V ± 5%, T_A = 0°C to 70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{IH}	Input High Voltage	2.0		V _{CC} + 0.3	V	LVC MOS
V _{IL}	Input Low Voltage			0.8	V	LVC MOS
V _{OH}	Output High Voltage	2.4			V	I _{OH} = -24 mA ^a
V _{OL}	Output Low Voltage			0.55 0.30	V V	I _{OL} = 24 mA I _{OL} = 12 mA
Z _{OUT}	Output Impedance		14 - 17		Ω	
I _{IN}	Input Current ^b			±100	μA	V _{IN} = V _{CC} or GND
I _{CC_PLL}	Maximum PLL Supply Current		5.0	10	mA	V _{CC_PLL} Pin
I _{CCQ}	Maximum Quiescent Supply Current		5.0	10	mA	All V _{CC} Pins

a. The MPC9330 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

b. Inputs have pull-down or pull-up resistors affecting the input current.

Table 7: AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Reference Frequency ^b PLL mode, external feedback ÷ 4 feedback ^c ÷ 8 feedback ÷ 12 feedback ÷ 16 feedback ÷ 24 feedback PLL mode, internal feedback (÷ 16 feedback) Input Reference Frequency in PLL bypass mode ^d	50 25 16.67 12.5 8.33 12.5		120 60 40 30 20 30 TBD	MHz MHz MHz MHz MHz MHz MHz	PLL locked
f_{VCO}	VCO Lock Frequency Range ^e	200		480	MHz	
f_{XTAL}	Crystal Interface Frequency Range ^f	10		25	MHz	
f_{MAX}	Output Frequency ÷ 4 output ÷ 8 output ÷ 12 output ÷ 16 output ÷ 24 output	50 25 16.67 12.5 8.33		120 60 40 30 20	MHz MHz MHz MHz MHz	PLL locked
f_{refDC} $t_{PW, MIN}$	Reference Input Duty Cycle Minimum Input Reference Pulse Width	25 2		75	% ns	
t_r, t_f	CCLK Input Rise/Fall Time			1.0	ns	0.8 to 2.0V
$t_{(\phi)}$	Propagation Delay (SPO) ^g for the – entire f_{ref} range – $f_{ref} = 8.33$ MHz – $f_{ref} = 50.0$ MHz	–1.2 –400 –70		+1.2 +400 +70	° ps ps	
$t_{sk(o)}$	Output-to-Output Skew ^h (within output bank) (any output)			50 150	ps ps	
DC	Output Duty Cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter		50	300	ps	
$t_{JIT(PER)}$	Period Jitter		35	250	ps	
$t_{JIT(\phi)}$	I/O Phase Jitter RMS (1σ)		10	70	ps	
BW	PLL closed loop bandwidth ⁱ PLL mode, external feedback ÷ 4 feedback ÷ 8 feedback ÷ 12 feedback ÷ 16 feedback ÷ 24 feedback		0.8–5.0 0.5–2.0 0.3–1.0 0.25–0.6 0.2–0.5		MHz MHz MHz MHz MHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b. PLL mode requires $PLL\_EN = 0$ to enable the PLL.

c. ÷4 feedback (FB) can be accomplished by setting $PWR\_DN = 0$ and the connection of one ÷2 output to FB_IN . See Table 1 to Table 3 for other feedback configurations.

d. In bypass mode, the MPC9330 divides the input reference clock.

e. The input frequency f_{ref} on CCLK must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.

f. The usable crystal frequency range depends on the VCO lock frequency and the PLL feedback ratio.

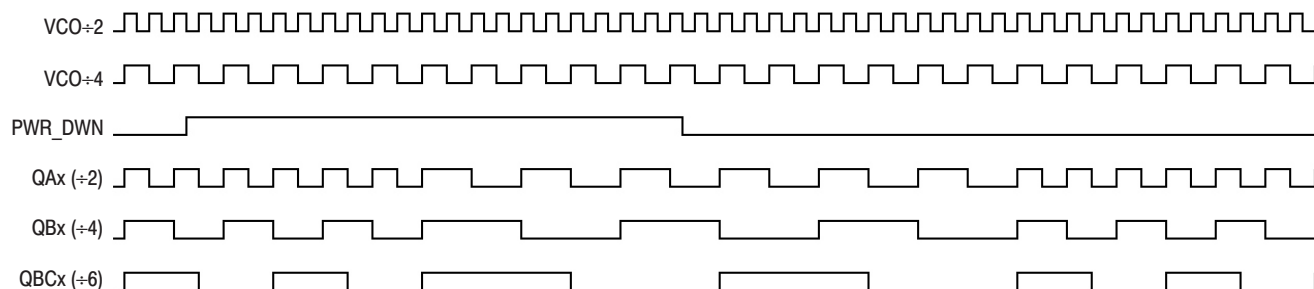
g. SPO is the static phase offset between CCLK and FB_IN ($FB\_SEL=1$ and PLL locked). $t_{sk(o)} [ps] = t_{sk(o)} [^\circ] \div (f_{ref} \bullet 360^\circ)$

h. Skew data applicable for equally loaded outputs only.

i. –3 dB point of PLL transfer characteristics.

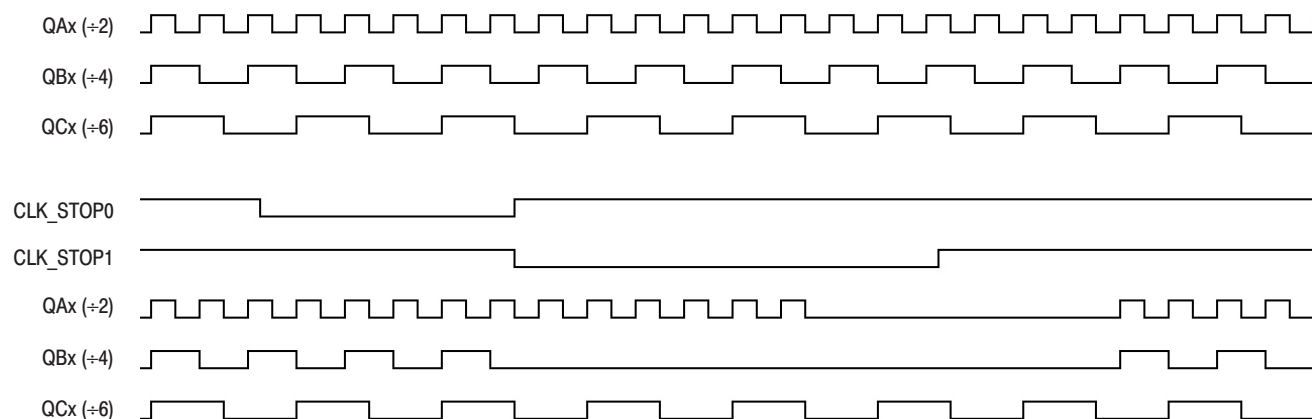
APPLICATIONS INFORMATION

Output power down (PWR_DN) timing diagram



2

Output clock stop (CLK_STOP) timing diagram



Programming the MPC9330

The MPC9330 supports output clock frequencies from 8.33 to 120 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency lock range

between 200 and 480 MHz for stable and optimal operation. The FSELA, FSELB, FSELC and PWR_DN pins select the desired output clock frequencies. Possible frequency ratios of the reference clock input to the outputs are 1:4, 1:3, 1:2, 1:1, 2:3, 4:3 and 3:2. Tables 10 through 12 illustrate the various output configurations and frequency ratios supported by the MPC9330.

Table 10: MPC9330 Example Configurations (Internal Feedback: FB_SEL = 0)

fref ^a [MHz]	PWR_DN	FSELA	FSELB	FSELC	QA[0:1]:fref ratio	QB[0:1]:fref ratio	QC[0:1]:fref ratio
12.5-30.0	0	0	0	0	fref · 4 (50-120 MHz)	fref · 4 (50-120 MHz)	fref · 2 (25-60 MHz)
	0	0	0	1	fref · 4 (50-120 MHz)	fref · 4 (50-120 MHz)	fref · 4÷3 (16.6-40 MHz)
	0	0	1	0	fref · 4 (50-120 MHz)	fref · 2 (25-60 MHz)	fref · 2 (25-60 MHz)
	0	0	1	1	fref · 4 (50-120 MHz)	fref · 2 (25-60 MHz)	fref · 4÷3 (16.6-40 MHz)
	0	1	0	0	fref · 2 (25-60 MHz)	fref · 4 (50-120 MHz)	fref · 2 (25-60 MHz)
	0	1	0	1	fref · 2 (25-60 MHz)	fref · 4 (50-120 MHz)	fref · 4÷3 (16.6-40 MHz)
	0	1	1	0	fref · 2 (25-60 MHz)	fref · 2 (25-60 MHz)	fref · 2 (25-60 MHz)
	0	1	1	1	fref · 2 (25-60 MHz)	fref · 2 (25-60 MHz)	fref · 4÷3 (16.6-40 MHz)
	1	0	0	0	fref · 2 (25-60 MHz)	fref · 2 (25-60 MHz)	fref (12.5-30 MHz)
	1	0	0	1	fref · 2 (25-60 MHz)	fref · 2 (25-60 MHz)	fref · 2÷3 (8.33-20 MHz)
	1	0	1	0	fref · 2 (25-60 MHz)	fref (12.5-30 MHz)	fref (12.5-30 MHz)
	1	0	1	1	fref · 2 (25-60 MHz)	fref (12.5-30 MHz)	fref · 2÷3 (8.33-20 MHz)
	1	1	0	0	fref (12.5-30 MHz)	fref · 2 (25-60 MHz)	fref (12.5-30 MHz)
	1	1	0	1	fref (12.5-30 MHz)	fref · 2 (25-60 MHz)	fref · 2÷3 (8.33-20 MHz)
	1	1	1	0	fref (12.5-30 MHz)	fref (12.5-30 MHz)	fref (12.5-30 MHz)
	1	1	1	1	fref (12.5-30 MHz)	fref (12.5-30 MHz)	fref · 2÷3 (8.33-20 MHz)

a. fref is the input clock reference frequency (CCLK or XTAL)

Table 11: MPC9330 Example Configurations (External Feedback and PWR_DN = 0)

PLL Feedback	fref ^a [MHz]	FSELA	FSELB	FSELC	QA[0:1]:fref ratio	QB[0:1]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 4 ^b	50-120	0	0	0	fref (50-120 MHz)	fref (50-120 MHz)	fref÷2 (25-60 MHz)
		0	0	1	fref (50-120 MHz)	fref (50-120 MHz)	fref÷3 (16.6-40 MHz)
		0	1	0	fref (50-120 MHz)	fref÷2 (25-60 MHz)	fref÷2 (25-60 MHz)
		0	1	1	fref (50-120 MHz)	fref÷2 (25-60 MHz)	fref÷3 (16.6-40 MHz)
VCO ÷ 8 ^c	25-60	1	0	0	fref (25-60 MHz)	fref · 2 (50-120 MHz)	fref (25-60 MHz)
		1	0	1	fref (25-60 MHz)	fref · 2 (50-120 MHz)	fref 2÷3 (16.6-40 MHz)
		1	1	0	fref (25-60 MHz)	fref (25-60 MHz)	fref (25-60 MHz)
		1	1	1	fref (25-60 MHz)	fref (25-60 MHz)	fref 2÷3 (16.6-40 MHz)
VCO ÷ 12 ^d	16.67-40	0	0	1	fref · 3 (50-120 MHz)	fref · 3 (50-120 MHz)	fref (16.6-40 MHz)
		0	1	1	fref · 3 (50-120 MHz)	fref · 3÷2 (25-60 MHz)	fref (16.6-40 MHz)
		1	0	1	fref · 3÷2 (25-60 MHz)	fref · 3 (50-120 MHz)	fref (16.6-40 MHz)
		1	1	1	fref · 3÷2 (25-60 MHz)	fref · 3÷2 (25-60 MHz)	fref (16.6-40 MHz)

a. fref is the input clock reference frequency (CCLK or XTAL)

b. QAx connected to FB_IN and FSELA=0, PWR_DN=0

c. QAx connected to FB_IN and FSELA=1, PWR_DN=0

d. QCx connected to FB_IN and FSELC=1, PWR_DN=0

Table 12: MPC9330 Example Configurations (External Feedback and PWR_DN = 1)

PLL Feedback	fref ^a [MHz]	FSELA	FSELB	FSELC	QA[0:1]:fref ratio	QB[0:1]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 16 ^b	12.5-30	1	0	0	fref (12.5-30 MHz)	fref 2 (25-60 MHz)	fref (12.5-30 MHz)
		1	0	1	fref (12.5-30 MHz)	fref 2 (25-60 MHz)	fref 2÷3 (8.33-20 MHz)
		1	1	0	fref (12.5-30 MHz)	fref (12.5-30 MHz)	fref (12.5-30 MHz)
		1	1	1	fref (12.5-30 MHz)	fref (12.5-30 MHz)	fref 2÷3 (8.33-20 MHz)
VCO ÷ 24 ^c	8.33-20	0	0	1	fref 3 (25-60 MHz)	fref 3 (25-60 MHz)	fref (8.33-20 MHz)
		0	1	1	fref 3 (25-60 MHz)	fref 3÷2 (12.5-30 MHz)	fref (8.33-20 MHz)
		1	0	1	fref 3÷2 (12.5-30 MHz)	fref 3 (25-60 MHz)	fref (8.33-20 MHz)
		1	1	1	fref 3÷2 (12.5-30 MHz)	fref 3÷2 (12.5-30 MHz)	fref (8.33-20 MHz)

a. fref is the input clock reference frequency (CCLK or XTAL)

b. QAx connected to FB_IN and FSELA=1, PWR_DN=1

c. QCx connected to FB_IN and FSELC=1, PWR_DN=1

APPLICATIONS INFORMATION

Power Supply Filtering

The MPC9330 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC9330 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CC_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9330. Figure 3 illustrates a typical power supply filter scheme. The MPC9330 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F . From the data sheet the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 5 mA (10 mA maximum), assuming that a minimum of 2.985V must be maintained on the V_{CC_PLL} pin. The resistor R_F shown in Figure 3 "V $_{CC\_PLL}$ Power Supply Filter" should have a resistance of 10–15 Ω to meet the voltage drop criteria.

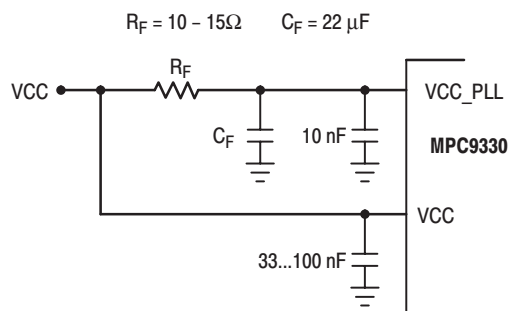


Figure 3. V $_{CC\_PLL}$ Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3 "V $_{CC\_PLL}$ Power Supply Filter", the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9330 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC9330 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC}+2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9330 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9330 clock driver is effectively doubled due to its capability to drive multiple lines.

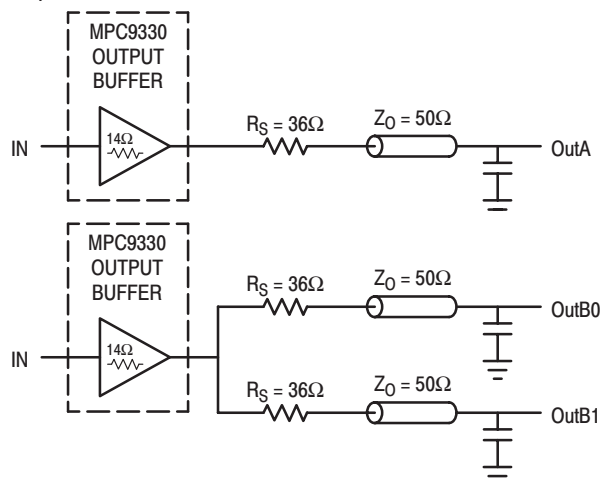


Figure 4. Single versus Dual Transmission Lines

The waveform plots in Figure 5 "Single versus Dual Line Termination Waveforms" show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9330 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9330. The output waveform in Figure 5 "Single versus Dual Line Termination Waveforms" shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$

$$Z_0 = 50\Omega \parallel 50\Omega$$

$$R_S = 36\Omega \parallel 36\Omega$$

$$R_0 = 14\Omega$$

$$V_L = 3.0 \left(25 \div (18+14+25) \right)$$

$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

1. Final skew data pending specification.

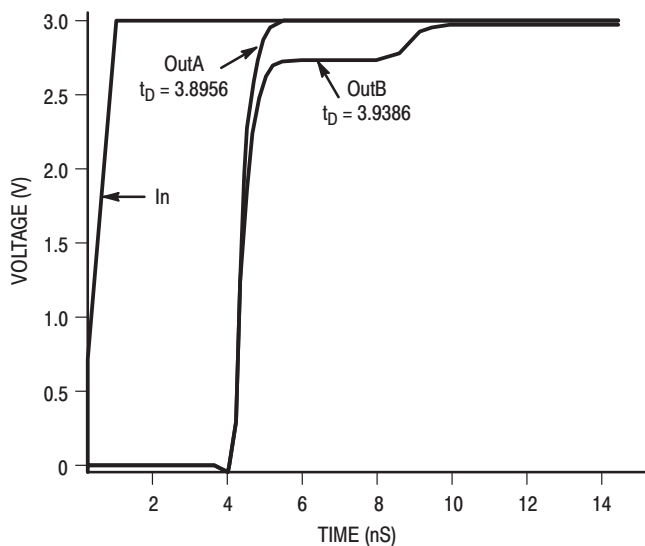


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

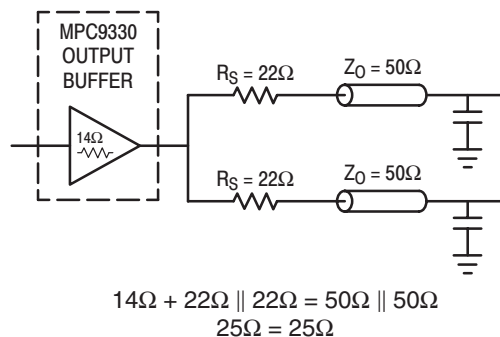


Figure 6. Optimized Dual Line Termination

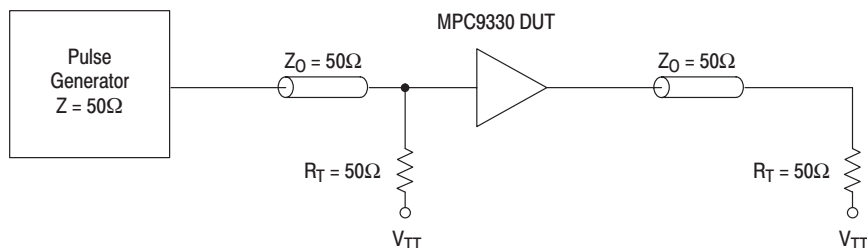
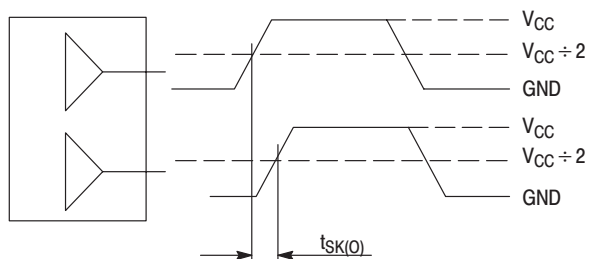


Figure 7. CCLK MPC9330 AC test reference for $V_{CC} = 3.3V$



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 8. Output-to-output Skew $t_{SK(O)}$

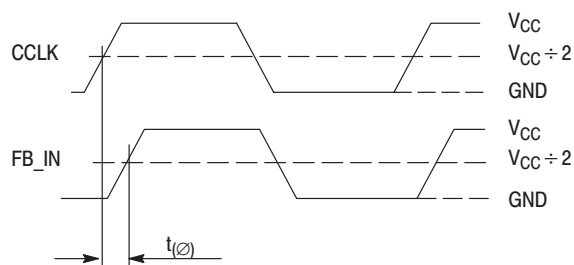
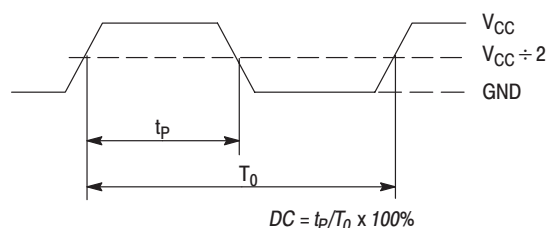
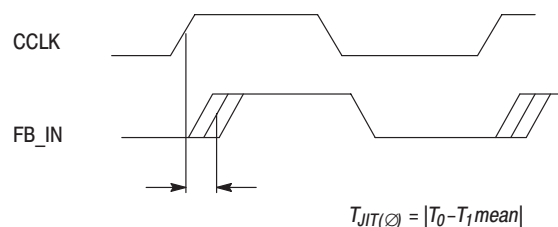


Figure 9. Propagation delay (t_{ϕ} , static phase offset) test reference



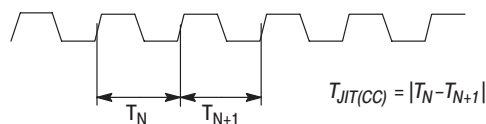
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 10. Output Duty Cycle (DC)



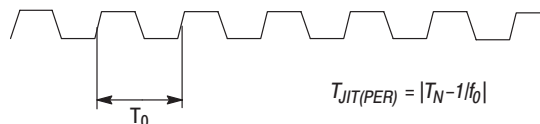
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 11. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 12. Cycle-to-cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 13. Period Jitter

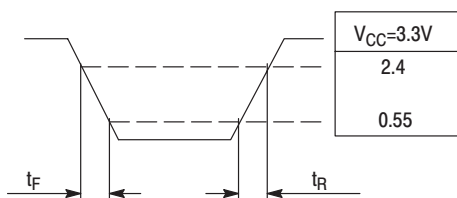


Figure 14. Output Transition Time Test Reference

2

3.3V 1:6 LVCMOS PLL Clock Generator

The MPC9331 is a 3.3V compatible, 1:6 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance telecom, networking, and computing applications. With output frequencies up to 240 MHz and output skews less than 150 ps, the device meets the needs of most the demanding clock applications. The MPC9331 is specified for the temperature range of 0°C to +70°C.

Features

- 1:6 PLL based low-voltage clock generator
- 3.3V power supply
- Generates clock signals up to 240 MHz
- Maximum output skew of 150 ps
- Differential LVPECL reference clock input
- Alternative LVCMOS PLL reference clock input
- Internal and external PLL feedback
- Supports zero-delay operation in external feedback mode
- PLL multiplies the reference clock by 4x, 3x, 2x, 1x, 4/3x, 3/2x, 2/3x, x/2, x/3 or x/4
- Synchronous output clock stop in logic low eliminates output runt pulses
- Power_down feature reduces output clock frequency
- Drives up to 12 clock lines
- 32 lead LQFP packaging
- Ambient temperature range 0°C to +70°C
- Internal Power-Up Reset
- Pin and function compatible to the MPC931

Functional Description

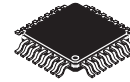
The MPC9331 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9331 requires either the selection of internal PLL feedback or the connection of one of the device outputs to the feedback input to close the PLL feedback path in external feedback mode. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. In external PLL feedback configuration and with the available post-PLL dividers (divide-by-2, divide-by-4, and divide-by-6), the internal VCO of the MPC9331 is running at either 2x, 4x, 6x, 8x, or 12x of the reference clock frequency. In internal feedback configuration (divide-by-8) the internal VCO is running 8x of the reference frequency. The frequency of the QA, QB, QC output banks is a division of the VCO frequency and can be configured independently for each output bank using the FSELA, FSELB, and FSELC pins, respectively. The available output to input frequency ratios are 4x, 3x, 2x, 1x, 4/3x, 3/2x, 2/3x, x/2, x/3, or x/4.

The REF_SEL pin selects the differential LVPECL or the LVCMOS compatible input as the reference clock signal. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply. The outputs can be disabled (high-impedance) by deasserting the OE/MR pin. In the PLL configuration with external feedback selected, deasserting OE/MR causes the PLL to loose lock due to missing feedback signal presence at FB_IN. Asserting OE/MR will enable the outputs and close the phase locked loop, enabling the PLL to recover to normal operation. The MPC9331 output clock stop control allows the outputs to start and stop synchronously in logic low state, without the potential generation of runt pulses.

The MPC9331 is fully 3.3V compatible and requires no external loop filter components. The inputs (except PCLK) accept LVCMOS except signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9331 outputs can drive one or two traces giving the devices an effective fanout of 1:12. The device is packaged in a 7x7 mm² 32-lead LQFP package.

MPC9331

**LOW VOLTAGE
3.3V LVCMOS 1:6
CLOCK GENERATOR**



FA SUFFIX
32 LEAD LQFP PACKAGE
CASE 873A

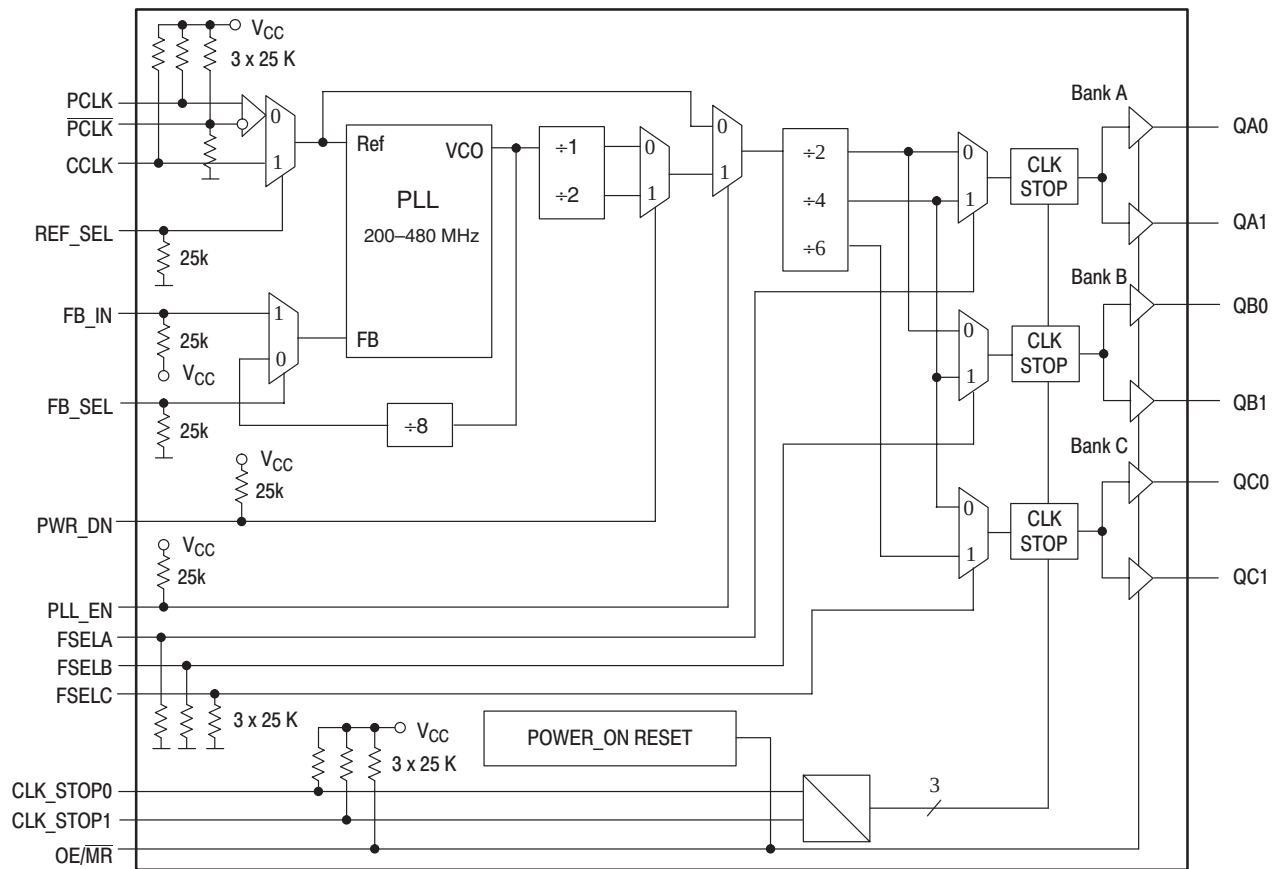
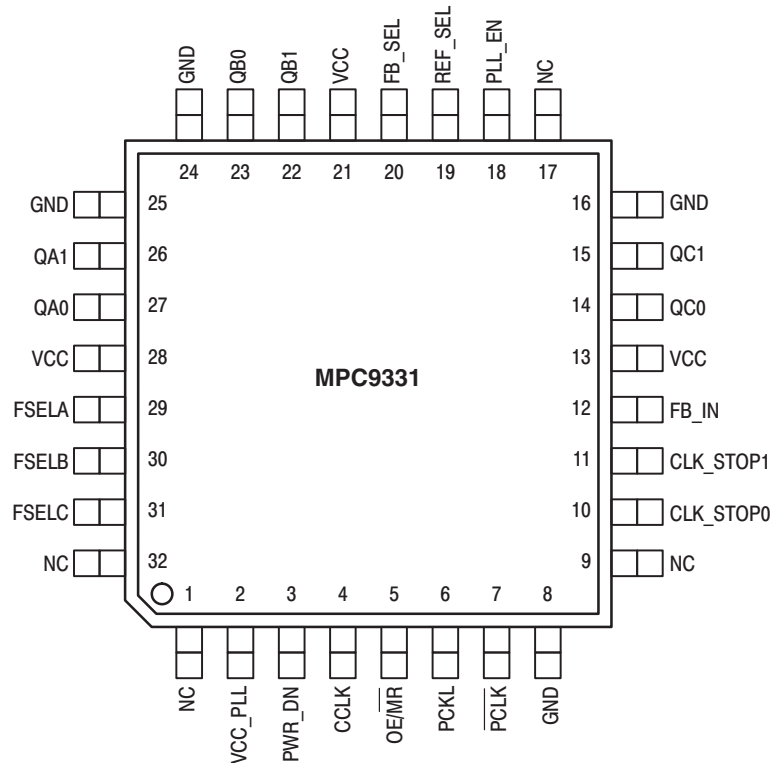


Figure 1. MPC9331 Logic Diagram



It is recommended to use an external RC filter for the analog VCC_PLL power supply pin. Please see application section for details.

Figure 2. MPC9331 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CCLK	Input	LVC MOS	PLL reference clock signal
PCLK, PCLK	Input	LVPECL	Differential PECL reference clock signal
FB_IN	Input	LVC MOS	PLL feedback signal input, connect to an output
FB_SEL	Input	LVC MOS	Feedback select
REF_SEL	Input	LVC MOS	Reference clock select
PWR_DN	Input	LVC MOS	Output frequency and power down select
FSELA	Input	LVC MOS	Frequency divider select for bank A outputs
FSELB	Input	LVC MOS	Frequency divider select for bank B outputs
FSELC	Input	LVC MOS	Frequency divider select for bank C outputs
PLL_EN	Input	LVC MOS	PLL enable/disable
CLK_STOP0-1	Input	LVC MOS	Clock output enable/disable
OE/MR	Input	LVC MOS	Output enable/disable (high-impedance tristate) and device reset
QA0-1, QB0-1, QC0-1	Output	LVC MOS	Clock outputs
GND	Supply	Ground	Negative power supply (GND)
V _{CC_PLL}	Supply	V _{CC}	PLL positive power supply (analog power supply). It is recommended to use external RC filter for the analog power supply pin V _{CC_PLL} . Please see applications section for details.
V _{CC}	Supply	V _{CC}	Positive power supply for I/O and core. All V _{CC} pins must be connected to the positive power supply for correct operation

Table 2. Function Table

Control	Default	0	1
REF_SEL	0	PCLK is the PLL reference clock	CCLK is the PLL reference clock
FB_SEL	1	Internal PLL feedback of 8. $f_{VCO} = 8 * f_{ref}$	External feedback. Zero-delay operation enabled for CCLK or PCLK as reference clock
PLL_EN	1	Test mode with PLL disabled. The reference clock is substituted for the internal VCO output. MPC9331 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Normal operation mode with PLL enabled.
PWR_DN	1	VCO ÷ 1 (High output frequency range)	VCO ÷ 2 (Low output frequency range)
FSELA	0	Output divider ÷ 2	Output divider ÷ 4
FSELB	0	Output divider ÷ 2	Output divider ÷ 4
FSELC	0	Output divider ÷ 4	Output divider ÷ 6
OE/MR	1	Outputs disabled (high-impedance state) and reset of the device. During reset in external feedback configuration, the PLL feedback loop is open. The VCO is tied to its lowest frequency. The MPC9331 requires reset after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLK or PCLK). Reset does not affect PLL lock in internal feedback configuration.	Outputs enabled (active)
CLK_STOP[0:1]	11	See Table 3	
PWR_DN, FSELA, FSELB and FSELC control the operating PLL frequency range and input/output frequency ratios. See Tables 8 – 10 for supported frequency ranges and output to input frequency ratios.			

Table 3. Clock Output Synchronous Disable (CLK_STOP) Function Table ^a

CLK_STOP0	CLK_STOP1	QA[0:1]	QB[0:1]	QC[0:1]
0	0	Active	Stopped in logic L state	Stopped in logic L state
0	1	Active	Stopped in logic L state	Active
1	0	Stopped in logic L state	Stopped in logic L state	Active
1	1	Active	Active	Active

a. Output operation for OE/MR=1 (outputs enabled). OE/MR=0 will high-impedance tristate all outputs independent on CLK_STOP[0:1]

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output termination voltage		V _{CC} ÷ 2		V	
MM	ESD protection (Machine model)	200			V	
HBM	ESD protection (Human body model)	2000			V	
LU	Latch-up immunity	200			mA	
C _{PD}	Power dissipation capacitance		10		pF	Per output
C _{IN}	Input capacitance		4.0		pF	Inputs

Table 5. Absolute Maximum Ratings^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	3.9	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} + 0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} + 0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0°C to +70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{IH}	Input high voltage	2.0		V _{CC} + 0.3	V	LVC MOS
V _{IL}	Input low voltage			0.8	V	LVC MOS
V _{PP}	Peak-to-peak input voltage PCLK, PCLK	250			mV	LVPECL
V _{CMR} ^a	Common Mode Range PCLK, PCLK	1.0		V _{CC} - 0.6	V	LVPECL
V _{OH}	Output High Voltage	2.4			V	I _{OH} = -24 mA ^b
V _{OL}	Output Low Voltage			0.55 0.30	V V	I _{OL} = 24 mA I _{OL} = 12 mA
Z _{OUT}	Output impedance		14 - 17		Ω	
I _{IN}	Input Current ^c			±200	μA	V _{IN} = V _{CC} or GND
I _{CC_PLL}	Maximum PLL Supply Current		8.0	12	mA	V _{CC_PLL} Pin
I _{CCQ}	Maximum Quiescent Supply Current ^d			26	mA	All V _{CC} Pins

a. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification

b. The MPC9331 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

c. Inputs have pull-down or pull-up resistors affecting the input current.

d. OE/MR=0 (outputs in high-impedance state).

Table 7. AC Characteristics ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{REF}	Input reference frequency	100.0		240.0	MHz	PLL locked
	PLL mode, external feedback	50.0		120.0	MHz	
	+2 feedback	33.3		80.0	MHz	
	+4 feedback	25.0		60.0	MHz	
	+6 feedback	16.67		40.0	MHz	
	+8 feedback	12.5		30.0	MHz	
f_{VCO}	PLL mode, internal feedback	25.0		60.0	MHz	
	Input reference frequency in PLL bypass mode ^b	25.0		240	MHz	
f_{MAX}	Output Frequency	100.0		240.0	MHz	PLL locked
	+2 output	50.0		120.0	MHz	
	+4 output	33.3		80.0	MHz	
	+6 output	25.0		60.0	MHz	
	+8 output	16.67		40.0	MHz	
	+12 output					
V_{PP}	Peak-to-peak input voltage	400		1000	mV	LVPECL
V_{CMR}^d	Common Mode Range	1.2		$V_{CC} - 0.9$	V	LVPECL
$t_{PW,MIN}$	Input Reference Pulse Width ^e	2.0			ns	
t_R, t_F	CCLK Input Rise/Fall Time ^f			1.0	ns	0.8 to 2.0V
t_{ϕ}	Propagation Delay	-250	-130	-50	ps	FB_SEL = 1 and PLL locked
	(static phase offset)	-180	-30	+120	ps	
	CCLK to FB_IN ^g PCLK to FB_IN ^g CCLK or PCLK to FB_IN ^h	-3.0		+3.0	ps	
$t_{sk(O)}$	Output-to-output Skew			150	ps	
DC	Output duty cycle ⁱ	$(T \div 2) - 500$	$T \div 2$	$(T \div 2) + 500$	ps	
t_R, t_F	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time			8.0	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter ^j			200	ps	
$t_{JIT(PER)}$	Period Jitter ^j			125	ps	
$t_{JIT(\phi)}$	I/O Phase Jitter	RMS (1 σ)		25	ps	
BW	PLL closed loop bandwidth ^k		2.0–8.0		MHz	
	PLL mode, external feedback		1.2–4.0		MHz	
	+ 4 feedback		1.0–3.0		MHz	
	+ 6 feedback		0.7–2.0		MHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

NOTES:

a AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b In bypass mode, the MPC9331 divides the input reference clock.

c The input frequency f_{REF} must match the VCO frequency range divided by the feedback divider ratio FB: $f_{REF} = f_{VCO} \div FB$.

d V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset t_{ϕ} .

e Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF,MAX} = 100\% - DC_{REF,MIN}$.

f The MPC9331 will operate with input rise/fall times up to 3.0 ns, but the AC characteristics, specifically t_{ϕ} , $t_{PW,MIN}$, DC and f_{MAX} can only be guaranteed if t_R, t_F are within the specified range.

g Data valid for $f_{REF}=50$ MHz and a PLL feedback of +8 (e.g. QAx connected to FB_IN and FSEL=1, PWR_DN=1).

h Data valid for $16.67 \text{ MHz} < f_{REF} < 100 \text{ MHz}$ and any feedback divider. $t_{sk(O)} [s] = t_{sk(O)} [^\circ] \div (f_{REF} \cdot 360^\circ)$.

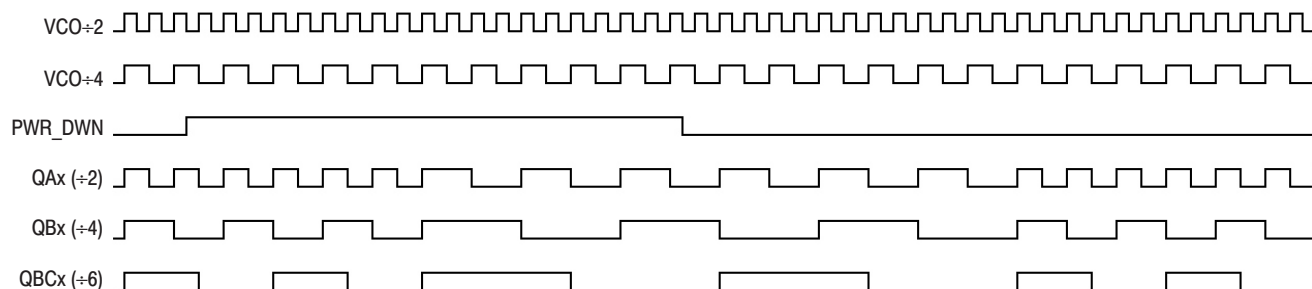
i Output duty cycle is $DC = (0.5 \pm 500 \text{ ps} \cdot f_{OUT}) \cdot 100\%$. (e.g. the DC range at $f_{OUT} = 100 \text{ MHz}$ is $45\% < DC < 55\%$).

j All outputs in +4 divider configuration.

k -3 dB point of PLL transfer characteristics.

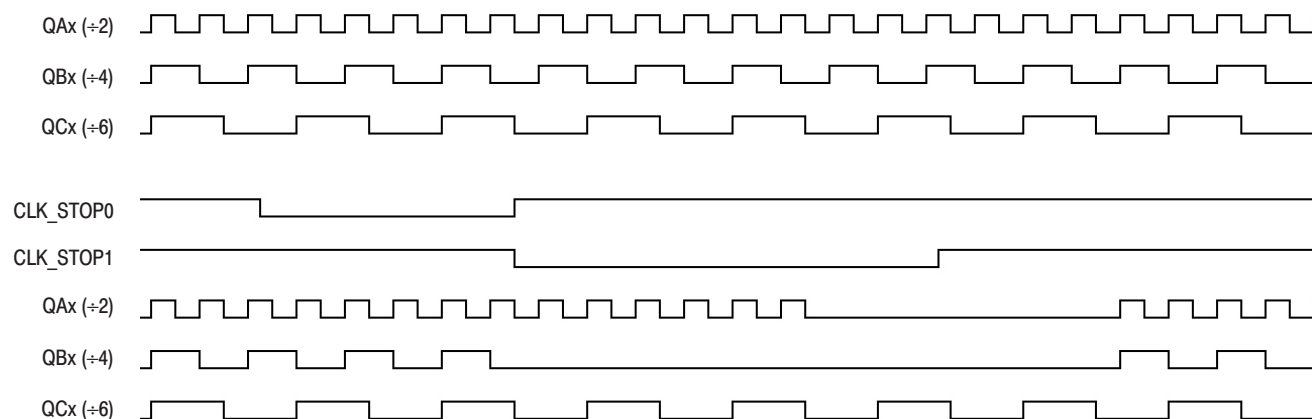
APPLICATIONS INFORMATION

Output power down (PWR_DN) timing diagram



2

Output clock stop (CLK_STOP) timing diagram



Programming the MPC9331

The MPC9331 supports output clock frequencies from 16.67 to 240 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency lock range between 200 and 480 MHz for stable and optimal operation.

The FSELA, FSELB, FSELC and PWR_DN pins select the desired output clock frequencies. Possible frequency ratios of the reference clock input to the outputs are 4:1, 3:1, 2:1, 1:1, 1:2, 2:3 and 3:2. Table 8 illustrates the various output configurations and frequency ratios supported by the MPC9331. See also Table 8 and 9 for further reference.

Table 8. MPC9331 Example Configurations (Internal Feedback and FB_SEL = 0)

fref ^a [MHz]	PWR_DN	FSELA	FSELB	FSELC	QA[0:1]:fref ratio	QB[0:1]:fref ratio	QC[0:1]:fref ratio
25.0 - 60.0	0	0	0	0	fref · 4 (100-240 MHz)	fref · 4 (100-240 MHz)	fref · 2 (50-120 MHz)
	0	0	0	1	fref · 4 (100-240 MHz)	fref · 4 (100-240 MHz)	fref · 4÷3 (33.3-80 MHz)
	0	0	1	0	fref · 4 (100-240 MHz)	fref · 2 (50-120 MHz)	fref · 2 (50-120 MHz)
	0	0	1	1	fref · 4 (100-240 MHz)	fref · 2 (50-120 MHz)	fref · 4÷3 (33.3-80 MHz)
	0	1	0	0	fref · 2 (50-120 MHz)	fref · 4 (100-240 MHz)	fref · 2 (50-120 MHz)
	0	1	0	1	fref · 2 (50-120 MHz)	fref · 4 (100-240 MHz)	fref · 4÷3 (33.3-80 MHz)
	0	1	1	0	fref · 2 (50-120 MHz)	fref · 2 (50-120 MHz)	fref · 2 (50-120 MHz)
	0	1	1	1	fref · 2 (50-120 MHz)	fref · 2 (50-120 MHz)	fref · 4÷3 (33.3-80 MHz)
	1	0	0	0	fref · 2 (50-120 MHz)	fref · 2 (50-120 MHz)	fref (25.0-60 MHz)
	1	0	0	1	fref · 2 (50-120 MHz)	fref · 2 (50-120 MHz)	fref · 2÷3 (16.67-40 MHz)
	1	0	1	0	fref · 2 (50-120 MHz)	fref (25.0-60 MHz)	fref (25.0-60 MHz)
	1	0	1	1	fref · 2 (50-120 MHz)	fref (25.0-60 MHz)	fref · 2÷3 (16.67-40 MHz)
	1	1	0	0	fref (25.0-60 MHz)	fref · 2 (50-120 MHz)	fref (25.0-60 MHz)
	1	1	0	1	fref (25.0-60 MHz)	fref · 2 (50-120 MHz)	fref · 2÷3 (16.67-40 MHz)
	1	1	1	0	fref (25.0-60 MHz)	fref (25.0-60 MHz)	fref (25.0-60 MHz)
	1	1	1	1	fref (25.0-60 MHz)	fref (25.0-60 MHz)	fref · 2÷3 (16.67-40 MHz)

a. fref is the input clock reference frequency (CCLK or PCLK)

Table 9. MPC9331 Example Configurations (External Feedback and PWR_DN = 0)

PLL Feedback	fref ^a [MHz]	FSELA	FSELB	FSELC	QA[0:1]:fref ratio	QB[0:1]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 2 ^b	100 - 240	0	0	0	fref (100-240 MHz)	fref (100-240 MHz)	fref ÷ 2 (50-120 MHz)
		0	0	1	fref (100-240 MHz)	fref (100-240 MHz)	fref ÷ 3 (33.3-80 MHz)
		0	1	0	fref (100-240 MHz)	fref ÷ 2 (50-120 MHz)	fref ÷ 2 (50-120 MHz)
		0	1	1	fref (100-240 MHz)	fref ÷ 2 (50-120 MHz)	fref ÷ 3 (33.3-80 MHz)
VCO ÷ 4 ^c	50 - 120	1	0	0	fref (50-120 MHz)	fref ÷ 2 (100-240 MHz)	fref (50-120 MHz)
		1	0	1	fref (50-120 MHz)	fref ÷ 2 (100-240 MHz)	fref ÷ 2 ÷ 3 (33.3-80 MHz)
		1	1	0	fref (50-120 MHz)	fref (100-240 MHz)	fref (50-120 MHz)
		1	1	1	fref (50-120 MHz)	fref (100-240 MHz)	fref ÷ 2 ÷ 3 (33.3-80 MHz)
VCO ÷ 6 ^d	33.3-80	0	0	1	fref ÷ 3 (100-240 MHz)	fref ÷ 3 (100-240 MHz)	fref (33.3-80 MHz)
		0	1	1	fref ÷ 3 (100-240 MHz)	fref ÷ 3 ÷ 2 (50-120 MHz)	fref (33.3-80 MHz)
		1	0	1	fref ÷ 3 ÷ 2 (50-120 MHz)	fref ÷ 3 (100-240 MHz)	fref (33.3-80 MHz)
		1	1	1	fref ÷ 3 ÷ 2 (50-120 MHz)	fref ÷ 3 ÷ 2 (50-120 MHz)	fref (33.3-80 MHz)

a. fref is the input clock reference frequency (CCLK or PCLK)

b. QAx connected to FB_IN and FSELA = 0, PWR_DN = 0

c. QAx connected to FB_IN and FSELA = 1, PWR_DN = 0

d. QCx connected to FB_IN and FSELC = 1, PWR_DN = 0

Table 10. MPC9331 Example Configurations (External Feedback and PWR_DN = 1)

PLL Feedback	fref ^a [MHz]	FSELA	FSELB	FSELC	QA[0:1]:fref ratio	QB[0:1]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 8 ^b	25.0 - 60.0	1	0	0	fref (25-60 MHz)	fref ÷ 2 (50-120 MHz)	fref (2.25-60 MHz)
		1	0	1	fref (25-60 MHz)	fref ÷ 2 (50-120 MHz)	fref ÷ 2 ÷ 3 (16.6-40 MHz)
		1	1	0	fref (25-60 MHz)	fref (25-60 MHz)	fref (25-60 MHz)
		1	1	1	fref (25-60 MHz)	fref (25-60 MHz)	fref ÷ 2 ÷ 3 (16.6-40 MHz)
VCO ÷ 12 ^c	16.67 - 40	0	0	1	fref ÷ 3 (50-120 MHz)	fref ÷ 3 (50-120 MHz)	fref (16.67-40 MHz)
		0	1	1	fref ÷ 3 (50-120 MHz)	fref ÷ 3 ÷ 2 (25-60 MHz)	fref (16.67-40 MHz)
		1	0	1	fref ÷ 3 ÷ 2 (25-60 MHz)	fref ÷ 3 (50-120 MHz)	fref (16.67-40 MHz)
		1	1	1	fref ÷ 3 ÷ 2 (25-60 MHz)	fref ÷ 3 ÷ 2 (25-60 MHz)	fref (16.67-40 MHz)

a. fref is the input clock reference frequency (CCLK or PCLK)

b. QAx connected to FB_IN and FSELA = 1, PWR_DN = 1

c. QCx connected to FB_IN and FSELC = 1, PWR_DN = 1

APPLICATIONS INFORMATION

Power Supply Filtering

The MPC9331 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the VCC_PLL power supply impacts the device characteristics, for instance I/O jitter. The MPC9331 provides separate power supplies for the output buffers (VCC) and the phase-locked loop (VCC_PLL) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the VCC_PLL pin for the MPC9331. Figure 7 illustrates a typical power supply filter scheme. The MPC9331 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F . From the data sheet the I_{CC_PLL} current (the current sourced through the VCC_PLL pin) is typically 8 mA (12 mA maximum), assuming that a minimum of 3.0V must be maintained on the VCC_PLL pin.

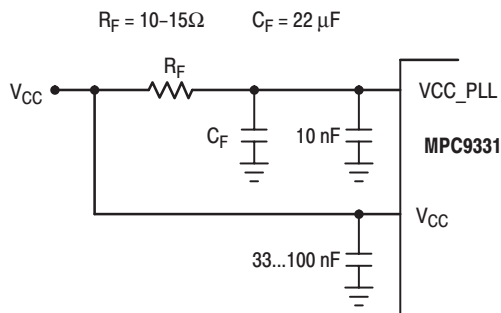


Figure 3. VCC_PLL Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9331 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC9331 clock driver was designed to drive high speed signals in a terminated transmission line environment.

To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}+2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9331 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9331 clock driver is effectively doubled due to its capability to drive multiple lines.

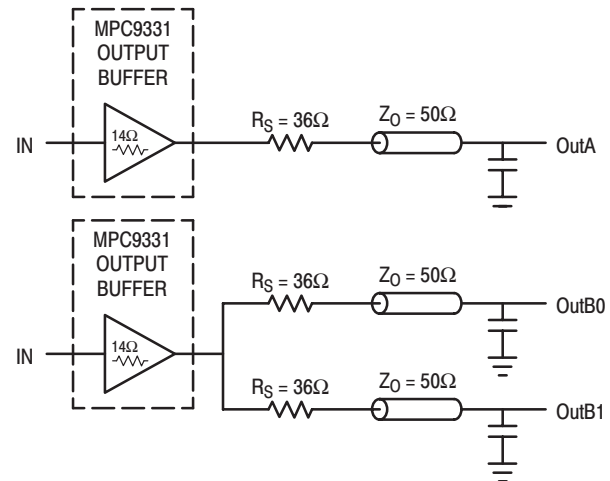


Figure 4. Single versus Dual Transmission Lines

The waveform plots in Figure 5 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9331 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9331. The output waveform in Figure 5 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned}
 V_L &= V_S (Z_0 \div (R_S + R_0 + Z_0)) \\
 Z_0 &= 50\Omega \parallel 50\Omega \\
 R_S &= 36\Omega \parallel 36\Omega \\
 R_0 &= 14\Omega \\
 V_L &= 3.0 (25 \div (18 + 14 + 25))
 \end{aligned}$$

= 1.31V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

1. Final skew data pending specification.

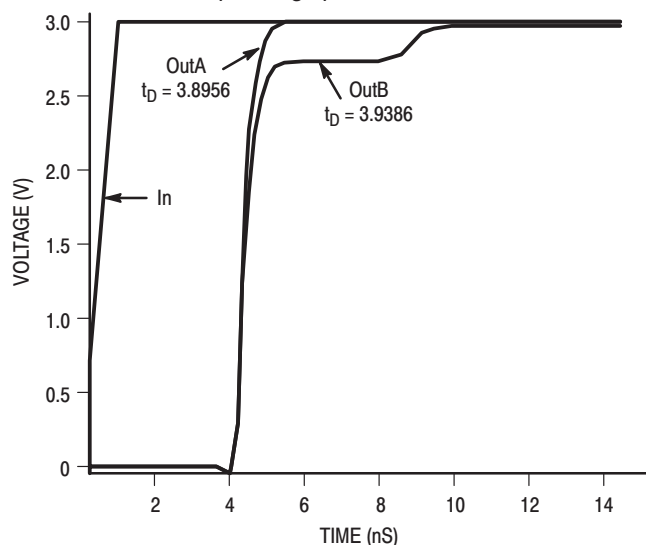


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

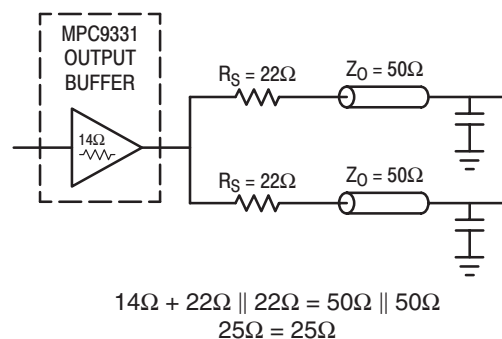


Figure 6. Optimized Dual Line Termination

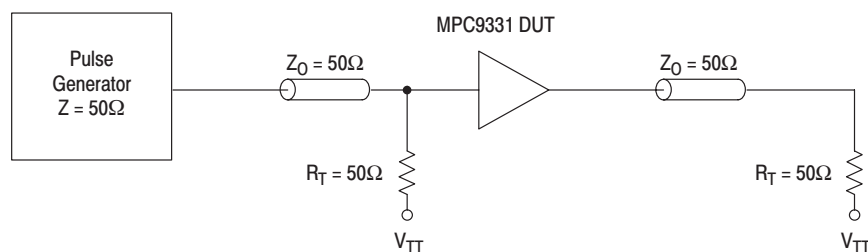
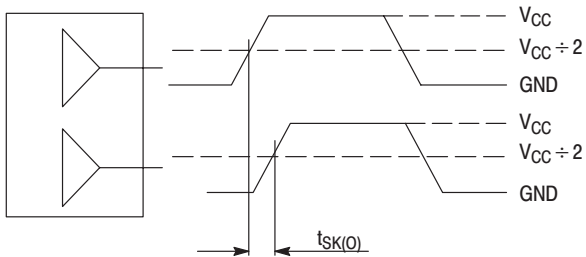
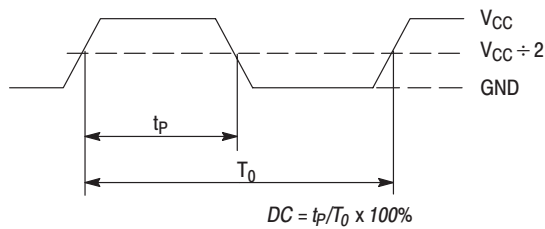


Figure 7. CCLK MPC9331 AC test reference for $V_{CC} = 3.3V$



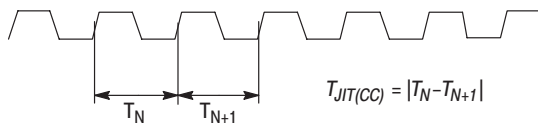
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 8. Output-to-output Skew $t_{SK(O)}$



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 10. Output Duty Cycle (DC)



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 12. Cycle-to-cycle Jitter

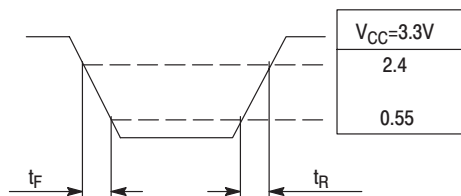


Figure 14. Output Transition Time Test Reference

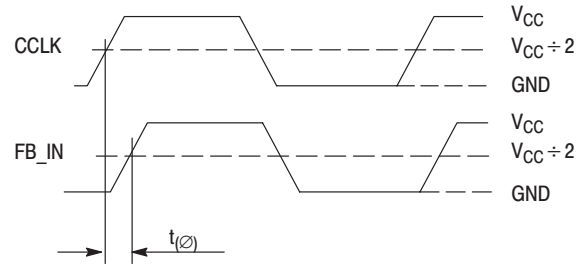
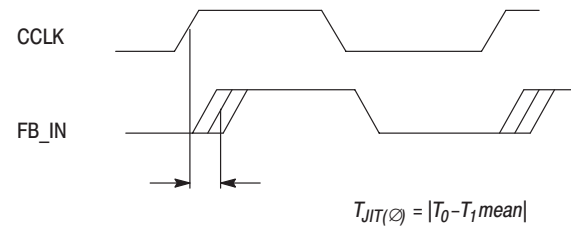
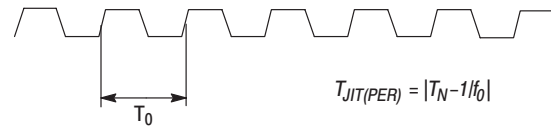


Figure 9. Propagation delay (t_{ϕ} , static phase offset) test reference



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 11. I/O Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 13. Period Jitter

Low Voltage PLL Clock Driver

2

The MPC9350 is a 2.5V and 3.3V compatible, PLL based clock generator targeted for high performance clock distribution systems. With output frequencies of up to 200 MHz and maximum output skews of 150 ps the MPC9350 is ideal for the most demanding clock tree designs. The device offers 9 low skew clock outputs, each is configurable to support the clocking needs of the various high-performance microprocessors including the PowerQuicc II integrated communication microprocessor. The extended temperature range of the MPC9350 supports telecommunication and networking requirements. The device employs a fully differential PLL design to minimize cycle-to-cycle and long-term jitter.

Features

- 9 outputs LVCMOS PLL clock generator
- 25 – 200 MHz output frequency range
- 2.5V and 3.3V compatible
- Compatible to various microprocessor such as PowerQuicc II
- Supports networking, telecommunications and computer applications
- Fully integrated PLL
- Configurable outputs: divide-by-2, 4 and 8 of VCO frequency
- Selectable output to input frequency ratio of 8:1, 4:1, 2:1 or 1:1
- Oscillator or crystal reference inputs
- Internal PLL feedback
- Output disable
- PLL enable/disable
- Low skew characteristics: maximum 150 ps output-to-output
- 32 lead LQFP package
- Temperature range –40°C to +85°C

Functional Description

The MPC9350 generates high frequency clock signals and provides nine exact frequency-multiplied copies of the reference clock signal. The internal PLL allows the MPC9350 to operate in frequency locked condition and to multiply the input reference clock. The reference clock frequency and the divider in the internal feedback path determine the VCO frequency. Two selectable PLL feedback frequency ratios are available on the MPC9350 to provide input frequency range flexibility. The FBSEL pin selects between divide-by-16 or divide-by-32 of the VCO frequency for PLL feedback. This feedback divider must be selected to match the VCO frequency range. With the available feedback output dividers the internal VCO of the MPC9350 is running at either 16x or 32x of the reference clock frequency. The frequency of the QA, QB, QC and QD outputs is either one half, one fourth or one eighth of the selected VCO frequency and can be configured for each output bank using the FSELA, FSELB, FSELC and FSELD pins, respectively. The available output to input frequency ratios are 16:1, 8:1, 4:1 and 2:1. The REF_SEL pin selects the crystal oscillator inputs or the LVCMOS compatible reference input (TCLK). TCLK also provides an external test clock in static test mode when the PLL enable pin (PLL_EN) is pulled to logic low state. In test mode, the selected input reference clock is routed directly to the output dividers without using the PLL. The test mode is intended for system diagnostics, test and debug purpose. This test mode is fully static and the minimum clock frequency specification does not apply. The outputs can be disabled by deasserting the OE pin (logic high state). In PLL mode, deasserting OE maintains PLL lock due to the internal feedback path. The MPC9350 is fully 2.5V and 3.3V compatible and requires no external loop filter components. The on-chip crystal oscillator requires no external components beyond a series resonant crystal. All inputs except the crystal oscillator interface accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9350 outputs can drive one or two traces giving the device an effective fanout of 1:18. The device is packaged in a 7x7 mm² 32-lead LQFP package.

MPC9350

**LOW VOLTAGE
3.3V AND 2.5V PLL
CLOCK GENERATOR**



FA SUFFIX
32 LEAD LQFP PACKAGE
CASE 873A

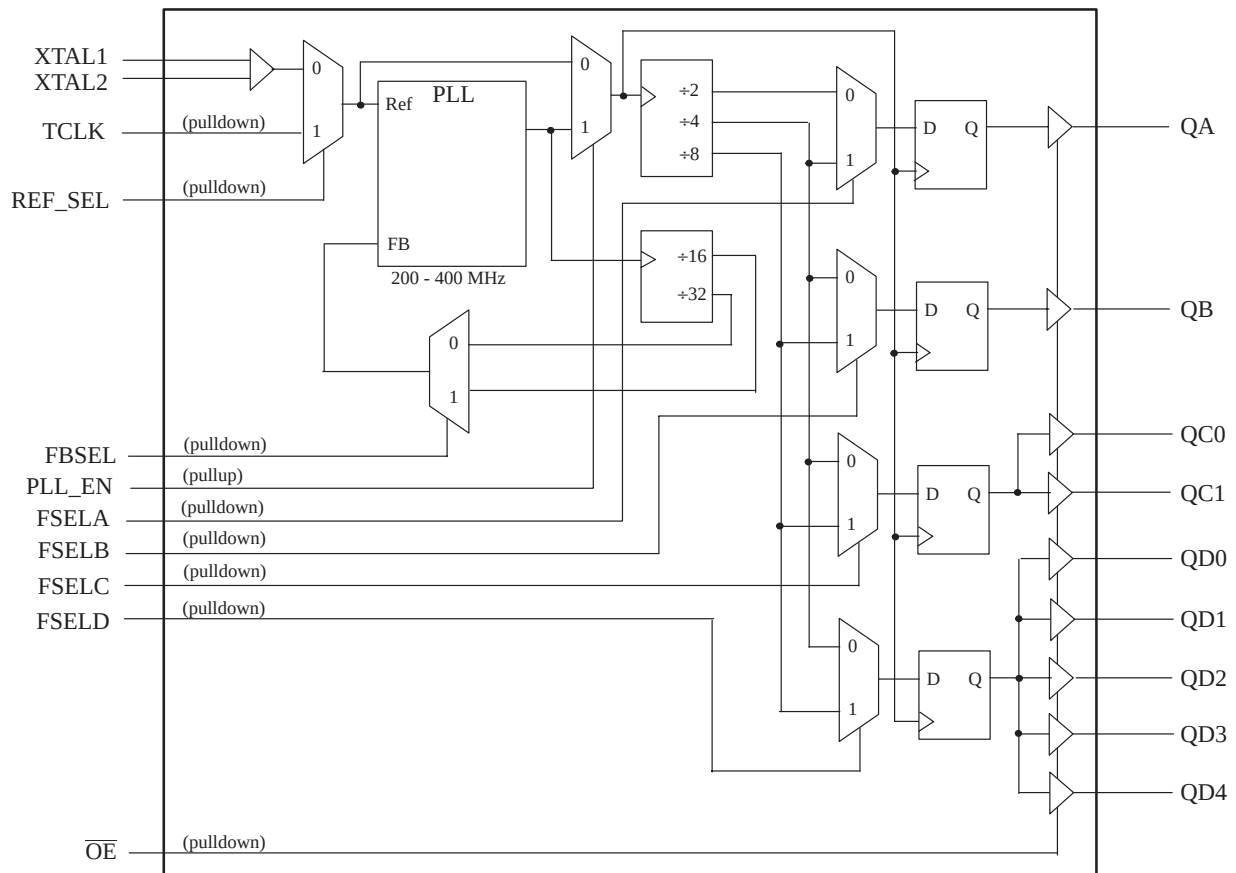


Figure 1. MPC9350 Logic Diagram

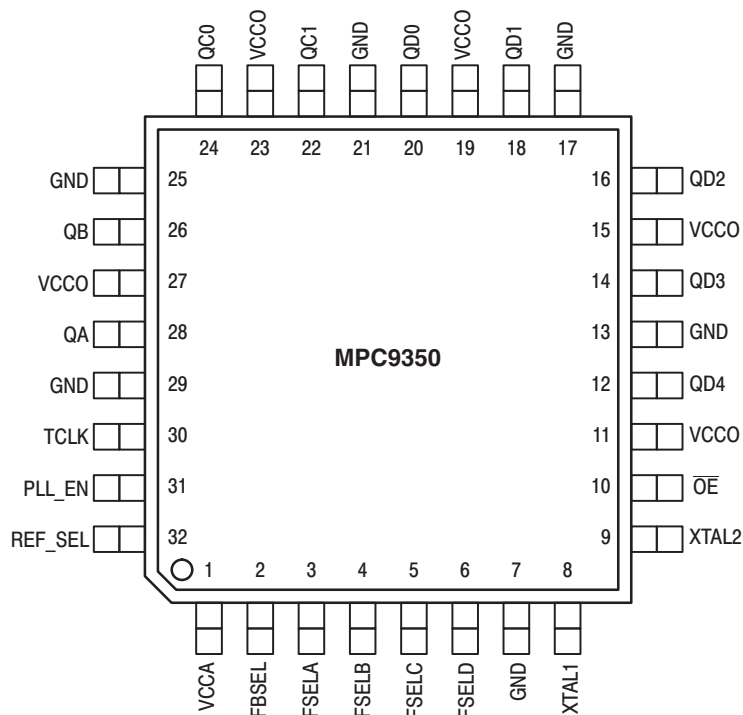


Figure 2. Pinout: 32-Lead Package Pinout (Top View)

PIN CONFIGURATION

Pin	I/O	Type	Function
XTAL1, XTAL2	Input	Analog	Crystal oscillator terminals
TCLK	Input	LVC MOS	Single ended reference clock signal or test clock
FBSEL	Input	LVC MOS	Selects feedback divider ratio
REF_SEL	Input	LVC MOS	Selects input reference source
FSELA	Input	LVC MOS	Output A divider selection
FSELB	Input	LVC MOS	Output B divider selection
FSELC	Input	LVC MOS	Outputs C divider selection
FSELD	Input	LVC MOS	Outputs D divider selection
$\overline{OE}$	Input	LVC MOS	Output enable/disable
QA	Output	LVC MOS	Bank A clock output
QB	Output	LVC MOS	Bank B clock output
QC0, QC1	Output	LVC MOS	Bank C clock outputs
QD0 - QD4	Output	LVC MOS	Bank D clock outputs
GND	Supply	Ground	Negative power supply
VCCA	Supply	VCC	Positive power supply for the PLL
VCC	Supply	VCC	Positive power supply for I/O and core

FUNCTION TABLE

Control	Default	0	1
REF_SEL	0	Selects XTAL	Selects TCLK
PLL_EN	1	Test mode with PLL disabled. The input clock is directly routed to the output dividers	PLL enabled. The VCO output is routed to the output dividers
FBSEL	0	Selects feedback divider $\div 32$ $VCO = 32 * \text{Input reference clock}$	Selects feedback divider $\div 16$ $VCO = 16 * \text{Input reference clock}$
$\overline{OE}$	0	Outputs enabled	Outputs disabled
FSELA	0	$QA = VCO \div 2$	$QA = VCO \div 4$
FSELB	0	$QB = VCO \div 4$	$QB = VCO \div 8$
FSELC	0	$QC = VCO \div 4$	$QC = VCO \div 8$
FSELD	0	$QD = VCO \div 4$	$QD = VCO \div 8$

ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	4.6	V	
V_{IN}	DC Input Voltage	-0.3	$V_{CC}+0.3$	V	
V_{OUT}	DC Output Voltage	-0.3	$V_{CC}+0.3$	V	
I_{IN}	DC Input Current		± 20	mA	
I_{OUT}	DC Output Current		± 50	mA	
T_S	Storage temperature	-40	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	2.0		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input low voltage	-0.3		0.8	V	LVC MOS
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -24 \text{ mA}^8$
V_{OL}	Output Low Voltage			0.55 0.30	V V	$I_{OL} = 24 \text{ mA}$ $I_{OL} = 12 \text{ mA}$
I_{IN}	Input Current			200	μA	$V_{IN} = 0V$ or $V_{IN} = V_{CC}$
Z_{OUT}	Output impedance		14 - 17		Ω	
C_{IN}	Input capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		10		pF	Per Output
I_{CCA}	Maximum PLL Supply Current			10	mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins
V_{TT}	Output termination voltage		$V_{CC} + 2$		V	

8. The MPC9350 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50 Ω series terminated transmission lines.

AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$ or $V_{CC} = 2.5V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency ÷ 16 feedback ÷ 32 feedback Static Test Mode	12.5 6.25 0		25 12.5 300	MHz MHz MHz	FBSEL = 1 FBSEL = 0 PLL_EN = 0
f_{XTAL}	Crystal Oscillator Frequency	10		25	MHz	XTAL inputs
f_{VCO}	VCO Frequency	200		400	MHz	PLL_EN = 1
f_{MAX}	Maximum Output Frequency ÷ 2 output ÷ 4 output ÷ 8 output	100 50 25		200 100 50	MHz MHz MHz	
f_{refDC}	Reference Input Duty Cycle	25		75	%	
t_r, t_f	TLCK Input Rise/Fall Time $V_{CC} = 2.5V$ $V_{CC} = 3.3V$			1.0 1.0	ns ns	0.7V to 1.7V 0.8V to 2.0V
$t_{sk(o)}$	Output-to-output Skew		45	150	ps	
t_{PW}	Output Duty Cycle	45	50	55	ps	T=Clock period
t_r, t_f	Output Rise/Fall Time	0.1	0.5	1.0	ns	see Figure 10
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
BW	PLL closed loop bandwidth ÷ 16 feedback ($V_{CC} = 3.3V$) ÷ 16 feedback ($V_{CC} = 2.5V$) ÷ 32 feedback ($V_{CC} = 3.3V$) ÷ 32 feedback ($V_{CC} = 2.5V$)		2.0 – 8.0 1.0 – 4.0 1.5 – 3.5 0.7 – 2.0		MHz MHz MHz MHz	
$t_{JIT(CC)}$	Cycle-to-cycle jitter single frequency multiple frequencies		30 100	200 300	ps ps	
$t_{JIT(PER)}$	Period Jitter ÷ 16 feedback ÷ 32 feedback		30 80	150 200	ps ps	
t_{LOCK}	Maximum PLL Lock Time			1	ms	
$t_{JIT(\varnothing)}$	I/O Phase Jitter (RMS)		5 – 20		ps	RMS value

a. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}

DC CHARACTERISTICS ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40^\circ$ to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	1.7		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input low voltage	-0.3		0.7	V	LVC MOS
V_{OH}	Output High Voltage	1.8			V	$I_{OH} = -15\text{ mA}^a$
V_{OL}	Output Low Voltage			0.6	V	$I_{OL} = 15\text{ mA}$
Z_{OUT}	Output impedance		17 - 20		Ω	
I_{IN}	Input Current			200	μA	$V_{IN} = 0V$ or $V_{IN} = V_{CC}$
C_{IN}	Input capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		10		pF	Per Output
I_{CCA}	Maximum PLL Supply Current			10	mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins
V_{TT}	Output termination voltage		$V_{CC} \pm 2$		V	

- a. The MPC9350 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

APPLICATIONS INFORMATION

Programming the MPC9350

The MPC9350 clock driver outputs can be configured into several divider modes, in addition the internal feedback of the device allows for flexibility in establishing two input to output frequency relationships. The output division settings establish the output frequency relationship. The output divider of the four output groups allows the user to configure the outputs into 1:1, 2:1, 4:1 and 4:2:1 frequency ratios. The use of even dividers ensure that the output duty cycle is always 50%. “Output Frequency Relationship FBSEL = 1, (VC0 = 32 * CLK)” and “Output Frequency Relationship FBSEL = 0, (VC0 = 16 * CLK)”

illustrate the various output configurations. The tables describes the outputs using the input clock frequency CLK as a reference.

In addition, it must be ensured that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL supports output frequencies from 25 MHz to 200 MHz while the VCO frequency range is specified from 200 MHz to 400 MHz and should not be exceeded for stable operation.

2

Output Frequency Relationship^a FBSEL = 1, (VC0 = 32 * CLK)

Inputs				Outputs			
FSELA	FSELB	FSELC	FSELD	QA	QB	QC0, QC1	QD0-QD4
0	0	0	0	16 * CLK	8 * CLK	8 * CLK	8 * CLK
0	0	0	1	16 * CLK	8 * CLK	8 * CLK	4 * CLK
0	0	1	0	16 * CLK	8 * CLK	4 * CLK	8 * CLK
0	0	1	1	16 * CLK	8 * CLK	4 * CLK	4 * CLK
0	1	0	0	16 * CLK	4 * CLK	8 * CLK	8 * CLK
0	1	0	1	16 * CLK	4 * CLK	8 * CLK	4 * CLK
0	1	1	0	16 * CLK	4 * CLK	4 * CLK	8 * CLK
0	1	1	1	16 * CLK	4 * CLK	4 * CLK	4 * CLK
1	0	0	0	8 * CLK	8 * CLK	8 * CLK	8 * CLK
1	0	0	1	8 * CLK	8 * CLK	8 * CLK	4 * CLK
1	0	1	0	8 * CLK	8 * CLK	4 * CLK	8 * CLK
1	0	1	1	8 * CLK	8 * CLK	4 * CLK	4 * CLK
1	1	0	0	8 * CLK	4 * CLK	8 * CLK	8 * CLK
1	1	0	1	8 * CLK	4 * CLK	8 * CLK	4 * CLK
1	1	1	0	8 * CLK	4 * CLK	4 * CLK	8 * CLK
1	1	1	1	8 * CLK	4 * CLK	4 * CLK	4 * CLK

a. Output frequency relationship with respect to input reference frequency CLK. Consult the MPC9351 datasheet more input to output relationships in external feedback mode.

Output Frequency Relationship^a FBSEL = 0, (VC0 = 16 * CLK)

Inputs				Outputs			
FSELA	FSELB	FSELC	FSELD	QA	QB	QC0, QC1	QD0-QD4
0	0	0	0	8 * CLK	4 * CLK	4 * CLK	4 * CLK
0	0	0	1	8 * CLK	4 * CLK	4 * CLK	2 * CLK
0	0	1	0	8 * CLK	4 * CLK	2 * CLK	4 * CLK
0	0	1	1	8 * CLK	4 * CLK	2 * CLK	2 * CLK
0	1	0	0	8 * CLK	2 * CLK	4 * CLK	4 * CLK
0	1	0	1	8 * CLK	2 * CLK	4 * CLK	2 * CLK
0	1	1	0	8 * CLK	2 * CLK	2 * CLK	4 * CLK
0	1	1	1	8 * CLK	2 * CLK	2 * CLK	2 * CLK
1	0	0	0	4 * CLK	4 * CLK	4 * CLK	4 * CLK
1	0	0	1	4 * CLK	4 * CLK	4 * CLK	2 * CLK
1	0	1	0	4 * CLK	4 * CLK	2 * CLK	4 * CLK
1	0	1	1	4 * CLK	4 * CLK	2 * CLK	2 * CLK
1	1	0	0	4 * CLK	2 * CLK	4 * CLK	4 * CLK
1	1	0	1	4 * CLK	2 * CLK	4 * CLK	2 * CLK
1	1	1	0	4 * CLK	2 * CLK	2 * CLK	4 * CLK
1	1	1	1	4 * CLK	2 * CLK	2 * CLK	2 * CLK

a. Output frequency relationship with respect to input reference frequency CLK. Consult the MPC9351 datasheet for more input to output relationships in external feedback mode.

Power Supply Filtering

The MPC9350 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC9350 provides separate power supplies for the output buffers (V_{CCO}) and the phase-locked loop (V_{CCA}) of the device.

The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC9350. Figure 3 illustrates a typical power supply filter scheme. The MPC9350 is most susceptible to noise with spectral content in the 10kHz to 5MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the MPC9350. From the data sheet the I_{VCCA} current (the current sourced through the V_{CCA} pin) is typically 10 mA (15 mA maximum), assuming that a minimum of 3.0V must be maintained on the V_{CCA} pin. Very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 3 “Power Supply Filter” must have a resistance of 10-15 Ω to meet the voltage drop criteria for $V_{CC}=3.3V$. For $V_{CC}=2.5V$ operation, R_S must be selected to maintain the minimum V_{CC} specification of 2.375V for the PLL supply pin for proper operation. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8-10 Ω resistor to avoid potential V_{CC} drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

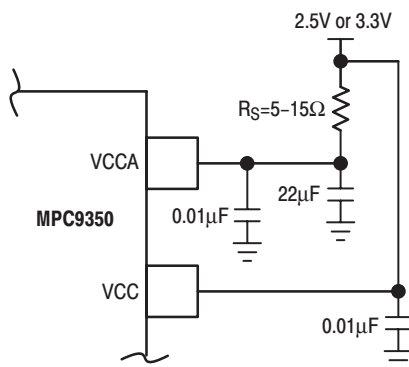


Figure 3. Power Supply Filter

Although the MPC9350 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC9350 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 15 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC}+2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9350 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel.

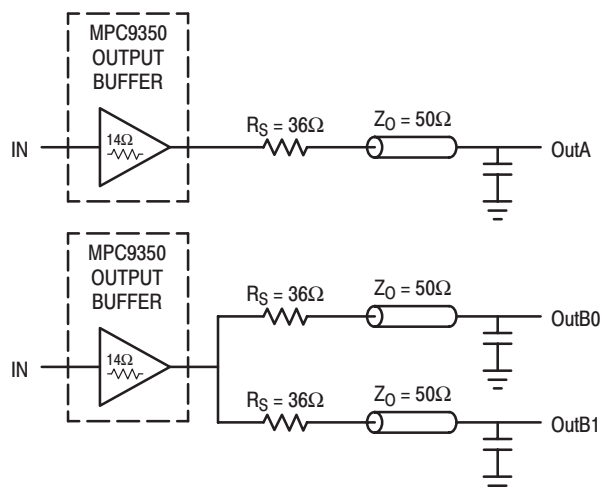


Figure 4. Single versus Dual Transmission Lines

The waveform plots in Figure 5 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9350 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9350. The output waveform in Figure 5 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned} V_L &= V_S (Z_0 \div (R_S + R_0 + Z_0)) \\ Z_0 &= 50\Omega \parallel 50\Omega \\ R_S &= 36\Omega \parallel 36\Omega \\ R_0 &= 17\Omega \\ V_L &= 3.0 (25 \div (18 + 17 + 25)) \\ &= 1.25V \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

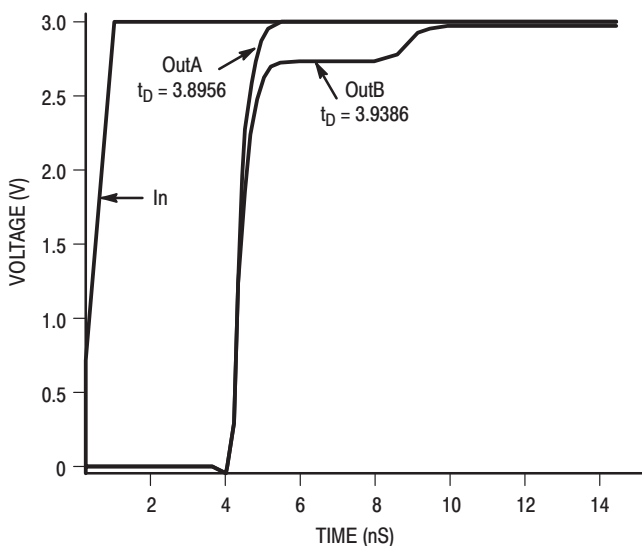


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

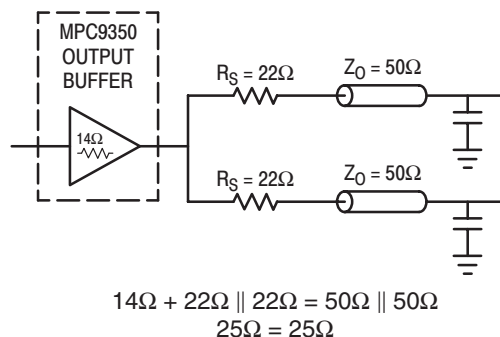


Figure 6. Optimized Dual Line Termination

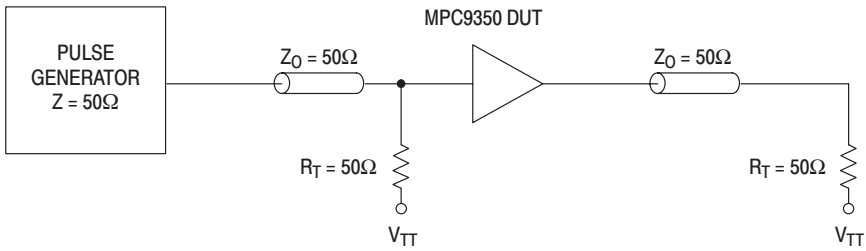
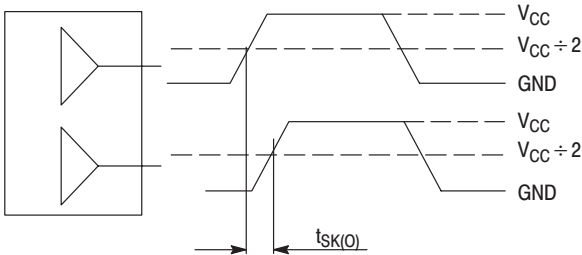
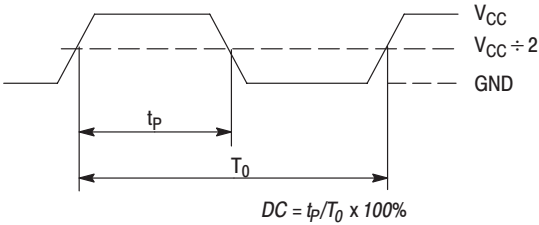


Figure 7. TCLK MPC9350 AC test reference for $V_{cc} = 3.3V$ and $V_{cc} = 2.5V$



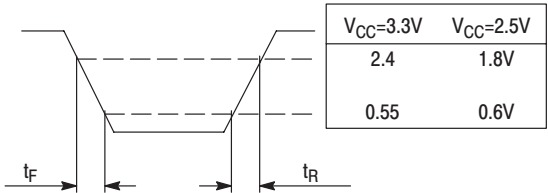
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 8. Output-to-output Skew $t_{SK(O)}$



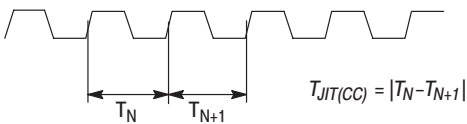
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 9. Output Duty Cycle (DC)



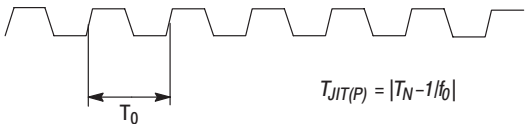
The time from the maximum low level voltage to minimum high level of a clock signal, expressed in ns

Figure 10. Transition Time Test Reference



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 11. Cycle-to-cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 12. Period Jitter

Low Voltage PLL Clock Driver

The MPC9351 is a 2.5V and 3.3V compatible, PLL based clock generator targeted for high performance clock distribution systems. With output frequencies of up to 200 MHz and a maximum output skew of 150 ps the MPC9351 is an ideal solution for the most demanding clock tree designs. The device offers 9 low skew clock outputs, each is configurable to support the clocking needs of the various high-performance microprocessors including the PowerQuicc II integrated communication microprocessor. The extended temperature range of the MPC9351 supports telecommunication and networking requirements. The device employs a fully differential PLL design to minimize cycle-to-cycle and long-term jitter.

Features

- 9 outputs LVCMOS PLL clock generator
- 25 - 200 MHz output frequency range
- Fully integrated PLL
- 2.5V and 3.3V compatible
- Compatible to various microprocessors such as PowerQuicc II
- Supports networking, telecommunications and computer applications
- Configurable outputs: divide-by-2, 4 and 8 of VCO frequency
- LVPECL and LVCMOS compatible inputs
- External feedback enables zero-delay configurations
- Output enable/disable and static test mode (PLL enable/disable)
- Low skew characteristics: maximum 150 ps output-to-output
- Cycle-to-cycle jitter max. 22 ps RMS
- 32 lead LQFP package
- Ambient Temperature Range -40°C to +85°C

Functional Description

The MPC9351 utilizes PLL technology to frequency and phase lock its outputs onto an input reference clock. Normal operation of the MPC9351 requires a connection of one of the device outputs to the EXT_FB input to close the PLL feedback path. The reference clock frequency and the output divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. With available output dividers of divide-by-2, divide-by-4 and divide-by-8 the internal VCO of the MPC9351 is running at either 2x, 4x or 8x of the reference clock frequency. The frequency of the QA, QB, QC and QD outputs is either the one half, one fourth or one eighth of the selected VCO frequency and can be configured for each output bank using the FSEL_A, FSEL_B, FSEL_C and FSEL_D pins, respectively. The available output to input frequency ratios are 4:1, 2:1, 1:1, 1:2 and 1:4. The REF_SEL pin selects the differential LVPECL (PCLK and PCLK) or the LVCMOS compatible reference input (TCLK). The MPC9351 also provides a static test mode when the PLL enable pin (PLL_EN) is pulled to logic low state. In test mode, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The test mode is intended for system diagnostics, test and debug purpose. This test mode is fully static and the minimum clock frequency specification does not apply. The outputs can be disabled by deasserting the OE pin (logic high state). In PLL mode, deasserting OE causes the PLL to loose lock due to no feedback signal presence at EXT_FB. Asserting OE will enable the outputs and close the phase locked loop, also enabling the PLL to recover to normal operation. The MPC9351 is fully 2.5V and 3.3V compatible and requires no external loop filter components. All inputs except PCLK and PCLK accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9351 outputs can drive one or two traces giving the devices an effective fanout of 1:18. The device is packaged in a 7x7 mm² 32-lead LQFP package.

Application Information

The fully integrated PLL of the MPC9351 allows the low skew outputs to lock onto a clock input and distribute it with essentially zero propagation delay to multiple components on the board. In zero-delay buffer mode, the PLL minimizes phase offset between the outputs and the reference signal.

MPC9351

**LOW VOLTAGE
2.5V AND 3.3V PLL
CLOCK GENERATOR**



FA SUFFIX
LQFP PACKAGE
CASE 873A

2

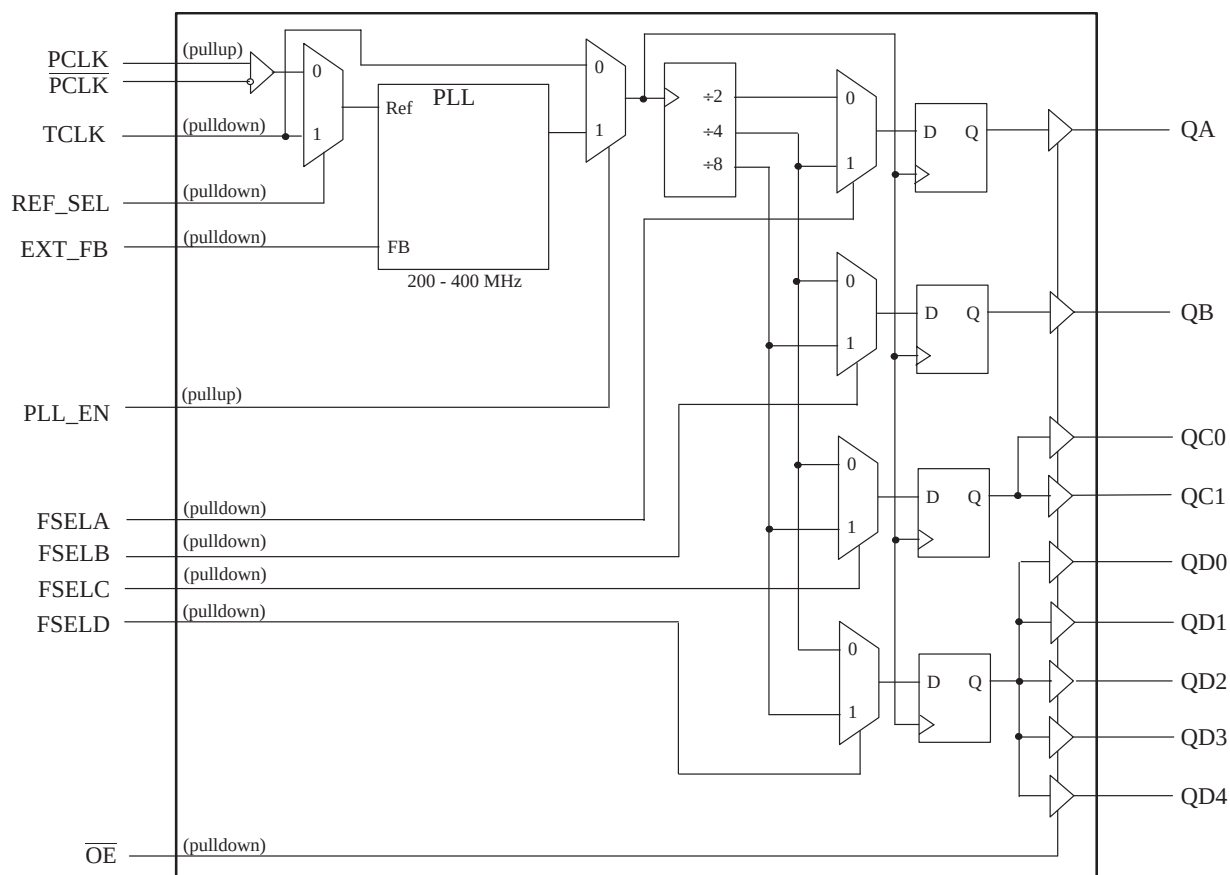


Figure 1. MPC9351 Logic Diagram

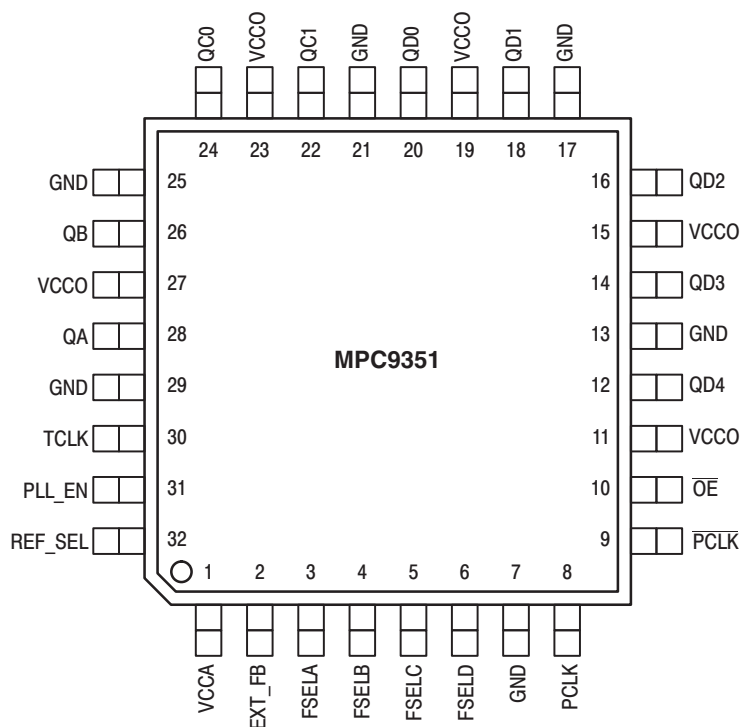


Figure 2. Pinout: 32-Lead Package Pinout (Top View)

PIN CONFIGURATION

Pin	I/O	Type	Function
PCLK, $\overline{\text{PCLK}}$	Input	LVPECL	Differential clock reference Low voltage positive ECL input
TCLK	Input	LVC MOS	Single ended reference clock signal or test clock
EXT_FB	Input	LVC MOS	Feedback signal input, connect to a QA, QB, QC, QD output
REF_SEL	Input	LVC MOS	Selects input reference clock
FSELA	Input	LVC MOS	Output A divider selection
FSELB	Input	LVC MOS	Output B divider selection
FSELC	Input	LVC MOS	Outputs C divider selection
FSELD	Input	LVC MOS	Outputs D divider selection
$\overline{\text{OE}}$	Input	LVC MOS	Output enable/disable
QA	Output	LVC MOS	Bank A clock output
QB	Output	LVC MOS	Bank B clock output
QC0, QC1	Output	LVC MOS	Bank C clock outputs
QD0 - QD4	Output	LVC MOS	Bank D clock outputs
VCCA	Supply	VCC	Positive power supply for the PLL
VCC	Supply	VCC	Positive power supply for I/O and core
GND	Supply	Ground	Negative power supply

FUNCTION TABLE

Control	Default	0	1
REF_SEL	0	Selects PCLK as reference clock	Selects TCLK as reference clock
PLL_EN	1	Test mode with PLL disabled. The input clock is directly routed to the output dividers	PLL enabled. The VCO output is routed to the output dividers
$\overline{\text{OE}}$	0	Outputs enabled	Outputs disabled, PLL loop is open VCO is forced to its minimum frequency
FSELA	0	$\text{QA} = \text{VCO} \div 2$	$\text{QA} = \text{VCO} \div 4$
FSELB	0	$\text{QB} = \text{VCO} \div 4$	$\text{QB} = \text{VCO} \div 8$
FSELC	0	$\text{QC} = \text{VCO} \div 4$	$\text{QC} = \text{VCO} \div 8$
FSELD	0	$\text{QD} = \text{VCO} \div 4$	$\text{QD} = \text{VCO} \div 8$

ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	4.6	V	
V_{IN}	DC Input Voltage	-0.3	$V_{\text{CC}}+0.3$	V	
V_{OUT}	DC Output Voltage	-0.3	$V_{\text{CC}}+0.3$	V	
I_{IN}	DC Input Current		± 20	mA	
I_{OUT}	DC Output Current		± 50	mA	
T_{S}	Storage Temperature	-55	150	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{\text{CC}} \div 2$		V	
MM	ESD (Machine Model)	200			V	
HBM	ESD (Human Body Model)	2000			V	
LU	Latch-Up	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}			4.0		pF	Inputs

DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input Low Voltage			0.8	V	LVC MOS
V_{PP}	Peak-to-Peak Input Voltage PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}^a	Common Mode Range PCLK, $\overline{PCLK}$	1.0		$V_{CC}-0.6$	V	LVPECL
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -24\text{ mA}^b$
V_{OL}	Output Low Voltage			0.55 0.30	V V	$I_{OL} = 24\text{ mA}$ $I_{OL} = 12\text{ mA}$
Z_{OUT}	Output Impedance		14 - 17		Ω	
I_{IN}	Input Leakage Current			± 200	μA	$V_{IN} = V_{CC}$ or GND
I_{CCA}	Maximum PLL Supply Current		3.0	5.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins

- a. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
- b. The MPC9351 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines.

AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency + 2 feedback + 4 feedback + 8 feedback Static test mode	100 50 25 0		200 100 50 300	MHz MHz MHz MHz	PLL_EN = 1 PLL_EN = 1 PLL_EN = 1 PLL_EN = 0
f_{VCO}	VCO Frequency	200		400	MHz	
f_{MAX}	Maximum Output Frequency + 2 output + 4 output + 8 output	100 50 25		200 100 50	MHz MHz MHz	
f_{refDC}	Reference Input Duty Cycle	25		75	%	
V_{PP}	Peak-to-Peak Input Voltage PCLK, $\overline{PCLK}$	500		1000	mV	LVPECL
V_{CMR}^b	Common Mode Range PCLK, $\overline{PCLK}$	1.2		$V_{CC}-0.9$	V	LVPECL
t_r, t_f	TCLK Input Rise/Fall Time			1.0	ns	0.8 to 2.0V
$t_{(\phi)}$	Propagation Delay (static phase offset) TCLK to EXT_FB PCLK to EXT_FB	-50 +25		+150 +325	ps ps	PLL locked PLL locked
$t_{sk(o)}$	Output-to-Output Skew			150	ps	
DC	Output Duty Cycle 100 – 200 MHz 50 – 100 MHz 25 – 50 MHz	45 47.5 48.75	50 50 50	55 52.5 51.75	% % %	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, ZH}$	Output Enable Time			10	ns	
BW	PLL closed loop bandwidth + 2 feedback + 4 feedback + 8 feedback		9.0 – 20.0 3.0 – 9.5 1.2 – 2.1		MHz MHz MHz	-3 db point of PLL transfer characteristic
$t_{JIT(CC)}$	Cycle-to-cycle jitter + 4 feedback Single Output Frequency Configuration		10	22	ps	RMS value
$t_{JIT(PER)}$	Period Jitter + 4 feedback Single Output Frequency Configuration		8.0	15	ps	RMS value
$t_{JIT(\phi)}$	I/O Phase Jitter		4.0 – 17		ps	RMS value
t_{LOCK}	Maximum PLL Lock Time			1.0	ms	

- a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
- b. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\phi)}$.

DC CHARACTERISTICS ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	1.7		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input Low Voltage			0.7	V	LVC MOS
V_{PP}	Peak-to-Peak Input Voltage PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}^a	Common Mode Range PCLK, $\overline{PCLK}$	1.0		$V_{CC}-0.6$	V	LVPECL
V_{OH}	Output High Voltage	1.8			V	$I_{OH} = -15\text{ mA}^b$
V_{OL}	Output Low Voltage			0.6	V	$I_{OL} = 15\text{ mA}$
Z_{OUT}	Output Impedance		17 - 20		Ω	
I_{IN}	Input Leakage Current			± 200	μA	$V_{IN} = V_{CC}$ or GND
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		10		pF	Per Output
I_{CCA}	Maximum PLL Supply Current		3.0	5.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins

- a. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
- b. The MPC9351 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

AC CHARACTERISTICS ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency ÷ 2 feedback ÷ 4 feedback ÷ 8 feedback	100 50 25		200 100 50	MHz MHz MHz	
f_{VCO}	VCO Frequency	200		400	MHz	
f_{MAX}	Maximum Output Frequency ÷ 2 output ÷ 4 output ÷ 8 output	100 50 25		200 100 50	MHz MHz MHz	
f_{refDC}	Reference Input Duty Cycle	25		75	%	
V_{PP}	Peak-to-Peak Input Voltage PCLK, $\overline{PCLK}$	500		1000	mV	LVPECL
V_{CMR}^b	Common Mode Range PCLK, $\overline{PCLK}$	1.2		$V_{CC}-0.6$	V	LVPECL
t_r, t_f	TCLK Input Rise/Fall Time			1.0	ns	0.7 to 1.7V
$t_{(\phi)}$	Propagation Delay (static phase offset) TCLK to EXT_FB PCLK to EXT_FB	-100 0		+100 +300	ps ps	PLL locked PLL locked
$t_{sk(o)}$	Output-to-Output Skew			150	ps	
DC	Output Duty Cycle 100 – 200 MHz 50 – 100 MHz 25 – 50 MHz	45 47.5 48.75	50 50 50	55 52.5 51.75	% % %	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.6 to 1.8V
$t_{PLZ, HZ}$	Output Disable Time			12	ns	
$t_{PZL, ZH}$	Output Enable Time			12	ns	
BW	PLL closed loop bandwidth ÷ 2 feedback ÷ 4 feedback ÷ 8 feedback		4.0 – 15.0 2.0 – 7.0 0.7 – 2.0		MHz MHz MHz	-3dB point of PLL transfer characteristic
$t_{JIT(CC)}$	Cycle-to-cycle jitter Single Output Frequency Configuration		10	22	ps	RMS value
$t_{JIT(PER)}$	Period Jitter Single Output Frequency Configuration		8.0	15	ps	RMS value
$t_{JIT(\phi)}$	I/O Phase Jitter		6.0 – 25		ps	RMS value
t_{LOCK}	Maximum PLL Lock Time			1.0	ms	

- a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
- b. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\phi)}$.

APPLICATIONS INFORMATION

Programming the MPC9351

The MPC9351 clock driver outputs can be configured into several divider modes, in addition the external feedback of the device allows for flexibility in establishing various input to output frequency relationships. The output divider of the four output groups allows the user to configure the outputs into 1:1, 2:1, 4:1 and 4:2:1 frequency ratios. The use of even dividers ensure that the output duty cycle is always 50%. "Output Frequency Relationship for an Example Configuration" illustrates

the various output configurations, the table describes the outputs using the input clock frequency CLK as a reference.

The output division settings establish the output relationship, in addition, it must be ensured that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL supports output frequencies from 25 MHz to 200 MHz while the VCO frequency range is specified from 200 MHz to 400 MHz and should not be exceeded for stable operation.

Output Frequency Relationship^a for an Example Configuration

Inputs				Outputs			
FSELA	FSELB	FSELC	FSELD	QA	QB	QC	QD
0	0	0	0	2 * CLK	CLK	CLK	CLK
0	0	0	1	2 * CLK	CLK	CLK	CLK ÷ 2
0	0	1	0	4 * CLK	2 * CLK	CLK	2 * CLK
0	0	1	1	4 * CLK	2 * CLK	CLK	CLK
0	1	0	0	2 * CLK	CLK ÷ 2	CLK	CLK
0	1	0	1	2 * CLK	CLK ÷ 2	CLK	CLK ÷ 2
0	1	1	0	4 * CLK	CLK	CLK	2 * CLK
0	1	1	1	4 * CLK	CLK	CLK	CLK
1	0	0	0	CLK	CLK	CLK	CLK
1	0	0	1	CLK	CLK	CLK	CLK ÷ 2
1	0	1	0	2 * CLK	2 * CLK	CLK	2 * CLK
1	0	1	1	2 * CLK	2 * CLK	CLK	CLK
1	1	0	0	CLK	CLK ÷ 2	CLK	CLK
1	1	0	1	CLK	CLK ÷ 2	CLK	CLK ÷ 2
1	1	1	0	2 * CLK	CLK	CLK	2 * CLK
1	1	1	1	2 * CLK	CLK	CLK	CLK

a. Output frequency relationship with respect to input reference frequency CLK. QC1 is connected to EXT_FB. More frequency ratios are available by the connection of QA to the feedback input (EXT_FB).

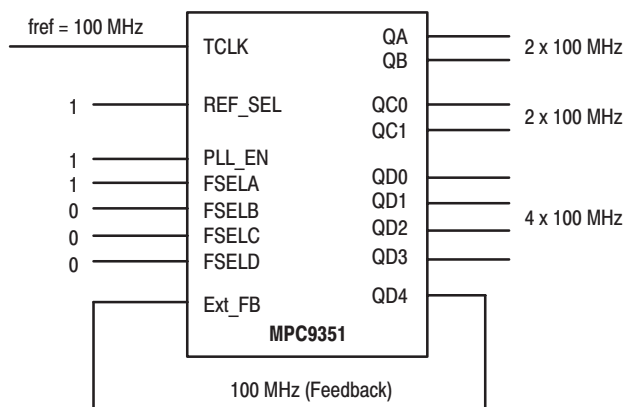
Using the MPC9351 in zero-delay applications

Nested clock trees are typical applications for the MPC9351. For these applications the MPC9351 offers a differential LVPECL clock input pair as a PLL reference. This allows for the use of differential LVPECL primary clock distribution devices such as the Motorola MC100EP111 or MC10EP222, taking advantage of its superior low-skew performance. Clock trees using LVPECL for clock distribution and the MPC9351 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers.

The external feedback option of the MPC9351 PLL allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge and virtually eliminates the propagation delay through the device.

The remaining insertion delay (skew error) of the MPC9351 in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the

static phase offset (SPO or t_{ϕ}), I/O jitter ($t_{JIT(\phi)}$, phase or long-term jitter), feedback path delay and the output-to-output skew ($t_{SK(O)}$) relative to the feedback output.



MPC9351 zero-delay configuration (feedback of QD4)

Calculation of part-to-part skew

The MPC9351 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs (TCLK or PCLK) of two or more MPC9351 are connected together, the maximum overall timing uncertainty from the common TCLK input to any output is:

$$t_{SK(PP)} = t_{(\emptyset)} + t_{SK(O)} + t_{PD, LINE(FB)} + t_{JIT(\emptyset)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

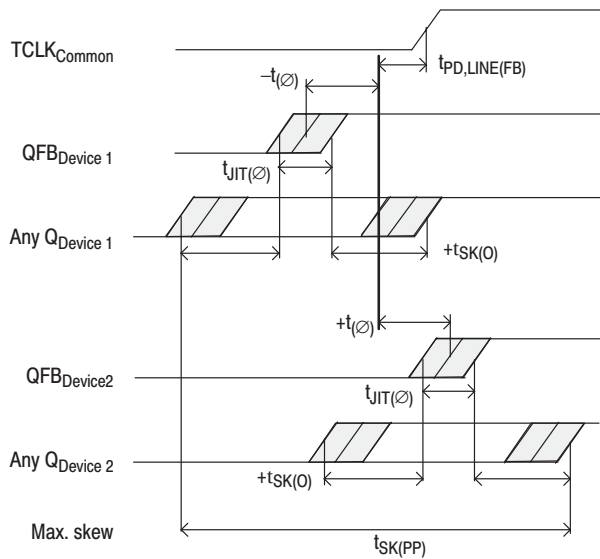


Figure 3. MPC9351 max. device-to-device skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

Table 8: Confidence Factor CF

CF	Probability of clock edge within the distribution
$\pm 1\sigma$	0.68268948
$\pm 2\sigma$	0.95449988
$\pm 3\sigma$	0.99730007
$\pm 4\sigma$	0.99993663
$\pm 5\sigma$	0.99999943
$\pm 6\sigma$	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% ($\pm 3\sigma$) is assumed, resulting in a worst case timing uncertainty from input to any output of -251 ps to 351 ps relative to TCLK ($V_{CC}=3.3V$ and $f_{VCO} = 400$ MHz):

$$t_{SK(PP)} = [-50ps...150ps] + [-150ps...150ps] + [(17ps \cdot -3)...(17ps \cdot 3)] + t_{PD, LINE(FB)}$$

$$t_{SK(PP)} = [-251ps...351ps] + t_{PD, LINE(FB)}$$

Above equation uses the maximum I/O jitter number shown in the AC characteristic table for $V_{CC}=3.3V$ (17 ps RMS). I/O jitter is frequency dependant with a maximum at the lowest

VCO frequency (200 MHz for the MPC9351). Applications using a higher VCO frequency exhibit less I/O jitter than the AC characteristic limit. The I/O jitter characteristics in Figure 4 and Figure 5 can be used to derive a smaller I/O jitter number at the specific VCO frequency, resulting in tighter timing limits in zero-delay mode and for part-to-part skew $t_{SK(PP)}$.

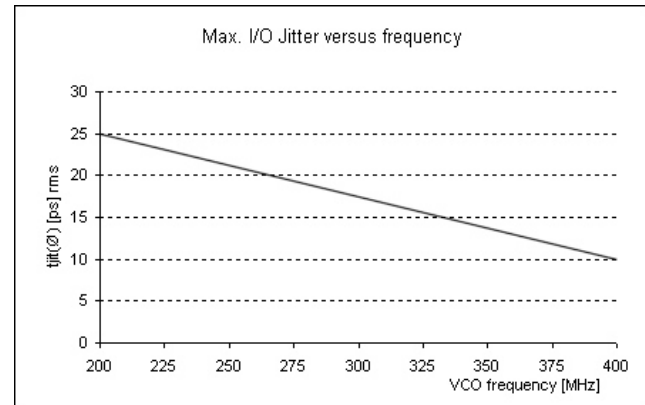


Figure 4. Max. I/O Jitter (RMS) versus frequency for $V_{CC}=2.5V$

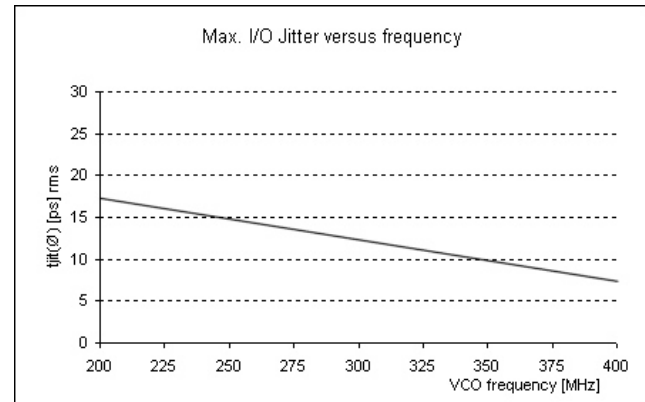


Figure 5. Max. I/O Jitter (RMS) versus frequency for $V_{CC}=3.3V$

Power Supply Filtering

The MPC9351 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9351 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC9351. Figure 6 illustrates a typical power supply filter scheme. The MPC9351 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F . From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 3 mA (5 mA maximum), assuming that a mini-

minimum of 2.325V ($V_{CC}=3.3V$ or $V_{CC}=2.5V$) must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 6 “ V_{CCA} Power Supply Filter” must have a resistance of 270 Ω ($V_{CC}=3.3V$) or 9-10 Ω ($V_{CC}=2.5V$) to meet the voltage drop criteria.

$R_F = 270\Omega$ for $V_{CC} = 3.3V$
 $R_F = 9-10\Omega$ for $V_{CC} = 2.5V$

$C_F = 1\mu F$ for $V_{CC} = 3.3V$
 $C_F = 22\mu F$ for $V_{CC} = 2.5V$

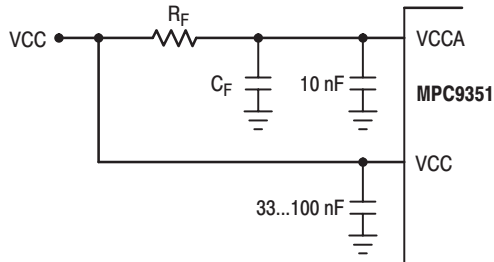


Figure 6. V_{CCA} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 6 “ V_{CCA} Power Supply Filter”, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9351 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC9351 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC}+2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9351 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 7 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9351 clock driver is effectively doubled due to its capability to drive multiple lines.

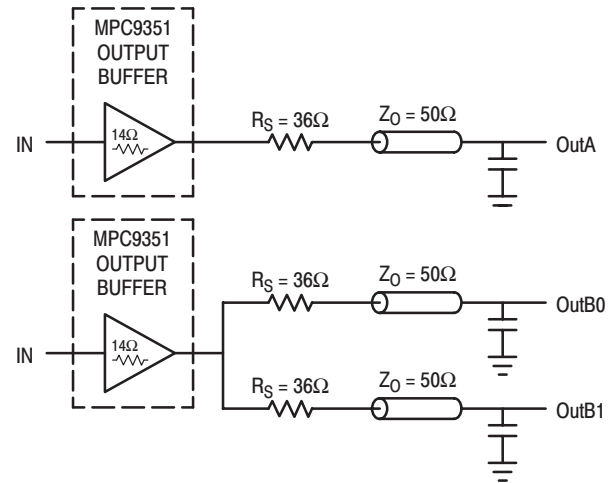


Figure 7. Single versus Dual Transmission Lines

The waveform plots in Figure 8 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9351 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9351. The output waveform in Figure 8 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned}
 V_L &= V_S (Z_0 \div (R_S + R_0 + Z_0)) \\
 Z_0 &= 50\Omega \parallel 50\Omega \\
 R_S &= 36\Omega \parallel 36\Omega \\
 R_0 &= 14\Omega \\
 V_L &= 3.0 (25 \div (18 + 17 + 25)) \\
 &= 1.31V
 \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

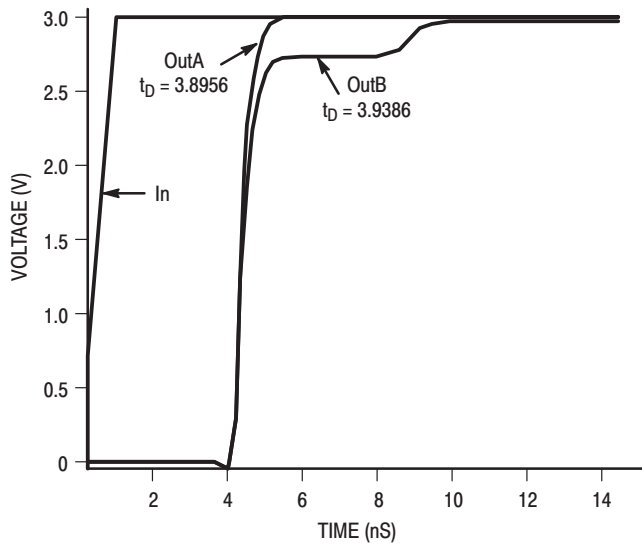


Figure 8. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be

uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 9 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

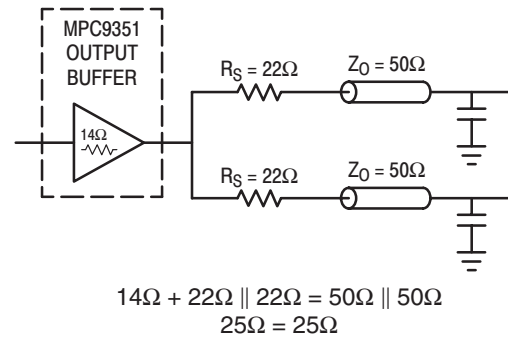


Figure 9. Optimized Dual Line Termination

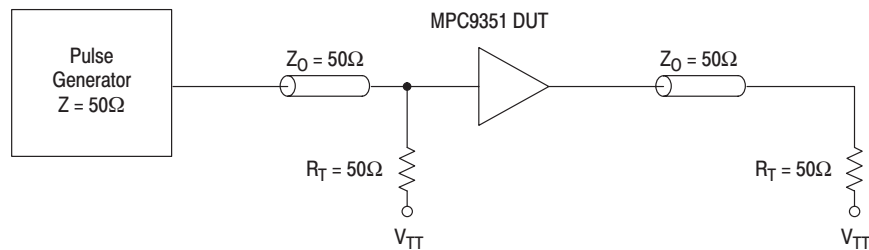
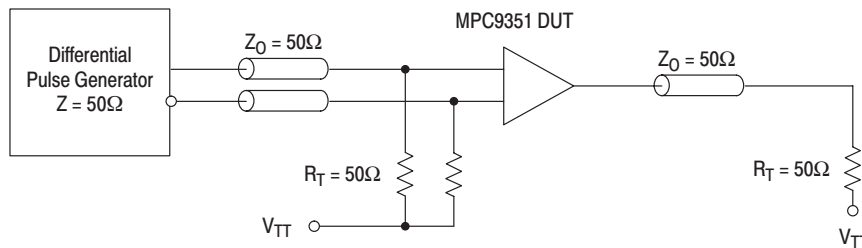
Figure 10. TCLK MPC9351 AC test reference for $V_{CC} = 3.3V$ and $V_{CC} = 2.5V$ 

Figure 11. PCLK MPC9351 AC test reference

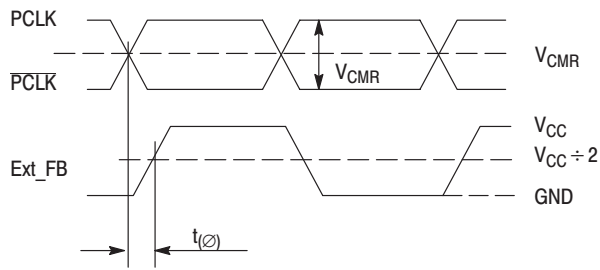


Figure 12. Propagation delay (t_{PD} , static phase offset) test reference

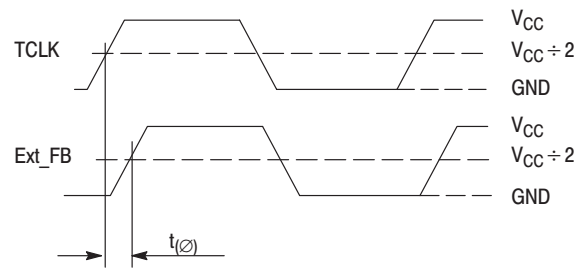
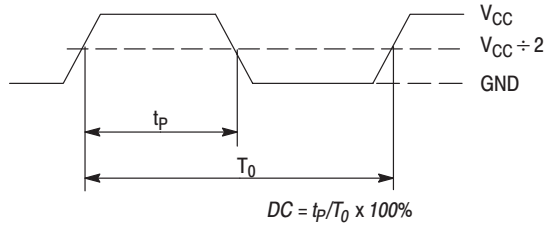
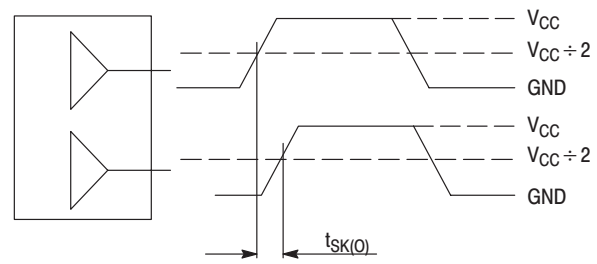


Figure 13. Propagation delay (t_{PD}) test reference



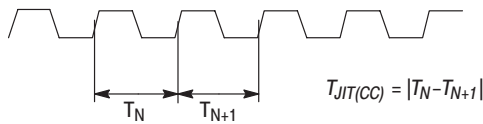
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 14. Output Duty Cycle (DC)



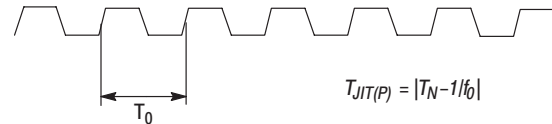
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 15. Output-to-output Skew $t_{SK(O)}$



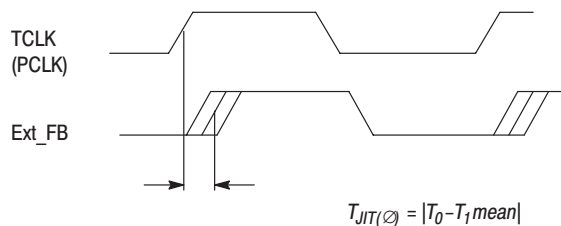
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 16. Cycle-to-cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 17. Period Jitter



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 18. I/O Jitter

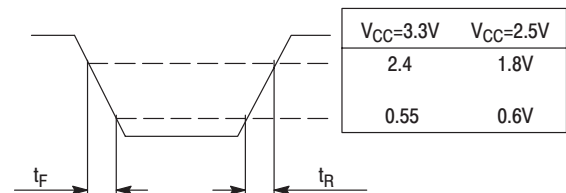


Figure 19. Transition Time Test Reference

3.3V/2.5V 1:11 LVCMOS Zero Delay Clock Generator

The MPC9352 is a 3.3V or 2.5V compatible, 1:11 PLL based clock generator targeted for high performance clock tree applications. With output frequencies up to 200 MHz and output skews lower than 200 ps the device meets the needs of most demanding clock applications.

Features

- Configurable 11 outputs LVCMOS PLL clock generator
- Fully integrated PLL
- Wide range of output clock frequency of 16.67 MHz to 200 MHz
- Multiplication of the input reference clock frequency by 3, 2, 1, $3 \div 2$, $2 \div 3$, $1 \div 3$ and $1 \div 2$
- 2.5V and 3.3V LVCMOS compatible
- Maximum output skew of 200 ps
- Supports zero-delay applications
- Designed for high-performance telecom, networking and computing applications
- 32 lead LQFP package
- Ambient Temperature Range -40°C to $+85^{\circ}\text{C}$

Functional Description

The MPC9352 is a fully 3.3V or 2.5V compatible PLL clock generator and clock driver. The device has the capability to generate output clock signals of 16.67 to 200 MHz from external clock sources. The internal PLL optimized for its frequency range and does not require external loop filter components. One output of the MPC9352 has to be connected to the PLL feedback input FB_IN to close the external PLL feedback path. The output divider of this output setting determines the PLL frequency multiplication factor. This multiplication factor, F_RANGE and the reference clock frequency must be selected to situate the VCO in its specified lock range. The frequency of the clock outputs can be configured individually for all three output banks by the FSELx pins supporting systems with different but phase-aligned clock frequencies.

The PLL of the MPC9352 minimizes the propagation delay and therefore supports zero-delay applications. All inputs and outputs are LVCMOS compatible. The outputs are optimized to drive parallel terminated 50Ω transmission lines. Alternatively, each output can drive up to two series terminated transmission lines giving the device an effective fanout of 22.

The device also supports output high-impedance disable and a PLL bypass mode for static system test and diagnosis. The MPC9352 is package in a 32 ld LQFP.

MPC9352**LOW VOLTAGE
3.3V/2.5V LVCMOS 1:11
CLOCK GENERATOR****FA SUFFIX
32 LEAD LQFP PACKAGE
CASE 873A****2**

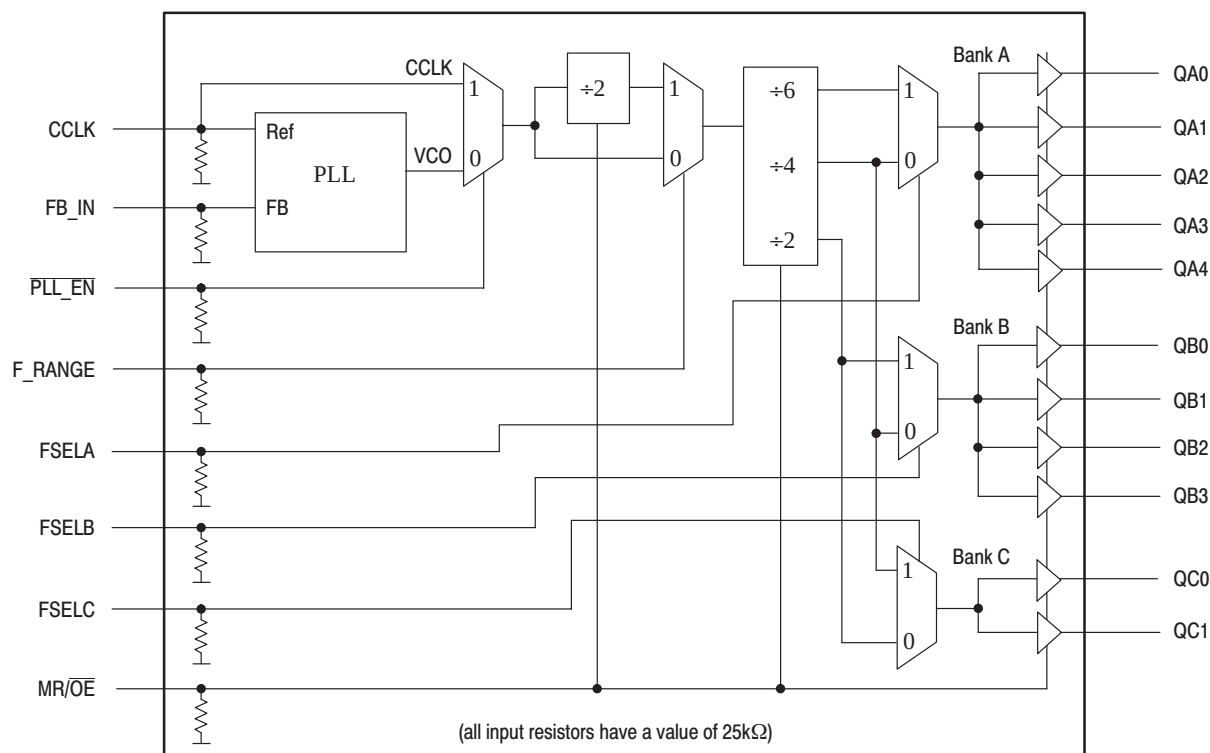
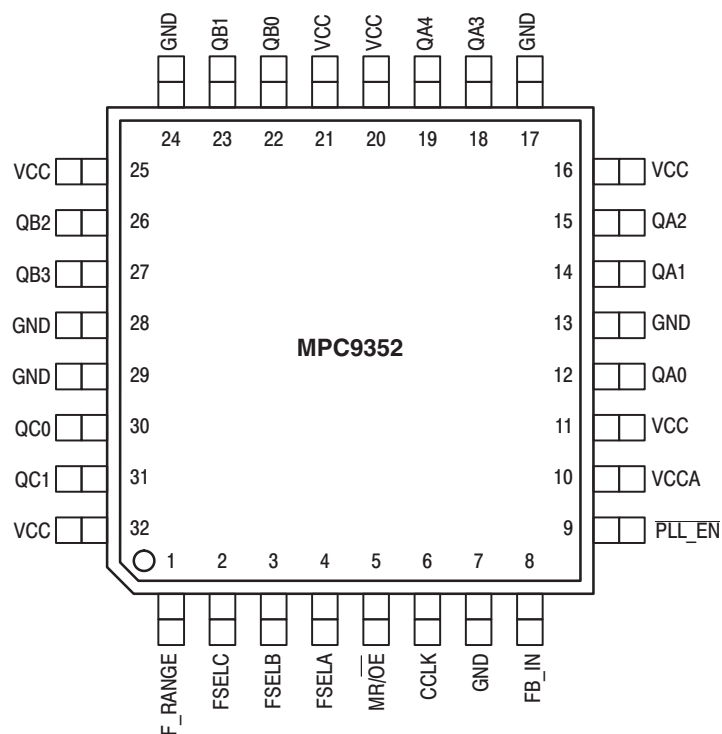


Figure 1. MPC9352 Logic Diagram



It is recommended to use an external RC filter for the analog power supply pin VCCA. Please see application section for details.

Figure 2. MPC9352 32-Lead Package Pinout (Top View)

Table 1: PIN CONFIGURATION

Pin	I/O	Type	Function
CCLK	Input	LVC MOS	PLL reference clock signal
FB_IN	Input	LVC MOS	PLL feedback signal input, connect to an output
F_RANGE	Input	LVC MOS	PLL frequency range select
FSELA	Input	LVC MOS	Frequency divider select for bank A outputs
FSELB	Input	LVC MOS	Frequency divider select for bank B outputs
FSELC	Input	LVC MOS	Frequency divider select for bank C outputs
PLL_EN	Input	LVC MOS	PLL enable/disable
MR/OE	Input	LVC MOS	Output enable/disable (high-impedance tristate) and device reset
QA0–4, QB0–3, QC0–1	Output	LVC MOS	Clock outputs
GND	Supply	Ground	Negative power supply
VCCA	Supply	VCC	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin VCCA. Please see applications section for details.
VCC	Supply	VCC	Positive power supply for I/O and core

2

Table 2: FUNCTION TABLE

Control	Default	0	1
F_RANGE, FSELA, FSELB, and FSELC control the operating PLL frequency range and input/output frequency ratios. See Table 1 and Table 2 for supported frequency ranges and output to input frequency ratios.			
F_RANGE	0	VCO ÷ 1 (High input frequency range)	VCO ÷ 2 (Low input frequency range)
FSELA	0	Output divider ÷ 4	Output divider ÷ 6
FSELB	0	Output divider ÷ 4	Output divider ÷ 2
FSELC	0	Output divider ÷ 2	Output divider ÷ 4
MR/OE	0	Outputs enabled (active)	Outputs disabled (high-impedance state) and reset of the device. During reset, the PLL feedback loop is open and the VCO is operating at its lowest frequency. The MPC9352 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than two reference clock cycles (CCLK).
PLL_EN	0	Normal operation mode with PLL enabled.	Test mode with PLL disabled. CCLK is substituted for the internal VCO output. MPC9352 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.

Table 3: GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 4: ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.6	V	
V_{IN}	DC Input Voltage	-0.3	$V_{CC}+0.3$	V	
V_{OUT}	DC Output Voltage	-0.3	$V_{CC}+0.3$	V	
I_{IN}	DC Input Current		± 20	mA	
I_{OUT}	DC Output Current		± 50	mA	
T_S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5: DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ$ to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	2.0		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input low voltage			0.8	V	LVC MOS
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -24 \text{ mA}^a$
V_{OL}	Output Low Voltage			0.55 0.30	V V	$I_{OL} = 24 \text{ mA}$ $I_{OL} = 12 \text{ mA}$
Z_{OUT}	Output impedance		14 - 17		Ω	
I_{IN}	Input Current ^b			± 200	μA	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$
I_{CCA}	Maximum PLL Supply Current		3.0	5.0	mA	V_{CCA} Pin
I_{CCQ}^c	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins

a. The MPC9352 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines.

b. Inputs have pull-down resistors affecting the input current.

c. I_{CCQ} is the DC current consumption of the device with all outputs open in high impedance state and the inputs in its default state or open.

Table 6: AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input reference frequency in PLL mode ^b +4 feedback	50.0		100.0	MHz	
	+6 feedback	33.3		66.6	MHz	
	+8 feedback	25.0		50.0	MHz	
	+12 feedback	16.67		33.3	MHz	
	Input reference frequency in PLL bypass mode ^c			250.0	MHz	
f_{VCO}	VCO lock frequency range ^d	200		400	MHz	
f_{MAX}	Output Frequency +2 output ^e	100		200	MHz	
	+4 output	50		100	MHz	
	+6 output	33.3		66.6	MHz	
	+8 output	25		50	MHz	
	+12 output	16.67		33.3	MHz	
f_{refDC}	Reference Input Duty Cycle	25		75	%	
t_r, t_f	CCLK Input Rise/Fall Time			1.0	ns	0.8 to 2.0V
$t_{(\phi)}$	Propagation Delay CCLK to FB_IN $f_{ref} > 40$ MHz (static phase offset) $f_{ref} < 40$ MHz	-50 -200		+150 +150	ps ps	PLL locked
$t_{sk(O)}$	Output-to-output Skew ^f all outputs, any frequency within QA output bank within QB output bank within QC output bank			200 200 100 100	ps ps ps ps	
DC	Output duty cycle	47	50	53	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time			8	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter output frequencies mixed RMS (1 σ) ^g outputs are in any +4 and +6 combination RMS (1 σ) all outputs same frequency RMS (1 σ)			400 250 100	ps ps ps	
$t_{JIT(PER)}$	Period Jitter output frequencies mixed RMS (1 σ) outputs are in any +4 and +6 combination RMS (1 σ) all outputs same frequency RMS (1 σ)			200 150 75	ps ps ps	
$t_{JIT(\phi)}$	I/O Phase Jitter +4 feedback divider RMS (1 σ) +6 feedback divider RMS (1 σ) +8 feedback divider RMS (1 σ) +12 feedback divider RMS (1 σ)		15 20 18 - 20 25		ps ps ps ps	
BW	PLL closed loop bandwidth ^h +4 feedback		3.0 - 10.0		MHz	
	+6 feedback		1.5 - 6.0		MHz	
	+8 feedback		1.0 - 3.5		MHz	
	+12 feedback		0.5 - 2.0		MHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

a AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b PLL mode requires $PLL\_EN=0$ to enable the PLL and zero-delay operation. It is not recommended to use a +2 divider for feedback.

c In PLL bypass mode, the MPC9352 divides the input reference clock.

d The input frequency f_{ref} on CCLK must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.

e See Table 9 and Table 10 for output divider configurations.

f See application section for part-to-part skew calculation.

g See application section for a jitter calculation for other confidence factors than 1 σ .

h -3 dB point of PLL transfer characteristics.

Table 7: DC CHARACTERISTICS ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40^\circ$ to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	1.7		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input low voltage	-0.3		0.7	V	LVC MOS
V_{OH}	Output High Voltage	1.8			V	$I_{OH} = -15\text{ mA}^a$
V_{OL}	Output Low Voltage			0.6	V	$I_{OL} = 15\text{ mA}$
Z_{OUT}	Output impedance		17 - 20		Ω	
I_{IN}	Input Current			± 200	μA	$V_{IN} = V_{CC}$ or GND
I_{CCA}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CCA} Pin
I_{CCQ}^b	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins

- a The MPC9352 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.
- b I_{CCQ} is the DC current consumption of the device with all outputs open in high impedance state and the inputs in its default state or open.

Table 8: AC CHARACTERISTICS ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input reference frequency in PLL mode ^b +4 feedback	50.0		100.0	MHz	
	+6 feedback	33.3		66.6	MHz	
	+8 feedback	25.0		50.0	MHz	
	+12 feedback	16.67		33.3	MHz	
	Input reference frequency in PLL bypass mode ^c			250.0	MHz	
f_{VCO}	VCO lock frequency range ^d	200		400	MHz	
f_{MAX}	Output Frequency +2 output ^e	100		200	MHz	
	+4 output	50		100	MHz	
	+6 output	33.3		66.6	MHz	
	+8 output	25		50	MHz	
	+12 output	16.67		33.3	MHz	
f_{refDC}	Reference Input Duty Cycle	25		75	%	
t_r, t_f	CCLK Input Rise/Fall Time			1.0	ns	0.8 to 2.0V
$t_{(\phi)}$	Propagation Delay CCLK to FB_IN $f_{ref} > 40$ MHz (static phase offset) $f_{ref} < 40$ MHz	-50 -200		+150 +150	ps ps	PLL locked
$t_{sk(O)}$	Output-to-output Skew ^f all outputs, any frequency within QA output bank within QB output bank within QC output bank			200 200 100 100	ps ps ps ps	
DC	Output duty cycle	47	50	53	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.6 to 1.8V
$t_{PLZ, HZ}$	Output Disable Time			8	ns	
$t_{PZL, ZH}$	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter output frequencies mixed RMS (1 σ) ^g outputs are in any +4 and +6 combination RMS (1 σ) all outputs same frequency RMS (1 σ)			400 250 100	ps ps ps	
$t_{JIT(PER)}$	Period Jitter output frequencies mixed RMS (1 σ) outputs are in any +4 and +6 combination RMS (1 σ) all outputs same frequency RMS (1 σ)			200 150 75	ps ps ps	
$t_{JIT(\phi)}$	I/O Phase Jitter +4 feedback divider RMS (1 σ) +6 feedback divider RMS (1 σ) +8 feedback divider RMS (1 σ) +12 feedback divider RMS (1 σ)		15 20 18 - 20 25		ps ps ps ps	
BW	PLL closed loop bandwidth ^h +4 feedback		1.0 - 8.0		MHz	
	+6 feedback		0.7 - 3.0		MHz	
	+8 feedback		0.5 - 2.5		MHz	
	+12 feedback		0.4 - 1.0		MHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

a AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b PLL mode requires $PLL\_EN=0$ to enable the PLL and zero-delay operation. It is not recommended to use a +2 divider for feedback.

c In PLL bypass mode, the MPC9352 divides the input reference clock.

d The input frequency f_{ref} on CCLK must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.

e See Table 9 and Table 10 for output divider configurations.

f See application section for part-to-part skew calculation.

g See application section for a jitter calculation for other confidence factors than 1 σ .

h -3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Programming the MPC9352

The MPC9352 supports output clock frequencies from 16.67 to 200 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency lock range between 200 and 400 MHz for stable and optimal operation.

The FSELA, FSELB, FSELC pins select the desired output clock frequencies. Possible frequency ratios of the reference clock input to the outputs are 1:1, 1:2, 1:3, 3:2 as well as 2:3, 3:1 and 2:1. Table 1 illustrates the various output configurations and frequency ratios supported by the MPC9352. See also Table 9, Table 10 and Figure 3 to Figure 6 for further reference. A +2 output divider cannot be used for feedback.

Table 9: MPC9352 Example Configuration (F_RANGE = 0)

PLL Feedback	fref ^a [MHz]	FSELA	FSELB	FSELC	QA[0:4]:fref ratio	QB[0:3]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 4 ^b	50-100	0	0	0	fref (50-100 MHz)	fref (50-100 MHz)	fref · 2 (100-200 MHz)
		0	0	1	fref (50-100 MHz)	fref (50-100 MHz)	fref (50-100 MHz)
		1	0	0	fref · 2÷3 (33-66 MHz)	fref (50-100 MHz)	fref · 2 (100-200 MHz)
		1	0	1	fref · 2÷3 (33-66 MHz)	fref (50-100 MHz)	fref (50-100 MHz)
VCO ÷ 6 ^c	33.3-66.67	1	0	0	fref (33-66 MHz)	fref · 3÷2 (50-100 MHz)	fref · 3 (100-200 MHz)
		1	0	1	fref (33-66 MHz)	fref · 3÷2 (50-100 MHz)	fref · 3÷2 (50-100 MHz)
		1	1	0	fref (33-66 MHz)	fref · 3 (100-200 MHz)	fref · 3 (100-200 MHz)
		1	1	1	fref (33-66 MHz)	fref · 3 (100-200 MHz)	fref · 3÷2 (50-100 MHz)

a. fref is the input clock reference frequency (CCLK)

b. QAx connected to FB_IN and FSELA=0

c. QAx connected to FB_IN and FSELA=1

Table 10: MPC9352 Example Configurations (F_RANGE = 1)

PLL Feedback	fref ^a [MHz]	FSELA	FSELB	FSELC	QA[0:4]:fref ratio	QB[0:3]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 8 ^b	25-50	0	0	0	fref (25-50 MHz)	fref (25-50 MHz)	fref · 2 (50-100 MHz)
		0	0	1	fref (25-50 MHz)	fref (25-50 MHz)	fref (25-50 MHz)
		1	0	0	fref · 2÷3 (16-33 MHz)	fref (25-50 MHz)	fref · 2 (50-100 MHz)
		1	0	1	fref · 2÷3 (16-33 MHz)	fref (25-50 MHz)	fref (25-50 MHz)
VCO ÷ 12 ^c	16.67-33.3	1	0	0	fref (16-33 MHz)	fref · 3÷2 (25-50 MHz)	fref · 3 (50-100 MHz)
		1	0	1	fref (16-33 MHz)	fref · 3÷2 (25-50 MHz)	fref · 3÷2 (25-50 MHz)
		1	1	0	fref (16-33 MHz)	fref · 3 (50-100 MHz)	fref · 3 (50-100 MHz)
		1	1	1	fref (16-33 MHz)	fref · 3 (50-100 MHz)	fref · 3÷2 (25-50 MHz)

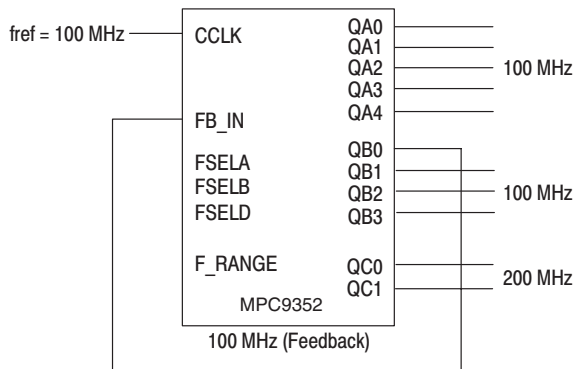
a. fref is the input clock reference frequency (CCLK)

b. QAx connected to FB_IN and FSELA=0

c. QAx connected to FB_IN and FSELA=1

Example Configurations for the MPC9352

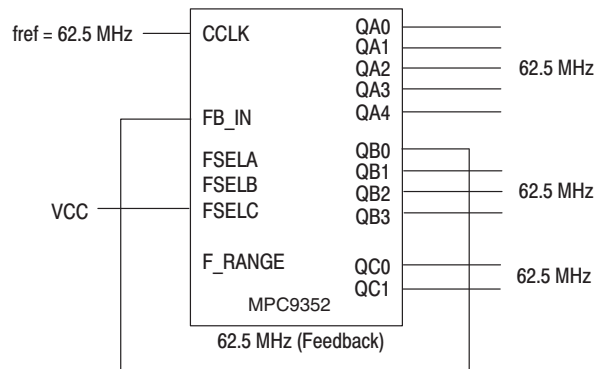
Figure 3. MPC9352 Default Configuration



MPC9352 default configuration (feedback of QB0 = 100 MHz). All control pins are left open.

Frequency range	Min	Max
Input	50 MHz	100 MHz
QA outputs	50 MHz	10 MHz
QB outputs	50 MHz	100 MHz
QC outputs	100 MHz	200 MHz

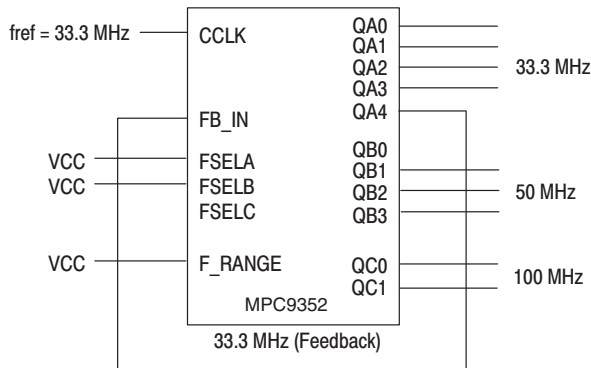
Figure 4. MPC9352 Zero Delay Buffer Configuration



MPC9352 zero-delay (feedback of QB0 = 62.5 MHz). All control pins are left open except FSEL C = 1. All outputs are locked in frequency and phase to the input clock.

Frequency range	Min	Max
Input	50 MHz	100 MHz
QA outputs	50 MHz	10 MHz
QB outputs	50 MHz	100 MHz
QC outputs	50 MHz	100 MHz

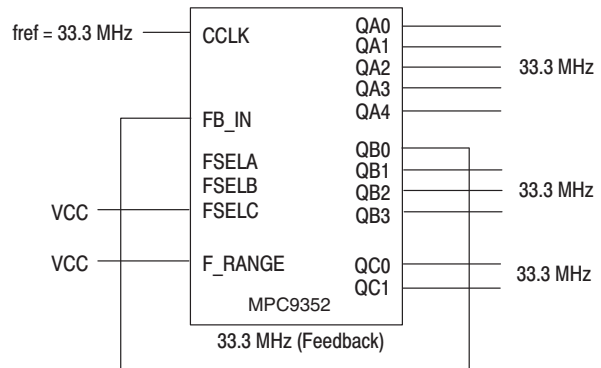
Figure 5. MPC9352 Default Configuration



MPC9352 configuration to multiply the reference frequency by 3, 3÷2 and 1. PLL feedback of QA4 = 33.3 MHz.

Frequency range	Min	Max
Input	25 MHz	50 MHz
QA outputs	50 MHz	10 MHz
QB outputs	50 MHz	100 MHz
QC outputs	100 MHz	200 MHz

Figure 6. MPC9352 Zero Delay Buffer Config. 2



MPC9352 zero-delay (feedback of QB0 = 33.3 MHz). Equivalent to Table 2 except F_RANGE = 1 enabling a lower input and output clock frequency.

Frequency range	Min	Max
Input	25 MHz	50 MHz
QA outputs	25 MHz	50 MHz
QB outputs	25 MHz	50 MHz
QC outputs	25 MHz	50 MHz

Power Supply Filtering

The MPC9352 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9352 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC9352. Figure 7 illustrates a typical power supply filter scheme. The MPC9352 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F . From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V ($V_{CC}=3.3V$ or $V_{CC}=2.5V$) must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 7 “ V_{CCA} Power Supply Filter” should have a resistance of 5–15 Ω ($V_{CC}=3.3V$) or 9–10 Ω ($V_{CC}=2.5V$) to meet the voltage drop criteria.

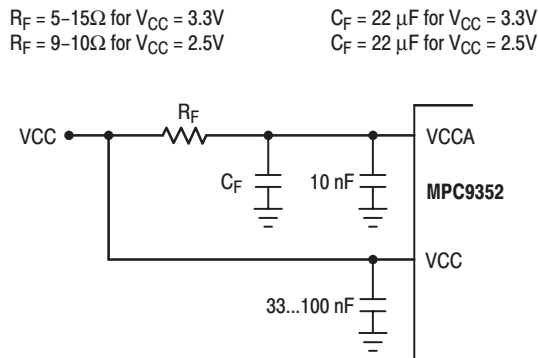


Figure 7. V_{CCA} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 7 “ V_{CCA} Power Supply Filter”, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9352 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power

supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9352 in zero-delay applications

Nested clock trees are typical applications for the MPC9352. Designs using the MPC9352 as LVCMOS PLL fan-out buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fan-out buffers. The external feedback option of the MPC9352 clock driver allows for its use as a zero delay buffer. One example configuration is to use a +4 output as a feedback to the PLL and configuring all other outputs to a divide-by-4 mode. The propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of part-to-part skew

The MPC9352 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9352 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD, LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

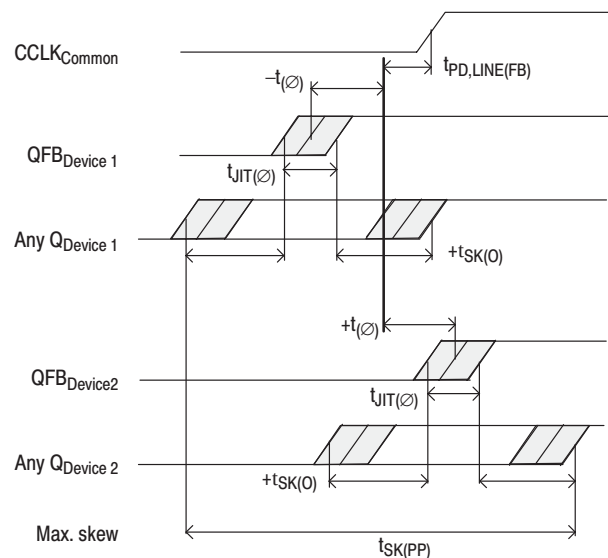


Figure 8. MPC9352 max. device-to-device skew

Due to the statistical nature of I/O jitter a RMS value (1σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 11.

Table 11: Confidence Factor CF

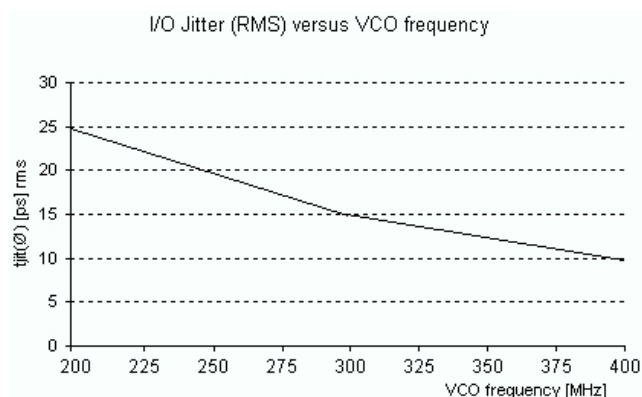
CF	Probability of clock edge within the distribution
$\pm 1\sigma$	0.68268948
$\pm 2\sigma$	0.95449988
$\pm 3\sigma$	0.99730007
$\pm 4\sigma$	0.99993663
$\pm 5\sigma$	0.99999943
$\pm 6\sigma$	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% ($\pm 3\sigma$) is assumed, resulting in a worst case timing uncertainty from input to any output of -445 ps to 395 ps relative to CCLK:

$$t_{SK(PP)} = [-200ps...150ps] + [-200ps...200ps] + [(15ps \cdot -3)...(15ps \cdot 3)] + t_{PD, LINE(FB)}$$

$$t_{SK(PP)} = [-445ps...395ps] + t_{PD, LINE(FB)}$$

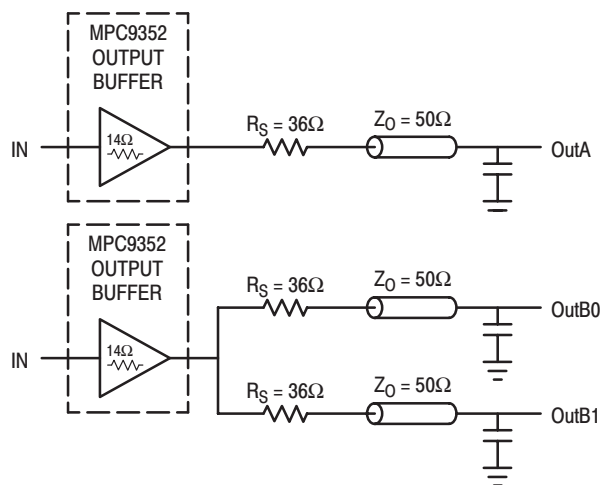
Due to the frequency dependence of the I/O jitter, Figure 9 “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis.

**Figure 9. Max. I/O Jitter versus frequency**

Driving Transmission Lines

The MPC9352 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}+2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9352 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 10 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9352 clock driver is effectively doubled due to its capability to drive multiple lines.

**Figure 10. Single versus Dual Transmission Lines**

The waveform plots in Figure 11 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9352 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9352. The output waveform in Figure 11 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned} V_L &= V_S (Z_0 \div (R_S + R_0 + Z_0)) \\ Z_0 &= 50\Omega \parallel 50\Omega \\ R_S &= 36\Omega \parallel 36\Omega \\ R_0 &= 14\Omega \\ V_L &= 3.0 (25 \div (18+17+25)) \\ &= 1.31V \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

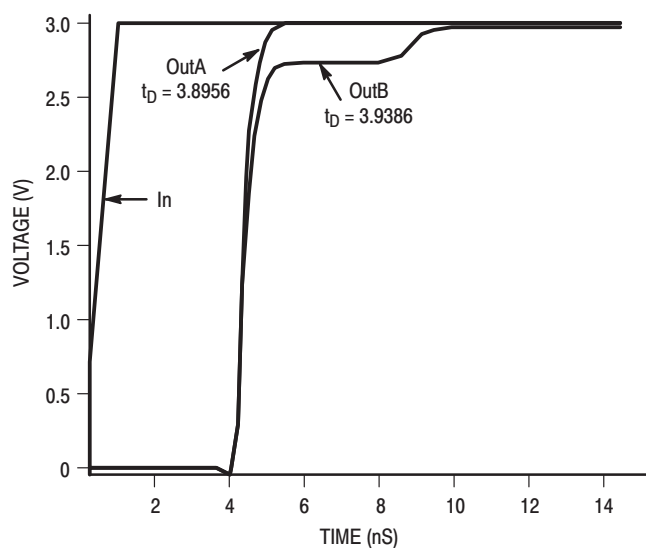


Figure 11. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be

uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 12 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

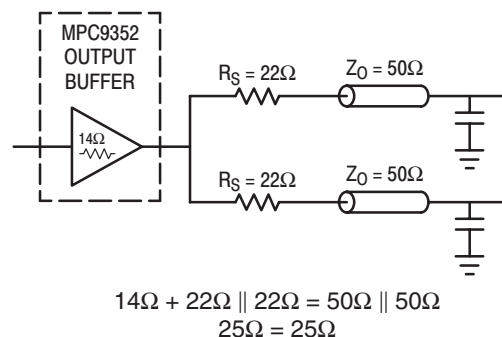
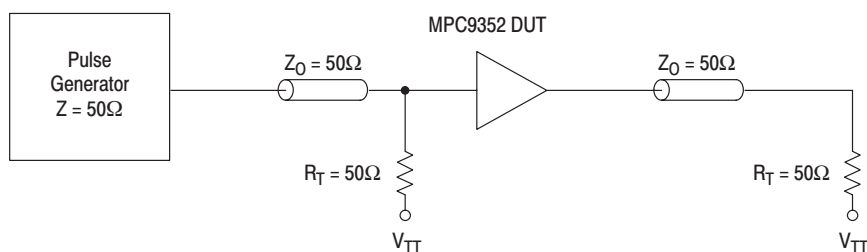
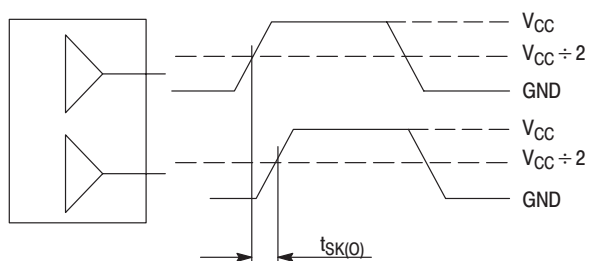


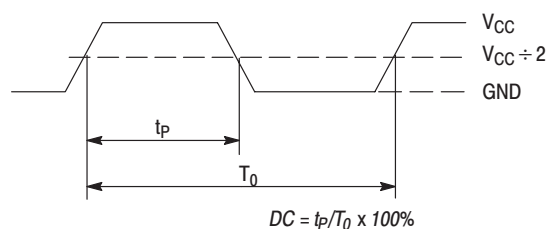
Figure 12. Optimized Dual Line Termination

Figure 13. CCLK MPC9352 AC test reference for $V_{CC} = 3.3V$ and $V_{CC} = 2.5V$



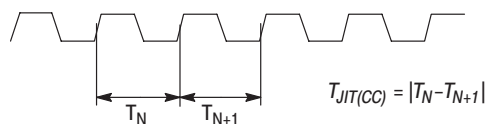
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 14. Output-to-output Skew $t_{SK(O)}$



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 16. Output Duty Cycle (DC)



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 18. Cycle-to-cycle Jitter

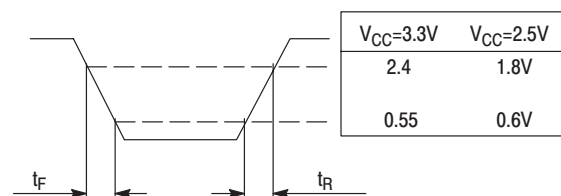


Figure 20. Output Transition Time Test Reference

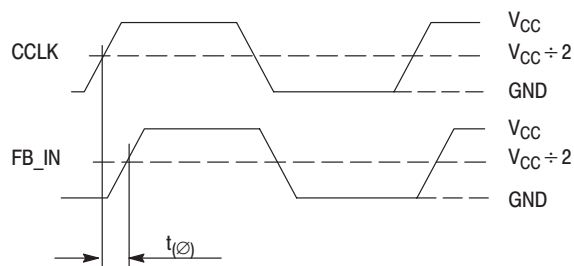
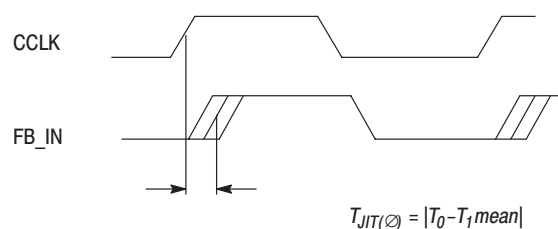
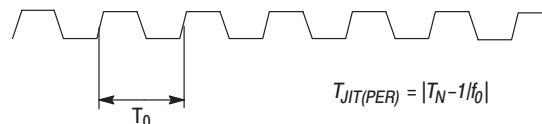


Figure 15. Propagation delay ($t_{(\phi)}$, static phase offset) test reference



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 17. I/O Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 19. Period Jitter

2

Low Voltage PLL Clock Driver

The MPC93R51 is a 3.3V compatible, PLL based clock generator targeted for high performance clock distribution systems. With output frequencies of up to 240 MHz and a maximum output skew of 150 ps the MPC93R51 is an ideal solution for the most demanding clock tree designs. The device offers 9 low skew clock outputs, each is configurable to support the clocking needs of the various high-performance microprocessors including the PowerQuicc II integrated communication microprocessor. The device employs a fully differential PLL design to minimize cycle-to-cycle and long-term jitter.

Features

- 9 outputs LVCMOS PLL clock generator
- 25 - 240 MHz output frequency range
- Fully integrated PLL
- Compatible to various microprocessors such as PowerQuicc II
- Supports networking, telecommunications and computer applications
- Configurable outputs: divide-by-2, 4 and 8 of VCO frequency
- LVPECL and LVCMOS compatible inputs
- External feedback enables zero-delay configurations
- Output enable/disable and static test mode (PLL enable/disable)
- Low skew characteristics: maximum 150 ps output-to-output
- Cycle-to-cycle jitter max. 22 ps RMS
- 32 lead LQFP package
- Ambient Temperature Range 0°C to +70°C
- Pin & Function Compatible with the MPC951

Functional Description

The MPC93R51 utilizes PLL technology to frequency and phase lock its outputs onto an input reference clock. Normal operation of the MPC93R51 requires a connection of one of the device outputs to the EXT_FB input to close the PLL feedback path. The reference clock frequency and the output divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. With available output dividers of divide-by-4 and divide-by-8 the internal VCO of the MPC93R51 is running at either 4x or 8x of the reference clock frequency. The frequency of the QA, QB, QC and QD outputs is either the one half, one fourth or one eighth of the selected VCO frequency and can be configured for each output bank using the FSELA, FSELB, FSELC and FSELD pins, respectively. The available output to input frequency ratios are 4:1, 2:1, 1:1, 1:2 and 1:4. The REF_SEL pin selects the differential LVPECL (PCLK and PCLK) or the LVCMOS compatible reference input (TCLK). The MPC93R51 also provides a static test mode when the PLL enable pin (PLL_EN) is pulled to logic low state. In test mode, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The test mode is intended for system diagnostics, test and debug purpose. This test mode is fully static and the minimum clock frequency specification does not apply. The outputs can be disabled by deasserting the OE pin (logic high state). In PLL mode, deasserting OE causes the PLL to lose lock due to no feedback signal presence at EXT_FB. Asserting OE will enable the outputs and close the phase locked loop, also enabling the PLL to recover to normal operation. The MPC93R51 is 3.3V compatible and requires no external loop filter components. All inputs except PCLK and PCLK accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC93R51 outputs can drive one or two traces giving the device an effective fanout of 1:18. The device is packaged in a 7x7 mm² 32-lead LQFP package.

Application Information

The fully integrated PLL of the MPC93R51 allows the low skew outputs to lock onto a clock input and distribute it with essentially zero propagation delay to multiple components on the board. In zero-delay buffer mode, the PLL minimizes phase offset between the outputs and the reference signal.

MPC93R51

**LOW VOLTAGE 3.3V
PLL CLOCK GENERATOR**



FA SUFFIX
LQFP PACKAGE
CASE 873A



Pin diagram of the MPC93R51 integrated circuit. The chip is a square package with pins numbered 1 to 32. The top pins (17-24) are labeled QC0, VCCO, QC1, GND, QD0, VCCO, QD1, and GND. The right pins (9-16) are labeled QD2, VCCO, QD3, GND, QD4, VCCO, OE, and PCLK. The bottom pins (1-8) are labeled VCCA, EXT_FB, FSEL A, FSEL B, FSEL C, FSEL D, GND, and PCLK. The left pins (31-25) are labeled REF_SEL, PLL_EN, TCLK, GND, QA, QB, and GND. The chip is labeled 'MPC93R51' in the center.

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PIN CONFIGURATION

Pin	I/O	Type	Function
PCLK, $\overline{\text{PCLK}}$	Input	LVPECL	Differential clock reference Low voltage positive ECL input
TCLK	Input	LVC MOS	Single ended reference clock signal or test clock
EXT_FB	Input	LVC MOS	Feedback signal input, connect to a QA, QB, QC, QD output
REF_SEL	Input	LVC MOS	Selects input reference clock
FSELA	Input	LVC MOS	Output A divider selection
FSELB	Input	LVC MOS	Output B divider selection
FSELC	Input	LVC MOS	Outputs C divider selection
FSELD	Input	LVC MOS	Outputs D divider selection
$\overline{\text{OE}}$	Input	LVC MOS	Output enable/disable
QA	Output	LVC MOS	Bank A clock output
QB	Output	LVC MOS	Bank B clock output
QC0, QC1	Output	LVC MOS	Bank C clock outputs
QD0 - QD4	Output	LVC MOS	Bank D clock outputs
VCCA	Supply	VCC	Positive power supply for the PLL
VCC	Supply	VCC	Positive power supply for I/O and core
GND	Supply	Ground	Negative power supply

FUNCTION TABLE

Control	Default	0	1
REF_SEL	0	Selects PCLK as reference clock	Selects TCLK as reference clock
PLL_EN	1	Test mode with PLL disabled. The input clock is directly routed to the output dividers	PLL enabled. The VCO output is routed to the output dividers
$\overline{\text{OE}}$	0	Outputs enabled	Outputs disabled, PLL loop is open VCO is forced to its minimum frequency
FSELA	0	$\text{QA} = \text{VCO} \div 2$	$\text{QA} = \text{VCO} \div 4$
FSELB	0	$\text{QB} = \text{VCO} \div 4$	$\text{QB} = \text{VCO} \div 8$
FSELC	0	$\text{QC} = \text{VCO} \div 4$	$\text{QC} = \text{VCO} \div 8$
FSELD	0	$\text{QD} = \text{VCO} \div 4$	$\text{QD} = \text{VCO} \div 8$

ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.9	V	
V_{IN}	DC Input Voltage	-0.3	$V_{\text{CC}}+0.3$	V	
V_{OUT}	DC Output Voltage	-0.3	$V_{\text{CC}}+0.3$	V	
I_{IN}	DC Input Current		± 20	mA	
I_{OUT}	DC Output Current		± 50	mA	
T_{S}	Storage Temperature	-55	150	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{\text{CC}} \div 2$		V	
MM	ESD (Machine Model)	200			V	
HBM	ESD (Human Body Model)	2000			V	
LU	Latch-Up	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}			4.0		pF	Inputs

DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ$ to 70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input Low Voltage			0.8	V	LVC MOS
V_{PP}	Peak-to-Peak Input Voltage PCLK, $\overline{\text{PCLK}}$	250			mV	LVPECL
V_{CMR}^a	Common Mode Range PCLK, $\overline{\text{PCLK}}$	1.0		$V_{CC}-0.6$	V	LVPECL
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -24\text{ mA}^b$
V_{OL}	Output Low Voltage			0.55 0.30	V V	$I_{OL} = 24\text{ mA}$ $I_{OL} = 12\text{ mA}$
Z_{OUT}	Output Impedance		14 - 17		Ω	
I_{IN}	Input Leakage Current			± 200	μA	$V_{IN} = V_{CC}$ or GND
I_{CCA}	Maximum PLL Supply Current		3.0	5.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current		7.0	10	mA	All V_{CC} Pins

- a. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
- b. The MPC93R51 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines.

AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ$ to 70°C)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency ^b ÷ 4 feedback ÷ 8 feedback Static test mode	50 25 0		120 60 300	MHz MHz MHz	PLL_EN = 1 PLL_EN = 1 PLL_EN = 0
f_{VCO}	VCO Frequency	200		480	MHz	
f_{MAX}	Maximum Output Frequency ^b ÷ 2 output ÷ 4 output ÷ 8 output	100 50 25		240 120 60	MHz MHz MHz	
f_{refDC}	Reference Input Duty Cycle	25		75	%	
V_{PP}	Peak-to-Peak Input Voltage PCLK, $\overline{\text{PCLK}}$	500		1000	mV	LVPECL
V_{CMR}^c	Common Mode Range PCLK, $\overline{\text{PCLK}}$	1.2		$V_{CC}-0.9$	V	LVPECL
t_r, t_f^d	TCLK Input Rise/Fall Time			1.0	ns	0.8 to 2.0V
$t_{(\phi)}$	Propagation Delay (static phase offset) TCLK to EXT_FB PCLK to EXT_FB	-50 +25		+150 +325	ps ps	PLL locked PLL locked
$t_{sk(o)}$	Output-to-Output Skew			150	ps	
DC	Output Duty Cycle 100 – 240 MHz 50 – 120 MHz 25 – 60 MHz	45 47.5 48.75	50 50 50	55 52.5 51.75	% % %	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time			7.0	ns	
$t_{PZL, ZH}$	Output Enable Time			6.0	ns	
BW	PLL closed loop bandwidth ÷ 4 feedback ÷ 8 feedback		3.0 – 9.5 1.2 – 2.1		MHz MHz	-3 db point of PLL transfer characteristic
$t_{JIT(CC)}$	Cycle-to-cycle jitter Single Output Frequency Configuration ÷ 4 feedback		10	22	ps	RMS value
$t_{JIT(PER)}$	Period Jitter Single Output Frequency Configuration ÷ 4 feedback		8.0	15	ps	RMS value
$t_{JIT(\phi)}$	I/O Phase Jitter		4.0 – 17		ps	RMS value
t_{LOCK}	Maximum PLL Lock Time			1.0	ms	

- a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
- b. The PLL will be unstable with a divide by 2 feedback ratio.
- c. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\phi)}$.
- d. The MPC93R51 will operate with input rise/fall times up to 3.0 ns, but the AC characteristics, specifically $t_{(\phi)}$, can only be guaranteed if t_r/t_f are within the specified range.

APPLICATIONS INFORMATION

Programming the MPC93R51

The MPC93R51 clock driver outputs can be configured into several divider modes, in addition the external feedback of the device allows for flexibility in establishing various input to output frequency relationships. The output divider of the four output groups allows the user to configure the outputs into 1:1, 2:1, 4:1 and 4:2:1 frequency ratios. The use of even dividers ensure that the output duty cycle is always 50%. “Output Frequency Relationship for an Example Configuration” illustrates

the various output configurations, the table describes the outputs using the input clock frequency CLK as a reference.

The output division settings establish the output relationship, in addition, it must be ensured that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL supports output frequencies from 25 MHz to 240 MHz while the VCO frequency range is specified from 200 MHz to 480 MHz and should not be exceeded for stable operation.

Output Frequency Relationship^a for an Example Configuration

Inputs				Outputs			
FSELA	FSELB	FSELC	FSELD	QA	QB	QC	QD
0	0	0	0	2 * CLK	CLK	CLK	CLK
0	0	0	1	2 * CLK	CLK	CLK	CLK ÷ 2
0	0	1	0	4 * CLK	2 * CLK	CLK	2 * CLK
0	0	1	1	4 * CLK	2 * CLK	CLK	CLK
0	1	0	0	2 * CLK	CLK ÷ 2	CLK	CLK
0	1	0	1	2 * CLK	CLK ÷ 2	CLK	CLK ÷ 2
0	1	1	0	4 * CLK	CLK	CLK	2 * CLK
0	1	1	1	4 * CLK	CLK	CLK	CLK
1	0	0	0	CLK	CLK	CLK	CLK
1	0	0	1	CLK	CLK	CLK	CLK ÷ 2
1	0	1	0	2 * CLK	2 * CLK	CLK	2 * CLK
1	0	1	1	2 * CLK	2 * CLK	CLK	CLK
1	1	0	0	CLK	CLK ÷ 2	CLK	CLK
1	1	0	1	CLK	CLK ÷ 2	CLK	CLK ÷ 2
1	1	1	0	2 * CLK	CLK	CLK	2 * CLK
1	1	1	1	2 * CLK	CLK	CLK	CLK

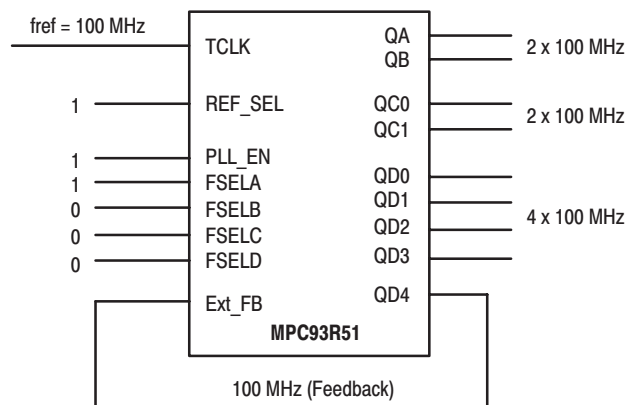
a. Output frequency relationship with respect to input reference frequency CLK. QC1 is connected to EXT_FB.

Using the MPC93R51 in zero-delay applications

Nested clock trees are typical applications for the MPC93R51. For these applications the MPC93R51 offers a differential LVPECL clock input pair as a PLL reference. This allows for the use of differential LVPECL primary clock distribution devices such as the Motorola MC100EP111 or MC10EP222, taking advantage of its superior low-skew performance. Clock trees using LVPECL for clock distribution and the MPC93R51 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers.

The external feedback option of the MPC93R51 PLL allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge and virtually eliminates the propagation delay through the device.

The remaining insertion delay (skew error) of the MPC93R51 in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset (SPO or t_{ϕ}), I/O jitter ($t_{JIT(\phi)}$, phase or long-term jitter), feedback path delay and the output-to-output skew ($t_{SK(O)}$) relative to the feedback output.



MPC93R51 zero-delay configuration (feedback of QD4)

Calculation of part-to-part skew

The MPC93R51 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs (TCLK or PCLK) of two or more MPC93R51 are connected together, the maxi-

imum overall timing uncertainty from the common TCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD, LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

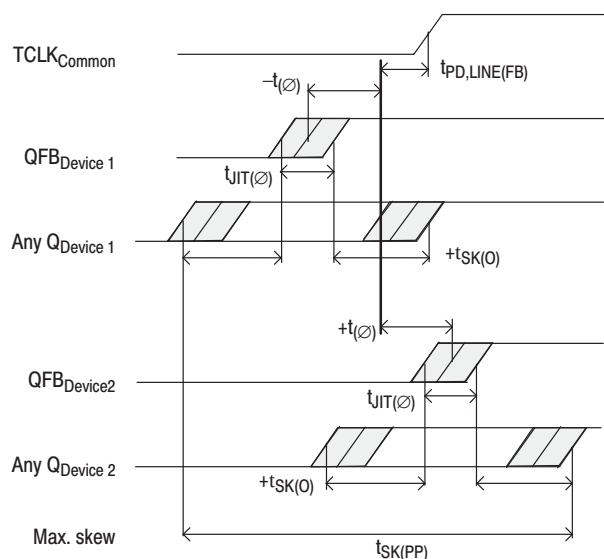


Figure 3. MPC93R51 max. device-to-device skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

Table 8: Confidence Factor CF

CF	Probability of clock edge within the distribution
$\pm 1\sigma$	0.68268948
$\pm 2\sigma$	0.95449988
$\pm 3\sigma$	0.99730007
$\pm 4\sigma$	0.99993663
$\pm 5\sigma$	0.99999943
$\pm 6\sigma$	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% ($\pm 3\sigma$) is assumed, resulting in a worst case timing uncertainty from input to any output of -251 ps to 351 ps relative to TCLK ($V_{CC}=3.3V$ and $f_{VCO} = 400$ MHz):

$$t_{SK(PP)} = [-50ps...150ps] + [-150ps...150ps] + [(17ps \cdot -3)...(17ps \cdot 3)] + t_{PD, LINE(FB)}$$

$$t_{SK(PP)} = [-251ps...351ps] + t_{PD, LINE(FB)}$$

Above equation uses the maximum I/O jitter number shown in the AC characteristic table for $V_{CC}=3.3V$ (17 ps RMS). I/O jitter is frequency dependant with a maximum at the lowest VCO frequency (200 MHz for the MPC93R51). Applications using a higher VCO frequency exhibit less I/O jitter than the AC characteristic limit. The I/O jitter characteristics in Figure 4 can be used to derive a smaller I/O jitter number at the specific VCO frequency, resulting in tighter timing limits in zero-delay mode and for part-to-part skew $t_{SK(PP)}$.

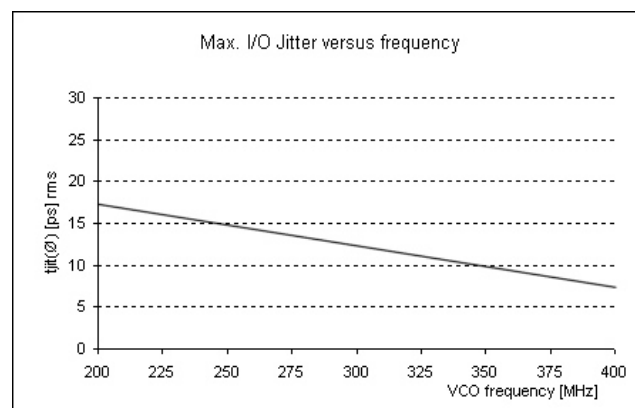


Figure 4. Max. I/O Jitter (RMS) versus frequency for $V_{CC}=3.3V$

Power Supply Filtering

The MPC93R51 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC93R51 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC93R51.

Figure 5 illustrates a typical power supply filter scheme. The MPC93R51 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F . From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 3.0V must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 5 "V_{CCA} Power Supply Filter" must have a resistance of 5–15 Ω to meet the voltage drop criteria.

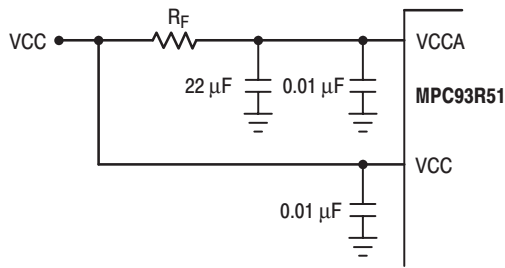


Figure 5. VCCA Power Supply Filter

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC93R51 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC93R51 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}/2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC93R51 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 6 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC93R51 clock driver is effectively doubled due to its capability to drive multiple lines.

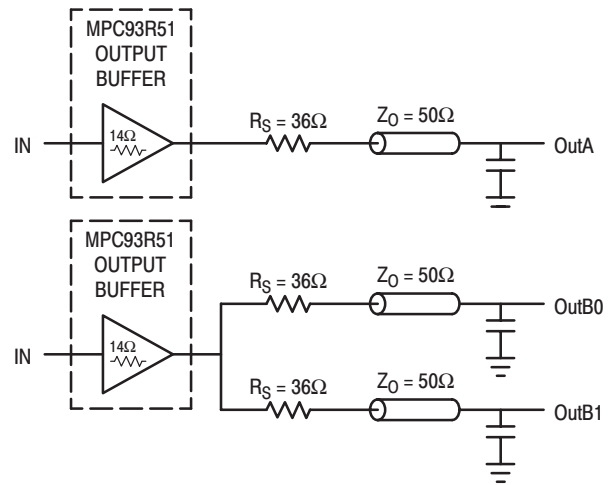


Figure 6. Single versus Dual Transmission Lines

The waveform plots in Figure 7 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC93R51 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC93R51. The output waveform in Figure 7 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned}
 V_L &= V_S (Z_0 \div (R_S + R_0 + Z_0)) \\
 Z_0 &= 50\Omega \parallel 50\Omega \\
 R_S &= 36\Omega \parallel 36\Omega \\
 R_0 &= 14\Omega \\
 V_L &= 3.0 (25 \div (18 + 17 + 25)) \\
 &= 1.31V
 \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

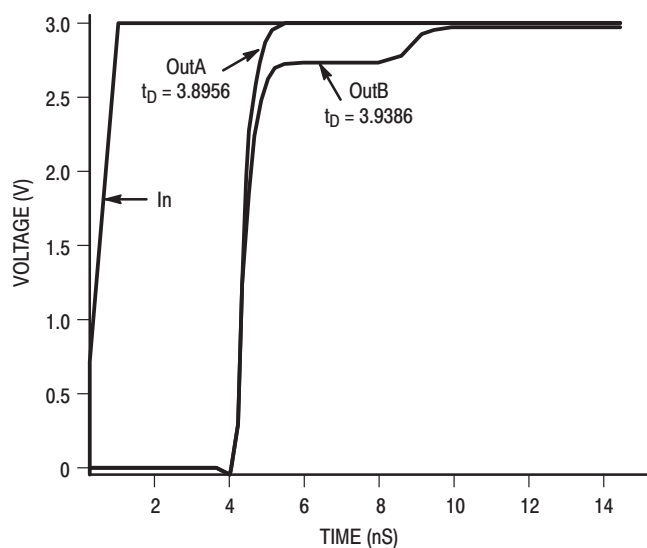


Figure 7. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be

uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 8 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

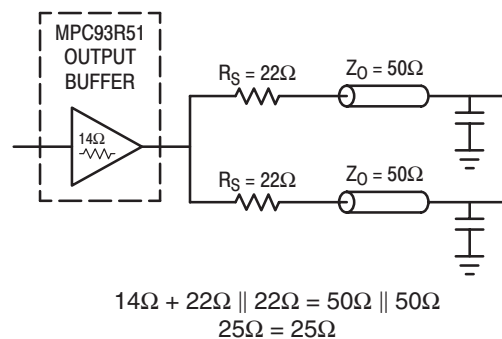


Figure 8. Optimized Dual Line Termination

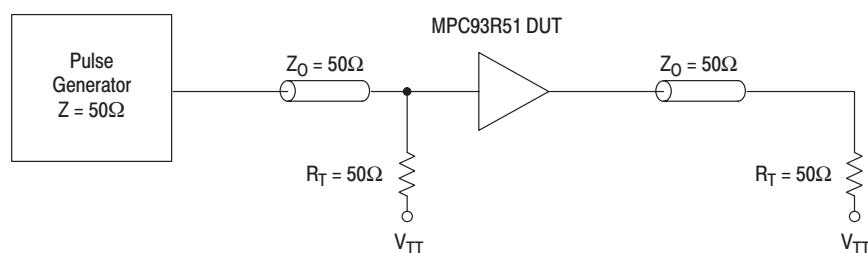
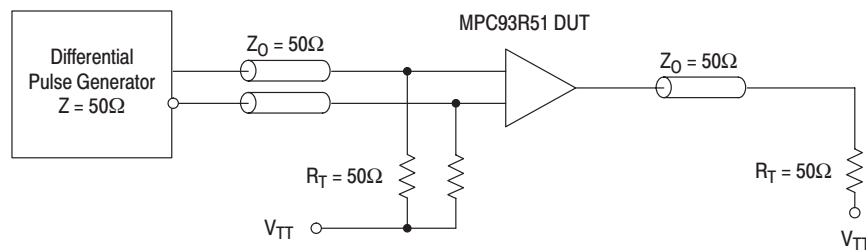
Figure 9. TCLK MPC93R51 AC test reference for $V_{CC} = 3.3V$ 

Figure 10. PCLK MPC93R51 AC test reference

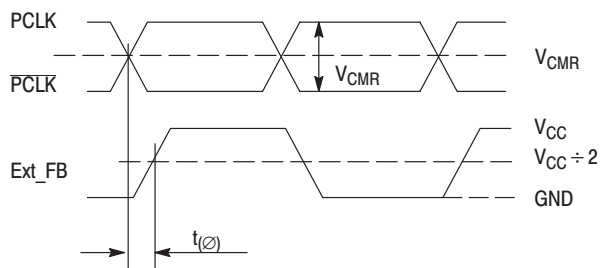


Figure 11. Propagation delay (t_{PD} , static phase offset) test reference

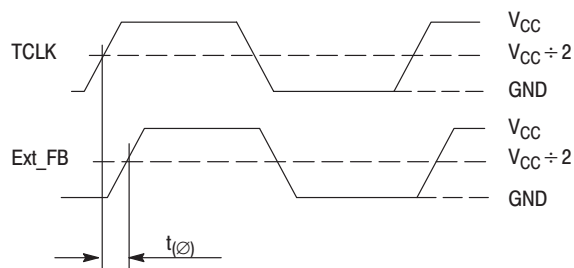
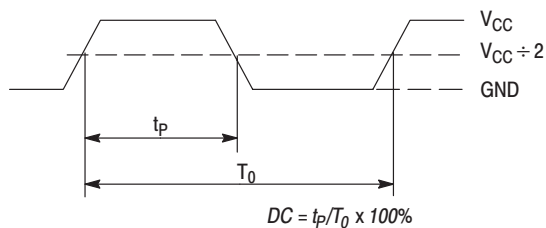
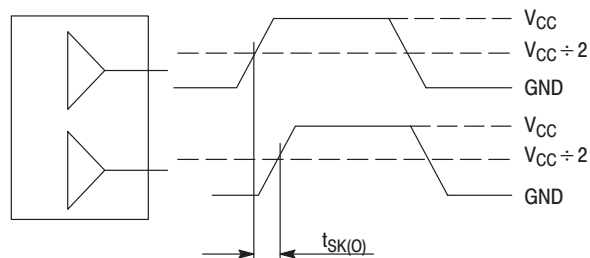


Figure 12. Propagation delay (t_{PD}) test reference



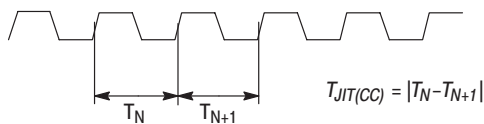
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 13. Output Duty Cycle (DC)



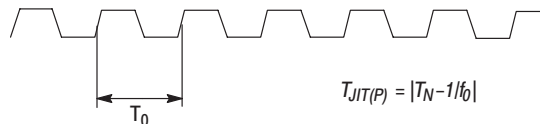
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 14. Output-to-output Skew $t_{SK(O)}$



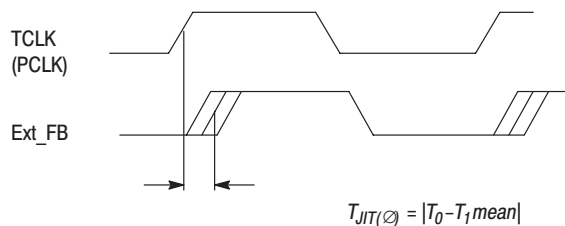
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 15. Cycle-to-cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 16. Period Jitter



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 17. I/O Jitter

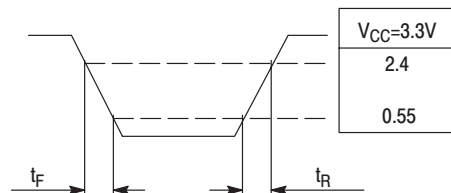


Figure 18. Transition Time Test Reference

3.3V 1:11 LVCMOS Zero Delay Clock Generator

The MPC93R52 is a 3.3V compatible, 1:11 PLL based clock generator targeted for high performance clock tree applications. With output frequencies up to 240 MHz and output skews lower than 200 ps the device meets the needs of most demanding clock applications.

Features

- Configurable 11 outputs LVCMOS PLL clock generator
- Fully integrated PLL
- Wide range of output clock frequency of 16.67 MHz to 240 MHz
- Multiplication of the input reference clock frequency by 3, 2, 1, $3 \div 2$, $2 \div 3$, $1 \div 3$ and $1 \div 2$
- 3.3V LVCMOS compatible
- Maximum output skew of 200 ps
- Supports zero-delay applications
- Designed for high-performance telecom, networking and computing applications
- 32 lead LQFP package
- Ambient Temperature Range – 0°C to +70°C
- Pin and function compatible to the MPC952

Functional Description

The MPC93R52 is a fully 3.3V compatible PLL clock generator and clock driver. The device has the capability to generate output clock signals of 16.67 to 240 MHz from external clock sources. The internal PLL optimized for its frequency range and does not require external loop filter components. One output of the MPC93R52 has to be connected to the PLL feedback input FB_IN to close the external PLL feedback path. The output divider of this output setting determines the PLL frequency multiplication factor. This multiplication factor, F_RANGE and the reference clock frequency must be selected to situate the VCO in its specified lock range. The frequency of the clock outputs can be configured individually for all three output banks by the FSELx pins supporting systems with different but phase-aligned clock frequencies.

The PLL of the MPC93R52 minimizes the propagation delay and therefore supports zero-delay applications. All inputs and outputs are LVCMOS compatible. The outputs are optimized to drive parallel terminated 50Ω transmission lines. Alternatively, each output can drive up to two series terminated transmission lines giving the device an effective fanout of 22.

The device also supports output high-impedance disable and a PLL bypass mode for static system test and diagnosis. The MPC93R52 is package in a 32 ld LQFP.

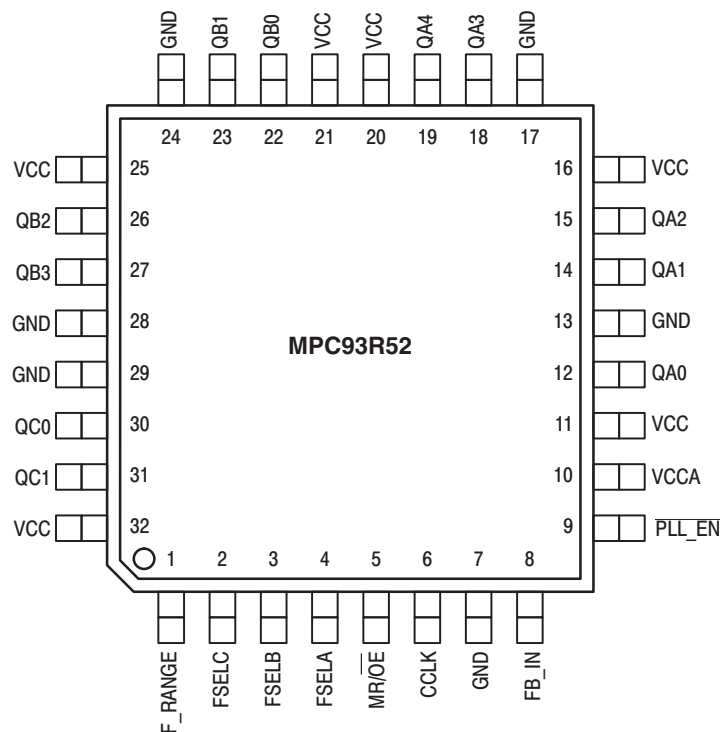
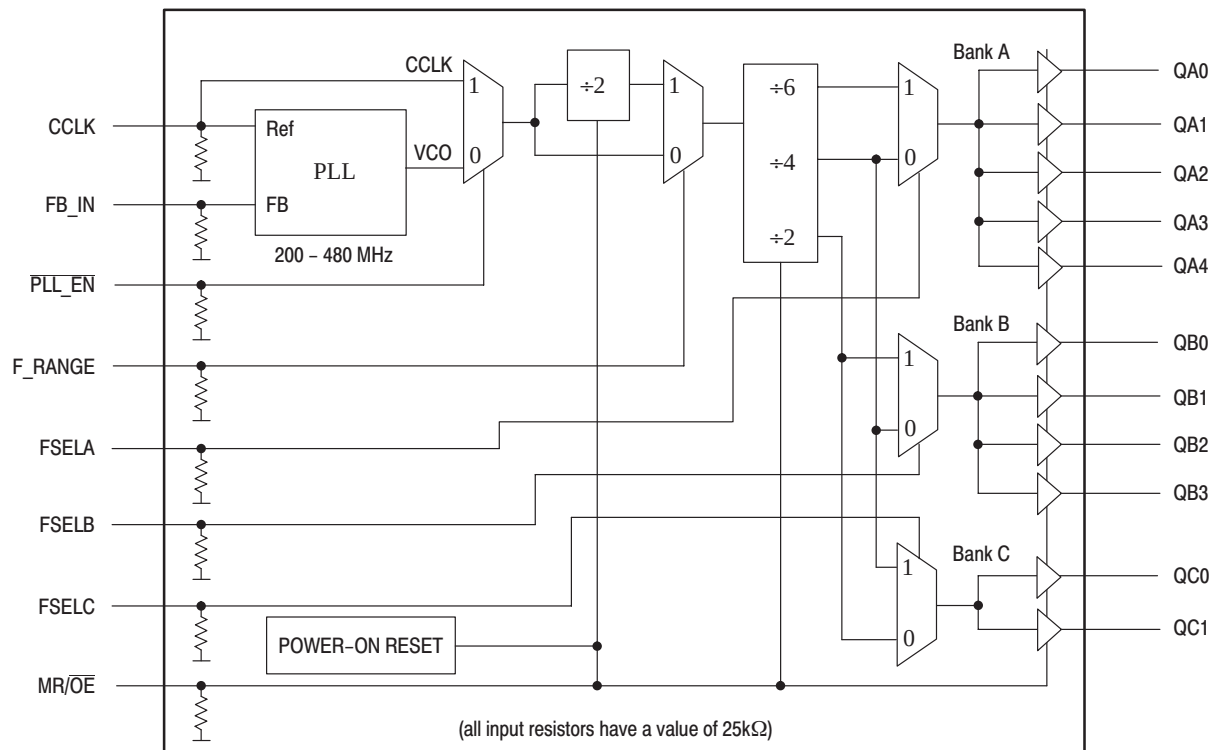
MPC93R52

**LOW VOLTAGE
3.3V LVCMOS 1:11
CLOCK GENERATOR**



FA SUFFIX
32 LEAD LQFP PACKAGE
CASE 873A

2



It is recommended to use an external RC filter for the analog power supply pin VCCA. Please see application section for details.

Table 1: PIN CONFIGURATION

Pin	I/O	Type	Function
CCLK	Input	LVC MOS	PLL reference clock signal
FB_IN	Input	LVC MOS	PLL feedback signal input, connect to an output
F_RANGE	Input	LVC MOS	PLL frequency range select
FSELA	Input	LVC MOS	Frequency divider select for bank A outputs
FSELB	Input	LVC MOS	Frequency divider select for bank B outputs
FSELC	Input	LVC MOS	Frequency divider select for bank C outputs
PLL_EN	Input	LVC MOS	PLL enable/disable
MR/OE	Input	LVC MOS	Output enable/disable (high-impedance tristate) and device reset
QA0–4, QB0–3, QC0–1	Output	LVC MOS	Clock outputs
GND	Supply	Ground	Negative power supply
VCCA	Supply	VCC	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin VCCA. Please see applications section for details.
VCC	Supply	VCC	Positive power supply for I/O and core

2

Table 2: FUNCTION TABLE

Control	Default	0	1
F_RANGE, FSELA, FSELB, and FSELC control the operating PLL frequency range and input/output frequency ratios. See Table 1 and Table 2 for supported frequency ranges and output to input frequency ratios.			
F_RANGE	0	VCO ÷ 1 (High input frequency range)	VCO ÷ 2 (Low input frequency range)
FSELA	0	Output divider ÷ 4	Output divider ÷ 6
FSELB	0	Output divider ÷ 4	Output divider ÷ 2
FSELC	0	Output divider ÷ 2	Output divider ÷ 4
MR/OE	0	Outputs enabled (active)	Outputs disabled (high-impedance state) and reset of the device. During reset, the PLL feedback loop is open and the VCO is operating at its lowest frequency. The MPC93R52 requires reset after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than two reference clock cycles (CCLK). The device is reset by the internal power-on reset (POR) circuitry during power-up.
PLL_EN	0	Normal operation mode with PLL enabled.	Test mode with PLL disabled. CCLK is substituted for the internal VCO output. MPC93R52 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.

Table 3: GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 4: ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.9	V	
V_{IN}	DC Input Voltage	-0.3	$V_{CC}+0.3$	V	
V_{OUT}	DC Output Voltage	-0.3	$V_{CC}+0.3$	V	
I_{IN}	DC Input Current		± 20	mA	
I_{OUT}	DC Output Current		± 50	mA	
T_S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5: DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ$ to 70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	2.0		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input low voltage			0.8	V	LVC MOS
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -24 \text{ mA}^a$
V_{OL}	Output Low Voltage			0.55 0.30	V V	$I_{OL} = 24 \text{ mA}$ $I_{OL} = 12 \text{ mA}$
Z_{OUT}	Output impedance		14 - 17		Ω	
I_{IN}	Input Current ^b			± 200	μA	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$
I_{CCA}	Maximum PLL Supply Current		3.0	5.0	mA	V_{CCA} Pin
I_{CCQ}^c	Maximum Quiescent Supply Current		7.0	10	mA	All V_{CC} Pins

a. The MPC93R52 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines.

b. Inputs have pull-down resistors affecting the input current.

c. I_{CCQ} is the DC current consumption of the device with all outputs open in high impedance state and the inputs in its default state or open.

Table 6: AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ$ to $70^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input reference frequency in PLL mode ^{bc} $\div 4$ feedback	50.0		120.0	MHz	
	$\div 6$ feedback	33.3		80.0	MHz	
	$\div 8$ feedback	25.0		60.0	MHz	
	$\div 12$ feedback	16.67		40.0	MHz	
	Input reference frequency in PLL bypass mode ^d	50.0		250.0	MHz	
f_{VCO}	VCO lock frequency range ^e	200		480	MHz	
f_{MAX}	Output Frequency $\div 2$ output ^f	100		240	MHz	
	$\div 4$ output	50		120	MHz	
	$\div 6$ output	33.3		80	MHz	
	$\div 8$ output	25		60	MHz	
	$\div 12$ output	16.67		40	MHz	
t_{PWMIN}	Minimum Reference Input Pulse Width	2.0			ns	
t_r, t_f	CCLK Input Rise/Fall Time ^g			1.0	ns	0.8 to 2.0V
$t_{(\phi)}$	Propagation Delay CCLK to FB_IN ($f_{ref} = 50MHz$) (static phase offset)	-100		+200	ps ps	PLL locked
$t_{sk(O)}$	Output-to-output Skew ^h all outputs, any frequency within QA output bank within QB output bank within QC output bank			150	ps	
				100	ps	
				100	ps	
				50	ps	
DC	Output duty cycle	47	50	53	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time			8	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter output frequencies mixed all outputs same frequency			450	ps	
				100	ps	
$t_{JIT(PER)}$	Period Jitter output frequencies mixed all outputs same frequency			450	ps	
				100	ps	
$t_{JIT(\phi)}$	I/O Phase Jitter ⁱ $\div 4$ feedback divider RMS (1 σ)		40		ps	
			50		ps	
			60		ps	
			80		ps	
BW	PLL closed loop bandwidth ^j $\div 4$ feedback		2.0–8.0		MHz	
			1.0–4.0		MHz	
			0.8–2.5		MHz	
			0.6–1.5		MHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

a AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b PLL mode requires $PLL\_EN=0$ to enable the PLL and zero-delay operation.

c The PLL may be unstable with a divide by 2 feedback ratio.

d In PLL bypass mode, the MPC93R52 divides the input reference clock.

e The input frequency f_{ref} on CCLK must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.

f See Table 9 and Table 10 for output divider configurations.

g The MPC93R52 will operate with input rise and fall times up to 3.0 ns, but the AC characteristics, specifically $t_{(\phi)}$, can only be guaranteed if t_r/t_f are within the specified range.

h See application section for part-to-part skew calculation.

i See application section for a jitter calculation for other confidence factors than 1 σ .

j -3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Programming the MPC93R52

The MPC93R52 supports output clock frequencies from 16.67 to 240 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency lock range between 200 and 480 MHz for stable and optimal operation.

The FSELA, FSELB, FSELC pins select the desired output clock frequencies. Possible frequency ratios of the reference clock input to the outputs are 1:1, 1:2, 1:3, 3:2 as well as 2:3, 3:1 and 2:1. Table 1 illustrates the various output configurations and frequency ratios supported by the MPC93R52. See also Table 9, Table 10 and Figure 3 to Figure 6 for further reference. A $\div 2$ output divider cannot be used for feedback.

Table 9: MPC93R52 Example Configuration (F_RANGE = 0)

PLL Feedback	fref ^a [MHz]	FSELA	FSELB	FSELC	QA[0:4]:fref ratio	QB[0:3]:fref ratio	QC[0:1]:fref ratio
VCO $\div 4^b$	50-120	0	0	0	fref (50-120 MHz)	fref (50-120 MHz)	fref $\cdot 2$ (100-240 MHz)
		0	0	1	fref (50-120 MHz)	fref (50-120 MHz)	fref (50-120 MHz)
		1	0	0	fref $\cdot 2 \div 3$ (33-80 MHz)	fref (50-120 MHz)	fref $\cdot 2$ (100-240 MHz)
		1	0	1	fref $\cdot 2 \div 3$ (33-80 MHz)	fref (50-120 MHz)	fref (50-120 MHz)
VCO $\div 6^c$	33.3-80	1	0	0	fref (33-80 MHz)	fref $\cdot 3 \div 2$ (50-120 MHz)	fref $\cdot 3$ (100-240 MHz)
		1	0	1	fref (33-80 MHz)	fref $\cdot 3 \div 2$ (50-120 MHz)	fref $\cdot 3 \div 2$ (50-120 MHz)
		1	1	0	fref (33-80 MHz)	fref $\cdot 3$ (100-240 MHz)	fref $\cdot 3$ (100-240 MHz)
		1	1	1	fref (33-80 MHz)	fref $\cdot 3$ (100-240 MHz)	fref $\cdot 3 \div 2$ (50-120 MHz)

a. fref is the input clock reference frequency (CCLK)

b. QAx connected to FB_IN and FSELA=0

c. QAx connected to FB_IN and FSELA=1

Table 10: MPC93R52 Example Configurations (F_RANGE = 1)

PLL Feedback	fref ^a [MHz]	FSELA	FSELB	FSELC	QA[0:4]:fref ratio	QB[0:3]:fref ratio	QC[0:1]:fref ratio
VCO $\div 8^b$	25-60	0	0	0	fref (25-60 MHz)	fref (25-60 MHz)	fref $\cdot 2$ (50-120 MHz)
		0	0	1	fref (25-60 MHz)	fref (25-60 MHz)	fref (25-60 MHz)
		1	0	0	fref $\cdot 2 \div 3$ (16-40 MHz)	fref (25-60 MHz)	fref $\cdot 2$ (50-120 MHz)
		1	0	1	fref $\cdot 2 \div 3$ (16-40 MHz)	fref (25-60 MHz)	fref (25-60 MHz)
VCO $\div 12^c$	16.67-40	1	0	0	fref (16-40 MHz)	fref $\cdot 3 \div 2$ (25-60 MHz)	fref $\cdot 3$ (50-120 MHz)
		1	0	1	fref (16-40 MHz)	fref $\cdot 3 \div 2$ (25-60 MHz)	fref $\cdot 3 \div 2$ (25-60 MHz)
		1	1	0	fref (16-40 MHz)	fref $\cdot 3$ (50-120 MHz)	fref $\cdot 3$ (50-120 MHz)
		1	1	1	fref (16-40 MHz)	fref $\cdot 3$ (50-120 MHz)	fref $\cdot 3 \div 2$ (25-60 MHz)

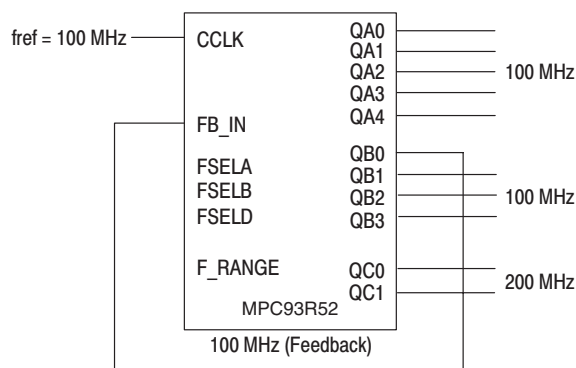
a. fref is the input clock reference frequency (CCLK)

b. QAx connected to FB_IN and FSELA=0

c. QAx connected to FB_IN and FSELA=1

Example Configurations for the MPC93R52

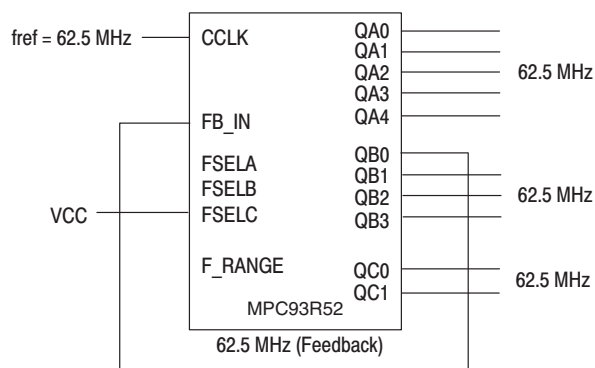
Figure 3. MPC93R52 Default Configuration



MPC93R52 default configuration (feedback of QB0 = 100 MHz). All control pins are left open.

Frequency range	Min	Max
Input	50 MHz	120 MHz
QA outputs	50 MHz	120 MHz
QB outputs	50 MHz	120 MHz
QC outputs	100 MHz	240 MHz

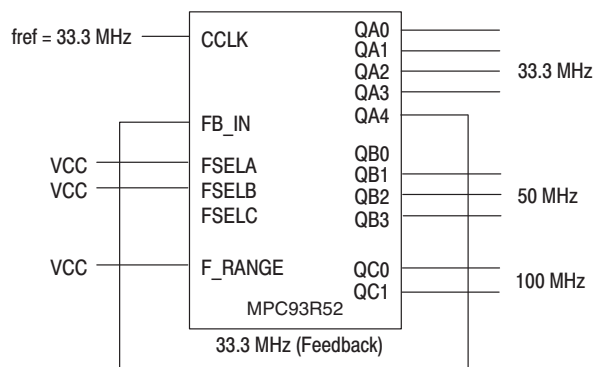
Figure 4. MPC93R52 Zero Delay Buffer Configuration



MPC93R52 zero-delay (feedback of QB0 = 62.5 MHz). All control pins are left open except FSEL C = 1. All outputs are locked in frequency and phase to the input clock.

Frequency range	Min	Max
Input	50 MHz	120 MHz
QA outputs	50 MHz	120 MHz
QB outputs	50 MHz	120 MHz
QC outputs	50 MHz	120 MHz

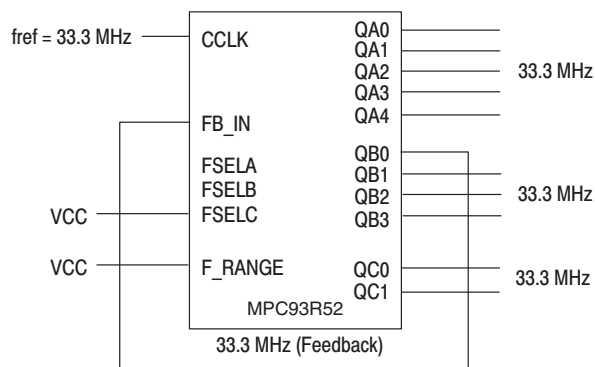
Figure 5. MPC93R52 Default Configuration



MPC93R52 configuration to multiply the reference frequency by 3, 3÷2 and 1. PLL feedback of QA4 = 33.3 MHz.

Frequency range	Min	Max
Input	25 MHz	60 MHz
QA outputs	50 MHz	120 MHz
QB outputs	50 MHz	120 MHz
QC outputs	100 MHz	240 MHz

Figure 6. MPC93R52 Zero Delay Buffer Config. 2



MPC93R52 zero-delay (feedback of QB0 = 33.3 MHz). Equivalent to Table 2 except F_RANGE = 1 enabling a lower input and output clock frequency.

Frequency range	Min	Max
Input	25 MHz	60 MHz
QA outputs	25 MHz	60 MHz
QB outputs	25 MHz	60 MHz
QC outputs	25 MHz	60 MHz

Power Supply Filtering

The MPC93R52 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC93R52 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation is a power supply filter on the V_{CCA} pin for the MPC93R52. Figure 7 illustrates a typical power supply filter scheme. The MPC93R52 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F . From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.98V must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 7 “ V_{CCA} Power Supply Filter” should have a resistance of 5–25 Ω to meet the voltage drop criteria.

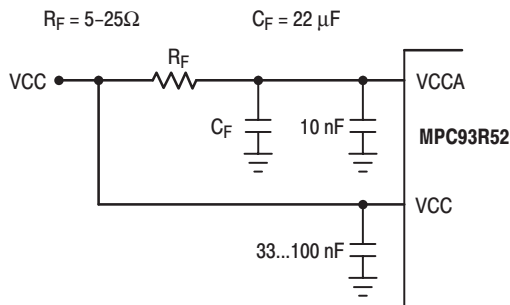


Figure 7. V_{CCA} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 7 “ V_{CCA} Power Supply Filter”, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC93R52 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC93R52 in zero-delay applications

Nested clock trees are typical applications for the MPC93R52. Designs using the MPC93R52 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC93R52 clock driver allows for its use as a zero delay buffer. One example configuration is to use a $\div 4$ output as a feedback to the PLL and configuring all other outputs to a divide-by-4 mode. The propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of part-to-part skew

The MPC93R52 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC93R52 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD, LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

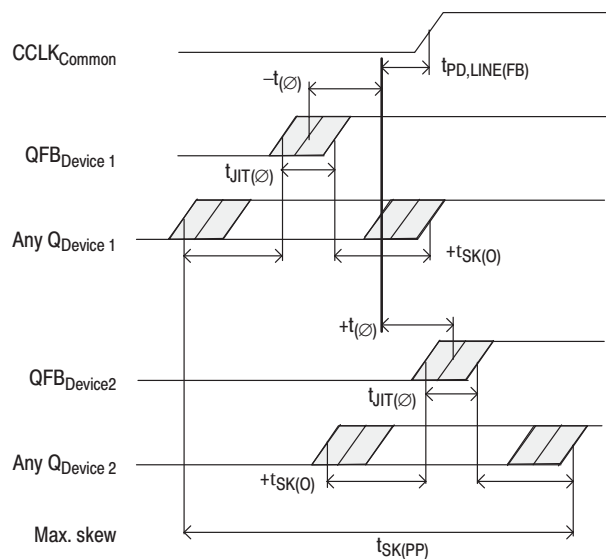


Figure 8. MPC93R52 max. device-to-device skew

Due to the statistical nature of I/O jitter a RMS value (1σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 11.

Table 11: Confidence Factor CF

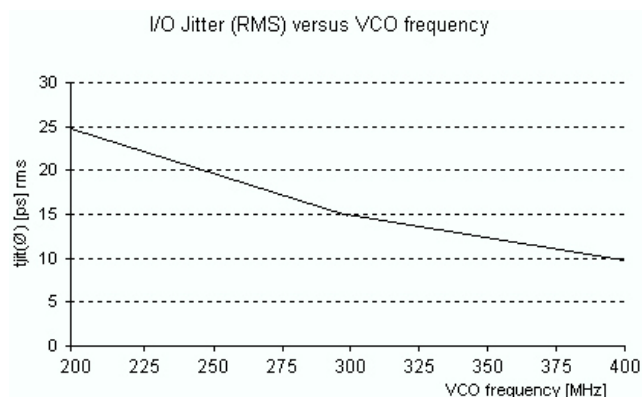
CF	Probability of clock edge within the distribution
$\pm 1\sigma$	0.68268948
$\pm 2\sigma$	0.95449988
$\pm 3\sigma$	0.99730007
$\pm 4\sigma$	0.99993663
$\pm 5\sigma$	0.99999943
$\pm 6\sigma$	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% ($\pm 3\sigma$) is assumed, resulting in a worst case timing uncertainty from input to any output of -445 ps to 395 ps relative to CCLK:

$$t_{SK(PP)} = [-200ps...150ps] + [-200ps...200ps] + [(15ps \cdot -3)...(15ps \cdot 3)] + t_{PD, LINE(FB)}$$

$$t_{SK(PP)} = [-445ps...395ps] + t_{PD, LINE(FB)}$$

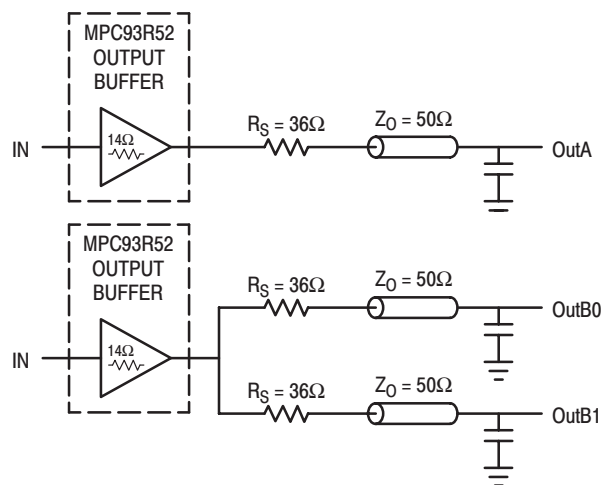
Due to the frequency dependence of the I/O jitter, Figure 9 “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis.

**Figure 9. Max. I/O Jitter versus frequency**

Driving Transmission Lines

The MPC93R52 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}+2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC93R52 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 10 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC93R52 clock driver is effectively doubled due to its capability to drive multiple lines.

**Figure 10. Single versus Dual Transmission Lines**

The waveform plots in Figure 11 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC93R52 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC93R52. The output waveform in Figure 11 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned} V_L &= V_S (Z_0 \div (R_S + R_0 + Z_0)) \\ Z_0 &= 50\Omega \parallel 50\Omega \\ R_S &= 36\Omega \parallel 36\Omega \\ R_0 &= 14\Omega \\ V_L &= 3.0 (25 \div (18+17+25)) \\ &= 1.31V \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

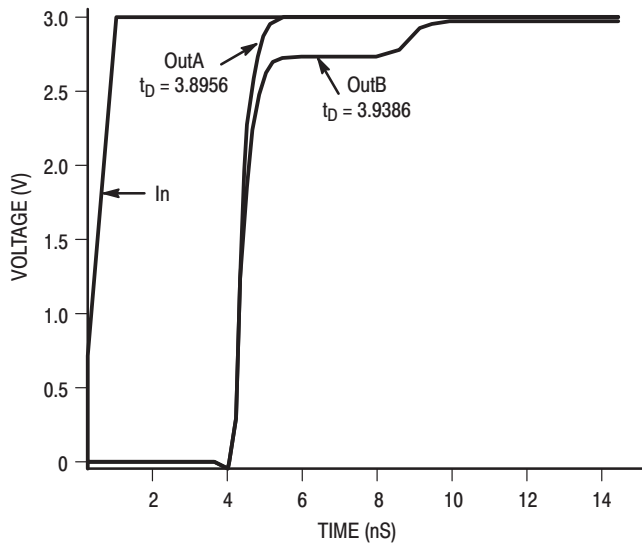


Figure 11. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be

uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 12 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

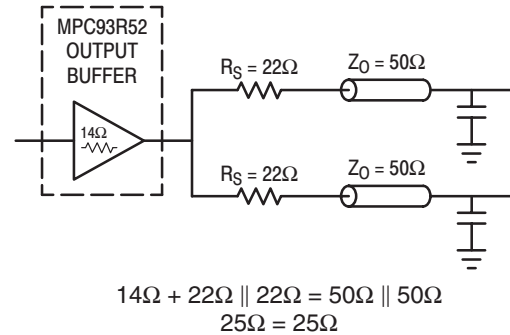
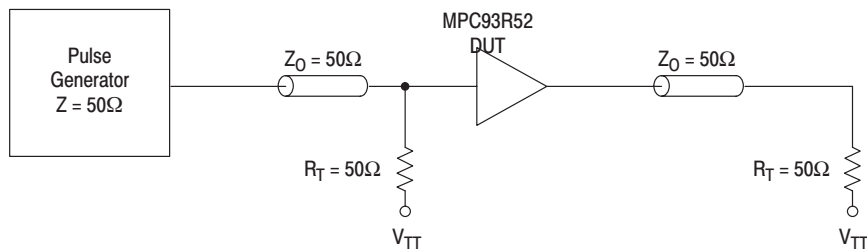
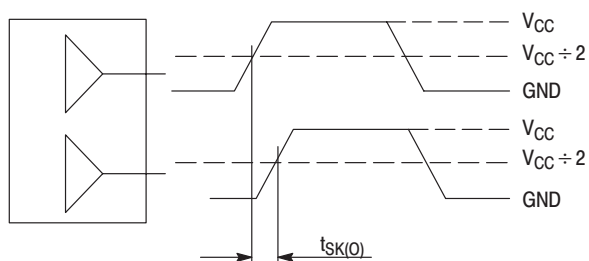


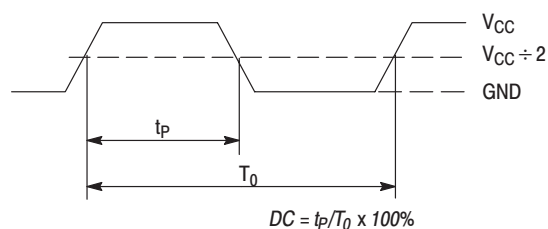
Figure 12. Optimized Dual Line Termination

Figure 13. CCLK MPC93R52 AC test reference for $V_{CC} = 3.3V$ and $V_{CC} = 2.5V$



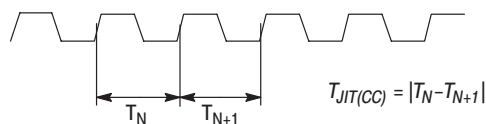
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 14. Output-to-output Skew $t_{SK(O)}$



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 16. Output Duty Cycle (DC)



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 18. Cycle-to-cycle Jitter

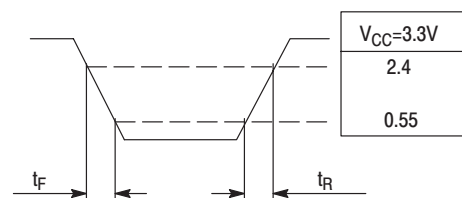


Figure 20. Output Transition Time Test Reference

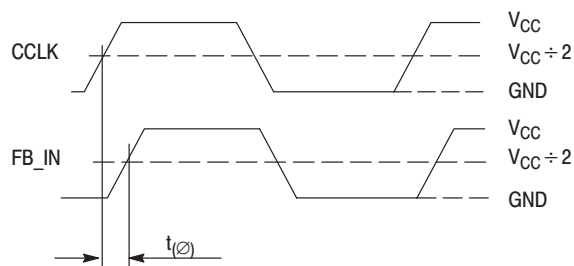
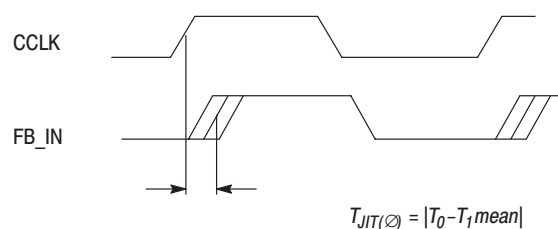
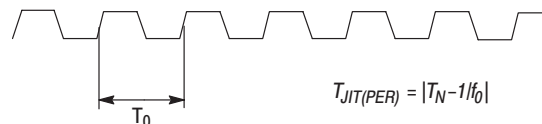


Figure 15. Propagation delay ($t_{(\phi)}$, static phase offset) test reference



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 17. I/O Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 19. Period Jitter

Low Voltage PLL Clock Driver

The MPC950 is a 3.3V compatible, PLL based clock driver device targeted for high performance clock tree designs. With output frequencies of up to 180MHz and output skews of 375ps the MPC950 is ideal for the most demanding clock tree designs. The devices employ a fully differential PLL design to minimize cycle-to-cycle and long term jitter. This parameter is of significant importance when the clock driver is providing the reference clock for PLL's on board today's microprocessors and ASIC's. The devices offer 9 low skew outputs, the outputs are configurable to support the clocking needs of the various high performance microprocessors.

- Fully Integrated PLL
- Oscillator or Crystal Reference Input
- Output Frequency up to 180MHz
- Outputs Disable in High Impedance
- Compatible with **PowerPC™**, Intel and High Performance RISC Microprocessors
- LQFP Packaging
- Output Frequency Configurable
- ± 100 ps Typical Cycle-to-Cycle Jitter

Two selectable feedback division ratios are available on the MPC950 to provide input reference clock flexibility. The FBSEL pin will choose between a divide by 8 or a divide by 16 of the VCO frequency to be compared with the input reference to the MPC950. The internal VCO is running at either 2x or 4x the high speed output, depending on configuration, so that the input reference will be either one half, one fourth or one eighth the high speed output.

The MPC950 provides an external test clock input for scan clock distribution or system diagnostics. In addition the REF_SEL pin allows the user to select between a crystal input to an on-board oscillator for the reference or to chose a TTL level oscillator input directly. The on-board crystal oscillator requires no external components beyond a series resonant crystal.

The MPC950 is fully 3.3V compatible and require no external loop filter components. All inputs accept LVCMOS or LVTTTL compatible levels while the outputs provide LVCMOS levels with the capability to drive terminated 50 Ω transmission lines. Select inputs do not have internal pull-up/pull-down resistors and thus must be set externally. For series terminated 50 Ω lines, each of the MPC950 outputs can drive two traces giving the device an effective fanout of 1:18. The device is packaged in a 7x7mm 32-lead LQFP package to provide the optimum combination of board density and performance.

MPC950

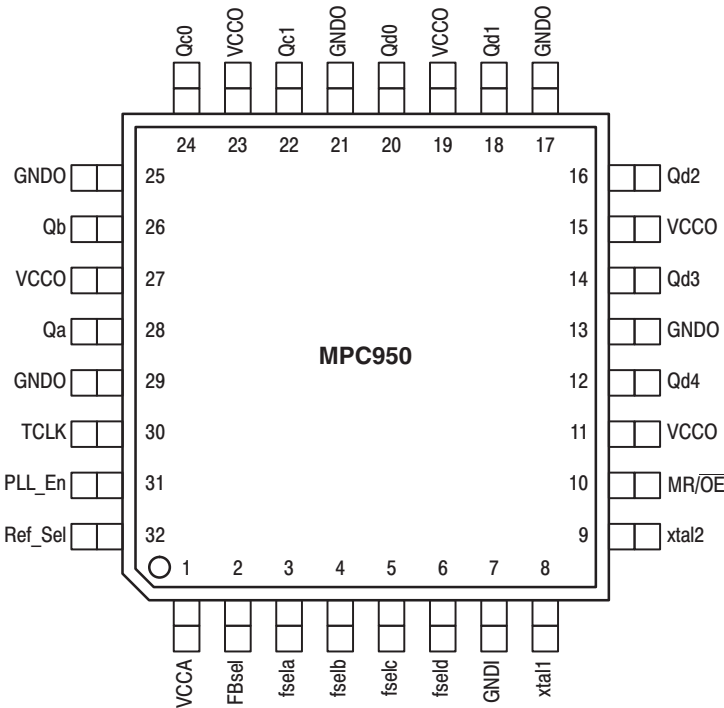
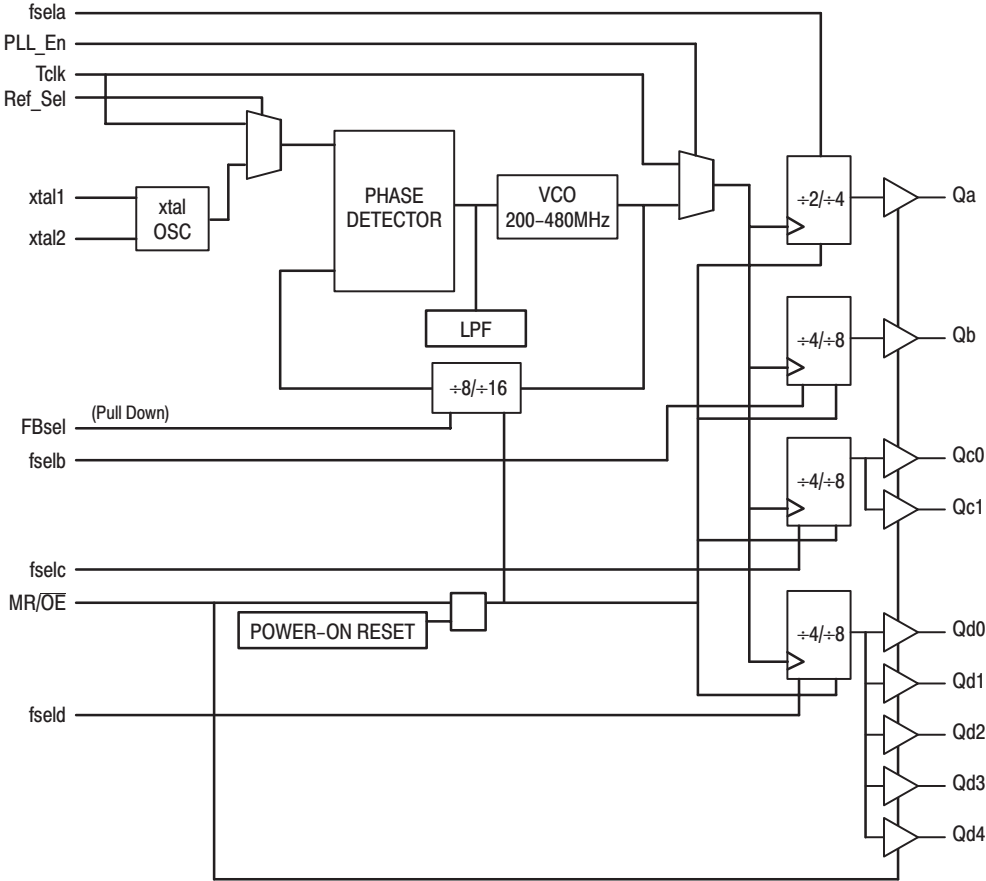
See Upgrade Product – MPC9350

LOW VOLTAGE PLL CLOCK DRIVER



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-02

MPC950 LOGIC DIAGRAM



FUNCTION TABLES

Ref_Sel	Function
1	TCLK
0	XTAL_OSC

PLL_En	Function
1	PLL Enabled
0	PLL Bypass

FBsel	Function
1	+8
0	+16

MR/OE	Function
1	Outputs Disabled
0	Outputs Enabled

fseln	Function
1	Qa = +4; Qb:d = +8
0	Qa = +2; Qb:d = +4

FUNCTION TABLE – MPC950

INPUTS				OUTPUTS				TOTALS		
fsel _a	fsel _b	fsel _c	fsel _d	Qa(1)	Qb(1)	Qc(2)	Qd(5)	Total 2x	Total x	Total x/2
0	0	0	0	2x	x	x	x	1	8	0
0	0	0	1	2x	x	x	x/2	1	3	5
0	0	1	0	2x	x	x/2	x	1	6	2
0	0	1	1	2x	x	x/2	x/2	1	1	7
0	1	0	0	2x	x/2	x	x	1	7	1
0	1	0	1	2x	x/2	x	x/2	1	2	6
0	1	1	0	2x	x/2	x/2	x	1	3	5
0	1	1	1	2x	x/2	x/2	x/2	1	0	8
1	0	0	0	x	x	x	x	0	9	0
1	0	0	1	x	x	x	x/2	0	4	5
1	0	1	0	x	x	x/2	x	0	7	2
1	0	1	1	x	x	x/2	x/2	0	2	7
1	1	0	0	x	x/2	x	x	0	8	1
1	1	0	1	x	x/2	x	x/2	0	3	6
1	1	1	0	x	x/2	x/2	x	0	6	3
1	1	1	1	x	x/2	x/2	x/2	0	1	8

NOTE: $x = f_{VCO}/4$; $200\text{MHz} < f_{VCO} < 480\text{MHz}$.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	4.6	V
V_I	Input Voltage	-0.3	$V_{CC} + 0.3$	V
I_{IN}	Input Current		± 20	mA
T_{Stor}	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

THERMAL CHARACTERISTICS

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage LVC MOS Inputs	2.0		3.6	V	
V_{IL}	Input LOW Voltage LVC MOS Inputs			0.8	V	
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -40\text{mA}$, Note 1.
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 40\text{mA}$, Note 1.
I_{IN}	Input Current			± 120	μA	
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	Per Output
I_{CC}	Maximum Quiescent Supply Current		90	115	mA	All VCC Pins
I_{CCPLL}	Maximum PLL Supply Current		15	20	mA	VCCA Pin Only

1. The MPC950 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}/2$) transmission lines on the incident edge (see Applications Info section).

PLL INPUT REFERENCE CHARACTERISTICS ($T_A = 0$ to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	Note 1.	Note 1.	MHz	
f_{xtal}	Crystal Oscillator Frequency	10	25	MHz	Note 2.
f_{refDC}	Reference Input Duty Cycle	25	75	%	

1. Maximum and minimum input reference is limited by the VCO lock range and the feedback divider for the TCLK inputs.
2. See Applications Info section for more crystal information.

AC CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time	0.10		1.0	ns	0.8 to 2.0V, Note 1.
t_{pw}	Output Duty Cycle	$t_{CYCLE}/2 - 1000$		$t_{CYCLE}/2 + 1000$	ps	Note 1.
$t_{sk(O)}$	Output-to-Output Skews Same Frequencies		200	375	ps	Note 1.
	Different Frequencies Qa _{fmax} < 150MHz Qa _{fmax} > 150MHz		325	500 750		
f_{VCO}	PLL VCO Lock Range	200		480	MHz	
f_{max}	Maximum Output Frequency Qa (+2) Qa/Qb (+4) Qb (+8)			180 120 60	MHz	Note 1.
$t_{PLZ,HZ}$	Output Disable Time			7	ns	Note 1.
t_{PZL}	Output Enable Time			6	ns	Note 1.
t_{jitter}	Cycle-to-Cycle Jitter (Peak-to-Peak)		± 100		ps	Note 2.
t_{lock}	Maximum PLL Lock Time			10	ms	

1. Termination of 50Ω to $V_{CC}/2$.
2. See Applications Info section for more jitter information.

APPLICATIONS INFORMATION**Programming the MPC950**

The MPC950 clock driver outputs can be configured into several frequency relationships. The output dividers for the four output groups allows the user to configure the outputs into 1:1, 2:1, 4:1 and 4:2:1 frequency ratios. The use of even dividers ensures that the output duty cycle is always 50%. Table 1 illustrates the various output configurations, the table describes the outputs using the VCO frequency as a reference. As an example for a 4:2:1 relationship the Qa outputs would be set at $VCO/2$, the Qb's and Qc's at $VCO/4$ and the Qd's at $VCO/8$. These settings will provide output frequencies with a 4:2:1 relationship.

The division settings establish the output relationship, but one must still ensure that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL is such that for output frequencies between 25 and 180MHz the MPC950 can generally be configured into a stable region.

The relationship between the input reference and the output frequency is also very flexible. Table 2 shows the multiplication factors between the inputs and outputs for the MPC950. Figure 1 through Figure 4 illustrates several programming possibilities, although not exhaustive it is representative of the potential applications.

Table 1. Programmable Output Frequency Relationships

INPUTS				OUTPUTS			
fsela	fselb	fselc	fseld	Qa	Qb	Qc	Qd
0	0	0	0	VCO/2	VCO/4	VCO/4	VCO/4
0	0	0	1	VCO/2	VCO/4	VCO/4	VCO/8
0	0	1	0	VCO/2	VCO/4	VCO/8	VCO/4
0	0	1	1	VCO/2	VCO/4	VCO/8	VCO/8
0	1	0	0	VCO/2	VCO/8	VCO/4	VCO/4
0	1	0	1	VCO/2	VCO/8	VCO/4	VCO/8
0	1	1	0	VCO/2	VCO/8	VCO/8	VCO/4
0	1	1	1	VCO/2	VCO/8	VCO/8	VCO/8
1	0	0	0	VCO/4	VCO/4	VCO/4	VCO/4
1	0	0	1	VCO/4	VCO/4	VCO/4	VCO/8
1	0	1	0	VCO/4	VCO/4	VCO/8	VCO/4
1	0	1	1	VCO/4	VCO/4	VCO/8	VCO/8
1	1	0	0	VCO/4	VCO/8	VCO/4	VCO/4
1	1	0	1	VCO/4	VCO/8	VCO/4	VCO/8
1	1	1	0	VCO/4	VCO/8	VCO/8	VCO/4
1	1	1	1	VCO/4	VCO/8	VCO/8	VCO/8

Table 2. Input Reference versus Output Frequency Relationships

Config	fsela	fselb	fselc	fseld	FB_Sel = '1'				FB_Sel = '0'			
					Qa	Qb	Qc	Qd	Qa	Qb	Qc	Qd
1	0	0	0	0	4x	2x	2x	2x	8x	4x	4x	4x
2	0	0	0	1	4x	2x	2x	x	8x	4x	4x	2x
3	0	0	1	0	4x	2x	x	2x	8x	4x	2x	4x
4	0	0	1	1	4x	2x	x	x	8x	4x	2x	2x
5	0	1	0	0	4x	x	2x	2x	8x	2x	4x	4x
6	0	1	0	1	4x	x	2x	x	8x	2x	4x	2x
7	0	1	1	0	4x	x	x	2x	8x	2x	2x	4x
8	0	1	1	1	4x	x	x	x	8x	2x	2x	2x
9	1	0	0	0	2x	2x	2x	2x	4x	4x	4x	4x
10	1	0	0	1	2x	2x	2x	x	4x	4x	4x	2x
11	1	0	1	0	2x	2x	x	2x	4x	4x	2x	4x
12	1	0	1	1	2x	2x	x	x	4x	4x	2x	2x
13	1	1	0	0	2x	x	2x	2x	4x	2x	4x	4x
14	1	1	0	1	2x	x	2x	x	4x	2x	4x	2x
15	1	1	1	0	2x	x	x	2x	4x	2x	2x	4x
16	1	1	1	1	2x	x	x	x	4x	2x	2x	2x

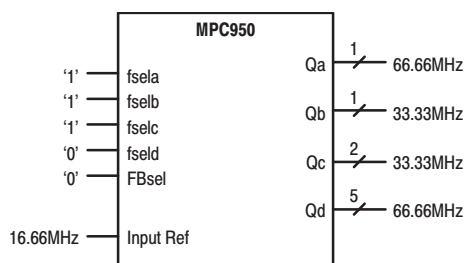


Figure 1. Dual Frequency Configuration

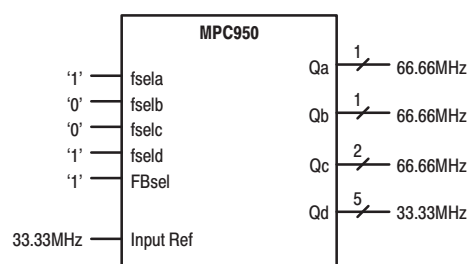


Figure 2. Dual Frequency Configuration

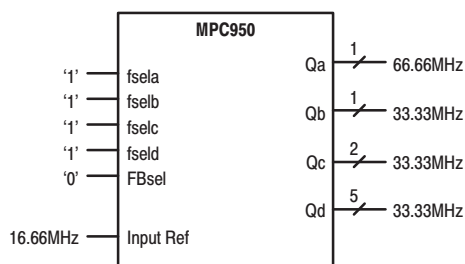


Figure 3. Dual Frequency Configuration

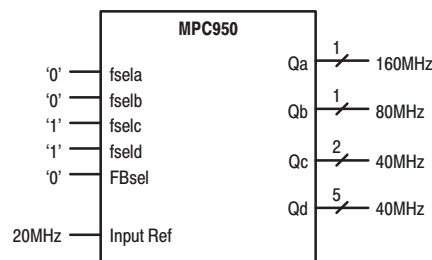


Figure 4. Triple Frequency Configuration

Jitter Performance of the MPC950

With the clock rates of today's digital systems continuing to increase more emphasis is being placed on clock distribution design and management. Among the issues being addressed is system clock jitter and how that affects the overall system timing budget. The MPC950 was designed to minimize clock jitter by employing a differential bipolar PLL as well as incorporating numerous power and ground pins in the design. The following few paragraphs will outline the jitter performance of the MPC950, illustrate the measurement limitations and provide guidelines to minimize the jitter of the device.

The most commonly specified jitter parameter is cycle-to-cycle jitter. Unfortunately with today's high performance measurement equipment there is no way to measure this parameter for jitter performance in the class demonstrated by the MPC950. As a result different methods are used which approximate cycle-to-cycle jitter. The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak-to-peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. If this is not the case the measurement inaccuracy will add significantly to the measured jitter. The oscilloscope cannot collect adjacent pulses, rather it collects data from a very large sample of pulses. It is safe to assume that collecting pulse information in this mode will produce jitter values somewhat larger than if consecutive cycles were measured, therefore, this measurement will represent an upper bound of

cycle-to-cycle jitter. Most likely, this is a conservative estimate of the cycle-to-cycle jitter.

There are two sources of jitter in a PLL based clock driver, the commonly known random jitter of the PLL and the less intuitive jitter caused by synchronous, different frequency outputs switching. For the case where all of the outputs are switching at the same frequency the total jitter is exactly equal to the PLL jitter. In a device, like the MPC950, where a number of the outputs can be switching synchronously but at different frequencies a "multi-modal" jitter distribution can be seen on the highest frequency outputs. Because the output being monitored is affected by the activity on the other outputs it is important to consider what is happening on those other outputs. From Figure 5, one can see for each rising edge on the higher frequency signal the activity on the lower frequency signal is not constant. The activity on the other outputs tends to alter the internal thresholds of the device such that the placement of the edge being monitored is displaced in time. Because the signals are synchronous the relationship is periodic and the resulting jitter is a compilation of the PLL jitter superimposed on the displaced edges. When histograms are plotted the jitter looks like a "multi-modal" distribution as pictured in Figure 5. Depending on the size of the PLL jitter and the relative displacement of the edges the "multi-modal" distribution will appear truly "multi-modal" or simply like a "fat" Gaussian distribution. Again note that in the case where all the outputs are switching at the same frequency there is no edge displacement and the jitter is reduced to that of the PLL.

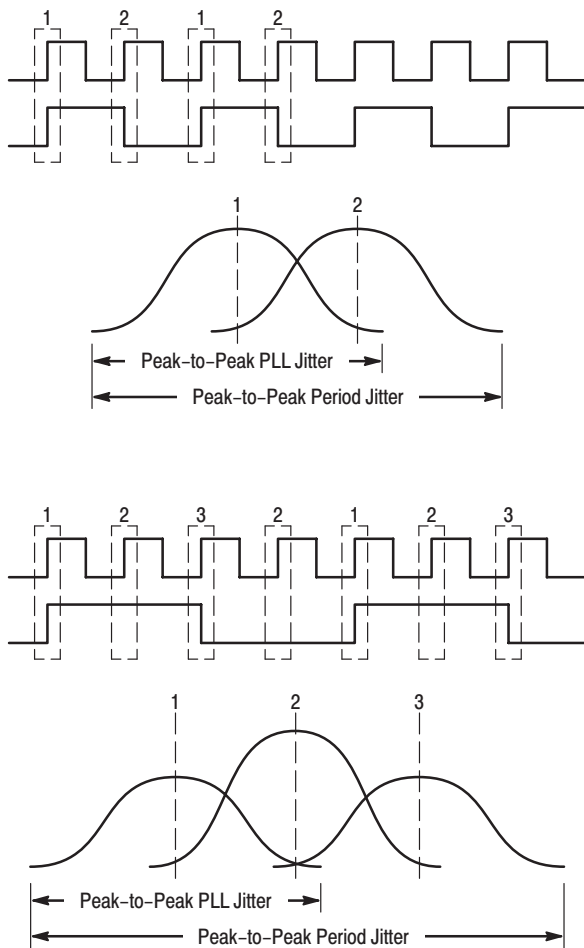
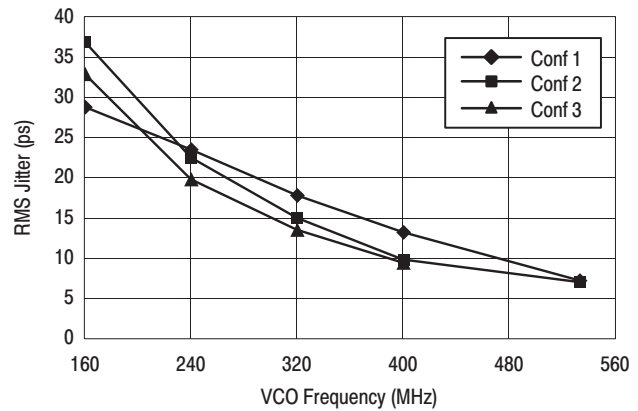


Figure 5. PLL Jitter and Edge Displacement

Figure 6 graphically represents the PLL jitter of the MPC950. The data was taken for several different output configurations. By triggering on the lowest frequency output the PLL jitter can be measured for configurations in which outputs are switching at different frequencies. As one can see in the figure the PLL jitter is much less dependent on output configuration than on internal VCO frequency.

Two different configurations were chosen to look at the period displacement caused by the switching outputs. Configuration 3 is considered worst case as the “trimodal” distribution (as pictured in Figure 5) represents the largest spread between distribution peaks. Configuration 2 is considered a typical configuration with half the outputs at a high frequency and the remaining outputs at one half the high frequency. For these cases the peak-to-peak numbers are reported in Figure 7 as the sigma numbers are useless because the distributions are not Gaussian. For situations where the outputs are synchronous and switching at different frequencies the measurement technique described here is insufficient to use for establishing guaranteed limits. Other techniques are currently being investigated to identify a more accurate and repeatable measurement so that guaranteed limits can be provided. The data generated does give a good indication of the general performance, a performance that in most cases is well within the requirements of today’s microprocessors.

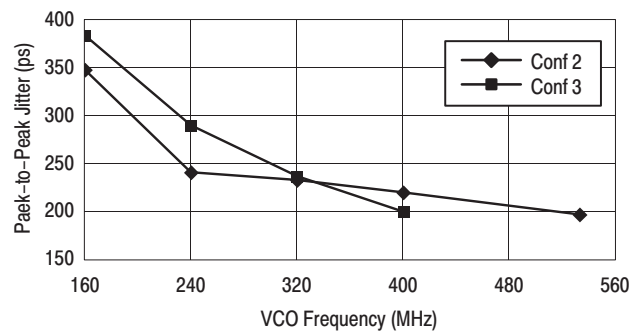


Conf 1 = All Outputs at the Same Frequency

Conf 2 = 4 Outputs at X, 5 Outputs at X/2

Conf 3 = 1 Output at X, 8 Outputs at X/4

Figure 6. RMS PLL Jitter versus VCO Frequency



Conf 2 = 4 Outputs at X, 5 Outputs at X/2

Conf 3 = 1 Output at X, 8 Outputs at X/4

Figure 7. Peak-to-Peak Period Jitter versus VCO Frequency

Finally from the data there are some general guidelines that, if followed, will minimize the output jitter of the device. First and foremost always configure the device such that the VCO runs as fast as possible. This is by far the most critical parameter in minimizing jitter. Second keep the reference frequency as high as possible. More frequent updates at the phase detector will help to reduce jitter. Note that if there is a tradeoff between higher reference frequencies and higher VCO frequency always chose the higher VCO frequency to minimize jitter. The third guideline may be the most difficult, and in some cases impossible, to follow. Try to minimize the number of different frequencies sourced from a single chip. The fixed edge displacement associated with the switching noise in most cases nearly doubles the “effective” jitter of a high speed output.

Power Supply Filtering

The MPC950 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC950 provides separate power supplies for the output buffers (VCCO) and the phase-locked loop (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital out-

puts from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC950.

Figure 8 illustrates a typical power supply filter scheme. The MPC950 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the VCCA pin of the MPC950. From the data sheet the I_{VCCA} current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 8 must have a resistance of 10–15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8–10 Ω resistor to avoid potential V_{CC} drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

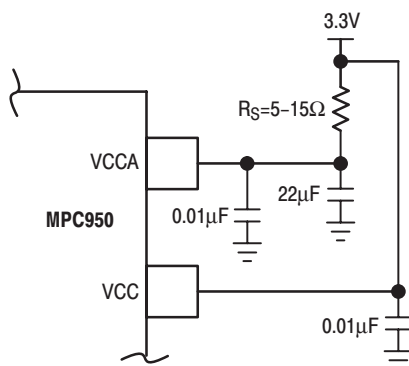


Figure 8. Power Supply Filter

Although the MPC950 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the On-Board Crystal Oscillator

The MPC950 features an on-board crystal oscillator to allow for seed clock generation as well as final distribution. The on-board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC950 as possible to avoid any board level parasitics. To facilitate co-location surface mount crystals are recommended, but not required.

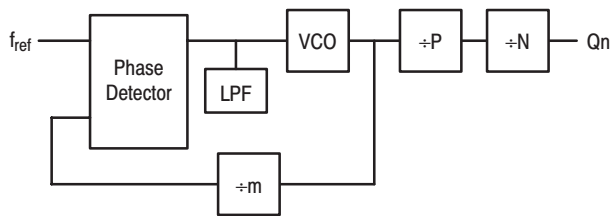
The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on-board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most off the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC950 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

Table 3. Crystal Recommendation

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	± 75 ppm at 25°C
Frequency/Temperature Stability	± 150 ppm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80 Ω Max
Correlation Drive Level	100 μ W
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

The MPC950 is a clock driver which was designed to generate outputs with programmable frequency relationships and not a synthesizer with a fixed input frequency. As a result the crystal input frequency is a function of the desired output frequency. To determine the crystal required to produce the desired output frequency for an application which utilizes internal feedback the block diagram of Figure 9 should be used. The P and the M values for the MPC950 are also included in Figure 9. The M values can be found in the configuration tables included in this applications section.



$$f_{\text{ref}} = \frac{f_{\text{VCO}}}{m}, \quad f_{\text{VCO}} = f_{\text{Qn}} \cdot N \cdot P$$

$$\therefore f_{\text{ref}} = \frac{f_{\text{Qn}} \cdot N \cdot P}{m}$$

$$m = 8 \text{ (FBsel = '1')}, 16 \text{ (FBsel = '0')}$$

$$P = 1$$

Figure 9. PLL Block Diagram

For the MPC950 clock driver, the following will provide an example of how to determine the crystal frequency required for a given design.

Given:

$$\begin{aligned} Q_a &= 160\text{MHz} \\ Q_b &= 80\text{MHz} \\ Q_c &= 40\text{MHz} \\ Q_d &= 40\text{MHz} \\ \text{FBsel} &= '0' \end{aligned}$$

$$f_{\text{ref}} = \frac{f_{\text{Qn}} \cdot N \cdot P}{m}$$

From Table 3

$$f_{\text{Qd}} = \text{VCO}/8 \text{ then } N = 8 \text{ OR } f_{\text{Qa}} = \text{VCO}/2 \text{ then } N = 2$$

From Figure 9

$$m = 16 \text{ and } P = 1$$

$$f_{\text{ref}} = \frac{40 \cdot 8 \cdot 1}{16} = 20\text{MHz} \text{ OR } \frac{160 \cdot 2 \cdot 1}{16} = 20\text{MHz}$$

Driving Transmission Lines

The MPC950 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to

$V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC950 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 10 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fan-out of the MPC950 clock driver is effectively doubled due to its capability to drive multiple lines.

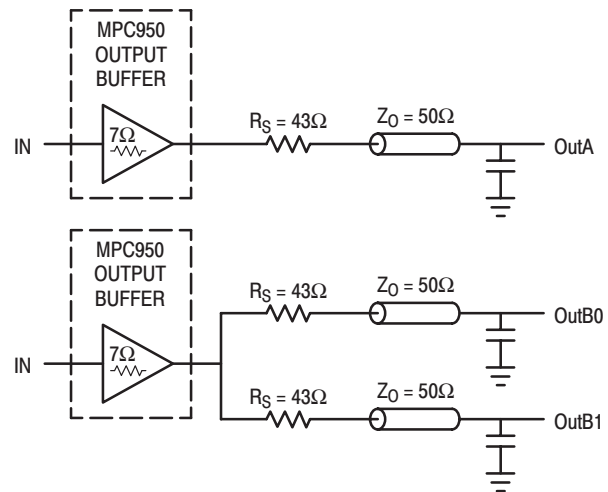


Figure 10. Single versus Dual Transmission Lines

The waveform plots of Figure 11 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC950 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC950. The output waveform in Figure 11 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S \left(Z_0 / (R_s + R_o + Z_0) \right)$$

$$Z_0 = 50\Omega \parallel 50\Omega$$

$$R_s = 43\Omega \parallel 43\Omega$$

$$R_o = 7\Omega$$

$$V_L = 3.0 \left(25 / (21.5 + 7 + 25) \right) = 3.0 \left(25 / 53.5 \right) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

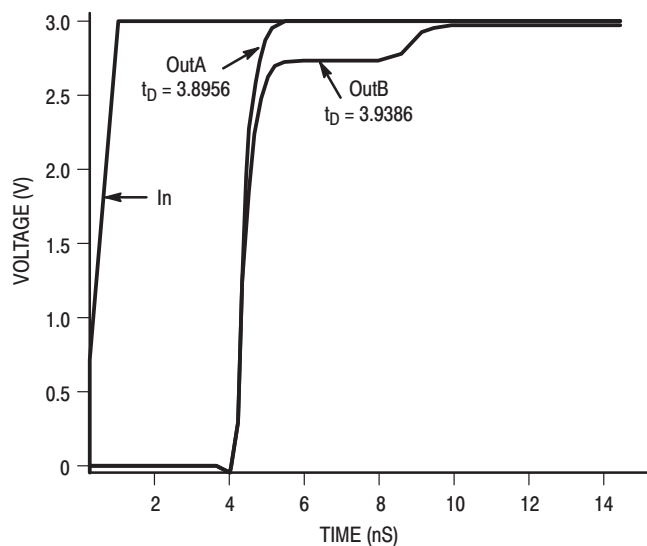


Figure 11. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better

match the impedances when driving multiple lines the situation in Figure 12 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

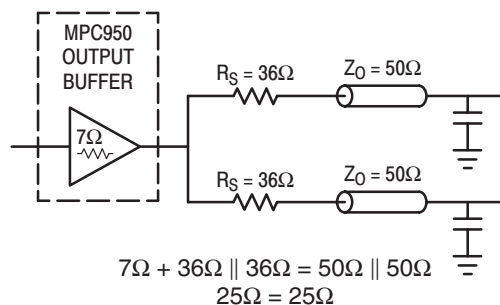


Figure 12. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Low Voltage PLL Clock Driver

The MPC951 is a 3.3V compatible, PLL based clock driver device targeted for high performance clock tree designs. With output frequencies of up to 180MHz and output skews of 375ps the MPC951 is ideal for the most demanding clock tree designs. The devices employ a fully differential PLL design to minimize cycle-to-cycle and long term jitter. This parameter is of significant importance when the clock driver is providing the reference clock for PLL's on board today's microprocessors and ASIC's. The devices offer 9 low skew outputs, the outputs are configurable to support the clocking needs of the various high performance microprocessors.

- Fully Integrated PLL
- Output Frequency up to 180MHz
- Outputs Disable in High Impedance
- Compatible with **PowerPC™**, Intel and High Performance RISC Microprocessors
- LQFP Packaging
- Output Frequency Configurable
- ± 100 ps Typical Cycle-to-Cycle Jitter

The MPC951 uses a differential PECL reference input and an external feedback input. These features allow for the MPC951 to be used as a zero delay, low skew fanout buffer. In addition, the external feedback allows for a wider variety of input-to-output frequency relationships. The REF_SEL pin allows for the selection of an alternate LVCMOS input clock to be used as a test clock or to provide the reference for the PLL from an LVCMOS source.

The MPC951 is fully 3.3V compatible and require no external loop filter components. All inputs accept LVCMOS or LVTTTL compatible levels while the outputs provide LVCMOS levels with the capability to drive terminated 50 Ω transmission lines. Select inputs do not have internal pull-up/pull-down resistors and thus must be set externally. If the PECL_CLK inputs are not used, they can be left open. For series terminated 50 Ω lines, each of the MPC951 outputs can drive two traces giving the device an effective fanout of 1:18. The device is packaged in a 7x7mm 32-lead LQFP package to provide the optimum combination of board density and performance.

MPC951

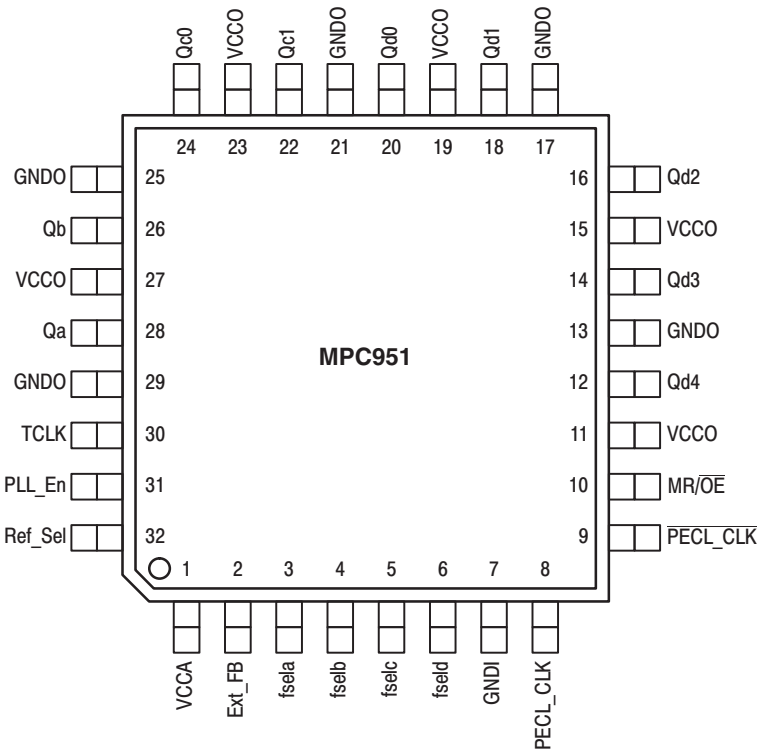
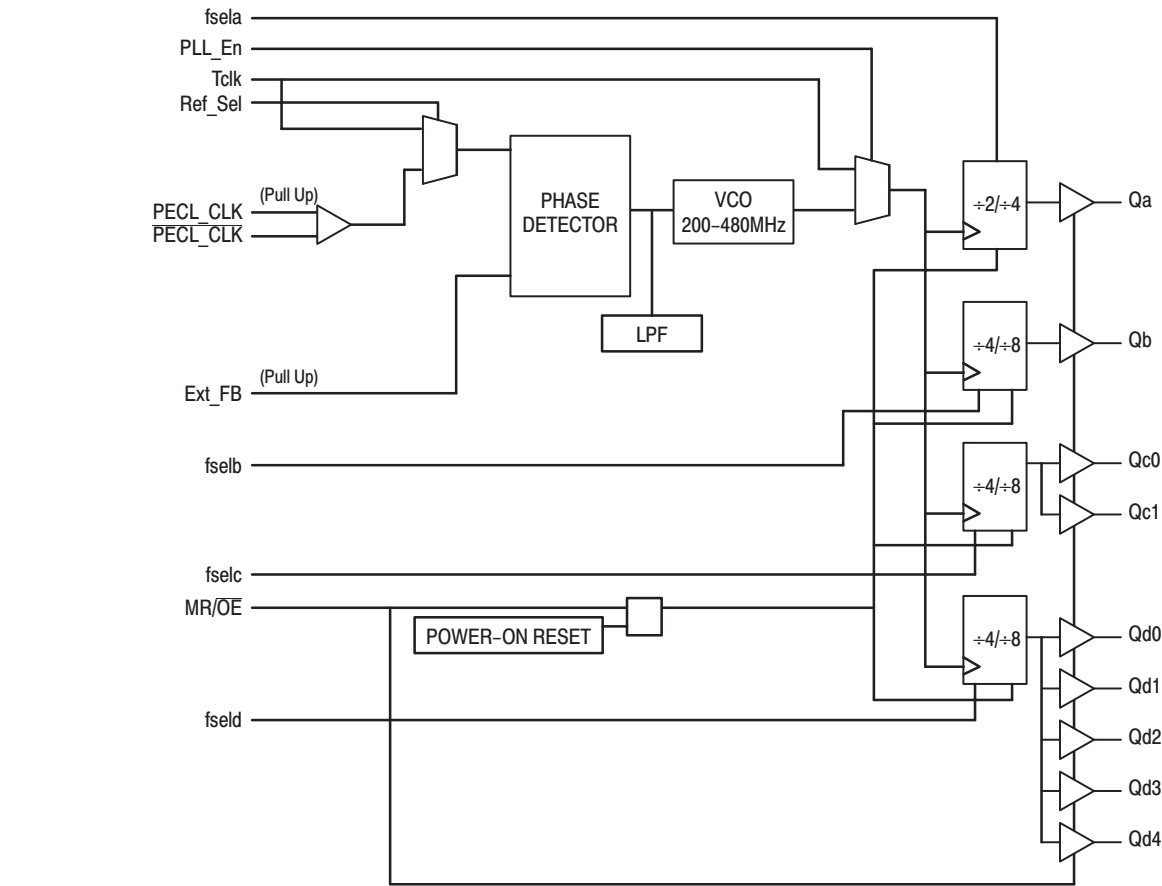
See Upgrade Product – MPC9351

LOW VOLTAGE PLL CLOCK DRIVER



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-02

MPC951 LOGIC DIAGRAM



FUNCTION TABLES

Ref_Sel	Function
1	TCLK
0	PECL_CLK

PLL_En	Function
1	PLL Enabled
0	PLL Bypass

MR/OE	Function
1	Outputs Disabled
0	Outputs Enabled

fseln	Function
1	Qa = $\div 4$; Qb:d = $\div 8$
0	Qa = $\div 2$; Qb:d = $\div 4$

FUNCTION TABLE – MPC951

INPUTS				OUTPUTS				TOTALS		
fsela	fselb	fselc	fseld	Qa(1)	Qb(1)	Qc(2)	Qd(5)	Total 2x	Total x	Total x/2
0	0	0	0	2x	x	x	x	1	8	0
0	0	0	1	2x	x	x	x/2	1	3	5
0	0	1	0	2x	x	x/2	x	1	6	2
0	0	1	1	2x	x	x/2	x/2	1	1	7
0	1	0	0	2x	x/2	x	x	1	7	1
0	1	0	1	2x	x/2	x	x/2	1	2	6
0	1	1	0	2x	x/2	x/2	x	1	3	5
0	1	1	1	2x	x/2	x/2	x/2	1	0	8
1	0	0	0	x	x	x	x	0	9	0
1	0	0	1	x	x	x	x/2	0	4	5
1	0	1	0	x	x	x/2	x	0	7	2
1	0	1	1	x	x	x/2	x/2	0	2	7
1	1	0	0	x	x/2	x	x	0	8	1
1	1	0	1	x	x/2	x	x/2	0	3	6
1	1	1	0	x	x/2	x/2	x	0	6	3
1	1	1	1	x	x/2	x/2	x/2	0	1	8

NOTE: $x = f_{VCO}/4$; $200\text{MHz} < f_{VCO} < 480\text{MHz}$.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	4.6	V
V_I	Input Voltage	-0.3	$V_{CC} + 0.3$	V
I_{IN}	Input Current		± 20	mA
T_{Stor}	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

THERMAL CHARACTERISTICS

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

DC CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage LVC MOS Inputs	2.0		3.6	V	
V_{IL}	Input LOW Voltage LVC MOS Inputs			0.8	V	
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK	300		1000	mV	
V_{CMR}	Common Mode Range PECL_CLK	$V_{CC} - 2.0$		$V_{CC} - 0.6$	V	Note 1.
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -40\text{mA}$, Note 2.
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 40\text{mA}$, Note 2.
I_{IN}	Input Current			± 120	μA	
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	Per Output
I_{CC}	Maximum Quiescent Supply Current		90	115	mA	All VCC Pins
I_{CCPLL}	Maximum PLL Supply Current		15	20	mA	VCCA Pin Only

- V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "HIGH" input is within the V_{CMR} range and the input swing lies within the V_{PP} specification.
- The MPC951 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}/2$) transmission lines on the incident edge (see Applications Info section).

PLL INPUT REFERENCE CHARACTERISTICS ($T_A = 0$ to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency		100	MHz	Note 1.
f_{refDC}	Reference Input Duty Cycle	25	75	%	

1. Maximum and minimum input reference is limited by the VCO lock range and the feedback divider for the TCLK or PECL_CLK inputs.

AC CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time	0.10		1.0	ns	0.8 to 2.0V, Note 4.
t_{pw}	Output Duty Cycle	$t_{CYCLE}/2-1000$		$t_{CYCLE}/2+1000$	ps	Note 4.
$t_{sk(O)}$	Output-to-Output Skews Same Frequencies		200	375	ps	Note 4.
	Different Frequencies Qa _{fmax} < 150MHz Qa _{fmax} > 150MHz		325	500 750		
f_{VCO}	PLL VCO Lock Range	200		480	MHz	Note 3.
f_{max}	Maximum Output Frequency Qa (+2) Qa/Qb (+4) Qb (+8)			180 120 60	MHz	Note 4.
t_{pd}	Input to Ext_FB Delay (Note 1.) TCLK PECL_CLK	50 -950	250 -770	400 -600	ps	$f_{ref} = 50\text{MHz}$ Feedback=VCO/8 Note 4.
$t_{PLZ,HZ}$	Output Disable Time			7	ns	Note 4.
t_{PZL}	Output Enable Time			6	ns	Note 4.
t_{jitter}	Cycle-to-Cycle Jitter (Peak-to-Peak)		± 100		ps	Note 2.
t_{lock}	Maximum PLL Lock Time			10	ms	

1. The t_{pd} window is specified for a 50Mhz input reference clock. The window will enlarge/reduce proportionally from the minimum limits with an increase/decrease of the input reference clock period. The t_{pd} does not include jitter.
2. See Applications Info section for more jitter information.
3. The PLL will be unstable with a divide by 2 feedback ratio.
4. Termination of 50Ω to $V_{CC}/2$.

APPLICATIONS INFORMATION**Programming the MPC951**

The MPC951 clock driver outputs can be configured into several frequency relationships. The output dividers for the four output groups allows the user to configure the outputs into 1:1, 2:1, 4:1 and 4:2:1 frequency ratios. The use of even dividers ensures that the output duty cycle is always 50%. Table 1 illustrates the various output configurations, the table describes the outputs using the VCO frequency as a reference. As an example for a 4:2:1 relationship the Qa outputs would be set at VCO/2, the Qb's and Qc's at VCO/4 and the Qd's at VCO/8. These settings will provide output frequencies with a 4:2:1 relationship.

The division settings establish the output relationship, but

one must still ensure that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL is such that for output frequencies between 25 and 180MHz the MPC951 can generally be configured into a stable region.

The relationship between the input reference and the output frequency is also very flexible. Table 1 can be used to determine the multiplication factor, there are too many potential combinations to tabularize the external feedback condition. Figure 1 through Figure 2 illustrates several programming possibilities, although not exhaustive it is representative of the potential applications.

Using the MPC951 as a Zero Delay Buffer

The external feedback of the MPC951 clock driver allows for its use as a zero delay buffer. By using one of the outputs as a feedback to the PLL the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The input reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs.

When used as a zero delay buffer the MPC951 will likely be in a nested clock tree application. For these applications the MPC951 offers a LVPECL clock input as a PLL reference. This allows the user to use LVPECL as the primary clock distribution device to take advantage of its far superior skew performance. The MPC951 then can lock onto the LVPECL refer-

ence and translate with near zero delay to low skew LVCMOS outputs. Clock trees implemented in this fashion will show significantly tighter skews than trees developed from CMOS fan-out buffers.

To minimize part-to-part skew the external feedback option again should be used. The PLL in the MPC951 decouples the delay of the device from the propagation delay variations of the internal gates. From the specification table one sees a Tpd variation of only $\pm 200\text{ps}$, thus for multiple devices under identical configurations the part-to-part skew will be around 1000ps (350ps for Tpd variation plus 350ps output-to-output skew plus 300ps for I/O jitter). By running the devices at the highest possible input reference, this part-to-part skew can be minimized. Higher input reference frequencies will minimize both I/O jitter and t_{pd} variations.

Table 1. Programmable Output Frequency Relationships

INPUTS				OUTPUTS			
fsela	fselb	fselc	fseld	Qa	Qb	Qc	Qd
0	0	0	0	VCO/2	VCO/4	VCO/4	VCO/4
0	0	0	1	VCO/2	VCO/4	VCO/4	VCO/8
0	0	1	0	VCO/2	VCO/4	VCO/8	VCO/4
0	0	1	1	VCO/2	VCO/4	VCO/8	VCO/8
0	1	0	0	VCO/2	VCO/8	VCO/4	VCO/4
0	1	0	1	VCO/2	VCO/8	VCO/4	VCO/8
0	1	1	0	VCO/2	VCO/8	VCO/8	VCO/4
0	1	1	1	VCO/2	VCO/8	VCO/8	VCO/8
1	0	0	0	VCO/4	VCO/4	VCO/4	VCO/4
1	0	0	1	VCO/4	VCO/4	VCO/4	VCO/8
1	0	1	0	VCO/4	VCO/4	VCO/8	VCO/4
1	0	1	1	VCO/4	VCO/4	VCO/8	VCO/8
1	1	0	0	VCO/4	VCO/8	VCO/4	VCO/4
1	1	0	1	VCO/4	VCO/8	VCO/4	VCO/8
1	1	1	0	VCO/4	VCO/8	VCO/8	VCO/4
1	1	1	1	VCO/4	VCO/8	VCO/8	VCO/8

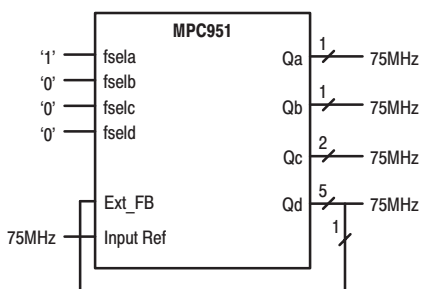


Figure 1. “Zero” Delay Buffer

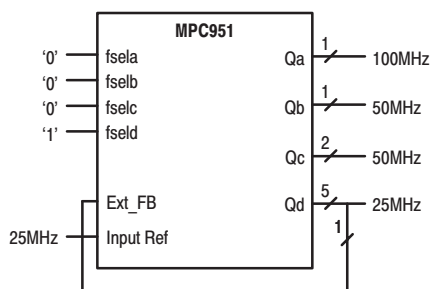


Figure 2. “Zero” Delay Frequency Multiplier

Jitter Performance of the MPC951

With the clock rates of today's digital systems continuing to increase more emphasis is being placed on clock distribution design and management. Among the issues being addressed is system clock jitter and how that affects the overall system timing budget. The MPC951 was designed to minimize clock jitter by employing a differential bipolar PLL as well as incorporating numerous power and ground pins in the design. The following few paragraphs will outline the jitter performance of the MPC951, illustrate the measurement limitations and provide guidelines to minimize the jitter of the device.

The most commonly specified jitter parameter is cycle-to-cycle jitter. Unfortunately with today's high performance measurement equipment there is no way to measure this parameter for jitter performance in the class demonstrated by the MPC951. As a result different methods are used which approximate cycle-to-cycle jitter. The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak-to-peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. If this is not the case the measurement inaccuracy

cy will add significantly to the measured jitter. The oscilloscope cannot collect adjacent pulses, rather it collects data from a very large sample of pulses. It is safe to assume that collecting pulse information in this mode will produce jitter values somewhat larger than if consecutive cycles were measured, therefore, this measurement will represent an upper bound of cycle-to-cycle jitter. Most likely, this is a conservative estimate of the cycle-to-cycle jitter.

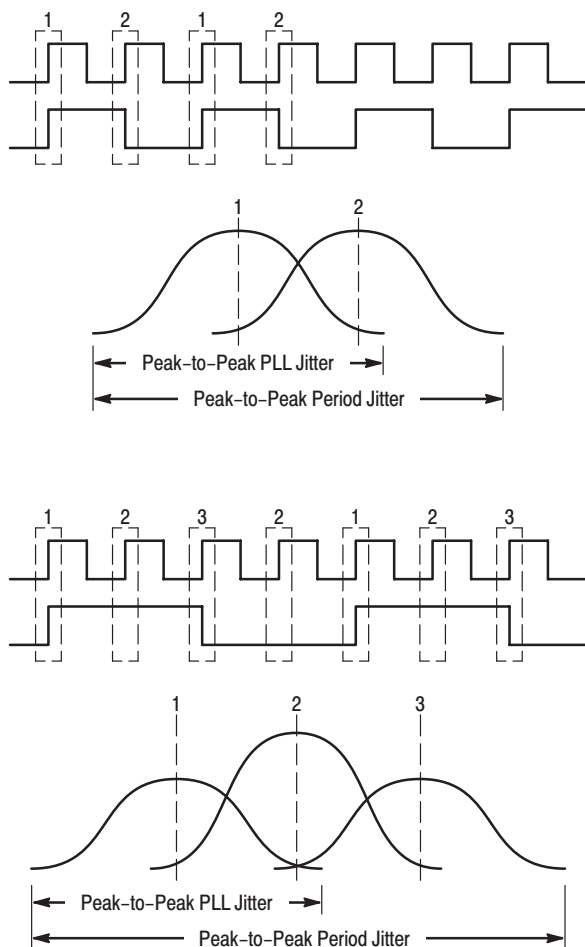


Figure 3. PLL Jitter and Edge Displacement

There are two sources of jitter in a PLL based clock driver, the commonly known random jitter of the PLL and the less intuitive jitter caused by synchronous, different frequency outputs switching. For the case where all of the outputs are switching at the same frequency the total jitter is exactly equal to the PLL jitter. In a device, like the MPC951, where a number of the outputs can be switching synchronously but at different frequencies a “multi-modal” jitter distribution can be seen on the highest frequency outputs. Because the output being monitored is affected by the activity on the other outputs it is important to consider what is happening on those other outputs. From Figure 3, one can see for each rising edge on the higher frequency signal the activity on the lower frequency signal is not constant. The activity on the other outputs tends to alter the internal thresholds of the device such that the placement of the edge being monitored is displaced in time. Because the signals are synchronous the relationship is periodic and the resulting jitter is a compilation of the PLL jitter superimposed on the dis-

placed edges. When histograms are plotted the jitter looks like a “multi-modal” distribution as pictured in Figure 3. Depending on the size of the PLL jitter and the relative displacement of the edges the “multi-modal” distribution will appear truly “multi-modal” or simply like a “fat” Gaussian distribution. Again note that in the case where all the outputs are switching at the same frequency there is no edge displacement and the jitter is reduced to that of the PLL.

Figure 4 graphically represents the PLL jitter of the MPC951. The data was taken for several different output configurations. By triggering on the lowest frequency output the PLL jitter can be measured for configurations in which outputs are switching at different frequencies. As one can see in the figure the PLL jitter is much less dependent on output configuration than on internal VCO frequency.

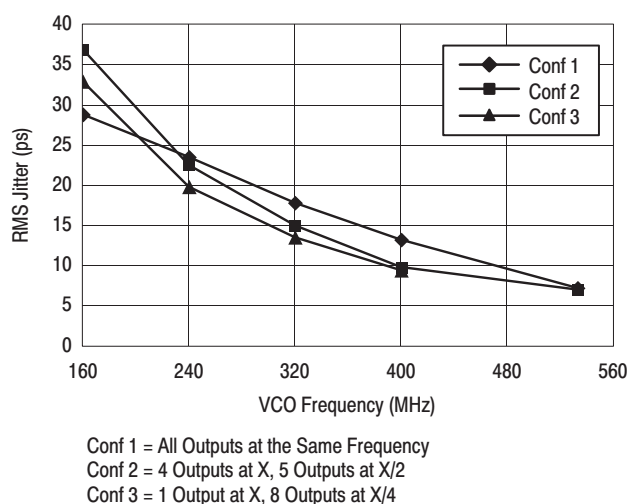


Figure 4. RMS PLL Jitter versus VCO Frequency

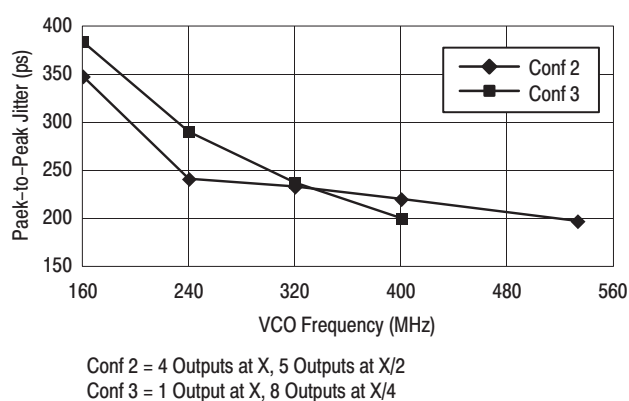


Figure 5. Peak-to-Peak Period Jitter versus VCO Frequency

Two different configurations were chosen to look at the period displacement caused by the switching outputs. Configuration 3 is considered worst case as the “trimodal” distribution (as pictured in Figure 3) represents the largest spread between distribution peaks. Configuration 2 is considered a typical configuration with half the outputs at a high frequency and the remaining outputs at one half the high frequency. For these cases the peak-to-peak numbers are reported in Figure 5 as

the sigma numbers are useless because the distributions are not Gaussian. For situations where the outputs are synchronous and switching at different frequencies the measurement technique described here is insufficient to use for establishing guaranteed limits. Other techniques are currently being investigated to identify a more accurate and repeatable measurement so that guaranteed limits can be provided. The data generated does give a good indication of the general performance, a performance that in most cases is well within the requirements of today's microprocessors.

Finally from the data there are some general guidelines that, if followed, will minimize the output jitter of the device. First and foremost always configure the device such that the VCO runs as fast as possible. This is by far the most critical parameter in minimizing jitter. Second keep the reference frequency as high as possible. More frequent updates at the phase detector will help to reduce jitter. Note that if there is a tradeoff between higher reference frequencies and higher VCO frequency always chose the higher VCO frequency to minimize jitter. The third guideline may be the most difficult, and in some cases impossible, to follow. Try to minimize the number of different frequencies sourced from a single chip. The fixed edge displacement associated with the switching noise in most cases nearly doubles the "effective" jitter of a high speed output.

Power Supply Filtering

The MPC951 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC951 provides separate power supplies for the output buffers (VCCO) and the phase-locked loop (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC951.

Figure 6 illustrates a typical power supply filter scheme. The MPC951 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the VCC supply and the VCCA pin of the MPC951. From the data sheet the I_{VCCA} current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V VCC supply is used. The resistor shown in Figure 6 must have a resistance of 10–15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency

crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8–10 Ω resistor to avoid potential VCC drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

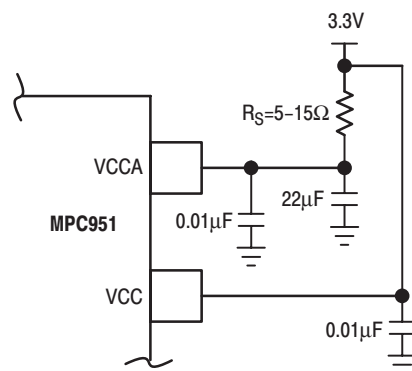


Figure 6. Power Supply Filter

Although the MPC951 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC951 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC951 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 7 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fan-out of the MPC951 clock driver is effectively doubled due to its capability to drive multiple lines.

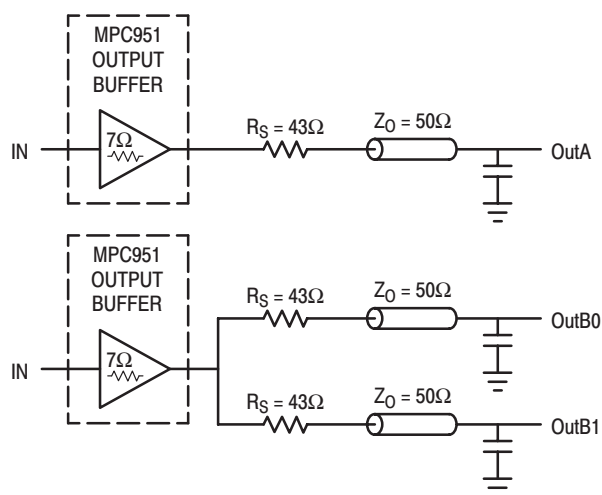


Figure 7. Single versus Dual Transmission Lines

The waveform plots of Figure 8 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC951 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC951. The output waveform in Figure 8 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_o / (R_s + R_o + Z_o))$$

$$Z_o = 50\Omega \parallel 50\Omega$$

$$R_s = 43\Omega \parallel 43\Omega$$

$$R_o = 7\Omega$$

$$V_L = 3.0 (25 / (21.5 + 7 + 25)) = 3.0 (25 / 53.5) \\ = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

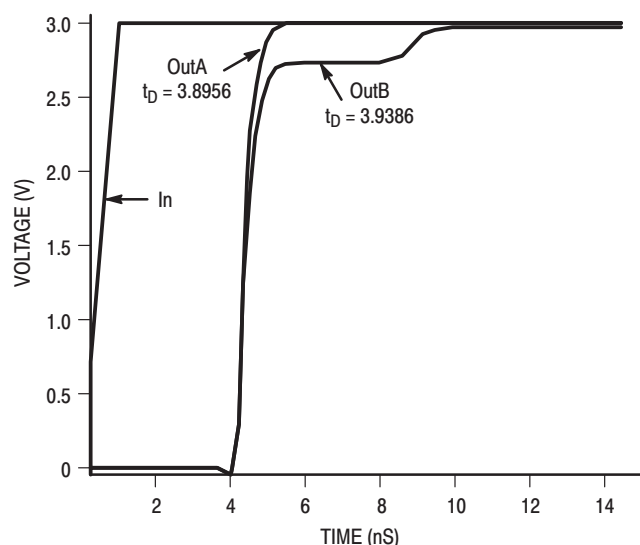


Figure 8. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 9 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

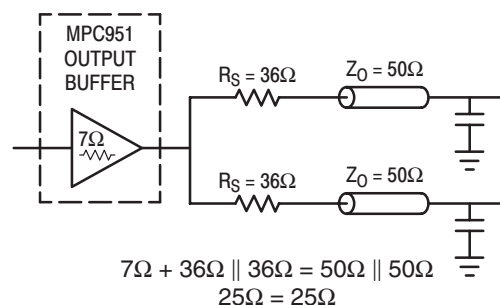


Figure 9. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Low Voltage PLL Clock Driver

The MPC952 is a 3.3V compatible, PLL based clock driver device targeted for high performance clock tree applications. The device features a fully integrated PLL with no external components required. With output frequencies of up to 180MHz and eleven low skew outputs the MPC952 is well suited for high performance designs. The device employs a fully differential PLL design to optimize jitter and noise rejection performance. Jitter is an increasingly important parameter as more microprocessors and ASIC's are employing on chip PLL clock distribution.

- Fully Integrated PLL
- Output Frequency up to 180MHz
- High Impedance Disabled Outputs
- Compatible with **PowerPC™**, Intel and High Performance RISC Microprocessors
- Output Frequency Configurable
- LQFP Packaging
- ± 100 ps Cycle-to-Cycle Jitter

The MPC952 features three banks of individually configurable outputs. The banks contain 5 outputs, 4 outputs and 2 outputs. The internal divide circuitry allows for output frequency ratios of 1:1, 2:1, 3:1 and 3:2:1. The output frequency relationship is controlled by the fsel frequency control pins. The fsel pins as well as the other inputs are LVCMOS/LVTTL compatible inputs.

The MPC952 uses external feedback to the PLL. This features allows for the use of the device as a "zero delay" buffer. Any of the eleven outputs can be used as the feedback to the PLL. The VCO_Sel pin allows for the choice of two VCO ranges to optimize PLL stability and jitter performance. The MR/OE pin allows the user to force the outputs into high impedance for board level test.

For system debug the PLL of the MPC952 can be bypassed. When forced to a logic HIGH, the PLEN input will route the signal on the RefClk input around the PLL directly to the internal dividers. Because the signal is routed through the dividers, it may take several transitions of the RefClk to affect a transition on the outputs. This features allows a designer to single step the design for debug purposes.

The outputs of the MPC952 are LVCMOS outputs. The outputs are optimally designed to drive terminated transmission lines. For applications using series terminated transmission lines each MPC952 output can drive two lines. This capability provides an effective fanout of 22, more than enough clocks for most clock tree designs. For more information on driving transmission lines consult the applications section of this data sheet.

MPC952

See Upgrade Product – MPC9352

LOW VOLTAGE PLL CLOCK DRIVER

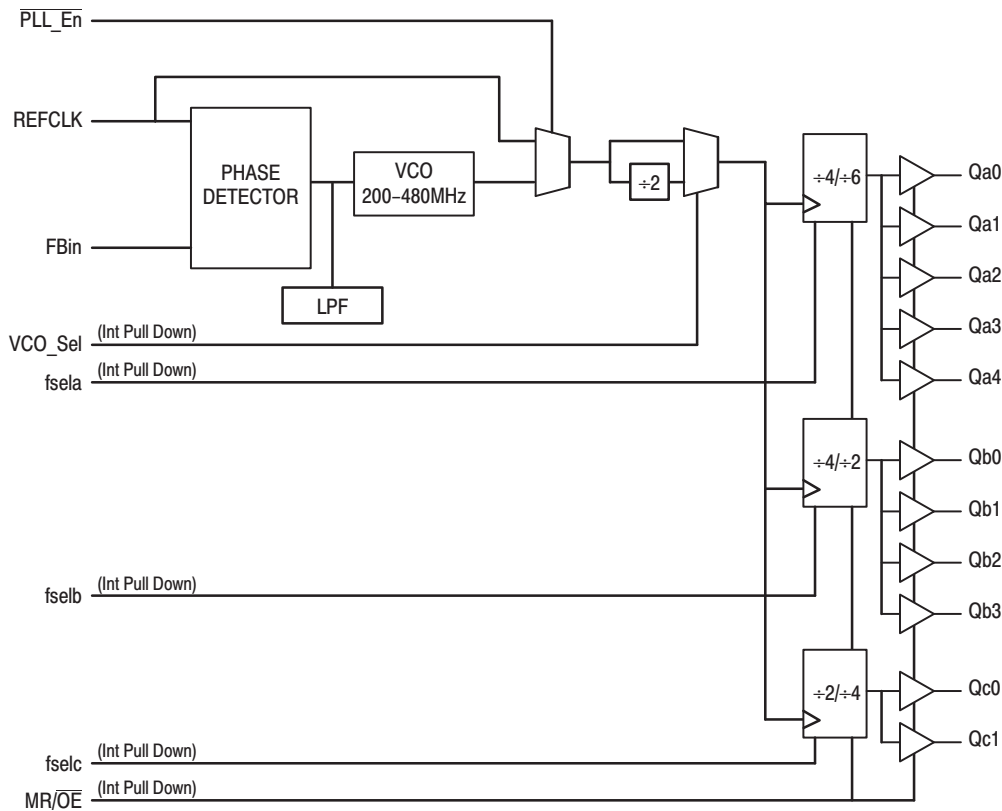


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Rev 5

Figure 1. MPC952 Logic Diagram



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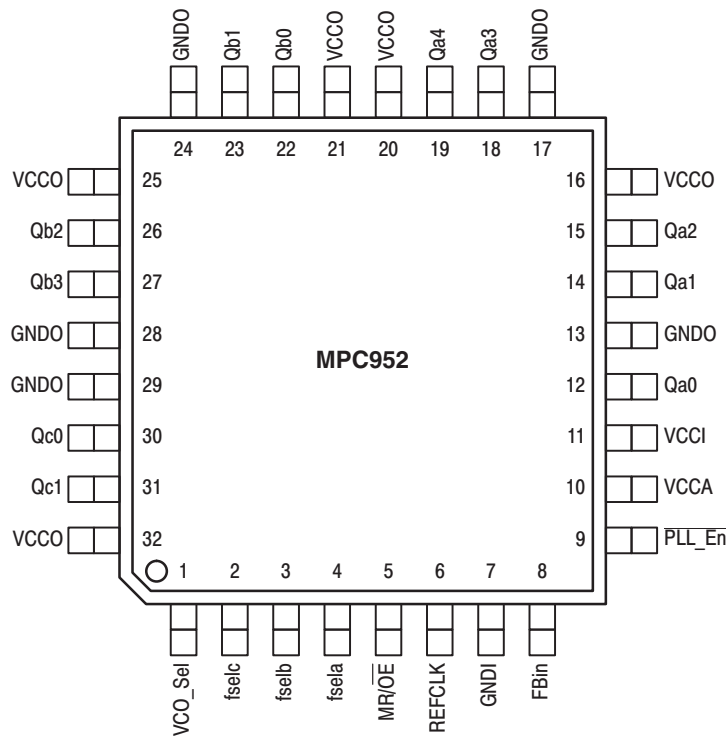


Figure 2. 32-Lead Pinout (Top View)

FUNCTION TABLES

fsela	Qan	fselb	Qbn	fselc	Qcn
0	÷4	0	÷4	0	÷2
1	÷6	1	÷2	1	÷4

Control Pin	Logic '0'	Logic '1'
VCO_Sel	fVCO	fVCO/2
MR/OE	Output Enable	High Z
PLL_En	Enable PLL	Disable PLL

Pin Name	Description
VCCA	PLL Power Supply
VCCO	Output Buffer Power Supply
VCCI	Internal Core Logic Power Supply
GNDI	Internal Ground
GND0	Output Buffer Ground

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	4.6	V
V_I	Input Voltage	-0.3	$V_{CC} + 0.3$	V
I_{IN}	Input Current		± 20	mA
T_{Stor}	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

THERMAL CHARACTERISTICS

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CCO} = V_{CCI} = V_{CCA} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		3.6	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -20\text{mA}$ (Note 1.)
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 20\text{mA}$ (Note 1.)
I_{IN}	Input Current			± 120	μA	Note 2.
C_{IN}	Input Capacitance		2.7	4.0	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	
I_{CC}	Maximum Quiescent Supply Current			160	mA	Total ICC Static Current
I_{CCA}	PLL Supply Current		15	20	mA	

1. The MPC952 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CCO}/2$) transmission lines on the incident edge (see Applications Info section).
2. Inputs have pull-up, pull-down resistors which affect input current.

PLL INPUT REFERENCE CHARACTERISTICS ($T_A = 0$ to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency		100	MHz	Note 3.
f_{refDC}	Reference Input Duty Cycle	25	75	%	

3. Maximum and minimum input reference is limited by the VCO lock range and the feedback divider.

AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC0} = V_{CCI} = V_{CCA} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time (Note 4.)	0.10		1.0	ns	0.8 to 2.0V
t_{pw}	Output Pulse Width (Note 4.)	$t_{CYCLE}/2$ -750	$t_{CYCLE}/2$ ± 500	$t_{CYCLE}/2$ +750	ps	
t_{os}	Output-to-Output Skew (Note 4.)			350 450 550	ps	Same Frequencies Same Frequencies Different Frequencies
f_{VCO}	PLL VCO Lock Range	200		480	MHz	Note 6.
f_{max}	Maximum Output Frequency Qc,Qb (+2) Qa,Qb,Qc (+4) Qa (+6)	180 120 80			MHz	Note 4.
t_{pd}	REFCLK to FBIN Delay	-200	0	200	ps	Notes 4., 5.
t_{PLZ}, t_{PHZ}	Output Disable Time	2		8	ns	Note 4.
t_{PZL}, t_{PLH}	Output Enable Time	2		10	ns	Note 4.
$t_{jit(cc)}$	Cycle-to-Cycle Jitter		± 100		ps	
t_{lock}	Maximum PLL Lock Time			10	ms	

4. Termination of 50Ω to $V_{CC0}/2$.

5. t_{pd} is specified for 50MHz input ref, the window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The t_{pd} does not include jitter.

6. The PLL may be unstable with a divide by 2 feedback ratio.

APPLICATIONS INFORMATION**Driving Transmission Lines**

The MPC952 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 7Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091.

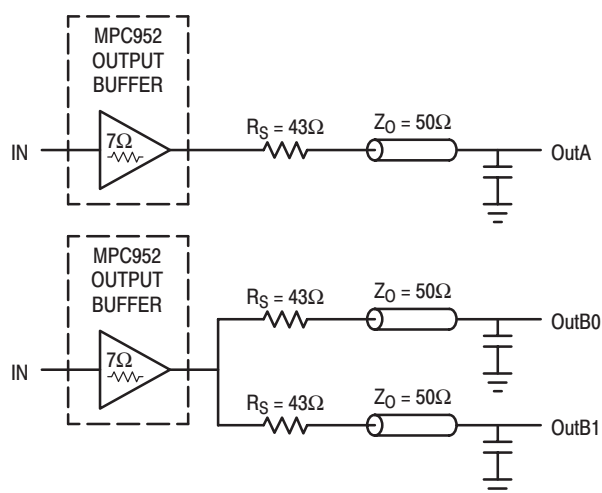


Figure 3. Single versus Dual Transmission Lines

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated

transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC0}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC952 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fan-out of the MPC952 clock driver is effectively doubled due to its capability to drive multiple lines.

The waveform plots of Figure 4 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC952 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC952. The output waveform in Figure 4 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_o / R_s + R_o + Z_o) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

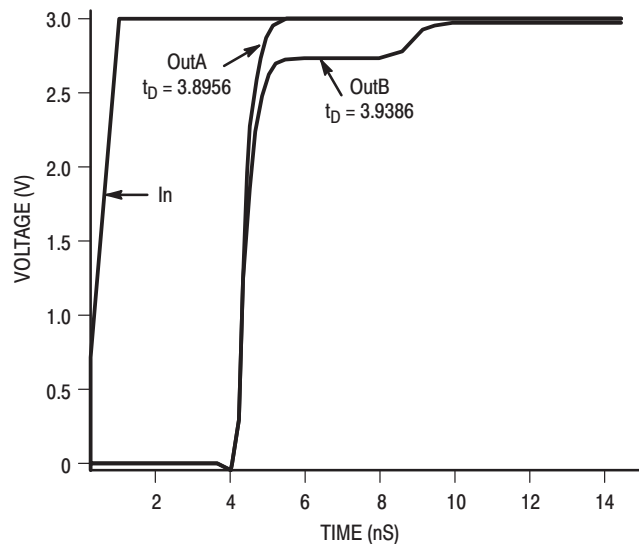


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

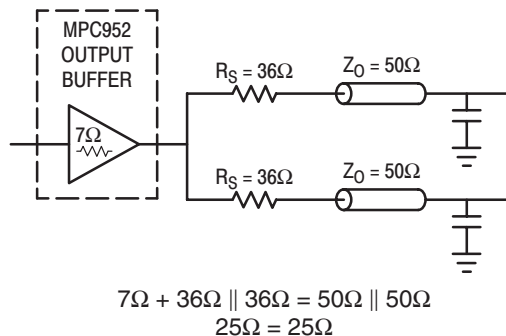


Figure 5. Optimized Dual Line Termination

Power Supply Filtering

The MPC952 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC952 provides separate power supplies for the output buffers (V_{CCO}) and the internal PLL (V_{CCA}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The sim-

plest form of isolation is a power supply filter on the V_{CCA} pin for the MPC952.

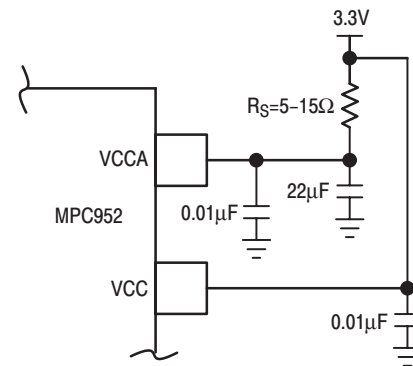


Figure 6. Power Supply Filter

Figure 6 illustrates a typical power supply filter scheme. The MPC952 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the MPC952. From the data sheet the $I_{V_{CCA}}$ current (the current sourced through the V_{CCA} pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.3V – 5% must be maintained on the V_{CCA} pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 6 must have a resistance of 5–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC952 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

2

Low Voltage 2.5 V and 3.3 V CMOS PLL Clock Driver

The MPC9600 is a low voltage 2.5 V or 3.3 V compatible, 1:21 PLL based clock driver and fanout buffer. With output frequencies up to 200 MHz and output skews of 150 ps, the device meets the needs of the most demanding clock tree applications.

Features:

- Multiplication of input frequency by 2, 3, 4 and 6
- Distribution of output frequency to 21 outputs organized in three output banks: QA0-QA6, QB0-QB6, QC0-QC6, each fully selectable
- Fully integrated PLL
- Selectable output frequency range is 50 to 100 MHz and 100 to 200 MHz
- Selectable input frequency range is 16.67 to 33 MHz and 25 to 50 MHz
- LVC MOS outputs
- Outputs disable to high impedance (except QFB)
- LVC MOS or LVPECL reference clock options
- 48 lead QFP packaging
- ± 50 ps cycle-to-cycle jitter
- 150 ps maximum output-to-output skew
- 200 ps maximum static phase offset window

The MPC9600 is a fully LVC MOS 2.5 V or 3.3 V compatible PLL clock driver. The MPC9600 has the capability to generate clock signals of 50 to 200 MHz from clock sources of 16.67 to 50 MHz. The internal PLL is optimized for this frequency range and does not require external loop filter components. QFB provides an output for the external feedback path to the feedback input FB_IN. The QFB divider ratio is configurable and determines the PLL frequency multiplication factor when QFB is directly connected to FB_IN. The MPC9600 is optimized for minimizing the propagation delay between the clock input and FB_IN.

Three output banks of 7 outputs each bank can be individually configured to divide the VCO frequency by 2 or by 4. Combining the feedback and output divider ratios, the MPC9600 is capable to multiply the input frequency by 2, 3, 4 and 6.

The reference clock is selectable either LVPECL or LVC MOS. The LVPECL reference clock feature allows the designer to use LVPECL fanout buffers for the inner branches of the clock distribution tree. All control inputs accept LVC MOS compatible levels. The outputs provide low impedance LVC MOS outputs capable of driving parallel terminated 50 Ω transmission to $V_{TT}=V_{CC}/2$. For series terminated lines the MPC9600 can drive two lines per output giving the device an effective total fanout of 1:42. With guaranteed maximum output-to-output skew of 150 ps, the MPC9600 PLL clock driver meets the synchronization requirements of the most demanding systems.

The V_{CCA} analog power pin doubles as a PLL bypass select line for test purpose. When the V_{CCA} is driven to GND the reference clock will bypass the PLL.

The device is packaged in a 48-lead LQFP package to provide optimum combination of board density and performance.

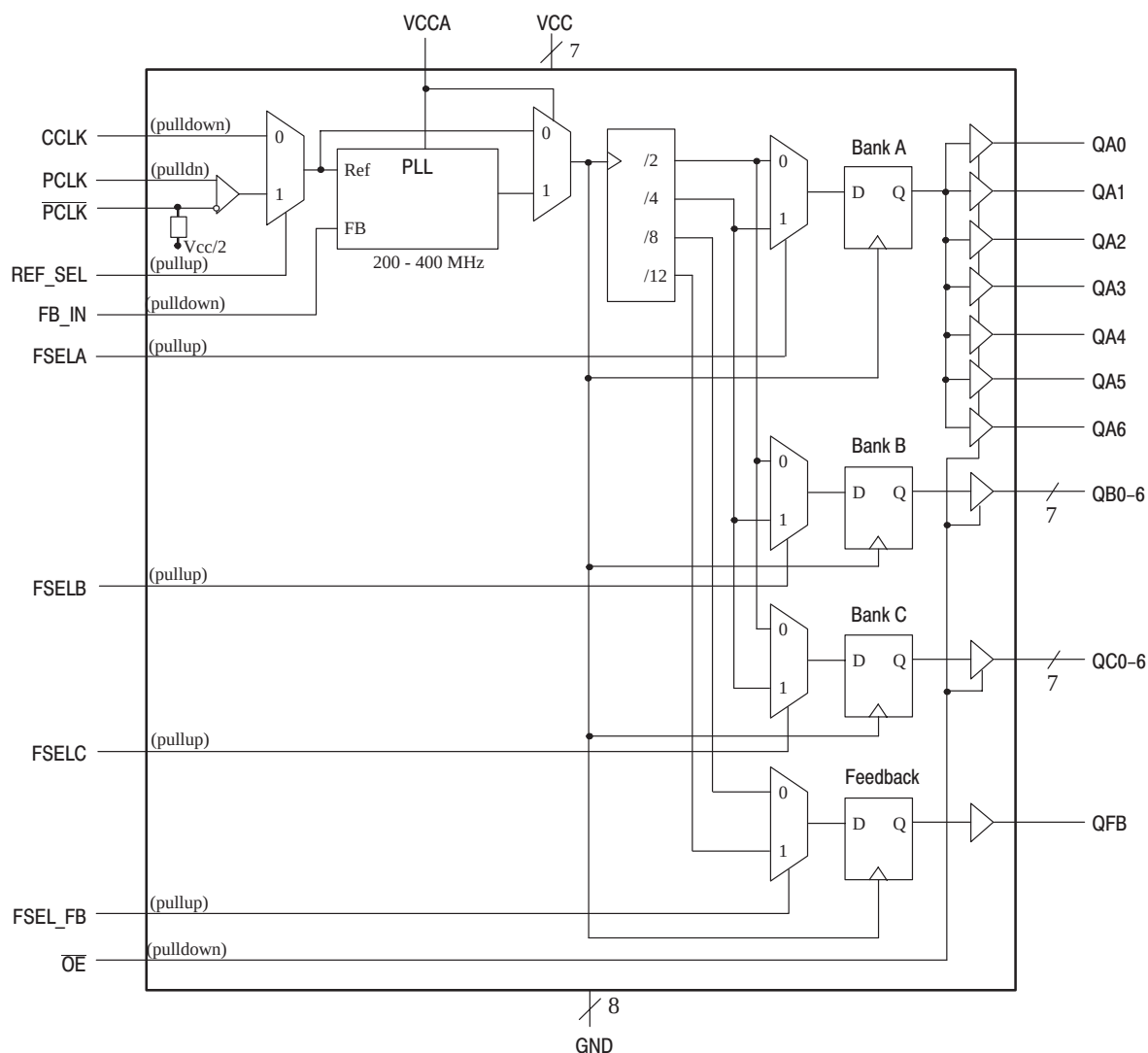
Rev 2

MPC9600

**3.3 V OR 2.5 V
LOW VOLTAGE CMOS
PLL CLOCK DRIVER**



FA SUFFIX
48-LEAD LQFP PACKAGE
CASE 932-03



PIN CONFIGURATION

Pin	I/O	Type	Description
PCLK, PCLK	Input	PECL	Differential reference clock frequency input
CCLK	Input	LVC MOS	Reference clock input
FB_IN	Input	LVC MOS	PLL feedback clock input
QAn	Output	LVC MOS	Bank A outputs
QBn	Output	LVC MOS	Bank B outputs
QCn	Output	LVC MOS	Bank C outputs
QFB	Output	LVC MOS	Differential feedback output
REF_SEL	Input	LVC MOS	Reference clock input select
FSELA	Input	LVC MOS	Selection of bank A output frequency
FSELB	Input	LVC MOS	Selection of bank B output frequency
FSELC	Input	LVC MOS	Selection of bank C output frequency
FSEL_FB	Input	LVC MOS	Selection of feedback frequency
OE	Input	LVC MOS	Output enable
VCCA		Power supply	Analog power supply and PLL bypass. An external VCC filter is recommended for VCCA
VCC		Power supply	Core power supply
GND		Ground	Ground

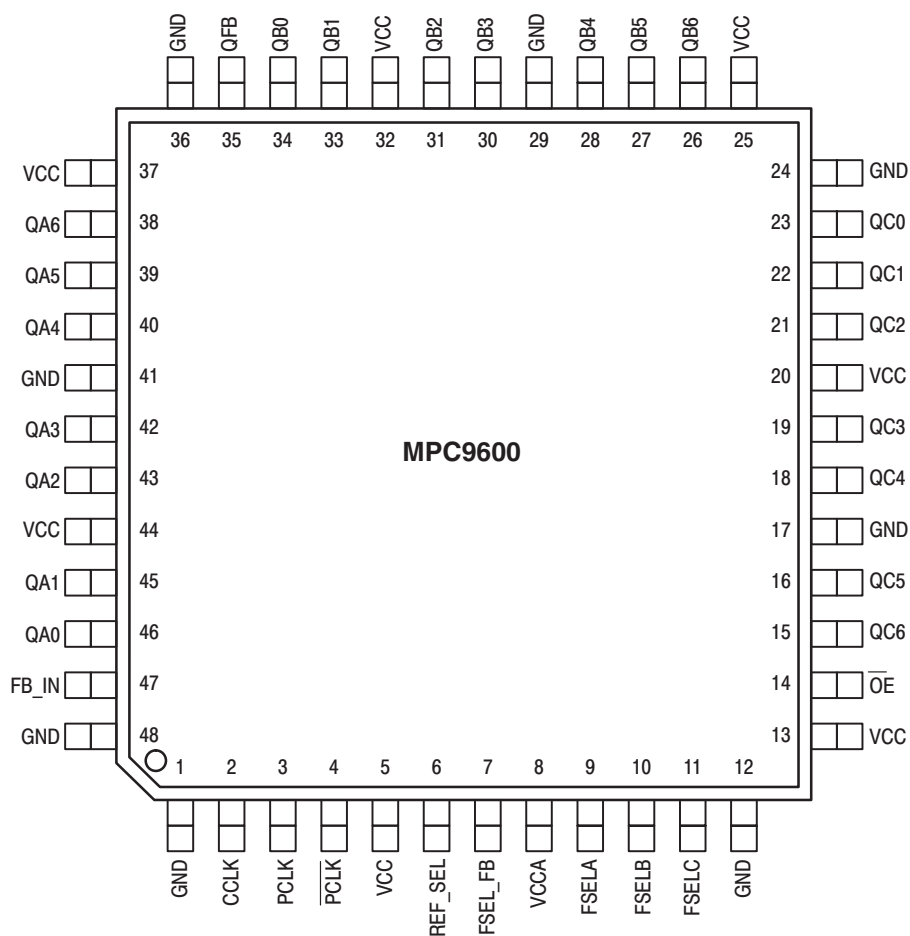


Figure 2. 48 Lead Package Pinout (Top View)

FUNCTION TABLE (CONTROLS)

Control Pin	0	1
REF_SEL	CCLK	PCLK
VCCA	PLL Bypass ¹	PLL Power
OE	Outputs Enabled	Outputs Disabled (except QFB)
FSELA	Output Bank A at VCO/2	Output Bank A at VCO/4
FSELB	Output Bank B at VCO/2	Output Bank B at VCO/4
FSELC	Output Bank C at VCO/2	Output Bank C at VCO/4
FSEL_FB	Feedback Output at VCO/8	Feedback Output at VCO/12

1. VCCA = GND, PLL off and bypassed for static test and diagnosis

Table 1: ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	−0.3	4.6	V
V _{IN}	DC Input Voltage	−0.3	V _{CC} + 0.3	V
V _{OUT}	DC Output Voltage	−0.3	V _{CC} + 0.3	V
I _{IN}	DC Input Current		±20	mA
I _{OUT}	DC Output Current		±50	mA
T _{Stor}	Storage Temperature Range	−40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 2: GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output Termination Voltage		V _{CC} ÷ 2		V	
MM	ESD Protection (Machine Model)	400			V	
HBM	ESD Protection (Human Body Model)	4000			V	
CDM	ESD Protection (Charged Device Model)	1500			V	
LU	Latch-Up Immunity	200			mA	
C _{PD}	Power Dissipation Capacitance		10		pF	Per output
C _{IN}	Input Capacitance		4.0		pF	Inputs

Table 3: DC CHARACTERISTICS (V_{CC} = 3.3 V ±5%, T_A = −40° to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{IH}	Input High Voltage	2.0		V _{CC} + 0.3	V	LVC MOS
V _{IL}	Input Low Voltage			0.8	V	LVC MOS
V _{PP}	Peak-to-peak Input Voltage (DC) PCLK, PCLK	250			mV	LVPECL
V _{CMR} ^a	Common Mode Range (DC) PCLK, PCLK	1.0		V _{CC} -0.6	V	LVPECL
V _{OH}	Output High Voltage	2.4			V	I _{OH} = −24 mA ^b
V _{OL}	Output Low Voltage			0.55 0.30	V V	I _{OL} = 24mA I _{OL} = 12mA
Z _{OUT}	Output Impedance		14 – 17		Ω	
I _{IN}	Input Leakage Current			±150	μA	V _{IN} = V _{CC} or GND
I _{CCA}	Maximum PLL Supply Current		2.0	5.0	mA	V _{CCA} Pin
I _{CCQ}	Maximum Quiescent Supply Current			1.0	mA	All V _{CC} Pins

a. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.

b. The MPC9600 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

Table 4: DC CHARACTERISTICS ($V_{CC} = 2.5 \text{ V} \pm 5\%$, $T_A = -40^\circ$ to $+85^\circ\text{C}$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	1.7		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input Low Voltage			0.7	V	LVC MOS
V_{PP}	Peak-to-peak input voltage (DC) PCLK, $\overline{\text{PCLK}}$	250			mV	LVPECL
V_{CMR}^a	Common Mode Range (DC) PCLK, $\overline{\text{PCLK}}$	1.0		$V_{CC} - 0.6$	V	LVPECL
V_{OH}	Output High Voltage	1.8			V	$I_{OH} = -15 \text{ mA}^b$
V_{OL}	Output Low Voltage			0.6	V	$I_{OL} = 15 \text{ mA}$
Z_{OUT}	Output Impedance		17 – 20		Ω	
I_{IN}	Input Leakage Current			± 150	μA	$V_{IN} = V_{CC}$ or GND
I_{CCA}	Maximum PLL Supply Current		3.0	5.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins

- a. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
- b. The MPC9600 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50 Ω series terminated transmission lines per output.

Table 5: AC CHARACTERISTICS ($V_{CC} = 3.3 \text{ V} \pm 5\%$ or $V_{CC} = 2.5 \text{ V} \pm 5\%$, $T_A = -40^\circ$ to $+85^\circ\text{C}$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency ÷ 8 feedback (FSEL_FB=0) ÷ 12 feedback (FSEL_FB=1) Static test mode ($V_{CCA} = \text{GND}$)	25 16.67 0		50 33 500	MHz MHz MHz	PLL locked PLL locked $V_{CCA} = \text{GND}$
f_{VCO}	VCO Frequency	200		400	MHz	
f_{MAX}	Maximum Output Frequency ÷ 2 outputs (FSELx=0) ÷ 4 outputs (FSELx=1)	100 50		200 100	MHz MHz	PLL locked PLL locked
f_{refDC}	Reference Input Duty Cycle	25		75	%	
V_{PP}	Peak-to-peak Input Voltage PCLK, $\overline{\text{PCLK}}$	500		1000	mV	LVPECL
V_{CMR}^b	Common Mode Range PCLK, $\overline{\text{PCLK}}$ ($V_{CC} = 3.3 \text{ V} \pm 5\%$) PCLK, $\overline{\text{PCLK}}$ ($V_{CC} = 2.5 \text{ V} \pm 5\%$)	1.2 1.2		$V_{CC} - 0.8$ $V_{CC} - 0.6$	V V	LVPECL LVPECL
t_r, t_f	CCLK Input Rise/Fall Time			1.0	ns	see Figure 12
$t_{(\odot)}$	Propagation Delay (static phase offset) CCLK to FB_IN PECL_CLK to FB_IN	-60 +30	+40 +130	+140 +230	ps ps	PLL locked PLL locked
$t_{sk(o)}$	Output-to-output Skew all outputs, single frequency all outputs, multiple frequency within QAx output bank within QBx outputs within QCx outputs		70 70 30 40 30	150 150 75 125 75	ps ps ps ps ps	Measured at coincident rising edge
DC	Output Duty Cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	see Figure 12
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, ZH}$	Output Enable Time			10	ns	
BW	PLL Closed Loop Bandwidth ÷ 8 feedback (FSEL_FB=0) ÷ 12 feedback (FSEL_FB=1)		1.0 – 10 0.6 – 4.0		MHz MHz	-3 dB point of PLL transfer characteristic

Table 5: AC CHARACTERISTICS ($V_{CC} = 3.3\text{ V} \pm 5\%$ or $V_{CC} = 2.5\text{ V} \pm 5\%$, $T_A = -40^\circ$ to $+85^\circ\text{C}$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
$t_{JIT(CC)}$	Cycle-to-cycle Jitter ^c All outputs in $\div 2$ configuration All outputs in $\div 4$ configuration		40 40	130 180	ps ps	See application section for other configurations
$t_{JIT(PER)}$	Period Jitter ^c All outputs in $\div 2$ configuration All outputs in $\div 4$ configuration		25 20	70 100	ps ps	See application section for other configurations
$t_{JIT(\emptyset)}$	I/O Phase Jitter (1σ) $V_{CC} = 3.3\text{V}$ $V_{CC} = 2.5\text{V}$			17 ^d 15 ^c	ps ps	RMS value at $f_{VCO}=400\text{MHz}$
t_{LOCK}	Maximum PLL Lock Time			5.0	ms	

- a. AC characteristics are applicable over the entire ambient temperature and supply voltage range and are production tested. AC characteristics apply for parallel output termination of $50\ \Omega$ to V_{TT} .
- b. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\emptyset)}$.
- c. Cycle-to-cycle and period jitter depends on output divider configuration.
- d. See applications section for max I/O phase jitter versus frequency.

APPLICATIONS INFORMATION

Programming the MPC9600

The MPC9600 clock driver outputs can be configured into several divider modes. Additionally the external feedback of the device allows for flexibility in establishing various input to output frequency relationships. The selectable feedback divider of the three output groups allows the user to configure the device for 1:2, 1:3, 1:4 and 1:6 input:output frequency ratios. The use of even dividers ensure that the output duty cycle is always 50%. Table 6 illustrates the various output configura-

tions, the table describes the outputs using the input clock frequency CLK as a reference.

The feedback divider division settings establish the output relationship, in addition, it must be ensured that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL supports output frequencies from 50 MHz to 200 MHz while the VCO frequency range is specified from 200 MHz to 400 MHz and should not be exceeded for stable operation.

Table 6: Output Frequency Relationship^a for QFB connected to FB_IN

Configuration Inputs				Input Frequency Range CLK [MHz]	Output Frequency Ratio and Range		
FSEL_FB	FSELA	FSELB	FSELC		Ratio, QAx [MHz]	Ratio, QBx [MHz]	Ratio, QCx [MHz]
0	0	0	0	25.0–50.0	4•CLK (100–200)	4•CLK (100–200)	4•CLK (100–200)
0	0	0	1		4•CLK (100–200)	4•CLK (100–200)	2•CLK (50.0–100)
0	0	1	0		4•CLK (100–200)	2•CLK (50.0–100)	4•CLK (100–200)
0	0	1	1		4•CLK (100–200)	2•CLK (50.0–100)	2•CLK (50.0–100)
0	1	0	0		2•CLK (50.0–100)	4•CLK (100–200)	4•CLK (100–200)
0	1	0	1		2•CLK (50.0–100)	4•CLK (100–200)	2•CLK (50.0–100)
0	1	1	0		2•CLK (50.0–100)	2•CLK (50.0–100)	4•CLK (100–200)
0	1	1	1		2•CLK (50.0–100)	2•CLK (50.0–100)	2•CLK (50.0–100)
1	0	0	0	16.67–33.33	6•CLK (100–200)	6•CLK (100–200)	6•CLK (100–200)
1	0	0	1		6•CLK (100–200)	6•CLK (100–200)	3•CLK (50.0–100)
1	0	1	0		6•CLK (100–200)	3•CLK (50.0–100)	6•CLK (100–200)
1	0	1	1		6•CLK (100–200)	3•CLK (50.0–100)	3•CLK (50.0–100)
1	1	0	0		3•CLK (50.0–100)	6•CLK (100–200)	6•CLK (100–200)
1	1	0	1		3•CLK (50.0–100)	6•CLK (100–200)	3•CLK (50.0–100)
1	1	1	0		3•CLK (50.0–100)	3•CLK (50.0–100)	6•CLK (100–200)
1	1	1	1		3•CLK (50.0–100)	3•CLK (50.0–100)	3•CLK (50.0–100)

a. Output frequency relationship with respect to input reference frequency CLK. The VCO frequency range is always 200–400.

Typical and Maximum Period Jitter Specification

Device Configuration	QA0 to QA6		QB0 to QB6		QC0 to QC6	
	Typ	Max	Typ	Max	Typ	Max
All output banks in ÷ 2 or ÷ 4 divider configuration ^a ÷ 2 (FSELA=0 and FESLB=0 and FSELC=0) ÷ 4 (FSELA=1 and FESLB=1 and FSELC=1)	25	50	50	70	25	50
	20	70	50	100	20	70
Mixed ÷ 2/ ÷ 4 divider configurations ^b for output banks in ÷ 2 divider configurations for output banks in ÷ 4 divider configurations	80	130	100	150	80	130
	25	70	60	100	25	70

a. In this configuration, all MPC9600 outputs generate the same clock frequency. See Figure 1 for an example configuration.

b. Multiple frequency generation. Jitter data are specified for each output divider separately. See Figure 2 for an example.

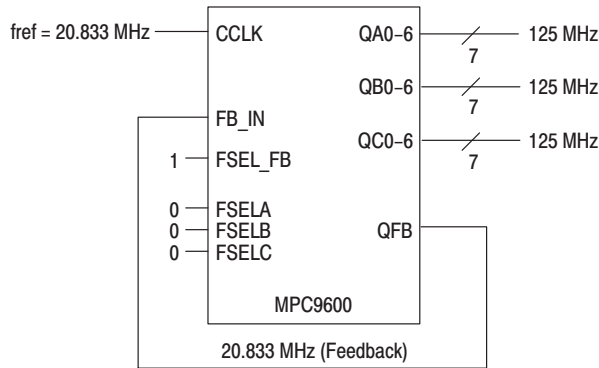
Typical and Maximum Cycle-to-cycle Jitter Specification

Device Configuration	QA0 to QA6		QB0 to QB6		QC0 to QC6	
	Typ	Max	Typ	Max	Typ	Max
All output banks in ÷ 2 or ÷ 4 divider configuration ^a ÷ 2 (FSELA=0 and FESLB=0 and FSELC=0) ÷ 4 (FSELA=1 and FESLB=1 and FSELC=1)	40	90	80	130	40	90
	40	110	120	180	40	110
Mixed ÷ 2/ ÷ 4 divider configurations ^b for output banks in ÷ 2 divider configurations for output banks in ÷ 4 divider configurations	150	250	200	280	150	250
	30	110	120	180	30	110

a. In this configuration, all MPC9600 outputs generate the same clock frequency.

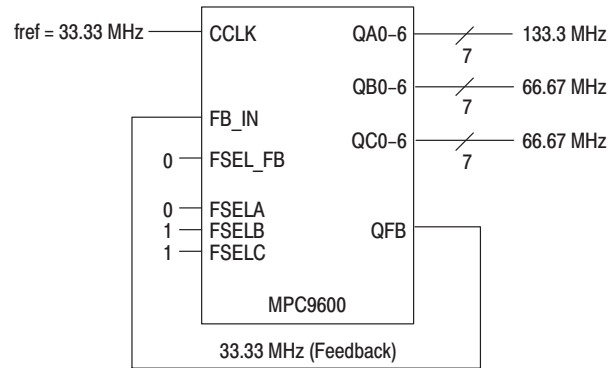
b. Multiple frequency generation. Jitter data are specified for each output divider separately.

Figure 3. Configuration for 125 MHz clocks



Frequency range	Min	Max
Input	16.67 MHz	33.33 MHz
QA outputs	100 MHz	200 MHz
QB outputs	100 MHz	200 MHz
QC outputs	100 MHz	200 MHz

Figure 4. Configuration for 133.3/66.67 MHz clocks

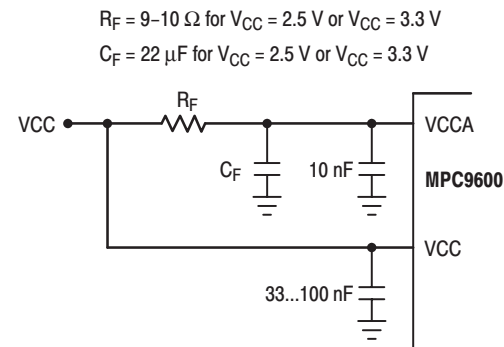


Frequency range	Min	Max
Input	25 MHz	50 MHz
QA outputs	100 MHz	200 MHz
QB outputs	100 MHz	200 MHz
QC outputs	100 MHz	200 MHz

Power Supply Filtering

The MPC9600 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9600 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC9600. Figure 5 illustrates a typical power supply filter scheme. The MPC9600 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F . From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325 V ($V_{CC}=3.3$ V or $V_{CC}=2.5$ V) must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 5 "V_{CCA} Power Supply Filter" must have a resistance of 9-10 Ω ($V_{CC}=2.5$ V) to meet the voltage drop criteria.

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 5 "V_{CCA} Power Supply Filter", the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

Figure 5. V_{CCA} Power Supply Filter

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9600 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9600 in zero-delay applications

Nested clock trees are typical applications for the MPC9600. For these applications the MPC9600 offers a differential LVPECL clock input pair as a PLL reference. This allows for the use of differential LVPECL primary clock distribution devices such as the Motorola MC100ES6111 or MC100ES6226, taking advantage of its superior low-skew performance. Clock trees using LVPECL for clock distribution and the MPC9600 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers.

The external feedback option of the MPC9600 PLL allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge and virtually eliminates the propagation delay through the device.

The remaining insertion delay (skew error) of the MPC9600 in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset (SPO or $t_{(\varnothing)}$), I/O jitter ($t_{JIT(\varnothing)}$), phase or long-term jitter, feedback path delay and the output-to-output skew ($t_{SK(O)}$) relative to the feedback output.

Calculation of part-to-part skew

The MPC9600 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs (CCLK or PCLK) of two or more MPC9600 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD, LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

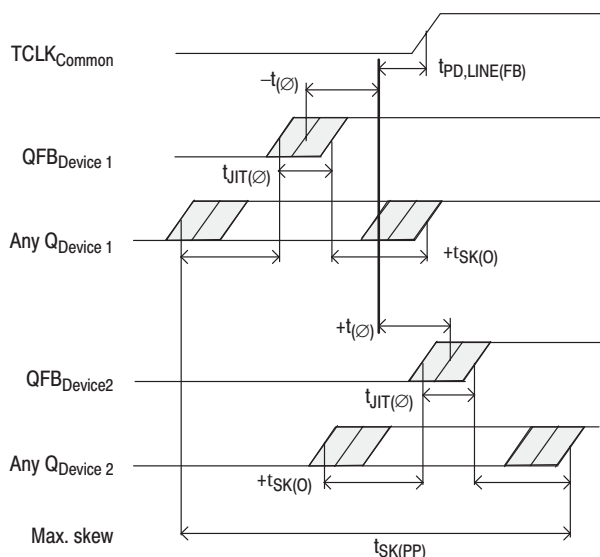


Figure 6. MPC9600 max. device-to-device skew

Due to the statistical nature of I/O jitter a RMS value (1σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

Table 8: Confidence Factor CF

CF	Probability of clock edge within the distribution
$\pm 1\sigma$	0.68268948
$\pm 2\sigma$	0.95449988
$\pm 3\sigma$	0.99730007
$\pm 4\sigma$	0.99993663
$\pm 5\sigma$	0.99999943
$\pm 6\sigma$	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% ($\pm 3\sigma$) is assumed, resulting in a worst case timing uncertainty from input to any output of -261 ps to 341 ps relative to CCLK ($V_{CC}=3.3V$ and $f_{VCO} = 200$ MHz):

$$t_{SK(PP)} = [-60ps...140ps] + [-150ps...150ps] + [(17ps \cdot -3)...(17ps \cdot 3)] + t_{PD, LINE(FB)}$$

$$t_{SK(PP)} = [-261ps...341ps] + t_{PD, LINE(FB)}$$

Above equation uses the maximum I/O jitter number shown in the AC characteristic table for $V_{CC}=3.3V$ (17 ps RMS). I/O jitter is frequency dependant with a maximum at the lowest VCO frequency (200 MHz for the MPC9600). Applications using a higher VCO frequency exhibit less I/O jitter than the AC characteristic limit. The I/O jitter characteristics in Figure 7 can be used to derive a smaller I/O jitter number at the specific VCO frequency, resulting in tighter timing limits in zero-delay mode and for part-to-part skew $t_{SK(PP)}$.

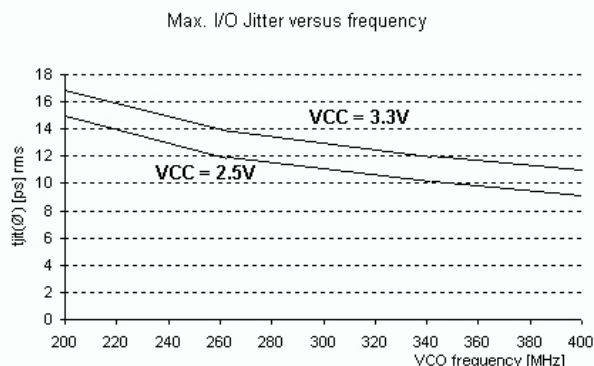


Figure 7. Max. I/O Jitter versus VCO frequency for $V_{CC}=2.5V$ and $V_{CC}=3.3V$

Driving Transmission Lines

The MPC9600 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}+2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output

of the MPC9600 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 8 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9600 clock driver is effectively doubled due to its capability to drive multiple lines.

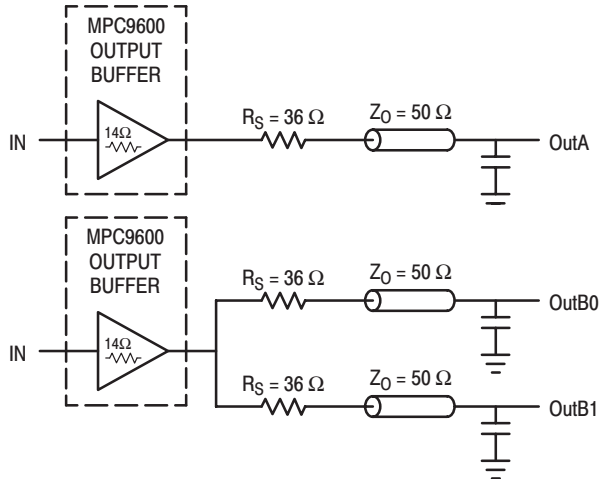


Figure 8. Single versus Dual Transmission Lines

The waveform plots in Figure 9 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9600 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9600. The output waveform in Figure 9 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$

$$Z_0 = 50 \Omega \parallel 50 \Omega$$

$$R_S = 36 \Omega \parallel 36 \Omega$$

$$R_0 = 14 \Omega$$

$$V_L = 3.0 (25 \div (18 + 17 + 25))$$

$$= 1.31 \text{ V}$$

At the load end the voltage will double due to the near unity reflection coefficient, to 2.6 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

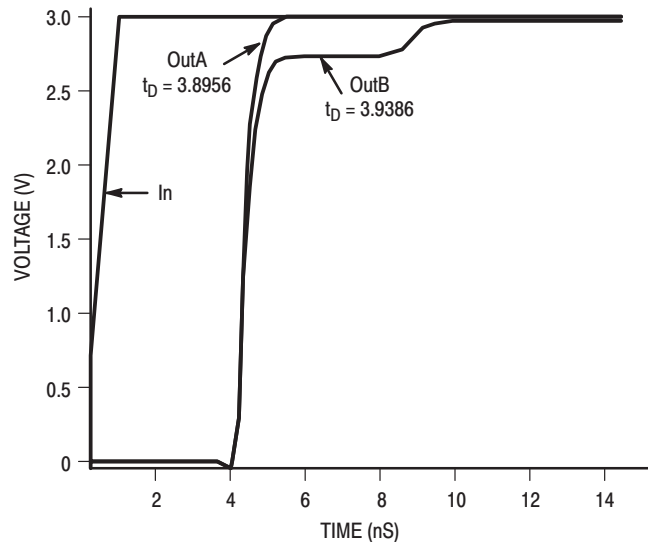


Figure 9. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 10 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

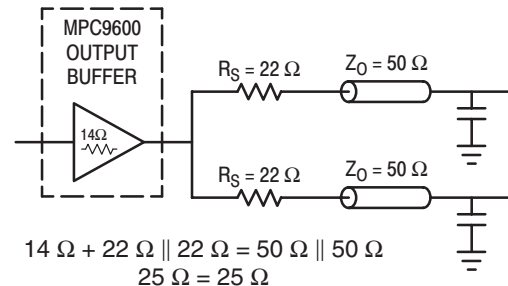


Figure 10. Optimized Dual Line Termination

The Following Figures Illustrate the Measurement Reference for the MPC9600 Clock Driver Circuit

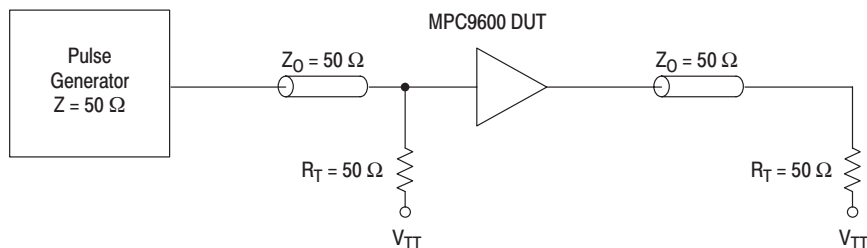


Figure 11. CCLK MPC9600 AC test reference

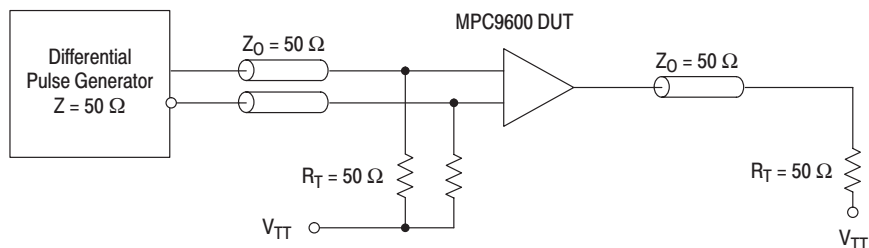


Figure 12. PCLK MPC9600 AC test reference

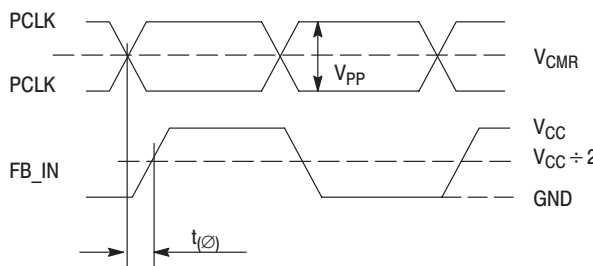


Figure 13. Propagation delay t_{ϕ} , static phase offset) test reference

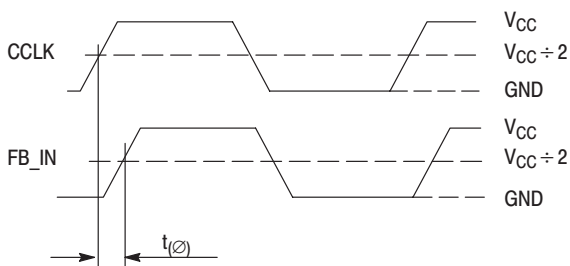
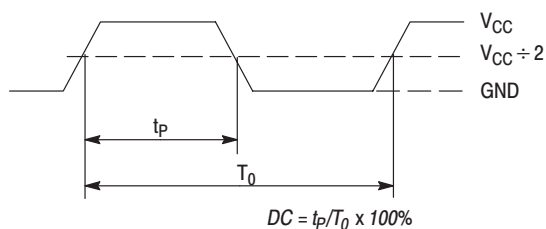
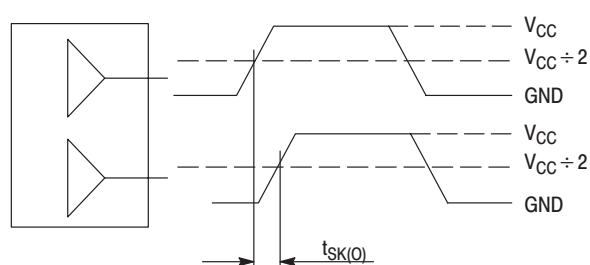


Figure 14. Propagation delay t_{ϕ} test reference



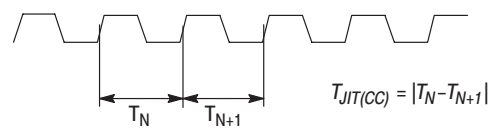
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 15. Output Duty Cycle (DC)



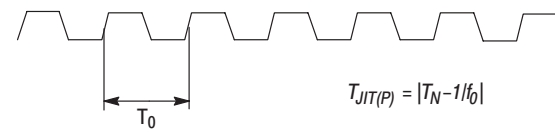
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 16. Output-to-output Skew $t_{SK(O)}$



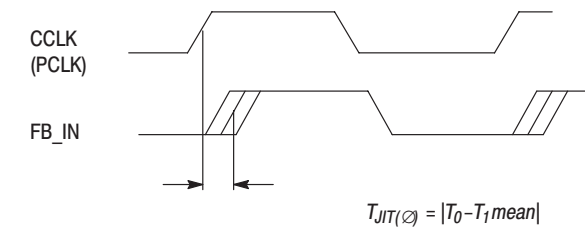
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 17. Cycle-to-cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 18. Period Jitter



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 19. I/O Jitter

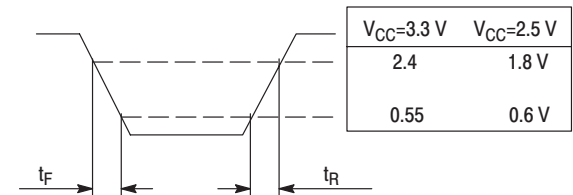


Figure 20. Output Transition Time Test Reference

2

Low Voltage PLL Clock Driver

The MPC972 is a 3.3 V compatible, PLL based clock driver device targeted for high performance CISC or RISC processor based systems. With output frequencies of up to 125 MHz and skews of 550 ps the MPC972 is ideally suited for most synchronous systems. The device offers twelve low skew outputs plus a feedback and sync output for added flexibility and ease of system implementation.

- Fully Integrated PLL
- Output Frequency up to 125 MHz
- Compatible with **PowerPC™** and Pentium™ Microprocessors
- LQFP Packaging
- 3.3 V V_{CC}
- ± 100 ps Typical Cycle-to-Cycle Jitter

The MPC972 features an extensive level of frequency programmability between the 12 outputs as well as the input vs output relationships. Using the select lines output frequency ratios of 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 5:1, 5:2, 5:3, 6:1 and 6:5 between outputs can be realized by pulsing low one clock edge prior to the coincident edges of the Qa and Qc outputs. The Sync output will indicate when the coincident rising edges of the above relationships will occur. The selectability of the feedback frequency is independent of the output frequencies, this allows for very flexible programming of the input reference vs output frequency relationship. The output frequencies can be either odd or even multiples of the input reference. In addition the output frequency can be less than the input frequency for applications where a frequency needs to be reduced by a non-binary factor. The Power-On Reset ensures proper programming if the frequency select pins are set at power up. If the fselFB2 pin is held high, it may be necessary to apply a reset after power-up to ensure synchronization between the QFB output and the other outputs. The internal power-on reset is designed to provide this function, but with power-up conditions being dependent, it is difficult to guarantee. All other conditions of the fsel pins will automatically synchronize during PLL lock acquisition.

The MPC972 offers a very flexible output enable/disable scheme. This enable/disable scheme helps facilitate system debug as well as provide unique opportunities for system power down schemes to meet the requirements of "green" class machines. The MPC972 allows for the enabling of each output independently via a serial input port. When disabled or "frozen" the outputs will be locked in the "LOW" state, however the internal state machines will continue to run. Therefore when "unfrozen" the outputs will activate synchronous and in phase with those outputs which were not frozen. The freezing and unfreezing of outputs occurs only when they are already in the "LOW" state, thus the possibility of runt pulse generation is eliminated. A power-on reset will ensure that upon power up all of the outputs will be active. Note that all of the control inputs on the MPC972 have internal pull-up resistors.

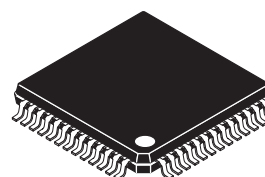
The MPC972 is fully 3.3 V compatible and requires no external loop filter components. All inputs accept LVCMOS/LVTTL compatible levels while the outputs provide LVCMOS levels with the capability to drive 50 Ω transmission lines. For series terminated lines each MPC972 output can drive two 50 Ω lines in parallel thus effectively doubling the fanout of the device.

The MPC972 can consume significant power in some configurations. Users are encouraged to review Application Note AN1545/D in the Advanced Clock Drivers Device Data book (DL207/D) for a discussion on the thermal issues with the MPC family of clock drivers.

MPC972

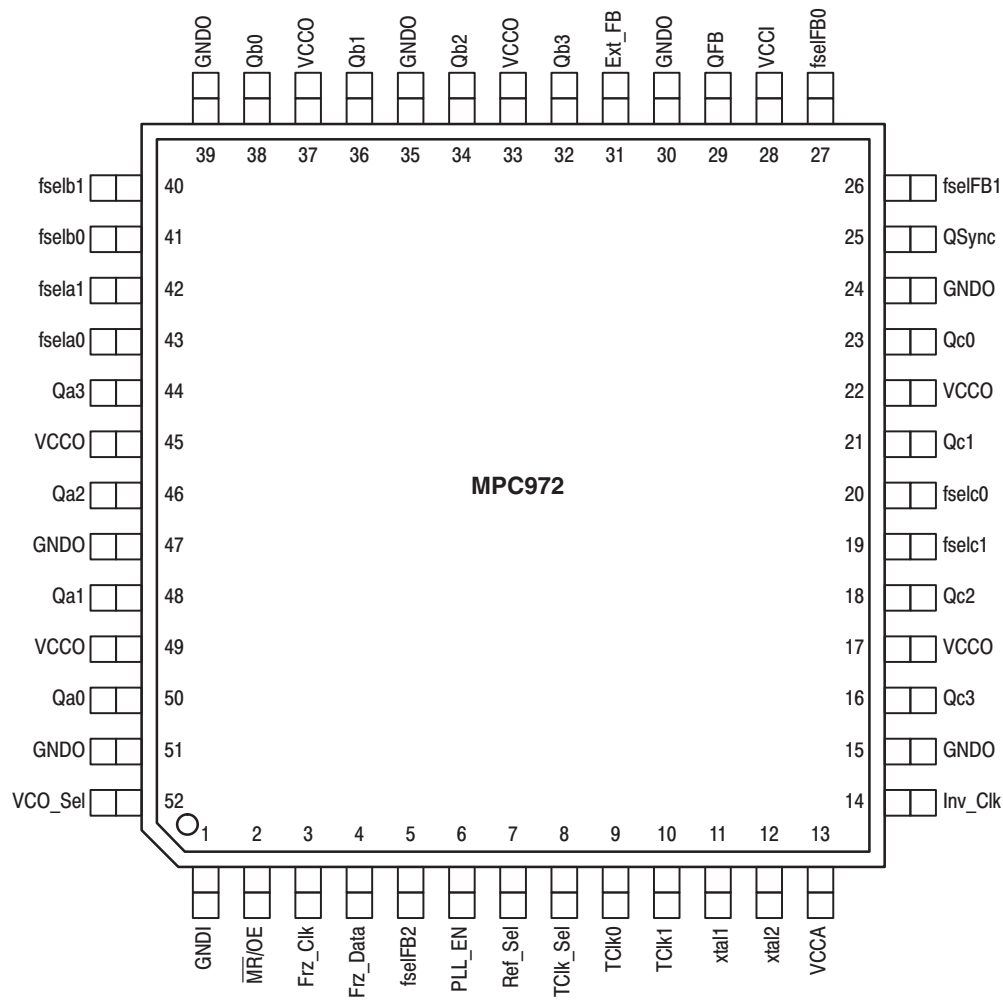
See Upgrade Product – MPC9772

LOW VOLTAGE PLL CLOCK DRIVER



SCALE 2:1

FA SUFFIX
52-LEAD LQFP PACKAGE
CASE 848D-03



All inputs have internal pull-up resistors (appr. 50 K) except for the xtal1 and xtal2 pins.

Figure 1. 52-Lead Pinout (Top View)

FUNCTION TABLE 1

fsela1	fsela0	Qa	fselb1	fselb0	Qb	fselc1	fselc0	Qc
0	0	÷4	0	0	÷4	0	0	÷2
0	1	÷6	0	1	÷6	0	1	÷4
1	0	÷8	1	0	÷8	1	0	÷6
1	1	÷12	1	1	÷10	1	1	÷8

FUNCTION TABLE 2

*fselFB2	fselFB1	fselFB0	QFB
0	0	0	÷4
0	0	1	÷6
0	1	0	÷8
0	1	1	÷10
1	0	0	÷8
1	0	1	÷12
1	1	0	÷16
1	1	1	÷20

*If the fselFB2 is 1, it may be necessary to apply a reset after power up to ensure synchronization between QFB and the other inputs.

FUNCTION TABLE 3

Control Pin	Logic '0'	Logic '1'
VCO_Sel	VCO/2	VCO
Ref_Sel	TCLK	Xtal (PECL)
TCLK_Sel	TCLK0	TCLK1
PLL_En	Bypass PLL	Enable PLL
MR/OE	Master Reset/Output Hi-Z	Enable Outputs
Inv_Clk	Non-Inverted Qc2, Qc3	Inverted Qc2, Qc3

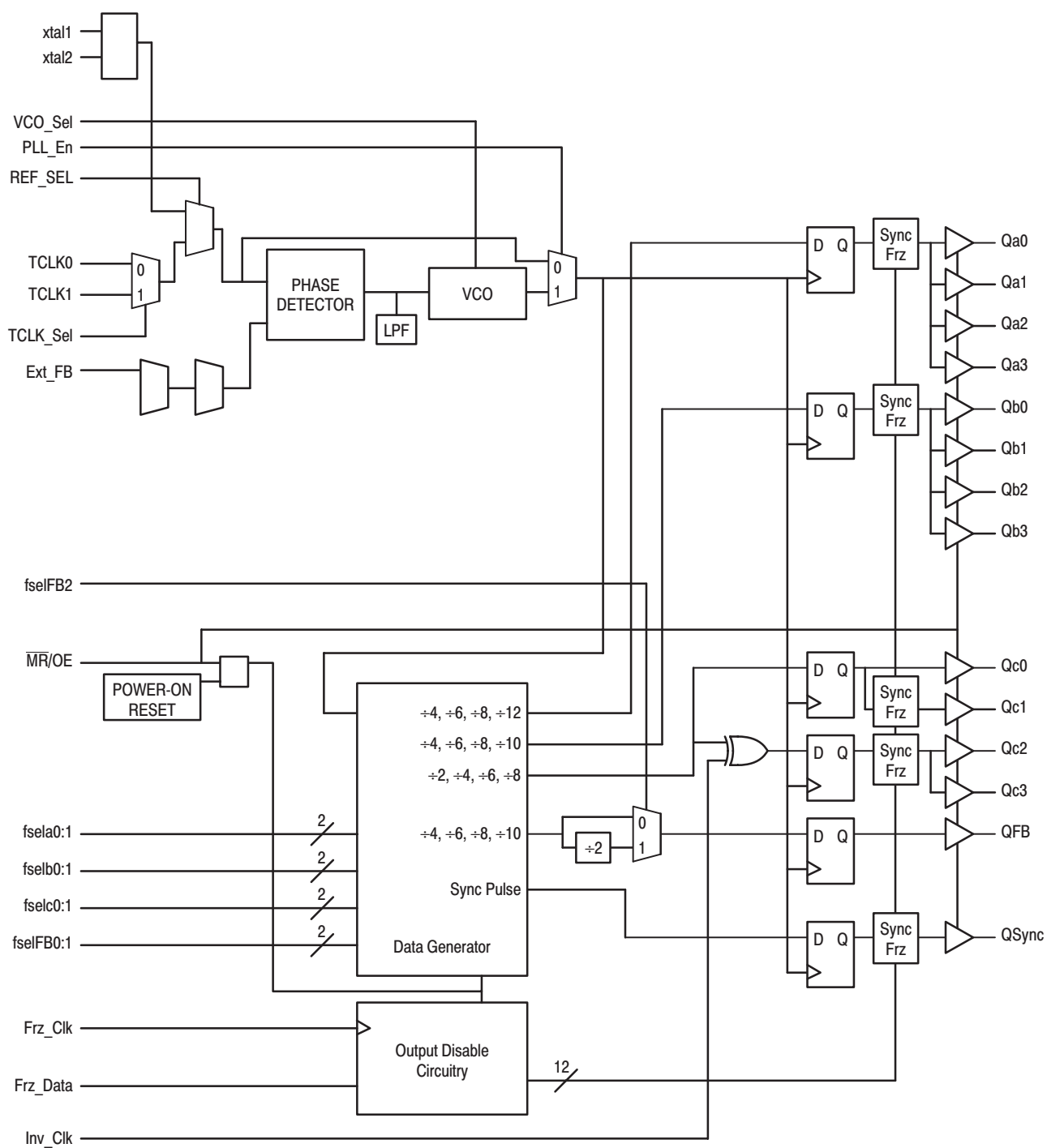


Figure 2. Logic Diagram

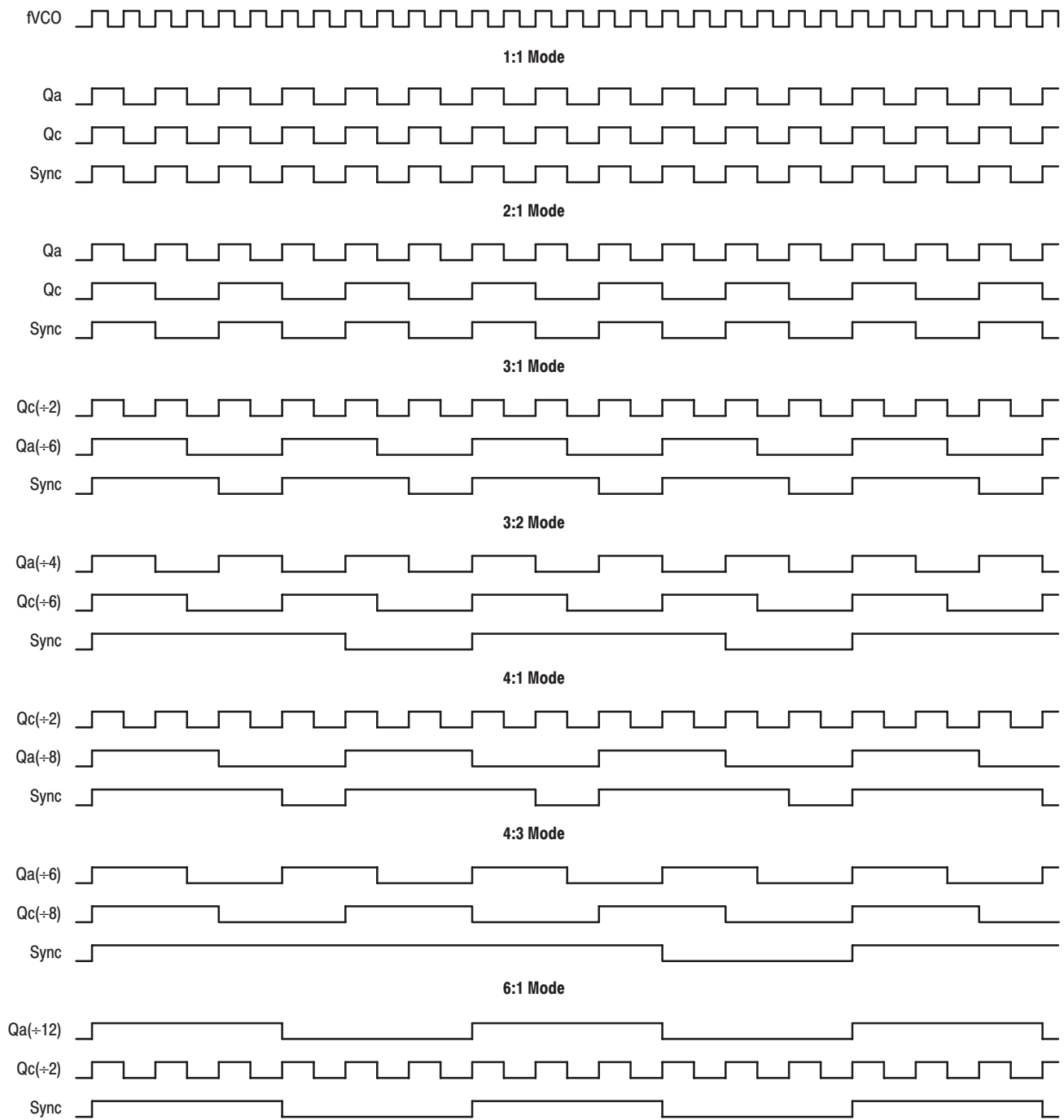


Figure 3. Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	4.6	V
V_I	Input Voltage	-0.3	$V_{CC} + 0.3$	V
I_{IN}	Input Current		± 20	mA
T_{Stor}	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

THERMAL CHARACTERISTICS

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to long-term reliability is addressed in the Motorola application note AN1545.

DC CHARACTERISTICS (Note 3.; $T_A = 0^\circ$ to 70°C ; $V_{CC} = 3.3\text{ V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{CCA}	Analog V_{CC} Voltage	2.935		V_{CC}	V	
V_{IH}	Input HIGH Voltage	2.0		3.6	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -20\text{ mA}$ (Note 1.)
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 20\text{ mA}$ (Note 1.)
I_{IN}	Input Current			± 120	μA	Note 2.
I_{CC}	Maximum Quiescent Supply Current		190	215	mA	All VCC Pins
I_{CCA}	Analog V_{CC} Current		15	20	mA	
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	Per Output

1. The MPC972 outputs can drive series or parallel terminated $50\ \Omega$ (or $50\ \Omega$ to $V_{CC}/2$) transmission lines on the incident edge (see Applications Info section).
2. Inputs have pull-up/pull-down resistors which affect input current.
3. Special thermal handling may be required in some configurations.

PLL INPUT REFERENCE CHARACTERISTICS ($T_A = 0^\circ$ to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	Note 1.	100 Note 1.	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	
t_{xtal}	Crystal Oscillator Frequency	10	25	MHz	Note 2.

1. Maximum input reference frequency is limited by the VCO lock range and the feedback divider or 100MHz, minimum input reference frequency is limited by the VCO lock range and the feedback divider.
2. See Applications Info section for more crystal information.

AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C ; $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time	0.15		1.2	ns	0.8 to 2.0V, Note 1.
t_{pw}	Output Duty Cycle	$t_{CYCLE}/2$ -750	$t_{CYCLE}/2$ ± 500	$t_{CYCLE}/2$ +750	ps	Note 1.
t_{pd}	SYNC to Feedback Propagation Delay	TCLK0 -270 TCLK1 -330	130 70	530 470	ps	Notes 1., 2.; QFB = ± 8
t_{os}	Output-to-Output Skew			550	ps	Note 1.
f_{VCO}	VCO Lock Range	200		480	MHz	
f_{max}	Maximum Output Frequency	Q (± 2) Q (± 4) Q (± 6) Q (± 8)		125 120 80 60	MHz	Note 1.
t_{jitter}	Cycle-to-Cycle Jitter (Peak-to-Peak)		± 100		ps	Note 1.
t_{PLZ}, t_{PHZ}	Output Disable Time	2		8	ns	Note 1.
t_{PZL}, t_{PZH}	Output ENable Time	2		10	ns	Note 1.
t_{lock}	Maximum PLL Lock Time			10	ms	
f_{MAX}	Maximum Frz_Clk Frequency			20	MHz	

1. 50Ω transmission line terminated into $V_{CC}/2$.

2. t_{pd} is specified for a 50MHz input reference. The window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The t_{pd} does not include jitter.

APPLICATIONS INFORMATION**Programming the MPC972**

The MPC972 is one of the most flexible frequency programming devices in the Motorola timing solution portfolio. With three independent banks of four outputs as well as an independent PLL feedback output the total number of possible configurations is too numerous to tabulate. Table 1 tabulates the various selection possibilities for the three banks of outputs. The divide numbers presented in the table represent the divider applied to the output of the VCO for that bank of outputs. To determine the relationship between the three banks the three divide ratios would be compared. For instance if a frequency relationship of 5:3:2 was desired the following selection could be made. The Qb outputs could be set to ± 10 , the Qa outputs to ± 6 and the Qc outputs to ± 4 . With this output divide selection the desired 5:3:2 relationship would be generated. For situations where the VCO will run at relatively low frequencies the PLL may not be stable for the desired divide ratios. For these circumstances the VCO_Sel pin allows for an extra ± 2 to be added into the clock path. When asserted this pin will maintain the desired output relationships, but will provide an enhanced lock range for the PLL. Once the output frequency relationship is set and the VCO is in its stable range the feedback output would be programmed to match the input reference frequency.

The MPC972 offers only an external feedback to the PLL. A separate feedback output is provided to optimize the flexibility of the device. If in the example above the input reference

frequency was equal to the lowest output frequency the feedback output would be set in the ± 10 mode. If the input needed to be half the lowest frequency output the fselFB2 input could be asserted to halve the feedback frequency. This action multiplies the output frequencies by two relative to the input reference frequency. With 7 unique feedback divide capabilities there is a tremendous amount of flexibility. Again assume the above 5:3:2 relationship is needed with the highest frequency output equal to 100 MHz. If one was also constrained because the only reference frequency available was 50 MHz the setup in Figure 6 could be used. The MPC972 provides the 100, 66 and 40 MHz outputs all synthesized from the 50 MHz source. With its multitude of divide ratio capabilities the MPC972 can generate almost any frequency from a standard, common frequency already present in a design. Figure 7 and Figure 8 illustrate a few more examples of possible MPC972 configurations.

The MPC972 has one more programming feature added to its arsenal. The Inv_Clk input pin when asserted will invert the Qc2 and Qc3 outputs. This inversion will not affect the output-to-output skew of the device. This inversion allows for the development of 180° phase shifted clocks. This output could also be used as a feedback output to the MPC972 or a second PLL device to generate early or late clocks for a specific design. Figure 9 illustrates the use of two MPC972's to generate two banks of clocks with one bank divided by 2 and delayed by 180° relative to the first.

2 SYNC Output Description

In situations where output frequency relationships are not integer multiples of each other there is a need for a signal for system synchronization purposes. The SYNC output of the MPC972 is designed to specifically address this need. The MPC972 monitors the relationship between the Qa and the Qc banks of outputs. It provides a low going pulse, one period in duration, one period prior to the coincident rising edges of the

Qa and Qc outputs. The duration and the placement of the pulse is dependent on the higher of the Qa and Qc output frequencies. The timing diagrams in the data sheet show the various waveforms for the SYNC output. Note that the SYNC output is defined for all possible combinations of the Qa and Qc outputs even though under some relationships the lower frequency clock could be used as a synchronizing signal.

Table 1. Programmable Output Frequency Relationships (VCO_Sel = '1')

fselc1	fselc0	Qa	fselb1	fselb0	Qb	fselc1	fselc0	Qc
0	0	VCO/4	0	0	VCO/4	0	0	VCO/2
0	1	VCO/6	0	1	VCO/6	0	1	VCO/4
1	0	VCO/8	1	0	VCO/8	1	0	VCO/6
1	1	VCO/12	1	1	VCO/10	1	1	VCO/8

Table 2. Programmable Output Frequency Relationships (VCO_Sel = '1')

fselFB2	fselFB1	fselFB0	QFB
0	0	0	VCO/4
0	0	1	VCO/6
0	1	0	VCO/8
0	1	1	VCO/10
1	0	0	VCO/8
1	0	1	VCO/12
1	1	0	VCO/16
1	1	1	VCO/20

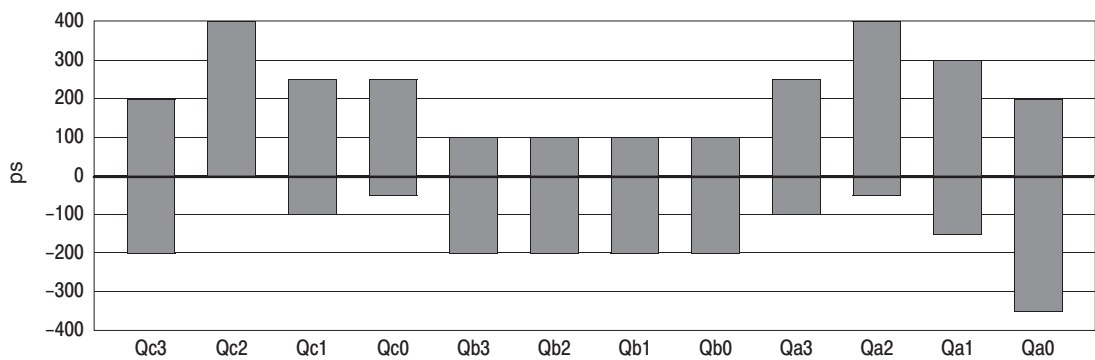


Figure 4. Typical Skews Relative to QFB

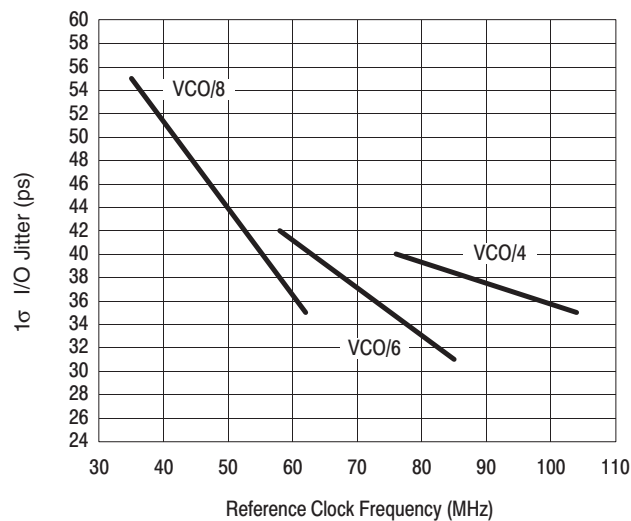


Figure 5. Typical Phase Jitter versus Reference Frequency
I/O Jitter

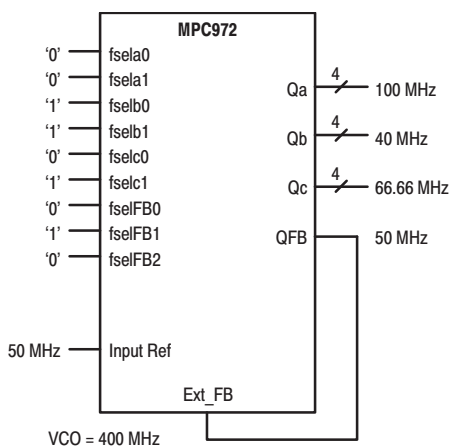


Figure 6. Programming Configuration Example

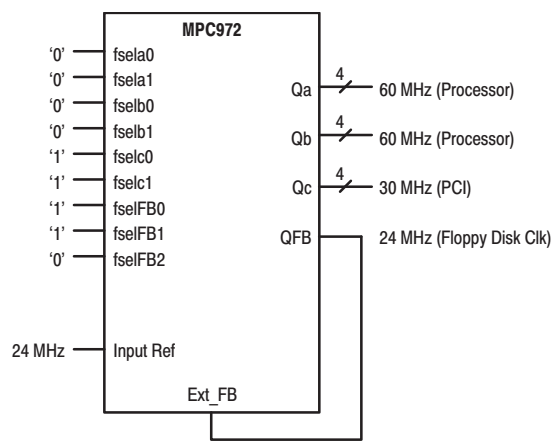


Figure 7. Generating Pentium Clocks from Floppy Clock

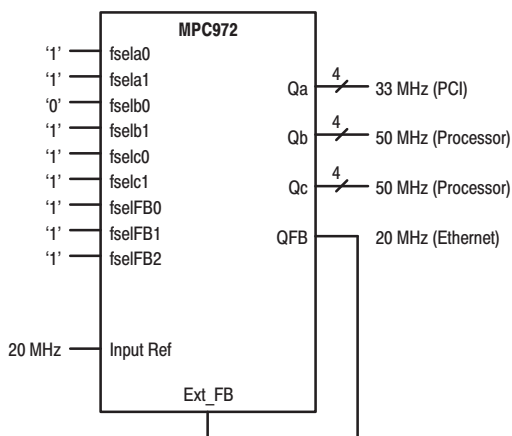


Figure 8. Generating MPC604 Clocks from Ethernet Clocks

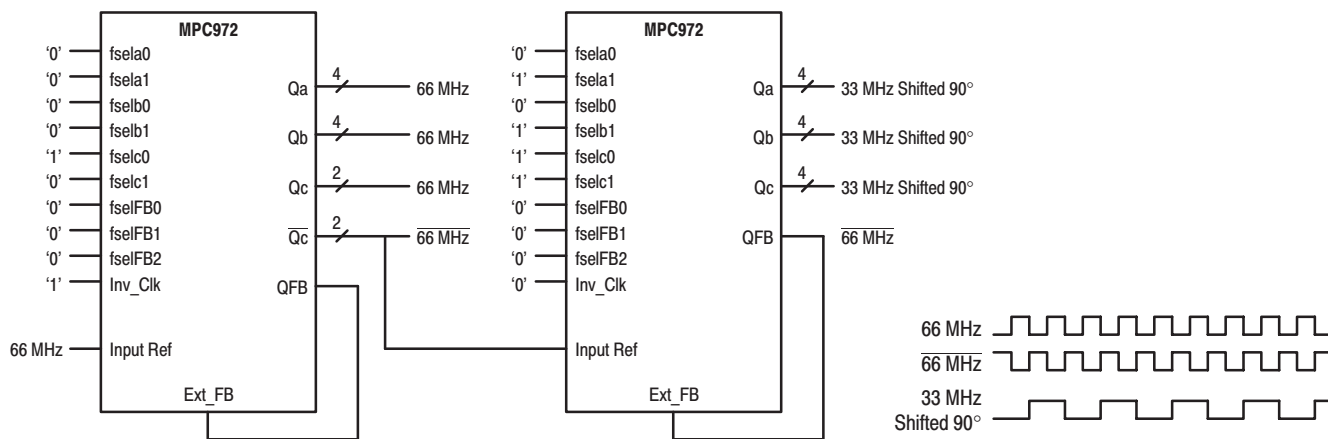


Figure 9. Phase Delay Using Multiple MPC972's

Using the On-Board Crystal Oscillator

The MPC972 features an on-board crystal oscillator to allow for seed clock generation as well as final distribution. The on-board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC972 as possible to avoid any board level parasitics. To facilitate co-location surface mount crystals are recommended, but not required.

The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on-board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most of the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC972 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

3. Crystal Recommendations

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	± 75 ppm at 25°C
Frequency/Temperature Stability	± 150 pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7 pF
Equivalent Series Resistance (ESR)	50 to 80 Ω Max
Correlation Drive Level	100 μ W
Aging	5 ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

The MPC972 is a clock driver which was designed to generate outputs with programmable frequency relationships and not a synthesizer with a fixed input frequency. As a result the crystal input frequency is a function of the desired output frequency. For a design which utilizes the external feedback to the PLL the selection of the crystal frequency is straight forward; simply chose a crystal which is equal in frequency to the feedback signal.

Recommended External Reset Timing

For MPC972 applications requiring synchronization of the output clock to the input clock and if $\text{fselfB2} = 1$, the assertion of $\overline{\text{MR}}$ is recommended. The timing of asserting $\overline{\text{MR}}$ should be as shown in Figure 10. The power supply should be at or above the minimum specified voltage and the reference clock input (refclk) should be present a minimum of t_1 prior to the reset pulse being applied to the $\overline{\text{MR}}$ pin.

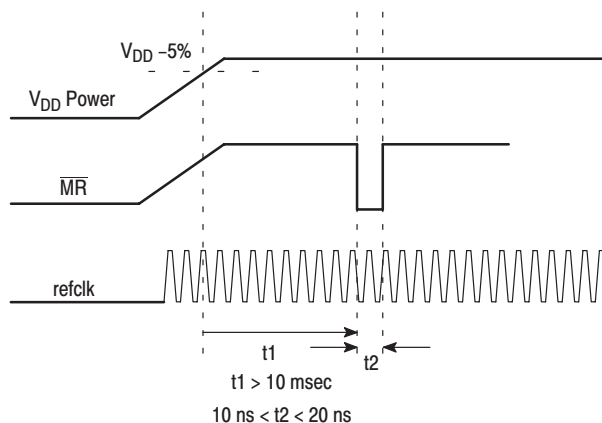


Figure 10. Assertion of $\overline{\text{MR}}$

Power Supply Filtering

The MPC972 is a mixed analog/digital product and exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC972 provides separate power supplies for the output buffers (V_{CCO}) and the internal PLL (V_{CCA}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC972.

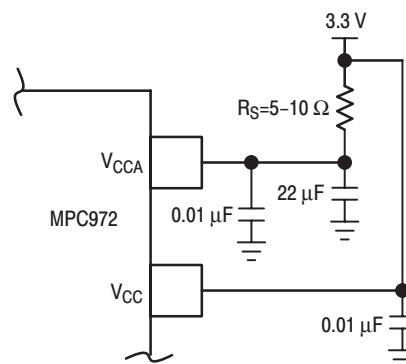


Figure 11. Power Supply Filter

Figure 11 illustrates a typical power supply filter scheme. The MPC972 is most susceptible to noise with spectral content in the 1 KHz to 1 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the

MPC972. From the data sheet the $I_{V_{CCA}}$ current (the current sourced through the V_{CCA} pin) is typically 15 mA (20 mA maximum), assuming that a minimum of 2.935 V must be maintained on the V_{CCA} pin very little DC voltage drop can be tolerated when a 3.3 V V_{CC} supply is used. The resistor shown in Figure 11 must have a resistance of 5–10 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC972 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC972 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC972 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 12 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC972 clock driver is effectively doubled due to its capability to drive multiple lines.

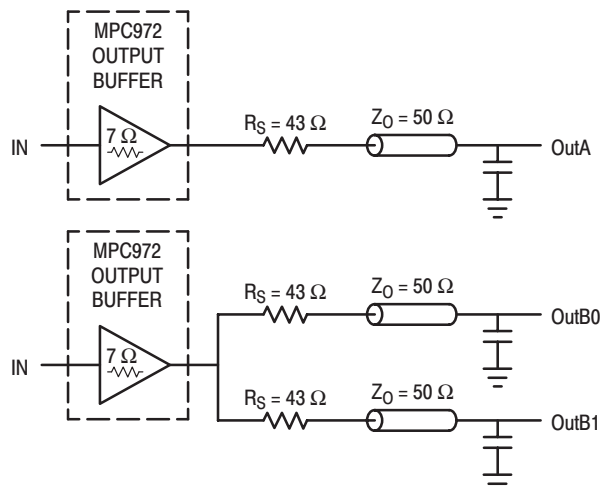


Figure 12. Single versus Dual Transmission Lines

The waveform plots of Figure 13 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC972 output buffers is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC972. The output waveform in Figure 13 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 / R_s + R_o + Z_0) = 3.0 (25/53.5) = 1.40 \text{ V}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 14 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

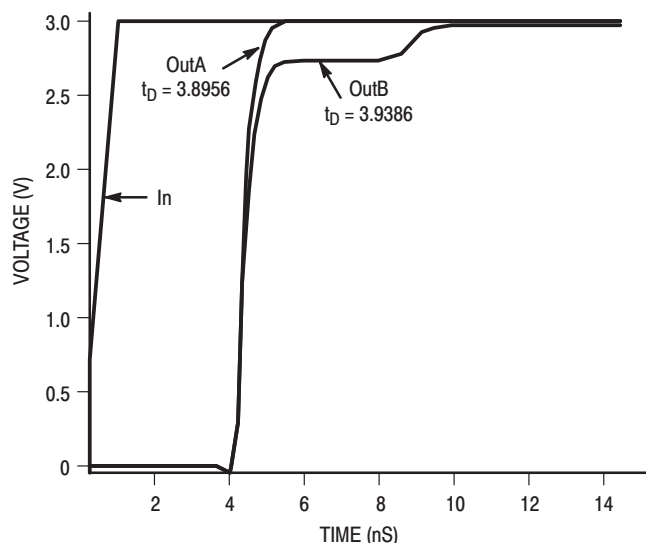


Figure 13. Single versus Dual Waveforms

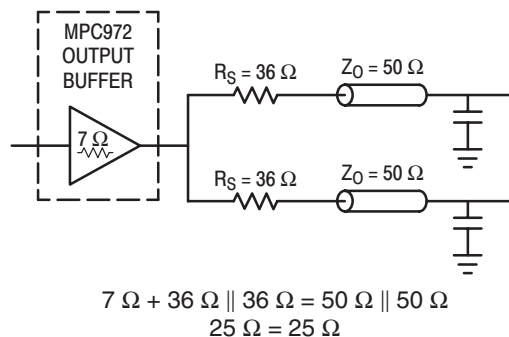


Figure 14. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Using the Output Freeze Circuitry

With the recent advent of a “green” classification for computers the desire for unique power management among system designers is keen. The individual output enable control

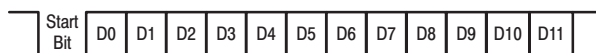
of the MPC972 allows designers, under software control, to implement unique power management schemes into their designs. Although useful, individual output control at the expense of one pin per output is too high, therefore a simple serial interface was derived to economize on the control pins.

The freeze control logic provides a mechanism through which the MPC972 clock outputs may be frozen (stopped in the logic ‘0’ state):

The freeze mechanism allows serial loading of the 12-bit Serial Input Register, this register contains one programmable freeze enable bit for 12 of the 14 output clocks. The Qc0 and QFB outputs cannot be frozen with the serial port, this avoids any potential lock up situation should an error occur in the loading of the Serial Input Register. The user may program an output clock to freeze by writing logic ‘0’ to the respective freeze enable bit. Likewise, the user may programmably unfreeze an output clock by writing logic ‘1’ to the respective enable bit.

The freeze logic will never force a newly-frozen clock to a logic ‘0’ state before the time at which it would normally transition there. The logic simply keeps the frozen clock at logic ‘0’ once it is there. Likewise, the freeze logic will never force a newly-unfrozen clock to a logic ‘1’ state before the time at which it would normally transition there. The logic re-enables the unfrozen clock during the time when the respective clock would normally be in a logic ‘0’ state, eliminating the possibility of ‘runt’ clock pulses.

The user may write to the Serial Input register through the Frz_Data input by supplying a logic ‘0’ start bit followed serially by 12 NRZ freeze enable bits. The period of each Frz_Data bit equals the period of the free-running Frz_Clk signal. The Frz_Data serial transmission should be timed so the MPC972 can sample each Frz_Data bit with the rising edge of the free-running Frz_Clk signal.



D0–D3 are the control bits for Qa0–Qa3, respectively

D4–D7 are the control bits for Qb0–Qb3, respectively

D8–D10 are the control bits for Qc1–Qc3, respectively

D11 is the control bit for QSync

Figure 15. Freeze Data Input Protocol

Low Voltage PLL Clock Driver

2

The MPC973 is a 3.3 V compatible, PLL based clock driver device targeted for high performance CISC or RISC processor based systems. With output frequencies of up to 125 MHz and skews of 550 ps the MPC973 is ideally suited for most synchronous systems. The device offer twelve low skew outputs plus a feedback and sync output for added flexibility and ease of system implementation.

- Fully Integrated PLL
- Output Frequency up to 125 MHz
- Compatible with **PowerPC™** and **Pentium™** Microprocessors
- LQFP Packaging
- 3.3 V V_{CC}
- ± 100 ps Typical Cycle-to-Cycle Jitter

The MPC973 features an extensive level of frequency programmability between the 12 outputs as well as the input vs output relationships. Using the select lines output frequency ratios of 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 5:1, 5:2, 5:3, 6:1 and 6:5 between outputs can be realized by pulsing low one clock edge prior to the coincident edges of the Qa and Qc outputs. The Sync output will indicate when the coincident rising edges of the above relationships will occur. The selectability of the feedback frequency is independent of the output frequencies, this allows for very flexible programming of the input reference vs output frequency relationship. The output frequencies can be either odd or even multiples of the input reference. In addition the output frequency can be less than the input frequency for applications where a frequency needs to be reduced by a non-binary factor. The Power-On Reset ensures proper programming if the frequency select pins are set at power up. If the fselFB2 pin is held high, it may be necessary to apply a reset after power-up to ensure synchronization between the QFB output and the other outputs. The internal power-on reset is designed to provide this function, but with power-up conditions being dependent, it is difficult to guarantee. All other conditions of the fsel pins will automatically synchronize during PLL lock acquisition.

The MPC973 offers a very flexible output enable/disable scheme. This enable/disable scheme helps facilitate system debug as well as provide unique opportunities for system power down schemes to meet the requirements of "green" class machines. The MPC973 allows for the enabling of each output independently via a serial input port. When disabled or "frozen" the outputs will be locked in the "LOW" state, however the internal state machines will continue to run. Therefore when "unfrozen" the outputs will activate synchronous and in phase with those outputs which were not frozen. The freezing and unfreezing of outputs occurs only when they are already in the "LOW" state, thus the possibility of runt pulse generation is eliminated. A power-on reset will ensure that upon power up all of the outputs will be active. Note that all of the control inputs on the MPC973 have internal pull-up resistors.

The MPC973 is fully 3.3 V compatible and requires no external loop filter components. All inputs accept LVCMOS/LVTTL compatible levels while the outputs provide LVCMOS levels with the capability to drive 50 Ω transmission lines. For series terminated lines each MPC973 output can drive two 50 Ω lines in parallel thus effectively doubling the fanout of the device.

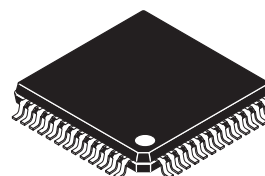
The MPC973 can consume significant power in some configurations. Users are encouraged to review Application Note AN1545/D in the Advanced Clock Drivers Device Data book (DL207/D) for a discussion on the thermal issues with the MPC family of clock drivers.

Rev 2

MPC973

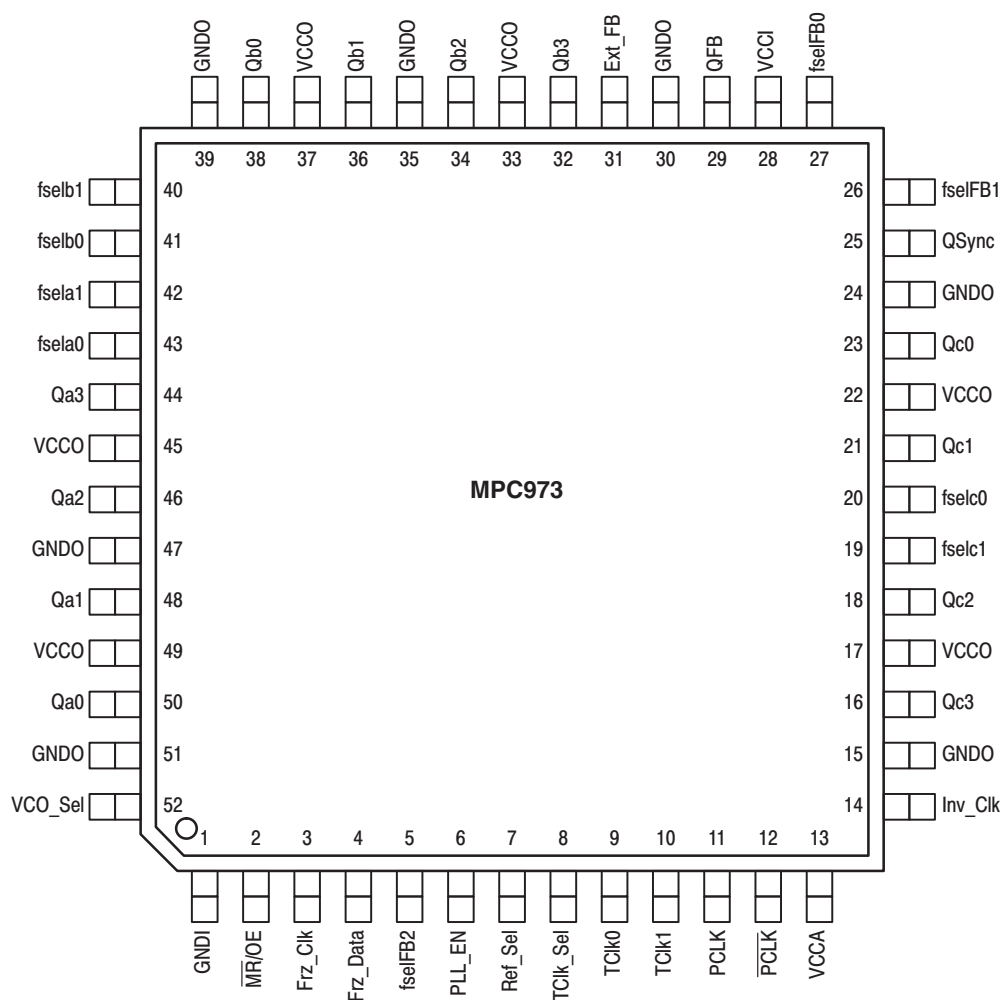
See Upgrade Product – MPC9773

**LOW VOLTAGE
PLL CLOCK DRIVER**



SCALE 2:1

FA SUFFIX
52-LEAD LQFP PACKAGE
CASE 848D-03



All inputs have internal pull-up resistors (appr. 50 K) except for the xtal1 and xtal2 pins.

Figure 1. 52-Lead Pinout (Top View)

FUNCTION TABLE 1

fsela1	fsela0	Qa	fselb1	fselb0	Qb	fselc1	fselc0	Qc
0	0	÷4	0	0	÷4	0	0	÷2
0	1	÷6	0	1	÷6	0	1	÷4
1	0	÷8	1	0	÷8	1	0	÷6
1	1	÷12	1	1	÷10	1	1	÷8

FUNCTION TABLE 2

*fselFB2	fselFB1	fselFB0	QFB
0	0	0	÷4
0	0	1	÷6
0	1	0	÷8
0	1	1	÷10
1	0	0	÷8
1	0	1	÷12
1	1	0	÷16
1	1	1	÷20

* If the fselFB2 is 1, it may be necessary to apply a reset after power up to ensure synchronization between QFB and the other inputs.

FUNCTION TABLE 3

Control Pin	Logic '0'	Logic '1'
VCO_Sel	VCO/2	VCO
Ref_Sel	TCLK	Xtal (PECL)
TCLK_Sel	TCLK0	TCLK1
PLL_En	Bypass PLL	Enable PLL
MR/OE	Master Reset/Output Hi-Z	Enable Outputs
Inv_Clk	Non-Inverted Qc2, Qc3	Inverted Qc2, Qc3

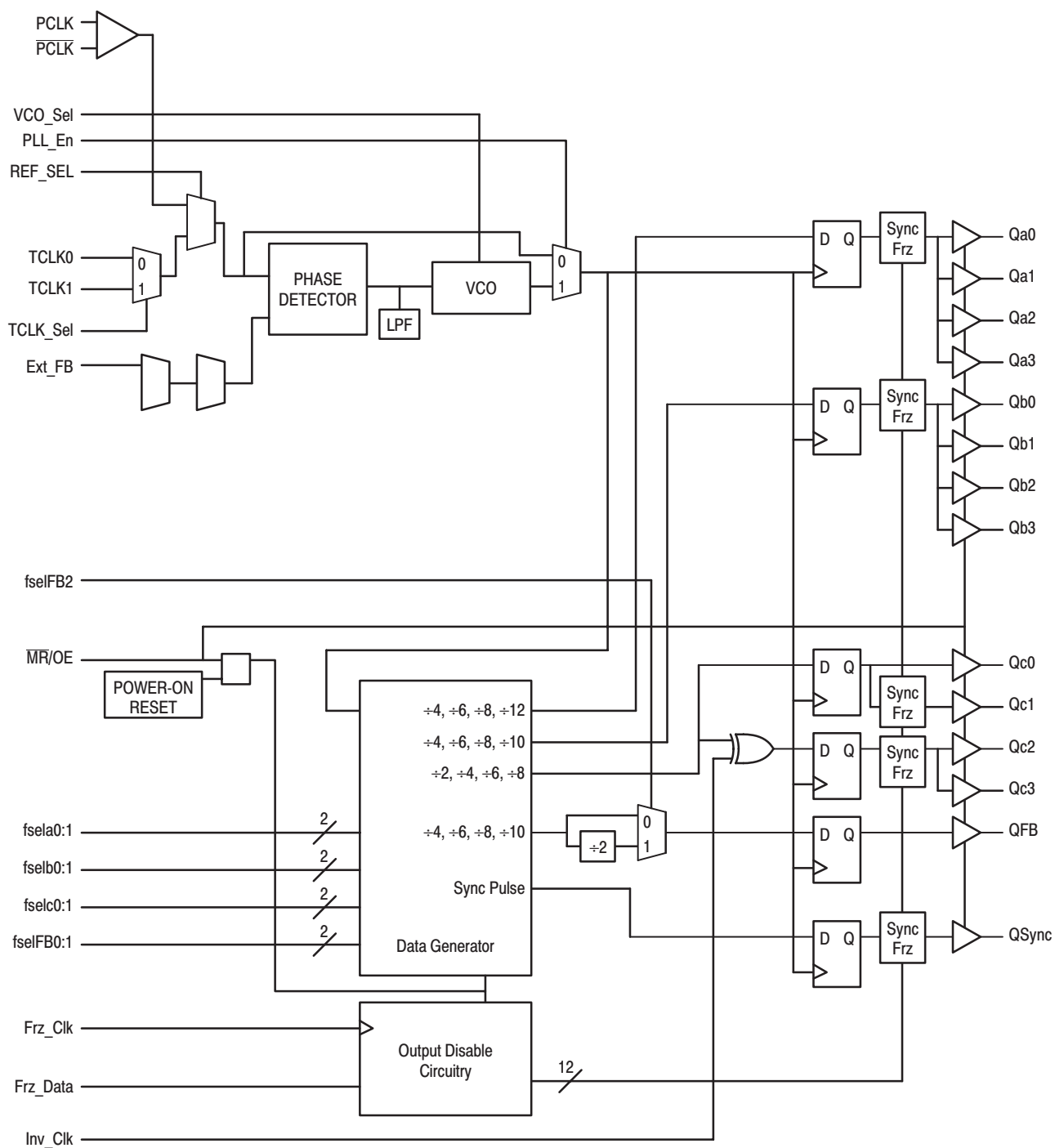


Figure 2. Logic Diagram

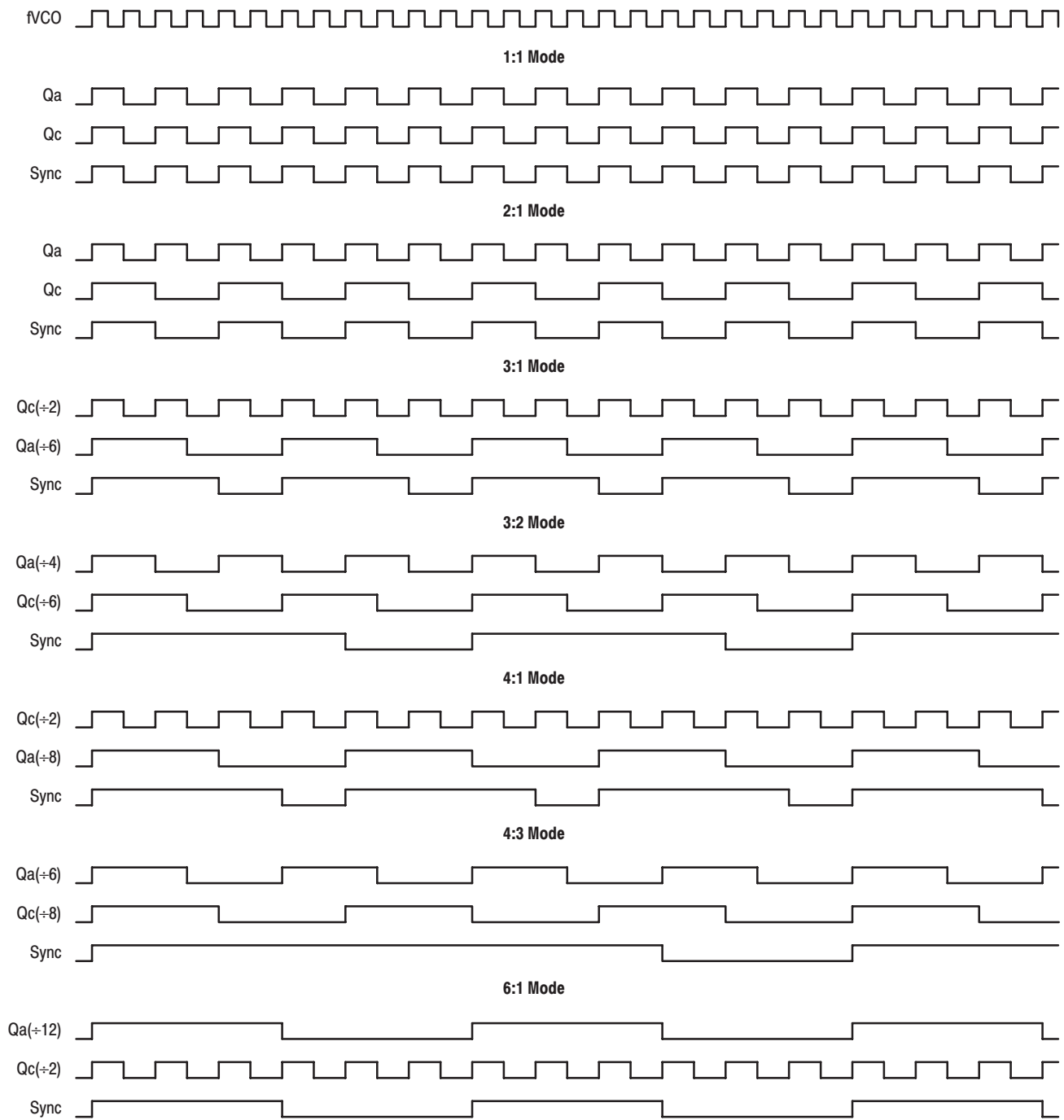


Figure 3. Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	4.6	V
V_I	Input Voltage	-0.3	$V_{CC} + 0.3$	V
I_{IN}	Input Current		± 20	mA
T_{Stor}	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

THERMAL CHARACTERISTICS

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

DC CHARACTERISTICS (Note 4.; $T_A = 0^\circ$ to 70°C ; $V_{CC} = 3.3\text{ V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{CCA}	Analog V_{CC} Voltage	2.935		V_{CC}	V	
V_{IH}	Input HIGH Voltage	2.0		3.6	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{PP}	Peak-to-Peak Input Voltage	PCLK 300		1000	mV	
V_{CMR}	Common Mode Range	PCLK $V_{CC}-2.0$		$V_{CC}-0.6$		Note 1.
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -20\text{ mA}$ (Note 2.)
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 20\text{ mA}$ (Note 2.)
I_{IN}	Input Current			± 120	μA	Note 3.
I_{CC}	Maximum Quiescent Supply Current		190	215	mA	All VCC Pins
I_{CCA}	Analog V_{CC} Current		15	20	mA	
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	Per Output

1. V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "High" input is within the V_{CMR} range and the input lies within the V_{PP} specification.
2. The MPC973 outputs can drive series or parallel terminated $50\ \Omega$ (or $50\ \Omega$ to $V_{CC}/2$) transmission lines on the incident edge (see Applications Info section).
3. Inputs have pull-up/pull-down resistors which affect input current.
4. Special thermal handling may be required in some configurations.

PLL INPUT REFERENCE CHARACTERISTICS ($T_A = 0^\circ$ to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	Note 5.	100 Note 5.	MHz	Note 5.
f_{refDC}	Reference Input Duty Cycle	25	75	%	

5. Maximum input reference frequency is limited by the VCO lock range and the feedback divider or 100MHz, minimum input reference frequency is limited by the VCO lock range and the feedback divider.

AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C ; $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time	0.15		1.2	ns	0.8 to 2.0V, Note 6.
t_{pw}	Output Duty Cycle	$t_{CYCLE}/2$ -750	$t_{CYCLE}/2$ ± 500	$t_{CYCLE}/2$ +750	ps	Note 6.
t_{pd}	SYNC to Feedback Propagation Delay	TCLK0 -70 TCLK1 -130 PCLK -225	130 70 -25	330 270 175	ps	Notes 6., 7.; QFB = $\div 8$
t_{os}	Output-to-Output Skew			550	ps	Note 6.
f_{VCO}	VCO Lock Range	200		480	MHz	
f_{max}	Maximum Output Frequency	Q ($\div 2$) Q ($\div 4$) Q ($\div 6$) Q ($\div 8$)		125 120 80 60	MHz	Note 6.
t_{jitter}	Cycle-to-Cycle Jitter (Peak-to-Peak)		± 100		ps	Note 6.
t_{PLZ}, t_{PHZ}	Output Disable Time	2		8	ns	Note 6.
t_{PZL}, t_{PZH}	Output ENable Time	2		10	ns	Note 6.
t_{lock}	Maximum PLL Lock Time			10	ms	
f_{MAX}	Maximum Frz_Clk Frequency			20	MHz	

6. 50Ω transmission line terminated into $V_{CC}/2$.

7. t_{pd} is specified for a 50MHz input reference. The window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The t_{pd} does not include jitter.

APPLICATIONS INFORMATION**Programming the MPC973**

The MPC973 is the most flexible frequency programming device in the Motorola timing solution portfolio. With three independent banks of four outputs as well as an independent PLL feedback output the total number of possible configurations is too numerous to tabulate. Table 1 tabulates the various selection possibilities for the three banks of outputs. The divide numbers presented in the table represent the divider applied to the output of the VCO for that bank of outputs. To determine the relationship between the three banks the three divide ratios would be compared. For instance if a frequency relationship of 5:3:2 was desired the following selection could be made. The Qb outputs could be set to $\div 10$, the Qa outputs to $\div 6$ and the Qc outputs to $\div 4$. With this output divide selection the desired 5:3:2 relationship would be generated. For situations where the VCO will run at relatively low frequencies the PLL may not be stable for the desired divide ratios. For these circumstances the VCO_Sel pin allows for an extra $\div 2$ to be added into the clock path. When asserted this pin will maintain the desired output relationships, but will provide an enhanced lock range for the PLL. Once the output frequency relationship is set and the VCO is in its stable range the feedback output would be programmed to match the input reference frequency.

The MPC973 offers only an external feedback to the PLL. A separate feedback output is provided to optimize the flexibility of the device. If in the example above the input reference

frequency was equal to the lowest output frequency the feedback output would be set in the $\div 10$ mode. If the input needed to be half the lowest frequency output the fselfB2 input could be asserted to halve the feedback frequency. This action multiplies the output frequencies by two relative to the input reference frequency. With 7 unique feedback divide capabilities there is a tremendous amount of flexibility. Again assume the above 5:3:2 relationship is needed with the highest frequency output equal to 100 MHz. If one was also constrained because the only reference frequency available was 50MHz the setup in figure 8 could be used. The MPC973 provides the 100, 66 and 40MHz outputs all synthesized from the 50 MHz source. With its multitude of divide ratio capabilities the MPC973 can generate almost any frequency from a standard, common frequency already present in a design. Figures 9 and 10 illustrate a few more examples of possible MPC973 configurations.

The MPC973 has one more programming feature added to its arsenal. The Inv_Clk input pin when asserted will invert the Qc2 and Qc3 outputs. This inversion will not affect the output-to-output skew of the device. This inversion allows for the development of 180° phase shifted clocks. This output could also be used as a feedback output to the MPC973 or a second PLL device to generate early or late clocks for a specific design. Figure 11 illustrates the use of two MPC973's to generate two banks of clocks with one bank divided by 2 and delayed by 180° relative to the first.

Using the MPC973 as a Zero Delay Buffer

The external feedback of the MPC973 clock driver allows for its use as a zero delay buffer. By using one of the outputs as a feedback to the PLL the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs. Because the static phase offset is a function of the reference clock the Tpd of the MPC973 is a function of the configuration used.

When used as a zero delay buffer the MPC973 will likely be in a nested clock tree application. For these applications the MPC973 offers a LVPECL clock input as a PLL reference. This allows the user to use LVPECL as the primary clock distribution device to take advantage of its far superior skew performance. The MPC973 then can lock onto the LVPECL reference and translate with near zero delay to low skew LVCMOS outputs. Clock trees implemented in this fashion will show significantly tighter skews than trees developed from CMOS fanout buffers.

To calculate the overall uncertainty between the input reference clock and the output clocks the following approach should be used. Figure 4 through 7 contains performance information to assist in calculating the overall uncertainty. Data presented in Figures 4 through 7 is representative data but is not guaranteed under all conditions. Since the overall skew performance is a function of the input reference frequency all of the graphs provide relevant data with respect to the input reference frequency.

The overall uncertainty can be broken down into three parts; the static phase offset variation (Tpd), the I/O phase jitter and the output skew. If we assume that we have a 75 MHz reference clock, from the graphs we can pull the following information for

static phase offset (SPO) and I/O jitter: the SPO variation will be 300 ps (–100 ps to +200 ps assuming a TCLK is used) and the I/O jitter will be ± 105 ps (assuming a VCO/6 configuration and a ± 3 sigma for min and max). The nominal delay from Figure 5 is 50 ps so that the propagation delay between the reference clock and the feedback clock is 50 ps ± 255 ps.

Figure 4 can now be used to establish the uncertainty between the reference clock and all of the outputs for the MPC973. Figure 4 provides the skew of the MC973 outputs with respect to the feedback output. From Figure 4, if all of the outputs are used the propagation delay of the device will range from –555 ps (50 ps – 255 ps – 350 ps) to +705 ps (50 ps + 255 ps + 400 ps) for a total uncertainty of 1.26 ns. This 1.26ns uncertainty would hold true if multiple 973's are used in parallel in the application given that the skew between the reference clock for the devices were zero. Notice from the data in Figure 4 that if a subset of the outputs were used significant reductions in uncertainty could be obtained.

SYNC Output Description

In situations where output frequency relationships are not integer multiples of each other there is a need for a signal for system synchronization purposes. The SYNC output of the MPC973 is designed to specifically address this need. The MPC973 monitors the relationship between the Qa and the Qc banks of outputs. It provides a low going pulse, one period in duration, one period prior to the coincident rising edges of the Qa and Qc outputs. The duration and the placement of the pulse is dependent on the higher of the Qa and Qc output frequencies. The timing diagrams in the data sheet show the various waveforms for the SYNC output. Note that the SYNC output is defined for all possible combinations of the Qa and Qc outputs even though under some relationships the lower frequency clock could be used as a synchronizing signal.

1. Programmable Output Frequency Relationships (VCO_Sel='1')

fsela1	fsela0	Qa	fselb1	fselb0	Qb	fselc1	fselc0	Qc
0	0	VCO/4	0	0	VCO/4	0	0	VCO/2
0	1	VCO/6	0	1	VCO/6	0	1	VCO/4
1	0	VCO/8	1	0	VCO/8	1	0	VCO/6
1	1	VCO/12	1	1	VCO/10	1	1	VCO/8

2. Programmable Output Frequency Relationships (VCO_Sel='1')

fselfB2	fselfB1	fselfB0	QFB
0	0	0	VCO/4
0	0	1	VCO/6
0	1	0	VCO/8
0	1	1	VCO/10
1	0	0	VCO/8
1	0	1	VCO/12
1	1	0	VCO/16
1	1	1	VCO/20

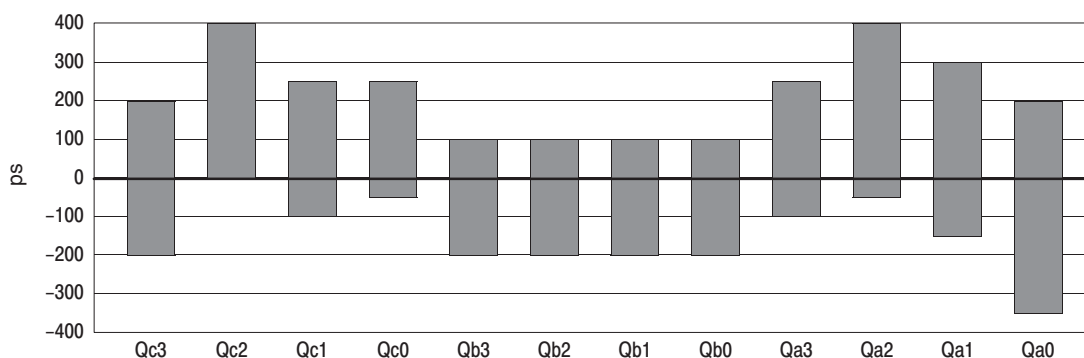
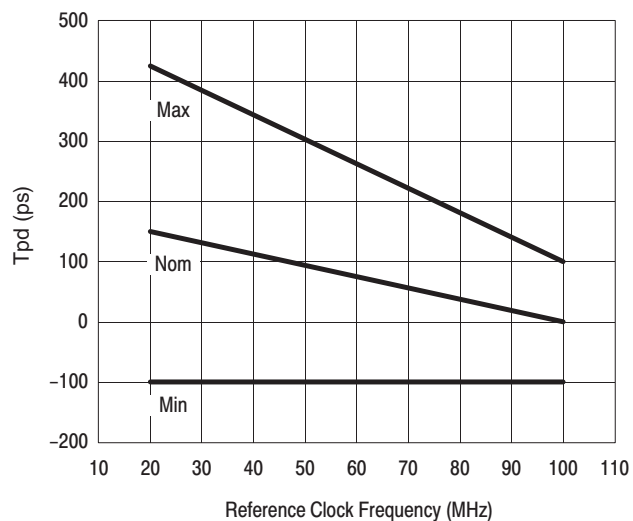
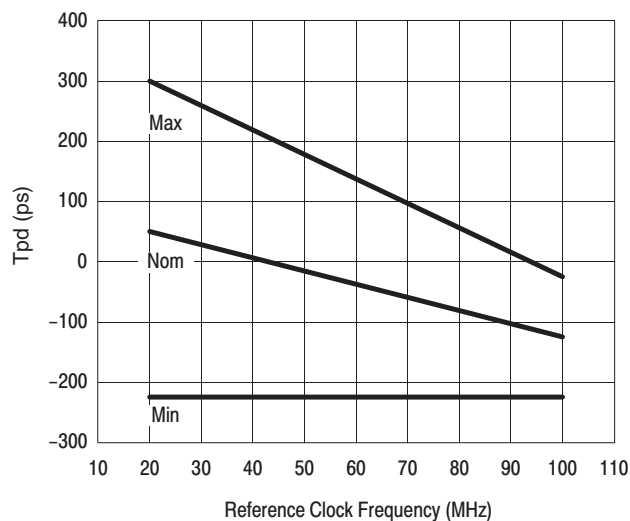
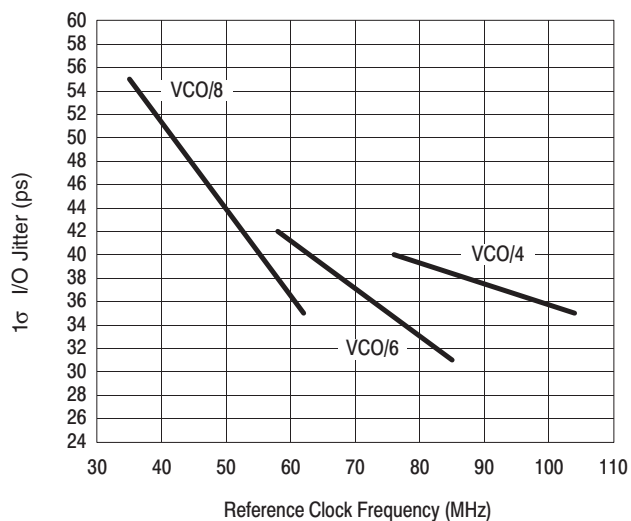


Figure 4. Typical Skews Relative to QFB

Figure 5. Typical Static Phase Offset
versus Reference Frequency
 T_{pd} versus TCLKFigure 6. Typical Static Phase Offset
versus Reference Frequency
 T_{pd} versus PCLKFigure 7. Typical Phase Jitter versus Reference Frequency
I/O Jitter

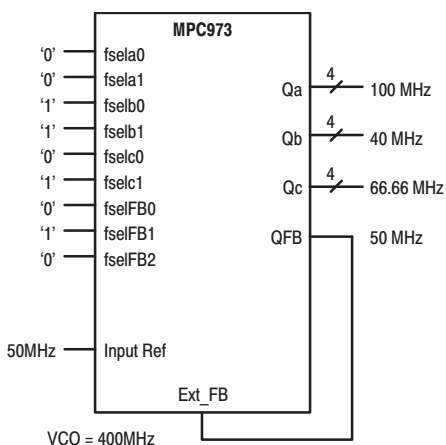


Figure 8. Programming Configuration Example

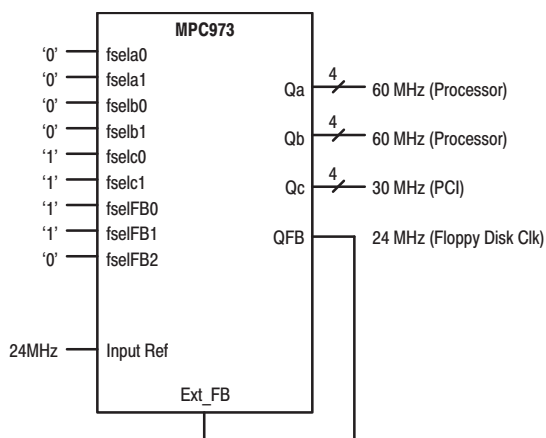


Figure 9. Generating Pentium Clocks from Floppy Clock

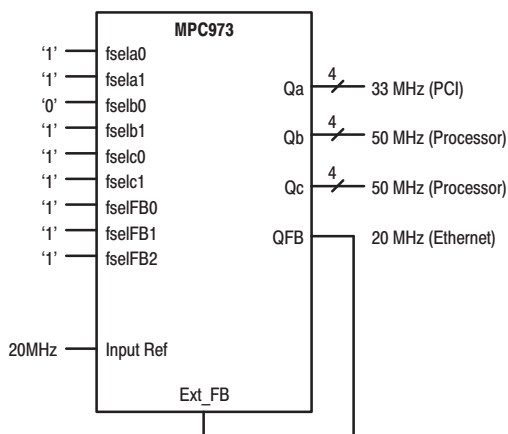


Figure 10. Generating MPC604 Clocks from Ethernet Clocks

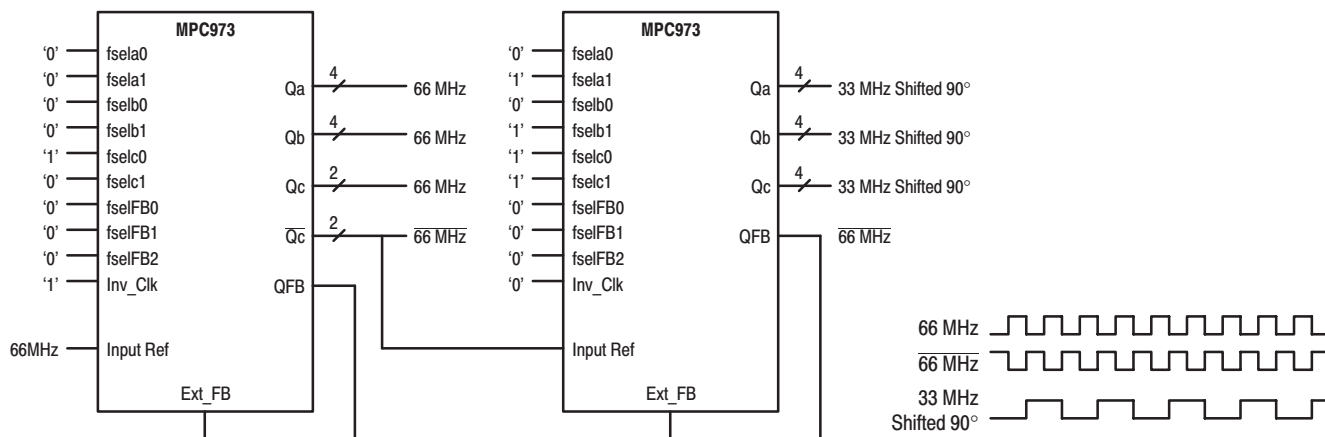


Figure 11. Phase Delay Using Multiple MPC973's

Recommended External Reset Timing

For MPC973 applications requiring synchronization of the output clock to the input clock and if $f_{selfB2} = 1$, the assertion of the $\overline{MR}$ is recommended. The timing of asserting $\overline{MR}$ should be as shown in Figure 12. The power supply should be at or above the minimum specified voltage and the reference clock input (refclk) should be present a minimum of t_1 prior to the reset pulse being applied to the $\overline{MR}$ pin.

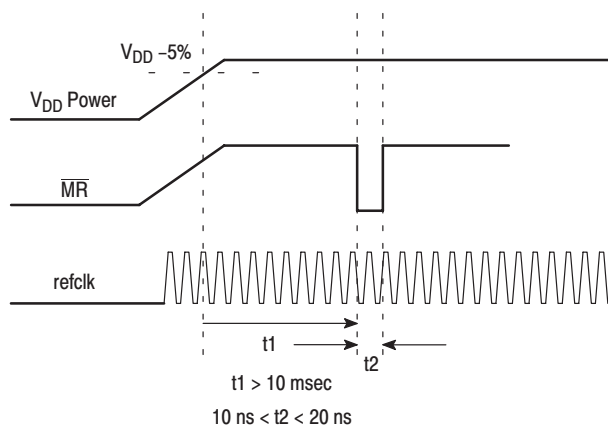


Figure 12. Assertion of $\overline{MR}$

Power Supply Filtering

The MPC973 is a mixed analog/digital product and exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC973 provides separate power supplies for the output buffers (V_{CCO}) and the internal PLL (V_{CCA}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC973.

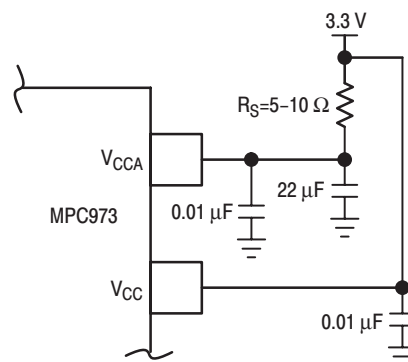


Figure 13. Power Supply Filter

Figure 13 illustrates a typical power supply filter scheme. The MPC973 is most susceptible to noise with spectral content in the 1 KHz to 1 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the MPC973. From the data sheet the I_{VCCA} current (the current sourced through the V_{CCA} pin) is typically 15 mA (20 mA maximum), assuming that a minimum of 2.935 V must be maintained on the V_{CCA} pin very little DC voltage drop can be tolerated when a 3.3 V V_{CC} supply is used. The resistor shown in Figure 13 must have a resistance of 5–10 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 KHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC973 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC973 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated

transmission lines can be used. The parallel technique terminates the signal at the end of the line with a $50\ \Omega$ resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC973 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 14 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC973 clock driver is effectively doubled due to its capability to drive multiple lines.

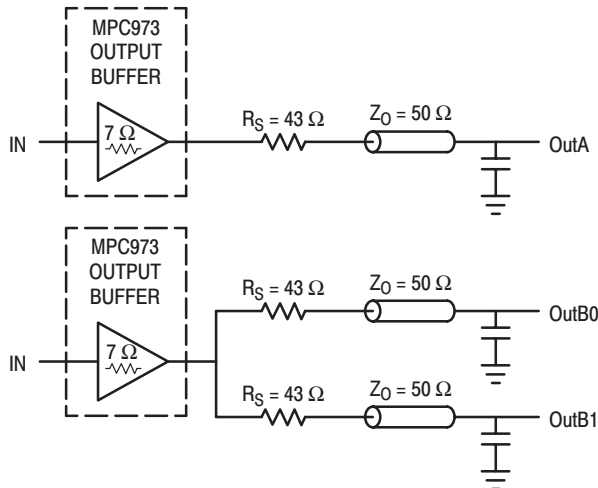


Figure 14. Single versus Dual Transmission Lines

The waveform plots of Figure 15 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC973 output buffers is more than sufficient to drive $50\ \Omega$ transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC973. The output waveform in Figure 15 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the $43\ \Omega$ series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 / R_S + R_o + Z_0) = 3.0 (25/53.5) = 1.40\text{ V}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 15 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

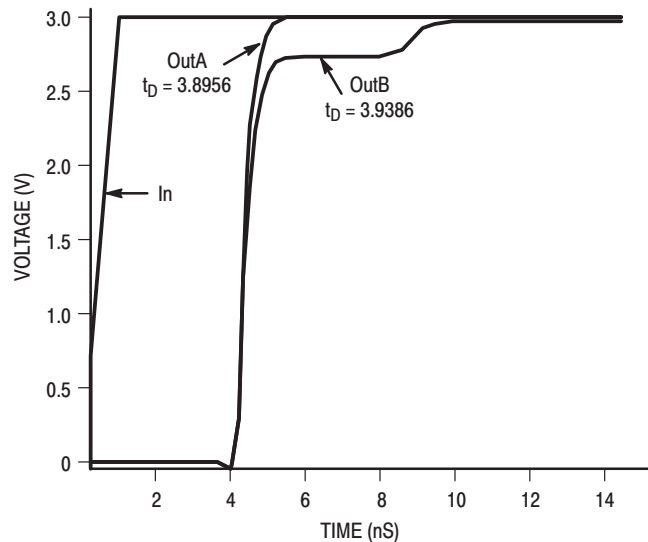


Figure 15. Single versus Dual Waveforms

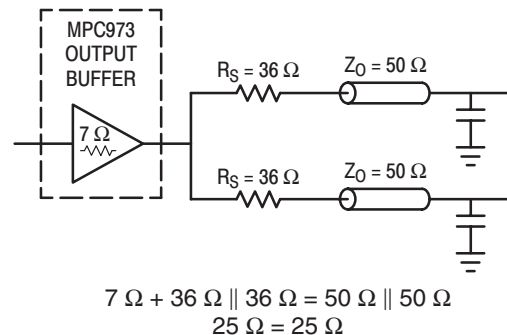


Figure 16. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Using the Output Freeze Circuitry

With the recent advent of a “green” classification for computers the desire for unique power management among system designers is keen. The individual output enable control of the MPC973 allows designers, under software control, to implement unique power management schemes into their designs. Although useful, individual output control at the expense of one pin per output is too high, therefore a simple serial interface was derived to economize on the control pins.

The freeze control logic provides a mechanism through which the MPC973 clock outputs may be frozen (stopped in the logic ‘0’ state):

The freeze mechanism allows serial loading of the 12-bit Serial Input Register, this register contains one program-mable freeze enable bit for 12 of the 14 output clocks. The Qc0 and QFB outputs cannot be frozen with the serial port, this avoids any potential lock up situation should an error occur in the loading of the Serial Input Register. The user may program an output clock to freeze by writing logic ‘0’ to the respective freeze enable bit. Likewise, the user may programmably unfreeze an output clock by writing logic ‘1’ to the respective enable bit.

The freeze logic will never force a newly-frozen clock to a logic ‘0’ state before the time at which it would normally

transition there. The logic simply keeps the frozen clock at logic '0' once it is there. Likewise, the freeze logic will never force a newly-unfrozen clock to a logic '1' state before the time at which it would normally transition there. The logic re-enables the unfrozen clock during the time when the respective clock would normally be in a logic '0' state, eliminating the possibility of 'runt' clock pulses.

The user may write to the Serial Input register through the Frz_Data input by supplying a logic '0' start bit followed serially by 12 NRZ freeze enable bits. The period of each Frz_Data bit equals the period of the free-running Frz_Clk signal. The Frz_Data serial transmission should be timed so the MPC973

can sample each Frz_Data bit with the rising edge of the free-running Frz_Clk signal.



D0-D3 are the control bits for Qa0-Qa3, respectively
D4-D7 are the control bits for Qb0-Qb3, respectively
D8-D10 are the control bits for Qc1-Qc3, respectively
D11 is the control bit for QSync

Figure 17. Freeze Data Input Protocol

3.3V PLL Clock Driver

The MPC974 is a fully integrated PLL based clock generator and clock distribution chip which operates from a 3.3V supply. The MPC974 is ideally suited for high speed, timing critical designs which need a high level of clock fanout. The device features 15 high drive LVCMOS outputs, each output has the capability of driving a 50Ω parallel terminated transmission line or two 50Ω series terminated transmission lines on the incident edge.

- Fully Integrated PLL
- Two Reference Clock Inputs for Redundant Clock Applications
- High Impedance Output Control
- Logic Enable on the Outputs
- 3.3V V_{CC} Supply
- Output Frequency Configurable
- LQFP Packaging
- ± 100 ps Typical Cycle-to-Cycle Jitter

The MPC974 features 3 independent frequency programmable banks of outputs. The frequency programmability offers the capability of establishing output frequency relationships of 1:1, 2:1, 3:1, 3:2 and 3:2:1. In addition, the device features a separate feedback output which allows for a wide variety of input/output frequency multiplication alternatives. The VCO_Sel pin provides an extended VCO lock range for added flexibility and general purpose usage.

The TCLK0 and TCLK1 inputs provide a method for dynamically switching the PLL between two different clock sources. The PLL has been optimized to provide small deviations in output pulse width and well controlled, slow transition back to lock when the inputs are switched between two references that are equal in frequency but out of phase with each other. This feature makes the MPC974 a solution for fault tolerant applications which require redundant clock sources.

For designs in which fault tolerance is critical, other products may provide more control over the clock switch functions. For these features please refer to the MPC993 datasheet.

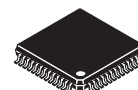
All of the control pins are LVTTTL/LVCMOS level inputs. The Fsel pins control the VCO divide ratios that are applied to the various output banks and the feedback output. The $\overline{MR}$ input will reset the internal flip flops and place the outputs in high impedance when driven LOW. The OE pin will force all of the outputs except the feedback output LOW to allow for acquiring phase lock prior to providing clocks to the rest of the system. Note that the OE pin is not synchronized to the internal clock. As a result, the initial pulse after de-assertion of the OE pin may be distorted. The PLL_En pin allows the PLL to be bypassed for board level functional test. When bypassed the signal on the selected TCLK will be routed around the PLL and will drive the internal dividers directly.

The MPC974 is packaged in the 52-lead LQFP package to provide optimum electrical performance as well as minimize board space requirements. The device is specified for 3.3V V_{CC} .

MPC974

See Upgrade Product – MPC9774

LOW VOLTAGE PLL CLOCK DRIVER



FA SUFFIX
52-LEAD LQFP PACKAGE
CASE 848D-03

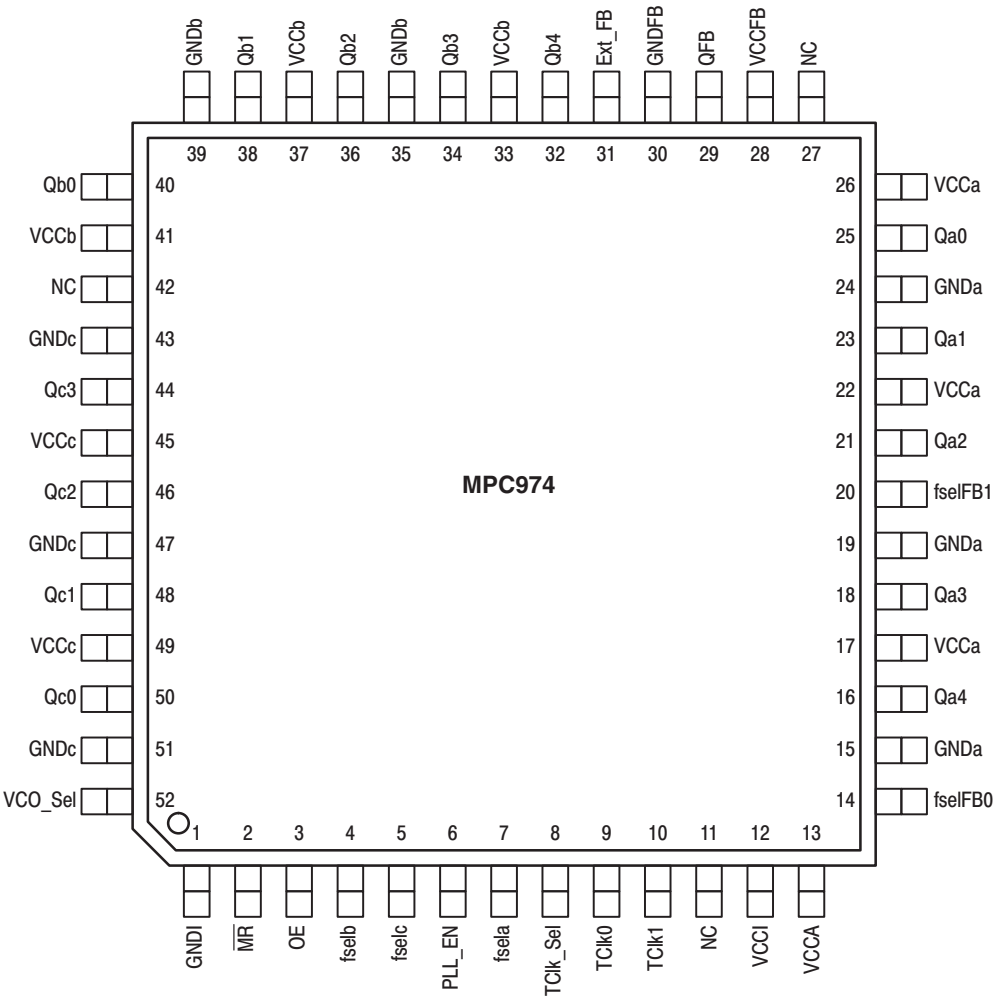


Figure 1. 52-Lead Pinout (Top View)

FUNCTION TABLE 1

fsela	Qa	fselb	Qb	fselc	Qc
0	÷2	0	÷2	0	÷4
1	÷4	1	÷4	1	÷6

FUNCTION TABLE 2

fselFB0	fselFB1	QFB
0	0	÷4
0	1	÷6
1	0	÷8
1	1	÷12

FUNCTION TABLE 3

VCO_Sel	fVCO
0	VCO/2
1	VCO/4

FUNCTION TABLE 4

Control Pin	Logic '0'	Logic '1'
MR	Master Reset/Output High Z	–
PLL_EN	Bypass PLL	Enable PLL
TCik_Sel	TCLK0	TCLK1
OE	Qa, Qb, Qc Logic LOW	All Outputs Enabled

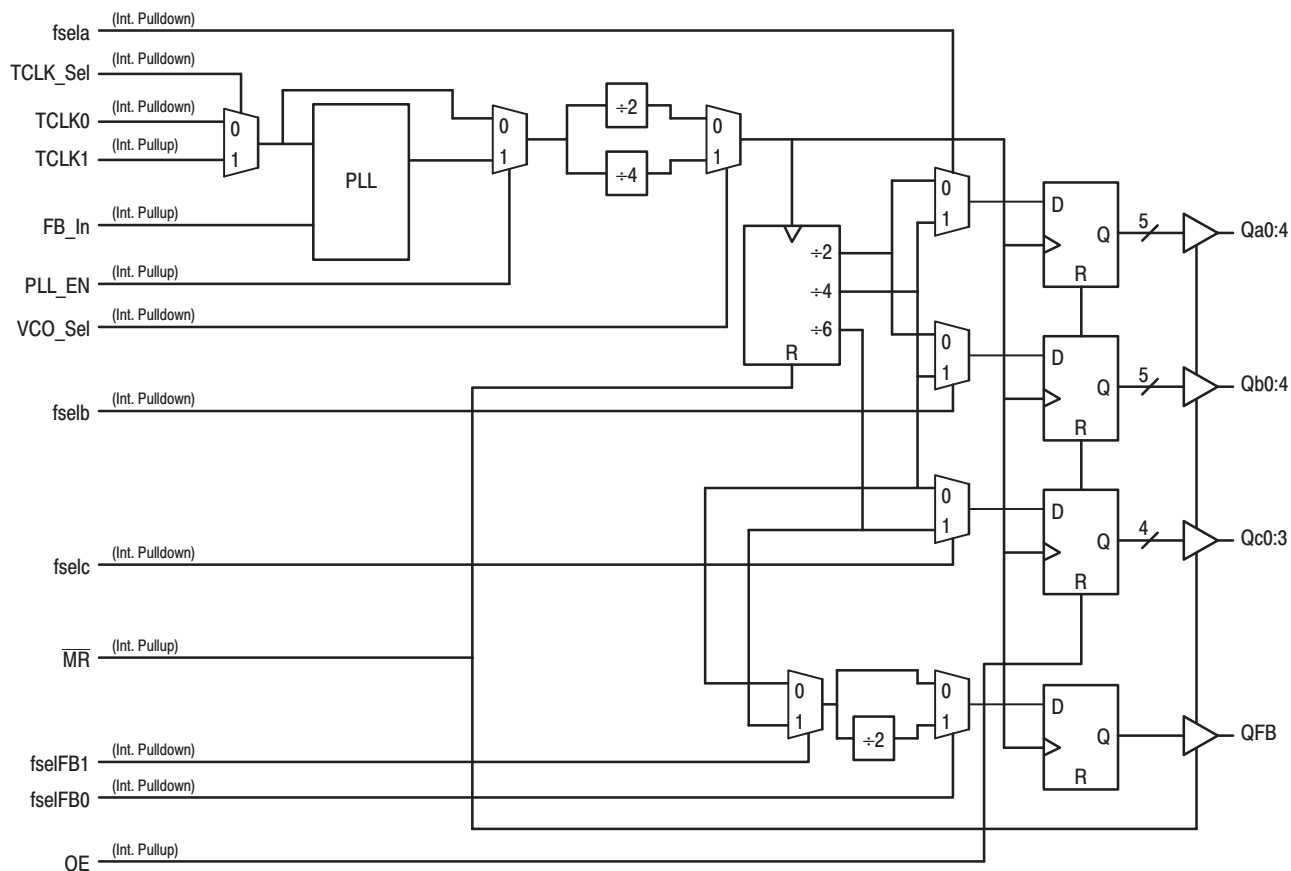


Figure 2. Logic Diagram

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	5.6	V
V_I	Input Voltage	-0.3	$V_{CC} + 0.3$	V
I_{IN}	Input Current		8	mA
T_{Stor}	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

THERMAL CHARACTERISTICS

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -20\text{mA}$ (Note 1.)
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 20\text{mA}$ (Note 1.)
I_{IN}	Input Current			± 100	μA	Note 2.
I_{CC}	Maximum Quiescent Supply Current			120	mA	
C_{IN}	Input Capacitance			8	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	Per Output

1. The MPC974 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}/2$) transmission lines on the incident edge (see Applications Info section).

2. Inputs have either pull-up or pull-down resistors which affect input current.

PLL INPUT REFERENCE CHARACTERISTICS ($T_A = 0$ to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	Note 3.	Note 3.	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

3. Input reference frequency is limited by the divider selection and the VCO lock range.

AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time	0.15		1.5	ns	0.8 to 2.0V, Note 4.
t_{pw}	Output Duty Cycle	$t_{CYCLE}/2$ -800	$t_{CYCLE}/2$ ± 500	$t_{CYCLE}/2$ +800	ps	Note 4.
f_{VCO}	PLL VCO Lock Range $f_{seln}, f_{selfBn} = +4$ to $+12$	200		500	MHz	Note 5.
t_{pd}	SYNC to Feedback Propagation Delay	-250		100	ps	Notes 4., 6.
t_{os}	Output-to-Output Skew			350	ps	Note 4.
f_{max}	Maximum Output Frequency Q (+2) Q (+4) Q (+6)			125 63 42	MHz	VCO_Sel = 0
t_{PZL}	Output Enable Time	2		10	ns	Note 4.
t_{PLZ}, t_{PHZ}	Output Disable Time	2		10	ns	Note 4.
t_{jitter}	Cycle-to-Cycle Jitter (Peak-to-Peak)		± 100		ps	Note 4.
t_{lock}	Maximum PLL Lock Time			10	ms	

4. 50Ω transmission lines terminated to $V_{CC}/2$.

5. The PLL will be unstable if the total divide between the VCO and the feedback pin is less < 8. VCO_SEL = '0', f_sela or f_selb = '0' cannot be used for the PLL feedback signal.

6. t_{pd} is specified for 50MHz input reference. The window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The t_{pd} does not include jitter.

APPLICATIONS INFORMATION**Programming the MPC974**

The MPC974 clock driver outputs can be configured into several frequency relationships, in addition the external feedback option allows for a great deal of flexibility in establishing unique input-to-output frequency relationships. The output dividers for the four output groups allows the user to configure the outputs into 1:1, 2:1, 3:2 and 3:2:1 frequency ratios. The use of even dividers ensures that the output duty cycle is always 50%. Function Table 1 illustrates the various output configurations, the table describes the outputs using the VCO frequency as a reference. As an example for a 3:2:1 relationship the Qa outputs would be set at VCO/2, the Qb's and Qc's at VCO/4 and the Qd's at VCO/6. These settings will provide output frequencies with a 3:2:1 relationship.

The division settings establish the output relationship, but one must still ensure that the VCO will be stable given the frequency of the outputs desired. The VCO lock range can be found in the specification tables. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL is such that for output frequencies between 10 and 125MHz the MPC974 can generally be configured into a stable region.

The relationship between the input reference and the output frequency is also very flexible. The separate PLL feedback output allows for a wide range of output vs input frequency

relationships. Function Table 1 can be used to identify the potential relationships available. Figure 3 illustrates several programming possibilities, although not exhaustive it is representative of the potential applications.

Using the MPC974 as a Zero Delay Buffer

The external feedback option of the MPC974 clock driver allows for its use as a zero delay buffer. By using one of the outputs as a feedback to the PLL the propagation delay through the device is near zero. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The static phase offset is a function of the input reference frequency of the MPC974. The Tpd of the device is specified in the specification tables.

To minimize part-to-part skew the external feedback option again should be used. The PLL in the MPC974 decouples the delay of the device from the propagation delay variations of the internal gates. From the specification table one sees a Tpd variation of only $\pm 150\text{ps}$, thus for multiple devices under identical configurations the part-to-part skew will be around 850ps (300ps for Tpd variation plus 350ps output-to-output skew plus 200ps for jitter). To minimize this value, the highest possible reference frequencies should be used. Higher reference frequencies will minimize both the t_{pd} parameter as well as the input to output jitter.

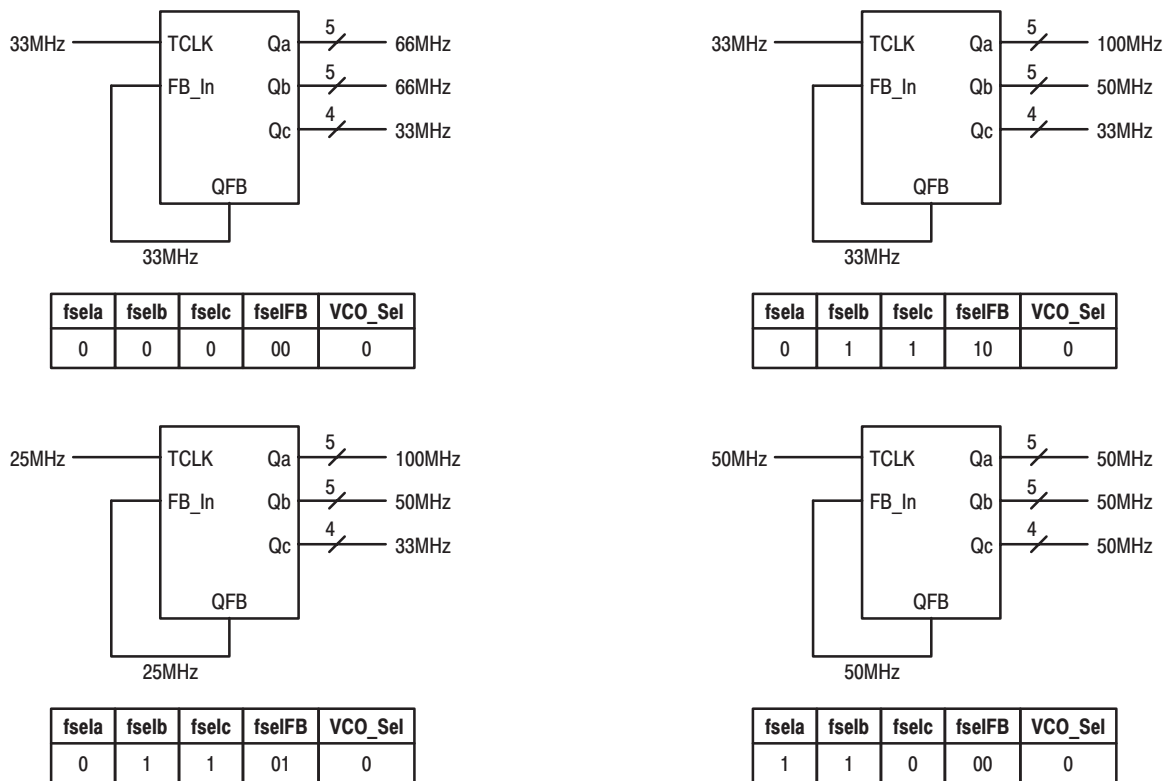


Figure 3. MPC974 Programming Schemes

Power Supply Filtering

The MPC974 is a mixed analog/digital product and exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC974 provides separate power supplies for the output buffers (V_{CCO}) and the internal PLL (V_{CCA}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC974.

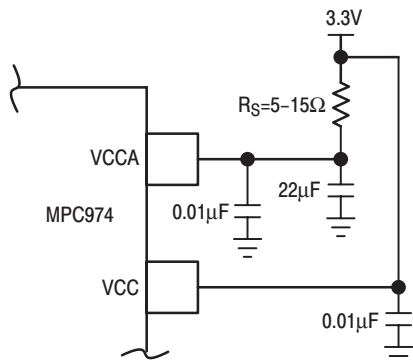


Figure 4. Power Supply Filter

Figure 4 illustrates a typical power supply filter scheme. The MPC974 is most susceptible to noise with spectral content in

the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the MPC974. From the data sheet the I_{VCCA} current (the current sourced through the V_{CCA} pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the V_{CCA} pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 4 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC974 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC974 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

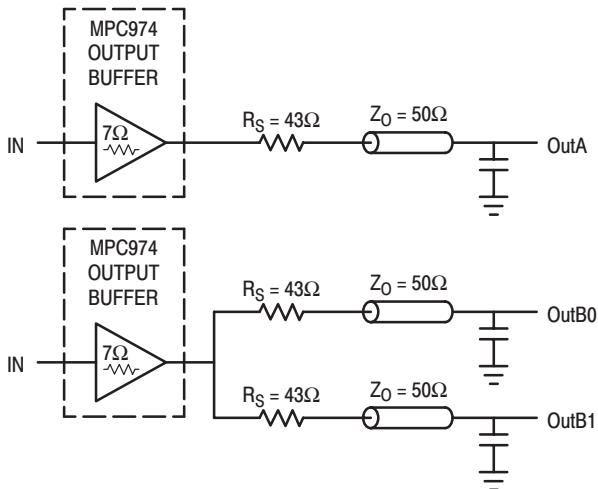


Figure 5. Single versus Dual Transmission Lines

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC974 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 5 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fan-out of the MPC974 clock driver is effectively doubled due to its capability to drive multiple lines.

The waveform plots of Figure 6 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC974 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC974. The output waveform in Figure 6 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match

the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

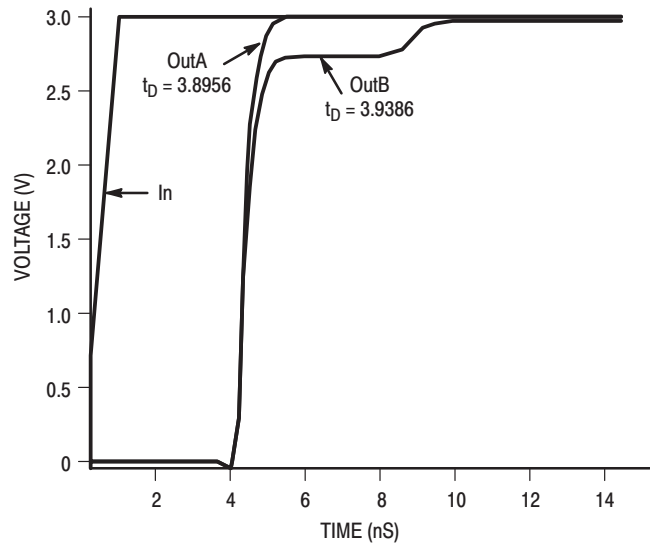


Figure 6. Single versus Dual Waveforms

$$V_L = V_S (Z_0 / R_S + R_o + Z_0) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 7 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

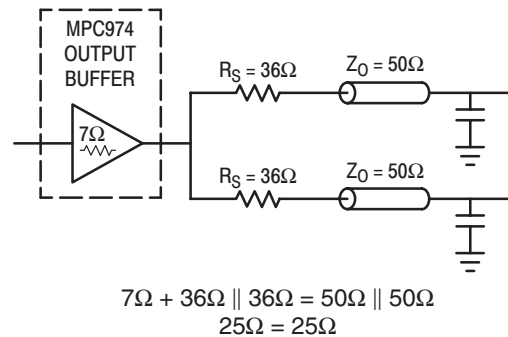


Figure 7. Optimized Dual Line Termination

2

3.3V 1:12 LVCMOS PLL Clock Generator

The MPC9772 is a 3.3V compatible, 1:12 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance networking, computing and telecom applications. With output frequencies up to 240 MHz and output skews less than 250 ps the device meets the needs of the most demanding clock applications.

Features

- 1:12 PLL based low-voltage clock generator
- 3.3V power supply
- Internal power-on reset
- Generates clock signals up to 240 MHz
- Maximum output skew of 250 ps
- On-chip crystal oscillator clock reference
- Two LVCMOS PLL reference clock inputs
- External PLL feedback supports zero-delay capability
- Various feedback and output dividers (see application section)
- Supports up to three individual generated output clock frequencies
- Synchronous output clock stop circuitry for each individual output for power down support
- Drives up to 24 clock lines
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MPC972

Functional Description

The MPC9772 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9772 requires the connection of the PLL feedback output QFB to feedback input FB_IN to close the PLL feedback path. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. The MPC9772 features an extensive level of frequency programmability between the 12 outputs as well as the output to input relationships, for instance 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 5:1, 5:2, 5:3, 5:4, 5:6, 6:1, 8:1 and 8:3.

The QSYNC output will indicate when the coincident rising edges of the above relationships will occur. The selectability of the feedback frequency is independent of the output frequencies. This allows for very flexible programming of the input reference versus output frequency relationship. The output frequencies can be either odd or even multiples of the input reference. In addition the output frequency can be less than the input frequency for applications where a frequency needs to be reduced by a non-binary factor. The MPC9772 also supports the 180° phase shift of one of its output banks with respect to the other output banks. The QSYNC outputs reflects the phase relationship between the QA and QC outputs and can be used for the generation of system baseline timing signals.

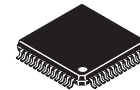
The REF_SEL pin selects the internal crystal oscillator or the LVCMOS compatible inputs as the reference clock signal. Two alternative LVCMOS compatible clock inputs are provided for clock redundancy support. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The outputs can be individually disabled (stopped in logic low state) by programming the serial CLOCK_STOP interface of the MPC9772. The MPC9772 has an internal power-on reset.

The MPC9772 is fully 3.3V compatible and requires no external loop filter components. All inputs (except XTAL) accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9772 outputs can drive one or two traces giving the devices an effective fanout of 1:24. The device is pin and function compatible to the MPC972 and is packaged in a 52-lead LQFP package.

MPC9772

**3.3V 1:12 LVCMOS
PLL CLOCK GENERATOR**



FA SUFFIX
52 LEAD LQFP PACKAGE
CASE 848D



Table 1. PIN CONFIGURATION

Pin	I/O	Type	Function
CCLK0	Input	LVC MOS	PLL reference clock
CCLK1	Input	LVC MOS	Alternative PLL reference clock
XTAL_IN, XTAL_OUT		Analog	Crystal oscillator interface
FB_IN	Input	LVC MOS	PLL feedback signal input, connect to an QFB
CCLK_SEL	Input	LVC MOS	LVC MOS clock reference select
REF_SEL	Input	LVC MOS	LVC MOS/PECL reference clock select
VCO_SEL	Input	LVC MOS	VCO operating frequency select
PLL_EN	Input	LVC MOS	PLL enable/PLL bypass mode select
MR/OE	Input	LVC MOS	Output enable/disable (high-impedance tristate) and device reset
FSEL_A[0:1]	Input	LVC MOS	Frequency divider select for bank A outputs
FSEL_B[0:1]	Input	LVC MOS	Frequency divider select for bank B outputs
FSEL_C[0:1]	Input	LVC MOS	Frequency divider select for bank C outputs
FSEL_FB[0:2]	Input	LVC MOS	Frequency divider select for the QFB output
INV_CLK	Input	LVC MOS	Clock phase selection for outputs QC2 and QC3
STOP_CLK	Input	LVC MOS	Clock input for clock stop circuitry
STOP_DATA	Input	LVC MOS	Configuration data input for clock stop circuitry
QA[0-3]	Output	LVC MOS	Clock outputs (Bank A)
QB[0-3]	Output	LVC MOS	Clock outputs (Bank B)
QC[0-3]	Output	LVC MOS	Clock outputs (Bank C)
QFB	Output	LVC MOS	PLL feedback output. Connect to FB_IN.
QSYNC	Output	LVC MOS	Synchronization pulse output
GND	Supply	Ground	Negative power supply
VCC_PLL	Supply	VCC	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V _{CC_PLL} . Please see applications section for details.
VCC	Supply	VCC	Positive power supply for I/O and core. All VCC pins must be connected to the positive power supply for correct operation

Table 2. FUNCTION TABLE (Configuration Controls)

Control	Default	0	1
REF_SEL	1	Selects CCLKx as the PLL reference clock	Selects the crystal oscillator as the PLL reference clock
CCLK_SEL	1	Selects CCLK0	Selects CCLK1
VCO_SEL	1	Selects VCO+2. The VCO frequency is scaled by a factor of 2 (low VCO frequency range).	Selects VCO+1. (high VCO frequency range)
PLL_EN	1	Test mode with the PLL bypassed. The reference clock is substituted for the internal VCO output. MPC9772 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Normal operation mode with PLL enabled.
INV_CLK	1	QC2 and QC3 are in phase with QC0 and QC1	QC2 and QC3 are inverted (180° phase shift) with respect to QC0 and QC1
MR/OE	1	Outputs disabled (high-impedance state) and device is reset. During reset/output disable the PLL feedback loop is open and the internal VCO is tied to its lowest frequency. The MPC9772 requires reset after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLKx). The device is reset by the internal power-on reset (POR) circuitry during power-up.	Outputs enabled (active)
VCO_SEL, FSEL_A[0:1], FSEL_B[0:1], FSEL_C[0:1], FSEL_FB[0:2] control the operating PLL frequency range and input/output frequency ratios. See Table 3 to Table 6 and the applications section for supported frequency ranges and output to input frequency ratios.			

Table 3. Output Divider Bank A (N_A)

VCO_SE L	FSEL_A1	FSEL_A0	QA[0:3]
0	0	0	VCO÷8
0	0	1	VCO÷12
0	1	0	VCO÷16
0	1	1	VCO÷24
1	0	0	VCO÷4
1	0	1	VCO÷6
1	1	0	VCO÷8
1	1	1	VCO÷12

Table 4. Output Divider Bank B (N_B)

VCO_SE L	FSEL_B1	FSEL_B0	QB[0:3]
0	0	0	VCO÷8
0	0	1	VCO÷12
0	1	0	VCO÷16
0	1	1	VCO÷20
1	0	0	VCO÷4
1	0	1	VCO÷6
1	1	0	VCO÷8
1	1	1	VCO÷10

Table 5. Output Divider Bank C (N_C)

VCO_SE L	FSEL_C1	FSEL_C0	QC[0:3]
0	0	0	VCO÷4
0	0	1	VCO÷8
0	1	0	VCO÷12
0	1	1	VCO÷16
1	0	0	VCO÷2
1	0	1	VCO÷4
1	1	0	VCO÷6
1	1	1	VCO÷8

2

Table 6. Output Divider PLL Feedback (M)

VCO_SEL	FSEL_FB2	FSEL_FB1	FSEL_FB0	QFB
0	0	0	0	VCO÷8
0	0	0	1	VCO÷12
0	0	1	0	VCO÷16
0	0	1	1	VCO÷20
0	1	0	0	VCO÷16
0	1	0	1	VCO÷24
0	1	1	0	VCO÷32
0	1	1	1	VCO÷40
1	0	0	0	VCO÷4
1	0	0	1	VCO÷6
1	0	1	0	VCO÷8
1	0	1	1	VCO÷10
1	1	0	0	VCO÷8
1	1	0	1	VCO÷12
1	1	1	0	VCO÷16
1	1	1	1	VCO÷20

Table 7. GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		12		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 8. ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.9	V	
V_{IN}	DC Input Voltage	-0.3	$V_{CC}+0.3$	V	
V_{OUT}	DC Output Voltage	-0.3	$V_{CC}+0.3$	V	
I_{IN}	DC Input Current		± 20	mA	
I_{OUT}	DC Output Current		± 50	mA	
T_S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 9. DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ$ to 70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{CC_PLL}	PLL Supply Voltage	3.0		V_{CC}	V	LVC MOS
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input Low Voltage			0.8	V	LVC MOS
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -24 \text{ mA}^a$
V_{OL}	Output Low Voltage			0.55 0.30	V V	$I_{OL} = 24 \text{ mA}$ $I_{OL} = 12 \text{ mA}$
Z_{OUT}	Output Impedance		14 - 17		Ω	
I_{IN}	Input Current ^b			± 200	μA	$V_{IN} = V_{CC}$ or GND
I_{CC_PLL}	Maximum PLL Supply Current		8.0	13.5	mA	V_{CC_PLL} Pin
I_{CCQ}	Maximum Quiescent Supply Current			35	mA	All V_{CC} Pins

a. The MPC9772 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines.

b. Inputs have pull-down resistors affecting the input current.

Table 10. AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ$ to $70^\circ C$)^{a b}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{REF}	Input reference frequency					
	+4 feedback	50.0		120.0	MHz	PLL locked
	+6 feedback	33.3		80.0	MHz	
	+8 feedback	25.0		60.0	MHz	
	+10 feedback	20.0		48.0	MHz	
	+12 feedback	16.6		40.0	MHz	
	+16 feedback	12.5		30.0	MHz	
	+20 feedback	10.0		24.0	MHz	
	+24 feedback	8.33		20.0	MHz	
	+32 feedback	6.25		15.0	MHz	
	+40 feedback	5.00		12.0	MHz	
	Input reference frequency in PLL bypass mode ^c			250	MHz	PLL bypass
f_{VCO}	VCO frequency range ^d	200		480	MHz	
f_{XTAL}	Crystal interface frequency range ^d	10		25	MHz	
f_{MAX}	Output Frequency					
	+2 output	100.0		240.0	MHz	PLL locked
	+4 output	50.0		120.0	MHz	
	+6 output	33.3		80.0	MHz	
	+8 output	25.0		60.0	MHz	
	+10 output	20.0		48.0	MHz	
	+12 output	16.6		40.0	MHz	
	+16 output	12.5		30.0	MHz	
	+20 output	10.0		24.0	MHz	
	+24 output	8.33		20.0	MHz	
f_{STOP_CLK}	Serial interface clock frequency			20	MHz	
$t_{PW,MIN}$	Input Reference Pulse Width ^e	2.0			ns	
t_R, t_F	CCLKx Input Rise/Fall Time ^f			1.0	ns	0.8 to 2.0V
$t_{(\phi)}$	Propagation Delay (static phase offset) ^g CCLK to FB_IN					PLL locked
	6.25 MHz < f_{REF} < 65.0 MHz	-3		+3	°	
	65.0 MHz < f_{REF} < 125 MHz	-4		+4	°	
	$f_{REF}=50$ MHz and feedback= ± 8	-166		+166	ps	
$t_{SK(O)}$	Output-to-output Skew ^h					
	within QA outputs			100	ps	
	within QB outputs			100	ps	
	within QC outputs			100	ps	
	all outputs			250	ps	
DC	Output Duty Cycle ⁱ	(T $\div$ 2) - 200	T $\div$ 2	(T $\div$ 2) +200	ps	
t_R, t_F	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time			8.0	ns	
$t_{PZL, LZ}$	Output Enable Time			8.0	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter ^j		150	200	ps	
$t_{JIT(PER)}$	Period Jitter ^k			150	ps	
$t_{JIT(\phi)}$	I/O Phase Jitter RMS (1 σ) ^l					
	+4 feedback			11	ps	(VCO=400 MHz)
	+6 feedback			86	ps	
	+8 feedback			13	ps	
	+10 feedback			88	ps	
	+12 feedback			16	ps	
	+16 feedback			19	ps	
	+20 feedback			21	ps	
	+24 feedback			22	ps	
	+32 feedback			27	ps	
	+40 feedback			30	ps	

Table 10. AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ$ to 70°C)^{a b}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
BW	PLL closed loop bandwidth ^m					
	+4 feedback		1.20 - 3.50		MHz	
	+6 feedback		0.70 - 2.50		MHz	
	+8 feedback		0.50 - 1.80		MHz	
	+10 feedback		0.45 - 1.20		MHz	
	+12 feedback		0.30 - 1.00		MHz	
	+16 feedback		0.25 - 0.70		MHz	
	+20 feedback		0.20 - 0.55		MHz	
	+24 feedback		0.17 - 0.40		MHz	
	+32 feedback		0.12 - 0.30		MHz	
	+40 feedback		0.11 - 0.28		MHz	
t _{LOCK}	Maximum PLL Lock Time			10	ms	

a AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b In bypass mode, the MPC9772 divides the input reference clock.

c The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{REF} = f_{VCO} \div (M \cdot VCO\_SEL)$.

d The crystal frequency range must both meet the interface frequency range and VCO lock range divided by the feedback divider ratio:

$$f_{XTAL(min, max)} = f_{VCO(min, max)} \div (M \cdot VCO\_SEL) \text{ and } 10 \text{ MHz} \leq f_{XTAL} \leq 25 \text{ MHz.}$$

e Calculation of reference duty cycle limits: $DC_{REF, MIN} = t_{PW, MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF, MAX} = 100\% - DC_{REF, MIN}$.

f The MPC9772 will operate with input rise/fall times up to 3.0 ns, but the A.C. characteristics, specifically $t_{(\phi)}$, $t_{PW, MIN}$, DC and f_{MAX} can only be guaranteed if t_R , t_F are within the specified range.

g Static phase offset depends on the reference frequency. $t_{(\phi)} [s] = t_{(\phi)} [^\circ] \div (f_{REF} \cdot 360^\circ)$.

h Excluding QSYNC output. See application section for part-to-part skew calculation.

i Output duty cycle is $DC = (0.5 \pm 200 \text{ ps} \cdot f_{OUT}) \cdot 100\%$. E.g. the DC range at $f_{OUT}=100\text{MHz}$ is $48\% < DC < 52\%$. T = output period.

j Cycle jitter is valid for all outputs in the same divider configuration. See application section for more details.

k Period jitter is valid for all outputs in the same divider configuration. See application section for more details.

l I/O jitter is valid for a VCO frequency of 400 MHz. See application section for I/O jitter vs. VCO frequency.

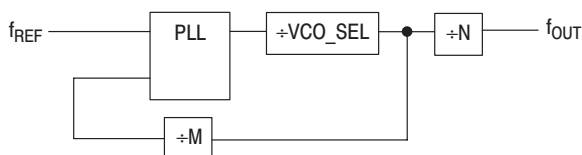
m -3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

MPC9772 Configurations

Configuring the MPC9772 amounts to properly configuring the internal dividers to produce the desired output frequencies. The output frequency can be represented by this formula:

$$f_{OUT} = f_{REF} \cdot M \div N$$



where f_{REF} is the reference frequency of the selected input clock source (CCLK0, CCLK1 or XTAL interface), M is the PLL feedback divider and N is a output divider. The PLL feedback divider is configured by the FSEL_FB[2:0] and the output dividers are individually configured for each output bank by the FSEL_A[1:0], FSEL_B[1:0] and FSEL_C[1:0] inputs.

The reference frequency f_{REF} and the selection of the feedback-divider M is limited by the specified VCO frequency range. f_{REF} and M must be configured to match the VCO frequency range of 200 to 480 MHz in order to achieve stable PLL operation:

$$f_{VCO,MIN} \leq (f_{REF} \cdot VCO\_SEL \cdot M) \leq f_{VCO,MAX}$$

The PLL post-divider VCO_SEL is either a divide-by-one or a divide-by-two and can be used to situate the VCO into the specified frequency range. This divider is controlled by the

VCO_SEL pin. VCO_SEL effectively extends the usable input frequency range while it has no effect on the output to reference frequency ratio.

The output frequency for each bank can be derived from the VCO frequency and output divider:

$$f_{QA[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_A)$$

$$f_{QB[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_B)$$

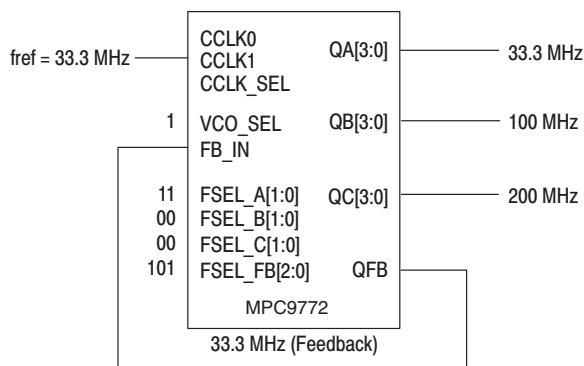
$$f_{QC[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_C)$$

Table 11. MPC9772 Divider

Divider	Function	VCO_SEL	Values
M	PLL feedback FSEL_FB[0:3]	÷1	4, 6, 8, 10, 12, 16
		÷2	8, 12, 16, 20, 24, 32, 40
N _A	Bank A Output Divider FSEL_A[0:1]	÷1	4, 6, 8, 12
		÷2	8, 12, 16, 24
N _B	Bank B Output Divider FSEL_B[0:1]	÷1	4, 6, 8, 10
		÷2	8, 12, 16, 20
N _C	Bank C Output Divider FSEL_C[0:1]	÷1	2, 4, 6, 8
		÷2	4, 8, 12, 16

Table 11 shows the various PLL feedback and output dividers and Figure 3 and Figure 4 display example configurations for the MPC9772:

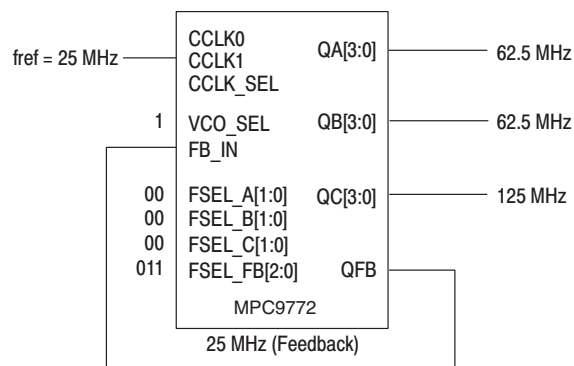
Figure 3. Example Configuration



MPC9772 example configuration (feedback of QFB = 33.3 MHz, f_{VCO} =400 MHz, VCO_SEL=÷1, M=12, N_A=12, N_B=4, N_C=2).

Frequency range	Min	Max
Input	16.6 MHz	40 MHz
QA outputs	16.6 MHz	40 MHz
QB outputs	50 MHz	120 MHz
QC outputs	100 MHz	240 MHz

Figure 4. Example Configuration



MPC9772 example configuration (feedback of QFB = 25 MHz, f_{VCO} =250 MHz, VCO_SEL=÷1, M=10, N_A=4, N_B=4, N_C=2).

Frequency range	Min	Max
Input	20 MHz	48 MHz
QA outputs	50 MHz	120 MHz
QB outputs	50 MHz	120 MHz
QC outputs	100 MHz	240 MHz

MPC9772 Individual Output Disable (Clock Stop) Circuitry

The individual clock stop (output enable) control of the MPC9772 allows designers, under software control, to implement power management into the clock distribution design. A simple serial interface and a clock stop control logic provides a mechanism through which the MPC9772 clock outputs can be individually stopped in the logic '0' state: The clock stop mechanism allows serial loading of a 12-bit serial input register. This register contains one programmable clock stop bit for 12 of the 14 output clocks. The QC0 and QFB outputs cannot be stopped (disabled) with the serial port.

The user can program an output clock to stop (disable) by

writing logic '0' to the respective stop enable bit. Likewise, the user may programmably enable an output clock by writing logic '1' to the respective enable bit. The clock stop logic enables or disables clock outputs during the time when the output would be in normally in logic low state, eliminating the possibility of short or 'runt' clock pulses.

The user can write to the serial input register through the STOP_DATA input by supplying a logic '0' start bit followed serially by 12 NRZ disable/enable bits. The period of each STOP_DATA bit equals the period of the free-running STOP_CLK signal. The STOP_DATA serial transmission should be timed so the MPC9772 can sample each STOP_DATA bit with the rising edge of the free-running STOP_CLK signal. (see Figure 5)



Figure 5. Clock Stop Circuit Programming

SYNC Output Description

The MPC9772 has a system synchronization pulse output QSYNC. In configurations with the output frequency relationships are not integer multiples of each other QSYNC provides a signal for system synchronization purposes. The MPC9772 monitors the relationship between the A bank and the B bank of outputs. The QSYNC output is asserted (logic low) one peri-

od in duration and one period prior to the coincident rising edges of the QA and QC outputs. The duration and the placement of the pulse is dependent QA and QC output frequencies: the QSYNC pulse width is equal to the period of the higher of the QA and QC output frequencies. Figure 6 shows various waveforms for the QSYNC output. The QSYNC output is defined for all possible combinations of the bank A and bank C outputs.

2

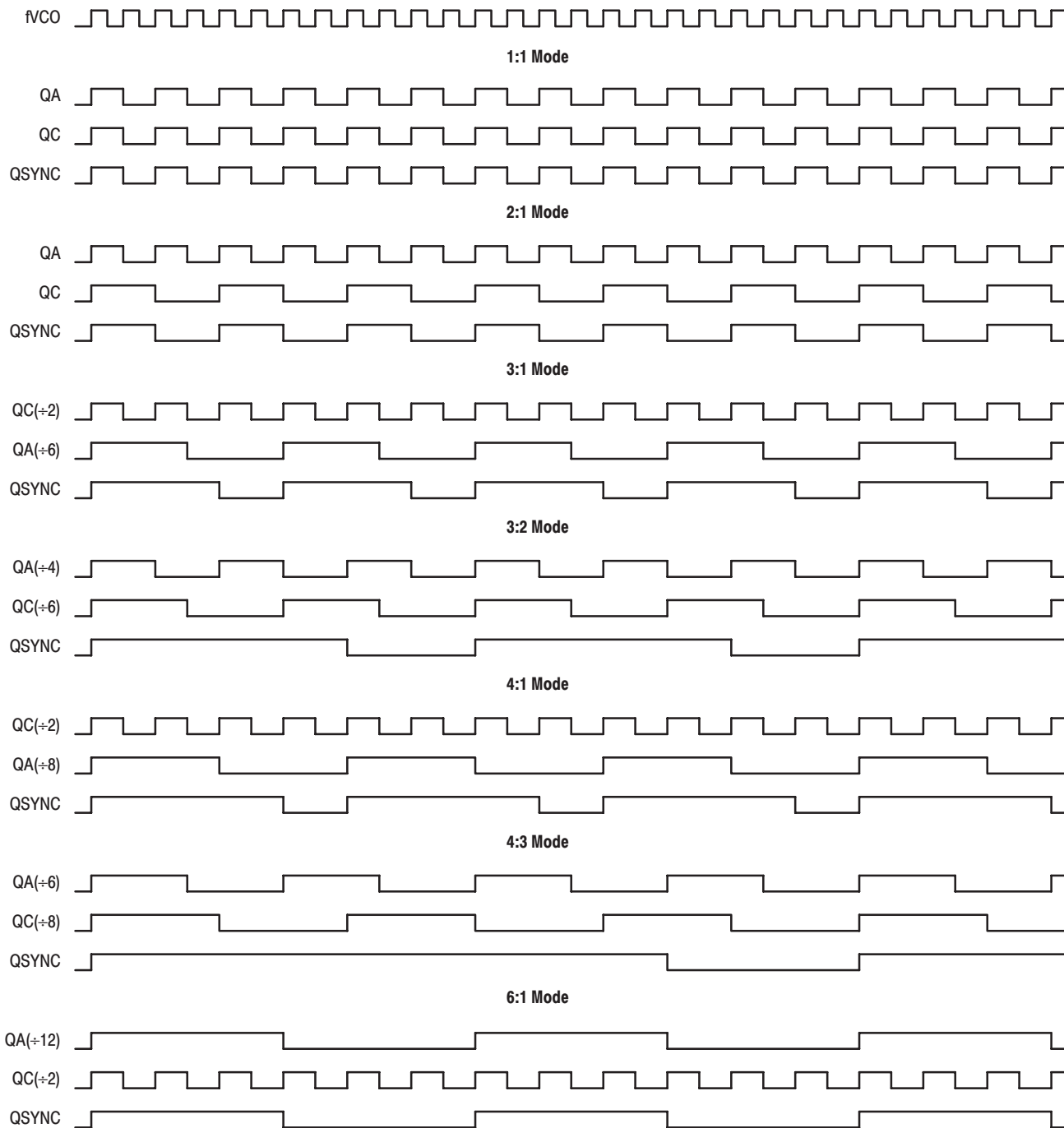


Figure 6. QSYNC Timing Diagram

Power Supply Filtering

The MPC9772 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC9772 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CC_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA_PLL} pin for the MPC9772. Figure 7 illustrates a typical power supply filter scheme. The MPC9772 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F . From the data sheet the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 8 mA (13.5 mA maximum), assuming that a minimum of 3.0V must be maintained on the V_{CC_PLL} pin. The resistor R_F shown in Figure 7 “ V_{CC_PLL} Power Supply Filter” must have a resistance of 5-10 Ω to meet the voltage drop criteria.

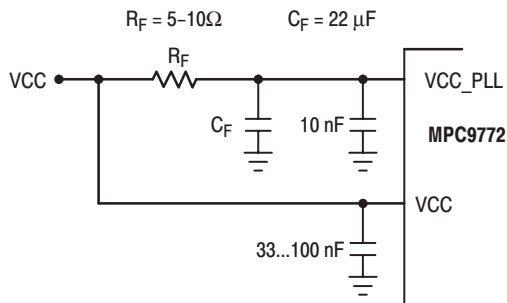


Figure 7. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 7 “ V_{CC_PLL} Power Supply Filter”, the filter cut-off frequency is around 4.5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9772 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9772 in zero-delay applications

Nested clock trees are typical applications for the MPC9772. Designs using the MPC9772 as LVCMOS PLL fan-out buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fan-out buffers. The external feedback option of the MPC9772 clock driver allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device (the propagation delay through the device is virtually eliminated). The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of part-to-part skew

The MPC9772 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9772 are connected together, the maximum overall timing uncertainty from the common CCLKx input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD, LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

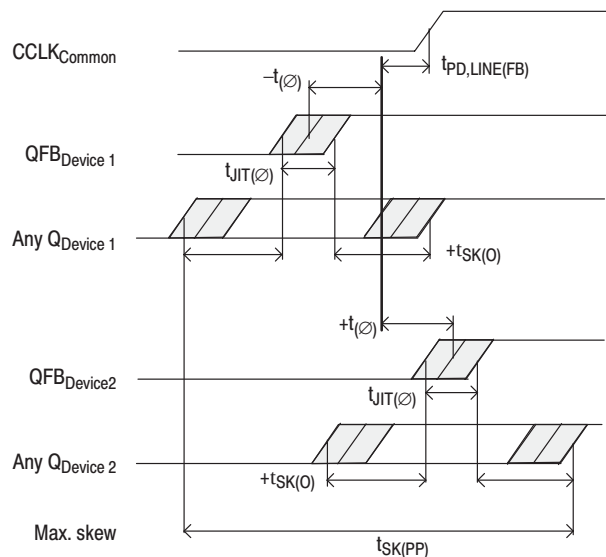


Figure 8. MPC9772 max. device-to-device skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 12.

Table 12. Confidence Factor CF

CF	Probability of clock edge within the distribution
$\pm 1\sigma$	0.68268948
$\pm 2\sigma$	0.95449988
$\pm 3\sigma$	0.99730007
$\pm 4\sigma$	0.99993663
$\pm 5\sigma$	0.99999943
$\pm 6\sigma$	0.99999999

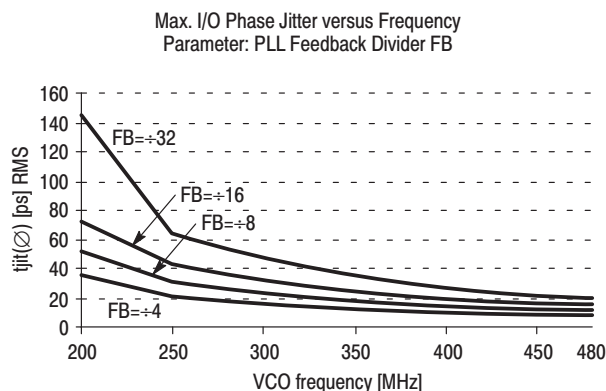
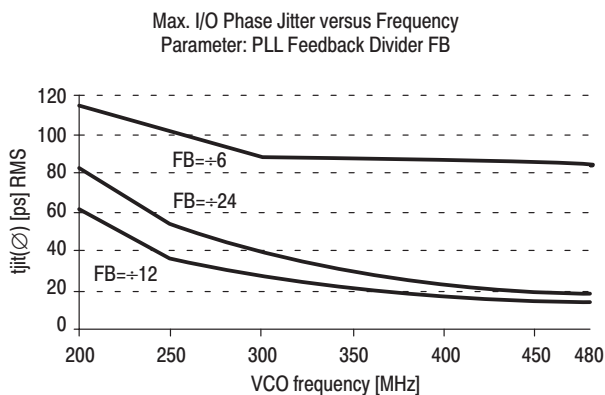
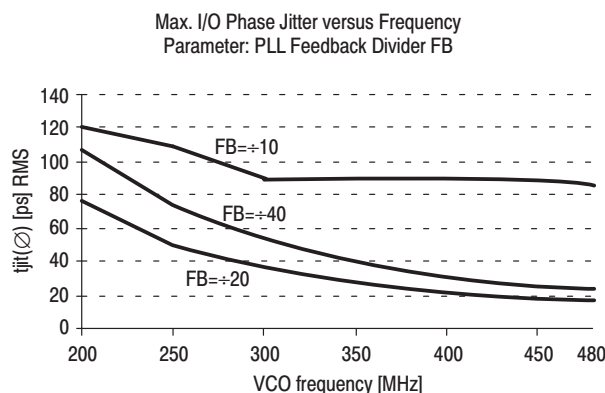
The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device.

Due to the frequency dependence of the static phase offset and I/O jitter, using Figure 9 to Figure 11 to predict a maximum I/O jitter and the specified $t_{j(\phi)}$ parameter relative to the input reference frequency results in a precise timing performance analysis.

In the following example calculation an I/O jitter confidence factor of 99.7% ($\pm 3\sigma$) is assumed, resulting in a worst case timing uncertainty from the common input reference clock to any output of -455 ps to +455 ps relative to CCLK (PLL feedback = ± 8 , reference frequency = 50 MHz, VCO frequency = 400 MHz, I/O jitter = 13 ps rms max., static phase offset $t_{j(\phi)}$ = ± 166 ps):

$$t_{SK(PP)} = [-166ps...166ps] + [-250ps...250ps] + [(13ps \cdot -3)...(13ps \cdot 3)] + t_{PD, LINE(FB)}$$

$$t_{SK(PP)} = [-455ps...455ps] + t_{PD, LINE(FB)}$$

**Figure 9. MPC9772 I/O Jitter****Figure 10. MPC9772 I/O Jitter****Figure 11. MPC9772 I/O Jitter**

Driving Transmission Lines

The MPC9772 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}+2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9772 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 12 "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9772 clock driver is effectively doubled due to its capability to drive multiple lines.

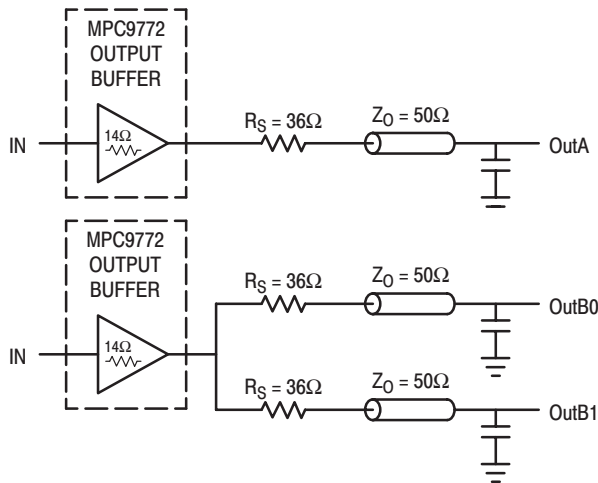


Figure 12. Single versus Dual Transmission Lines

The waveform plots in Figure 13 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9772 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9772. The output waveform in Figure 13 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned} V_L &= V_S (Z_0 \div (R_S + R_0 + Z_0)) \\ Z_0 &= 50\Omega \parallel 50\Omega \\ R_S &= 36\Omega \parallel 36\Omega \\ R_0 &= 14\Omega \\ V_L &= 3.0 (25 \div (18 + 17 + 25)) \\ &= 1.31V \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

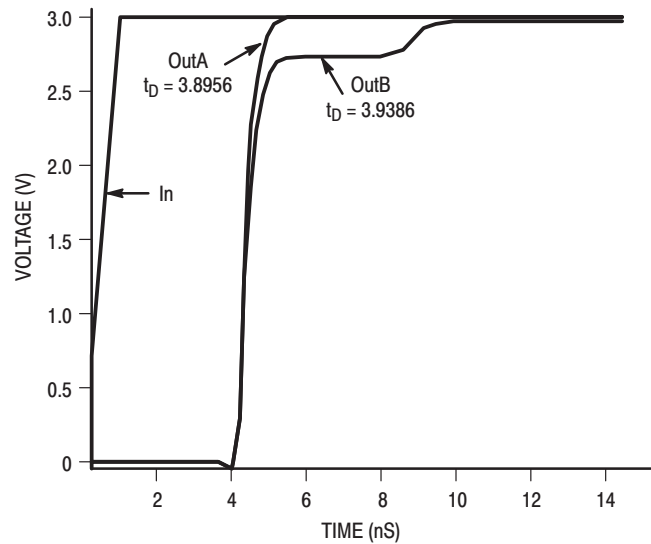


Figure 13. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 14 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

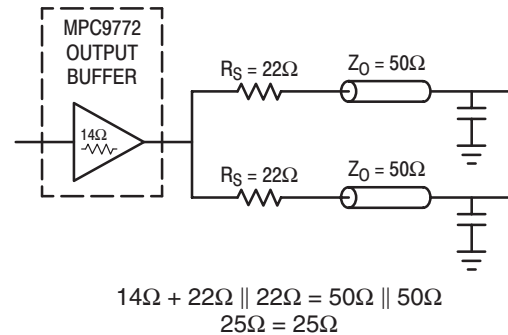


Figure 14. Optimized Dual Line Termination

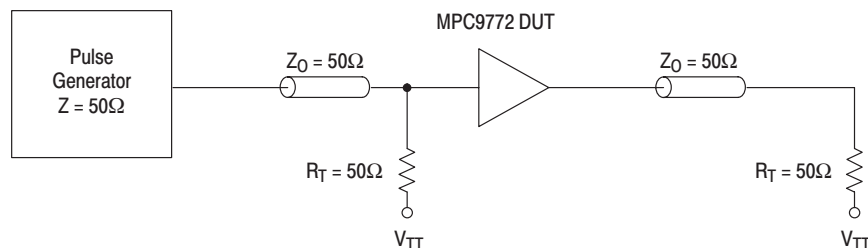
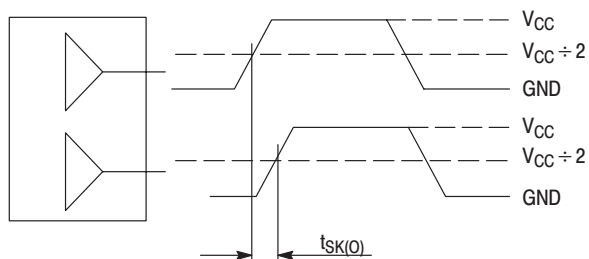
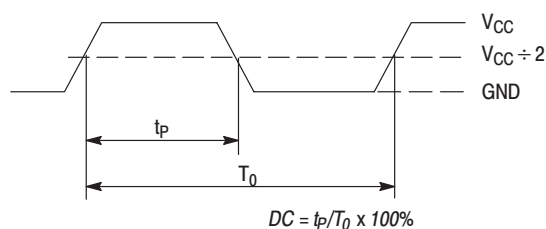


Figure 15. CCLK MPC9772 AC test reference



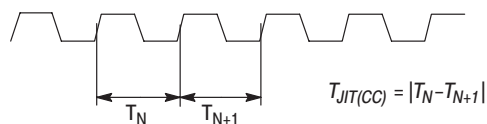
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 16. Output-to-output Skew $t_{SK(O)}$



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 18. Output Duty Cycle (DC)



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 20. Cycle-to-cycle Jitter

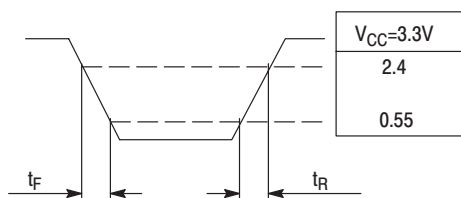


Figure 22. Output Transition Time Test Reference

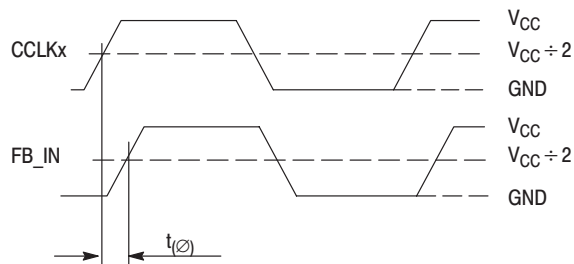
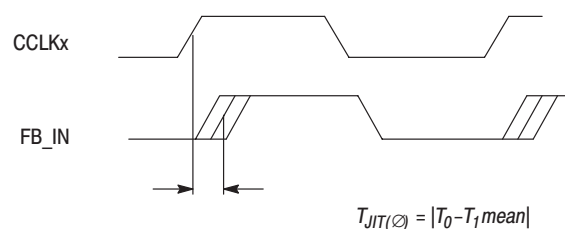
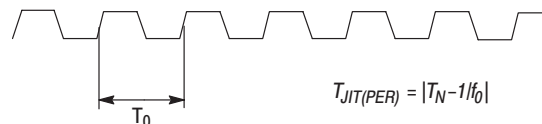


Figure 17. Propagation delay (t_{ϕ} , static phase offset) test reference



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 19. I/O Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 21. Period Jitter

2

3.3V 1:12 LVCMOS PLL Clock Generator

The MPC9773 is a 3.3V compatible, 1:12 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance networking, computing and telecom applications. With output frequencies up to 240 MHz and output skews less than 250 ps the device meets the needs of the most demanding clock applications.

Features

- 1:12 PLL based low-voltage clock generator
- 3.3V power supply
- Internal power-on reset
- Generates clock signals up to 240 MHz
- Maximum output skew of 250 ps
- Differential PECL reference clock input
- Two LVCMOS PLL reference clock inputs
- External PLL feedback supports zero-delay capability
- Various feedback and output dividers (see application section)
- Supports up to three individual generated output clock frequencies
- Synchronous output clock stop circuitry for each individual output for power down support
- Drives up to 24 clock lines
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MPC973

Functional Description

The MPC9773 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9773 requires the connection of the PLL feedback output QFB to feedback input FB_IN to close the PLL feedback path. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. The MPC9773 features an extensive level of frequency programmability between the 12 outputs as well as the output to input relationships, for instance 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 5:1, 5:2, 5:3, 5:4, 5:6, 6:1, 8:1 and 8:3.

The QSYNC output will indicate when the coincident rising edges of the above relationships will occur. The selectability of the feedback frequency is independent of the output frequencies. This allows for very flexible programming of the input reference versus output frequency relationship. The output frequencies can be either odd or even multiples of the input reference. In addition the output frequency can be less than the input frequency for applications where a frequency needs to be reduced by a non-binary factor. The MPC9773 also supports the 180° phase shift of one of its output banks with respect to the other output banks. The QSYNC outputs reflects the phase relationship between the QA and QC outputs and can be used for the generation of system baseline timing signals.

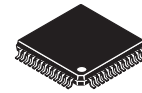
The REF_SEL pin selects the LVPECL or the LVCMOS compatible inputs as the reference clock signal. Two alternative LVCMOS compatible clock inputs are provided for clock redundancy support. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The outputs can be individually disabled (stopped in logic low state) by programming the serial CLOCK_STOP interface of the MPC9773. The MPC9773 has an internal power-on reset.

The MPC9773 is fully 3.3V compatible and requires no external loop filter components. All inputs (except PCLK) accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9773 outputs can drive one or two traces giving the devices an effective fanout of 1:24. The device is pin and function compatible to the MPC973 and is packaged in a 52-lead LQFP package.

MPC9773

**3.3V 1:12 LVCMOS
PLL CLOCK GENERATOR**



FA SUFFIX
52 LEAD LQFP PACKAGE
CASE 848D

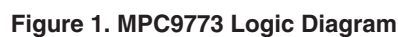


Table 1. PIN CONFIGURATION

Pin	I/O	Type	Function
CCLK0	Input	LVC MOS	PLL reference clock
CCLK1	Input	LVC MOS	Alternative PLL reference clock
PCLK, PCLK	Input	LVPECL	Differential LVPECL reference clock
FB_IN	Input	LVC MOS	PLL feedback signal input, connect to an QFB
CCLK_SEL	Input	LVC MOS	LVC MOS clock reference select
REF_SEL	Input	LVC MOS	LVC MOS/PECL reference clock select
VCO_SEL	Input	LVC MOS	VCO operating frequency select
PLL_EN	Input	LVC MOS	PLL enable/PLL bypass mode select
M $\overline{R}$ /OE	Input	LVC MOS	Output enable/disable (high-impedance tristate) and device reset
FSEL_A[0:1]	Input	LVC MOS	Frequency divider select for bank A outputs
FSEL_B[0:1]	Input	LVC MOS	Frequency divider select for bank B outputs
FSEL_C[0:1]	Input	LVC MOS	Frequency divider select for bank C outputs
FSEL_FB[0:2]	Input	LVC MOS	Frequency divider select for the QFB output
INV_CLK	Input	LVC MOS	Clock phase selection for outputs QC2 and QC3
STOP_CLK	Input	LVC MOS	Clock input for clock stop circuitry
STOP_DATA	Input	LVC MOS	Configuration data input for clock stop circuitry
QA[0-3]	Output	LVC MOS	Clock outputs (Bank A)
QB[0-3]	Output	LVC MOS	Clock outputs (Bank B)
QC[0-3]	Output	LVC MOS	Clock outputs (Bank C)
QFB	Output	LVC MOS	PLL feedback output. Connect to FB_IN.
QSYNC	Output	LVC MOS	Synchronization pulse output
GND	Supply	Ground	Negative power supply
VCC_PLL	Supply	VCC	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin VCC_PLL. Please see applications section for details.
VCC	Supply	VCC	Positive power supply for I/O and core. All VCC pins must be connected to the positive power supply for correct operation

Table 2. FUNCTION TABLE (Configuration Controls)

Control	Default	0	1
REF_SEL	1	Selects CCLKx as the PLL reference clock	Selects the LVPECL inputs as the PLL reference clock
CCLK_SEL	1	Selects CCLK0	Selects CCLK1
VCO_SEL	1	Selects VCO÷2. The VCO frequency is scaled by a factor of 2 (low VCO frequency range).	Selects VCO÷1. (high VCO frequency range)
PLL_EN	1	Test mode with the PLL bypassed. The reference clock is substituted for the internal VCO output. MPC9773 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Normal operation mode with PLL enabled.
INV_CLK	1	QC2 and QC3 are in phase with QC0 and QC1	QC2 and QC3 are inverted (180° phase shift) with respect to QC0 and QC1
M $\overline{R}$ /OE	1	Outputs disabled (high-impedance state) and device is reset. During reset/output disable the PLL feedback loop is open and the internal VCO is tied to its lowest frequency. The MPC9773 requires reset after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLKx). The device is reset by the internal power-on reset (POR) circuitry during power-up.	Outputs enabled (active)
VCO_SEL, FSEL_A[0:1], FSEL_B[0:1], FSEL_C[0:1], FSEL_FB[0:2] control the operating PLL frequency range and input/output frequency ratios. See Table 3 to Table 6 and the applications section for supported frequency ranges and output to input frequency ratios.			

Table 3. Output Divider Bank A (N_A)

VCO_SE L	FSEL_A1	FSEL_A0	QA[0:3]
0	0	0	VCO÷8
0	0	1	VCO÷12
0	1	0	VCO÷16
0	1	1	VCO÷24
1	0	0	VCO÷4
1	0	1	VCO÷6
1	1	0	VCO÷8
1	1	1	VCO÷12

Table 4. Output Divider Bank B (N_B)

VCO_SE L	FSEL_B1	FSEL_B0	QB[0:3]
0	0	0	VCO÷8
0	0	1	VCO÷12
0	1	0	VCO÷16
0	1	1	VCO÷20
1	0	0	VCO÷4
1	0	1	VCO÷6
1	1	0	VCO÷8
1	1	1	VCO÷10

Table 5. Output Divider Bank C (N_C)

VCO_SE L	FSEL_C1	FSEL_C0	QC[0:3]
0	0	0	VCO÷4
0	0	1	VCO÷8
0	1	0	VCO÷12
0	1	1	VCO÷16
1	0	0	VCO÷2
1	0	1	VCO÷4
1	1	0	VCO÷6
1	1	1	VCO÷8

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Table 6. Output Divider PLL Feedback (M)

VCO_SEL	FSEL_FB2	FSEL_FB1	FSEL_FB0	QFB
0	0	0	0	VCO÷8
0	0	0	1	VCO÷12
0	0	1	0	VCO÷16
0	0	1	1	VCO÷20
0	1	0	0	VCO÷16
0	1	0	1	VCO÷24
0	1	1	0	VCO÷32
0	1	1	1	VCO÷40
1	0	0	0	VCO÷4
1	0	0	1	VCO÷6
1	0	1	0	VCO÷8
1	0	1	1	VCO÷10
1	1	0	0	VCO÷8
1	1	0	1	VCO÷12
1	1	1	0	VCO÷16
1	1	1	1	VCO÷20

Table 7. GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		12		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 8. ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.9	V	
V_{IN}	DC Input Voltage	-0.3	$V_{CC}+0.3$	V	
V_{OUT}	DC Output Voltage	-0.3	$V_{CC}+0.3$	V	
I_{IN}	DC Input Current		± 20	mA	
I_{OUT}	DC Output Current		± 50	mA	
T_S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 9. DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{CC_PLL}	PLL Supply Voltage	3.0		V_{CC}	V	LVC MOS
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input Low Voltage			0.8	V	LVC MOS
V_{PP}	Peak-to-peak Input Voltage PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}^a	Common Mode Range PCLK, $\overline{PCLK}$	1.0		$V_{CC} - 0.6$	V	LVPECL
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -24 \text{ mA}^b$
V_{OL}	Output Low Voltage			0.55 0.30	V V	$I_{OL} = 24 \text{ mA}$ $I_{OL} = 12 \text{ mA}$
Z_{OUT}	Output Impedance		14 - 17		Ω	
I_{IN}	Input Current ^c			± 200	μA	$V_{IN} = V_{CC}$ or GND
I_{CC_PLL}	Maximum PLL Supply Current		8.0	13.5	mA	V_{CC_PLL} Pin
I_{CCQ}	Maximum Quiescent Supply Current			35	mA	All V_{CC} Pins

a. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.

b. The MPC9773 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines.

c. Inputs have pull-down resistors affecting the input current.

Table 10. AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$)^{a b}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{REF}	Input reference frequency					
	+4 feedback	50.0		120.0	MHz	PLL locked
	+6 feedback	33.3		80.0	MHz	
	+8 feedback	25.0		60.0	MHz	
	+10 feedback	20.0		48.0	MHz	
	+12 feedback	16.6		40.0	MHz	
	+16 feedback	12.5		30.0	MHz	
	+20 feedback	10.0		24.0	MHz	
	+24 feedback	8.33		20.0	MHz	
	+32 feedback	6.25		15.0	MHz	
	+40 feedback	5.00		12.0	MHz	
	Input reference frequency in PLL bypass mode			250	MHz	PLL bypass
f_{VCO}	VCO frequency range ^c	200		480	MHz	
f_{MAX}	Output Frequency					PLL locked
	+2 output	100.0		240.0	MHz	
	+4 output	50.0		120.0	MHz	
	+6 output	33.3		80.0	MHz	
	+8 output	25.0		60.0	MHz	
	+10 output	20.0		48.0	MHz	
	+12 output	16.6		40.0	MHz	
	+16 output	12.5		30.0	MHz	
	+20 output	10.0		24.0	MHz	
	+24 output	8.33		20.0	MHz	
f_{STOP_CLK}	Serial interface clock frequency			20	MHz	
V_{PP}	Peak-to-peak input voltage	PCLK, $\overline{PCLK}$	400	1000	mV	LVPECL
V_{CMR}^d	Common Mode Range	PCLK, $\overline{PCLK}$	1.2	$V_{CC}-0.9$	V	LVPECL
$t_{PW,MIN}$	Input Reference Pulse Width ^d	2.0			ns	
t_R, t_F	CCLKx Input Rise/Fall Time ^e			1.0	ns	0.8 to 2.0V
$t_{(\odot)}$	Propagation Delay (static phase offset) ^f					PLL locked
	6.25 MHz < f_{REF} < 65.0 MHz	-3		+3	°	
	65.0 MHz < f_{REF} < 125 MHz	-4		+4	°	
	$f_{REF}=50$ MHz and feedback=+8	-166		+166	ps	
$t_{SK(O)}$	Output-to-output Skew ^g					
	within QA outputs			100	ps	
	within QB outputs			100	ps	
	within QC outputs			100	ps	
	all outputs			250	ps	
DC	Output Duty Cycle ^h	(T+2) - 200	T+2	(T+2) +200	ps	
t_R, t_F	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time			8.0	ns	
$t_{PZL, LZ}$	Output Enable Time			8.0	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter ⁱ		150	200	ps	
$t_{JIT(PER)}$	Period Jitter ^j			150	ps	
$t_{JIT(\odot)}$	I/O Phase Jitter RMS (1 σ) ^k					(VCO=400 MHz)
	+4 feedback			11	ps	
	+6 feedback			86	ps	
	+8 feedback			13	ps	
	+10 feedback			88	ps	
	+12 feedback			16	ps	
	+16 feedback			19	ps	
	+20 feedback			21	ps	
	+24 feedback			22	ps	
	+32 feedback			27	ps	
	+40 feedback			30	ps	

Table 10. AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^{\circ}C$ to $70^{\circ}C$)^{a b}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
BW	PLL closed loop bandwidth ^l					
	+4 feedback		1.20 - 3.50		MHz	
	+6 feedback		0.70 - 2.50		MHz	
	+8 feedback		0.50 - 1.80		MHz	
	+10 feedback		0.45 - 1.20		MHz	
	+12 feedback		0.30 - 1.00		MHz	
	+16 feedback		0.25 - 0.70		MHz	
	+20 feedback		0.20 - 0.55		MHz	
	+24 feedback		0.17 - 0.40		MHz	
	+32 feedback		0.12 - 0.30		MHz	
	+40 feedback		0.11 - 0.28		MHz	
t _{LOCK}	Maximum PLL Lock Time			10	ms	

a AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b The input reference frequency must match the VCO lock range divided by the feedback divider ratio: $f_{REF} = f_{VCO} \div (M \cdot VCO\_SEL)$.

c V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\phi)}$.

d Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF,MAX} = 100\% - DC_{REF,MIN}$.

e The MPC9773 will operate with input rise/fall times up to 3.0 ns, but the A.C. characteristics, specifically $t_{(\phi)}$, $t_{PW,MIN}$, DC and f_{MAX} can only be guaranteed if t_R , t_F are within the specified range.

f CCLKx or PCLK to FB_IN. Static phase offset depends on the reference frequency. $t_{(\phi)} [s] = t_{(\phi)} [^{\circ}] \div (f_{REF} \cdot 360^{\circ})$.

g Excluding QSYNC output. See application section for part-to-part skew calculation.

h Output duty cycle is $DC = (0.5 \pm 200 \text{ ps} \cdot f_{OUT}) \cdot 100\%$. E.g. the DC range at $f_{OUT}=100\text{MHz}$ is $48\% < DC < 52\%$. T = output period.

i Cycle jitter is valid for all outputs in the same divider configuration. See application section for more details.

j Period jitter is valid for all outputs in the same divider configuration. See application section for more details.

k I/O jitter is valid for a VCO frequency of 400 MHz. See application section for I/O jitter vs. VCO frequency.

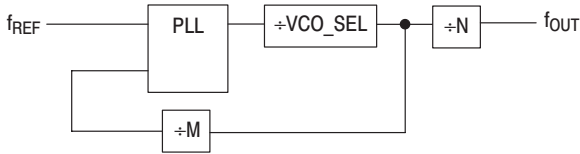
l -3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

MPC9773 Configurations

Configuring the MPC9773 amounts to properly configuring the internal dividers to produce the desired output frequencies. The output frequency can be represented by this formula:

$$f_{OUT} = f_{REF} \cdot M \div N$$



where f_{REF} is the reference frequency of the selected input clock source (CCLK0, CCLK1 or PCLK), M is the PLL feedback divider and N is a output divider. The PLL feedback divider is configured by the FSEL_FB[2:0] and the output dividers are individually configured for each output bank by the FSEL_A[1:0], FSEL_B[1:0] and FSEL_C[1:0] inputs.

The reference frequency f_{REF} and the selection of the feedback-divider M is limited by the specified VCO frequency range. f_{REF} and M must be configured to match the VCO frequency range of 200 to 480 MHz in order to achieve stable PLL operation:

$$f_{VCO,MIN} \leq (f_{REF} \cdot VCO\_SEL \cdot M) \leq f_{VCO,MAX}$$

The PLL post-divider VCO_SEL is either a divide-by-one or a divide-by-two and can be used to situate the VCO into the specified frequency range. This divider is controlled by the

VCO_SEL pin. VCO_SEL effectively extends the usable input frequency range while it has no effect on the output to reference frequency ratio.

The output frequency for each bank can be derived from the VCO frequency and output divider:

$$f_{QA[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_A)$$

$$f_{QB[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_B)$$

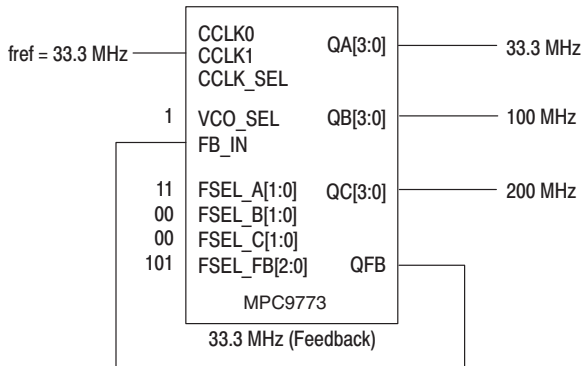
$$f_{QC[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_C)$$

Table 11. MPC9773 Divider

Divider	Function	VCO_SEL	Values
M	PLL feedback FSEL_FB[0:3]	÷1	4, 6, 8, 10, 12, 16
		÷2	8, 12, 16, 20, 24, 32, 40
N _A	Bank A Output Divider FSEL_A[0:1]	÷1	4, 6, 8, 12
		÷2	8, 12, 16, 24
N _B	Bank B Output Divider FSEL_B[0:1]	÷1	4, 6, 8, 10
		÷2	8, 12, 16, 20
N _C	Bank C Output Divider FSEL_C[0:1]	÷1	2, 4, 6, 8
		÷2	4, 8, 12, 16

Table 11 shows the various PLL feedback and output dividers and Figure 3 and Figure 4 display example configurations for the MPC9773:

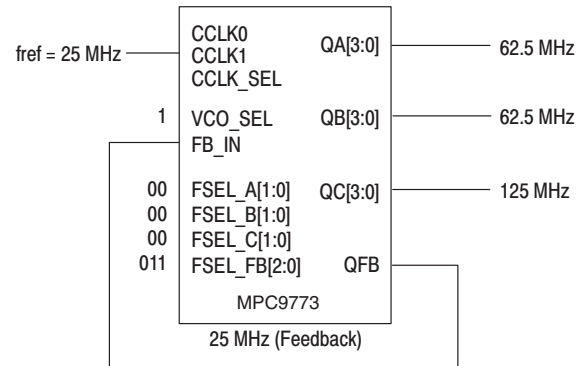
Figure 3. Example Configuration



MPC9773 example configuration (feedback of QFB = 33.3 MHz, f_{VCO} =400 MHz, VCO_SEL=÷1, M=12, N_A=12, N_B=4, N_C=2).

Frequency range	Min	Max
Input	16.6 MHz	40 MHz
QA outputs	16.6 MHz	40 MHz
QB outputs	50 MHz	120 MHz
QC outputs	100 MHz	240 MHz

Figure 4. Example Configuration



MPC9773 example configuration (feedback of QFB = 25 MHz, f_{VCO} =250 MHz, VCO_SEL=÷1, M=10, N_A=4, N_B=4, N_C=2).

Frequency range	Min	Max
Input	20 MHz	48 MHz
QA outputs	50 MHz	120 MHz
QB outputs	50 MHz	120 MHz
QC outputs	100 MHz	240 MHz

MPC9773 Individual Output Disable (Clock Stop) Circuitry

The individual clock stop (output enable) control of the MPC9773 allows designers, under software control, to implement power management into the clock distribution design. A simple serial interface and a clock stop control logic provides a mechanism through which the MPC9773 clock outputs can be individually stopped in the logic '0' state: The clock stop mechanism allows serial loading of a 12-bit serial input register. This register contains one programmable clock stop bit for 12 of the 14 output clocks. The QC0 and QFB outputs cannot be stopped (disabled) with the serial port.

The user can program an output clock to stop (disable) by

writing logic '0' to the respective stop enable bit. Likewise, the user may programmably enable an output clock by writing logic '1' to the respective enable bit. The clock stop logic enables or disables clock outputs during the time when the output would be in normally in logic low state, eliminating the possibility of short or 'runt' clock pulses.

The user can write to the serial input register through the STOP_DATA input by supplying a logic '0' start bit followed serially by 12 NRZ disable/enable bits. The period of each STOP_DATA bit equals the period of the free-running STOP_CLK signal. The STOP_DATA serial transmission should be timed so the MPC9773 can sample each STOP_DATA bit with the rising edge of the free-running STOP_CLK signal. (see Figure 5)



Figure 5. Clock Stop Circuit Programming

SYNC Output Description

The MPC9773 has a system synchronization pulse output QSYNC. In configurations with the output frequency relationships are not integer multiples of each other QSYNC provides a signal for system synchronization purposes. The MPC9773 monitors the relationship between the A bank and the B bank of outputs. The QSYNC output is asserted (logic low) one period

in duration and one period prior to the coincident rising edges of the QA and QC outputs. The duration and the placement of the pulse is dependent QA and QC output frequencies: the QSYNC pulse width is equal to the period of the higher of the QA and QC output frequencies. Figure 6 shows various waveforms for the QSYNC output. The QSYNC output is defined for all possible combinations of the bank A and bank C outputs.

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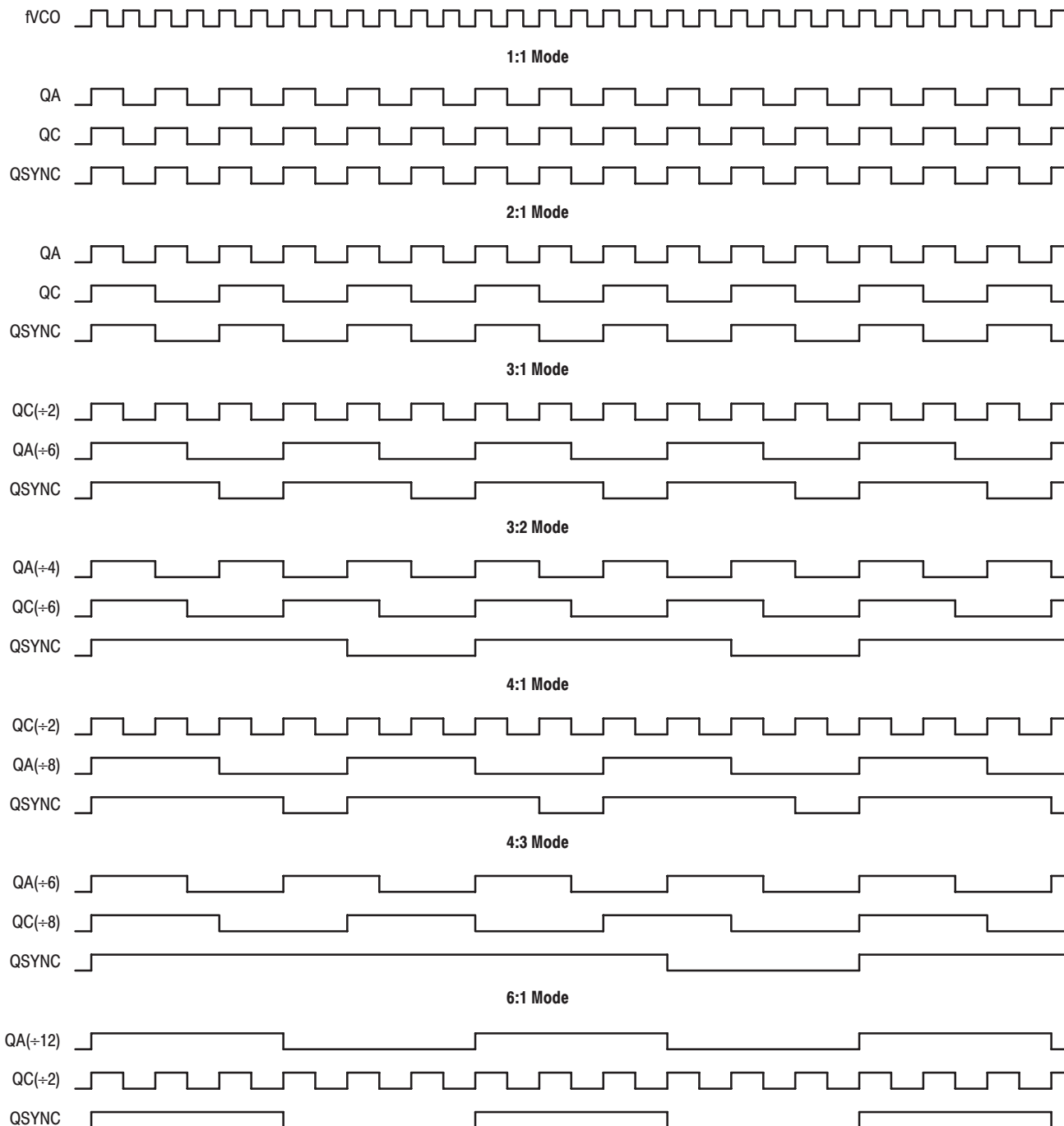


Figure 6. QSYNC Timing Diagram

Power Supply Filtering

The MPC9773 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC9773 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CC_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA_PLL} pin for the MPC9773. Figure 7 illustrates a typical power supply filter scheme. The MPC9773 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F . From the data sheet the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 8 mA (13.5 mA maximum), assuming that a minimum of 3.0V must be maintained on the V_{CC_PLL} pin. The resistor R_F shown in Figure 7 “ V_{CC_PLL} Power Supply Filter” must have a resistance of 5-10 Ω to meet the voltage drop criteria.

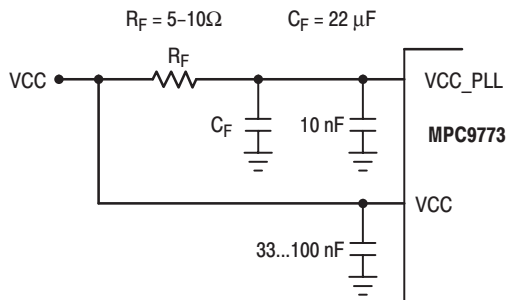


Figure 7. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 7 “ V_{CC_PLL} Power Supply Filter”, the filter cut-off frequency is around 4.5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9773 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9773 in zero-delay applications

Nested clock trees are typical applications for the MPC9773. Designs using the MPC9773 as LVCMOS PLL fan-out buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fan-out buffers. The external feedback option of the MPC9773 clock driver allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device (the propagation delay through the device is virtually eliminated). The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of part-to-part skew

The MPC9773 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9773 are connected together, the maximum overall timing uncertainty from the common CCLKx input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD, LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

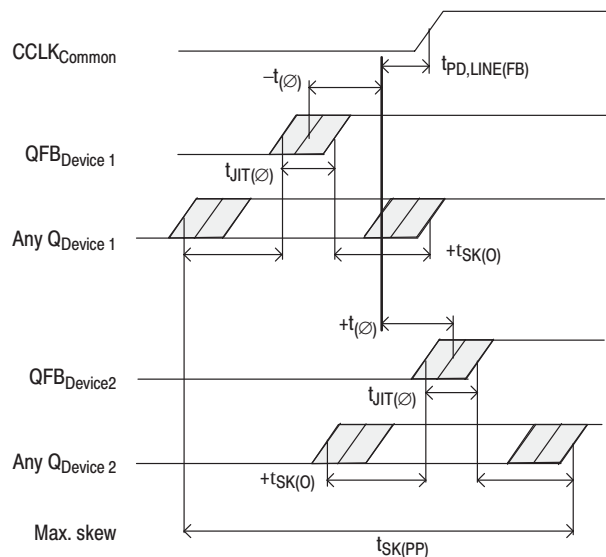


Figure 8. MPC9773 max. device-to-device skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 12.

Table 12. Confidence Factor CF

CF	Probability of clock edge within the distribution
$\pm 1\sigma$	0.68268948
$\pm 2\sigma$	0.95449988
$\pm 3\sigma$	0.99730007
$\pm 4\sigma$	0.99993663
$\pm 5\sigma$	0.99999943
$\pm 6\sigma$	0.99999999

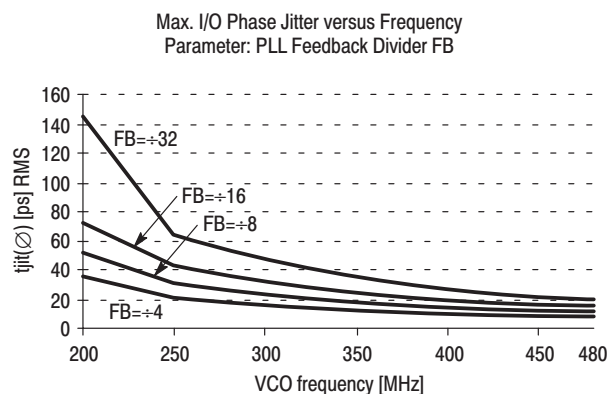
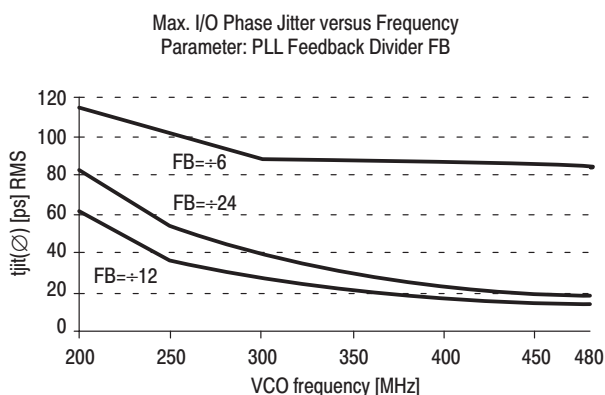
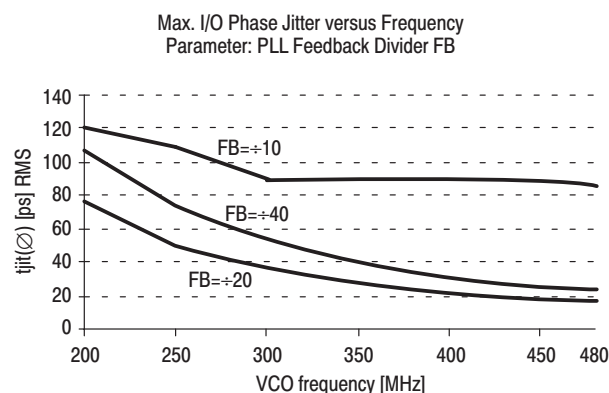
The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device.

Due to the frequency dependence of the static phase offset and I/O jitter, using Figure 9 to Figure 11 to predict a maximum I/O jitter and the specified $t_{j(\phi)}$ parameter relative to the input reference frequency results in a precise timing performance analysis.

In the following example calculation an I/O jitter confidence factor of 99.7% ($\pm 3\sigma$) is assumed, resulting in a worst case timing uncertainty from the common input reference clock to any output of -455 ps to +455 ps relative to CCLK (PLL feedback = +8, reference frequency = 50 MHz, VCO frequency = 400 MHz, I/O jitter = 13 ps rms max., static phase offset $t_{j(\phi)}$ = ± 166 ps):

$$t_{SK(PP)} = [-166ps...166ps] + [-250ps...250ps] + [(13ps \cdot -3)...(13ps \cdot 3)] + t_{PD, LINE(FB)}$$

$$t_{SK(PP)} = [-455ps...455ps] + t_{PD, LINE(FB)}$$

**Figure 9. MPC9772 I/O Jitter****Figure 10. MPC9772 I/O Jitter****Figure 11. MPC9772 I/O Jitter**

Driving Transmission Lines

The MPC9773 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}+2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9773 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 12 "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9773 clock driver is effectively doubled due to its capability to drive multiple lines.

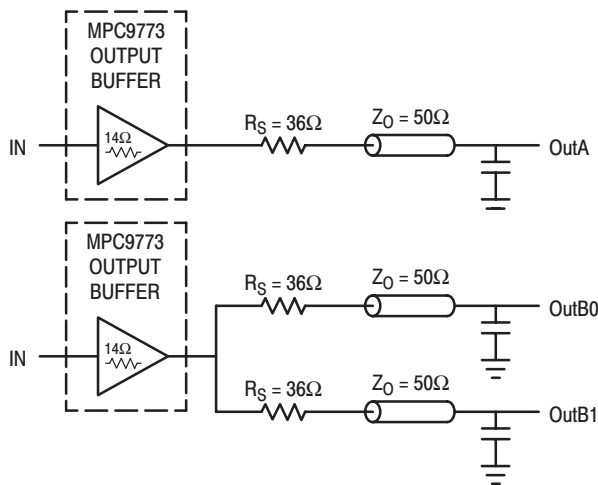


Figure 12. Single versus Dual Transmission Lines

The waveform plots in Figure 13 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9773 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9773. The output waveform in Figure 13 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned}
 V_L &= V_S (Z_0 \div (R_S + R_0 + Z_0)) \\
 Z_0 &= 50\Omega \parallel 50\Omega \\
 R_S &= 36\Omega \parallel 36\Omega \\
 R_0 &= 14\Omega \\
 V_L &= 3.0 (25 \div (18 + 17 + 25)) \\
 &= 1.31V
 \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

1. Final skew data pending specification.

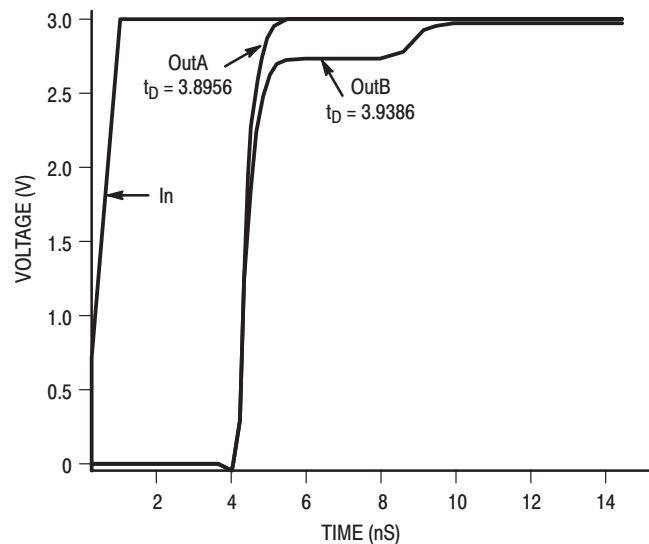


Figure 13. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 14 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

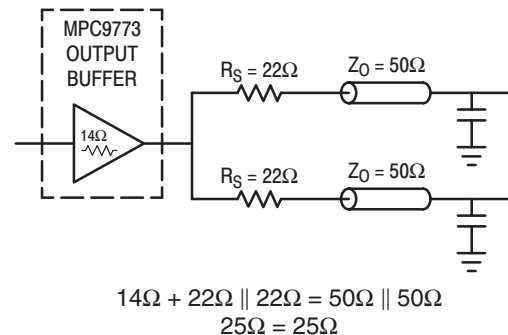


Figure 14. Optimized Dual Line Termination

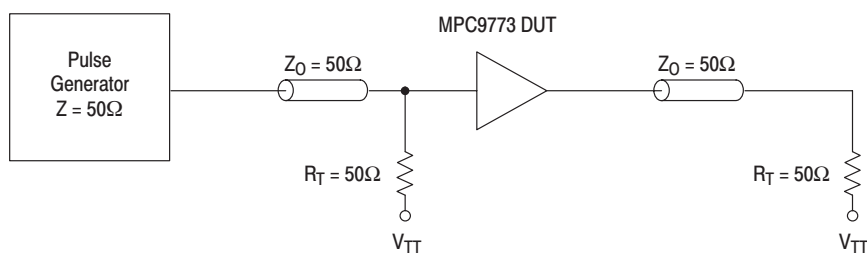


Figure 15. CCLK MPC9773 AC test reference

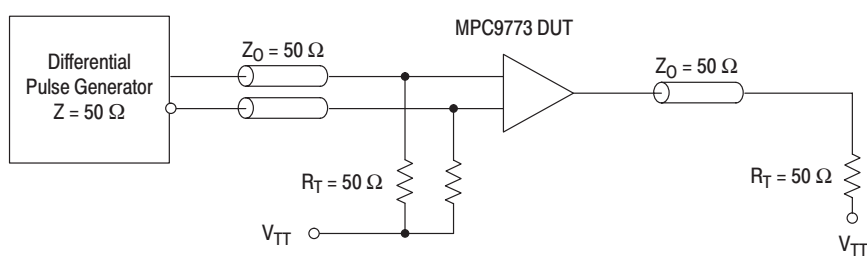
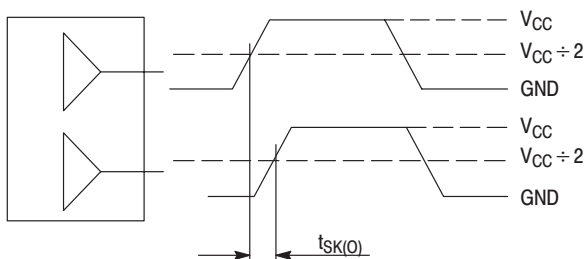
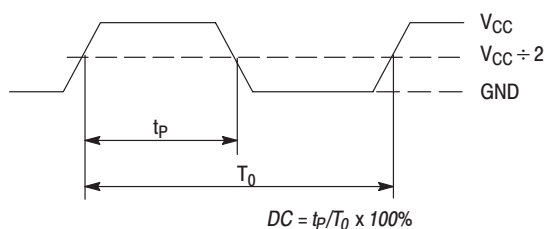


Figure 16. PCLK MPC9773 AC test reference



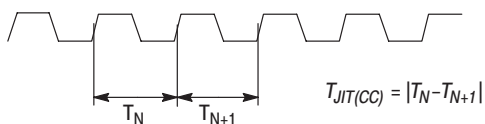
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 17. Output-to-output Skew $t_{SK(O)}$



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 19. Output Duty Cycle (DC)



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 21. Cycle-to-cycle Jitter

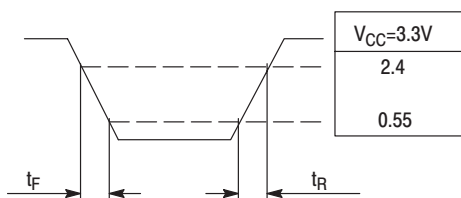


Figure 23. Output Transition Time Test Reference

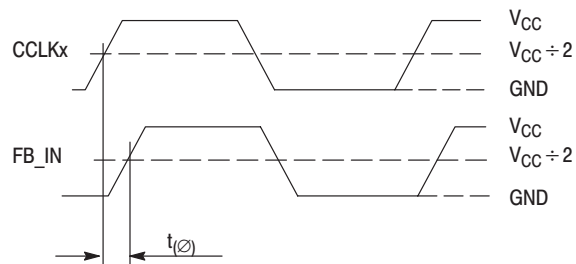
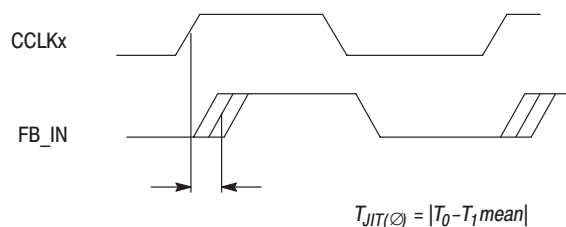
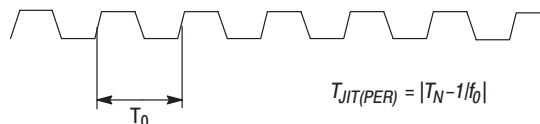


Figure 18. Propagation delay (t_{ϕ} , static phase offset) test reference



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 20. I/O Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 22. Period Jitter

3.3V 1:14 LVCMOS PLL Clock Generator

The MPC9774 is a 3.3V compatible, 1:14 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance networking, computing and telecom applications. With output frequencies up to 125 MHz and output skews less than 175 ps the device meets the needs of the most demanding clock applications.

Features

- 1:14 PLL based low-voltage clock generator
- 3.3V power supply
- Internal power-on reset
- Generates clock signals up to 125 MHz
- Maximum output skew of 175 ps
- Two LVCMOS PLL reference clock inputs
- External PLL feedback supports zero-delay capability
- Various feedback and output dividers (see application section)
- Supports up to three individual generated output clock frequencies
- Drives up to 28 clock lines
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MPC974

Functional Description

The MPC9774 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9774 requires the connection of the PLL feedback output QFB to feedback input FB_IN to close the PLL feedback path. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range.

The MPC9774 features frequency programmability between the three output banks outputs as well as the output to input relationships. Output frequency ratios of 1:1, 2:1, 3:1, 3:2 and 3:2:1 can be realized. Additionally, the device supports a separate configurable feedback output which allows for a wide variety of input/output frequency multiplication alternatives. The VCO_SEL pin provides an extended PLL input reference frequency range.

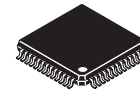
The REF_SEL pin selects the internal crystal oscillator or the LVCMOS compatible inputs as the reference clock signal. Two alternative LVCMOS compatible clock inputs are provided for clock redundancy support. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The MPC9774 has an internal power-on reset.

The MPC9774 is fully 3.3V compatible and requires no external loop filter components. All inputs (except XTAL) accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9774 outputs can drive one or two traces giving the devices an effective fanout of 1:12. The device is pin and function compatible to the MPC974 and is packaged in a 52-lead LQFP package.

MPC9774

**3.3V 1:14 LVCMOS
PLL CLOCK GENERATOR**



FA SUFFIX
52 LEAD LQFP PACKAGE
CASE 848D

2

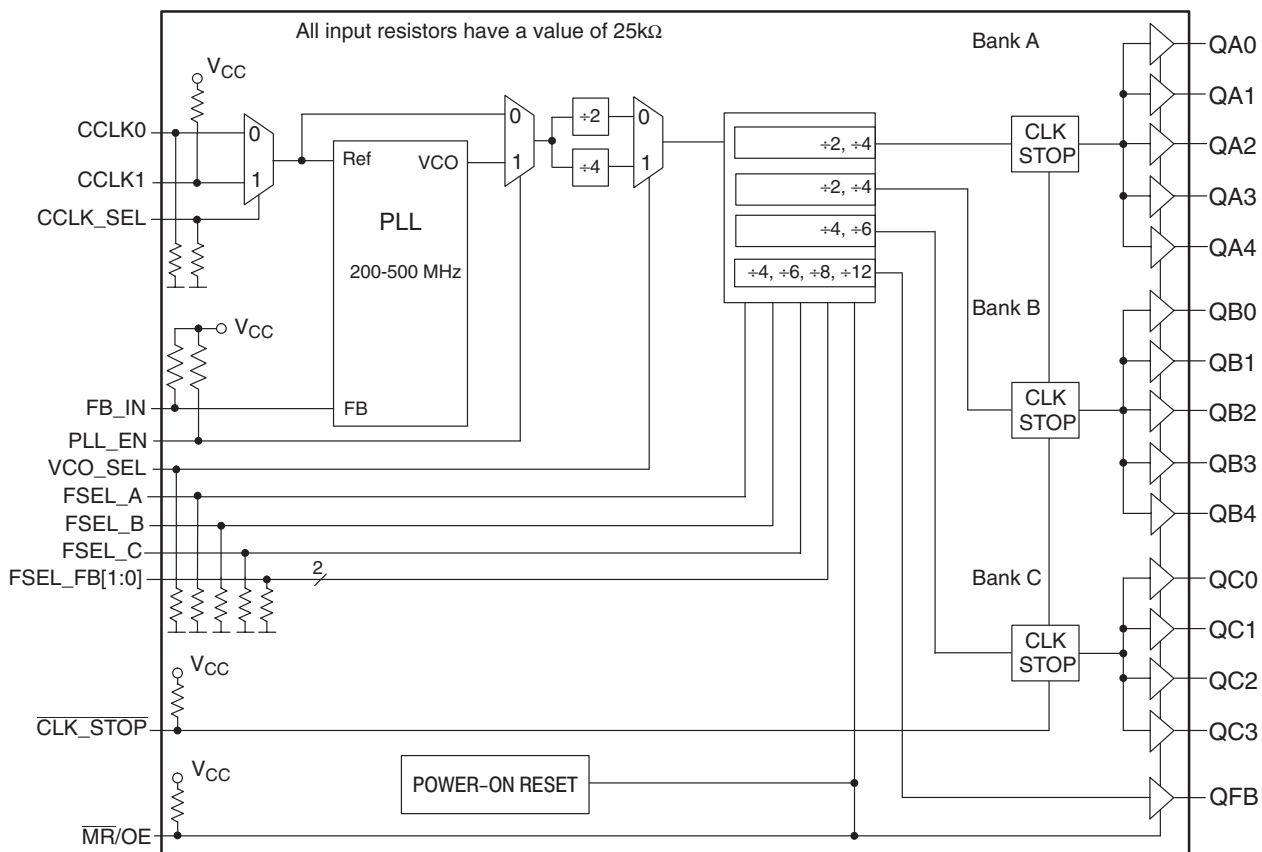


Figure 1. MPC9774 Logic Diagram

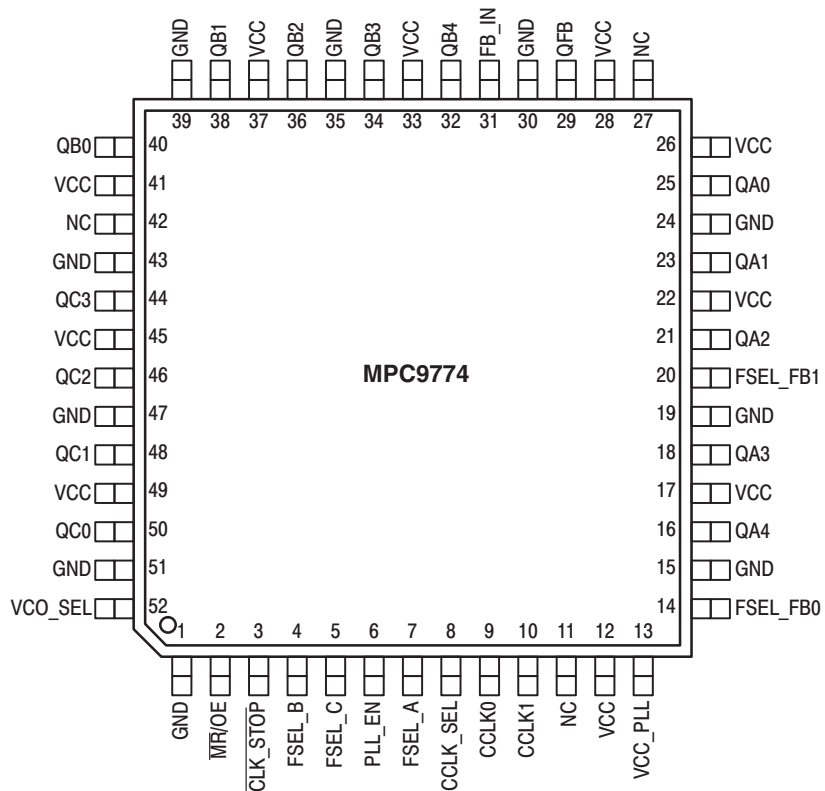


Figure 2. MPC9774 52-Lead Package Pinout (Top View)

Table 1. PIN CONFIGURATION

Pin	I/O	Type	Function
CCLK0	Input	LVC MOS	PLL reference clock
CCLK1	Input	LVC MOS	Alternative PLL reference clock
FB_IN	Input	LVC MOS	PLL feedback signal input, connect to QFB
CCLK_SEL	Input	LVC MOS	LVC MOS clock reference select
VCO_SEL	Input	LVC MOS	VCO operating frequency select
PLL_EN	Input	LVC MOS	PLL enable/PLL bypass mode select
MR/OE	Input	LVC MOS	Output enable/disable (high-impedance tristate) and device reset
CLK_STOP	Input	LVC MOS	Output enable/clock stop (logic low state)
FSEL_A	Input	LVC MOS	Frequency divider select for bank A outputs
FSEL_B	Input	LVC MOS	Frequency divider select for bank B outputs
FSEL_C	Input	LVC MOS	Frequency divider select for bank C outputs
FSEL_FB[1:0]	Input	LVC MOS	Frequency divider select for the QFB output
QA[4:0]	Output	LVC MOS	Clock outputs (Bank A)
QB[4:0]	Output	LVC MOS	Clock outputs (Bank B)
QC[3:0]	Output	LVC MOS	Clock outputs (Bank C)
QFB	Output	LVC MOS	PLL feedback output. Connect to FB_IN.
GND	Supply	Ground	Negative power supply
VCC_PLL	Supply	V _{CC}	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V _{CC_PLL} . Please see applications section for details.
VCC	Supply	V _{CC}	Positive power supply for I/O and core. All V _{CC} pins must be connected to the positive power supply for correct operation

Table 2. Function Table (MPC9774 configuration controls)

Control	Default	0	1
CCLK_SEL	0	Selects CCLK0 as PLL reference signal input	Selects CCLK1 as PLL reference signal input
VCO_SEL	0	Selects VCO ÷ 2. The VCO frequency is scaled by a factor of 2 (high input frequency range)	Selects VCO ÷ 4. The VCO frequency is scaled by a factor of 4 (low input frequency range).
PLL_EN	1	Test mode with the PLL bypassed. The reference clock is substituted for the internal VCO output. MPC9774 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Normal operation mode with PLL enabled.
CLK_STOP	1	QA, QB and QC outputs disabled in logic low state. QFB is not affected by CLK_STOP. CLK_STOP deassertion may cause the initial output clock pulse to be distorted.	Outputs enabled (active)
MR/OE	1	Outputs disabled (high-impedance state) and reset of the device. During reset/output disable the PLL feedback loop is open and the internal VCO is tied to its lowest frequency. The MPC9774 requires reset after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLKx). The device is reset by the internal power-on reset (POR) circuitry during power-up.	Outputs enabled (active)
VCO_SEL, FSEL_A, FSEL_B, FSEL_C and FSEL_FB[1:0] control the operating PLL frequency range and input/output frequency ratios. See Table 3 and Table 4 for the device frequency configuration.			

Table 3. Function Table (Output Dividers Bank A, B, and C)

VCO_SEL	FSEL_A	QA[4:0]	VCO_SEL	FSEL_B	QB[4:0]	VCO_SEL	FSEL_C	QC[3:0]
0	0	VCO ÷ 4	0	0	VCO ÷ 4	0	0	VCO ÷ 8
0	1	VCO ÷ 8	0	1	VCO ÷ 8	0	1	VCO ÷ 12
1	0	VCO ÷ 8	1	0	VCO ÷ 8	1	0	VCO ÷ 16
1	1	VCO ÷ 16	1	1	VCO ÷ 16	1	1	VCO ÷ 24

Table 4. Function Table (QFB)

VCO_SEL	FSEL_B1	FSEL_B0	QFB
0	0	0	VCO ÷ 8
0	0	1	VCO ÷ 16
0	1	0	VCO ÷ 12
0	1	1	VCO ÷ 24
1	0	0	VCO ÷ 16
1	0	1	VCO ÷ 32
1	1	0	VCO ÷ 24
1	1	1	VCO ÷ 48

Table 5. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output Termination Voltage		V _{CC} ÷ 2		V	
MM	ESD protection (Machine Model)	200			V	
HBM	ESD protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C _{PD}	Power Dissipation Capacitance		12		pF	Per output
C _{IN}	Input Capacitance		4.0		pF	Inputs

Table 6. Absolute Maximum Ratings^a

Symbol	Characteristics	Min	Max	Unit	Condition ⁵
V _{CC}	Supply Voltage	-0.3	3.9	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} + 0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} + 0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 7. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0°C to +70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{CC_PLL}	PLL Supply Voltage	3.02		V _{CC}	V	LVC MOS
V _{IH}	Input High Voltage	2.0		V _{CC} + 0.3	V	LVC MOS
V _{IL}	Input Low Voltage			0.8	V	LVC MOS
V _{OH}	Output High Voltage	2.4			V	I _{OH} = -24 mA ^a
V _{OL}	Output Low Voltage			0.55 0.30	V V	I _{OL} = 24 mA I _{OL} = 12 mA
Z _{OUT}	Output Impedance		14 - 17		Ω	
I _{IN}	Input Current ^b			±200	μA	V _{IN} = V _{CC} or GND
I _{CC_PLL}	Maximum PLL Supply Current		5.0	7.5	mA	V _{CC_PLL} Pin
I _{CCQ}	Maximum Quiescent Supply Current			8.0	mA	All V _{CC} Pins

a. The MPC9774 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

b. Inputs have pull-down or pull-up resistors affecting the input current.

Table 8. AC Characteristics ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{REF}	Input Reference Frequency					
	+8 feedback	25.0		62.5	MHz	PLL locked
	+12 feedback	16.6		41.6	MHz	
	+16 feedback	12.5		31.25	MHz	
	+24 feedback	8.33		20.83	MHz	
	+32 feedback	6.25		15.625	MHz	
	+48 feedback	4.16		10.41	MHz	
	Input Reference Frequency in PLL Bypass Mode ^b			250	MHz	PLL bypass
f_{VCO}	VCO Frequency Range ^c	200		500	MHz	
f_{MAX}	Output Frequency					PLL locked
	+4 output	50.0		125.0	MHz	
	+8 output	25.0		62.5	MHz	
	+12 output	16.6		41.6	MHz	
	+16 output	12.5		31.25	MHz	
	+24 output	8.33		20.83	MHz	
$t_{PW,MIN}$	Input Reference Pulse Width ^d	2.0			ns	
t_R, t_F	CCLKx Input Rise/Fall Time			1.0	ns	0.8 to 2.0V
$t_{(\phi)}$	Propagation Delay (static phase offset) ^e CCLKx to FB_IN (FB=+8 and $f_{REF}=50$ MHz)	-250		+100	ps	PLL locked
$t_{SK(O)}$	Output-to-output Skew ^f					
	within QA bank			100	ps	
	within QB bank			125	ps	
	within QC bank			100	ps	
	any output			175	ps	
DC	Output Duty Cycle	47	50	53	%	
t_R, t_F	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
t_{PZL}	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle Jitter ^g			90	ps	
$t_{JIT(PER)}$	Period Jitter ^f			90	ps	
$t_{JIT(\phi)}$	I/O Phase Jitter RMS (1 σ) ^h					
	FB=+8			15	ps	
	FB=+12			49	ps	
	FB=+16			18	ps	
	FB=+24			22	ps	
	FB=+32			26	ps	
	FB=+48			34	ps	
BW	PLL Closed Loop Bandwidth ⁱ					
	FB=+8		0.50 - 1.80		MHz	
	FB=+12		0.30 - 1.00		MHz	
	FB=+16		0.25 - 0.70		MHz	
	FB=+24		0.17 - 0.40		MHz	
	FB=+32		0.12 - 0.30		MHz	
	FB=+48		0.07 - 0.20		MHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

a AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b In bypass mode, the MPC9774 divides the input reference clock.

c The input reference frequency must match the VCO lock range divided by the total feedback divider ratio (FB): $f_{REF}=f_{VCO}/(M \cdot VCO\_SEL)$.

d Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF,MAX} = 100\% - DC_{REF,MIN}$. E.g. at $f_{REF}=62.5$ MHz the input duty cycle range is $12.5\% < DC < 87.5\%$.

e Static phase offset depends on the reference frequency: $t_{(\phi)} = +50 \text{ ps} \pm (1/(120 \cdot f_{REF}))$ for any reference frequency.

f See application section for part-to-part skew calculation.

g Valid for all outputs at the same frequency.

h I/O jitter for $f_{VCO}=400$ MHz. See application section for I/O jitter at other frequencies and for a jitter calculation for confidence factors other than 1 σ .

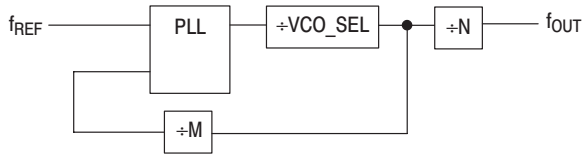
i -3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

MPC9774 Configurations

Configuring the MPC9774 amounts to properly configuring the internal dividers to produce the desired output frequencies. The output frequency can be represented by this formula:

$$f_{OUT} = f_{REF} \cdot M \div N$$



where f_{REF} is the reference frequency of the selected input clock source (CCLK0 or CCLK1), M is the PLL feedback divider and N is a output divider. M is configured by the FSEL_FB[0:1] and N is individually configured for each output bank by the FSEL_A, FSEL_B and FSEL_C inputs.

The reference frequency f_{REF} and the selection of the feedback-divider M is limited by the specified VCO frequency range. f_{REF} and M must be configured to match the VCO frequency range of 200 to 500 MHz in order to achieve stable PLL operation:

$$f_{VCO,MIN} \leq (f_{REF} \cdot VCO\_SEL \cdot M) \leq f_{VCO,MAX}$$

The PLL post-divider VCO_SEL is either a divide-by-two or a divide-by-four and can be used to situate the VCO into the

specified frequency range. This divider is controlled by the VCO_SEL pin. VCO_SEL effectively extends the usable input frequency range while it has no effect on the output to reference frequency ratio. The output frequency for each bank can be derived from the VCO frequency and the output divider:

$$f_{QA[4:0]} = f_{VCO} \div (VCO\_SEL \cdot N_A)$$

$$f_{QB[4:0]} = f_{VCO} \div (VCO\_SEL \cdot N_B)$$

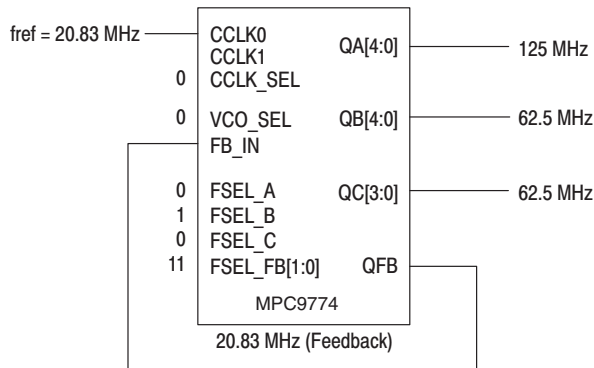
$$f_{QC[3:0]} = f_{VCO} \div (VCO\_SEL \cdot N_C)$$

Table 9. MPC9774 Divider

Divider	Function	VCO_SEL	Values
M	PLL feedback FSEL_FB[0:1]	÷2	8, 12, 16, 24
		÷4	16, 24, 32, 48
N _A	Bank A Output Divider FSEL_A	÷2	4, 8
		÷4	8, 16
N _B	Bank B Output Divider FSEL_B	÷2	4, 8
		÷4	8, 16
N _C	Bank C Output Divider FSEL_C	÷2	8, 12
		÷4	16, 24

Table 9 shows the various PLL feedback and output dividers. The output dividers for the three output banks allow the user to configure the outputs into 1:1, 2:1, 3:2 and 3:2:1 frequency ratios. Figure 3 and Figure 4 display example configurations for the MPC9774:

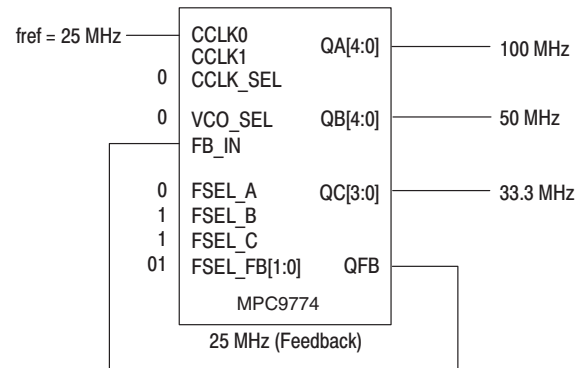
Figure 3. Example Configuration



MPC9774 example configuration (feedback of QFB = 20.83 MHz, VCO_SEL = ÷2, M = 12, N_A = 2, N_B = 4, N_C = 4, f_{VCO} = 500 MHz).

Frequency range	Min	Max
Input	8.33 MHz	20.83 MHz
QA outputs	50 MHz	125 MHz
QB outputs	25 MHz	62.5 MHz
QC outputs	25 MHz	62.5 MHz

Figure 4. Example Configuration



MPC9774 example configuration (feedback of QFB = 25 MHz, VCO_SEL = ÷2, M = 8, N_A = 2, N_B = 4, N_C = 6, f_{VCO} = 400 MHz).

Frequency range	Min	Max
Input	20 MHz	48 MHz
QA outputs	50 MHz	120 MHz
QB outputs	50 MHz	120 MHz
QC outputs	100 MHz	200 MHz

Using the MPC9774 in zero-delay applications

Nested clock trees are typical applications for the MPC9774. Designs using the MPC9774 as LVCMOS PLL fan-out buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fan-out buffers. The external feedback of the MPC9774 clock driver allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device (the propagation delay through the device is virtually eliminated). The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of part-to-part skew

The MPC9774 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9774 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD, LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

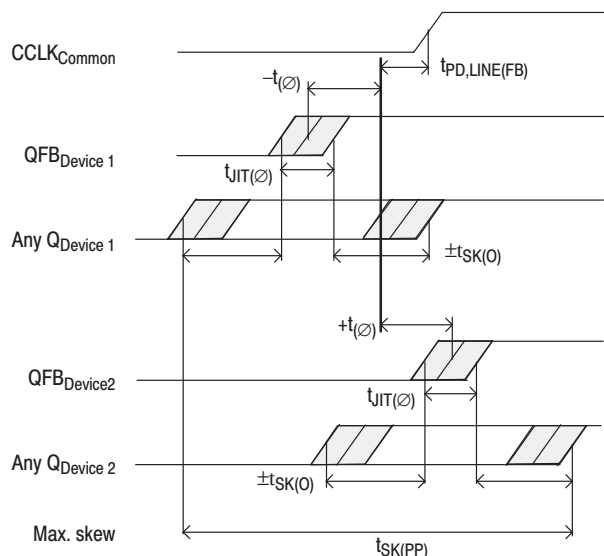


Figure 5. MPC9774 max. device-to-device skew

Due to the statistical nature of I/O jitter a rms value (1σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 10.

Table 10. Confidence factor CF

CF	Probability of clock edge within the distribution
$\pm 1\sigma$	0.68268948
$\pm 2\sigma$	0.95449988
$\pm 3\sigma$	0.99730007
$\pm 4\sigma$	0.99993663
$\pm 5\sigma$	0.99999943
$\pm 6\sigma$	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device.

Due to the frequency dependence of the static phase offset and I/O jitter, using Figure 6 and Figure 7 to predict a maximum I/O jitter and the specified $t_{(\varnothing)}$ parameter relative to the input reference frequency results in a precise timing performance analysis.

In the following example calculation a I/O jitter confidence factor of 99.7% ($\pm 3\sigma$) is assumed, resulting in a worst case timing uncertainty from the common input reference clock to any output of -470 ps to +320 ps relative to CCLK (PLL feedback = $\div 8$, reference frequency = 50 MHz, VCO frequency = 400 MHz, I/O jitter = 15 ps rms max., static phase offset $t_{(\varnothing)} = -250$ ps to +100 ps):

$$t_{SK(PP)} = [-250 \text{ ps} \dots +100 \text{ ps}] + [-175 \text{ ps} \dots 175 \text{ ps}] + [(15 \text{ ps} \cdot -3) \dots (15 \text{ ps} \cdot 3)] + t_{PD, LINE(FB)}$$

$$t_{SK(PP)} = [-470 \text{ ps} \dots +320 \text{ ps}] + t_{PD, LINE(FB)}$$

Max. I/O Phase Jitter (RMS) versus Frequency
Parameter: PLL Feedback Divider FB

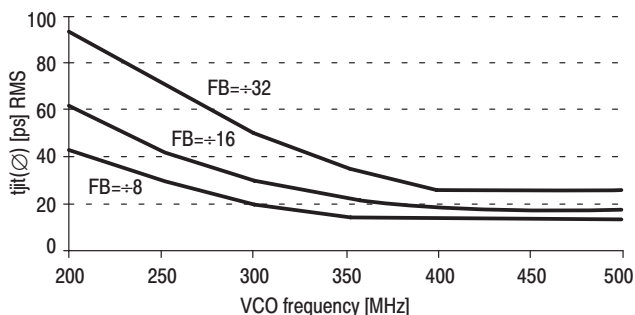


Figure 6. MPC9774 I/O Jitter

Max. I/O Phase Jitter (RMS) versus Frequency
Parameter: PLL Feedback Divider FB

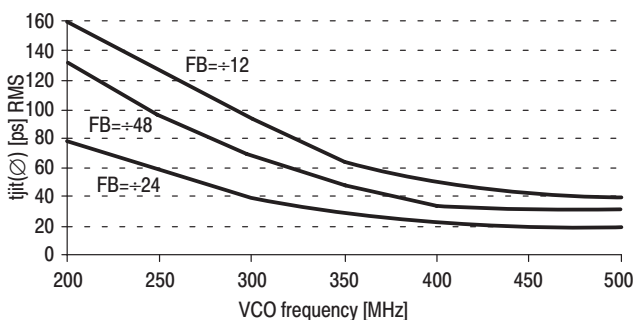


Figure 7. MPC9774 I/O Jitter

Driving Transmission Lines

The MPC9774 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC} \div 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9774 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 8 "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9774 clock driver is effectively doubled due to its capability to drive multiple lines.

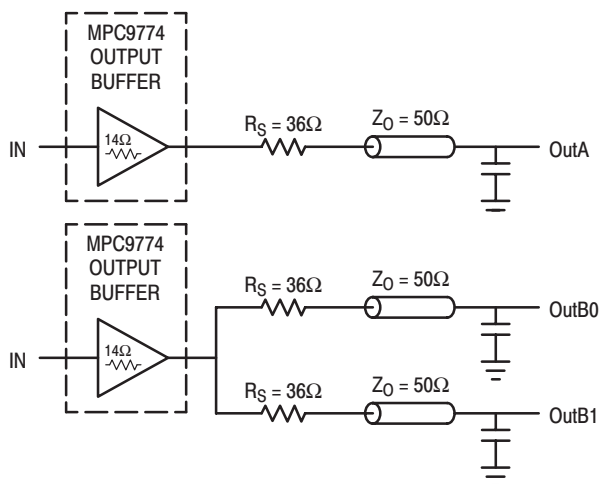


Figure 8. Single versus Dual Transmission Lines

The waveform plots in Figure 9 "Single versus Dual Line Termination Waveforms" show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9774 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9774. The output waveform in Figure 9 "Single versus Dual Line Termination Waveforms" shows a step in the waveform, this step is caused by the impedance mismatch seen

looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned} V_L &= V_S (Z_0 \div (R_S + R_0 + Z_0)) \\ Z_0 &= 50\Omega \parallel 50\Omega \\ R_S &= 36\Omega \parallel 36\Omega \\ R_0 &= 14\Omega \\ V_L &= 3.0 (25 \div (18 + 17 + 25)) \\ &= 1.31V \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

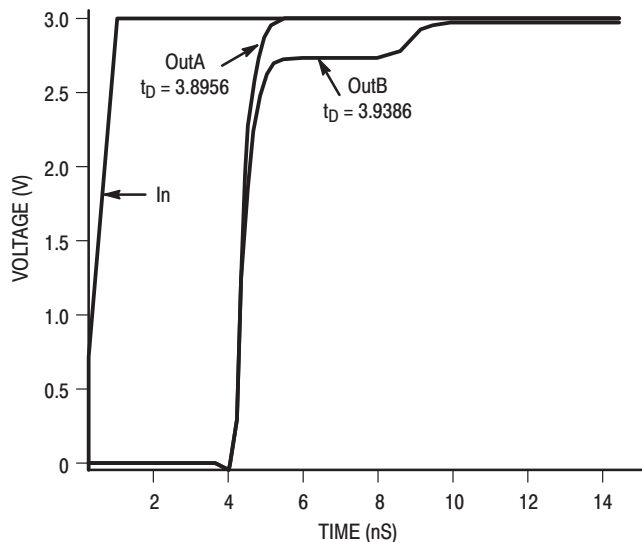


Figure 9. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 10 "Optimized Dual Line Termination" should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

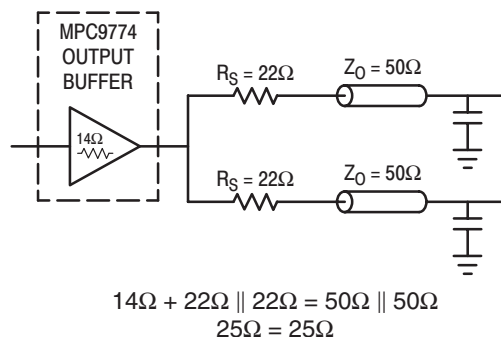


Figure 10. Optimized Dual Line Termination

Power Supply Filtering

The MPC9774 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the VCC_PLL power supply impacts the device characteristics, for instance I/O jitter. The MPC9774 provides separate power supplies for the output buffers (VCC) and the phase-locked loop (VCC_PLL) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the VCC_PLL pin for the MPC9774. Figure 11 illustrates a typical power supply filter scheme. The MPC9774 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F . From the data sheet the ICC_PLL current (the current sourced through the VCC_PLL pin) is typically 5 mA (7.5 mA maximum), assuming that a minimum of 3.02 V (VCC_PLL, min) must be maintained on the VCC_PLL pin. The resistor R_F shown in Figure 11 must have a resistance of 5-15 Ω to meet the voltage drop criteria.

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC

filter shown in Figure 11, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

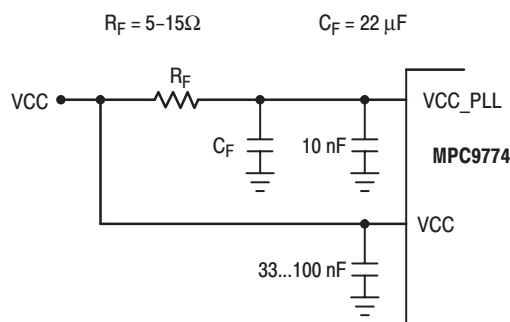


Figure 11. VCC_PLL Power Supply Filter

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9774 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

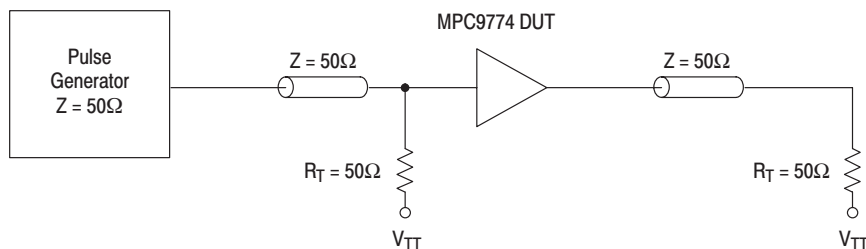
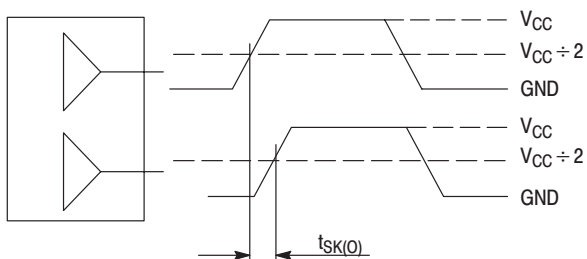
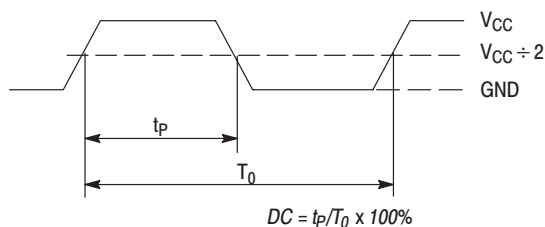


Figure 12. CCLK MPC9774 AC test reference



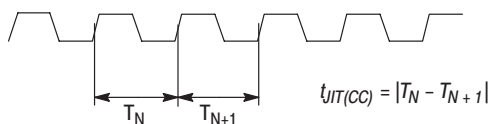
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 13. Output-to-output Skew $t_{SK(O)}$



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 15. Output Duty Cycle (DC)



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 17. Cycle-to-cycle Jitter

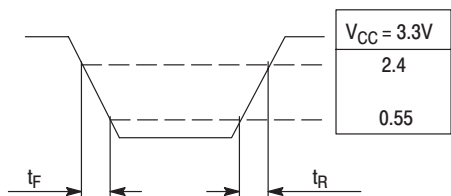


Figure 19. Output Transition Time Test Reference

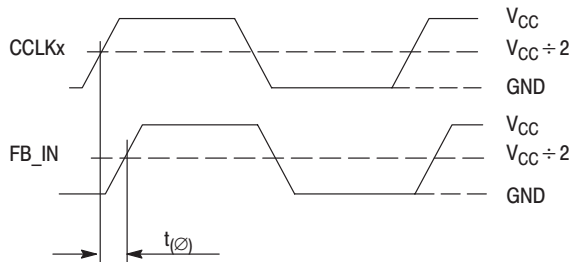
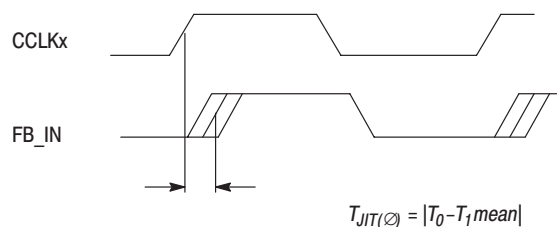
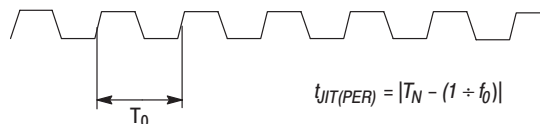


Figure 14. Propagation delay (t_{ϕ} , static phase offset) test reference



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 16. I/O Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 18. Period Jitter

Product Preview

Clock Generator for Power- QUICC III

The MPC9850 is a PLL based clock generator specifically designed for Motorola Microprocessor And Microcontroller applications including the PowerQUICC III. This device generates a microprocessor input clock plus the 500 MHz Rapid I/O clock. The microprocessor clock is selectable in output frequency to any of the commonly used microprocessor input and bus frequencies. The Rapid I/O outputs are LVDS compatible. The device offers eight low skew clock outputs organized into two output banks, each configurable to support different clock frequencies. The extended temperature range of the MPC9850 supports telecommunication and networking requirements.

Features

- 8 LVCMOS outputs for processor and other circuitry
- 2 differential LVDS outputs for Rapid I/O interface
- Crystal oscillator or external reference input
- 25 or 33 MHz Input reference frequency
- Selectable output frequencies include = 200, 166, 133, 125, 111, 100, 83, 66, 50, 33 or 16 MHz
- Buffered reference clock output
- Rapid I/O (LVDS) Output = 500, 250 or 125 MHz
- Low cycle-to-cycle and period jitter
- 100 lead PBGA package
- 3.3V supply with 3.3V or 2.5V (Bank B) output LVCMOS drive
- Supports computing, networking, telecommunications applications
- Ambient temperature range -40°C to +85°C

Functional Description

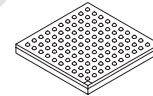
The MPC9850 uses either a 25 or 33 MHz reference frequency to generate 8 LVCMOS output clocks, of which, the frequency is selectable from 16 MHz to 200 MHz. The reference is applied to the input of a PLL and multiplied to 2 GHz. Output dividers, divide this frequency by 10, 12, 15, 16, 18, 20, 24, 30, 40, 60 or 120 to produce output frequencies of 200, 166, 133, 125, 111, 100, 83, 66, 50, 33 or 16 MHz. The single-ended LVCMOS outputs are divided into two banks of 4 low skew outputs each, for use in driving a microprocessor or microcontroller clock input as well as other system components. The 2 GHz PLL output frequency is also divided to produce a 125, 250 or 500 MHz clock output for Rapid I/O applications such as found on the PowerQUICC III communications processor. The input reference, either crystal or external input is also buffered to a separate output that may be used as the clock source for a Gigabit Ethernet PHY if desired.

The reference clock may be provided by either an external clock input of 25 MHz or 33 MHz. An internal oscillator requiring a 25 MHz crystal for frequency control may also be used. The external clock source may be applied to either of two clock inputs and selected via the CLK_SEL control input. Both single ended LVCMOS and differential LVPECL inputs are available. The crystal oscillator or external clock input is selected via the input pin of REF_SEL. Other than the crystal, no external components are required for crystal oscillator operation. The REF_33MHz configuration pins is used to select between a 33 and 25 MHz input frequency.

The MPC9850 is packaged in a 100 lead MAPBGA package to optimize both performance and board density.

MPC9850

**MICROPROCESSOR
CLOCK GENERATOR**



VF SUFFIX
100 MAP PBGA PACKAGE
CASE 1462

2

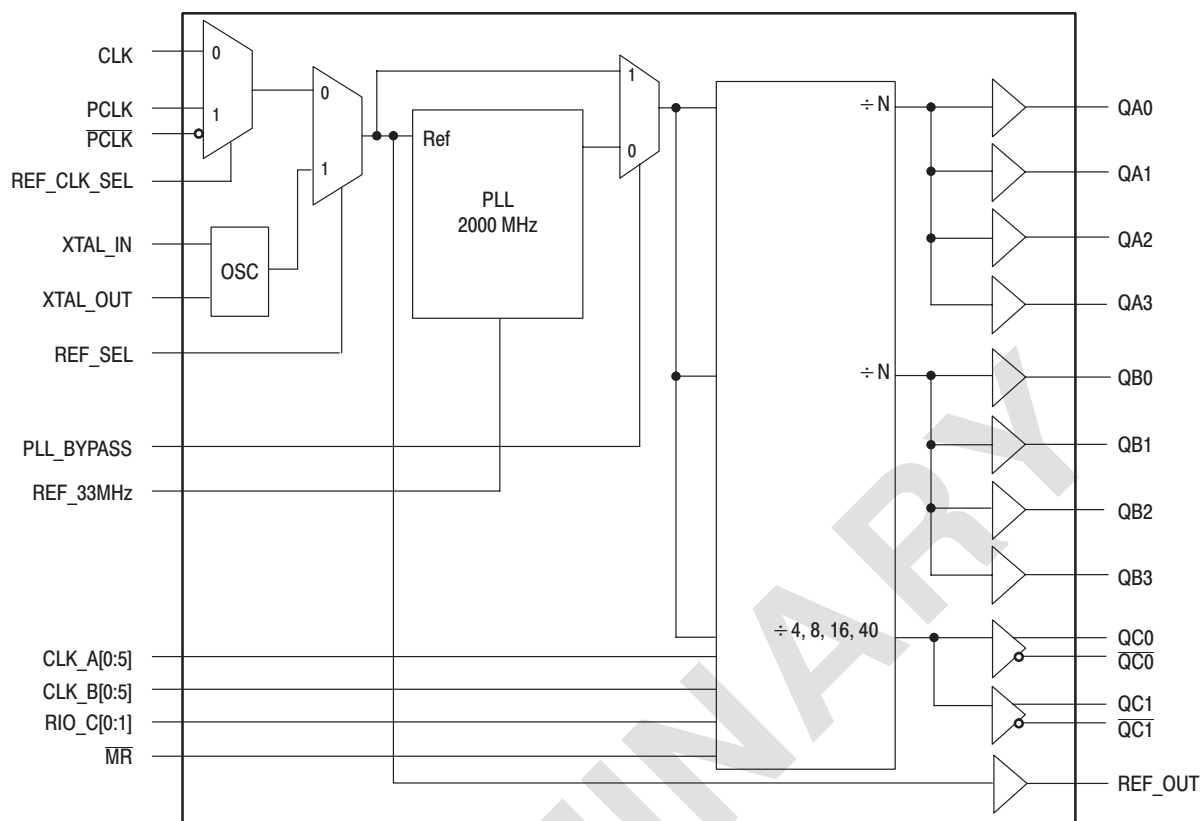


Figure 1. MPC9850 Block Diagram

Table 1. PIN CONFIGURATIONS

Pin	I/O	Type	Function	Supply	Active/State
CLK	Input	LVC MOS	PLL reference clock input (pull-down)	V _{DD}	
PCLK, PCLK	Input	LVPECL	PLL reference clock input (PCLK – pull-down, PCLK – pull-up and pull-down)	V _{DD}	
QA0, QA1, QA2, QA3	Output	LVC MOS	Bank A Outputs	V _{DDOA}	
QB0, QB1, QB2, QB3	Output	LVC MOS	Bank B Outputs	V _{DD}	
QC0, QC1, QC0, QC1	Output	LVDS	Bank C Outputs		
REF_OUT	Output	LVC MOS	Reference Output (25 MHz or 33 MHz)	V _{DD}	
XTAL_IN	Input	LVC MOS	Crystal Oscillator Input Pin	V _{DD}	
XTAL_OUT	Output	LVC MOS	Crystal Oscillator Output Pin	V _{DD}	
REF_CLK_SEL	Input	LVC MOS	Select between CLK and PCLK input (pull-down)	V _{DD}	high
REF_SEL	Input	LVC MOS	Select between External Input and Crystal Oscillator Input (pull-down)	V _{DD}	high
REF_33MHz	Input	LVC MOS	Selects 33MHz input (pull-down)	V _{DD}	high
MR	Input	LVC MOS	Master Reset (pull-up)	V _{DD}	low
PLL_BYPASS	Input	LVC MOS	Select PLL or static test mode (pull-down)	V _{DD}	high
CLK_A[0:5] ^a	Input	LVC MOS	Configures Bank A clock output frequency (pull-up)	V _{DD}	high
CLK_B[0:5] ^b	Input	LVC MOS	Configures Bank B clock output frequency (pull-up)	V _{DDOB}	high
RIO_C[0:1]	Input	LVC MOS	Configures Bank C clock output frequency (pull-down)	V _{DD}	
V _{DD}			3.3 V Supply		
V _{DDA}			Analog Supply		
V _{DDOB}			Supply for Output Bank B		
GND			Ground		

a. PowerPC bit ordering (bit 0 = msb, bit 5 = lsb)

b. PowerPC bit ordering (bit 0 = msb, bit 5 = lsb)

c. PowerPC bit ordering (bit 0 = msb, bit 1 = lsb)

Table 2. FUNCTION TABLE

Control	Default	0	1
REF_CLK_SEL	0	CLK	PCLK
REF_SEL	0	CLK or PCLK	XTAL
PLL_BYPASS	0	Normal	Bypass
REF_33MHz	0	Selects 25MHz Reference	Selects 33MHz Reference
$\overline{MR}$	1	Reset	Normal

CLK_A, CLK_B, and RIO_C control output frequencies. See Table 3 and Table 4 for specific device configuration

2

Table 3. OUTPUT CONFIGURATIONS (BANKS A & B)

CLK_x[0:5] ^a	CLK_x[0] (msb)	CLK_x[1]	CLK_x[2]	CLK_x[3]	CLK_x[4]	CLK_x[5] (lsb)	N	Frequency (MHz)
111111	1	1	1	1	1	1	126	15.87
111100	1	1	1	1	0	0	120	16.67
101000	1	0	1	0	0	0	80	25.00
011110	0	1	1	1	1	0	60	33.33
010100	0	1	0	1	0	0	40	50.00
001111	0	0	1	1	1	1	30	66.67
001100	0	0	1	1	0	0	24	83.33
001010	0	0	1	0	1	0	20	100.00
001001	0	0	1	0	0	1	18	111.11
001000	0	0	1	0	0	0	16	125.00
000111	0	0	0	1	1	1	15	133.33
000110	0	0	0	1	1	0	12	166.67
000101	0	0	0	1	0	1	10	200.00
000100	0	0	0	1	0	0	8 ^b	250

a. PowerPC bit ordering (bit 0 = msb, bit 5 = lsb)

b. Minimum value for N

Table 4. OUTPUT CONFIGURATIONS (BANK C)

RIO_C[0:1]	Frequency (MHz)
00	50 (test output)
01	125
10	250
11	500

OPERATION INFORMATION

Output Frequency Configuration

The MPC9850 was designed to provide the commonly used frequencies in PowerQUICC, PowerPC and other microprocessor systems. Table 3 lists the configuration values that will generate those common frequencies. The MPC9850 can generate numerous other frequencies that may be useful in specific applications. The output frequency (f_{out}) of either Bank A or Bank B may be calculated by the following equation.

$$f_{out} = 2000 / N$$

where f_{out} is in MHz and $N = 2 * CLK\_x[0:5]$

This calculation is valid for all values of N from 8 to 126. Note that N = 15 is a modified case of the configuration inputs

$CLK\_x[0:5]$. To achieve N = 15 $CLK\_x[0:5]$ is configured to 00111 or 7.

Crystal Input Operation

TBD

Power-Up and $\overline{MR}$ Operation

Figure 2 defines the release time and the minimum pulse length for $\overline{MR}$ pin. The $\overline{MR}$ release time is based upon the power supply being stable and within V_{DD} specifications. See Table 11 for actual parameter values. The MPC9850 may be configured after release of reset and the outputs will be stable for use after lock indication is obtained.

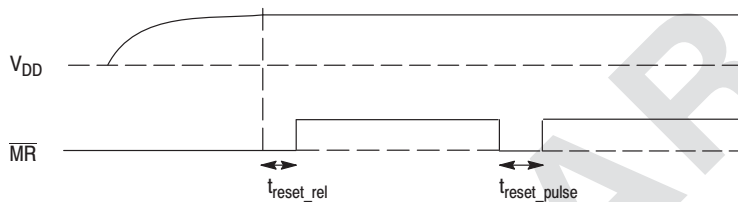


Figure 2. MR operation

Power Supply Bypassing

The MPC9850 is a mixed analog/digital product. The architecture of the MPC9850 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{DD} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

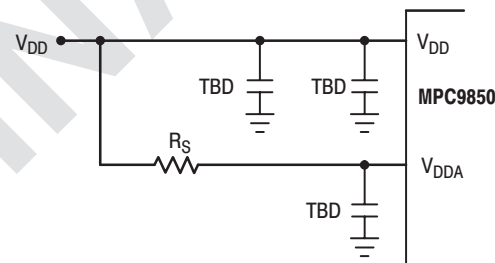


Figure 3. V_{CC} Power Supply Bypass

Table 5. ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{DD}	Supply Voltage (core)	-0.3	3.8	V	
V _{DDA}	Supply Voltage (Analog Supply Voltage)	-0.3	V _{DD}	V	
V _{DDOB}	Supply Voltage (LVCMOS output for Bank B)	-0.3	V _{DD}	V	
V _{IN}	DC Input Voltage	-0.3	V _{DD} +0.3	V	
V _{OUT}	DC Output Voltage ^b	-0.3	V _{DDx} +0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

b. V_{DDx} references power supply pin associated with specific output pin.

Table 6. GENERAL SPECIFICATIONS

Sym- bol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output Termination Voltage		V _{DD} ÷ 2 V _{DDOB} ÷ 2		V	Bank A output Bank B output
MM	ESD Protection (Machine Model)	TBD			V	
HBM	ESD Protection (Human Body Model)	TBD			V	
CDM	ESD Protection (Charged Device Model)	TBD			V	
LU	Latch-Up Immunity	200			mA	
C _{IN}	Input capacitance		TBD		pF	Inputs
θ _{JC}	Thermal resistance (junction-to-ambient, junction-to-board, junction-to-case)		TBD		°C/W	
T _A	Ambient Temperature ^a	-40		85	°C	

a. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MPC9850 to be used in applications requiring industrial temperature range. It is recommended that users of the MPC9850 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 7. DC CHARACTERISTICS (T_A = -40°C to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Supply Current for V _{DD} =3.3V±5% and V _{DDOB} = 3.3V±5%						
I _{DD}	Maximum Quiescent Supply Current (Core)		TBD	TBD	mA	V _{DD} pins
I _{DDC}	Maximum Quiescent Supply Current (Analog Supply)		TBD	TBD	mA	V _{DDIN} pins
I _{DDOB}	Maximum Bank B Supply Current		TBD	TBD	mA	V _{DDOB} pins
Supply Current for V _{DD} =3.3V±5% and V _{DDOB} = 2.5V±5%						
I _{DD}	Maximum Quiescent Supply Current (Core)		TBD	TBD	mA	V _{DD} pins
I _{DDC}	Maximum Quiescent Supply Current (Analog Supply)		TBD	TBD	mA	V _{DDIN} pins
I _{DDOB}	Maximum Bank B Supply Current		TBD	TBD	mA	V _{DDOB} pins

Table 8. LVDS DC CHARACTERISTICS ($T_A = -40^{\circ}\text{C}$ to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Differential LVDS clock outputs ($\overline{\text{QC0}}$, $\overline{\text{QC0}}$ Cnd $\overline{\text{QC1}}$, $\overline{\text{QC1}}$) for $V_{DD}=3.3\text{V}\pm 5\%$						
V_{PP}	Output Differential Voltage ^a (peak-to-peak) (LVDS)	250			mV	
V_{OS}	Output Offset Voltage (LVDS)	1125		1275	mV	

a. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.

Table 9. LVPECL DC CHARACTERISTICS ($T_A = -40^{\circ}\text{C}$ to 85°C)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Differential LVPECL clock inputs (CLK1 , $\overline{\text{CLK1}}$) for $V_{DD}=3.3\text{V}\pm 0.5\%$						
V_{PP}	Differential Voltage ^b (peak-to-peak) (LVPECL)	250			mV	
V_{CMR}	Differential Input Crosspoint Voltage ^c (LVPECL)	1.0		$V_{DD} - 0.6$	V	

a. AC characteristics are design targets and pending characterization.

b. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.

c. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.

Table 10. LVCMOS I/O DC CHARACTERISTICS ($T_A = -40^{\circ}\text{C}$ to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS for $V_{DD}=3.3\text{V}\pm 5\%$						
V_{IH}	Input High Voltage	2.0		$V_{DD} + 0.3$	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current ^a			10	μC	$V_{IN}=V_{DDL}$ or GND
LVCMOS for $V_{DD}=3.3\text{V}\pm 5\%$ and $V_{DDOB} = 3.3\text{V}\pm 5\%$						
V_{OH}	Output High Voltage	2.4			V	$I_{OH}=-24\text{ ma}$
V_{OL}	Output Low Voltage			0.4	V	$I_{OL}= 24\text{ ma}$
Z_{OUT}	Output Impedance		14		Ω	
LVCMOS for $V_{DD}=3.3\text{V}\pm 5\%$ and $V_{DDOB} = 2.5\text{V}\pm 5\%$						
V_{OH}	Output High Voltage	1.9			V	$I_{OH}=-15\text{ ma}$
V_{OL}	Output Low Voltage			0.4	V	$I_{OL}= 15\text{ ma}$
Z_{OUT}	Output Impedance		22		Ω	

a. Inputs have pull-down resistors affecting the input current.

Table 11. AC CHARACTERISTICS ($V_{DD}=3.3V\pm5\%$, $V_{DDOB}=3.3V\pm5\%$, $T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$)^{a b}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Input and output timing specification						
f_{ref}	Input reference frequency (25 MHz input) Input reference frequency (33 MHz input) XTAL Input Input reference frequency in PLL bypass mode ^c	TBD TBD TBD	25 33 25	TBD TBD TBD	MHz MHz MHz	PLL bypass
f_{VCO}	VCO frequency range ^d		2000		MHz	
f_{MCX}	Output Frequency Bank C output Bank B output Bank C output			TBD TBD TBD	MHz MHz MHz	PLL locked
f_{refPW}	Reference Input Pulse Width	TBD			ps	
f_{refCcc}	Input Frequency Accuracy			100	ppm	
t_r, t_f	Output Rise/Fall Time	TBD		TBD	ns	20% to 80%
DC	Output duty cycle	47.5 45	50 50	52.5 55	%	3.3V operation 2.5V operation
DC _{OSC}	Reference Output for Crystal Input	TBD	50	TBD	%	
PLL specifications						
BW	PLL closed loop bandwidth ^e		TBD		kHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	
t_{reset_ref}	MR hold time on power up	TBD			ns	
t_{reset_pulse}	MR hold time	TBD			ns	
Skew and jitter specifications						
$t_{sk(O)}$	Output-to-output Skew (within a bank)			50	ps	
$t_{sk(O)}$	Output-to-output Skew (across banks A and B)			100	ps	$V_{DDOB} = 3.3V$
$t_{JIT(CC)}$	Cycle-to-cycle jitter RMS (1 σ) ^f			10	ps	
$t_{JIT(PER)}$	Period Jitter RMS (1 σ)		TBD		ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter RMS (1 σ)		TBD		ps	
t_r, t_f	Output Rise/Fall Time			TBD	ns	20% to 80%

a. AC characteristics are design targets and pending characterization.

b. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

c. In bypass mode, the MPC9850 divides the input reference clock.

d. The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{ref} = (f_{VCO} \div M) \cdot N$.

e. -3 dB point of PLL transfer characteristics.

f. See application note AN1934 for a jitter calculation for other confidence factors than 1 σ .

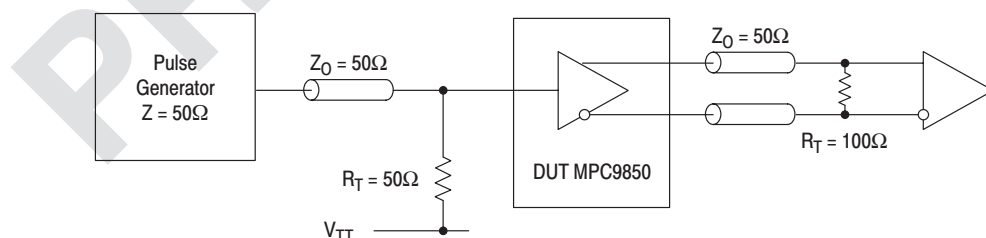
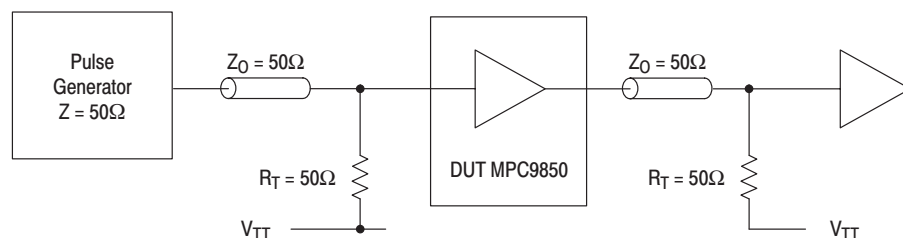
**Figure 4. MPC9850 AC test reference (LVDS outputs)****Figure 5. MPC9850 AC test reference (LVCMOS outputs)**

Table 12. MPC9850 Pin Diagram (Top View)

	1	2	3	4	5	6	7	8	9	10
A	V _{DDOB}	V _{DDOB}	CLKA[1]	CLKA[3]	CLKA[5]	V _{DD}	QA1	QA2	V _{DDOB}	V _{DDOB}
B	V _{DDOB}	V _{DDOB}	CLKA[0]	CLKA[2]	CLKA[4]	QA0	V _{DD}	QA3	V _{DDOB}	V _{DDOB}
C	RSVD	RSVD	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	REF_OUT
D	V _{DDA}	V _{DDA}	V _{DD}	GND	GND	GND	GND	V _{DD}	QC0	QC0
E	REF_SEL	CLK	V _{DD}	GND	GND	GND	GND	V _{DD}	V _{DD}	GND
F	PCLK	PCLK	V _{DD}	GND	GND	GND	GND	V _{DD}	QC1	QC1
G	REF_CLK_SEL	REF_33MHz	V _{DD}	GND	GND	GND	GND	V _{DD}	PLL_BY-PASS	M $\overline{R}$
H	XTAL_IN	XTAL_OUT	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	RIO_C[1]	RIO_C[0]
J	V _{DDOB}	V _{DDOB}	CLKB[0]	CLK[2]	CLK[4]	QB0	V _{DDOB}	QB3	V _{DDOB}	V _{DDOB}
K	V _{DDOB}	V _{DDOB}	CLKB[1]	CLKB[3]	CLKB[5]	V _{DDOB}	QB1	QB2	V _{DDOB}	V _{DDOB}

Table 13. MPC9850 Pin List

Signal	100 Pin MAPBGA	Signal	100 Pin MAPBGA	Signal	100 Pin MAPBGA	Signal	100 Pin MAPBGA	Signal	100 Pin MAPBGA
V _{DDOB}	A1	RSVD ^a	C1	REF_SEL	E1	REF_CLK_SEL	G1	V _{DDOB}	J1
V _{DDOB}	A2	RSVD ^a	C2	CLK	E2	REF_33MHz	G2	V _{DDOB}	J2
CLKA[1]	A3	V _{DD}	C3	V _{DD}	E3	V _{DD}	G3	CLKB[0]	J3
CLKA[3]	A4	V _{DD}	C4	GND	E4	GND	G4	CLKB[2]	J4
CLKA[5]	A5	V _{DD}	C5	GND	E5	GND	G5	CLKB[4]	J5
V _{DD}	A6	V _{DD}	C6	GND	E6	GND	G6	QB0	J6
QA1	A7	V _{DD}	C7	GND	E7	GND	G7	V _{DDOB}	J7
QA2	A8	V _{DD}	C8	V _{DD}	E8	V _{DD}	G8	QB3	J8
V _{DDOB}	A9	V _{DD}	C9	V _{DD}	E9	PLL_BYPASS	G9	V _{DDOB}	J9
V _{DDOB}	A10	REF_OUT	C10	GND	E10	M $\overline{R}$	G10	V _{DDOB}	J10
V _{DDOB}	B1	V _{DDA}	D1	PCLK	F1	XTAL_IN	H1	V _{DDOB}	K1
V _{DDOB}	B2	V _{DDA}	D2	PCLK	F2	XTAL_OUT	H2	V _{DDOB}	K2
CLKA[0]	B3	V _{DD}	D3	V _{DD}	F3	V _{DD}	H3	CLKB[1]	K3
CLKA[2]	B4	GND	D4	GND	F4	V _{DD}	H4	CLKB[3]	K4
CLKA[4]	B5	GND	D5	GND	F5	V _{DD}	H5	CLKB[5]	K5
QA0	B6	GND	D6	GND	F6	V _{DD}	H6	V _{DDOB}	K6
V _{DD}	B7	GND	D7	GND	F7	V _{DD}	H7	QB1	K7
QA3	B8	V _{DD}	D8	V _{DD}	F8	V _{DD}	H8	QB2	K8
V _{DDOB}	B9	QC0	D9	QC1	F9	RIO_C[1]	H9	V _{DDOB}	K9
V _{DDOB}	B10	QC0	D10	QC1	F10	RIO_C[0]	H10	V _{DDOB}	K10

a. RSVD pins must be left open.

Low Voltage PLL Clock Driver

The MPC990 is a 3.3 V compatible, PLL based clock driver. The fully differential design ensures optimum skew and PLL jitter performance. The performance of the MPC990 makes the device ideal for Workstation, Mainframe Computer and Telecommunication applications. The MPC990 offers an on-board crystal oscillator as the PLL reference and offers a secondary single-ended ECL clock for system test capabilities.

- Fully Integrated PLL
- Output Frequency Up to 400 MHz
- Operates from a 3.3 V Supply
- Output Frequency Configurable
- TQFP Packaging
- ± 50 ps Cycle-to-Cycle Jitter

The MPC990 offers three banks of outputs which can each be programmed via the the four fsel pins of the device. There are 16 different output frequency configurations available in the device. The configurations include output ratios of 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 4:3:1 and 4:3:2. The programming table in this data sheet illustrates the various programming options. The SYNC output monitors the relationship between the Qa and Qc output banks. The output pulses per the timing diagrams in this data sheet signal the coincident edges of the two output banks. This feature is useful for non binary relationships between output frequencies (i.e., 3:2 or 4:3 relationships). The Sync_Sel input toggles the Qd outputs between sync signals and extensions to the Qc bank of outputs.

The MPC990 provides a separate output for the feedback to the PLL. This allows for the feedback frequency to be programmed independently of the other outputs allowing for unique input vs output frequency relationships. The fselfB inputs provide 6 different feedback frequencies from the QFB differential output pair. The MPC990 features an external feedback to the PLL.

The PLL_En, Ref_Sel and the Test_Clk input pins provide a means of bypassing the PLL and driving the output buffers directly. This allows the user to single step a design during system debug. Note that the Test_Clk input is routed through the dividers so that, depending on the programming, several edges on the Test_Clk input will be needed to get corresponding edge transitions on the outputs. The VCO_Sel input provides a means of recentering the VCO to provide a broader range of VCO frequencies for stable PLL operation.

If the frequency select or the VCO_Sel pins are changed during operation, a master reset signal must be applied to ensure output synchronization and phase-lock. If the VCO is driven beyond its maximum frequency, the VCO can outrun the internal dividers when the VCO_Sel pin is low. This will also prevent the PLL from achieving lock. Again, a master reset signal will need to be applied to allow for phase-lock. The device employs a power-on reset circuit which will ensure output synchronization and PLL lock on initial power-up.

MPC990

**LOW VOLTAGE
PLL CLOCK DRIVER**



FA SUFFIX
52-LEAD TQFP PACKAGE
CASE 848D-03

2

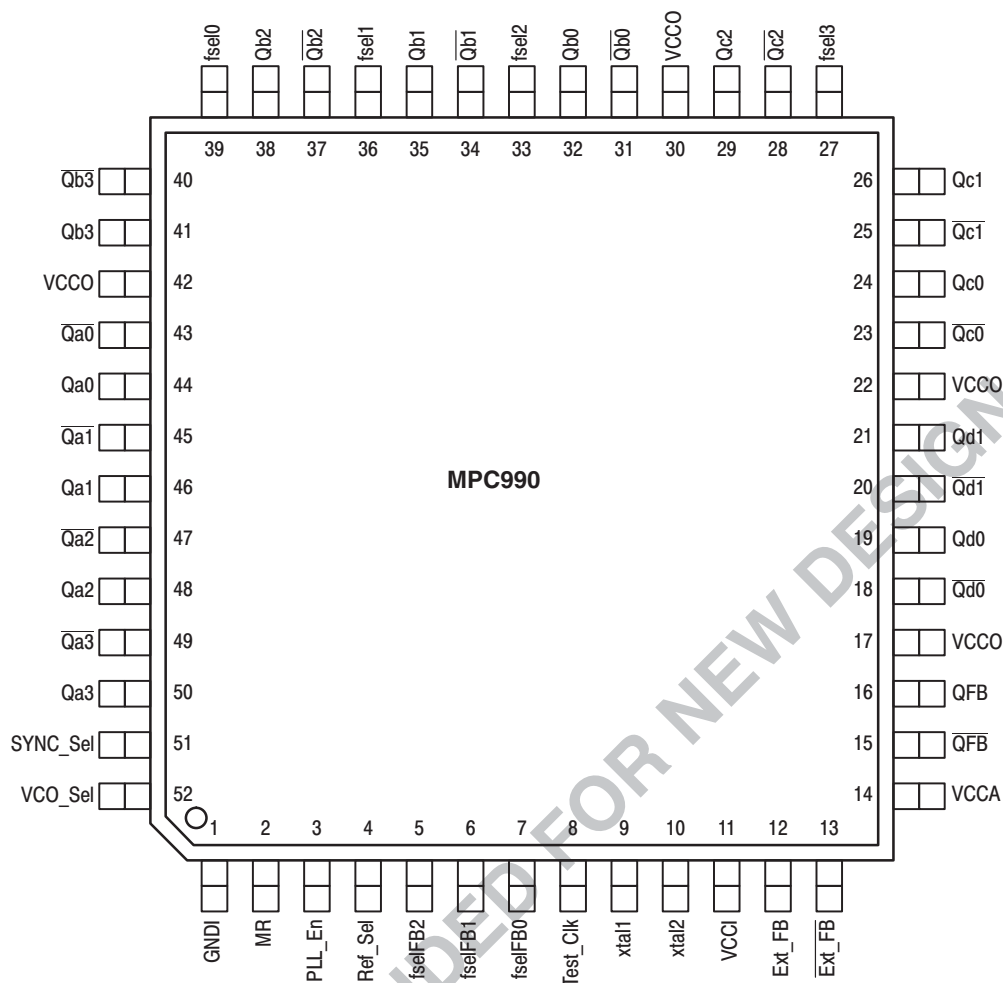


Figure 1. 52-Lead Pinout (Top View)

FUNCTION TABLE 1

INPUTS				OUTPUTS		
fsel3	fsel2	fsel1	fsel0	Qa	Qb	Qc
0	0	0	0	+2	+2	+2
0	0	0	1	+2	+2	+4
0	0	1	0	+2	+4	+4
0	0	1	1	+2	+2	+6
0	1	0	0	+2	+6	+6
0	1	0	1	+2	+4	+6
0	1	1	0	+2	+4	+8
0	1	1	1	+2	+6	+8
1	0	0	0	+2	+2	+8
1	0	0	1	+2	+8	+8
1	0	1	0	+4	+4	+6
1	0	1	1	+4	+6	+6
1	1	0	0	+4	+6	+8
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1	1	1	0	+6	+8	+8
1	1	1	1	+8	+8	+8

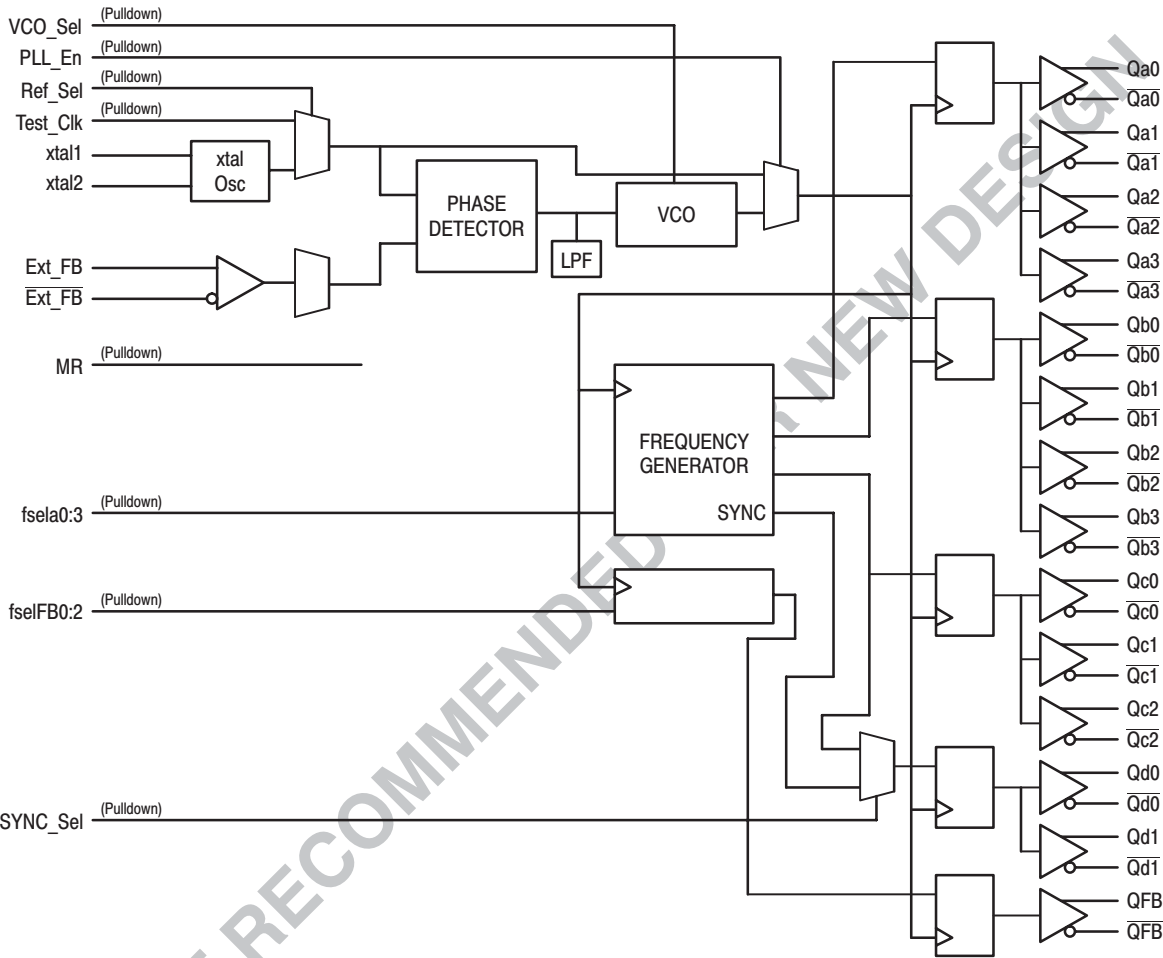
FUNCTION TABLE 2

fselFB2	fselFB1	fselFB0	QFB
0	0	0	+2
0	0	1	+4
0	1	0	+6
0	1	1	+8
1	0	0	+8
1	0	1	+16
1	1	0	+24
1	1	1	+32

FUNCTION TABLE 3

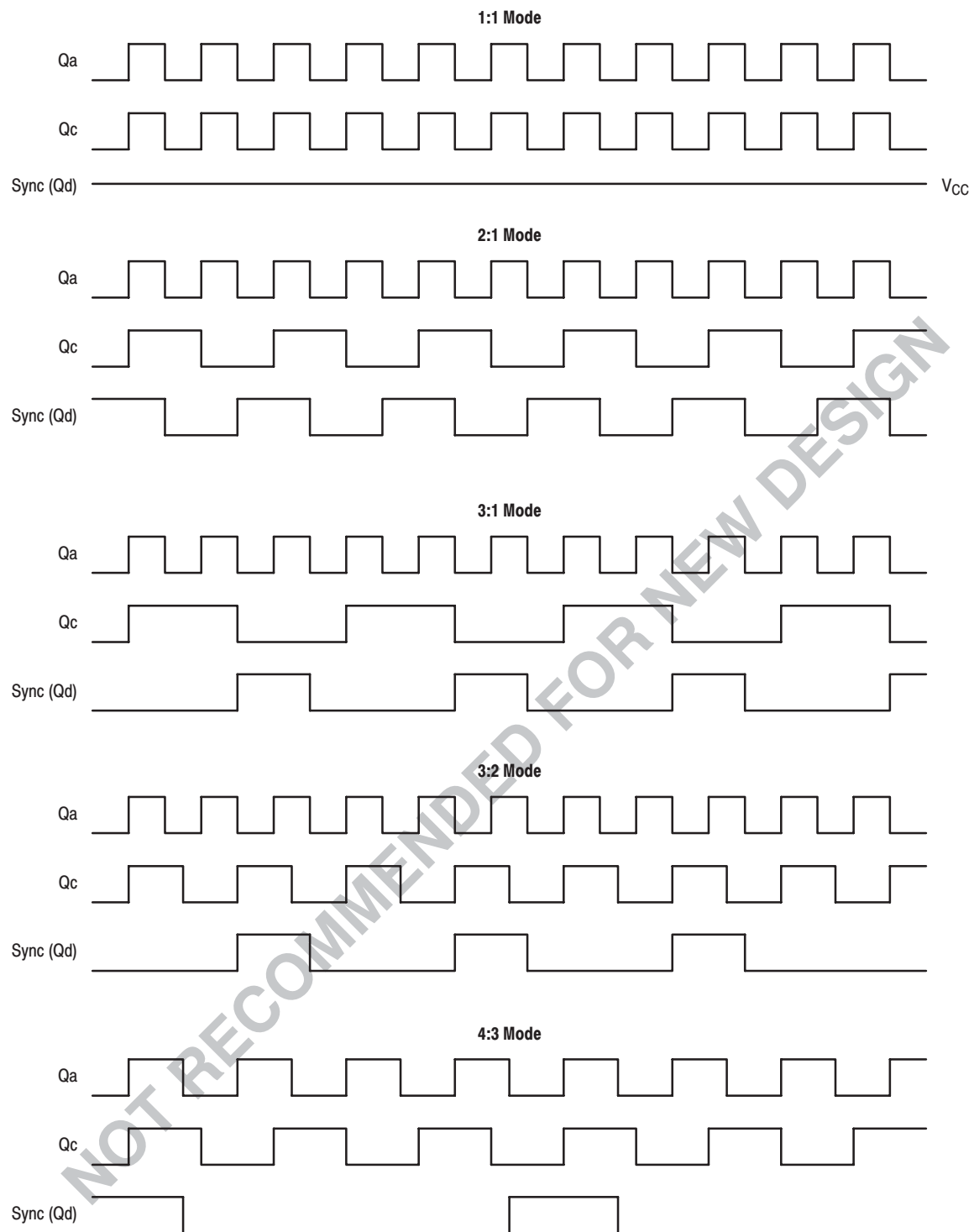
Control Pin	Logic '0'	Logic '1'
PLL_En	Enable PLL	Bypass PLL
VCO_Sel	fVCO	fVCO/2
Ref_Sel	xtal	Test_Clk
MR	—	Reset Outputs
SYNC_Sel	SYNC Outputs	Match Qc Outputs

2



NOTE: Ext_FB has internal pulldowns, while $\overline{\text{Ext\_FB}}$ has external pullups to ensure stability under open input conditions.

Figure 2. MPC990 Logic Diagram

**Figure 3. Timing Diagrams**

ECL DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CCA} = V_{CCI} = V_{CCO} = 0\text{ V}$, $GNDI = -3.3\text{ V} \pm 5\%$, Note 1.)

Symbol	Characteristic	0°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	-1.3		-0.7	-1.3	-1.0	-0.7	-1.3		-0.7	V
V_{OL}	Output LOW Voltage	-2.0		-1.4	-2.0	-1.7	-1.4	-2.0		-1.4	V
V_{IH}	Input HIGH Voltage	-1.1		-0.9	-1.1		-0.9	-1.1		-0.9	V
V_{IL}	Input LOW Voltage	-1.8		-1.5	-1.8		-1.5	-1.8		-1.5	V
V_{PP}	Minimum Input Swing	500			500			500			mV
V_{CMR}	Common Mode Range	V_{CC} -1.3 V		V_{CC} -0.5 V	V_{CC} -1.3 V		V_{CC} -0.5 V	V_{CC} -1.3 V		V_{CC} -0.5 V	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{GNDI}	Power Supply Current		200	240		200	240		200	240	mA

1. Refer to Motorola Application Note AN1545/D "Thermal Data for MPC Clock Drivers" for thermal management guidelines.

PECL DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CCA} = V_{CCI} = V_{CCO} = 3.3\text{ V} \pm 5\%$, $GNDI = 0\text{ V}$, Note 2.)

Symbol	Characteristic	0°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage (Note 3.)	2.0		2.6	2.0	2.3	2.6	2.3		2.6	V
V_{OL}	Output LOW Voltage (Note 3.)	1.3		1.9	1.3	1.6	1.9	1.3		1.9	V
V_{IH}	Input HIGH Voltage (Note 3.)	2.2		2.4	2.2		2.4	2.2		2.4	V
V_{IL}	Input LOW Voltage (Note 3.)	1.5		1.8	1.5		1.8	1.5		1.8	V
V_{PP}	Minimum Input Swing	500			500			500			mV
V_{CMR}	Common Mode Range	V_{CC} -1.3 V		V_{CC} -0.5 V	V_{CC} -1.3 V		V_{CC} -0.5 V	V_{CC} -1.3 V		V_{CC} -0.5 V	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{GNDI}	Power Supply Current		200	240		200	240		200	240	mA

2. Refer to Motorola Application Note AN1545/D "Thermal Data for MPC Clock Drivers" for thermal management guidelines.

3. These values are for $V_{CC} = 3.3\text{ V}$. Level Specifications will vary 1:1 with V_{CC} .

AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CCA} = V_{CCI} = V_{CCO} = 3.3\text{ V} \pm 5\%$, Termination of $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f_{xtal}	Crystal Oscillator Frequency	10		25	MHz	
t_r, t_f	Output Rise/Fall Time	0.2		1.0	ns	20% to 80%
t_{pw}	Output Duty Cycle	47.5	50	52.5	%	
t_{os}	Output-to-Output Skew Same Frequency Different Frequencies		150 250	250 350	ps	
f_{VCO}	PLL VCO Lock Range VCO_Sel = '0' VCO_Sel = '1'	400 200		800 400	MHz	FB +8 to +32 (Note 4.) FB +4 to +32
t_{pd}	Ref to Feedback Offset	75	250	425	ps	$f_{\text{ref}} = 50\text{ MHz}$ (Note 5.)
f_{max}	Maximum Output Frequency Qa,Qb,Qc (+2) Qa,Qb,Qc (+4) Qa,Qb,Qc (+6) Qa,Qb,Qc (+8)			400 200 133 100	MHz	
t_{jitter}	Cycle-to-Cycle Jitter (Peak-to-Peak)		± 50		ps	
t_{lock}	Maximum PLL Lock Time			10	ms	

4. With VCO_Sel = '0', the PLL will be unstable with a +2, +4 and some +6 feedback configurations. With VCO_Sel = '1', the PLL will be unstable with a +2 feedback ratio.
5. t_{pd} is specified for 50MHz input reference FB +8. The window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The t_{pd} does not include jitter.

PLL INPUT REFERENCE CHARACTERISTICS ($T_A = 0$ to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency VCO_SEL='0' Feedback divide 6 Feedback divide 8 Feedback divide 16 Feedback divide 24 Feedback divide 32 VCO_SEL='1' Feedback divide 4 Feedback divide 6 Feedback divide 8 Feedback divide 16 Feedback divide 24 Feedback divide 32	100 50 25 16.67 12.5 50 33.3 25 12.5 8.33 6.25	125 100 50 33.33 25 100 66.67 50 25 16.67 12.5	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

APPLICATIONS INFORMATION

Using the On-Board Crystal Oscillator

The MPC990 features an on-board crystal oscillator to allow for seed clock generation as well as final distribution. The on-board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC990 as possible to avoid any board level parasitics. To facilitate co-location surface mount crystals are recommended, but not required.

The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on-board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most of the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC990 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

The MPC990 is a clock driver which was designed to generate outputs with programmable frequency relationships and not a synthesizer with a fixed input frequency. As a result the crystal input frequency is a function of the desired output frequency. For a design which utilizes the external feedback to the PLL the selection of the crystal frequency is straight forward; simply chose a crystal which is equal in frequency to the fed back signal.

Table 14. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental at Cut
Resonance	Series Resonance*
Frequency Tolerance	± 75 ppm at 25°C
Frequency/Temperature Stability	± 150 pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7 pF
Equivalent Series Resistance (ESR)	50 to 80 Ω Max
Correlation Drive Level	100 μ W
Aging	5 ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

Power Supply Filtering

The MPC990 provides a separate power supply for the internal PLL of the device. The purpose of this design technique is to allow the user to filter externally generated system noise from the internal, relatively sensitive analog PLL.

Figure 4 illustrates a suggested power supply filter using an LC filter network. The inductor value should be chosen to maximize the AC filter impedance while maintaining a low DC resistance. An inductor with a maximum DC series resistance of 5 Ω should be used. The parallel capacitor combination on the V_{CCA} pin ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

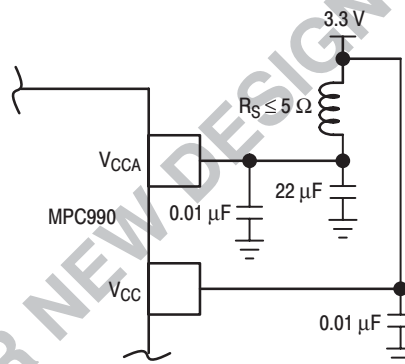


Figure 4. Power Supply Filter

Low Voltage PLL Clock Driver

The MPC991 is a 3.3 V compatible, PLL based ECL/PECL clock driver. The fully differential design ensures optimum skew and PLL jitter performance. The performance of the MPC991 makes the device ideal for Workstation, Mainframe Computer and Telecommunication applications. The MPC991 offers a differential ECL/PECL input for applications which need to lock to an existing clock signal. It also offers a secondary single-ended ECL clock for system test capabilities.

- Fully Integrated PLL
- Output Frequency up to 400 MHz
- ECL/PECL Inputs and Outputs
- Operates from a 3.3 V Supply
- Output Frequency Configurable
- TQFP Packaging
- ± 50 ps Cycle-to-Cycle Jitter

The MPC991 offers three banks of outputs which can each be programmed via the the four fsel pins of the device. There are 16 different output frequency configurations available in the device. The configurations include output ratios of 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 4:3:1 and 4:3:2. The programming table in this data sheet illustrates the various programming options. The SYNC output monitors the relationship between the Qa and Qc output banks. The output pulses per the timing diagrams in this data sheet signal the coincident edges of the two output banks. This feature is useful for non binary relationships between output frequencies (i.e., 3:2 or 4:3 relationships). The Sync_Sel input toggles the Qd outputs between sync signals and extensions to the Qc bank of outputs.

The MPC991 provides a separate output for the feedback to the PLL. This allows for the feedback frequency to be programmed independently of the other outputs allowing for unique input vs output frequency relationships. The fselFB inputs provide 6 different feedback frequencies from the QFB differential output pair.

The MPC991 features an external differential ECL/PECL feedback to the PLL. This external feedback feature allows the MPC991 to be used as a "zero" delay buffer. The propagation delay between the input reference and the output is dependent on the input reference frequency. The selection of higher reference frequencies will provide near zero delay through the device.

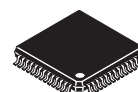
The PLL_En, Ref_Sel and the Test_Clk input pins provide a means of bypassing the PLL and driving the output buffers directly. This allows the user to single step a design during system debug. Note that the Test_Clk input is routed through the dividers so that depending on the programming several edges on the Test_Clk input will be needed to get corresponding edge transitions on the outputs. The VCO_Sel input provides a means of recentering the VCO to provide a broader range of VCO frequencies for stable PLL operation.

If the frequency select or the VCO_Sel pins are changed during operation, a master reset signal must be applied to ensure output synchronization and phase-lock. If the VCO is driven beyond its maximum frequency, the VCO can outrun the internal dividers when the VCO_Sel pin is low. This will also prevent the PLL from achieving lock. Again, a master reset signal will need to be applied to allow for phase-lock. The device employs a power-on reset circuit which will ensure output synchronization and PLL lock on initial power-up.

MPC991

See Upgrade Product – MPC9991

LOW VOLTAGE PLL CLOCK DRIVER



FA SUFFIX
52-LEAD TQFP PACKAGE
CASE 848D-03

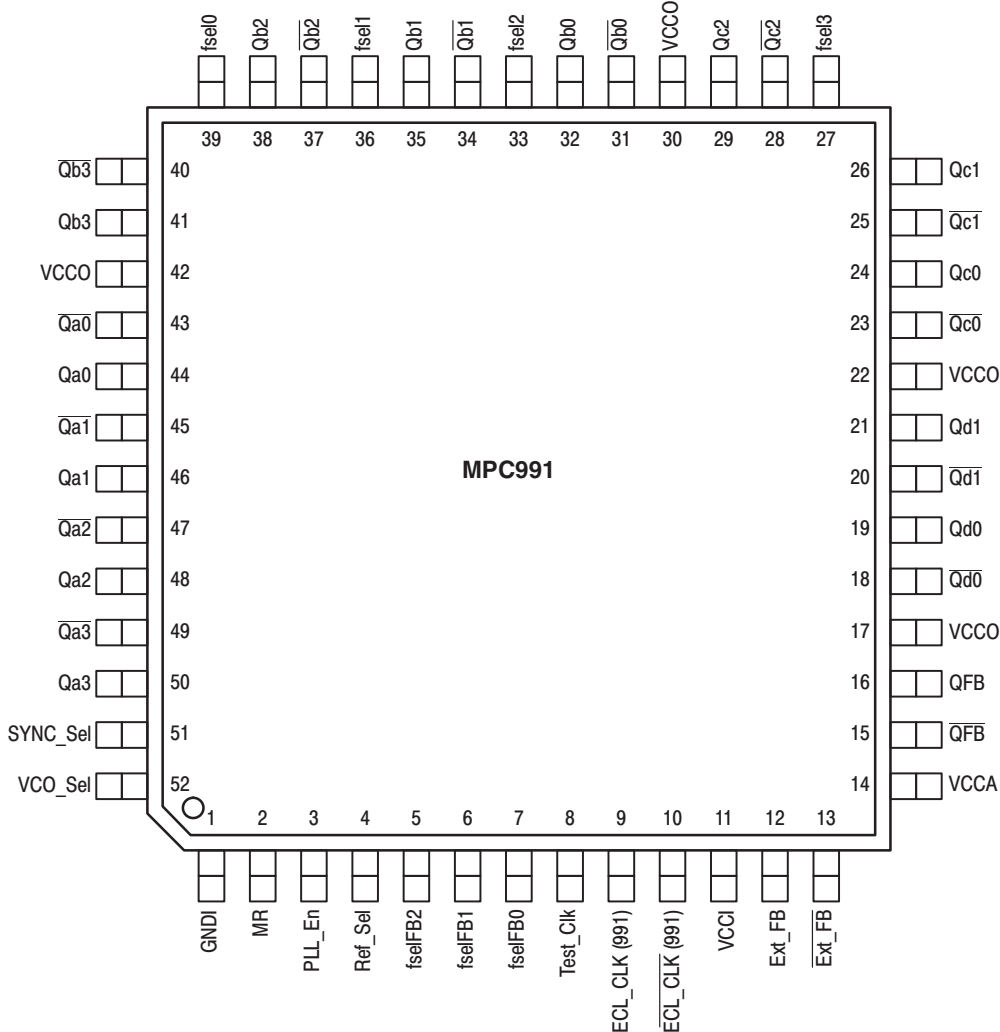


Figure 1. 52-Lead Pinout (Top View)

FUNCTION TABLE 1

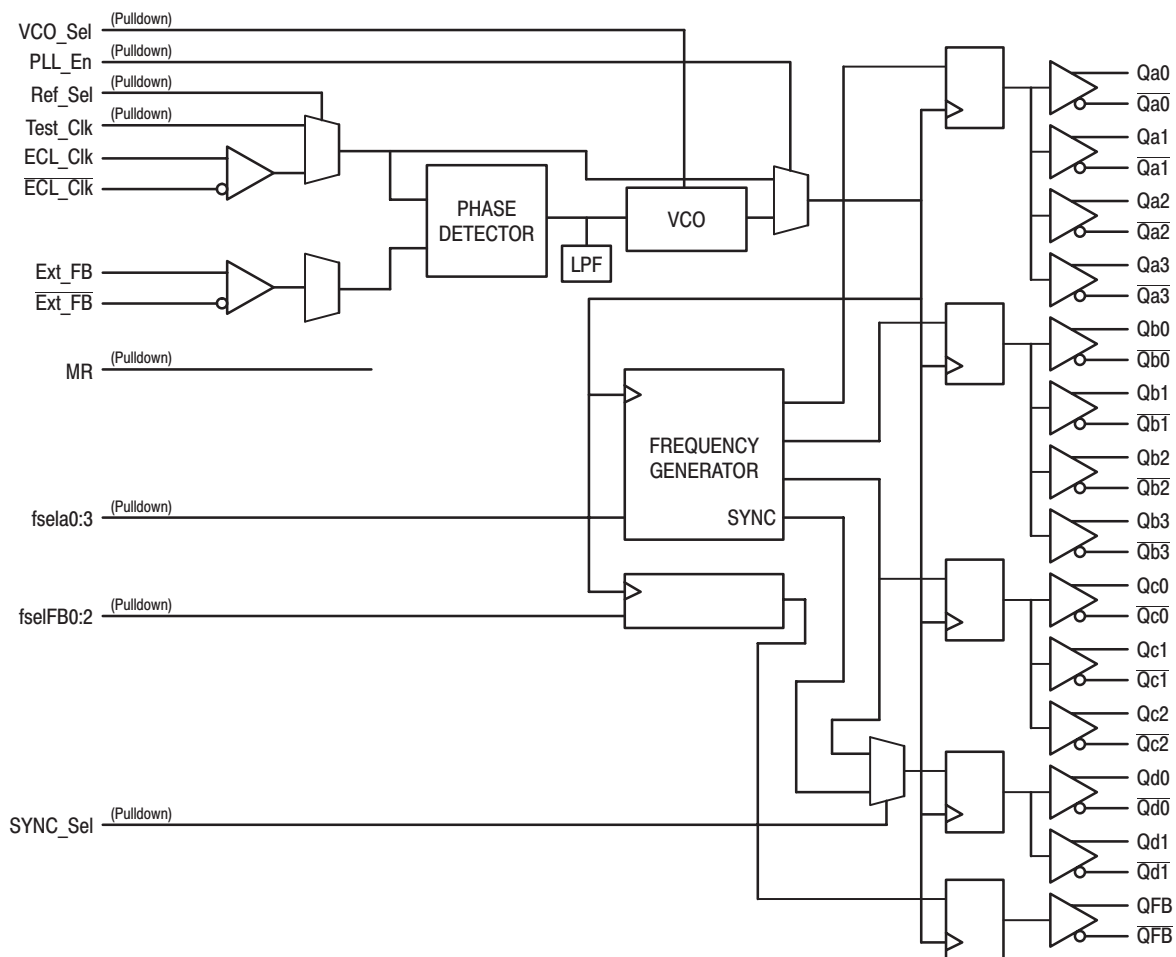
INPUTS				OUTPUTS		
fsel3	fsel2	fsel1	fsel0	Qa	Qb	Qc
0	0	0	0	+2	+2	+2
0	0	0	1	+2	+2	+4
0	0	1	0	+2	+4	+4
0	0	1	1	+2	+2	+6
0	1	0	0	+2	+6	+6
0	1	0	1	+2	+4	+6
0	1	1	0	+2	+4	+8
0	1	1	1	+2	+6	+8
1	0	0	0	+2	+2	+8
1	0	0	1	+2	+8	+8
1	0	1	0	+4	+4	+6
1	0	1	1	+4	+6	+6
1	1	0	0	+4	+6	+8
1	1	0	1	+6	+6	+8
1	1	1	0	+6	+8	+8
1	1	1	1	+8	+8	+8

FUNCTION TABLE 2

fselFB2	fselFB1	fselFB0	QFB
0	0	0	+2
0	0	1	+4
0	1	0	+6
0	1	1	+8
1	0	0	+8
1	0	1	+16
1	1	0	+24
1	1	1	+32

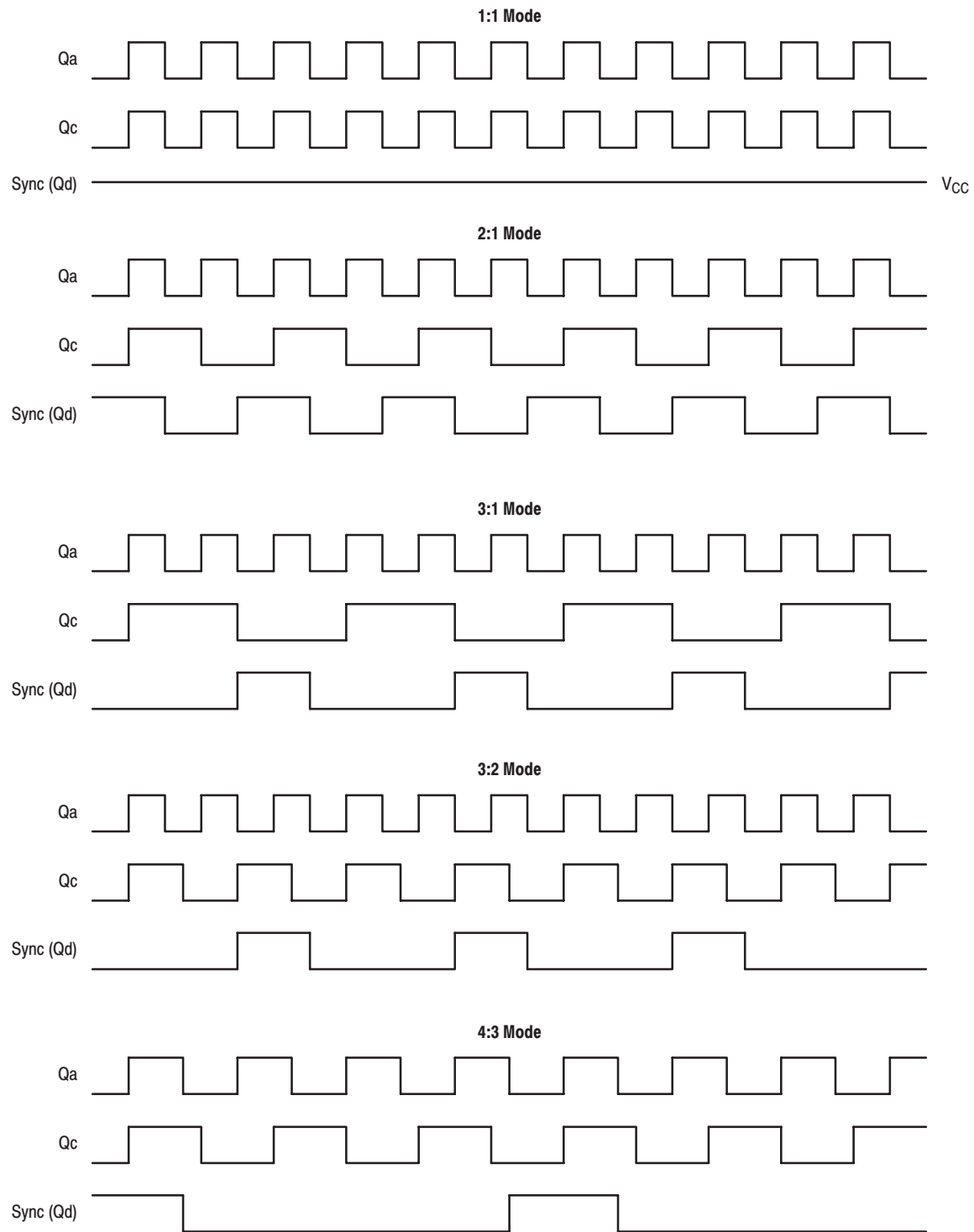
FUNCTION TABLE 3

Control Pin	Logic '0'	Logic '1'
PLL_En	Enable PLL	Bypass PLL
VCO_Sel	fVCO	fVCO/2
Ref_Sel	ECL/PECL	Test_Clk
MR	—	Reset Outputs
SYNC_Sel	SYNC Outputs	Match Qc Outputs



NOTE: ECL_Clk, Ext_FB have internal pulldowns, while $\overline{\text{ECL\_Clk}}$, $\overline{\text{Ext\_FB}}$ have external pullups to ensure stability under open input conditions.

Figure 2. MPC991 Logic Diagram

**Figure 3. Timing Diagrams**

ECL DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CCA} = V_{CCI} = V_{CCO} = 0\text{ V}$, $\text{GNDI} = -3.3\text{ V} \pm 5\%$, Note 1.)

Symbol	Characteristic	0°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	-1.3		-0.7	-1.3	-1.0	-0.7	-1.3		-0.7	V
V_{OL}	Output LOW Voltage	-2.0		-1.4	-2.0	-1.7	-1.4	-2.0		-1.4	V
V_{IH}	Input HIGH Voltage	-1.1		-0.9	-1.1		-0.9	-1.1		-0.9	V
V_{IL}	Input LOW Voltage	-1.8		-1.5	-1.8		-1.5	-1.8		-1.5	V
V_{PP}	Minimum Input Swing	500			500			500			mV
V_{CMR}	Common Mode Range	V_{CC} -1.3V		V_{CC} -0.5V	V_{CC} -1.3V		V_{CC} -0.5V	V_{CC} -1.3V		V_{CC} -0.5V	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{GNDI}	Power Supply Current		200	240		200	240		200	240	mA

1. Refer to Motorola Application Note AN1545/D "Thermal Data for MPC Clock Drivers" for thermal management guidelines.

PECL DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CCA} = V_{CCI} = V_{CCO} = 3.3\text{ V} \pm 5\%$, $\text{GNDI} = 0\text{ V}$, Note 2.)

Symbol	Characteristic	0°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage (Note 3.)	2.0		2.6	2.0	2.3	2.6	2.3		2.6	V
V_{OL}	Output LOW Voltage (Note 3.)	1.3		1.9	1.3	1.6	1.9	1.3		1.9	V
V_{IH}	Input HIGH Voltage (Note 3.)	2.2		2.4	2.2		2.4	2.2		2.4	V
V_{IL}	Input LOW Voltage (Note 3.)	1.5		1.8	1.5		1.8	1.5		1.8	V
V_{PP}	Minimum Input Swing	500			500			500			mV
V_{CMR}	Common Mode Range	V_{CC} -1.3V		V_{CC} -0.5V	V_{CC} -1.3V		V_{CC} -0.5V	V_{CC} -1.3V		V_{CC} -0.5V	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{GNDI}	Power Supply Current		200	240		200	240		200	240	mA

2. Refer to Motorola Application Note AN1545/D "Thermal Data for MPC Clock Drivers" for thermal management guidelines.

3. These values are for $V_{CC} = 3.3\text{V}$. Level Specifications will vary 1:1 with V_{CC} .

AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CCA} = V_{CCI} = V_{CCO} = 3.3\text{ V} \pm 5\%$, Termination of $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time	0.2		1.0	ns	20% to 80%
t_{pw}	Output Duty Cycle	47.5	50	52.5	%	
t_{os}	Output-to-Output Skew Same Frequency Different Frequencies		150 250	250 350	ps	
f_{VCO}	PLL VCO Lock Range $V_{CO\_Sel} = '0'$ $V_{CO\_Sel} = '1'$	400 200		800 400	MHz	FB +8 to +32 (Note 4.) FB +4 to +32
t_{pd}	Ref to Feedback Offset	75	250	425	ps	$f_{ref} = 50\text{MHz}$ (Note 5.)
f_{max}	Maximum Output Frequency Qa,Qb,Qc (+2) Qa,Qb,Qc (+4) Qa,Qb,Qc (+6) Qa,Qb,Qc (+8)			400 200 133 100	MHz	
t_{jitter}	Cycle-to-Cycle Jitter (Peak-to-Peak)		± 50		ps	
t_{lock}	Maximum PLL Lock Time			10	ms	

4. With $V_{CO\_Sel} = '0'$, the PLL will be unstable with a +2, +4 and some +6 feedback configurations. With $V_{CO\_Sel} = '1'$, the PLL will be unstable with a +2 feedback ratio.

5. t_{pd} is specified for 50MHz input reference FB + 8. The window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The t_{pd} does not include jitter.

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t _r , t _f	TCLK Input Rise/Falls		3.0	ns	
f _{ref}	Reference Input Frequency			MHz	
	Feedback divide 6	100	125		
	Feedback divide 8	50	100		
	Feedback divide 16	25	50		
	Feedback divide 24	16.67	33.33		
	Feedback divide 32	12.5	25		
	VCO_SEL='0'				
	Feedback divide 4	50	100		
	Feedback divide 6	33.3	66.67		
	Feedback divide 8	25	50		
f _{refDC}	Reference Input Duty Cycle	25	75	%	

APPLICATIONS INFORMATION

Power Supply Filtering

The MPC991 provides a separate power supply for the internal PLL of the device. The purpose of this design technique is to allow the user to filter externally generated system noise from the internal, relatively sensitive analog PLL.

Figure 4 illustrates a suggested power supply filter using an LC filter network. The inductor value should be chosen to maximize the AC filter impedance while maintaining a low DC resistance. An inductor with a maximum DC series resistance of 5 Ω should be used. The parallel capacitor combination on the V_{CCA} pin ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

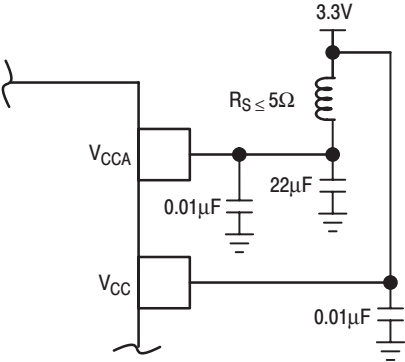
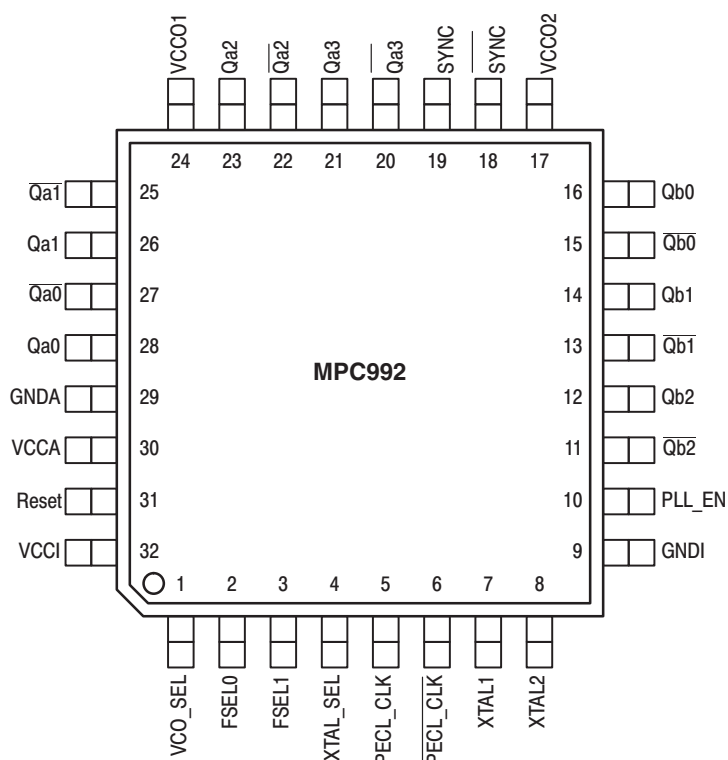


Figure 4. Power Supply Filter

2

The MPC992 is packaged in a 32-lead TQFP package to optimize both performance and board density.

FA SUFFIX
PLASTIC TQFP PACKAGE
CASE 873A-02



FUNCTION TABLE 1

FSEL0	FSEL1	Qa	Qb	Feedback	Ratio
0	0	VCO/4	VCO/6	VCO/24	3:2
0	1	VCO/2	VCO/4	VCO/16	2:1
1	0	VCO/4	VCO/10	VCO/40	5:2
1	1	VCO/2	VCO/6	VCO/24	3:1

FUNCTION TABLE 2

Control Signal	Logic '0'	Logic '1'
Reset	Outputs Enabled	Outputs Disabled
XTAL_SEL	PECL REF	XTAL REF
PLL_EN	Disabled	Enabled
VCO_SEL	High Frequency	Low Frequency

INPUT vs OUTPUT FREQUENCY

FSEL0	FSEL1	Qa	Qb	Int Feedback
0	0	6 (f_{ref})	4 (f_{ref})	f_{ref}
0	1	8 (f_{ref})	4 (f_{ref})	f_{ref}
1	0	10 (f_{ref})	4 (f_{ref})	f_{ref}
1	1	12 (f_{ref})	4 (f_{ref})	f_{ref}

PIN DESCRIPTION

Pin Name	Function
VCO_SEL	VCO range select pin (Int Pullup)
PLL_EN	PLL bypass select pin (Int Pullup)
XTAL_SEL	Input reference source select pin (Int Pullup)
XTAL1:2	Crystal interface pins for the internal oscillator
PECL_CLK	True PECL reference clock input (Int Pulldown)
PECL_CLK	Compliment PECL reference clock input (Int Pullup)
FSELn	Internal divider select pins (Int Pullup)
RESET	Internal flip-flop reset, true outputs go LOW (Int Pulldown)

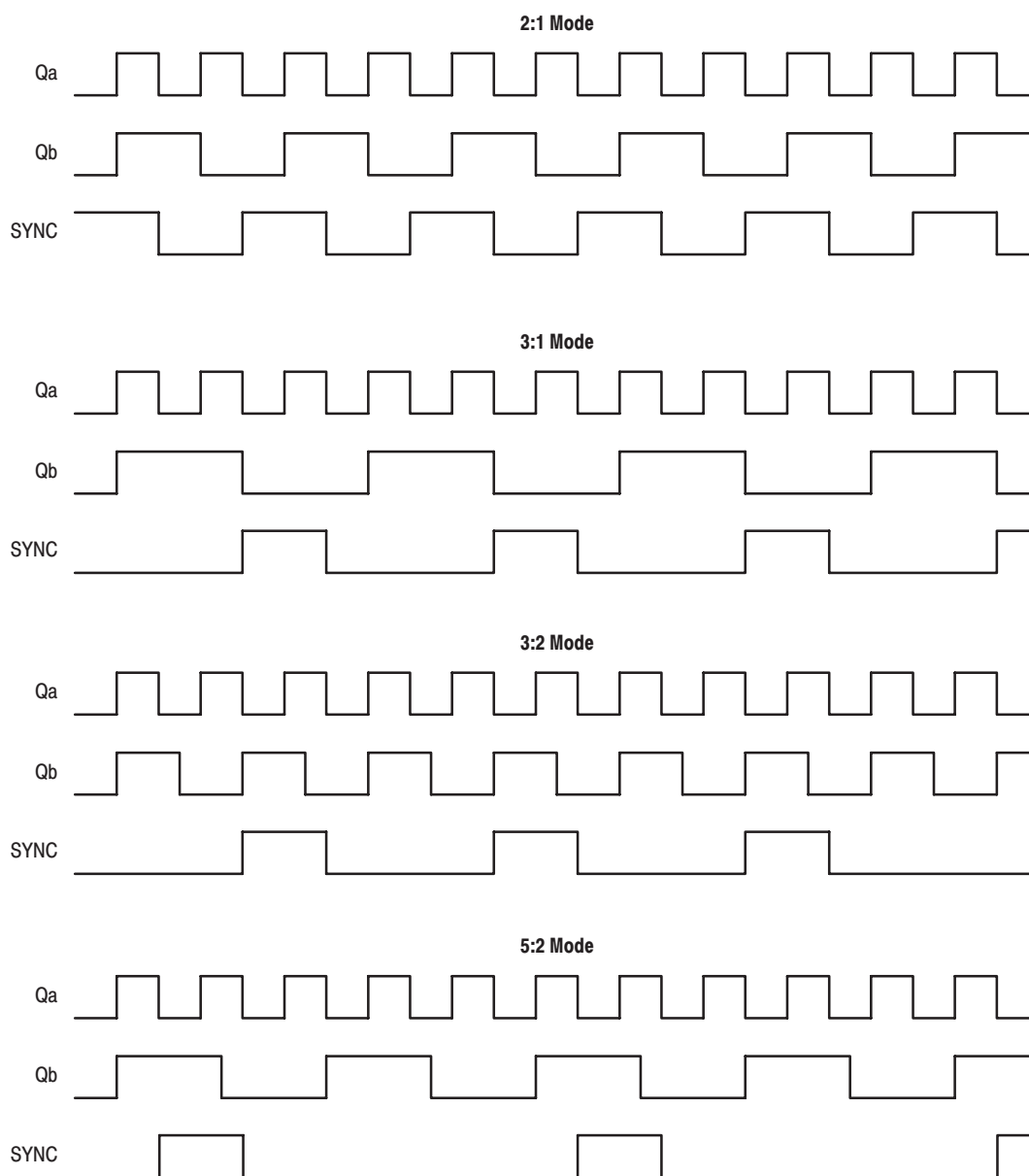


Figure 1. Output Waveforms

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	4.6	V
V_I	Input Voltage	-0.3	$V_{DD} + 0.3$	V
I_{OUT}	Output Current		50 100	mA
T_{Stor}	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage PECL_CLK ¹ Other	2.15 2.0		2.4 V_{CC}	V	$V_{CC} = 3.3\text{V}$
V_{IL}	Input LOW Voltage PECL_CLK ¹ Other	1.5 0		1.8 0.8	V	$V_{CC} = 3.3\text{V}$
V_{OH}	Output HIGH Voltage ¹	1.8		2.4	V	$V_{CC} = 3.3\text{V}$
V_{OL}	Output LOW Voltage ¹	1.2		1.7	V	$V_{CC} = 3.3\text{V}$
I_{IN}	Input Current	-120		120	μA	
I_{CCI}	Maximum Quiescent Supply Current		130	150	mA	
I_{CCA}	Maximum PLL Supply Current		15	20	mA	

1. DC levels will vary 1:1 with V_{CC} .

AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time	200		850	ps	20% to 80%
t_{pw1}	Output Duty Cycle	49		51	%	
t_{pw2}	SYNC Output Duty Cycle	0.95		1.05	%	PCLK Period
f_{ref}	Input Reference Frequency Xtal FREF	10 Note 2		20 Note 2	MHz	
t_{os}	Output-to-Output Skew Qa, Qb Qa (-) to SYNC (+)			100 300	ps	
f_{VCO}	PLL VCO Lock Range	200 400		440 750	MHz	$VCO\_SEL = 1$ $VCO\_SEL = 0$
f_{max}	Maximum Output Frequency Qa (+2) Qa, Qb (+4) Qb (+6) Qb (+10)			375 187.5 125 75	MHz	Note 1
t_{jitter}	Cycle-to-Cycle Jitter (Peak-to-Peak)		± 25	± 50	ps	Note 3
t_{lock}	Maximum PLL Lock Time			10	ms	

1. At 400MHz the output swing will be less than the nominal value.
2. ECLK and XTAL input reference limited by the feedback divide and the guaranteed VCO lock range.
3. Guaranteed by characterization.

APPLICATIONS INFORMATION

Using the On-Board Crystal Oscillator

The MPC992 features an on-board crystal oscillator to allow for seed clock generation as well as final distribution. The on-board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC992 as possible to avoid any board level parasitics. To facilitate co-location surface mount crystals are recommended, but not required.

The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on-board capacitors. Because the design is a series resonant design, for optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most off the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC992 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

Figure 2 shows an optional series capacitor in the crystal oscillator interface. The on-board oscillator introduces a small phase shift in the overall loop which causes the oscillator to operate at a frequency slightly slower than the specified crystal. The series capacitor is used to compensate the loop and allow the oscillator to function at the specified crystal frequency. If a 100ppm type error is not important, the capacitor can be left off the PCB. For more detailed information, order Motorola Application Note AN1579/D.

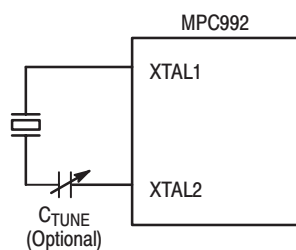


Figure 2. Recommended Crystal Interface

Table 15. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150ppm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω max
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

Power Supply Filtering

The MPC992 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC992 provides separate power supplies for the digital circuitry (V_{CC1}) and the internal PLL (V_{CCA}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC992.

Figure 3 illustrates a typical power supply filter scheme. The MPC992 is most susceptible to noise with spectral content in the 10kHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the MPC992. From the data sheet the $I_{V_{CCA}}$ current (the current sourced through the V_{CCA} pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the V_{CCA} pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 3 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

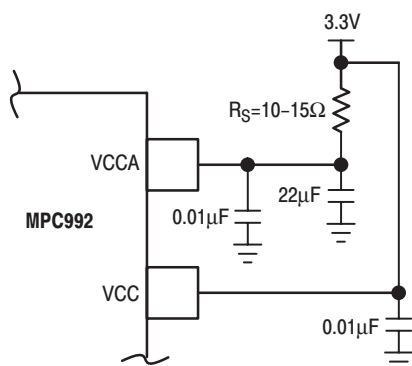


Figure 3. Power Supply Filter

A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000μH choke will show a significant impedance at 10KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the VCCA pin a low DC resistance inductor is required (less than 15Ω). Generally the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering.

The MPC992 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. The important aspect of the layout for the MPC992 is low impedance connections between VCC and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantane-

ous switching current for the MPC992 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

No active signal lines should pass below the crystal interface to the MPC992. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator. In addition, the crystal interface circuitry will be adversely affected by activity on the PECL_CLK inputs. Therefore, it is recommended that the PECL input signals be static when the crystal oscillator circuitry is being used.

Although the MPC992 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Low Voltage PLL Clock Driver

The MPC9952 is a 3.3V compatible, PLL based clock driver device targeted for high performance clock tree applications. The device features a fully integrated PLL with no external components required. With output frequencies of up to 180MHz and eleven low skew outputs the MPC9952 is well suited for high performance designs. The device employs a fully differential PLL design to optimize jitter and noise rejection performance. Jitter is an increasingly important parameter as more microprocessors and ASIC's are employing on chip PLL clock distribution.

- Fully Integrated PLL
- Output Frequency up to 180MHz
- High Impedance Disabled Outputs
- Compatible with **PowerPC™**, Intel and High Performance RISC Microprocessors
- Output Frequency Configurable
- LQFP Packaging
- ± 100 ps Cycle-to-Cycle Jitter

The MPC9952 features three banks of individually configurable outputs. The banks contain 5 outputs, 4 outputs and 2 outputs. The internal divide circuitry allows for output frequency ratios of 1:1, 2:1, 3:1 and 3:2:1. The output frequency relationship is controlled by the fsel frequency control pins. The fsel pins as well as the other inputs are LVCMOS/LVTTL compatible inputs.

The MPC9952 uses external feedback to the PLL. This features allows for the use of the device as a "zero delay" buffer. Any of the eleven outputs can be used as the feedback to the PLL. The VCO_Sel pin allows for the choice of two VCO ranges to optimize PLL stability and jitter performance. The MR/OE pin allows the user to force the outputs into high impedance for board level test.

For system debug the PLL of the MPC9952 can be bypassed. When forced to a logic HIGH, the PLEN input will route the signal on the RefClk input around the PLL directly to the internal dividers. Because the signal is routed through the dividers, it may take several transitions of the RefClk to affect a transition on the outputs. This features allows a designer to single step the design for debug purposes.

The outputs of the MPC9952 are LVCMOS outputs. The outputs are optimally designed to drive terminated transmission lines. For applications using series terminated transmission lines each MPC9952 output can drive two lines. This capability provides an effective fanout of 22, more than enough clocks for most clock tree designs. For more information on driving transmission lines consult the applications section of this data sheet.

MPC9952

See Upgrade Product – MPC9352

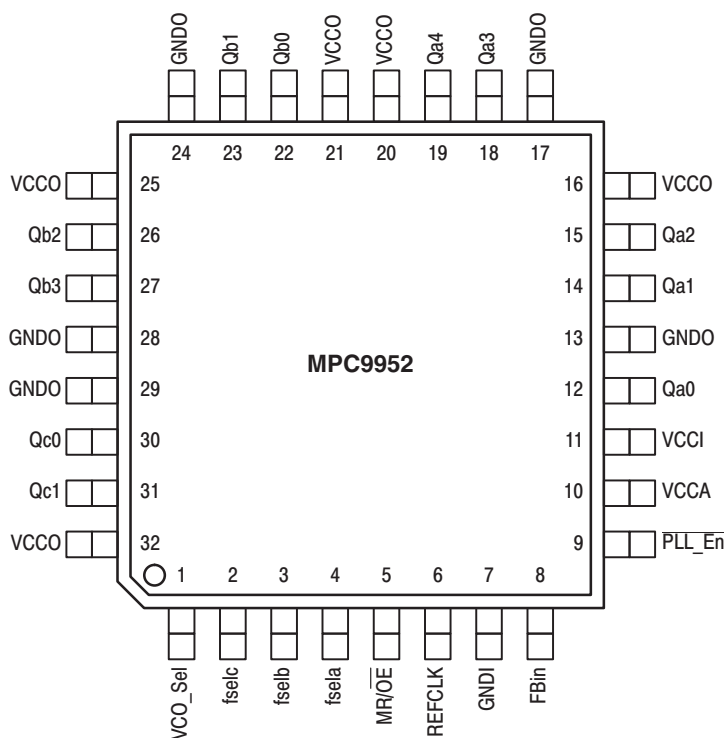
LOW VOLTAGE PLL CLOCK DRIVER



FA SUFFIX
LQFP PACKAGE
CASE 873A-02

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Rev 2



FUNCTION TABLES

fsela	Qan	fselb	Qbn	fselc	Qcn
0	+4	0	+4	0	+2
1	+6	1	+2	1	+4

Control Pin	Logic '0'	Logic '1'
VCO_Sel	fVCO	fVCO/2
MR/OE	Output Enable	High Z
PLL_En	Enable PLL	Disable PLL

Pin Name	Description
VCCA	PLL Power Supply
VCCO	Output Buffer Power Supply
VCCI	Internal Core Logic Power Supply
GNDI	Internal Ground
GNDO	Output Buffer Ground

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	4.6	V
V_I	Input Voltage	-0.3	$V_{CC} + 0.3$	V
I_{IN}	Input Current		± 20	mA
T_{Stor}	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

THERMAL CHARACTERISTICS

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CCO} = V_{CCI} = V_{CCA} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		3.6	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -20\text{mA}$ (Note 1.)
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 20\text{mA}$ (Note 1.)
I_{IN}	Input Current			± 120	μA	Note 2.
C_{IN}	Input Capacitance		2.7	4.0	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	
I_{CC}	Maximum Quiescent Supply Current			160	mA	Total ICC Static Current
I_{CCA}	PLL Supply Current		15	20	mA	

1. The MPC9952 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CCO}/2$) transmission lines on the incident edge (see Applications Info section).
2. Inputs have pull-up, pull-down resistors which affect input current.

PLL INPUT REFERENCE CHARACTERISTICS ($T_A = 0$ to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency		100	MHz	Note 3.
f_{refDC}	Reference Input Duty Cycle	25	75	%	

3. Maximum and minimum input reference is limited by the VCO lock range and the feedback divider.

AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time (Note 4.)	0.10		1.0	ns	0.8 to 2.0V
t_{pw}	Output Pulse Width (Note 4.)	$t_{CYCLE}/2 - 750$	$t_{CYCLE}/2 \pm 500$	$t_{CYCLE}/2 + 750$	ps	
t_{os}	Output-to-Output Skew (Note 4.)			350 450 550	ps	Same Frequencies Same Frequencies Different Frequencies
f_{VCO}	PLL VCO Lock Range	200		480	MHz	Note 6.
f_{max}	Maximum Output Frequency	180 120 80			MHz	Note 4.
						Qc,Qb (+2) Qa,Qb,Qc (+4) Qa (+6)
t_{pd}	REFCLK to FBIN Delay	-200	0	200	ps	Notes 4., 5.
t_{PLZ}, t_{PHZ}	Output Disable Time	2		8	ns	Note 4.
t_{PZL}, t_{PLH}	Output Enable Time	2		10	ns	Note 4.
$t_{jit(cc)}$	Cycle-to-Cycle Jitter		± 100		ps	
t_{lock}	Maximum PLL Lock Time			10	ms	

4. Termination of 50Ω to $V_{CCO}/2$.

5. t_{pd} is specified for 50MHz input ref, the window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The t_{pd} does not include jitter.

6. The PLL may be unstable with a divide by 2 feedback ratio.

APPLICATIONS INFORMATION**Driving Transmission Lines**

The MPC9952 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 7Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091.

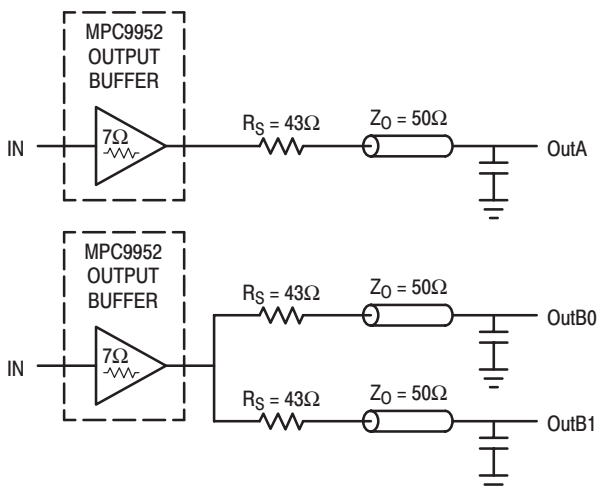


Figure 3. Single versus Dual Transmission Lines

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated

transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CCO}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9952 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fan-out of the MPC9952 clock driver is effectively doubled due to its capability to drive multiple lines.

The waveform plots of Figure 4 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC9952 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9952. The output waveform in Figure 4 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_o / R_s + R_o + Z_o) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

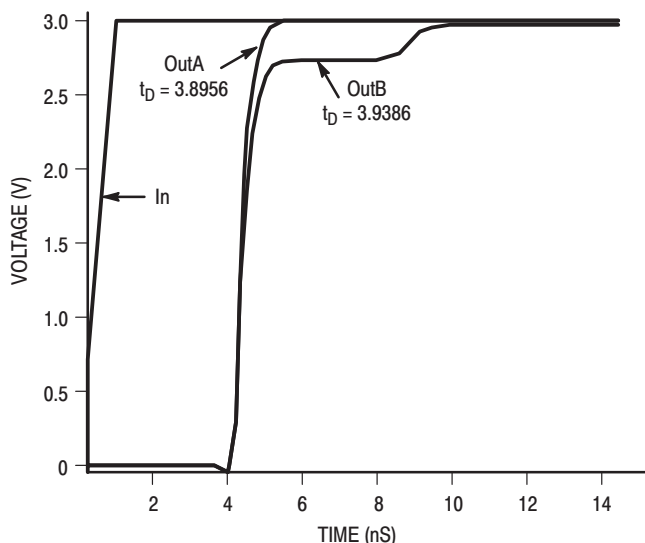


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

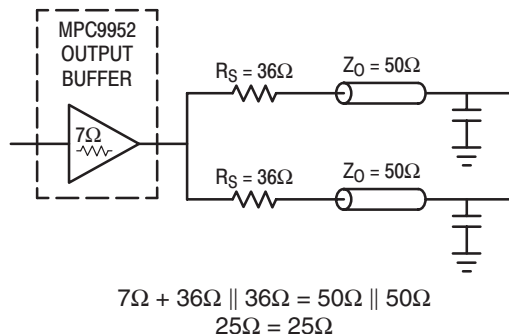


Figure 5. Optimized Dual Line Termination

Power Supply Filtering

The MPC9952 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC9952 provides separate power supplies for the output buffers (V_{CCO}) and the internal PLL

(V_{CCA}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC9952.

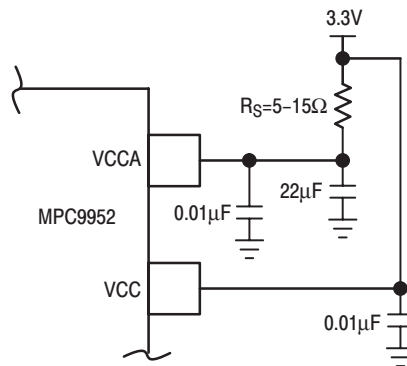


Figure 6. Power Supply Filter

Figure 6 illustrates a typical power supply filter scheme. The MPC9952 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the MPC9952. From the data sheet the I_{VCCA} current (the current sourced through the V_{CCA} pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.3V – 5% must be maintained on the V_{CCA} pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 6 must have a resistance of 5–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC9952 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Product Preview

Low Voltage PLL Clock Driver

The MPC9990 is a low voltage PLL clock driver designed for high speed clock generation and distribution in high performance computer, workstation and server applications. The clock driver accepts a LVPECL compatible clock signal and provides 10 low skew, differential HSTL¹ compatible outputs, one HSTL compatible output for system synchronization purposes and one HSTL compatible PLL feedback output. The device operates from a dual voltage supply: 3.3 V for the core logic and 1.8 V for the HSTL outputs. The fully integrated PLL supports an input frequency range of 75 to 287.5 MHz. The output frequencies are configurable.

- Supports high performance HSTL clock distribution systems
- Compatible to IA64 processor systems
- Fully Integrated PLL, differential design
- Core logic operates from 3.3 V power supply
- HSTL outputs operate from a 1.8 V supply
- Programmable frequency by output bank
- 10 HSTL compatible outputs (two banks)
- HSTL compatible PLL feedback output
- HSTL compatible synchronization output (QSYNC)
- Max. skew of 80 ps within output bank
- Zero-delay capability: max. SPO (tpd) window of 150 ps
- LVPECL compatible clock input, LVCMOS compatible control inputs
- Temperature range of 0 to +70°C

The MPC9990 provides output clock frequencies required for high-performance computer system optimization. The device drives up to 10 differential clock loads within the frequency range of 75 to 287.5 MHz. The 10 outputs are organized in 2 banks of 3 and 7 differential outputs. In the standard configuration the QFB output pair is connected to the FB input pair closing the PLL loop and enabling zero delay operation from the CLK input to the outputs. Bank B outputs are frequency and phase aligned to the CLK input, providing exact copies of the high-speed input signal. Bank A outputs are configured to operate at slower speeds driving the system bus devices. The output frequency ratio of bank A to bank B is adjustable (for available ratios, see "MPC9990 Application: CPU to System Bus Frequency Ratios" on page 288) for system optimization. In a computer application, bank B outputs generate the clock signals for the devices operating at the CPU frequency, while Bank A outputs are configured to drive the clock signals for the devices running at lower speeds (system clock). Four individual frequency ratios are available, providing a high degree of flexibility. The frequency ratios between CPU clock and system clock provided by the MPC9990 are listed in the table "Output configuration" on page 290.

The QSYNC output functionality is designed for system synchronization purpose. QSYNC is asserted at coincident rising edges of CPU (bank B and QFB signal) and slower system clock (bank A) outputs (see "QSYNC Phase Relation Diagram" on page 290), providing baseline timing in systems with fractional clocks. The QSYNC output is asserted for one QFB high pulse, centered on the rising QFB output.

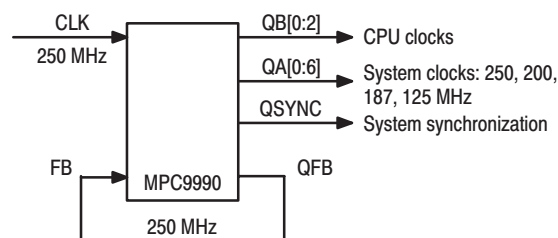


Figure 1. MPC9990 Application Example

1. In order to minimize output-to-output skew, HSTL outputs of the MPC9990 are generated with an open emitter architecture. For output termination, see "HSTL Output Termination and AC Test Reference" on page 291.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MPC9990

**LOW VOLTAGE
DIFFERENTIAL PECL-HSTL
PLL CLOCK DRIVER**



FA SUFFIX
48-LEAD LQFP PACKAGE
CASE 932

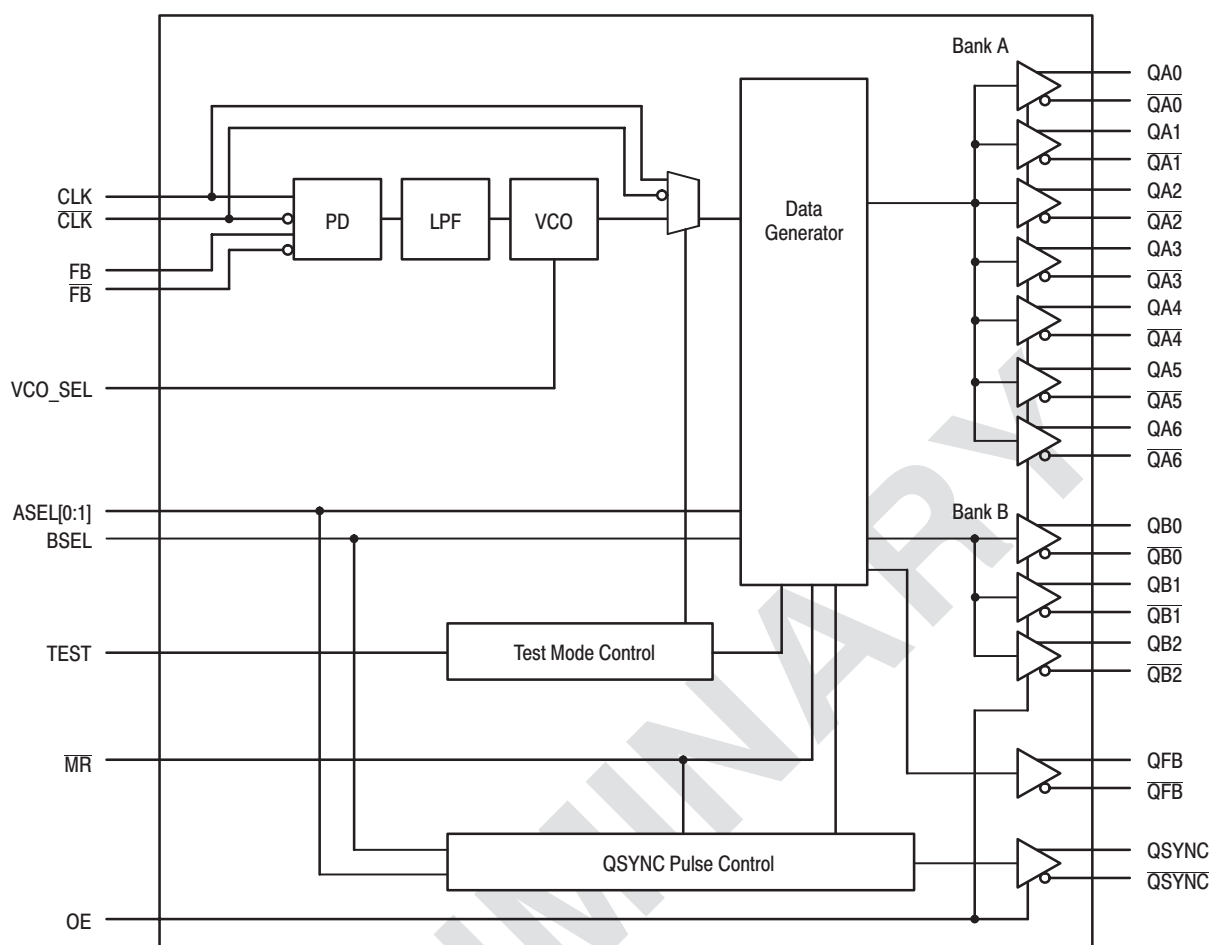


Figure 2. MPC9990 Logic Diagram

Table 1: MPC9990 Application: CPU to System Bus Frequency Ratios

QA to QB frequency ratio	1:1	1:2	3:4	4:5	
Output frequencies for CLK = 75 MHz (BSEL=1, VCO_SEL=1)					
QA output frequency	75	37.5	56.25	60	MHz
QB output frequency	75	75	75	75	MHz
Output frequencies for CLK = 100 MHz (BSEL=1, VCO_SEL=1)					
QA output frequency	100	50	75	80	MHz
QB output frequency	100	100	100	100	MHz
Output frequencies for CLK = 125 MHz (BSEL=1, VCO_SEL=1)					
QA output frequency	125	62.5	93.75	100	MHz
QB output frequency	125	125	125	125	MHz
Output frequencies for CLK = 150 MHz (BSEL=1, VCO_SEL=0)					
QA output frequency	150	75	112.5	120	MHz
QB output frequency	150	150	150	150	MHz
Output frequencies for CLK = 200 MHz (BSEL=1, VCO_SEL=0)					
QA output frequency	200	100	150	160	MHz
QB output frequency	200	200	200	200	MHz
Output frequencies for CLK = 250 MHz (BSEL=1, VCO_SEL=0)					
QA output frequency	250	125	187.5	200	MHz
QB output frequency	250	250	250	250	MHz

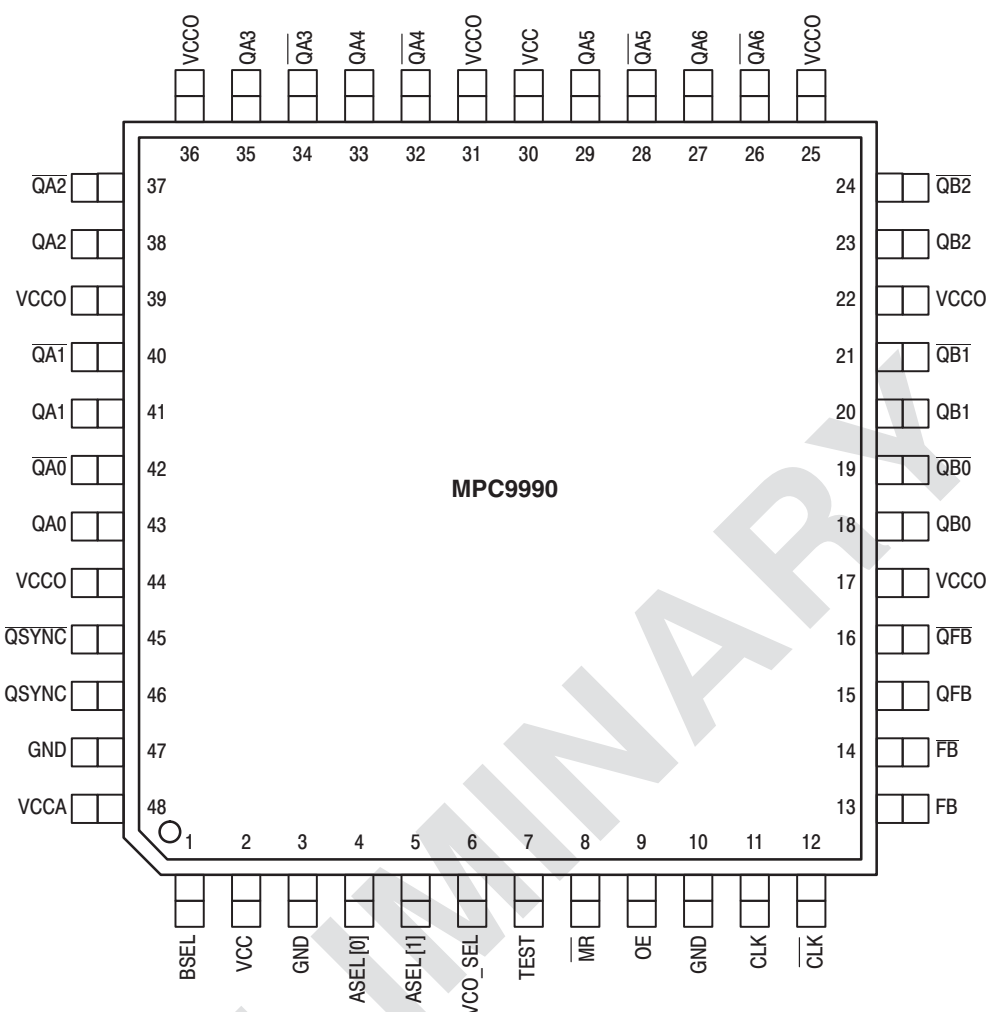


Figure 3. 48-Lead Package Pinout (Top View)

Table 2: Pin configuration

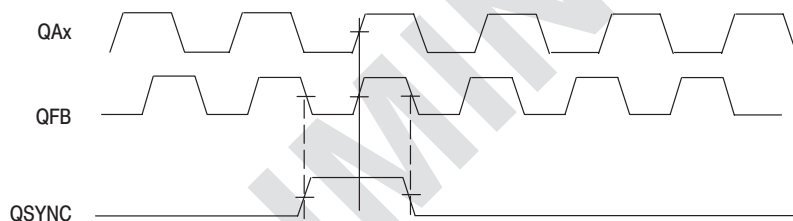
Pin	I/O	Type	Internal resistor	Description
CLK, $\overline{\text{CLK}}$	Input	LVPECL	CLK: pull-down, $\overline{\text{CLK}}$: pull-up	Differential clock frequency input
FB, $\overline{\text{FB}}$	Input	HSTLL	FB: pull-down, $\overline{\text{FB}}$: pull-up	Differential feedback input
QAn, $\overline{\text{QAn}}$	Output	HSTL		Bank A outputs
QBn, $\overline{\text{QBn}}$	Output	HSTL		Bank B outputs
QSYNC, $\overline{\text{QSYNC}}$	Output	HSTL		Synchronization output
QFB, $\overline{\text{QFB}}$	Output	HSTL		Differential feedback output
VCO_SEL	Input	LVC MOS	pull-down	Selection of operating frequency range
ASEL[0:1]	Input	LVC MOS	pull-down	Selection of bank A output frequency
BSEL	Input	LVC MOS	pull-down	Selection of bank B output frequency
TEST	Input	LVC MOS	pull-down	Selection of PLL operation or TEST mode (PLL bypass)
MR	Input	LVC MOS	pull-up	Master reset. Assertion of master reset required on startup
OE	Input	LVC MOS	pull-up	Output enable
VCCA		Power supply		Analog power supply, typical 3.3 V
VCC		Power supply		Core power supply, typical 3.3 V
VCCO		Power supply		Output power supply, typical 1.8 V
GND		Ground		Output, analog and core logic ground, 0V (VEE)

Table 3: Output Frequency Relationship for an Example Configuration

ASEL[0]	ASEL[1]	BSEL	f QAn	f QBn	f QFB	QSYNC
0	0	0	CLK	CLK	CLK	L
0	1	0	$\text{CLK} \div 2$	$\text{CLK} \div 2$	CLK	enabled
1	0	0	$\text{CLK} \times 3 \div 4$	$\text{CLK} \times 3 \div 4$	CLK	enabled
1	1	0	$\text{CLK} \times 4 \div 5$	$\text{CLK} \times 4 \div 5$	CLK	enabled
0	0	1	CLK	CLK	CLK	L
0	1	1	$\text{CLK} \div 2$	CLK	CLK	enabled
1	0	1	$\text{CLK} \times 3 \div 4$	CLK	CLK	enabled
1	1	1	$\text{CLK} \times 4 \div 5$	CLK	CLK	enabled

Table 4: Function Table (Controls)

Control Pin	0	1
TEST	PLL enabled	PLL bypassed (Static test mode)
MR	Reset (Internal logic and PLL)	Normal operation mode
OE	Outputs disabled ($Q_X = L$, $\bar{Q}_X = H$), except QFB, QFB	Outputs enabled
VCO_SEL	High frequency operation (VCO frequency range from 600 to 1150 MHz)	Low frequency operation (VCO frequency range from 300 to 575 MHz)

**Figure 4. QSYNC Phase Relation Diagram**

The MPC9990 QSYNC output is designed for system synchronization purpose. The output frequency relationship between the QA-bank and the QFB-output (see table 3) controls the status of QSYNC. The internal QSYNC pulse circuitry is enabled if the frequency relationship between the QA-banks and QFB is not an integer multiple of each other ($f_{QA}:f_{QFB} = 1:2, 3:4$ and $4:5$) (see table 3). QSYNC is asserted (logic high pulse) centered on coincident rising edges at the QA-bank outputs and QFB. The QSYNC output transitions at the falling edges of QFB (assertion at the last falling edge of QFB prior to

the coincident edge event, deassertion at the next falling edge of QFB). The QSYNC output pulse width is equal to period of the QFB output (see figure 4, also see the max. skew specification QFB to QSYNC).

If BSEL=1 and the PLL is frequency and phase locked, QSYNC output pulses occur centered on coincident edges between the QA-bank and QB-bank outputs (offset by the feed-back path delay) due to the fixed relationship between CLK, QFB and QB bank outputs.

Table 5: ABSOLUTE MAXIMUM RATINGS*

Symbol	Characteristics	Min	Max	Units	Condition
V_{CCA}	Analog power supply	-0.5	3.6	V	
V_{CC}	Core power supply	-0.5	3.6	V	
V_{CCO}	Output power supply	-0.5	3.6	V	
V_{IN}	Input voltage	-0.5	$V_{CC} + 0.3$	V	
I_{IN}	Input current	-1.0	1.0	mA	DC
I_{OUT}	Output current	-50	50	mA	DC
T_S	Storage temperature	-50	150	°C	

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6: DC CHARACTERISTICS ($V_{CC} = V_{CCA} = 3.3 \text{ V} \pm 5\%$, $V_{CCO} = 1.7 \text{ to } 2.1 \text{ V}$, $T_A = 0^\circ \text{ to } 70^\circ \text{C}$)

Symbol	Characteristics	0 °C			25 °C			70 °C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
HSTL I/O ^a												
V _{CCO}	Output power supply	1.7	1.8	2.1	1.7	1.8	2.1	1.7	1.8	2.1		
V _{IN}	Input voltage (FB)	-0.3		1.45	-0.3		1.45	-0.3		1.45	V	Differential
V _{DIF}	Differential input voltage ^b (FB)	0.2		1.75	0.2		1.75	0.2		1.75	V	Differential
V _{CM}	Common mode input voltage ^c (FB)	0.64		0.9	0.68		0.9	0.68		1.0	V	
V _{OH}	Output high voltage	1.0	V _X +0.4	1.4	1.0	V _X +0.4	1.4	1.0	V _X +0.4	1.4	V	
V _{OL}	Output low voltage	0	V _X -0.4	0.4	0	V _X -0.4	0.4	0	V _X -0.4	0.4	V	
LVPECL I/O												
V _{CC}	Power supply voltage (core)	3.135	3.3	3.465	3.135	3.3	3.465	3.135	3.3	3.465	V	
V _{CCA}	Power supply voltage (PLL)	3.135	3.3	3.465	3.135	3.3	3.465	3.135	3.3	3.465	V	
V _{PP}	Peak-to-peak input voltage CLK, PCLK	500		1000	500		1000	500		1000	mV	
V _{CMR}	Common Mode Range ^d CLK, PCLK	V _{CC} -1.4		V _{CC} -0.6	V _{CC} -1.4		V _{CC} -0.6	V _{CC} -1.4		V _{CC} -0.6	V	
I _{IH}	Input high current			±150			±150			±150	μA	
I _{CC}	Power supply current (core)		141	180		141	180		141	180	mA	
I _{CCA}	Power supply current (PLL)		15	20		15	20		15	20	mA	
LVCMOS Inputs												
V _{IH}	Input high voltage	2		V _{CC}	2		V _{CC}	2		V _{CC}	V	
V _{IL}	Input low voltage	0		0.8	0		0.8	0		0.8	V	
I _I	Input current			±100			±100			±100	μA	

- a. See "HSTL Differential Input Levels" in Figure 5
b. V_{DIF} specifies the input differential voltage.
c. V_{CM} is the maximum allowable range of $V_{TR} - ((V_{TR} - V_{CP})/2)$. V_{TR} is true input signal, V_{CP} is its complementary input signal.
d. V_{CMR} is the difference from V_{CC} and the crosspoint of the differential input signal. Normal operation is obtained when the "high" input is within the V_{CMR} range and the input swing lies within the V_{PP} specification.
e. LVPECL input level specifications will vary 1:1 with V_{CC} .

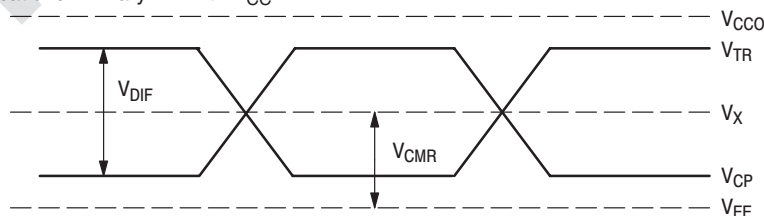
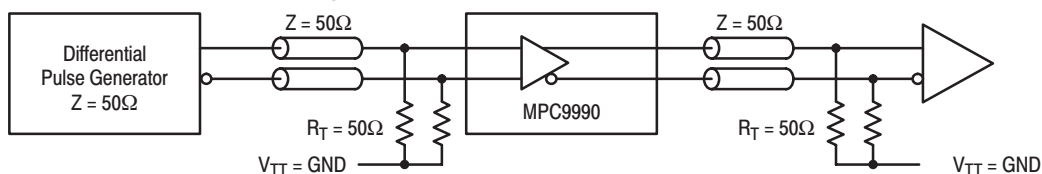
**Figure 5. HSTL Differential Input Levels****Figure 6. HSTL Output Termination and AC Test Reference**

Table 7: AC CHARACTERISTICS ($V_{CCI} = V_{CCA} = 3.3 \text{ V} \pm 5\%$, $V_{CCO} = 1.7 \text{ to } 2.1 \text{ V}$, $T_A = 0^\circ \text{ to } 70^\circ \text{C}$)^a

Symbol	Characteristics	0°C			25°C			70°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{IN}	Input frequency ^b for VCO_SEL = 0 (high range)											
	1:1 ratio, ASEL=00	150.0		287.5	150.0		287.5	150.0		287.5	MHz	600 <
	1:2 ratio, ASEL=01	150.0		287.5	150.0		287.5	150.0		287.5	MHz	$f_{VCO} <$
	3:4 ratio, ASEL=10	200.0		287.5	200.0		287.5	200.0		287.5	MHz	1150
	4:5 ratio, ASEL=11	150.0		287.5	150.0		287.5	150.0		287.5	MHz	MHz
	Input frequency ^b for VCO_SEL = 1 (low range)											
	1:1 ratio, ASEL=00	75.0		143.75	75.0		150.0	75.0		150.0	MHz	300 <
	1:2 ratio, ASEL=01	75.0		143.75	75.0		150.0	75.0		150.0	MHz	$f_{VCO} <$
	3:4 ratio, ASEL=10	100.0		191.67	100.0		191.6	100.0		191.6	MHz	575 MHz
	4:5 ratio, ASEL=11	75.0		143.75	75.0		150.0	75.0		150.0	MHz	
f_{VCO}	VCO frequency											
	VCO_SEL = 0 (high range)	600		1150	600		1150	600		1150	MHz	
	VCO_SEL = 1 (low range)	300		575	300		575	300		575	MHz	
f_{OUT}	Output frequency ^c			287.5			287.5			287.5	MHz	
SPO	Static phase offset, t_{PD} between CLK and FB											
	VCO_SEL=0	-200		-50	-200		-50	-200		-50	ps	
	VCO_SEL=1	-250		-50	-250		-50	-250		-50	ps	
DC	Output duty cycle	45	50	55	45	50	55	45	50	55	%	
t_{SK}	Differential output skew											
	$t_{SK(OB)}$ within bank ^d			80			80			80	ps	Diff. HSTL outputs
	$t_{SK(O)}$ single frequency ^e			100			100			100	ps	
	$t_{SK(O)}$ multiple frequency ^f			250			250			250	ps	
	$t_{SK(OFB)}$ QFB to QA0-6											
	for ASEL=00	85		-115	85		-115	85		-115	ps	
	for ASEL=01	25		-175	25		-175	25		-175	ps	
	for ASEL=10	135		-115	135		-115	135		-115	ps	
	for ASEL=11	65		-135	65		-135	65		-135	ps	
	$t_{SK(O)}$ QFB to QSYNC	-500		500	-500		500	-500		500	ps	
V_{PP}^g	Minimum input swing	0.5		1	0.5		1	0.5		1	V	LVPECL
V_{CMR}	Common mode range	1		$V_{CC}-0.4$	1		$V_{CC}-0.4$	1		$V_{CC}-0.4$	V	LVPECL
$V_{DIF,OUT}$	Minimum output swing	0.6	0.8		0.6	0.8		0.6	0.8		V	HSTL
V_X	Differential output crosspoint voltage	0.64		0.9	0.68		0.9	0.68		1.0	V	HSTL
$t_{JIT(CC)}$	Cycle-to-cycle jitter											
	$f_{VCO} \geq 750 \text{ MHz}$			75			75			75	ps	
	$f_{VCO} < 750 \text{ MHz}$			125			125			125	ps	
$t_{JIT(PER)}$	Period Jitter											
	VCO_SEL=0			75			75			75	ps	
	VCO_SEL=1			125			125			125	ps	
$t_{JIT(IO)}$	I/O Phase Jitter RMS (1 σ)											
	600 MHz < f_{VCO} < 750 MHz			50			50			50	ps	
	750 MHz < f_{VCO} < 900 MHz			40			40			40	ps	
	900 MHz < f_{VCO} < 1150 MHz			30			30			30	ps	
BW	PLL bandwidth											
	1:1 ratio, ASEL=00		0.6-1.0			0.6-1.0			0.6-1.0		MHz	
	1:2 ratio, ASEL=01		0.6-1.0			0.6-1.0			0.6-1.0		MHz	
	3:4 ratio, ASEL=10		1.0-1.2			1.0-1.2			1.0-1.2		MHz	
	4:5 ratio, ASEL=11		0.6-1.0			0.6-1.0			0.6-1.0		MHz	
t_r, t_f	Output transition rate	0.8		2	0.8		2	0.8		2	V/ns	
t_{Lock}	PLL lock time			10			10			10	ms	

a. Refer to "HSTL Output Termination and AC Test Reference" for AC test conditions in Figure 6

b. The input frequency for the output configurations are limited by the VCO frequency range and the feedback divider.

c. f_{OUT} at which output-to-output skew, V_X and DC specification are still meet. f_{OUT} is primary a function of f_{IN} and the input-to-output frequency ratio (M:N).

d. Output skew within bank A outputs (QA0-QA6) and output skew within bank B outputs (QB0-QB2).

e. Output skew within all outputs (QA0-QA6, QB0-QB2) running at the same output frequency.

f. Output skew within all outputs (QA0-QA6, QB0-QB2) running at any output frequency.

g. V_{PP} specifies the minimum input differential voltage required for switching.

APPLICATIONS INFORMATION

Using the MPC9990 in zero-delay applications

Nested clock trees are typical applications for the MPC9990. Designs using the MPC9990 as PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from static fanout buffers. The external feedback option of the MPC9990 clock driver allows for its use as a zero delay buffer. By using the differential QFB output pair as a feedback to the PLL the propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input (CLK) and any output. This effective delay consists of the static phase offset (SPO), I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of part-to-part skew

The MPC9990 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9990 are connected together, the maximum overall timing uncertainty from the common CLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD, LINE(FB)} + t_{JIT(PER)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset (SPO), output skew, feedback board trace delay and I/O phase and period jitter. The output skew ($t_{SK(O)}$) specification of the MPC9990 is different for single or for dual frequency bank configurations. :

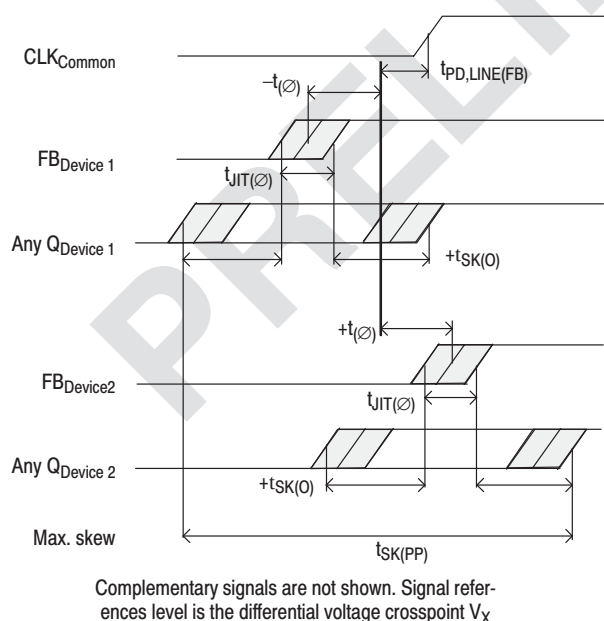


Figure 7. MPC9990 max. device-to-device skew

Due to the statistical nature of I/O jitter a rms value (1σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

Table 8: Confidence Factor CF

CF	Probability of clock edge within the distribution
$\pm 1\sigma$	0.68268948
$\pm 2\sigma$	0.95449988
$\pm 3\sigma$	0.99730007
$\pm 4\sigma$	0.99993663
$\pm 5\sigma$	0.99999943
$\pm 6\sigma$	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% ($\pm 3\sigma$) and single frequency configuration is assumed, resulting in a worst case timing uncertainty from input to any output of -495 ps to +245 ps relative to CLK.

$$t_{SK(PP)} = [-200ps...-50ps] + [-100ps...100ps] + [-75ps...75ps] + [(30ps \cdot -3)...(30ps \cdot 3)] + t_{PD, LINE(FB)}$$

$$t_{SK(PP)} = [-495ps...+245ps] + t_{PD, LINE(FB)}$$

Due to the frequency dependence of the I/O jitter, Figure 8 “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis. The number for the I/O jitter at a specific frequency can be substituted for the more general datasheet specification number:

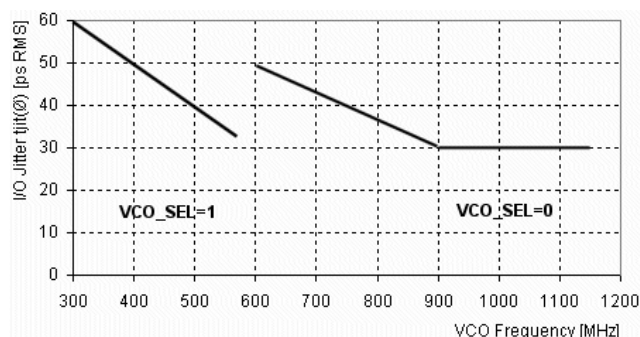
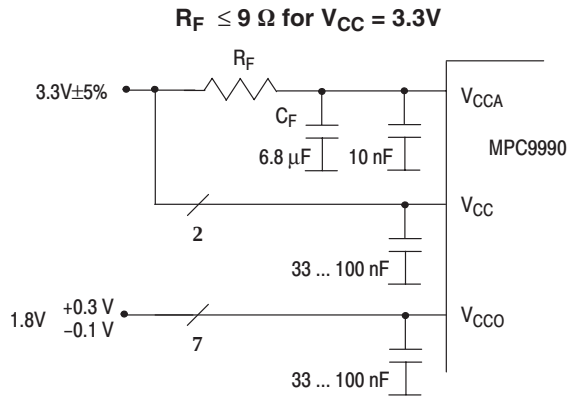


Figure 8. Max. I/O Jitter versus frequency

Power Supply Filtering

The MPC9990 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply. Random noise on the V_{CCA} power supply impacts the device AC characteristics, for instance I/O jitter. The MPC9990 provides separate power supplies for the output buffers (V_{CCO}) and the phase-locked loop (V_{CCA}) of the device.



Place V_{CCA} filter and V_{CCO} , V_{CC} bypass capacitors as close as possible to the device

Figure 9. Recommended Power Supply Filter

The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is difficult to minimize noise on the power supplies a second level of isolation may be required. A simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC9990. Figure 9 illustrates a recommended power supply low-pass frequency filter scheme. The MPC9990 VCO frequency and phase stability is most susceptible to noise with spectral content in the 300 kHz to 3 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F . The maximum voltage drop on V_{CCA} that can be tolerated is 135 mV with respect to $V_{CC} = 3.3V \pm 5\%$, resulting in a lowest allowable supply voltage for V_{CCA} equal to 2.835 V.

From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 11 mA (15 mA maximum), assuming that the minimum of 3.0V ($V_{CC}=3.3V-5\%-0.135V$) must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 9 “Recommended Power Supply Filter” should have a

maximum resistance of 9Ω to meet the voltage drop criteria. The minimum resistance for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater 40 dB for noise whose spectral content is above 300 kHz. In the example RC filter shown in Figure 9 “Recommended Power Supply Filter”, the filter cut-off frequency is 16.3 kHz and the noise attenuation at 300 kHz is approximately 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ($6.8 \mu F \parallel 10 \text{ nF}$) ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9990 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds, internal voltage regulation and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Recommended Power-up Sequence

The MPC9990 does not require any special supply ramp sequence in case the system provides all supply voltages (3.3V and 1.8V) at the same time. The reference clock signal (CLK, $\overline{\text{CLK}}$) can be applied any time during or after the power up sequence if V_{IN} is smaller or equal V_{CC} during the voltage transition. Following are guidelines for the MPC9990 power-up sequence in case the 3.3V and 1.8V voltage supply cannot be applied at the same time:

- HSTL output supply voltage V_{CCO} must be powered up to the specified voltage range before or at the same time as V_{CC} . V_{CCA} can be powered up before, at the same time or after V_{CC} and V_{CCO} .
- At the time the power supplies are powered up, the device should be reset ($\overline{\text{MR}}=0$).
- Apply the clock input signals to the PLL (CLK, $\overline{\text{CLK}}$) after all power supplies are stable. Then, $\overline{\text{MR}}$ can be deasserted ($\overline{\text{MR}}=1$). This will release the internal PLL which will attempt to lock.
- The time from $\overline{\text{MR}}$ deassertion to PLL lock will be specified by the PLL lock time t_{Lock} . After the PLL achieved lock, the AC characteristics are valid.
- Outputs can be enabled by OE any time. QFB is not affected by OE and the PLL can achieve lock even if OE is tied high (OE = 1, disable).

Calculating the Power Consumption

The total power dissipated in the MPC9990 (P_{TOT}) can be represented by this formula:

$$P_{TOT} = P_{CORE} + (N \cdot P_{OUTPUT})$$

where P_{CORE} is the core and PLL power consumption (V_{CC} and V_{CCA} pins), P_{OUTPUT} is the power consumption of the output drivers (V_{CCO} pins) and N is the number of terminated outputs:

$$P_{CORE} = V_{CC} \cdot I_{CC}$$

$$P_{OUTPUT} = (V_{CCO} - V_{OUT}) \cdot [(V_X - V_{TT}) \div R_{TERM}]$$

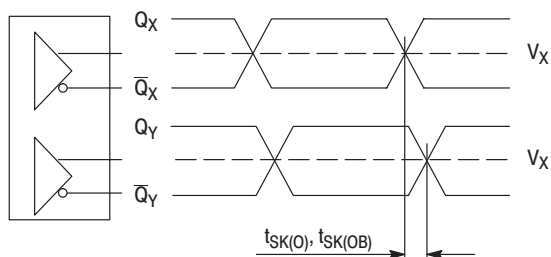
I_{CC} is the current consumption of the core including the current consumption of the PLL. V_X represents the average output voltage for a 50% duty cycle output signal. V_X and I_{CC} can be obtained from the specification values. V_{CC} , V_{CCO} , and the termination resistor R_{TERM} are application-dependent.

Table 9: Example Calculation

Term	Value (worst case)	Value (typical case)
V_{CC}	3.3V+5%	3.3V
I_{CCA}	180 mA	141 mA
P_{CORE}	624 mW	465 mW
V_{CCO}	2.1V	1.8V
V_{OUT}^b	0.68V	0.8V
V_X	0.9V	0.8V
V_{TT}	0V	0V
R_{TERM}	50Ω	50Ω
P_{OUTPUT}	25.5 mW	16 mW
N	24	24
P_{TOT}	1237 mW	849 mW

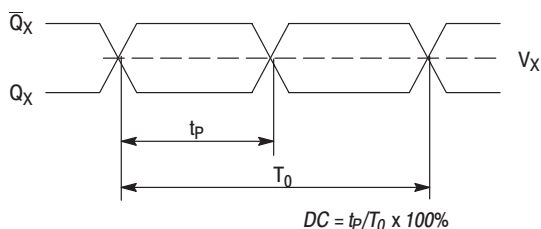
a. I_{CC} already includes I_{CCA} .

b. The value for V_{OUT} is average output voltage assuming the duty cycle of the output is approx. 50%.



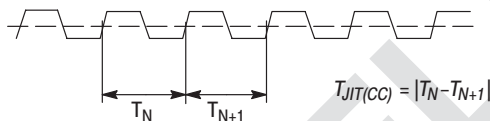
The pin-to-pin skew is defined as the worst case difference in propagation delay between any two similar delay path within a single device ($t_{SK(O)}$) or within a single output bank ($t_{SK(OB)}$)

Figure 10. Output-to-output Skew $t_{SK(O)}$, $t_{SK(OB)}$



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 12. Output Duty Cycle (DC)



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs, measured at an output (only true signal shown)

Figure 14. Cycle-to-cycle Jitter

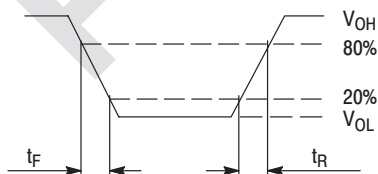


Figure 16. Output Transition Time Test Reference

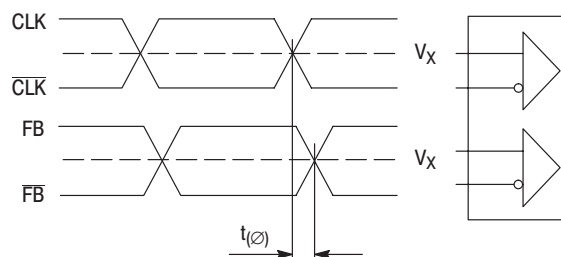
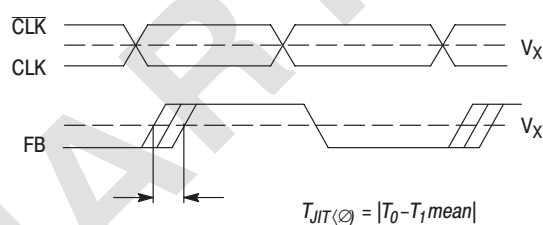
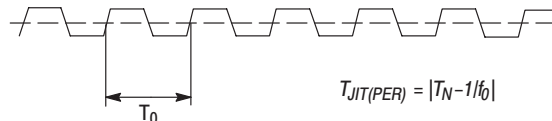


Figure 11. Propagation delay (t_O , static phase offset, SPO) test reference



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles, measured at the FB signal (only true signal shown)

Figure 13. I/O Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles (only true signal shown)

Figure 15. Period Jitter

3.3V Differential ECL/PECL PLL Clock Generator

The MPC9992 is a 3.3 V compatible, PLL based PECL clock driver. Using SiGe technology and a fully differential design ensures optimum skew and PLL jitter performance. The performance of the MPC9992 makes the device ideal for workstation, mainframe computer and telecommunication applications. With output frequencies up to 400 MHz and output skews less than 100 ps the device meets the needs of the most demanding clock applications. The MPC9992 offers a differential PECL input and a crystal oscillator interface. All control signals are LVCMOS compatible.

Features

- 7 differential outputs, PLL based clock generator
- SiGe technology supports minimum output skew (max. 100 ps)
- Supports up to two generated output clock frequencies with a maximum clock frequency up to 400 MHz
- Selectable crystal oscillator interface and PECL compatible clock input
- SYNC pulse generation
- PECL compatible differential clock inputs and outputs
- Single 3.3V (PECL) supply
- Ambient temperature range 0°C to +70°C
- Standard 32 lead LQFP package
- Pin and function compatible to the MPC992

Functional Description

The MPC9992 utilizes PLL technology to frequency lock its outputs onto an input reference clock. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. The MPC9992 features frequency programmability between the three output banks outputs as well as the output to input relationships. Output frequency ratios of 2:1, 3:1, 3:2 and 5:2 can be realized. The two banks of outputs and the feedback frequency divider can be programmed by the FSEL[2:0] pins of the device. The VCO_SEL pin provides an extended PLL input reference frequency range.

The SYNC pulse generator monitors the phase relationship between the QA[3:0] and QB[2:0] output banks. The SYNC generator output signals the coincident edges of the two output banks. This feature is useful for non binary relationships between output frequencies.

The REF_SEL pin selects the differential PECL compatible input pair or crystal oscillator interface as the reference clock signal. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The MPC9992 requires an external reset signal for start-up and for PLL recovery in case the reference input is interrupted. Assertion of the reset signal forces all outputs to the logic low state.

The MPC9992 is fully 3.3V compatible and requires no external loop filter components. The differential clock input (PCLK) is PECL compatible and all control inputs accept LVCMOS compatible signals while the outputs provide PECL compatible levels with the capability to drive terminated 50 Ω transmission lines.

The device is pin and function compatible to the MPC992 and is packaged in a 32-lead LQFP package.

MPC9992

**3.3V DIFFERENTIAL
ECL/PECL
PLL CLOCK GENERATOR**



FA SUFFIX
32 LEAD LQFP PACKAGE
CASE 873A

2

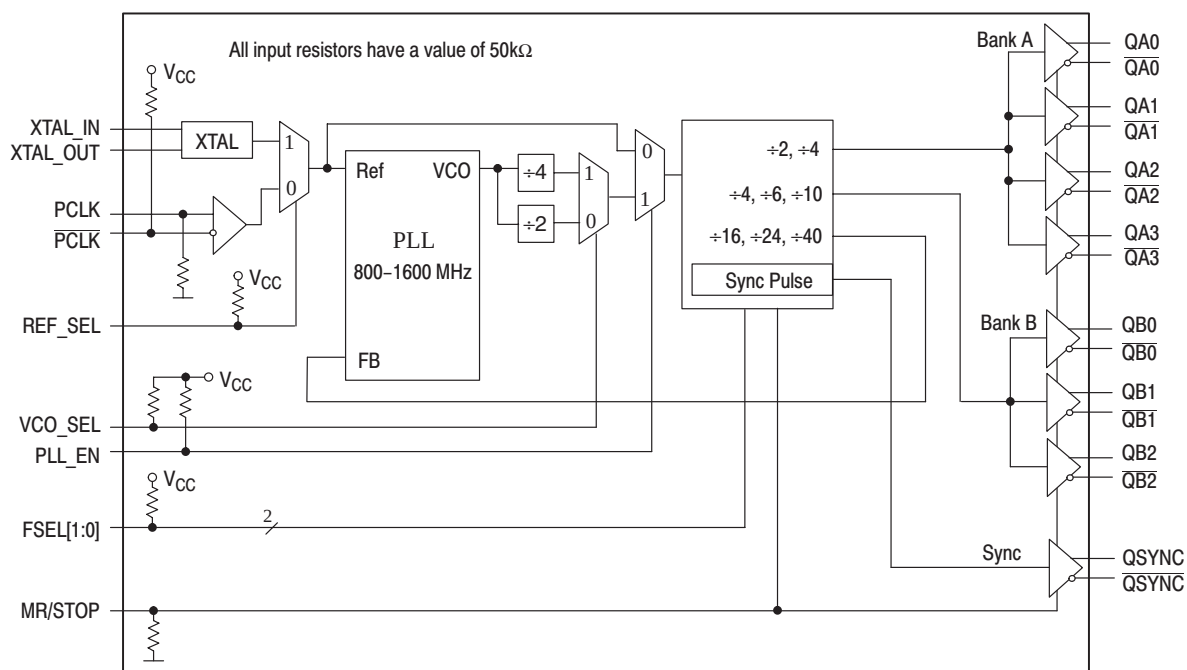


Figure 1. MPC9992 Logic Diagram

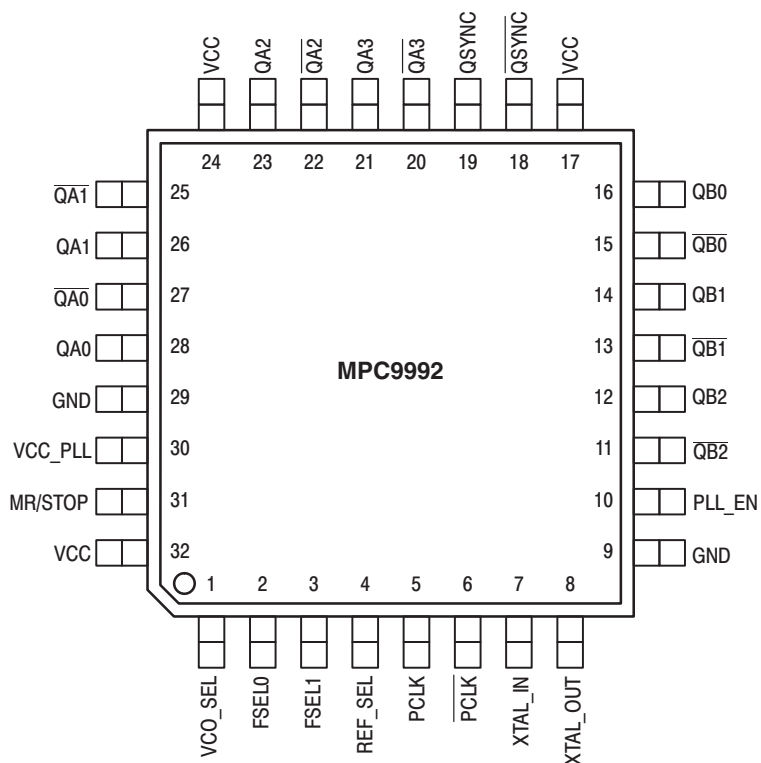


Figure 2. MPC9992 32-Lead Package Pinout (Top View)

Table 1: MPC9992 PLL Configurations

VCO_SEL	FSEL_0	FSEL_1	f _{REF} (MHz)	QA[3:0] (N _A)	QB[2:0] (N _B)	Frequency Ratio QA to QB	Internal Feedback (M · VCO_SEL)
0	0	0	16.6–33.3	VCO÷8 (6 · f _{REF})	VCO÷12 (4 · f _{REF})	3÷2	VCO÷48
0	0	1	25–50	VCO÷4 (8 · f _{REF})	VCO÷8 (4 · f _{REF})	2÷1	VCO÷32
0	1	0	10–20	VCO÷8 (10 · f _{REF})	VCO÷20 (4 · f _{REF})	5÷2	VCO÷80
0	1	1	16.6–33.3	VCO÷4 (12 · f _{REF})	VCO÷12 (4 · f _{REF})	3÷1	VCO÷48
1	0	0	8.3–16.6	VCO÷16 (6 · f _{REF})	VCO÷24 (4 · f _{REF})	3÷2	VCO÷96
1	0	1	12.5–25	VCO÷8 (8 · f _{REF})	VCO÷16 (4 · f _{REF})	2÷1	VCO÷64
1	1	0	5–10	VCO÷16 (10 · f _{REF})	VCO÷40 (4 · f _{REF})	5÷2	VCO÷160
1	1	1	8.3–16.6	VCO÷8 (12 · f _{REF})	VCO÷24 (4 · f _{REF})	3÷1	VCO÷96

Table 2: FUNCTION TABLE (Configuration Controls)

Control	Default	0	1
REF_SEL	1	Selects PCLK, PCLK̄ as PLL reference signal input	Selects the crystal oscillator as PLL reference signal input
VCO_SEL	1	Selects VCO÷2. The VCO frequency is scaled by a factor of 2 (high input frequency range)	Selects VCO÷4. The VCO frequency is scaled by a factor of 4 (low input frequency range).
PLL_EN	1	Test mode with the PLL bypassed. The reference clock is substituted for the internal VCO output. MPC9992 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Normal operation mode with PLL enabled.
MR/STOP	0	Normal operation	Reset of the device and output disable (output clock stop). The outputs are stopped in logic low state: Qx=L, Q̄x=H. The minimum reset period should be greater than one reference clock cycle.
VCO_SEL and FSEL[1:0] control the operating PLL frequency range and input/output frequency ratios. See Table 1 for the device frequency configuration.			

Table 3: PIN CONFIGURATION

Pin	I/O	Type	Function
PCLK, PCLK̄	Input	PECL	Differential reference clock signal input
XTAL_IN, XTAL_OUT		Analog	Crystal oscillator interface
VCO_SEL	Input	LVC MOS	VCO operating frequency select
PLL_EN	Input	LVC MOS	PLL Enable/Bypass mode select
REF_SEL	Input	LVC MOS	PLL reference signal input select
MR/STOP	Input	LVC MOS	Device reset and output clock disable (stop in logic low state)
FSEL[1:0]	Input	LVC MOS	Output and PLL feedback frequency divider select
QA[0-3], QĀ[0-3]	Output	PECL	Differential clock outputs (bank A)
QB[0-2], QB̄[0-2]	Output	PECL	Differential clock outputs (bank B)
QSYNC, QSYNC̄	Output	PECL	Differential clock outputs (bank C)
GND	Supply	GND	Negative power supply
VCC	Supply	VCC	Positive power supply. All V _{CC} pins must be connected to the positive power supply for correct DC and AC operation
VCC_PLL	Supply	VCC	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin VCC_PLL. Please see applications section for details

Table 4: ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	3.9	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} +0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} +0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5: GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output Termination Voltage		V _{CC} - 2		V	
MM	ESD Protection (Machine Model)	175			V	
HBM	ESD Protection (Human Body Model)	2000			V	
CDM	ESD Protection (Charged Device Model)	1000			V	
LU	Latch-Up Immunity	200			mA	
C _{IN}	Input capacitance		4.0		pF	Inputs
θ _{JA}	Thermal resistance junction to ambient JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ _{JC}	Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
T _J	Operating junction temperature ^a (continuous operation) MTBF = 9.1 years	0		110	°C	

a. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MPC9992 to be used in applications requiring industrial temperature range. It is recommended that users of the MPC9992 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 6: DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $GND = 0V$, $T_A = 0^{\circ}C$ to $70^{\circ}C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Differential PECL clock inputs (PCLK, PCLK) ^a						
V_{PP}	AC differential input voltage ^b	0.2		1.3	V	Differential operation
V_{CMR}	Differential cross point voltage ^c	1.0		$V_{CC}-0.3$	V	Differential operation
I_{IN}	Input Current ^d			± 120	μA	$V_{IN}=V_{CC}$ or GND
LVCMOS control inputs (VCO_SEL, PLL_EN, MR/STOP, REF_SEL, FSEL[1:0])						
V_{IH}	Input high voltage	2.0		$V_{CC} + 0.3$	V	LVCMOS
V_{IL}	Input low voltage			0.8	V	LVCMOS
I_{IN}	Input Current ^d			± 120	μA	$V_{IN}=V_{CC}$ or GND
PECL clock outputs (QA[3:0], QA[3:0], QB[2:0], QB[2:0], QSYNC, QSYNC)						
V_{OH}	Output High Voltage	$V_{CC}-1.025$		$V_{CC}-0.880$	V	$I_{OH} = -30 \text{ mA}^e$
V_{OL}	Output Low Voltage	$V_{CC}-1.920$		$V_{CC}-1.620$	V	$I_{OL} = -5 \text{ mA}$
Supply Current and voltage						
V_{CC_PLL}	PLL Supply Voltage	2.955		V_{CC}	V	V_{CC_PLL} pin
I_{CC_PLL}	Maximum PLL Supply Current		9.0	12	mA	V_{CC_PLL} pin
I_{GND}^f	Maximum Supply Current		80	110	mA	GND pins

a. Clock inputs driven by PECL compatible signals.

b. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.

c. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

d. Inputs have pull-down resistors affecting the input current.

e. Equivalent to a termination of 50Ω to V_{TT} .

f. Does not include output drive current which is dependant on output termination methods.

Table 7: AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $GND = 0V$, $T_A = 0^\circ C$ to $+70^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input reference frequency					
	+32 feedback	25.0		50.0	MHz	PLL locked
	+48 feedback	16.67		33.3	MHz	
	+64 feedback	12.5		25.0	MHz	
	+80 feedback	10.0		20.0	MHz	
	+96 feedback	8.33		16.67	MHz	
	+160 feedback	5.0		10.0	MHz	
	Input reference frequency in PLL bypass mode ^b			400	MHz	PLL bypass
f_{XTAL}	Crystal interface frequency range ^c	10		20	MHz	
f_{VCO}	VCO frequency range ^d	800		1600	MHz	
f_{MAX}	Output Frequency					
	+4 output	200.0		400.0	MHz	PLL locked
	+8 output	100.0		200.0	MHz	
	+12 output	66.6		133.3	MHz	
	+16 output	50.0		100.0	MHz	
	+20 output	40.0		80.0	MHz	
	+24 output	33.3		66.6	MHz	
	+48 output	16.6		33.3	MHz	
V_{PP}	Differential input voltage ^e (peak-to-peak)	0.3		1.3	V	
V_{CMR}	Differential input crosspoint voltage ^f (PCLK)	1.2		$V_{CC}-0.3$	V	
$V_{O(P-P)}$	Differential output voltage (peak-to-peak) (PCLK)	0.6	0.8		V	
$t_{PW,MIN}$	Input reference pulse width ^g	2.0			ns	
$t_{sk(O)}$	Output-to-output Skew			100	ps	
DC	Output duty cycle ^h	48	50	52	%	
$t_{JIT(CC)}$	Cycle-to-cycle jitter ⁱ		30	79	ps	
$t_{JIT(PER)}$	Period Jitter ⁱ		43	106	ps	
$t_{JIT(\emptyset)}$	I/O Phase Jitter ⁱ RMS (1 σ) ^j		86	212	ps	
BW	PLL closed loop bandwidth ^k					
	+32 feedback		0.60–1.5		MHz	
	+48 feedback		0.40–1.2		MHz	
	+64 feedback		0.30–1.0		MHz	
	+80 feedback		0.30–0.8		MHz	
	+96 feedback		0.20–0.7		MHz	
	+160 feedback		0.15–0.4		MHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	
t_r, t_f	Output Rise/Fall Time	0.05		1.0	ns	20% to 80%

- a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
- b. In bypass mode, the MPC9992 divides the input reference clock.
- c. The crystal frequency range must both meet the interface frequency range and VCO lock range divided by the feedback divider ratio:
 $f_{XTAL(min, max)} = f_{VCO(min, max)} \div (M \cdot VCO\_SEL)$ and $10 \text{ MHz} \leq f_{XTAL} \leq 20 \text{ MHz}$.
- d. The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{ref} = f_{VCO} \div (M \cdot VCO\_SEL)$
- e. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics.
- f. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification.
- g. Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF,MAX} = 100\% - DC_{REF,MIN}$. E.g. at $f_{REF}=50 \text{ MHz}$ the input duty cycle range is $10\% < DC < 90\%$.
- h. Output duty cycle for QAx and QBx outputs. The pulse width for the QSYNC output is equal to one QAx output period $T_{QA} \pm 5\%$.
- i. Jitter data is valid $f_{ref}=25 \text{ MHz}$.
- j. See application section for a jitter calculation for other confidence factors than 1 σ .
- k. -3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

SYNC Output Description

The MPC9992 has a system synchronization pulse output QSYNC. In configurations with the output frequency relationships are not integer multiples of each other QSYNC provides a signal for system synchronization purposes. The MPC9992 monitors the relationship between the A bank and the B bank

of outputs. The QSYNC output is asserted (logic high) one QA period in duration. The placement of the pulse is dependent on the QA and QB output frequencies ratio. Figure 3 shows the waveforms for the QSYNC output. The QSYNC output is defined for all possible combinations of the bank A and bank B outputs.

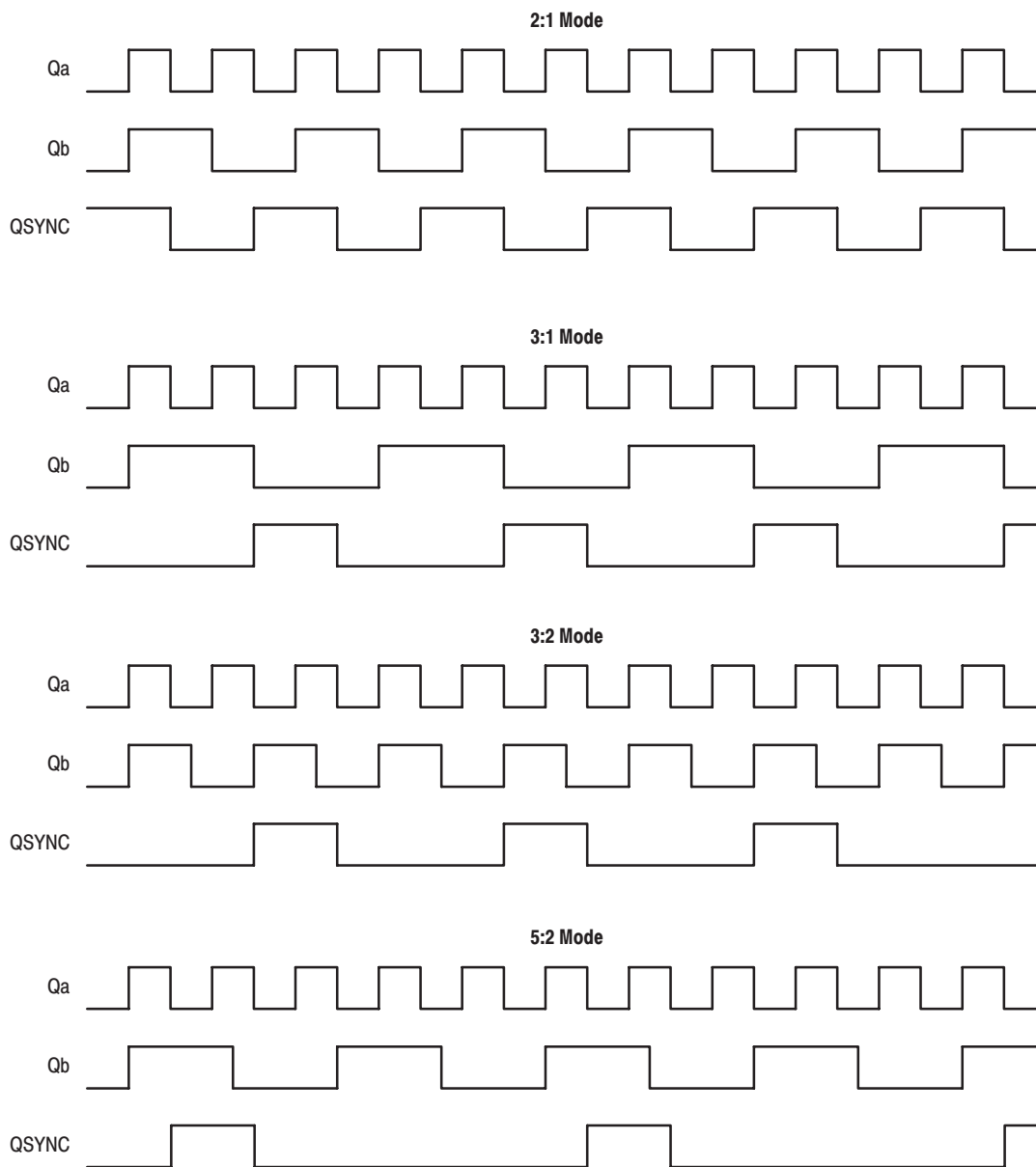


Figure 3. QSYNC Timing Diagram

Power Supply Filtering

The MPC9992 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC9992 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CC_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9992. Figure 4 illustrates a typical power supply filter scheme. The MPC9992 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F . From the data sheet the ICC_PLL current (the current sourced through the V_{CC_PLL} pin) is typically 9 mA (12 mA maximum), assuming that a minimum of 2.955V must be maintained on the V_{CC_PLL} pin. The resistor R_F shown in Figure 4 “ V_{CC_PLL} Power Supply Filter” must have a resistance of 10-15 Ω to meet the voltage drop criteria.

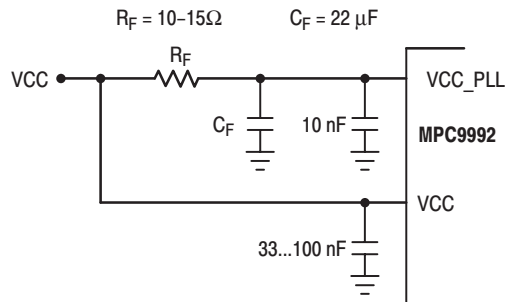


Figure 4. V_{CC_PLL} Power Supply Filter

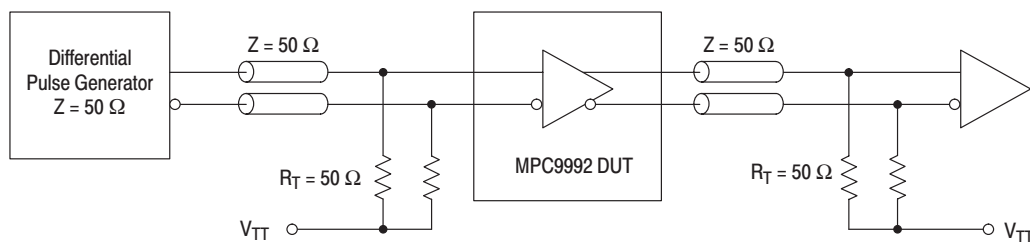


Figure 5. MPC9992 AC test reference

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 4 “ V_{CC_PLL} Power Supply Filter”, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9992 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Chapter Three

Failover or Redundant Clocks

Failover / Redundant Clock Device Index

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MPC9892	306
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MPC993	358
MPC9993	362

Product Preview

Intelligent Dynamic Clock Switch (IDCS) PLL Clock Driver

The MPC9892 is a PLL clock driver designed specifically for redundant clock tree designs. The device receives two differential LVPECL clock signals from which it generates 5 new differential LVPECL clock outputs. Two of the output pairs regenerate the input signals frequency and phase while the other three pairs generate 4x, phase aligned clock outputs. External PLL feedback is used to also provide zero delay buffer performance.

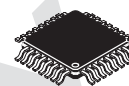
Features:

- Fully Integrated PLL
- Intelligent Dynamic Clock Switch
- LVPECL Clock Outputs
- LVCMOS Control I/O
- 3.3V Operation
- 32-Lead LQFP Packaging
- SiGe technology supports near-zero output skew

Functional Description

The MPC9892 Intelligent Dynamic Clock Switch (IDCS) circuit continuously monitors both input CLK signals. Upon detection of a failure (CLK stuck HIGH or LOW for at least 1 period), the INP_BAD for that CLK will be latched (H). If that CLK is the primary clock, the IDCS will switch to the good secondary clock and phase/frequency alignment will occur with minimal output phase disturbance. The typical phase bump caused by a failed clock is eliminated. (See Application Information section).

MPC9892



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A

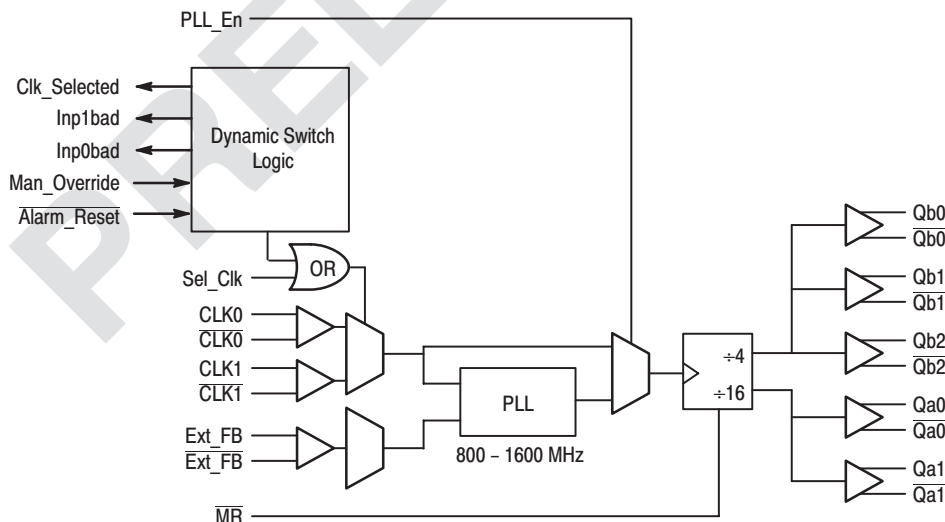


Figure 1. Block Diagram

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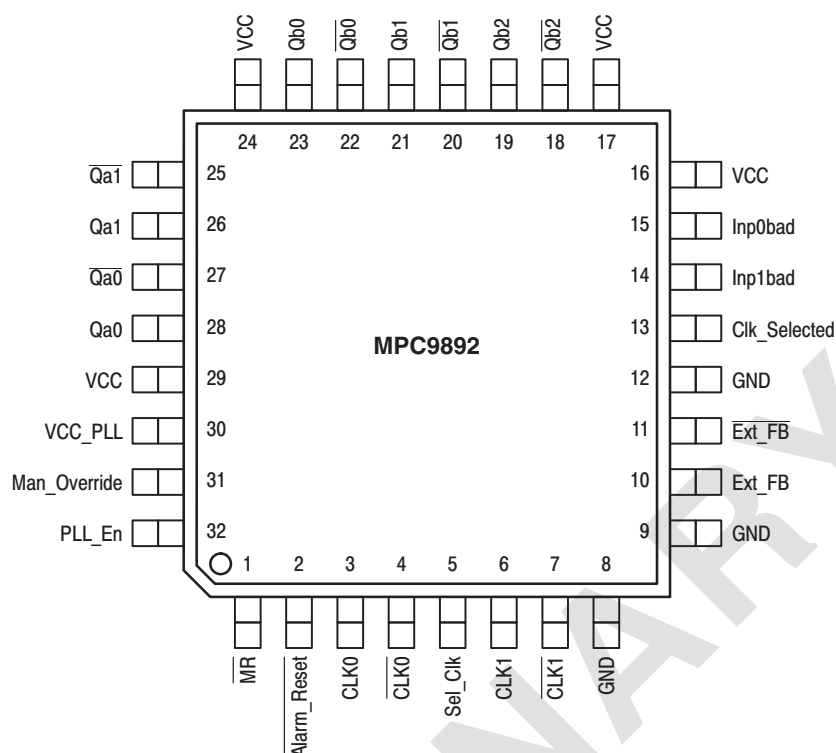


Figure 2. 32-Lead Pinout (Top View)

PIN DESCRIPTIONS

Pin Name	I/O	Pin Definition
CLK0, $\overline{\text{CLK0}}$ CLK1, $\overline{\text{CLK1}}$	LVPECL Input LVPECL Input	Differential PLL clock reference (CLK0 pulldown, $\overline{\text{CLK0}}$ pullup) Differential PLL clock reference (CLK1 pulldown, $\overline{\text{CLK1}}$ pullup)
Ext_FB, $\overline{\text{Ext\_FB}}$	LVPECL Input	Differential PLL feedback clock (Ext_FB pulldown, $\overline{\text{Ext\_FB}}$ pullup)
Qa0:1, $\overline{\text{Qa0:1}}$	LVPECL Output	Differential 1x output pairs
Qb0:2, $\overline{\text{Qb0:2}}$	LVPECL Output	Differential 4x output pairs
Inp0bad	LVC MOS Output	Indicates detection of a bad input reference clock 0 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted
Inp1bad	LVC MOS Output	Indicates detection of a bad input reference clock 1 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted
Clk_Selected	LVC MOS Output	'0' if clock 0 is selected, '1' if clock 1 is selected
Alarm_Reset	LVC MOS Input	'0' will reset the input bad flags and align Clk_Selected with Sel_Clk. The input is "one-shotted" (50k Ω pullup)
Sel_Clk	LVC MOS Input	'0' selects CLK0, '1' selects CLK1 (50k Ω pulldown)
Manual_Override	LVC MOS Input	'1' disables internal clock switch circuitry (50k Ω pulldown)
PLL_En	LVC MOS Input	'0' bypasses selected input reference around the phase-locked loop (50k Ω pullup)
$\overline{\text{MR}}$	LVC MOS Input	'0' resets the internal dividers forcing Q outputs LOW. Asynchronous to the clock (50k Ω pullup)
VCCA	Power Supply	PLL power supply
VCC	Power Supply	Digital power supply
GNDA	Power Supply	PLL ground
GND	Power Supply	Digital ground

ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	3.9	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} +0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} +0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

3**GENERAL SPECIFICATIONS**

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output termination voltage		V _{CC} - 2		V	
MM	ESD Protection (Machine model)	TBD			V	
HBM	ESD Protection (Human body model)	TBD			V	
CDM	ESD Protection (Charged device model)	TBD			V	
LU	Latch-up immunity	200			mA	
C _{IN}	Input Capacitance		4.0		pF	Inputs
θ _{JA}	Thermal resistance junction to ambient JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ _{JC}	Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
	Operating junction temperature ^a (continuous operation) MTBF = 9.1 years			110	°C	

a. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6226 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6226 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ$ to $+85^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS control inputs ($\overline{OE}$, FSEL0, FSEL1, MR)						
V_{IL}	Input voltage low			0.8	V	
V_{IH}	Input voltage high	2.0			V	
I_{IN}	Input Current ^b			$\pm$ TBD	μA	$V_{IN} = V_{CC}$ or $V_{IN} = GND$
LVPECL clock inputs (CLK, $\overline{CLK}$) ^c						
V_{PP}	AC differential input voltage ^d	0.1		1.3	V	Differential operation
V_{CMR}	Differential cross point voltage ^e	1.0		$V_{CC}-0.3$	V	Differential operation
V_{IH}	Input high voltage	TBD		TBD		
V_{IL}	Input low voltage	TBD		TBD		
I_{IN}	Input Current			$\pm$ TBD	μA	$V_{IN} = TBD$ or $V_{IN} = TBD$
LVPECL clock outputs (QA0-4, $\overline{QA0-4}$, QB0-4, $\overline{QB0-4}$)						
V_{OH}	Output High Voltage	TBD	$V_{CC}-1.005$	TBD	V	Termination 50Ω to V_{TT}
V_{OL}	Output Low Voltage	TBD	$V_{CC}-1.705$	TBD	V	Termination 50Ω to V_{TT}
I_{CC}	Maximum Power Supply VCC pins			TBD	mA	
I_{CCA}	Maximum PLL Power Supply VCC_PLL pin			TBD	mA	

- a. AC characteristics are design targets and pending characterization.
b. Input have internal pullup/pulldown resistors which affect the input current.
c. Clock inputs driven by LVPECL compatible signals.
d. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristic.
e. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

AC CHARACTERISTICS ($T_A = -40^\circ C$ to $85^\circ C$, $V_{CC} = 3.3V \pm 5\%$) (Note 5.)

Symbol	Parameter	Min	Typ	Max	Unit
f_{VCO}	PLL VCO Lock Range	800		1600	MHz
t_{pwi}		25		75	%
t_{pd}	Propagation Delay (Note 1.) CLKn to Q (Bypass) CLKn to Ext_FB (Locked (Note 2.))			TBD TBD	ns ps
V_{PP}	Differential input voltage (peak-to-peak)		0.3	1.3	V
V_{CMR}	Differential input crosspoint voltage			$V_{CC}-0.3$	V
t_r/t_f	Output Rise/Fall Time			TBD	ps
t_{skew}	Output Skew Within Bank All Outputs			35 50	ps
Δ_{pe}	Maximum Phase Error Deviation			TBD (Note 3.) TBD (Note 4.)	ps
$\Delta_{per/cycle}$	Rate of Change of Periods 75MHz Output (Note 1., 3.) 300MHz Output (Note 1., 3.) 75MHz Output (Note 1., 4.) 300MHz Output (Note 1., 4.)		20 10 200 100	50 25 400 200	ps/cycle
t_{pw}	Output Duty Cycle	45		55	%
t_{jitter}	Cycle-to-Cycle Jitter, Standard Deviation (RMS) (Note 1.)			20	ps
t_{lock}	Maximum PLL Lock Time			10	ms

1. Guaranteed, not production tested.
2. Static phase offset between the selected reference clock and the feedback signal.
3. Specification holds for a clock switch between two signals no greater than 400ps out of phase. Delta period change per cycle is averaged over the clock switch excursion. (See Applications Information section on page 310 for more detail)
4. Specification holds for a clock switch between two signals no greater than $\pm\pi$ out of phase. Delta period change per cycle is averaged over the clock switch excursion.
5. PECL output termination is 50 ohms to $V_{CC} - 2.0V$.

APPLICATIONS INFORMATION

The MPC9892 is a dual clock PLL with on-chip Intelligent Dynamic Clock Switch (IDCS) circuitry.

Definitions

primary clock: The input CLK selected by Sel_Clk.

secondary clock: The input CLK NOT selected by Sel_Clk.

PLL reference signal: The CLK selected as the PLL reference signal by Sel_Clk or IDCS. (IDCS can override Sel_Clk).

Status Functions

Clk_Selected: Clk_Selected (L) indicates CLK0 is selected as the PLL reference signal. Clk_Selected (H) indicates CLK1 is selected as the PLL reference signal.

INP_BAD: Latched (H) when it's CLK is stuck (H) or (L) for at least one Ext_FB period (Pos to Pos or Neg to Neg). Cleared (L) on assertion of Alarm_Reset.

Control Functions

Sel_Clk: Sel_Clk (L) selects CLK0 as the primary clock. Sel_Clk (H) selects CLK1 as the primary clock.

Alarm_Reset: Asserted by a negative edge. Generates a one-shot reset pulse that clears INPUT_BAD latches and Clk_Selected latch.

PLL_En: While (L), the PLL reference signal is substituted for the VCO output.

MR: While (L), internal dividers are held in reset which holds all Q outputs LOW.

Man Override (H)

(IDCS is disabled, PLL functions normally). PLL reference signal (as indicated by Clk_Selected) will always be the CLK selected by Sel_Clk. The status function INP_BAD is active in Man Override (H) and (L).

Man Override (L)

(IDCS is enabled, PLL functions enhanced). The first CLK to fail will latch it's INP_BAD (H) status flag and select the other input as the Clk_Selected for the PLL reference clock. Once latched, the Clk_Selected and INP_BAD remain latched until assertion of Alarm_Reset which clears all latches (INP_BADs are cleared and Clk_Selected = Sel_Clk). NOTE: If both CLKs are bad when Alarm_Reset is asserted, both INP_BADs will be latched (H) after one Ext_FB period and Clk_Selected will be

latched (L) indicating CLK0 is the PLL reference signal. While neither INP_BAD is latched (H), the Clk_Selected can be freely changed with Sel_Clk. Whenever a CLK switch occurs, (manually or by IDCS), following the next negative edge of the newly selected PLL reference signal, the next positive edge pair of Ext_FB and the newly selected PLL reference signal will slew to alignment.

To calculate the overall uncertainty between the input CLKs and the outputs from multiple MPC9892's, the following procedure should be used. Assuming that the input CLKs to all MPC9892's are exactly in phase, the total uncertainty will be the sum of the static phase offset, max I/O jitter, and output to output skew.

During a dynamic switch, the output phase between two devices may be increased for a short period of time. If the two input CLKs are 400ps out of phase, a dynamic switch of an MPC9892 will result in an instantaneous phase change of 400ps to the PLL reference signal without a corresponding change in the output phase (due to the limited response of the PLL). As a result, the I/O phase of a device, undergoing this switch, will initially be 400ps and diminish as the PLL slews to its new phase alignment. This transient timing issue should be considered when analyzing the overall skew budget of a system.

Hot insertion and withdrawal

In PECL applications, a powered up driver will experience a low impedance path through an MPC9892 input to its powered down VCC pins. In this case, a 100 ohm series resistance should be used in front of the input pins to limit the driver current. The resistor will have minimal impact on the rise and fall times of the input signals.

Acquiring Frequency Lock

1. While the MPC9892 is receiving a valid CLK signal, assert Man_Override HIGH.
2. The PLL will phase and frequency lock within the specified lock time.
3. Apply a HIGH to LOW transition to Alarm_Reset to reset Input Bad flags.
4. De-assert Man_Override LOW to enable Intelligent Dynamic Clock Switch mode.

Product Preview

Low Voltage PLL Intelligent Dynamic Clock (IDCS) Switch

The MPC9893 is a 2.5V and 3.3V compatible, PLL based intelligent dynamic clock switch and generator specifically designed for redundant clock distribution systems. The device receives two LVCMOS clock signals and generates 12 phase aligned output clocks. The MPC9893 is able to detect a failing reference clock signal and to dynamically switch to a redundant clock signal. The switch from the failing clock to the redundant clock occurs without interruption of the output clock signal (output clock slews to alignment). The phase bump typically caused by a clock failure is eliminated.

The device offers 12 low skew clock outputs organized into two output banks, each configurable to support the different clock frequencies.

The extended temperature range of the MPC9893 supports telecommunication and networking requirements. The device employs a fully differential PLL design to minimize jitter.

Features

- 12 output LVCMOS PLL clock generator
- 2.5V and 3.3V compatible
- IDCS - on-chip intelligent dynamic clock switch
- Automatically detects clock failure
- Smooth output phase transition during clock failover switch
- 6.25 - 200 MHz output frequency range
- LVCMOS compatible inputs and outputs
- External feedback enables zero-delay configurations
- Supports networking, telecommunications and computer applications
- Output enable/disable and static test mode (PLL bypass)
- Low skew characteristics: maximum 150 ps¹ output-to-output (within bank)
- 48 lead LQFP package
- Ambient operating temperature range of -40 to 85°C

Functional Description

The MPC9893 is a 3.3V or 2.5V compatible PLL clock driver and clock generator. The clock generator uses a fully integrated PLL to generate clock signals from redundant clock sources. The PLL multiplies the input reference clock signal by one, two, three, four or eight. The frequency-multiplied clock drives six bank A outputs. Six bank B outputs can run at either the same frequency than bank A or at half of the bank A frequency. Therefore, bank B outputs additionally support the frequency multiplication of the input reference clock by 3÷2 and 1÷2. Bank A and bank B outputs are phase-aligned². Due to the external PLL feedback, the clock signals of both output banks are also phase-aligned² to the selected input reference clock, providing virtually zero-delay capability. The integrated IDCS continuously monitors both clock inputs and indicates a clock failure individually for each clock input. When a false clock signal is detected, the MPC9893 switches to the redundant clock input, forcing the PLL to slowly slew to alignment and not produce any phase bumps at the outputs. Both clock inputs are interchangeable, also supporting the switch to a failed clock that was restored. The MPC9893 also provides a manual mode that allows for user-controlled clock switches.

The PLL bypass of the MPC9893 disables the IDCS and PLL-related specifications do not apply. In PLL bypass mode, the MPC9893 is fully static in order to distribute low-frequency clocks for system test and diagnosis. Outputs of the MPC9893 can be disabled (high-impedance tristate) to isolate the device from the system. Applying output disable also resets the MPC9893. On power-up this reset function needs to be applied for correct operation of the circuitry. Please see the application section for power-on sequence recommendations.

The device is packaged in a 7x7 mm² 48-lead LQFP package.

1. Final specification subject to change.
2. At coincident rising edges.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MPC9893

**LOW VOLTAGE 2.5V AND 3.3V
IDCS AND PLL
CLOCK GENERATOR**

3



FA SUFFIX
48-LEAD LQFP PACKAGE
CASE 932

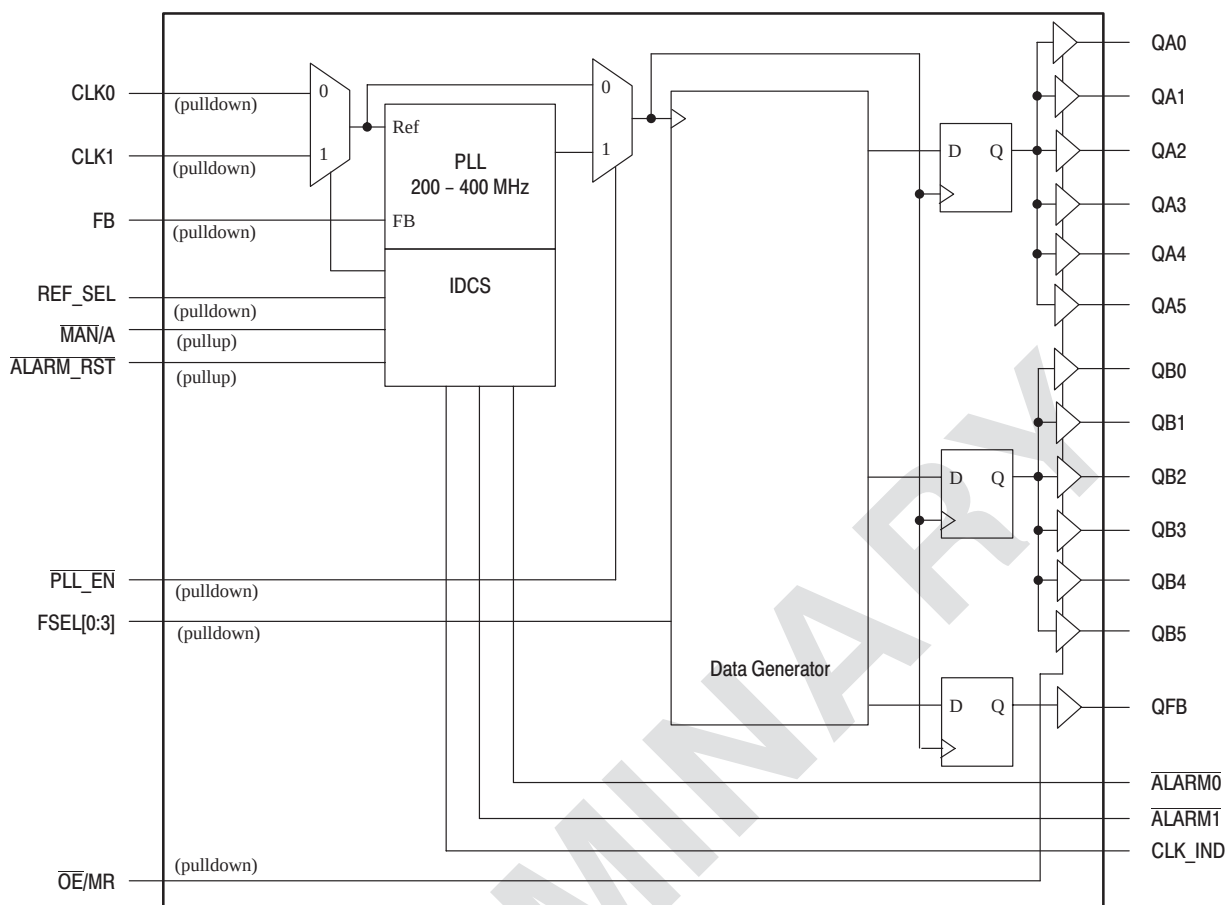
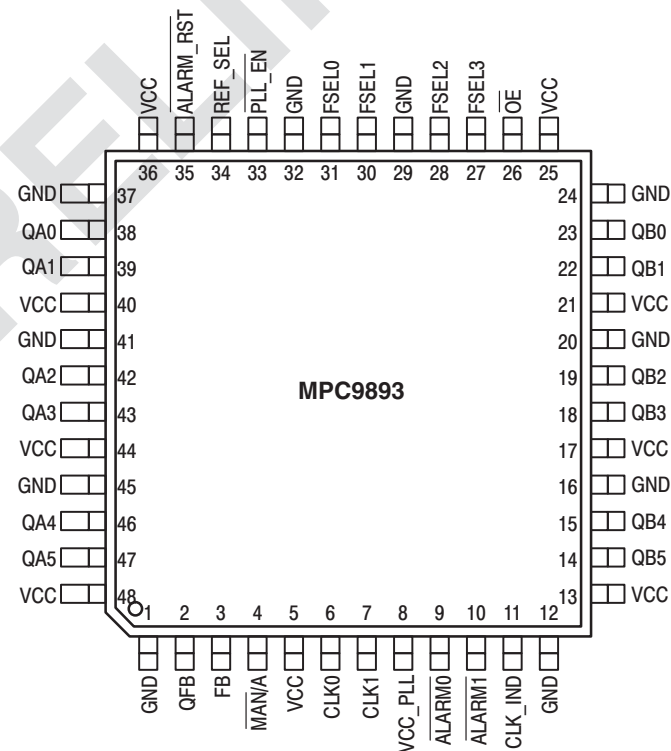


Figure 1. MPC9893 Logic Diagram



The MPC9893 requires an external RC filter for the analog power supply pin VCC_PLL. Please see application section for details.

Figure 2. 48-Lead Package Pinout (Top View)

Table 1: PIN CONFIGURATION

Pin	I/O	Type	Function
CLK0, CLK1	Input	LVC MOS	PLL reference clock inputs
FB	Input	LVC MOS	PLL feedback signal input, connect directly to QFB output
REF_SEL	Input	LVC MOS	Selects the primary reference clock
MAN/A	Input	LVC MOS	Selects automatic switch mode or manual reference clock selection
ALARM_RST	Input	LVC MOS	Reset of alarm flags and selected reference clock
PLL_EN	Input	LVC MOS	Select PLL or static test mode
FSEL[0:3]	Input	LVC MOS	Clock frequency selection and configuration of clock divider modes
OE/MR	Input	LVC MOS	Output enable/disable and device reset
QA[0:5]	Output	LVC MOS	Bank A clock outputs
QB[0:5]	Output	LVC MOS	Bank B clock outputs
QFB	Output	LVC MOS	Clock feedback output. QFB must be connected to FB for correct operation
ALARM0	Output	LVC MOS	Indicates clock failure on CLK0
ALARM1	Output	LVC MOS	Indicates clock failure on CLK1
CLK_IND	Output	LVC MOS	Indicates currently selected input reference clock
GND	Supply	Ground	Negative power supply
VCC_PLL	Supply	VCC	Positive power supply for the PLL (analog power supply). The MPC9893 requires an external RC filter for the analog power supply pin VCC_PLL. Please see the application section for details.
VCC	Supply	VCC	Positive power supply for I/O and core

3

Table 2: FUNCTION TABLE

Control	Default	0	1
Inputs			
PLL_EN	0	PLL enabled. The input to output frequency relationship is that according to Table 3 if the PLL is frequency locked.	PLL bypassed and IDCS disabled. The VCO output is replaced by the reference clock signal fref. The MPC9893 is in manual mode.
MAN/A	1	Manual clock switch mode. IDCS disabled. Clock failure detection and output flags ALARM0, ALARM1, CLK_IND are enabled.	Automatic clock switch mode. IDCS enabled. Clock failure detection and output flags ALARM0, ALARM1, CLK_IND are enabled. IDCS overrides REF_SEL on a clock failure. IDCS operation requires PLL_EN = 0.
ALARM_RST	1	ALARM0, ALARM1 and CLK_IND flags are reset: ALARM0=H, ALARM1=H and CLK_IND=REF_SEL. ALARM_RST is an one-shot function.	ALARM0, ALARM1 and CLK_IND active
REF_SEL	0	Selects CLK0 as the primary clock source	Selects CLK1 as the secondary clock source
FSEL[0:3]	0000	See Following Table	
OE/MR	0	Outputs enabled (active)	Outputs disabled (high impedance tristate), reset of data generators and output dividers. The MPC9893 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than two reference clock cycles (CLK0,1). MR/OE does not tristate the QFB output.
Outputs (ALARM0, ALARM1, CLK_IND are valid if PLL is locked)			
ALARM0		CLK0 failure	
ALARM1		CLK1 failure	
CLK_IND		CLK0 is the reference clock	CLK1 is the reference clock

Table 3: CLOCK FREQUENCY CONFIGURATION

Name	FSEL 0	FSEL 1	FSEL 2	FSEL 3	f _{REF} range [MHz]	QA _x		QB _x		QFB
						Ratio	f _{QAx} [MHz]	Ratio	f _{QBx} [MHz]	
M8	0	0	0	0	12.5—25	f _{REF} * 8	100—200	f _{REF} * 8	100—200	f _{REF}
M82	0	0	0	1				f _{REF} * 4	50—100	f _{REF}
M4	0	0	1	0	25.0—50.0	f _{REF} * 4	100—200	f _{REF} * 4	100—200	f _{REF}
M42	0	0	1	1				f _{REF} * 2	50—100	f _{REF}
M3	0	1	0	0	33.3—66.6	f _{REF} * 3	100—200	f _{REF} * 3	100—200	f _{REF}
M32	0	1	0	1				f _{REF} * 3 ÷ 2	50—100	f _{REF}
M2M	0	1	1	0	25.0—50.0	f _{REF} * 2	50—100	f _{REF} * 2	50—100	f _{REF}
M22M	0	1	1	1				f _{REF} * 1	25.0—50.0	f _{REF}
M2H	1	0	0	0	50.0—100.0	f _{REF} * 2	100—200	f _{REF} * 2	100—200	f _{REF}
M22H	1	0	0	1				f _{REF}	50—100	f _{REF}
M1L	1	0	1	0	12.5—25	f _{REF}	12.5—25	f _{REF}	12.5—25	f _{REF}
M12L	1	0	1	1				f _{REF} ÷ 2	6.25—12.5	f _{REF}
M1M	1	1	0	0	25.0—50.0	f _{REF}	25.0—50.0	f _{REF}	25.0—50.0	f _{REF}
M12M	1	1	0	1				f _{REF} ÷ 2	12.5—25	f _{REF}
M1H	1	1	1	0	50.0—100.0	f _{REF}	50.0—100.0	f _{REF}	50.0—100.0	f _{REF}
M12H	1	1	1	1				f _{REF} ÷ 2	25.0—50.0	f _{REF}

Table 4: GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output Termination Voltage		V _{CC} ÷ 2		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C _{PD}	Power Dissipation Capacitance		10		pF	Per output
C _{IN}	Input Capacitance		4.0		pF	Inputs

Table 5: ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	3.6	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} +0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} +0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6: DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input Low Voltage			0.8	V	LVC MOS
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -24 \text{ mA}^a$
V_{OL}	Output Low Voltage			0.55 0.30	V V	$I_{OL} = 24 \text{ mA}$ $I_{OL} = 12 \text{ mA}$
Z_{OUT}	Output Impedance		14 - 17		Ω	
I_{IN}	Input Current			± 200	μA	$V_{IN} = V_{CC}$ or GND
I_{CC_PLL}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CC_PLL} Pin
I_{CC}	Maximum Quiescent Supply Current				mA	All V_{CC} Pins
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	

a. The MPC9893 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines.

3

Table 7: AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)^{a b}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	FSEL= 000x	12.5	25.0	MHz	PLL locked
		FSEL= 001x	25.0	50.0	MHz	
		FSEL= 010x	33.3	66.6	MHz	
		FSEL= 011x	25.0	50.0	MHz	
		FSEL= 100x	50.0	100.0	MHz	
		FSEL= 101x	12.5	12.5	MHz	
		FSEL= 110x	25.0	50.0	MHz	
		FSEL= 111x	50.0	100.0	MHz	
f_{MAX}	Maximum Output Frequency	FSEL= 000x	50.0	200.0	MHz	PLL locked
		FSEL= 001x	50.0	200.0	MHz	
		FSEL= 010x	50.0	200.0	MHz	
		FSEL= 011x	25.0	100.0	MHz	
		FSEL= 100x	50.0	200.0	MHz	
		FSEL= 101x	6.25	25.0	MHz	
		FSEL= 110x	12.5	50.0	MHz	
		FSEL= 111x	25.0	100.0	MHz	
f_{refDC}	Reference Input Duty Cycle	25		75	%	
t_r, t_f	CLK0, 1 Input Rise/Fall Time			1.0	ns	0.8 to 2.0V
$t_{(\phi)}$	Propagation Delay (static phase offset) CLK to FB		± 100			PLL locked
Δt	Rate of period change (phase slew rate)				ps/cycle	Failover switch
$t_{sk(O)}$	Output-to-output Skew ^c	(within bank)		150	ps	
		(within device)		200	ps	
DC_O	Output duty Cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter	RMS (1 σ) ^d		TBD	ps	
$t_{JIT(PER)}$	Period Jitter	RMS (1 σ)		TBD	ps	
$t_{JIT(\phi)}$	I/O Phase Jitter	RMS (1 σ)		TBD	ps	
BW	PLL closed loop bandwidth ^e			TBD	kHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

a. All AC characteristics are design targets and subject to change upon device characterization

b. AC characteristics apply for parallel output termination of 50Ω to V_{TT}

c. See application section for part-to-part skew calculation

d. See application section for calculation for other confidence factors than 1 σ

e. -3dB point of PLL transfer characteristics

Table 8: DC CHARACTERISTICS ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	1.7		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input Low Voltage			0.7	V	LVC MOS
V_{OH}	Output High Voltage	1.8			V	$I_{OH} = -15 \text{ mA}^a$
V_{OL}	Output Low Voltage			0.6	V	$I_{OL} = 15 \text{ mA}$
Z_{OUT}	Output Impedance		17 - 20		Ω	
I_{IN}	Input Current			± 200	μA	$V_{IN} = V_{CC}$ or GND
I_{CC_PLL}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CC_PLL} Pin
I_{CC}	Maximum Quiescent Supply Current				mA	All V_{CC} Pins
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	

a. The MPC9893 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

Table 9: AC CHARACTERISTICS ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)^{a b}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	FSEL= 000x	12.5	25.0	MHz	PLL locked
		FSEL= 001x	25.0	50.0	MHz	
		FSEL= 010x	33.3	66.6	MHz	
		FSEL= 011x	25.0	50.0	MHz	
		FSEL= 100x	50.0	100.0	MHz	
		FSEL= 101x	12.5	12.5	MHz	
		FSEL= 110x	25.0	50.0	MHz	
		FSEL= 111x	50.0	100.0	MHz	
f_{MAX}	Maximum Output Frequency	FSEL= 000x	50.0	200.0	MHz	PLL locked
		FSEL= 001x	50.0	200.0	MHz	
		FSEL= 010x	50.0	200.0	MHz	
		FSEL= 011x	25.0	100.0	MHz	
		FSEL= 100x	50.0	200.0	MHz	
		FSEL= 101x	6.25	25.0	MHz	
		FSEL= 110x	12.5	50.0	MHz	
		FSEL= 111x	25.0	100.0	MHz	
f_{refDC}	Reference Input Duty Cycle	25		75	%	
t_r, t_f	CLK0, 1 Input Rise/Fall Time			1.0	ns	0.7 to 1.7V
$t_{(\phi)}$	Propagation Delay (static phase offset) CLK to FB		± 100			PLL locked
Δt	Rate of period change (phase slew rate)				ps/cycle	Failover switch
$t_{sk(O)}$	Output-to-output Skew ^c	(within bank)		150	ps	
		(within device)		200	ps	
DC_O	Output duty Cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.6 to 1.8V
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter	RMS (1 σ) ^d		TBD	ps	
$t_{JIT(PER)}$	Period Jitter	RMS (1 σ)		TBD	ps	
$t_{JIT(\phi)}$	I/O Phase Jitter	RMS (1 σ)		TBD	ps	
BW	PLL closed loop bandwidth ^e			TBD	kHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

a. All AC characteristics are design targets and subject to change upon device characterization

b. AC characteristics apply for parallel output termination of 50Ω to V_{TT}

c. See application section for part-to-part skew calculation

d. See application section for calculation for other confidence factors than 1 σ

e. -3dB point of PLL transfer characteristics

APPLICATIONS INFORMATION

Definitions

IDCS: Intelligent Dynamic Clock Switch. The IDCS monitors both primary and secondary clock signals. Upon a failure of the primary clock signal, the IDCS switches to a valid secondary clock signal and status flags are set.

Reference clock signal ref: The clock signal that is selected by the IDCS or REF_SEL as the input reference to the PLL.

Manual mode: The reference clock frequency is selected by REF_SEL.

Automatic mode: The reference clock frequency is determined by the internal IDCS logic.

Primary clock: The input clock signal selected by REF_SEL. The primary clock may or may not be the reference clock, depending on switch mode and IDCS status.

Secondary clock: The input clock signal not selected by REF_SEL.

Selected clock: The CLK_IND flag indicates the reference clock signal: CLK_IND = 0 indicates CLK0 is the clock reference signal, CLK_IND = 1 indicates CLK1 is the reference clock signal.

Clock failure: A valid clock signal that is stuck (high or low) for at least one input clock period. The primary clock and the secondary clock is monitored for failure. Valid clock signals must be within the AC and DC specification for the input reference clock. A loss of clock is detected if as well as the loss of both clocks. In the case of both clocks lost, the MPC9893 will set the alarm flags and the PLL will stall. The MPC9893 does not monitor and detect changes in the input frequency.

Automatic mode and IDCS commanded clock switch

$\overline{MAN}/A = 1$, IDCS enabled: Both primary and secondary clocks are monitored. The first clock failure is reported by its $\overline{ALARMx}$ status flag (clock failure is indicated by a logic low). The $\overline{ALARMx}$ status is flag latched and remains latched until reset by assertion of ALARM_RST.

If the clock failure occurs on the primary clock, the IDCS attempts to switch to the secondary clock. The secondary clock signal needs to be valid for a successful switch. Upon a successful switch, CLK_IND indicates the reference clock, which may now be different as that originally selected by REF_SEL.

Manual mode

$\overline{MAN}/A = 0$, IDCS disabled: PLL functions normally and both clocks are monitored. The reference clock signal will always be the clock signal selected by REF_SEL and will be indicated by CLK_IND.

Clock output transition

A clock switch, either in automatic or manual mode, follows the next negative edge of the newly selected reference clock signal. The feedback and newly selected reference clock edge

will start to slew to alignment at the next positive edge of both signals. Output runt pulses are eliminated.

Reset

ALARM_RST is asserted by a negative edge. It generates a one-shot reset pulse that clears both $\overline{ALARMx}$ latches and the CLK_IND latch. If both CLK0 and CLK1 are invalid or fail when ALARM_RST is asserted, both $\overline{ALARMx}$ flags will be latched after one FB signal period and CLK_IND will be latched (L) indicating CLK0 is the reference signal. While neither $\overline{ALARMx}$ flag is latched ($\overline{ALARMx} = H$), the CLK_IND can be freely changed with REF_SEL.

$\overline{OE}/MR$: Reset the data generator and output disable. Does not reset the IDCS flags.

Acquiring frequency lock at startup

1. On startup, $\overline{OE}/MR$ must be asserted to reset the output dividers. The IDCS should be disabled ($\overline{MAN}/A=0$) during startup to select the manual mode and the primary clock.
2. The PLL will attempt to gain lock if the primary clock is present on startup. PLL lock requires the specified lock time.
3. Applying a high to low transition to $\overline{ALARM_RST}$ will clear the alarm flags.
4. Enable the IDCS ($\overline{MAN}/A=1$) to enable to IDCS.

Power Supply Filtering

The MPC9893 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the VCC_PLL (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9893 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (VCC_PLL) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the VCC_PLL pin for the MPC9893. Figure 3 illustrates a typical power supply filter scheme. The MPC9893 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F . From the data sheet the I_{CC_PLL} current (the current sourced through the VCC_PLL pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V ($V_{CC}=3.3V$ or $V_{CC}=2.5V$) must be maintained on the VCC_PLL pin. The resistor R_F shown in Figure 3 "VCC_PLL Power Supply Filter" must have a resistance of 270 Ω ($V_{CC}=3.3V$) or 9-10 Ω ($V_{CC}=2.5V$) to meet the voltage drop criteria.

$R_F = 270\Omega$ for $V_{CC} = 3.3V$
 $R_F = 9-10\Omega$ for $V_{CC} = 2.5V$

$C_F = 1\mu F$ for $V_{CC} = 3.3V$
 $C_F = 22\mu F$ for $V_{CC} = 2.5V$

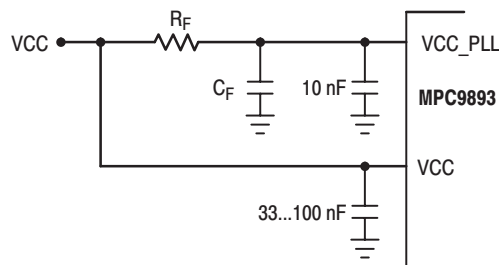


Figure 3. VCC_PLL Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3 “VCC_PLL Power Supply Filter”, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9893 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9893 in zero-delay applications

Nested clock trees are typical applications for the MPC9893. Designs using the MPC9893 as LVCMOS PLL fan-out buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fan-out buffers. The external feedback option of the MPC9893 clock driver allows for its use as a zero delay buffer. One example configuration is to use a +4 output as a feedback to the PLL and configuring all other outputs to a divide-by-4 mode. The propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of part-to-part skew

The MPC9893 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9893 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD, LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

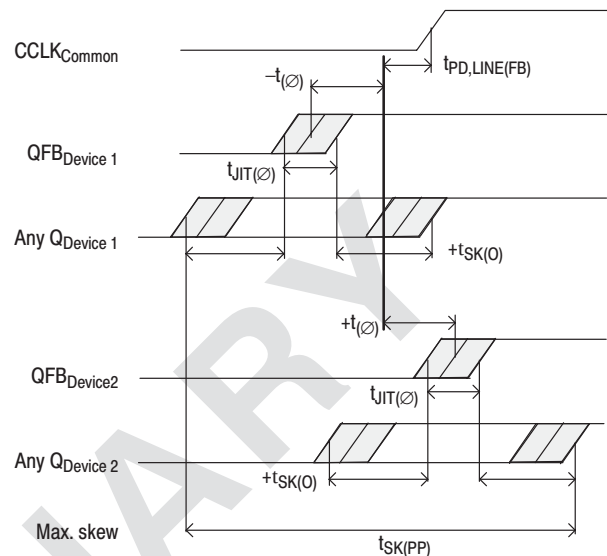


Figure 4. MPC9893 max. device-to-device skew

Due to the statistical nature of I/O jitter a RMS value (1σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 10.

Table 10: Confidence Factor CF

CF	Probability of clock edge within the distribution
$\pm 1\sigma$	0.68268948
$\pm 2\sigma$	0.95449988
$\pm 3\sigma$	0.99730007
$\pm 4\sigma$	0.99993663
$\pm 5\sigma$	0.99999943
$\pm 6\sigma$	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% ($\pm 3\sigma$) is assumed, resulting in a worst case timing uncertainty from input to any output of -TBD ps to TBD ps¹ relative to CCLK:

$$t_{SK(PP)} = [-TBDps...TBDps] + [-200ps...200ps] + [(15ps \cdot -3)...(15ps \cdot 3)] + t_{PD, LINE(FB)}$$

$$t_{SK(PP)} = [-TBDps...TBDps] + t_{PD, LINE(FB)}$$

Due to the frequency dependence of the I/O jitter, Figure 5 “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis.

TBD
 See MPC961C application section for
 an example I/O jitter characteristics

Figure 5. Max. I/O Jitter versus frequency

1. Final skew data pending specification.

Driving Transmission Lines

The MPC9893 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}+2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9893 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 6 "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9893 clock driver is effectively doubled due to its capability to drive multiple lines.

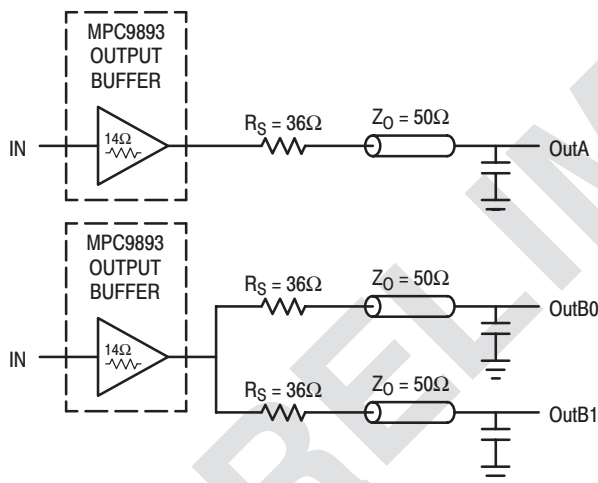


Figure 6. Single versus Dual Transmission Lines

The waveform plots in Figure 7 "Single versus Dual Line Termination Waveforms" show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9893 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9893. The output waveform in Figure 7 "Single versus Dual Line Termination Waveforms" shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the

parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$

$$Z_0 = 50\Omega \parallel 50\Omega$$

$$R_S = 36\Omega \parallel 36\Omega$$

$$R_0 = 14\Omega$$

$$V_L = 3.0 (25 \div (18 + 17 + 25)) \\ = 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

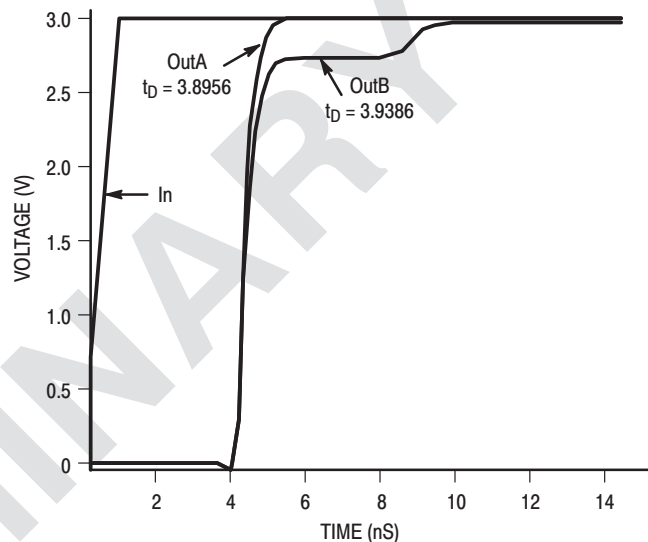


Figure 7. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 8 "Optimized Dual Line Termination" should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

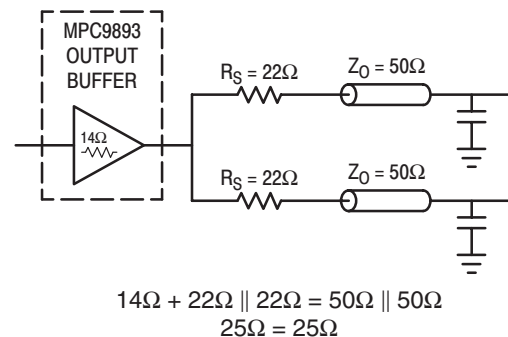


Figure 8. Optimized Dual Line Termination

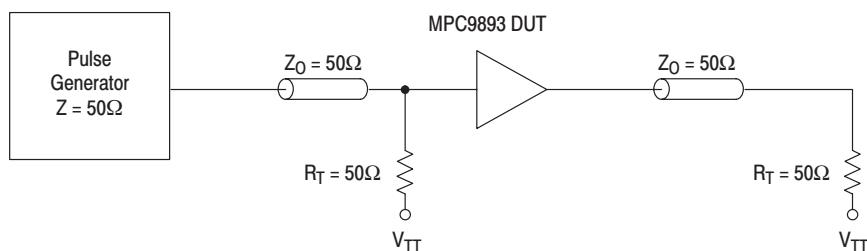
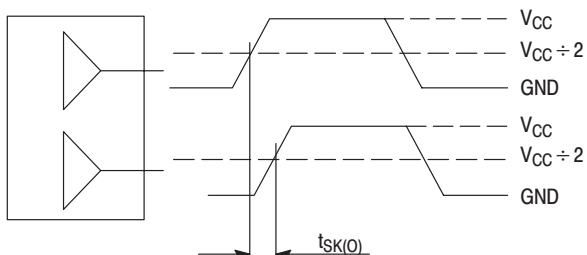


Figure 9. CLK0, CLK1 MPC9893 AC test reference for $V_{CC} = 3.3V$ and $V_{CC} = 2.5V$



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 10. Output-to-output Skew $t_{SK(O)}$

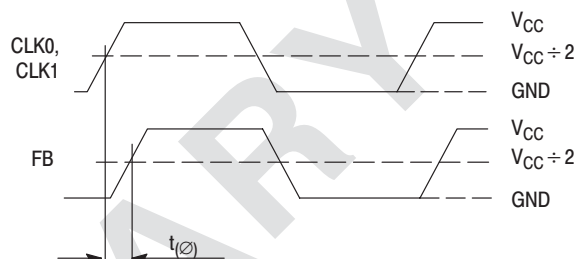
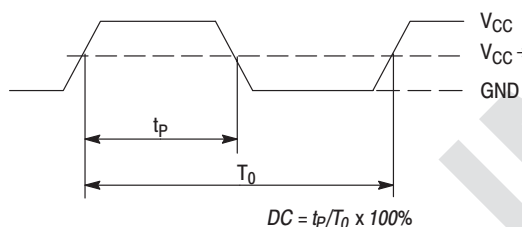
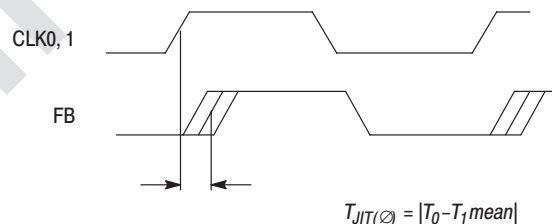


Figure 11. Propagation delay ($t_{(\phi)}$, static phase offset) test reference



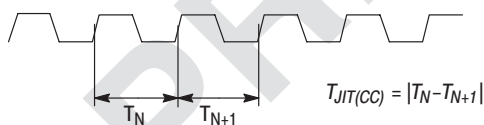
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 12. Output Duty Cycle (DC)



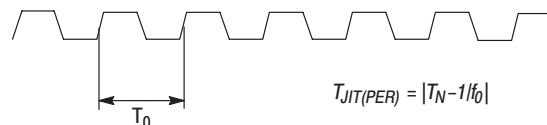
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 13. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 14. Cycle-to-cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 15. Period Jitter

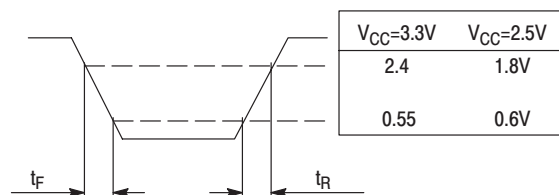


Figure 16. Output Transition Time Test Reference

Product Preview

Quad Input Redundant IDCS Clock Generator

The MPC9894 is a differential input and output, PLL-based Intelligent Dynamic Clock Switch (IDCS) and clock generator specifically designed for redundant clock distribution systems. The device receives up to four LVPECL clock signals and generates eight phase-aligned output clocks. The MPC9894 is able to detect failing clock signals and to dynamically switch to a redundant clock signal. The switch from the failing clock to the redundant clock occurs without interruption of the output clock signal (output clock slews to alignment). The phase bump typically caused by a clock failure is eliminated. The device offers eight low-skew clock outputs organized into four output banks, each configurable to support the different clock frequencies. The extended temperature range of the MPC9894 supports telecommunication and networking requirements.

Features

- 8 differential LVPECL output pairs
- Quad-redundancy reference clock inputs
- IDCS - on-chip intelligent dynamic clock switch
- Smooth output phase transition during clock failover switch
- Automatically detects clock failures
- Clock activity monitor
- Clock qualifier inputs
- Manual clock select and automatic switch modes
- 21.25 - 340 MHz output frequency range
- Specified frequency and phase slew rate on clock switch
- LVCMOS compatible control inputs and outputs
- External feedback enables zero-delay configurations
- Output enable/disable and static test mode (PLL bypass)
- low-skew characteristics: maximum 50 ps¹ output-to-output
- I²C interface for device configuration
- Low cycle-to-cycle and period jitter
- IEEE 1149.1 JTAG Interface
- 100-ball MAPBGA package
- Supports 2.5 or 3.3V supplies with 2.5V and 3.3V I/O
- Junction temperature range -40°C to +110°C

Functional Description

The MPC9894 is a quad differential redundant input clock generator. The device contains logic for clock failure detection and auto switching for clock redundant applications. The generator uses a fully integrated PLL to generate clock signals from any one of four redundant clock sources. The PLL multiplies the frequency of the input reference clock by one, two, four, eight or divides the reference clock by two or four. The frequency-multiplied clock signal drives four banks of two differential outputs. Each bank allows an individual frequency-divider configuration. All outputs are phase-aligned² to each other. Due to the external PLL feedback, the clock signals of all outputs are also phase-aligned² to the selected input reference clock, providing virtually zero-delay capability.

The integrated IDCS continuously monitors all four clock inputs and indicates a clock failure for each clock input. When a false clock signal is detected on the active clock, the MPC9894 switches to a redundant clock input, forcing the PLL to slowly slew to alignment and not produce any phase bumps at the outputs. The MPC9894 also provides a manual mode that allows for user-controlled clock switches.

The device is packaged in a 11x11 mm² 100-ball MAPBGA package.

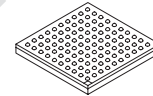
1. Final specification subject to change.
2. At coincident rising edges.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MPC9894

**QUAD INPUT REDUNDANT
IDCS CLOCK GENERATOR**

3



VF SUFFIX
100-LEAD MAP BGA PACKAGE
CASE 1462

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DEVICE DESCRIPTION

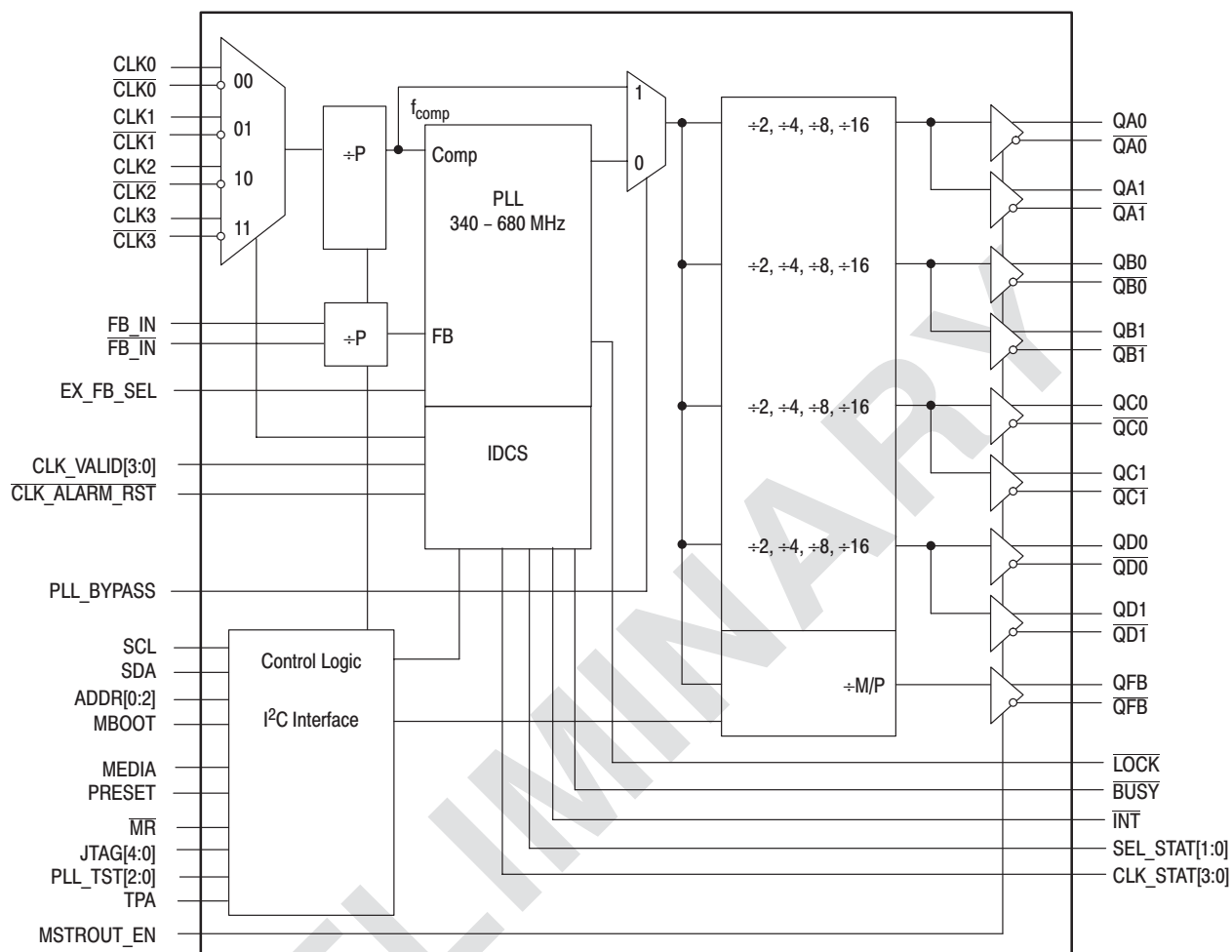


Figure 1. MPC9894 Block Diagram

Table 1. PIN CONFIGURATIONS

Pin	I/O	Type	Function	Supply	Active State
Clock Inputs and Outputs					
CLK0, $\overline{\text{CLK0}}$ CLK1, $\overline{\text{CLK1}}$ CLK2, $\overline{\text{CLK2}}$ CLK3, $\overline{\text{CLK3}}$	Input	LVPECL	PLL reference clock inputs (differential) (internal pulldown)	VDDIC	-
FB_IN, $\overline{\text{FB_IN}}$	Input	LVPECL	PLL feedback signal input (differential). When configured for external feedback, the QFB output should be connected to FB_IN. (internal pulldown)	VDDIC	-
QA[1:0], $\overline{\text{QA}}[1:0]$	Output	LVPECL	Bank A differential outputs	VDDAB	-
QB[1:0], $\overline{\text{QB}}[1:0]$	Output	LVPECL	Bank B differential outputs	VDDAB	-
QC[1:0], $\overline{\text{QC}}[1:0]$	Output	LVPECL	Bank C differential outputs	VDDCD	-
QD[1:0], $\overline{\text{QD}}[1:0]$	Output	LVPECL	Bank D differential outputs	VDDCD	-
QFB, $\overline{\text{QFB}}$	Output	LVPECL	Differential PLL feedback output. QFB must be connected to FB_IN for correct operation	VDDCD	-

Table 1. PIN CONFIGURATIONS

Pin	I/O	Type	Function	Supply	Active State
Control Inputs and Outputs					
EX_FB_SEL	Input	LVC MOS	Selects between external feedback and internal feedback	VDD	high
CLK_VALID[3:0] ^a	Input	LVC MOS	Validates the clock inputs CLK0 to CLK3 (internal pullup)	VDD	high
CLK_ALARM_RST	Input	LVC MOS	Reset of all four alarm status flags and clock selection status flag (internal pullup)	VDD	low
PLL_BYPASS	Input	LVC MOS	Select static test mode (internal pulldown)	VDD	high
MEDIA	Input	LVC MOS	Output impedance control	VDD	high
MR	Input	LVC MOS	Device reset (internal pullup)	VDD	low
LOCK	Output	LVC MOS	PLL lock indicator	VDD	low
CLK_STAT[3:0]	Output	LVC MOS	Clock input status indicator	VDD	high
SEL_STAT[1:0]	Output	LVC MOS	Reference clock selection indicator	VDD	high
BUSY	Output	LVC MOS	IDCS switching activity indicator	VDD	low
MBOOT	Input	LVC MOS	Activates I ² C boot sequence (internal pulldown)	VDD	high
PRESET	Input	LVC MOS	Enables Preset configuration of configuration registers on release of MR (internal pulldown)	VDD	high
INT	Output	OD	Indicate any status IDCS change	VDD	low
MSTROUT_EN	Input	LVC MOS	Master Enable for all Outputs (internal pullup)	VDD	high
SEL_2P5V	Input	LVC MOS	Device core power supply selection for VDD and VDDA	VDD	high
I²C Interface					
SCL	I/O	OD	I ² C interface control, clock	VDD	-
SDA	I/O	OD	I ² C interface control, data	VDD	-
ADDR[2:0]	Input	LVC MOS	I ² C interface address lines (10K pullup)	VDD	high
IEEE 1149.1 and Test					
TMS	Input	LVC MOS	JTAG test mode select(10K pullup)	VDDIC	-
TDI	Input	LVC MOS	JTAG test data input(10K pullup)	VDDIC	-
TDO	Output	LVC MOS	JTAG test data output	VDDIC	-
TCK	Input	LVC MOS	JTAG test clock	VDDIC	-
TRST	Input	LVC MOS	JTAG test reset(10K pullup)	VDDIC	-
PLL_TEST[2:0]	Input	LVC MOS	PLL_TEST pins (factory use only, MUST BE CONNECTED TO GND)	N/A	-
TPA	Output	LVC MOS	PLL Analog test pin (factory use only, MUST BE CONNECT TO GND)	VDDA	-
Power and Ground					
GND	Supply	Ground	Negative power supply	-	-
VDD	Supply	-	Positive power supply for the device core, output status and control inputs. (3.3V or 2.5V)	-	-
VDDAB	Supply	-	Supply voltage for output banks A and B (QA0 through QB1) (3.3V or 2.5V)	-	-
VDDCD	Supply	-	Supply voltage for output banks C and D (QC0 through QD1) and QFB (3.3V or 2.5V)	-	-
VDDIC	Supply	-	Supply voltage for differential inputs clock inputs CLK0 to CLK3 and FB_IN (3.3V or 2.5V)	-	-
VDDA	Supply	-	Clean supply for analog portions of the PLL (This voltage is derived via a RC filter from the VDD supply)	-	-

a. bit order = msb to lsb.

Table 2. FUNCTION TABLE

Control	Default	0	1
Control inputs			
PLL_BYPASS	0	PLL enabled. The input to output frequency relationship is according to Table 9 on page 332 if the PLL is frequency locked.	PLL bypassed and IDCS disabled. The VCO output is replaced by the reference clock signal fref. This is considered to be a test mode and clock monitoring and clock switching are disabled during this operation.
CLK_VALID[3:0]	0	The associated clock input is considered to be invalid and usable	The associated clock input is considered to be a valid usable clock input
CLK_ALARM_RST	1	CLK_STAT[3:0] and SEL_STAT[1:0] flags are reset: CLK_STAT[3:0]=0000 and SEL_STAT[1:0]=00. CLK_ALARM_RST is an one-shot function.	CLK_STAT[3:0] and SEL_STAT[1:0] flags are active
$\overline{MR}$	1	Reset of data generators and output dividers. The MPC9894 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than two reference clock cycles	Outputs enabled (active)
MBOOT	0	I ² C read/write mode	I ² C boot mode
PRESET	0	Normal Operation	Uses Configuration Register PRESET values on $\overline{MR}$
EX_FB_SEL	0	Selects internal feedback path	Selects external feedback path
MEDIA	0	low output impedance (QA0 to QD1 and QFB)	50 ohms output impedance (QA0 to QD1 and QFB)
SEL_2P5V	0	Selects 3.3 V for core VDD	Selects 2.5 V for core VDD
MSTROUT_EN		All outputs disabled (synchronous with clock being low)	All outputs enabled
Control outputs			
LOCK		PLL is locked	PLL is unlocked
BUSY		The IDCS has initiated a clock switch.	No clock switch currently performed
INT		IDCS status has changed (indicates an assertion of CLK_STAT[3:0] or deassertion of LOCK)	No status change
CLK_STAT[3:0]		Associated clock input not valid	Associated clock input valid
SEL_STAT[1:0]		Encoded value see Table 7	Encoded value see Table 7

OPERATION INFORMATION

Basic functional description

The MPC9894 is a quad-redundancy IDCS clock generator. The redundancy feature allows automatic switching from the reference clock source to a secondary clock source on detection of a failed reference clock. The MPC9894 will detect and report a missing clock on any of its four inputs. Based upon the current idcs mode setting and the qualifier input pins, the MPC9894 will switch to the next qualified secondary clock.

The input clock sources, CLK0, CLK1, CLK2 and CLK3, are assumed to be the same frequency¹ but non-phase-related sources. When a clock switch occurs, the phase alignment to the new clock source will occur over an extended time period, eliminating runt clock output pulses. The maximum rate of phase change is specified in the AC parameter Delta Period per Cycle ($\Delta_{PER/CYC}$). The device uses a fully integrated PLL to generate clock signals from redundant clock sources. The PLL multiplies the input reference clock signal by a variety of values, including 0.25, 0.5, 1, 2, 4 or 8. For a complete list see Table 9. The frequency multiplied clock signal drives four independent output banks. Each output bank is phase-aligned to the input reference clock phase, providing virtually zero-delay capability²

The configuration of the MPC9894 series of clock generators is performed through either the I²C interface or by the pre-set configuration mode. The I²C interface uses a 2 pin interface to transmit clock and data to and from a series of configuration and status registers in the MPC9894.

Definitions

IDCS:

Intelligent Dynamic Clock Switch. The IDCS monitors the clock inputs CLK0, CLK1, CLK2 and CLK3. Upon a failure of the reference clock signal, the IDCS switches to a qualified secondary clock signal and the status flags are set.

1. See Table 39 for clock frequency specification
2. using external feedback

Reference clock signal:

The input clock signal that is selected by the IDCS or IDCS_MODE[2:0] as the input reference to the PLL.

Primary clock:

The input clock signal selected by IDCS_MODE[2:0]. The primary clock may or may not be the reference clock, depending on idcs mode and IDCS status.

Secondary clock:

The input clock signal which will be selected by the IDCS upon an automatic clock switch.

Tertiary, Quaternary clocks:

The input clock signals that will be selected by the IDCS, in turn, after the current secondary clock. This clock selection is based upon a round robin rotational sequence

Manual IDCS mode:

The reference clock input is selected by IDCS_MODE[0xx].

Automatic IDCS mode:

The reference clock signal is determined by the IDCS.

Selected clock:

The SEL_STAT[1:0] flags indicate the reference clock signal.

Qualified clock:

The corresponding CLK_VALID[3:0] signal is logic high, the associated CLK_STAT status bit is logic high and no clock failure is present.

Bit Ordering:

The bit ordering convention used in this document for both pin and register documentation is NAME[7:0] where bit 7 is the most significant bit and 0 is the least significant bit.

DEVICE CONFIGURATION

I²C Configuration and I²C Addressing

The MPC9894 is configured via a series of 8-bit registers. The bits in these registers allow a wide range of control over the operation of the MPC9894 clock generator. These registers are accessed via an I²C interface through which a 7-bit address is sent from the I²C master to select the specific I²C slave device being accessed. The address for this clock driver is found in the first of the MPC9894 I²C registers. The format of this address has a fixed most-significant four bits of binary XXXX (TBD) while the least-significant 3 address bits are read from the 3 ADDR pins. This provides the capability to configure up to 8 clock devices on a single I²C interface.

In addition, activation of the MBOOT pin on power-up or reset initiates a automatic boot sequence allowing the clock generators to be initialized from a I²C compatible EEPROM. In

this case the MPC9894 becomes an I²C master and the configuration bits are filled by the information from the first 6 bytes of the EEPROM. This allows the clock to be configured without a controlling I²C bus master if desired. The PRESET pin allows the device to be configured without a I²C bus master.

The detailed register descriptions are found in the section, I²C Interface and configuration/status register.

IDCS MODE Configuration

Three register bits are used to configure the MPC9894 in either an automatic clock switch mode or into a manual clock select mode. The three mode select bits are defined in Table 3.

IDCS modes 000 through 011 allow manual selection between the four clock sources. IDCS modes 100 through 111 enable the automatic mode of the IDCS.

Table 3. MPC9894 IDCS Configuration

IDCS_MODE [2:0]	Description	Primary Clock	Secondary Clock ^a	Tertiary Clock	Quaternary Clock
000	Manual	CLK0	n/a	n/a	n/a
001		CLK1	n/a	n/a	n/a
010		CLK2	n/a	n/a	n/a
011		CLK3	n/a	n/a	n/a
100	Automatic	CLK0	CLK1	CLK2	CLK3
101		CLK1	CLK2	CLK3	CLK0
110		CLK2	CLK3	CLK0	CLK1
111		CLK3	CLK0	CLK1	CLK2

a. For CLK_VALID[3:0]=1111 and input clock validity

Automatic IDCS Mode

In the automatic mode, the clock failure detection is enabled and the IDCS overwrites the selected clock on a clock failure. The IDCS operation requires PLL_BYPASS=0 and IDCS_MODE[2]=1. The reference clock is handled in a round robin method based upon clock validity and the qualification input CLK_VALID[3:0]. The qualification input is obtained from the four input pins, CLK_VALID[3:0]. If any of the CLK_VALID pins are low the associated clock input will be considered “unqualified” and thus not selected as a reference clock. Alternatively, if a clock input does not have a valid clock signal, it will not be selected and the next qualified and valid clock is selected as the reference clock.

For example, if IDCS_MODE[2:0]=100 (the IDCS is in automatic mode), CLK_VALID[3:0]=1111 and CLK0, CLK1, CLK2 and CLK3 have valid input clock signals then CLK0 is the primary clock and CLK1 is the secondary clock. The IDCS selects the primary clock as the reference clock and the PLL will phase-lock the clock outputs to the CLK0 input. Upon the failure of CLK0 the IDCS will select CLK1 as the reference clock and initiate a switch, making CLK1 the reference clock and CLK2 the secondary clock. If CLK1 fails, the IDCS will switch to CLK2, etc.

A de-asserted CLK_VALID[] pin disables the associated clock input as secondary clock. The associated clock input cannot be selected by the IDCS as secondary clock signal. For instance, if CLK0 is the primary clock and CLK_VALID[3:0]=1101, the IDCS will select CLK2 upon a clock failure of

CLK0 (CLK1 is disabled by the CLK_VALID1 input, allowing external logic to control the IDCS switch logic). If a clock is the reference clock signal and its associated CLK_VALID signal is switched from ‘valid’ to ‘invalid’, the IDCS initiates a clock input switch, selecting the next available clock input (secondary clock).

An invalid clock³ signal triggers the associated clock status output (CLK_STAT[3:0]), independent of the primary and reference clock. These pins go set on a clock failure and remain set (sticky) until the CLK_ALARM_RST pin or the individual alarm reset bits (ALARM_RST[3:0]) are asserted. The CLK_STAT[3:0] outputs are mirrored in the device register 4 for I²C bus access.

After each successful IDCS-commanded switch, the primary clock as set by IDCS_MODE[1xx] is no longer the reference clock. The user may reset the IDCS flags by asserting the individual ALARM_RST[3:0] bits after each IDCS-commanded switch. Activation of ALARM_RST[3:0] does not change the reference clock. A user-commanded change of the primary clock in automatic mode requires a write command to the IDCS_MODE[2:0]=0xx bits (the primary clock and SEL_STAT[1:0] can be freely changed by setting IDCS_MODE[2:0]=1xx). If the reference clock is not the primary clock, a write command to IDCS_MODE[2:0]=1xx will cause the PLL to lock on the primary clock, given the new primary clock is a qualified clock.

3. See “Clock failure detection” on page 329.

Table 4. Input Clock Qualifier and Status Flag

Input Clock	Associated Input Qualifier ^a	Associated Input Clock Status Flag	
		Pin	Register location
CLK0	CLK_VALID0	CLK_STAT0	Device register 5, bit 3
CLK1	CLK_VALID1	CLK_STAT1	Device register 5, bit 4
CLK2	CLK_VALID2	CLK_STAT2	Device register 5, bit 5
CLK3	CLK_VALID3	CLK_STAT3	Device register 5, bit 6

a. The input qualifier logic can be enabled or disabled by setting the QUAL_EN bit in register 3.

Table 5. Input Clock Status CLK_STAT[3:0]

CLK_STAT[]	Description
0	Clock input failure
1	Clock input signal valid

Table 6. Clock Input Qualifier CLK_VALID[3:0]

CLK_VALID[]	Associated Input Clock
0	Not qualified and will not be selected
1	Qualified

The SEL_STAT[1:0] pins indicate which of the four input clocks is the current reference clock. In the automatic mode and in the case of the reference clock failure, the SEL_STAT

flag will indicate a reference clock different from the original primary clock selected by IDCS_MODE[2:0]. The CLK_STAT outputs are mirrored in register 5, bits 1:0 for I²C bus access.

Table 7. SEL_STAT[1:0]

SEL_STAT[1:0]	Selected clock input
00	CLK0
01	CLK1
10	CLK2
11	CLK3

If all four clock inputs are not qualified the VCO will slew to its lowest frequency. This condition will be indicated by the LOCK pin being de-asserted. The MPC9894 will remain in this state until an input clock is restored and the device is reset via the MR pin.

Clock failure detection

The MPC9894 clock failure detection is performed using an input clock amplitude check combined with an activity detector. The following conditions will trigger a failed clock status (CLK_STATn = 0) on any qualified clock (CLK_VALIDn=1). These conditions are:

- 1 Either or both CLKx, $\overline{\text{CLKx}}$ are disconnected from the input clock source and open.
- 2 CLKx and $\overline{\text{CLKx}}$ are shorted together
- 3 Either or both CLKx or $\overline{\text{CLKx}}$ are shorted to GND
- 4 Both CLKx and $\overline{\text{CLKx}}$ are shorted to a power supply
- 5 Amplitude of CLKx or $\overline{\text{CLKx}}$ is less than V_{PP,OK} (see AC specification, Table 36)

In addition, the currently selected clock is checked by a phase-frequency detector after the input divider (P). This is

triggered by a phase step of mae_(Q). This phase detector will issue a failed clock status (CLK_STATn = 0) within 'P' clock cycles.

The IDCS does not detect changes of the reference frequency or the reference frequency being out of the specified input frequency range. This includes errors such as reference frequency drift due to crystal aging etc.

Clearing of IDCS Alarm Flags

The input clock status flags are set by a clock failure and remain set until manually cleared (sticky). Clearing can be done by either of two methods. All status flags can be cleared by the package pin, $\overline{\text{CLK\_ALARM\_RST}}$. Or individual status flags can be cleared via register bits, ALARM_RST[3:0]. The $\overline{\text{CLK\_ALARM\_RST}}$ pin is activated by a negative edge on the pin. This clears all CLK_STAT[3:0] flags and returns the IDCS to the primary clock source. The SEL_STAT[1:0]-selected clock indicator now reflects the IDCS_MODE[2:0] setting.

By using ALARM_RST[3:0] (register 2) individual CLK_STAT[3:0] bits are cleared by writing a logic 0 to the individual bit in this register. It is important to note that this action does not return the IDCS to the primary clock.

IDCS Manual Mode

The manual request IDCS mode is selected by IDCS_MODE[2:0]=0xx. The PLL functions normally and all four inputs clocks are monitored. The reference clock will always be the clock signal selected by IDCS_MODE[1:0] and will be indicated by SEL_STAT[1:0]. A manual-requested clock switch (by changing the IDCS_MODE[0xx] signal) will only be executed if the new clock is valid. The SEL_STAT[1:0] pins/bits should be checked after the manual request to ensure the clock switch occurred.

Interrupt Operation

The MPC9894 pin, $\overline{\text{INT}}$, may be used to interrupt a micro-processor or microcontroller. This open drain output pin goes active or low on any of the following occurrences

- 1 A clock failure as indicated by any of bits 6 thru 3 being set in the status register
- 2 A out-of-lock condition for the PLL as indicated by either the $\overline{\text{LOCK}}$ pin or bit 2 of the status register.

The interrupted processor would then use the I²C interface to read the status register (bit 7) to determine if this MPC9894 generated the interrupt. If the interrupt was caused by this MC9894, the status register would then be analyzed to determine the reason for the interrupt and then the appropriate action taken.

In order for interrupts to occur, the INT_E bit must be set in the Device Configuration and Output Clock Enable Register. Once the interrupt flag has been set, reading of the Status Register clears the INT flag.

Clock Operation on Power-Up

On or after power-up, the MPC9894 must be reset via the $\overline{\text{MR}}$ pin. The MPC9894 may be powered-up in either of three configurations. These configurations are selected by the PRESET pin and MBOOT pin.

If PRESET is low, on release of the $\overline{\text{MR}}$ pin, the MPC9894 powers up in a benign mode with all clock outputs disabled. The device is ready to be and must be programmed via the I²C interface prior to operation.

If the PRESET pin is high on the release of the $\overline{\text{MR}}$ pin, the MPC9894 powers up in a run state. In this case the IDCS is configured for automatic mode, CLK0 to be the primary clock, a divide by 2 on clock bank A and B outputs, a divide by 8 on clock C and D outputs, all clock output banks enabled and interrupts enabled. If using the preset mode, then at least one of the clock inputs must have the correct input frequency prior to $\overline{\text{MR}}$ going high.

Later in this document, tables defining the I²C interface registers describe both configurations. The default (reset) information is for the normal reset operation, while the default (preset) information describes the values for each configuration bit on activation of the PRESET pin. In order to return the MPC9894 to either the preset or reset configuration the $\overline{\text{MR}}$ pin must be activated.

See the Boot Mode section for a description of the MBOOT pin.

PLL Feedback

The MPC9894 may be operated with either an internal or an external PLL feedback path. The selection of internal vs. external feedback is made with the pin, EX_FB_SEL. If external feedback is desired, the EX_FB_SEL pin should be connected to VDD and a connection from QFB/QFB to FB_IN/FB_IN should be made. External feedback provides a known relationship between the clock input and the feedback input for phase synchronization of output clock signals to the clock input. If this phase synchronization is not required, the MPC9894 may be configured for internal feedback by the connection of EX_FB_SEL to ground. In this configuration, the connection from the feedback output to the feedback input is not required. The feedback output may be used as a separate output to produce a reference clock output.

CLOCK OUTPUT TRANSITION

A MPC9894 clock switch, either in IDCS manual or IDCS automatic mode, follows the next positive edge of the newly selected reference clock signal. The positive edge of the feedback clock and the newly selected reference clock edge will start to slew to alignment by adjusting the feedback edge placement a small amount of time in each clock cycle. Table 2 “Clock Switch” shows a failed primary input clock with the MPC9894 switching to and aligning to the secondary clock. This small amount of additional time in each clock cycle will ensure that the output clock does not have any large phase changes or frequency changes in a short period of time. The alignment will be to either 1) the closest edge, either forward or

backward or 2) toward the lagging clock edge. The maximum rate of period change is specified in the AC parameter tables with the parameter of $\Delta_{PER/CYC}$. This parameter implies that the output clock edge will never change more than the specified amount in any one cycle.

The busy signal is used to indicate that the MPC9894 is in the process of slewing to the new input clock alignment. The signal is accessed thru the $\overline{\text{busy}}$ pin and goes set upon a clock switch. The pin is reset once the phase realignment is completed. During the period that $\overline{\text{busy}}$ is active, the configuration register of the MPC9894 should not be written with new configuration data.

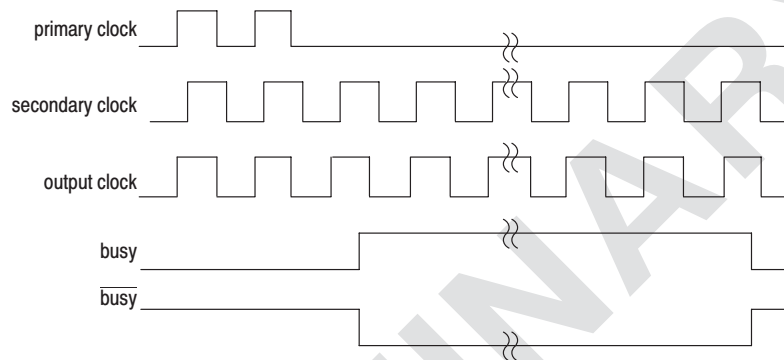


Figure 2. Clock Switch

For example, if the current input clock of 62.5 MHz and the secondary clock are 180 degrees out of phase then the minimum clock transition time can be calculated by

$$t_{\text{cycle}} = 1 \div f_{\text{cycle}} = 1 \div 62.5 \text{ MHz} = 16 \text{ ns}$$

Therefore 180 degree clock difference is

$$t_{\text{cycle}} \div 2 = 8 \text{ ns}$$

Assuming a $\Delta_{PER/CYC}$ of 40ps, then

$$8\text{ns} \div 40 \text{ ps/cycle} = 200 \text{ cycles.}$$

This is the minimum number of cycles that will be required for the alignment to the new clock. The alignment to the new clock phase may occur slower than this but never faster.

The alignment on clock failure is selectable between either 1) the closest edge, either forward or backward or 2) toward the lagging clock edge. The selection of the alignment method is selected in the Slew_Control bit (bit 5) of the Device Configuration and Output Enable Register. This selection allows the user to select the alignment method that best suits the application. The characteristics and subsequent advantages and disadvantages of each method are described as follows.

1 Slew to closest edge

- The alignment is either forward toward the lagging edge or backward toward the leading edge.

- The alignment to the closest edge ensures re-alignment to the new clock input in the minimum time.
- In applications where the input clocks are closely aligned, there is no ambiguity on the direction of clock slew.
- The clock output frequency will either increase or decrease based on direction of clock slew.

2 Slew to lagging edge

- The output frequency always decreases. Thus the clock frequency never violates a maximum frequency specification in the user system.
- when input clocks are closely aligned (within SPO + jitter) the MPC9894 may align to the closest edge or to the lagging edge. In the case of multiple MPC9894s with equivalent clock inputs one MPC9894 may align in one direction while another MPC9894 may align to the opposite direction.

If default values for the Slew_Control is not the configuration desired then the reconfiguration of the slew method should be performed soon after power-up and the configuration should remain fixed from that point.

INPUT AND OUTPUT FREQUENCY CONFIGURATION

Configuring the MPC9894 input and output frequencies requires programming the internal PLL input, feedback and output dividers. The output frequency is represented by the following formula:

$$f_{OUT} = [(f_{REF} \div P) \cdot M] \div N$$

where f_{REF} is the reference frequency of the selected input clock source (reference input), M is the PLL feedback divider and N is a output divider. The PLL input divider P, the feedback divider M and the output divider are configured by the device

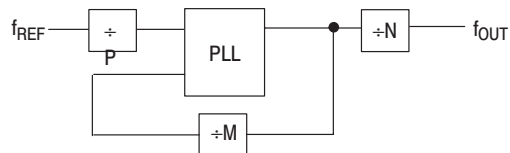


Figure 3. PLL Frequency Calculation

Table 8. Configuration of PLL P, M and N Frequency Dividers

Divider	Available Values	Configuration Through
PLL Input Divider (P)	+1, +2, +3, +4, +5, +6	Input_FB_Div[3:0], Register 4, bit 3:0
PLL Feedback Divider (M)	+8, +12, +16	
PLL Output Divider, Bank A (N _A)	+2, +4, +8, +16	FSEL_B[1:0], Register 1, bit 7:6
PLL Output Divider, Bank B (N _B)	+2, +4, +8, +16	FSEL_B[1:0], Register 1, bit 5:4
PLL Output Divider, Bank C (N _C)	+2, +4, +8, +16	FSEL_C[1:0], Register 1, bit 3:2
PLL Output Divider, Bank D (N _D)	+2, +4, +8, +16	FSEL_D[1:0], Register 1, bit 1:0

The reference frequency f_{REF} and the selection of the PLL input divider (P) and feedback-divider (M) is limited by the specified VCO frequency range. f_{REF} , P and M must be configured to match the VCO frequency range of 340 to 680 MHz in order to achieve stable PLL operation:

$$f_{VCO,MIN} \leq (f_{REF} \div P \cdot M) \leq f_{VCO,MAX}$$

The PLL input divider (P) can be used to situate the VCO in the specified frequency range. The PLL input divider effectively extends the usable input frequency range.

The output frequency for each bank can be derived from the VCO frequency and output divider (N):

$$f_{QA[1:0]} = f_{VCO} \div N_A$$

$$f_{QB[1:0]} = f_{VCO} \div N_B$$

$$f_{QC[1:0]} = f_{VCO} \div N_C$$

$$f_{QD[1:0]} = f_{VCO} \div N_D$$

Table 9 on page 332 illustrates the possible input clock frequency configurations of the MPC9894. Note that The VCO lock range is always 340 MHz to 680 MHz, setting lower and upper boundaries for the frequency range of the device.

Table 9. Input and output frequency ranges

Input_FB_Div[3:0]	P	M	f _{ref} range MHz	Output frequency for any bank A, B, C or D (FSEL_x) and ratio to f _{ref}			
				N=2	N=4	N=8	N=16
0	+1	+16	21.25 - 42.5	8·f _{ref}	4·f _{ref}	2·f _{ref}	f _{ref}
1	+1	+12	28.33 - 56.67	6·f _{ref}	3·f _{ref}	1.5·f _{ref}	0.75·f _{ref}
2	+2	+12	56.66 - 113.34	3·f _{ref}	1.5·f _{ref}	0.75·f _{ref}	0.375·f _{ref}
3	+1	+8	42.5 - 85.0	4·f _{ref}	2·f _{ref}	1·f _{ref}	0.5·f _{ref}
4	+2	+16	42.5 - 85.0	4·f _{ref}	2·f _{ref}	1·f _{ref}	0.5·f _{ref}
5	reserved						
6	+2	+8	85.0 - 170.0	2·f _{ref}	1·f _{ref}	0.5·f _{ref}	0.125·f _{ref}
7	+3	+12	85.0 - 170.0	2·f _{ref}	1·f _{ref}	0.5·f _{ref}	0.125·f _{ref}
8	+4	+16	85.0 - 170.0	2·f _{ref}	1·f _{ref}	0.5·f _{ref}	0.125·f _{ref}
9	reserved						
10	+4	+12	113.32 - 226.64	1.5·f _{ref}	0.75·f _{ref}	0.375·f _{ref}	0.1875·f _{ref}
11	reserved						
12	reserved						
13	reserved						
14	4	+8	170.0 - 340.0	1·f _{ref}	0.5·f _{ref}	0.25·f _{ref}	0.125·f _{ref}
15	6	+12	170.0 - 340.0	1·f _{ref}	0.5·f _{ref}	0.25·f _{ref}	0.125·f _{ref}

I²C INTERFACE AND CONFIGURATION/STATUS REGISTERS

The following tables summarize the bit configurations for the registers accessible via the I²C interface. The register values are read or written over the I²C interface by the I²C Master. This sequence starts with the I²C start command, followed by the I²C device address and read/write byte. This is then followed by the address of the register that is to be accessed. In the case of a write, the register address byte is followed by the

data to be written to that register. In the case of a read, the device will then respond with the data from that register. At the conclusion of the transfer an I²C Stop command is issued by the Master to terminate the transfer. For a complete description of the I²C protocol refer to the v2.1 I²C specification.

Table 10 lists the registers that are accessible via the I²C interface.

Table 10. I²C Registers

Address	Register
0x00	Table 11 “Slave Address (Register 0 – Read Only)”
0x01	Table 12 “Output Configuration Register (Register 1 – Read/Write)”
0x02	Table 14 “Mode Configuration and Alarm Reset Register (Register 2 – Read/Write)”
0x03	Table 17 “Device Configuration and Output Clock Enable Register (Register 3 – Read/Write)”
0x04	Table 22 “Input and Feedback Divider Configuration Register (Register 4 – Read/Write)”
0x05	Table 24 “Status Register (Register 5 – Read Only)”
0x06	Table 25 “Output Power-Up Register (Register 6 – Read/Write)”
0x07	Table 27 “Feedback Power-Up Register (Register 7 – Read/Write)”

Boot Mode

When the I²C boot mode is activated on power-up or reset via the MBOOT pin, the entire set of writable configuration registers are written with a 6-byte sequence. This sequence starts with the Output Configuration Register, and is followed by the Mode Configuration and Alarm Reset Register, the Device Configuration and Output Clock Enable Register, the Input and Feedback Divider Configuration Register, the Output Power-Up Register and the Feedback Power-Up Register. This

equates to the register sequence of 1, 2, 3, 4, 6, 7. This sequence starts with the start command, the device select and read/write(write) byte, followed by the beginning byte address for reading from the EEPROM. This is then followed by the start command, device select and read/write (read) and four current address read bytes. The device address is the binary 7-bit value of 1010000. This I²C sequence is compatible with industry standard I²C bus EEPROMs such as STMicroelectronics M24C01, or equivalent.

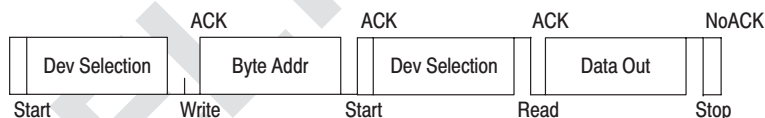


Figure 4. Boot mode random access read

Slave Address Register

The Slave Address register contains the I²C address that is used to determine if the data on the I²C interface is addressed to this device. The seven-bit address is determined with the fixed value of binary XXXX followed by variable bits that are

obtained from the three address pins. The three input pins allow for 8 different addresses for a given clock generator, allowing up to 8 clock generators to be addressed on a single I²C interface.

Table 11. Slave Address (Register 0 - Read Only)

Bit	7	6	5	4	3	2	1	0
Description	not used	ADDR_6	ADDR_5	ADDR_4	ADDR_3	ADDR_2 read from ADDR[2] pin	ADDR_1 read from ADDR[1] pin	ADDR_0 read from ADDR[0] pin
Reset default		x (TBD)	x (TBD)	x (TBD)	x (TBD)			
Preset default		x (TBD)	x (TBD)	x (TBD)	x (TBD)			

Output Configuration Register

The output configuration register is divided into four, 2 bit-groups with each group selecting the divide ratio for output

banks A through bank D (Table 12). For each bank, four output divider settings (+2, +4, +8, +16) are available (Table 12).

Table 12. Output Configuration Register (Register 1 - Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	FSEL_A[1:0]		FSEL_B[1:0]		FSEL_C[1:0]		FSEL_D[1:0]	
Reset default	0	0	0	0	0	0	0	0
Preset default	0	0	0	0	1	0	1	0

Table 13. PLL Output Divider N (FSEL_A to FSEL_D)

FSEL_x[1:0]	Value
00	+2
01	+4
10	+8
11	+16

Mode Configuration Register

The mode configuration register (Table 14) is a read/write register and contains the fields for mode selection as well as alarm reset.

The mode of the MPC9894 may be changed by writing the three least significant Mode Configuration Register bits to the desired value. The current idcs mode of the MPC9894 may be obtained by reading this register.

The alarm reset bits, found in bit positions 6 thru 3, may be

used to individually reset the status flags of register 5. Each of these flag bits are associated with the four clock inputs pins and indicate a failed clock input. Clearing of a clock status flag is performed by writing a logic 1 to the individual bit (or bits if more than one flag is to be cleared). Care should be taken to insure that the idcs mode information is written to the proper value when resetting the clock status bits. The four alarm reset bits always read as a logic 0. If a clock input status flag is cleared and the clock input is still in a failed state, the status flag will go set within 4 clock cycles after being cleared.

Table 14. Mode Configuration and Alarm Reset Register (Register 2 - Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	not used	ALARM_RST[3:0] (See Table 15)				IDCS_MODE[2:0] (See Table 16)		
Reset default	n/a	n/a	n/a	n/a	n/a	0	1	1
Preset default	n/a	n/a	n/a	n/a	n/a	1	0	0

Table 15. Individual reset of CLK_STAT[x] bits

ALARM_RST[x]	Description
0	no action
1	The status flag CLK_STAT[x] is cleared by setting of this bit. (bit always reads as zero)

Table 16. MPC9894 IDCS configuration^a

IDCS_MODE [2:0]	Description	Primary clock	Secondary clock ^b	Tertiary clock ^b	Quaternary clock ^b
000	Manual	CLK0	n/a	n/a	n/a
001		CLK1	n/a	n/a	n/a
010		CLK2	n/a	n/a	n/a
011		CLK3	n/a	n/a	n/a
100	Automatic	CLK0	CLK1	CLK2	CLK3
101		CLK1	CLK2	CLK3	CLK0
110		CLK2	CLK3	CLK0	CLK1
111		CLK3	CLK0	CLK1	CLK2

a. This is a repeat of table 3.

b. For CLK_VALID[3:0]=1111 and input clock validity.

Device Configuration and Output Enable Register

The Device Configuration and Output Enable Register is used to individually enable or disable each bank of outputs. Output banks are enabled by setting the corresponding bit to a logic 1 and disabled by setting the bit to a logic 0 as described in Table 21 “Output Clock Stop/Enable”. The disable logic sets the outputs of the addressed bank synchronously to logic low state ($Qx[] = 0$ and $\overline{Qx[]} = 1$). The clock output enable/stop bits can be set asynchronous to any clock signal without the risk of generating of runt pulses. The PLL feedback output QFB can-

not be disabled when MPC9894 is configured for external feedback.

The Device Configuration Register, bit 6, QUAL_EN is used to enable or disable all clock input qualifier pins. Asserting this bit enables the Clock Qualifier Input Pins CLK_VALID[3:0]. Deasserting this bit disables these pins such that inputs on CLK_VALID[3:0] are ignored.

The INT_E bit, in bit position 7, is used to enable or disable interrupts from occurring on the INT pin. The setting of the interrupt flag (bit 7 of the Status Register) is unaffected by this bit.

Table 17. Device Configuration and Output Clock Enable Register (Register 3 - Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	INT_E	QUAL_EN	Slew_Control	Enable_QFB	ENABLE_QA	ENABLE_QB	ENABLE_QC	ENABLE_QD
Reset default	0	0	0	0	0	0	0	0
Preset default	1	1	0	0	1	1	1	1

3

Table 18. Interrupt Signal ($\overline{\text{INT}}$) Enable INT_E

INT_E	Description
0	Interrupt signal $\overline{\text{INT}}$ is disabled
1	Interrupt signal $\overline{\text{INT}}$ is enabled

Table 19. Input Clock Qualifier Enable QUAL_EN

QUAL_EN	Description
0	CLK_VALID[3:0] are disabled (clock qualifier signals are disabled)
1	CLK_VALID[3:0] are enabled (clocks can be qualified)

Table 20. Slew Control

Slew_Control	Description
0	Clock slew direction on clock switch is toward the closest edge
1	Clock slew direction on clock switch is toward the lagging edge

Table 21. Output Clock Stop/Enable

ENABLE_Qx	Description
0	Output bank x is disabled (clock stop in logic low state)
1	Output bank x is enabled

Input and Feedback Divider Configuration Register

Table 22. Input and Feedback Divider Configuration Register (Register 4 - Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	Reserved	Reserved	Reserved	Reserved	Input_FB_Div[3:0]			
Reset default	n/a	n/a	n/a	n/a	0	0	0	0
Preset default	n/a	n/a	n/a	n/a	0	0	1	1

The Input and Feedback Divider Configuration Register is used to select the input divider value and the feedback divider values. The four bits for Input_FB_Div allow 16 combinations of input and feedback divider ratios. Some input and output

frequency ranges may overlap allowing a choice of PLL closed loop bandwidths. This selection may be useful when PLL devices are cascaded.

Table 23. Input_FB_Div[3:0]

Input_FB_Div[3:0]	Input Divider (P)	Feedback Divider (M)
0000	1	16
0001	1	12
0010	2	12
0011	1	8
0100	2	16
0101	reserved	
0110	2	8
0111	3	12
1000	4	16
1001	reserved	
1010	4	12
1011	reserved	
1100	reserved	
1101	reserved	
1110	4	8
1111	6	12

Device Status Register

The Device Status Register contains a copy of the status SEL_STAT[1:0], LOCK and CLK_STAT[3:0] pins. In addition, bit 7 is an INT flag bit, which is used to indicate a setting of a bit in the CLK_STAT[3:0], a clearing of the LOCK bit and a change in the value of the SEL_STAT[1:0] bits.

The CLK_STAT[3:0] bits are sticky and remain set until

manually reset through the Mode Configuration Register.

The setting of the register INT bit is reflected on the interrupt pin only if interrupts are enabled. Enabling interrupts is done by the setting of the INT_E bit which is located in the Device Configuration Register. Reading of the Status Register clears the INT flag.

Table 24. Status Register (Register 5 - Read Only)

Bit	7	6	5	4	3	2	1	0
Description	INT Inverse of INT signal	CLK_STAT[3:0] Status of CLK3, CLK2, CLK1 and CLK0 (sticky) Copy of CLK_STAT[3:0] signal				LOCK Inverse of LOCK signal	SEL_STAT[1:0] Copy of SEL_STAT[1:0] signal	

Output Power-Up Register

The Output Power-Up Register configures each of the 8 LVPECL outputs for either power-up or a power-down state. The use of these bits allows power consumption to be reduced

when all of the clock outputs are not used. Placing an output in the power-down condition is not synchronous with the clock edges.

Table 25. Output Power-Up Register (Register 6 – Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	PWR_QD1	PWR_QD0	PWR_QC1	PWR_QC0	PWR_QB1	PWR_QB0	PWR_QA1	PWR_QA0
Reset Default	0	0	0	0	0	0	0	0
Preset Default	1	1	1	1	1	1	1	1

Table 26. Clock Output Power-Up Bits

PWR_Qxx	Description
0	Output Power-Down
1	Output Power-Up

3**Feedback Power-Up Register**

The Feedback Power-Up register bit 0 is used to configure the MPC9894 feedback output in either a power-up state or a power-down state. Note this register bit is valid for internal

feedback configuration only. When external feedback is selected QFB is always enabled and in a power-up state. The remaining bits of this register are unused and read as a logic 0.

Table 27. Feedback Power-Up Register (Register 7 – Read/Write)

Bit	7	6	5	4	3	2	1	0
Description								PWR_QFB
Reset Default								0
Preset Default								1

Table 28. Feedback Output Power-Up Bit

PWR_QFB	Description
0	Feedback Output Power-Down
1	Feedback Output Power-Up

IEEE Std.1149.1(JTAG)

This section describes the IEEE Std. 1149.1 compliant Test Access Port (TAP) and Boundary Scan Architecture implementation in the MPC9894. Special Private instructions are provided to assist in production test control. These instructions combined with control of the test mode inputs and the use of

shared inputs and outputs provide for full production test mode access and control.

Test Access Port Interface Signals

Table 29 lists the Test Access Port (TAP) interface signals and their descriptions.

Table 29. TAP Interface Signals

Signal Name	Description	Function	Direction	Active State
TCK	Test Clock	Test logic clock.	Input	-
TMS	Test Mode Select	TAP mode control input.	Input	-
TDI	Test Data In	Serial test instruction/data input.	Input	-
TRST_B	Test Reset Bar	Asynchronous test controller reset.	Input	-
TDO	Test Data Out	Serial test instruction/data output.	Output	-

Instruction Register

Table 30. Instruction Register

Bit Position	4	3	2	1	0
Field	IR				
Capture-IR Value	0	0	0	0	1

Instructions

Table 31 lists the public instructions provided in the implementation and their instruction codes. Public instructions are

accessible by the customer for board test and may also be used for production chip test.

Table 31. Tap Controller Public Instructions

Instruction	Code	Enabled Serial Test Data Path
BYPASS	11111	Bypass Register
CLAMP	01100	Bypass Register
EXTEST	00000	Boundary Scan Register
HIGHZ	01001	Bypass Register
IDCODE	00001	ID Register
SAMPLE	00010	Boundary Scan Register

Boundary-Scan Register

A full description of the boundary scan register may be

found in the BSDL file.

Device Identification Register (0x0281D01D)

Table 32. Device Identification Register

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	version				part number																		manufacturer ID									
Value	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0	0	0	1	1	1	0	1

POWER SUPPLY CONFIGURATION

The MPC9894 operates from either a 3.3V or 2.5V voltage supply for the device core. The pin SEL_2P5V is used to logically indicate the core supply voltage. This selection is done by setting the pin to a logic 1 for 2.5 V or logic 0 for 3.3 V operation.

The input and output supply voltage may be set for either

3.3V or 2.5V and can be individually set for inputs and banks of outputs. Table 33 “Power Supply Configuration” lists the supply pins and what pin or group of pins are associated with each supply. Note, that for output skew and SPO specifications to be valid the input, feedback input and output, and the output bank must all be at the same voltage level.

Table 33. Power supply configuration

Supply voltage	Description	Value
V _{DD}	Positive power supply for the device core, output status and control inputs. (3.3V or 2.5V)	3.3V or 2.5V
V _{DDAB}	Supply voltage for output banks A and B (QA0 through QB1)	3.3V or 2.5V
V _{DDCD}	Supply voltage for output banks A and B (QC0 through QD1) and QFB	3.3V or 2.5V
V _{DDICa}	Supply voltage for differential inputs clock inputs CLK0 to CLK3 and FB_IN	3.3V or 2.5V
V _{DDA}	Clean supply for Analog portions of the PLL (This voltage is derived via a RC filter from the VDD supply)	derived from VDD

a. VDDIC (Supply of FB_IN) must be equal to VDDCD (Supply of QFB) to ensure the SPO specification is met.

Power Supply Sequencing and MR operation

Figure 5 defines the release time and the minimum pulse length for MR pin. The MR release time is based upon the power supply being stable and within V_{DD} specifications. See Table 39 for actual parameter values. The MPC9894 may be

configured after release of reset and the outputs will be stable for use after lock indication is obtained.

V_{DD} must ramp up prior to or concurrent with the other power supply pins. It is recommended that the maximum slew rate for the V_{DD} supply not exceed 0.5 V/μs.

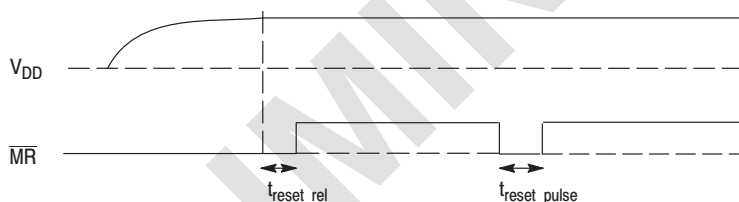


Figure 5. MR operation

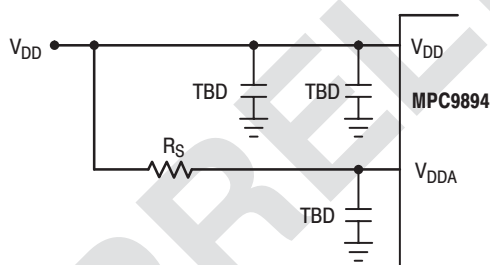


Figure 6. V_{CC} Power Supply Bypass

Power Supply Bypassing

The MPC9894 is a mixed analog/digital product. The differential architecture of the MPC9894 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth

Clock Outputs

The MPC9894 clock outputs are differential LVPECL voltage compatible. The outputs are designed to drive a single 50 ohm impedance load that is properly terminated. The media pin is used to select between either of two output termination techniques.

Selection of media = 0 sets all of the outputs to drive up to 50 ohm parallel terminated (to V_{tt}) transmission lines. With media = 1 the outputs are designed to drive 50 ohm transmission line terminated with a single 100 differential load resistor. Refer to figures 7 and 8 for diagrams of each of these termination techniques. Note, that the traditional output pulldown resistors for emitter follower biasing are not required for the MPC9894. If external feedback is used, the QFB output must be terminated with the same technique as selected with the media pin. Once a termination technique is chosen, that technique must be used for all MPC9894 outputs to guarantee output skew timing.

The recommended termination technique is media = 1. This provides a simpler termination method and also reduces overall power consumption of the MPC9894. Unused outputs may be powered-down via the Output Power-Up and Feedback Power-Up registers to conserve power. If external feedback is selected the programming of the PWR_QFB bit is ignored.

Board Layout Recommendations

TBD

Table 34. ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V_{DD}	Supply Voltage (core)	-0.3	4.0	V	
$V_{DDAB, CD}$	Supply Voltage (differential outputs)	-0.3	4.0	V	
V_{DDIC}	Supply Voltage (differential inputs)	-0.3	4.0	V	
V_{DDA}	Supply Voltage (Analog Supply Voltage)	-0.3	V_{DD}	V	
V_{IN}	DC Input Voltage ^b	-0.3	$V_{DDx}+0.3$	V	
V_{OUT}	DC Output Voltage ^c	-0.3	$V_{DDx}+0.3$	V	
I_{IN}	DC Input Current		± 20	mA	
I_{OUT}	DC Output Current		± 50	mA	
T_S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

b. V_{DDx} references power supply pin associated with specific input pin.

c. V_{DDx} references power supply pin associated with specific output pin.

Table 35. GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage (LVPECL)		$V_{DD} - 2$		V	LVPECL outputs
MM	ESD Protection (Machine Model)	TBD			V	
HBM	ESD Protection (Human Body Model)	TBD			V	
CDM	ESD Protection (Charged Device Model)	TBD			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		TBD		pF	Inputs
θ_{JC}	Thermal Resistance (junction-to-ambient, junction-to-board, junction-to-case)		TBD		°C/W	
T_J	Junction Temperature ^a	-40		110	°C	

a. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MPC9894 to be used in applications requiring industrial temperature range. It is recommended that users of the MPC9894 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 36. DC CHARACTERISTICS ($T_J = -40^\circ\text{C}$ to $+110^\circ\text{C}$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Supply Current for $V_{DD}=2.5V\pm 5\%$ and $V_{DDAB, CD}=2.5V\pm 5\%$						
I_{DD}	Maximum Quiescent Supply Current (Core)		TBD	TBD	mA	V_{DD} pins
$I_{DDAB, CD}^b$	Maximum Quiescent Supply Current, outputs terminated 50Ω to V_{TT}		TBD	TBD	mA	V_{DDAB} and V_{DDCD} pins
I_{DDA}	Maximum Supply Current (Analog Supply)		TBD	TBD	mA	V_{DDA} pin
I_{DDIC}	Maximum Quiescent Supply Current (I/O)		TBD	TBD	mA	V_{DDIC} pins
Supply Current for $V_{DD}=3.3V\pm 5\%$ and $V_{DDAB, CD}=3.3V\pm 5\%$ or $V_{DDAB, CD}=2.5V\pm 5\%$						
I_{DD}	Maximum Quiescent Supply Current (Core)		TBD	TBD	mA	V_{DD} pins
$I_{DDAB, CD}^c$	Maximum Quiescent Supply Current, outputs terminated 50Ω to V_{TT}		TBD	TBD	mA	V_{DDAB} and V_{DDCD} pins
I_{DDA}	Maximum Supply Current (Analog Supply)		TBD	TBD	mA	V_{DDIN} pins
I_{DDIC}	Maximum Quiescent Supply Current (I/O)		TBD	TBD	mA	V_{DDIC} pins

a. DC characteristics are design targets and pending characterization.

b. $I_{DDAB, CD}$ includes current through the output resistors (all outputs terminated to V_{TT}).

c. $I_{DDAB, CD}$ includes current through the output resistors (all outputs terminated to V_{TT}).

Table 37. PECL DC CHARACTERISTICS ($T_J = -40^{\circ}\text{C}$ to $+110^{\circ}\text{C}$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Differential PECL clock inputs (CLKx, $\overline{\text{CLKx}}$ and FB_IN, $\overline{\text{FB\_IN}}$) ^b for $V_{\text{DDIC}}=3.3\text{V}\pm 5\%$ or $V_{\text{DDIC}}=2.5\text{V}\pm 5\%$						
V_{PKPK}	AC Differential Input Voltage ^c	0.2		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage ^d	1.25		$V_{\text{DD}}-0.3$	V	Differential operation
I_{IN}	Input Current ^a			± 100	μA	$V_{\text{PP}}=0.8\text{V}$ and $V_{\text{CMR}}=V_{\text{DDL}}-0.7\text{V}$
Differential PECL clock outputs (QA0 to QD1 and QFB) for $V_{\text{DDAB,CD}}=3.3\text{V}\pm 5\%$ or $V_{\text{DDAB,CD}}=2.5\text{V}\pm 5\%$						
V_{OH}	Output High Voltage	TBD	$V_{\text{DDAB,CD}}-1.0$	TBD	V	Termination 50Ω to V_{TT}
V_{OL}	Output Low Voltage	TBD	$V_{\text{DDAB,CD}}-1.7$	TBD	V	Termination 50Ω to V_{TT}
Z_{OUT}	Output Impedance MEDIA=0 MEDIA=1		TBD 50		Ω Ω	see Figure 7 see Figure 8

a. DC characteristics are design targets and pending characterization.

b. Clock inputs driven by PECL compatible signals.

c. V_{PKPK} is the minimum differential input voltage swing required to maintain AC characteristics.

d. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 38. LVCMOS I/O DC CHARACTERISTICS ($T_J = -40^{\circ}\text{C}$ to $+110^{\circ}\text{C}$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Single ended LVCMOS inputs for $V_{\text{DD}}=3.3\text{V}\pm 5\%$						
V_{IH}	Input High Voltage	2.0		$V_{\text{DD}} + 0.3$	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	$I_{\text{OH}}=-6\text{ mA}$
V_{OL}	Output Low Voltage			0.4	V	$I_{\text{OL}}=6\text{ mA}$
Z_{OUT}	Output Impedance	40		62	Ω	
I_{IN}	Input Current ^b			10	μA	$V_{\text{IN}}=V_{\text{DDL}}$ or GND
Single ended LVCMOS inputs for $V_{\text{DD}}=2.5\text{V}\pm 5\%$						
V_{IH}	Input High Voltage	1.7		$V_{\text{DD}} + 0.3$	V	LVCMOS
V_{IL}	Input Low Voltage			0.7	V	LVCMOS
V_{OH}	Output High Voltage	1.9			V	$I_{\text{OH}}=-6\text{ mA}$
V_{OL}	Output Low Voltage			0.4	V	$I_{\text{OL}}=6\text{ mA}$
Z_{OUT}	Output Impedance	45		70	Ω	
I_{IN}	Input Current ^b			10	μA	$V_{\text{IN}}=V_{\text{DDL}}$ or GND

a. DC characteristics are design targets and pending characterization.

b. Inputs have pull-down resistors affecting the input current.

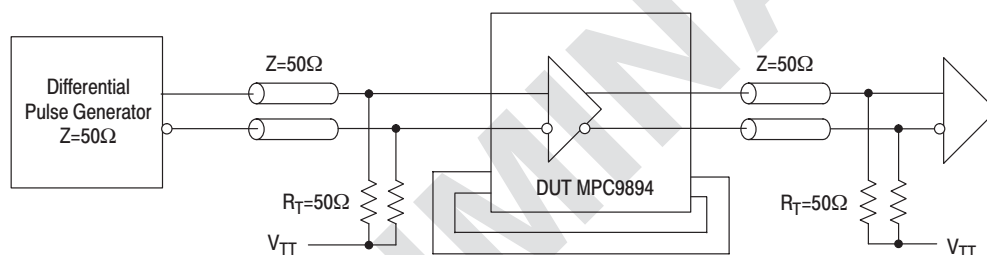
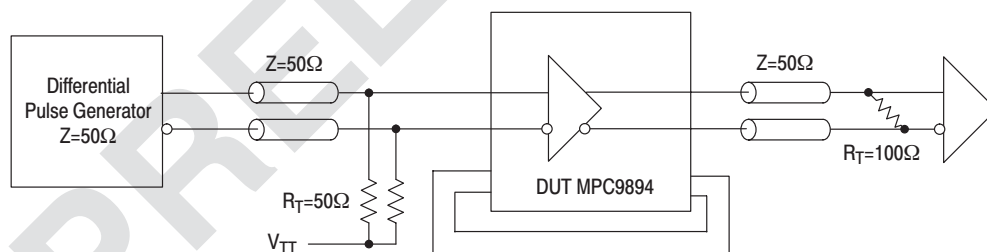
Table 39. AC CHARACTERISTICS ($T_J = -40^{\circ}\text{C}$ to $+110^{\circ}\text{C}$)^{a b}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
$V_{DD}=3.3V\pm5\%$, $V_{DDAB,CD,IC} = 3.3V\pm5\%$ or $V_{DDAB,CD,IC} = 2.5V\pm5\%$						
Input and output timing specification						
f_{ref}	Input reference frequency	21.25 28.33 56.66 42.5 85.0 113.32 170		42.5 56.67 113.34 85 170 226.68 340	MHz MHz MHz MHz MHz MHz MHz	Input_FB_Div[3:0]=0 Input_FB_Div[3:0]=1 Input_FB_Div[3:0]=2 Input_FB_Div[3:0]=3,4 Input_FB_Div[3:0]=6,7,8 Input_FB_Div[3:0]=10 Input_FB_Div[3:0]=14,15
	Input reference frequency in PLL bypass mode ^c			TBD	MHz	PLL bypass
f_{VCO}	VCO frequency range ^d	340		680	MHz	
f_{MAX}	Output Frequency	+2 output +4 output +8 output +16 output	170.0 85.0 42.5 21.25	340.0 170.0 85.0 42.5	MHz MHz MHz MHz	PLL locked
f_{refDC}	Reference Input Duty Cycle	40		60	%	
f_{refacc}	Input Frequency Accuracy ^e			500	ppm	
$mae(\varnothing)$	Misaligned Edge Specification	TBD			ps	
t_r, t_f	Output Rise/Fall Time			TBD	ns	20% to 80%
DC	Output duty cycle	47.5	50	52.5	%	
f_{I2C}	I ² C frequency range			100	kHz	
Differential input and output voltages						
V_{PP}	Differential input voltage ^f (peak-to-peak) (PECL)			1.3	V	
$V_{PP, OK}$	Differential input voltage ^g (peak-to-peak) (PECL)	TBD			V	
$V_{PP, NOK}$	Differential input voltage ^h (peak-to-peak) (PECL)			TBD	V	
$V_{O(P-P)}$	Differential output voltage (peak-to-peak) (PECL)	TBD	0.8		V	
PLL and IDCS specifications						
$t(\varnothing)$	Propagation Delay (static phase offset) CLKX, CLKX to FB_IN, FB_IN	-100		+100	ps	PLL locked with external feedback selected
$t_{sk(O)}$	Output-to-output Skew within a bank ⁱ Output-to-output Skew across a bank ⁱ			50 TBD	ps	
$\Delta_{PER/CYC}$	Rate of change of period ^j	+2 output +4 output +8 output +16 output		+40 +80 +120 +160	ps	slew_control = 1
$\Delta_{PER/CYC}$	Rate of change of period ^k	+2 output +4 output +8 output +16 output		+/-40 +/-80 +/-120 +/-160	ps	slew_control = 0
Jitter and bandwidth specifications						
$t_{JIT(CC)}$	Cycle-to-cycle jitter	RMS (1 σ)		10	ps	
$t_{JIT(PER)}$	Period Jitter	RMS (1 σ)	TBD		ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter	RMS (1 σ)	TBD		ps	
BW	PLL closed loop bandwidth ^l		TBD		kHz	

Table 39. AC CHARACTERISTICS ($T_J = -40^{\circ}\text{C}$ to $+110^{\circ}\text{C}$)^{a b}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
$V_{DD}=3.3V\pm5\%$, $V_{DDAB,CD,IC} = 3.3V\pm5\%$ or $V_{DDAB,CD,IC} = 2.5V\pm5\%$						
MR and PLL Lock						
t_{LOCK}	Maximum PLL Lock Time			10	ms	
t_{reset_ref}	MR hold time on power up	TBD			ns	
t_{reset_pulse}	MR hold time	TBD			ns	

- a. AC characteristics are design targets and pending characterization.
b. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
c. In bypass mode, the MPC9894 divides the input reference clock.
d. The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{ref} = (f_{VCO} \div M) \cdot N$.
e. All Input Clock frequencies must be within this value to guarantee smooth phase transition on input clock switch.
f. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
g. $V_{PP,OK}$ is the minimum differential input voltage swing required for a valid clock signal. Above $V_{PP,OK}$ the input will be detected as a good clock (see IDCS).
h. $V_{PP,NOK}$ is the maximum differential input voltage swing for a guaranteed bad clock. Below $V_{PP,NOK}$ the input will be detected as a failed clock (see IDCS).
i. $V_{DDAB} = V_{DDCD}$.
j. Rate of period change is the maximum change of the clock output signal period T per cycle on a IDCS commanded switch.
k. Rate of period change is the maximum change of the clock output signal period T per cycle on a IDCS commanded switch.
l. -3 dB point of PLL transfer characteristics.

**Figure 7. MPC9894 AC test reference (Media = 0)****Figure 8. MPC9894 AC test reference (Media = 1)**

MPC9894 Pin and Package

Table 40. MPC9894 Pin Listing

Signal Name	Description	Direction	Type	Active State	Supply	Pin
CLK0	Clock0 Positive Input	Input	LVPECL	-	VDDIC	D1
CLK0	Clock0 Negative Input	Input	LVPECL	-	VDDIC	D2
CLK1	Clock1 Positive Input	Input	LVPECL	-	VDDIC	E3
CLK1	Clock1 Negative Input	Input	LVPECL	-	VDDIC	E2
CLK2	Clock2 Positive Input	Input	LVPECL	-	VDDIC	F3
CLK2	Clock2 Negative Input	Input	LVPECL	-	VDDIC	F2
CLK3	Clock3 Positive Input	Input	LVPECL	-	VDDIC	G1
CLK3	Clock3 Negative Input	Input	LVPECL	-	VDDIC	G2
FB_IN	Feedback Clock Positive Input	Input	LVPECL	-	VDDIC	C1
FB_IN	Feedback Clock Negative Input	Input	LVPECL	-	VDDIC	C2
QA0	Positive Differential Clock Output	Output	LVPECL	-	VDDAB	K4
QA0	Negative Differential Clock Output	Output	LVPECL	-	VDDAB	J4
QA1	Positive Differential Clock Output	Output	LVPECL	-	VDDAB	K5
QA1	Negative Differential Clock Output	Output	LVPECL	-	VDDAB	J5
QB0	Positive Differential Clock Output	Output	LVPECL	-	VDDAB	K7
QB0	Negative Differential Clock Output	Output	LVPECL	-	VDDAB	J7
QB1	Positive Differential Clock Output	Output	LVPECL	-	VDDAB	K6
QB1	Negative Differential Clock Output	Output	LVPECL	-	VDDAB	J6
QC0	Positive Differential Clock Output	Output	LVPECL	-	VDDCD	A7
QC0	Negative Differential Clock Output	Output	LVPECL	-	VDDCD	B7
QC1	Positive Differential Clock Output	Output	LVPECL	-	VDDCD	A6
QC1	Negative Differential Clock Output	Output	LVPECL	-	VDDCD	B6
QD0	Positive Differential Clock Output	Output	LVPECL	-	VDDCD	A4
QD0	Negative Differential Clock Output	Output	LVPECL	-	VDDCD	B4
QD1	Positive Differential Clock Output	Output	LVPECL	-	VDDCD	A5
QD1	Negative Differential Clock Output	Output	LVPECL	-	VDDCD	B5
QFB	Positive Differential Clock Output	Output	LVPECL	-	VDDCD	A3
QFB	Negative Differential Clock Output	Output	LVPECL	-	VDDCD	B3
CLK_VALID3	Qualifier for clock input CLK3	Input	LVC MOS	High	VDD	F10
CLK_VALID2	Qualifier for clock input CLK2	Input	LVC MOS	High	VDD	E10
CLK_VALID1	Qualifier for clock input CLK1	Input	LVC MOS	High	VDD	E9
CLK_VALID0	Qualifier for clock input CLK0	Input	LVC MOS	High	VDD	E8
CLK_ALARM_RST	Reset of all four alarm status flags and clock selection status flag	Input	LVC MOS	Low	VDD	F8
PLL_BYPASS	Select PLL of static test mode	Input	LVC MOS	High	VDD	F9
MEDIA	Output impedance control (high = 50ohm)	Input	LVC MOS	High	VDD	E7
SCL	I2C Interface Control, Clock	I/O	LVC MOS	-	VDD	C9
SDA	I2C Interface Control, Data	I/O	LVC MOS	-	VDD	C10
ADDR2	I2C Interface Control, Address 2 (MSB)	Input	LVC MOS	-	VDD	A9
ADDR1	I2C Interface Control, Address 1	Input	LVC MOS	-	VDD	B8
ADDR0	I2C Interface Control, Address 1 (LSB)	Input	LVC MOS	-	VDD	A8

Table 40. MPC9894 Pin Listing

Signal Name	Description	Direction	Type	Active State	Supply	Pin
MR	Device Master Reset	Input	LVC MOS	Low	VDD	D10
LOCK	PLL Lock Indicator	Output	LVC MOS	Low	VDD	G10
CLK_STAT3	Input CLK3 status indicator	Output	LVC MOS	High	VDD	H9
CLK_STAT2	Input CLK2 status indicator	Output	LVC MOS	High	VDD	H10
CLK_STAT1	Input CLK1 status indicator	Output	LVC MOS	High	VDD	G8
CLK_STAT0	Input CLK0 status indicator	Output	LVC MOS	High	VDD	G9
SEL_STAT1	Reference Clock Selection Indicator (MSB)	Output	LVC MOS	High	VDD	K8
SEL_STAT0	Reference Clock Selection Indicator (LSB)	Output	LVC MOS	High	VDD	J8
BUSY	IDCS switch activity indicator	Output	LVC MOS	High	VDD	J10
MBOOT	Activates I2C Boot Sequence	Input	LVC MOS	High	VDD	D8
INT	Indicates any status IDCS change	Output	OD	n/a	VDD	D9
PRESET	Sets preset state	Input	LVC MOS	High	VDD	H7
TMS	JTAG Test Mode Select	Input	LVC MOS	High	VDDIC	D3
TDI	JTAG Test Data Input	Input	LVC MOS	-	VDDIC	H1
TRST	JTAG Test Reset Bar	Input	LVC MOS	Low	VDD	H2
TCK	JTAG Test Clock	Input	LVC MOS	-	VDDIC	G3
TDO	JTAG Test Data Out	Output	LVC MOS	-	VDDIC	J3
SEL_2P5V	Indicate core VDD level, (high = 2.5V, low = 3.3V)	Input	LVC MOS	-	VDD	D7
MSTROUT_EN	Enable all outputs in sync	Input	LVC MOS	High	VDD	K9
PLL_TEST2	PLL Test Bit 2	Input	LVC MOS	-	VDDAB	H4
PLL_TEST1	PLL Test Bit 1	Input	LVC MOS	-	VDDAB	G5
PLL_TEST0	PLL Test Bit 0 (LSB)	Input	LVC MOS	-	VDDCD	D5
TPA	PLL Analog Test Pin	Output	Analog	-	VDDA	E4
EX_FB_SEL	Select feedback mode (high = external)	Input	LVC MOS	-	VDD	C7
VDD	Control Input, Status Output and Core Supply	Power	-	-	VDD	A10, B9, C3, C8, G7, H8, J9, K10
VDDA	Analog Supply	Power	-	-	VDDA	E1
VDDAB	Supply for A and B bank outputs	Power	-	-	VDDAB	H6, J2, K2
VDDCD	Supply for C and D bank outputs	Power	-	-	VDDCD	A1, C4, C6
VDDIC	Supply for input clocks	Power	-	-	VDDIC	B2, H3, K1
GND	Control Input, Status Output and Core Ground	Ground	-	-	GND	A2, B1, B10, C5, D4, D6, E5, E6, F1, F4, F5, F6, F7, G4, G6, H5, J1, K3

Table 41. MPC9894 PIN DIAGRAM

	1	2	3	4	5	6	7	8	9	10
A	VDDCD	GND	QFB	QD0	QD1	QC1	QC0	ADDR0	ADDR2	VDD
B	GND	VDDIC	$\overline{QFB}$	$\overline{QD0}$	$\overline{QD1}$	$\overline{QC1}$	$\overline{QC0}$	ADDR1	VDD	GND
C	FB_IN	$\overline{FB\_IN}$	VDD	VDDCD	GND	VDDCD	EX_FB_SEL	VDD	SCL	SDA
D	CLK0	$\overline{CLK0}$	TMS	GND	PLL_TES T0	GND	SEL_2P5V	MBOOT	$\overline{INT}$	$\overline{MR}$
E	VDDA	$\overline{CLK1}$	CLK1	TPA	GND	GND	MEDIA	CLK_VALID0	CLK_VALID1	CLK_VALID2
F	GND	$\overline{CLK2}$	CLK2	GND	GND	GND	GND	$\overline{CLK\_ALARM\_RST}$	PLL_BYPASS	CLK_VALID3
G	CLK3	$\overline{CLK3}$	TCK	GND	PLL_TES T1	GND	VDD	CLK_STAT1	CLK_STAT0	$\overline{LOCK}$
H	TDI	TRST	VDDIC	PLL_TES T2	GND	VDDAB	PRESET	VDD	CLK_STAT3	CLK_STAT2
J	GND	VDDAB	TDO	$\overline{QA0}$	$\overline{QA1}$	$\overline{QB1}$	$\overline{QB0}$	SEL_STAT0	VDD	$\overline{BUSY}$
K	VDDIC	VDDAB	GND	QA0	QA1	QB1	QB0	SEL_STAT1	MSTROUT_EN	VDD

MPC9894 PROGRAMMING MODEL

Table 42. Slave Address (Register 0 - Read Only)

Bit	7	6	5	4	3	2	1	0
Description	not used	ADDR_6	ADDR_5	ADDR_4	ADDR_3	ADDR_2 read from ADDR[2] pin	ADDR_1 read from ADDR[1] pin	ADDR_0 read from ADDR[0] pin
Reset default		x (TBD)	x (TBD)	x (TBD)	x (TBD)			
Preset default		x (TBD)	x (TBD)	x (TBD)	x (TBD)			

Table 43. Output Configuration Register (Register 1 - Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	FSEL_A[1:0]		FSEL_B[1:0]		FSEL_C[1:0]		FSEL_D[1:0]	
Reset default	0	0	0	0	0	0	0	0
Preset default	0	0	0	0	1	0	1	0

3

Table 44. Mode Configuration and Alarm Reset Register (Register 2 - Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	not used	ALARM_RST[3:0] (See Table 15)				IDCS_MODE[2:0] (See Table 16)		
Reset default	n/a	n/a	n/a	n/a	n/a	0	1	1
Preset default	n/a	n/a	n/a	n/a	n/a	1	0	0

Table 45. Device Configuration and Output Clock Enable Register (Register 3 - Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	INT_E	QUAL_EN	Slew_Control	Enable_QFB	ENABLE_QA	ENABLE_QB	ENABLE_QC	ENABLE_QD
Reset default	0	0	0	0	0	0	0	0
Preset default	1	1	0	0	1	1	1	1

Table 46. Input and Feedback Divider Configuration Register (Register 4 - Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	Reserved	Reserved	Reserved	Reserved	Input_FB_Div[3:0]			
Reset default	n/a	n/a	n/a	n/a	0	0	0	0
Preset default	n/a	n/a	n/a	n/a	0	0	1	1

Table 47. Status Register (Register 5 - Read Only)

Bit	7	6	5	4	3	2	1	0
Description	INT Inverse of INT signal	CLK_STAT[3:0] Status of CLK3, CLK2, CLK1 and CLK0 (sticky) Copy of CLK_STAT[3:0] signal				LOCK Inverse of LOCK signal	SEL_STAT[1:0] Copy of SEL_STAT[1:0] signal	

Table 48. Output Power-Up Register (Register 6 – Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	PWR_QD1	PWR_QD0	PWR_QC1	PWR_QC0	PWR_QB1	PWR_QB0	PWR_QA1	PWR_QA0
Reset Default	0	0	0	0	0	0	0	0
Preset Default	1	1	1	1	1	1	1	1

Table 49. Feedback Power-Up Register (Register 7 – Read/Write)

Bit	7	6	5	4	3	2	1	0
Description								PWR_QFB
Reset Default								0
Preset Default								1

Product Preview

Low Voltage PLL Intelligent Dynamic Clock (IDCS) Switch

The MPC9895 is a 3.3V compatible, PLL based intelligent dynamic clock switch and generator specifically designed for redundant clock distribution systems. The device receives two LVCMOS clock signals and generates 12 phase aligned output clocks. The MPC9895 is able to detect a failing reference clock signal and to dynamically switch to a redundant clock signal. The switch from the failing clock to the redundant clock occurs without interruption of the output clock signal (output clock slews to alignment). The phase bump typically caused by a clock failure is eliminated.

The device offers 12 low skew clock outputs organized into two output banks.

The extended temperature range of the MPC9895 supports telecommunication and networking requirements. The device employs a fully differential PLL design to minimize jitter.

Features

- 12 output LVCMOS PLL clock generator
- 3.3V compatible
- IDCS - on-chip intelligent dynamic clock switch
- Automatically detects clock failure
- Smooth output phase transition during clock failover switch
- 50 - 200 MHz output frequency range
- LVCMOS compatible inputs and outputs
- External feedback enables zero-delay configurations
- Supports networking, telecommunications and computer applications
- Output enable/disable and static test mode (PLL bypass)
- Low skew characteristics: maximum 150 ps¹ output-to-output
- 100 ball MAPBGA package, 1 mm ball pitch
- Ambient temperature range -40°C to +85°C

Functional Description

The MPC9895 is a 3.3V compatible PLL clock driver and clock generator. The clock generator uses a fully integrated PLL to generate clock signals from redundant clock sources. The PLL multiplies the input reference clock signal by 4, 8, 16 or 32. The frequency-multiplied clock drives six bank A outputs and six bank B outputs. Bank A and bank B outputs are phase-aligned. Due to the external PLL feedback, the clock signals of both output banks are also phase-aligned to the selected input reference clock, providing virtually zero-delay capability. The integrated IDCS continuously monitors both clock inputs and indicates a clock failure individually for each clock input. When a false clock signal is detected, the MPC9895 switches to the redundant clock input, forcing the PLL to slowly slew to alignment and not produce any phase bumps at the outputs. Both clock inputs are interchangeable. The automatic switch operation to a restored (fixed) clock signal is also supported. The MPC9895 also provides a manual mode that allows for user-controlled clock switches.

The PLL bypass of the MPC9895 disables the IDCS and PLL-related PLL specifications do not apply. In PLL bypass mode, the MPC9895 is fully static in order to distribute low-frequency clocks for system test and diagnosis. Outputs of the MPC9895 can be disabled (high-impedance state) to isolate the device from the system. Applying output disable also resets the MPC9895. On power-up this reset function needs to be applied for correct operation of the circuitry. Please see the application section for power-on sequence recommendations.

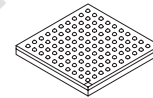
The device is packaged in 100-ball MAPBGA package.

1. Final specification subject to change.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MPC9895

**3.3V IDCS AND
PLL CLOCK GENERATOR**



VF SUFFIX
100 MAPBGA PACKAGE
CASE 1462

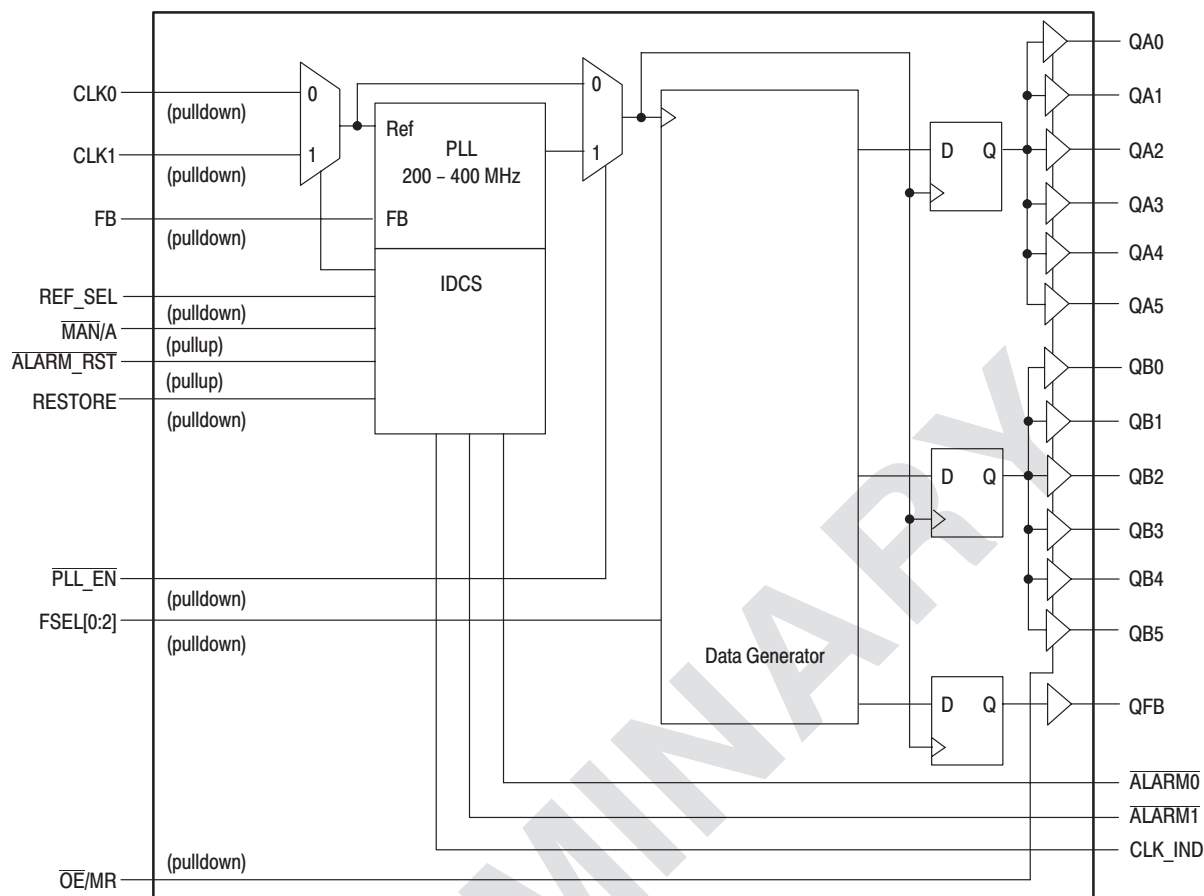


Figure 1. MPC9895 Logic Diagram

Table 1. SIGNAL CONFIGURATIONS

Signal	I/O	Type	Function
CLK0, CLK1	Input	LVC MOS	PLL reference clock inputs
FB	Input	LVC MOS	PLL feedback signal input, connect directly to QFB output
REF_SEL	Input	LVC MOS	Selects the primary reference clock
MAN/A	Input	LVC MOS	Selects switch mode and alarm flag reset
ALARM_RST	Input	LVC MOS	Reset of alarm flags and selected reference clock indicator
RESTORE	Input	LVC MOS	Selects the automatic restore mode
PLL_EN	Input	LVC MOS	Selects PLL or static test mode
FSEL[0:2]	Input	LVC MOS	Clock frequency selection and configuration of clock divider modes
OE/MR	Input	LVC MOS	Output enable/disable, device reset
QA[0:5]	Output	LVC MOS	Bank A clock outputs
QB[0:5]	Output	LVC MOS	Bank B clock outputs
QFB	Output	LVC MOS	Clock feedback output. QFB must be connected to FB for correct operation
ALARM0	Output	LVC MOS	Indicates clock failure on CLK0
ALARM1	Output	LVC MOS	Indicates clock failure on CLK1
CLK_IND	Output	LVC MOS	Indicates currently selected input reference clock
GND	Supply	Ground	Negative power supply
VCC_PLL	Supply	VCC	Positive power supply for the PLL (analog power supply). It is recommended to use an external RC filter for the analog power supply pin VCC_PLL. Please see the application section for details.
VCC	Supply	VCC	Positive power supply for I/O and core

Table 2. FUNCTION TABLE

Control	Default	0	1
Inputs			
PLL_EN	0	PLL enabled. The input to output frequency relationship is according to Table 3 if the PLL is frequency locked.	PLL bypassed and IDCS disabled. The VCO output is replaced by the reference clock signal f _{ref} . The MPC9895 is in manual mode.
MAN/A	1	Manual clock switch mode. IDCS disabled . Clock failure detection and output flags ALARM0, ALARM1, CLK_IND are enabled. Low-to-high transition: ALARM0, ALARM1 and CLK_IND flags are reset: ALARM0=H, ALARM1=H and CLK_IND=REF_SEL.	Automatic clock switch mode. IDCS enabled . Clock failure detection and output flags ALARM0, ALARM1, CLK_IND are enabled. IDCS overrides REF_SEL on a clock failure. IDCS operation requires PLL_EN = 0.
ALARM_RST	1	ALARM0, ALARM1 and CLK_IND flags are reset: ALARM0=H, ALARM1=H and CLK_IND=REF_SEL. ALARM_RST is an one-shot function.	ALARM0, ALARM1 and CLK_IND active
RESTORE	0	RESTORE operation is disabled	The IDCS attempts to automatically restore the primary clock source defined by REF_SEL. This operation requires PLL_EN = 0 and MAN/A=1
REF_SEL	0	Selects CLK0 as the primary clock source	Selects CLK1 as the primary clock source
FSEL[0:2]	00	See Table 3	
OE/MR	0	Outputs enabled (active)	Logic 1: Outputs disabled (high impedance state), reset of data generators and output dividers. The MPC9895 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than two reference clock cycles (CLK0,1). MR/OE does not affect the QFB output.
Outputs (ALARM0, ALARM1, CLK_IND are valid if PLL is locked)			
ALARM0		CLK0 failure	
ALARM1		CLK1 failure	
CLK_IND		CLK0 is the primary clock, CLK1 is the secondary clock	CLK1 is the primary clock, CLK0 is the secondary clock

Table 3. CLOCK FREQUENCY CONFIGURATION

Name	FSEL0	FSEL1	FSEL2	f _{REF} range [MHz]	QAx and QBx		QFB	M	N
					Ratio	f _{QAX} [MHz]			
M16H	0	0	0	6.25—12.5	f _{REF} · 16	100—200	f _{REF}	32	2
M8L	0	1	0	6.25—12.5	f _{REF} · 8	50—100	f _{REF}	32	4
M32	1	0	0	3.125—6.25	f _{REF} · 32	100—200	f _{REF}	64	2
M16L	1	1	0	3.125—6.25	f _{REF} · 16	50—100	f _{REF}	64	4
M8H	0	0	1	12.5—25.0	f _{REF} · 8	100—200	f _{REF}	16	2
M4	0	1	1	12.5—25.0	f _{REF} · 4	50—100	f _{REF}	16	4
	1	0	1	n/a					
	1	1	1	n/a					

Table 4. 100 BALL MAPBGA SIGNAL ALIGNMENT^a

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
MAN/A	A1	FB	C1	CLK1	E1	VCC_PLL	G1	ALARM1	J1
QA5	A2	GND	C2	VCC	E2	GND	G2	VCC	J2
QA4	A3	VCC	C3	VCC	E3	VCC	G3	GND	J3
GND	A4	VCC	C4	GND	E4	GND	G4	VCC	J4
QA3	A5	VCC	C5	GND	E5	GND	G5	VCC	J5
QA2	A6	VCC	C6	GND	E6	GND	G6	GND	J6
VCC	A7	VCC	C7	GND	E7	GND	G7	GND	J7
QA1	A8	VCC	C8	VCC	E8	VCC	G8	VCC	J8
QA0	A9	VCC	C9	GND	E9	GND	G9	VCC	J9
GND	A10	REF_SEL	C10	FSEL0	E10	FSEL2	G10	OE/MR	J10
QFB	B1	CLK0	D1	VCC_PLL	F1	ALARM0	H1	CLK_IND	K1
VCC	B2	VCC	D2	GND	F2	GND	H2	QB5	K2
GND	B3	VCC	D3	VCC	F3	VCC	H3	QB4	K3
VCC	B4	GND	D4	GND	F4	VCC	H4	GND	K4
VCC	B5	GND	D5	GND	F5	VCC	H5	QB3	K5
GND	B6	GND	D6	GND	F6	VCC	H6	QB2	K6
GND	B7	GND	D7	GND	F7	VCC	H7	VCC	K7
VCC	B8	VCC	D8	VCC	F8	VCC	H8	QB1	K8
VCC	B9	GND	D9	GND	F9	VCC	H9	QB0	K9
ALARM_RST	B10	PLL_EN	D10	FSEL1	F10	RESTORE	H10	GND	K10

a. See "MAPBGA Pin Configurations diagram (Bottom View)" on page 357.

Table 5. GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output Termination Voltage		V _{CC} ÷ 2		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C _{PD}	Power Dissipation Capacitance		10		pF	Per output
C _{IN}	Input Capacitance		4.0		pF	Inputs

Table 6. ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	3.9	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} +0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} +0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 7. DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	2.0		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input low voltage			0.8	V	LVC MOS
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -24 \text{ mA}^a$
V_{OL}	Output Low Voltage			0.55 0.30	V V	$I_{OL} = 24 \text{ mA}$ $I_{OL} = 12 \text{ mA}$
Z_{OUT}	Output impedance		14-17		Ω	
I_{IN}	Input Current			± 200	μA	$V_{IN} = V_{CC}$ or GND
I_{CC_PLL}	Maximum PLL Supply Current		2	5	mA	V_{CC_PLL} balls
I_{CC}	Maximum Quiescent Supply Current			4	mA	All V_{CC} balls
V_{TT}	Output termination voltage		$V_{CC} \pm 2$		V	

a. The MPC9895 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines.

Table 8. AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)^{a b}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	FSEL= 000 6.25 FSEL= 010 6.26 FSEL= 100 3.125 FSEL= 110 3.125 FSEL= 001 12.5 FSEL= 011 12.5		12.5 12.5 6.25 6.25 25.0 25.0	MHz MHz MHz MHz MHz MHz	PLL locked
f_{MAX}	Maximum Output Frequency	FSEL= 000 100 FSEL= 010 50 FSEL= 100 100 FSEL= 110 50 FSEL= 001 100 FSEL= 011 50		200 100 200 100 200 100	MHz MHz MHz MHz MHz MHz	PLL locked
f_{refDC}	Reference Input Duty Cycle	40		60	%	
t_r, t_f	CLK0, 1 Input Rise/Fall Time			1.0	ns	0.8 to 2.0V
t_{ϕ}	Propagation Delay (static phase offset, CLKx to FB)		± 3		ns	PLL locked
Δt	Rate of period change (phase slew rate)	FSEL=x0x FSEL=x1x	150 300		ps/cycle	$\overline{MAN}/A = 1$ $\overline{MAN}/A = 1$
N_F	IDCS Switch Delay ^c	1			T	
N_R	IDCS Restore Delay ^d	64			T	
$t_{sk(O)}$	Output-to-output Skew ^e	(within bank) (bank-to-bank)		50 100	ps ps	
DC_O	Output duty Cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter			100	ps	
$t_{JIT(PER)}$	Period Jitter			TBD	ps	
$t_{JIT(\phi)}$	I/O Phase Jitter		± 2		ns	
BW	PLL closed loop bandwidth ^f	FSEL=0x FSEL=1x	TBD TBD		MHz MHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

a. All AC characteristics are design targets and subject to change upon characterization.

b. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

c. Number of input clock cycles for clock failure detection. T=period of the feedback clock signal.

d. Number of consecutive, valid clock cycles of an input clock signal. T=period of the feedback clock signal.

e. See application section for part-to-part skew calculation.

f. -3dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Definitions

IDCS: Intelligent Dynamic Clock Switch. The IDCS monitors both primary and secondary clock signals. Upon a failure of the primary clock signal, the IDCS switches to a valid secondary clock signal and status flags are set.

Reference clock signal ref: The clock signal that is selected by the IDCS or REF_SEL as the input reference to the PLL.

Manual mode: The reference clock frequency is selected by REF_SEL.

Automatic mode: The reference clock frequency is selected by the internal IDCS logic.

Primary clock: The input clock signal selected by REF_SEL. The primary clock may or may not be the reference clock, depending on switch mode and IDCS status.

Secondary clock: The input clock signal not selected by REF_SEL.

Selected clock: The CLK_IND flag indicates the reference clock signal: CLK_IND = 0 indicates CLK0 is the clock reference signal, CLK_IND = 1 indicates CLK1 is the reference clock signal.

Clock failure: A valid clock signal that is stuck (high or low) for at least one input clock period ($N_F > 1$). The primary clock and the secondary clock is monitored for failure. Valid clock signals must be within the AC and DC specification for the input reference clock. A loss of clock is detected if as well as the loss of both clocks. In the case of both clocks are lost, the MPC9895 will set the alarm flags and the VCO will run at its lowest frequency. The PLL will not be locked. The MPC9895 has to be reset by $\overline{OE}/MR$ to recover from this situation, it is recommended to re-apply the startup sequence and to use the manual mode ($\overline{MAN}/A=0$) to select the primary clock.

The MPC9895 does not monitor and detect changes in the input frequency.

Automatic mode and IDCS commanded clock switch

$\overline{MAN}/A = 1$, IDCS enabled: Both primary and secondary clocks are monitored. The first clock failure is reported by its $\overline{ALARMx}$ status flag (clock failure is indicated by a logic low). The $\overline{ALARMx}$ status is flag latched and remains latched until reset by assertion of $\overline{ALARM\_RST}$ (if $RESTORE=0$) or the input clock is fixed (if $RESTORE=1$).

If the clock failure occurs on the primary clock, the IDCS attempts to switch to the secondary clock. The secondary clock signal needs to be valid for a successful switch. CLK_IND indicates the reference clock signal. Upon a successful switch, CLK_IND indicates the reference clock, which may now be different as that originally selected by REF_SEL.

Clock restore operation

If the RESTORE input is asserted ($RESTORE=1$, $\overline{MAN}/A = 1$) the IDCS attempts to restore the primary clock after a clock failure. After a successful IDCS-commanded clock switch, REF_SEL is not equal to CLK_IND. The IDCS continues to monitor the primary and secondary clock. If the primary clock becomes valid for at least 64 consecutive cycles ($N_R > 64$), the IDCS attempts to switch back to the primary clock (restore the primary clock).

Upon a successful clock restore operation, the primary clock is the reference clock, CLK_IND will be equal to REF_SEL and the ALARMx flags are cleared.

If REF_SEL is equal to the CLK_IND flag (no clock failure occurred) the IDCS does not change the selected input clock. Deassertion of RESTORE disables the clock restore option and the clock selection must be reset manually.

Manual mode

$\overline{MAN}/A = 0$, IDCS disabled: PLL functions normally and both clocks are monitored. The reference clock signal will always be the clock signal selected by REF_SEL and will be indicated by CLK_IND. The clock restore feature is disabled in manual mode.

Clock output transition

A clock switch, either in automatic or manual mode, follows the next negative edge of the newly selected reference clock signal. The feedback and newly selected reference clock edge will start to slew to alignment at the next positive edge of both signals. Output runt pulses are eliminated.

Reset

$\overline{ALARM\_RST}$ is asserted by a negative edge. It generates a one-shot reset pulse that clears both $\overline{ALARMx}$ latches and the CLK_IND latch. If both CLK0 and CLK1 are invalid or fail when $\overline{ALARM\_RST}$ is asserted, both $\overline{ALARMx}$ flags will be latched after one FB signal period and CLK_IND will be latched (L) indicating CLK0 is the reference signal. While neither $\overline{ALARMx}$ flag is latched ($\overline{ALARMx} = H$), the CLK_IND can be freely changed with REF_SEL.

$\overline{OE}/MR$: Reset the data generator and output disable.

$\overline{MAN}/A$: The rising edge of $\overline{OE}/MR$ resets $\overline{ALARMx}$ and CLK_IND as $\overline{ALARM\_RST}$ does.

Acquiring frequency lock (startup sequence)

1. On startup, $\overline{OE}/MR$ must be asserted to reset the output dividers. The IDCS should be disabled ($\overline{MAN}/A=0$) and RESTORE should be logic low (disable restore option) during startup. REF_SEL selects the primary clock.
2. Release $\overline{OE}/MR$ and the PLL will attempt to gain lock if the primary clock is present. PLL lock requires the specified lock time.
3. Enable the IDCS automatic mode ($\overline{MAN}/A=1$). The rising edge of the $\overline{MAN}/A$ signal clears the alarm flags and CLK_IND. The IDCS will now report clock failures by asserting ALARMx flags.
4. Enable the restore option ($RESTORE=1$) if needed.

Power Supply Filtering

The MPC9895 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the VCC_PLL (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9895 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (VCC_PLL) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-

locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the VCC_PLL pin for the MPC9895. Figure 2 illustrates a typical power supply filter scheme. The MPC9895 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F . From the data sheet the I_{CC_PLL} current (the current sourced through the VCC_PLL pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 3.0V must be maintained on the VCC_PLL pin. The resistor R_F shown in Figure 2 “VCC_PLL Power Supply Filter” must have a resistance of 9-10 Ω to meet the voltage drop criteria.

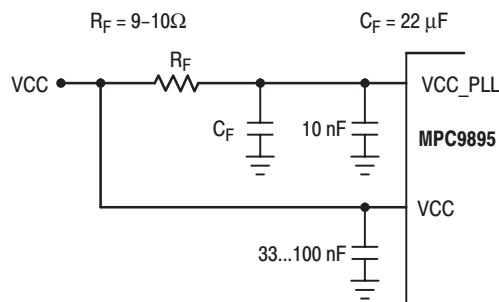


Figure 2. VCC_PLL Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 2 “VCC_PLL Power Supply Filter”, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9895 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC9895 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance

clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC}+2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9895 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9895 clock driver is effectively doubled due to its capability to drive multiple lines.

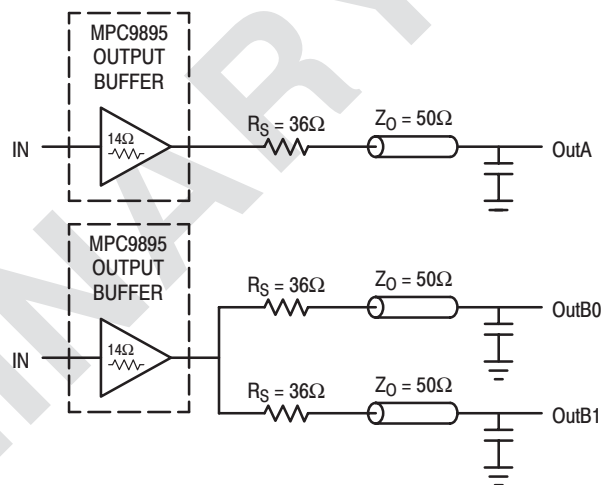


Figure 3. Single versus Dual Transmission Lines

The waveform plots in Figure 4 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9895 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9895. The output waveform in Figure 4 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned} V_L &= V_S (Z_0 \div (R_S + R_0 + Z_0)) \\ Z_0 &= 50\Omega \parallel 50\Omega \\ R_S &= 36\Omega \parallel 36\Omega \\ R_0 &= 14\Omega \\ V_L &= 3.0 (25 \div (18 + 17 + 25)) \\ &= 1.31V \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

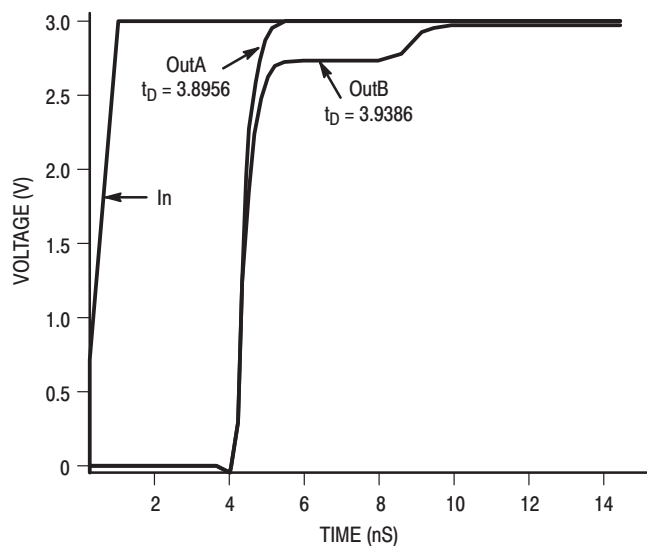


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be

uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

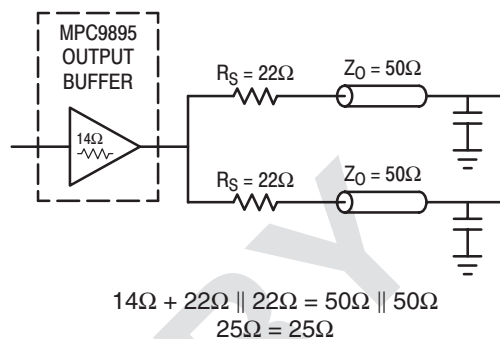


Figure 5. Optimized Dual Line Termination

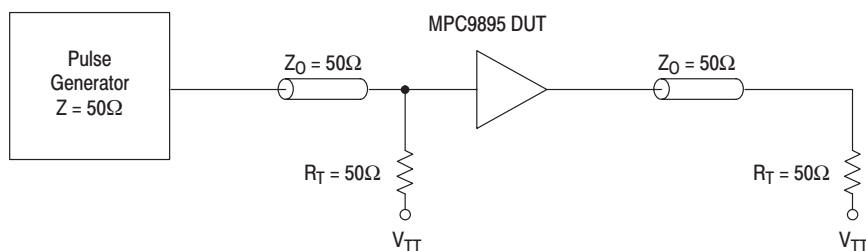
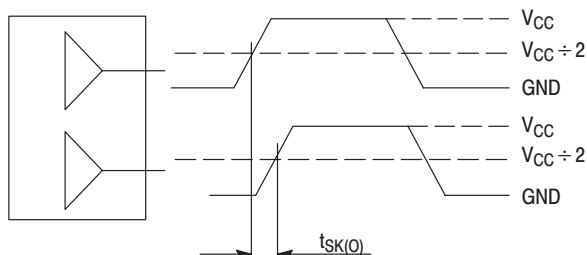
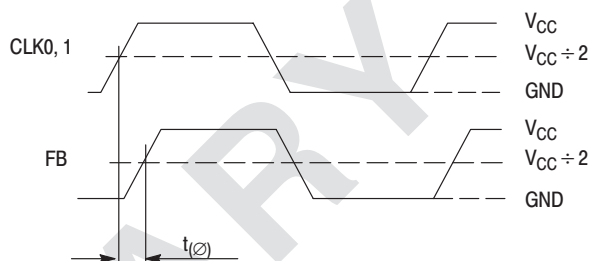
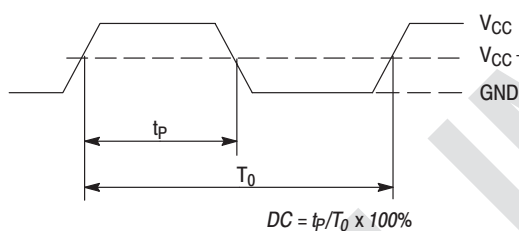


Figure 6. CLK0, CLK1 MPC9895 AC test reference

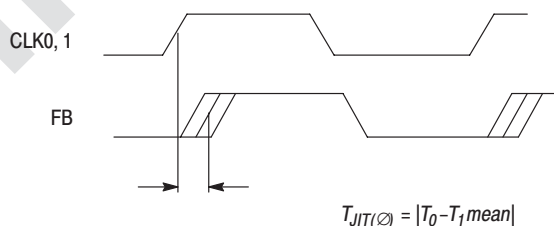


The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 7. Output-to-output Skew $t_{SK(O)}$ Figure 8. Propagation delay ($t_{(\phi)}$, static phase offset) test reference

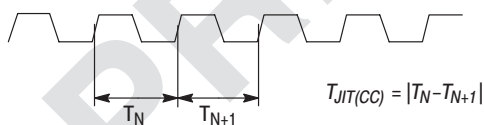
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 9. Output Duty Cycle (DC)



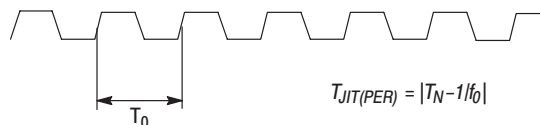
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 10. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 11. Cycle-to-cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 12. Period Jitter

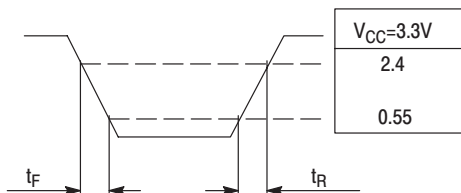


Figure 13. Output Transition Time Test Reference

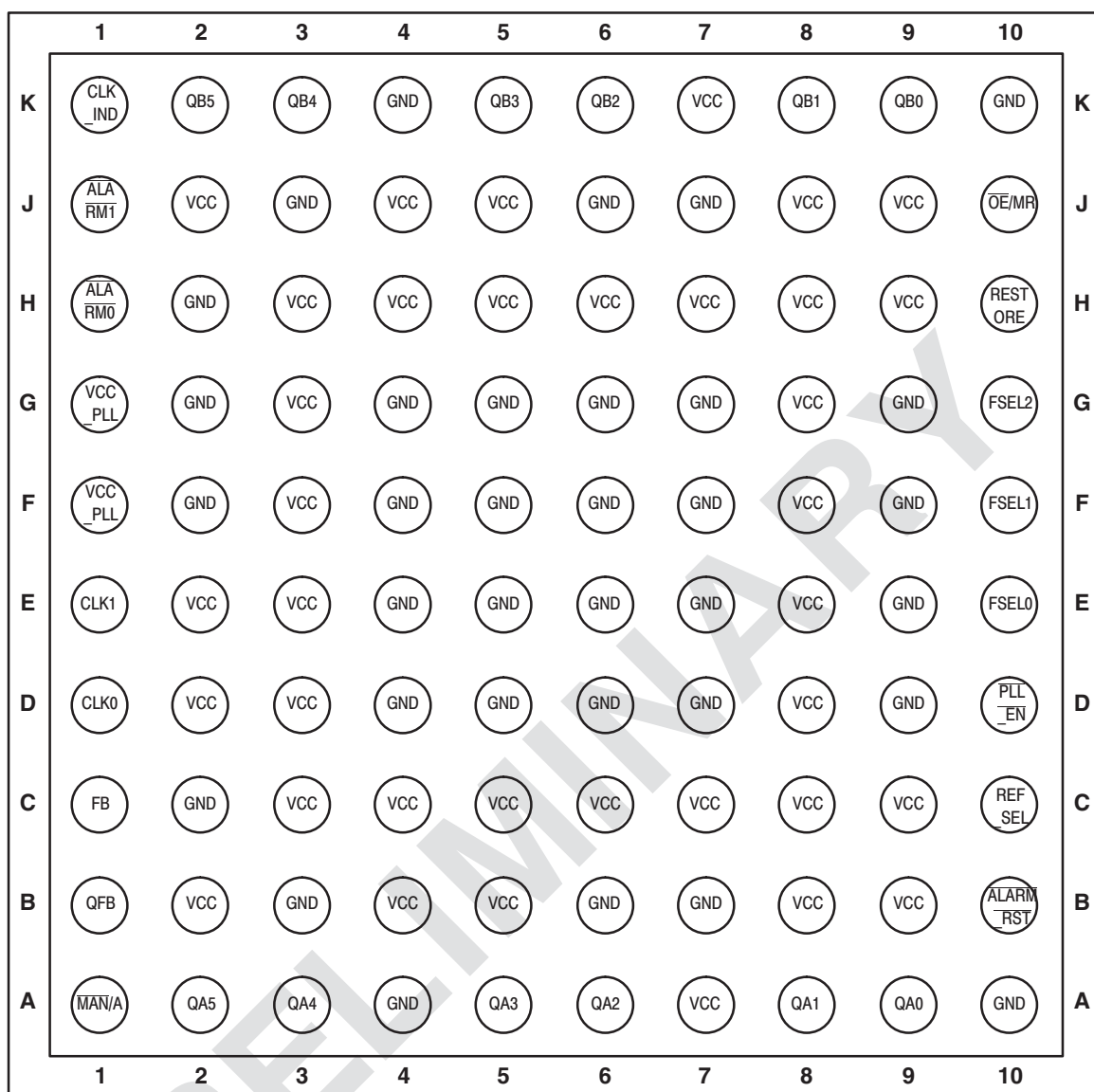


Figure 14. MAPBGA Pin Configurations (Bottom View)

Intelligent Dynamic Clock Switch (IDCS) PLL Clock Driver

The MPC993 is a PLL clock driver designed specifically for redundant clock tree designs. The device receives two differential LVPECL clock signals from which it generates 5 new differential LVPECL clock outputs. Two of the output pairs regenerate the input signals frequency and phase while the other three pairs generate 2x, phase aligned clock outputs. External PLL feedback is used to also provide zero delay buffer performance.

3

- Fully Integrated PLL
- Intelligent Dynamic Clock Switch
- LVPECL Clock Outputs
- LVCMOS Control/Status I/O
- 3.3V Operation
- 32-Lead LQFP Packaging
- $\pm 50\text{ps}$ Cycle-Cycle Jitter

The MPC993 Intelligent Dynamic Clock Switch (IDCS) circuit continuously monitors both input CLK signals. Upon detection of a failure (CLK stuck HIGH or LOW for at least 1 period), the INP_BAD for that CLK will be latched (H). If that CLK is the primary clock, the IDCS will switch to the good secondary clock and phase/frequency alignment will occur with minimal output phase disturbance. The typical phase bump caused by a failed clock is eliminated. (See Application Information section).

MPC993

See Upgrade Product – MPC9993



FA SUFFIX

32-LEAD PLASTIC LQFP PACKAGE
CASE 873A-02

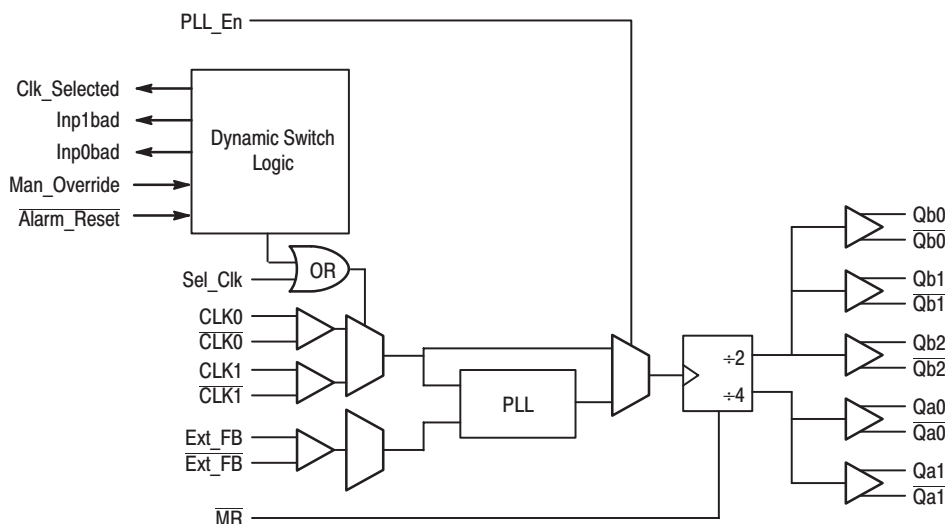


Figure 1. Block Diagram

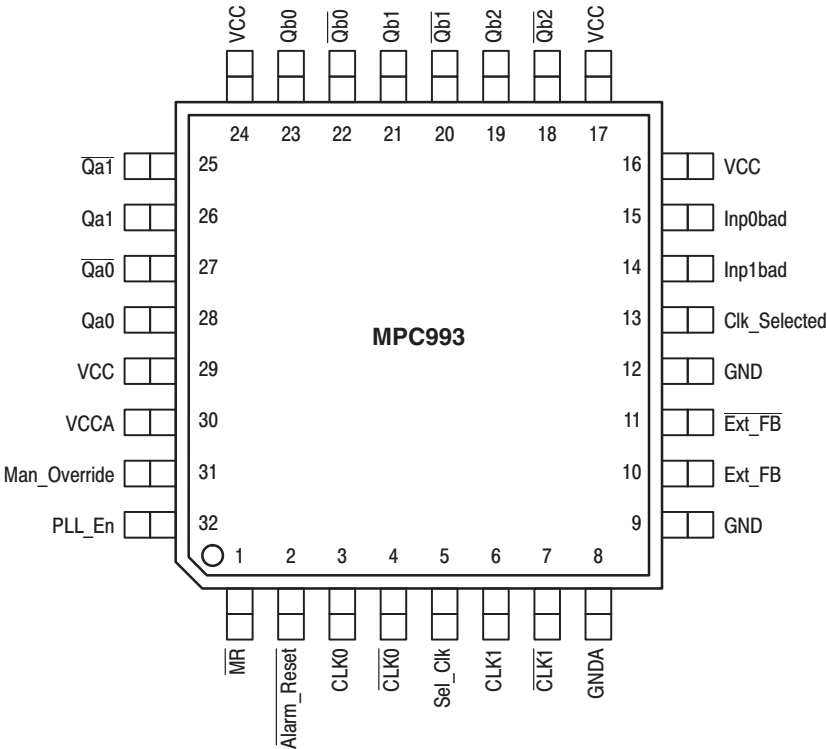


Figure 2. 32-Lead Pinout (Top View)

3.3V PECL DC Characteristics (T_A = -40°C to 85°C, V_{CC} = 3.3V ± 5%)

Symbol	Parameter	Min	Typ	Max	Unit
V _{OH}	Output HIGH Voltage (LVPECL Outputs) (50Ω to V _{CC} - 2.0V)	V _{CC} - 1.025		V _{CC} - 0.80	V
V _{OL}	Output LOW Voltage (LVPECL Outputs) (50Ω to V _{CC} - 2.0V)	V _{CC} - 1.80		V _{CC} - 1.60	V
V _{PP}	Input HIGH Voltage (LVPECL Inputs)	0.3		1.0	V
V _{CMR}	Input LOW Voltage (LVPECL Inputs)	1.0		V _{CC} - 0.6	V
V _{OH}	Output HIGH Voltage (LVCMOS Outputs)	2.4			V
V _{OL}	Output LOW Voltage (LVCMOS Outputs)			0.5	V
V _{IH}	Input HIGH Voltage (LVCMOS Inputs)	2.0		3.3	V
V _{IL}	Input LOW Voltage (LVCMOS Inputs)			0.8	V
I _{IL}	Input LOW Current	0.5			μA
I _{EE}	Power Supply Current		15 80	20 180	mA

3.3V PECL AC Characteristics ($T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 3.3\text{V} \pm 5\%$) (Note 6.)

Symbol	Parameter	Min	Typ	Max	Unit
f_{VCO}	PLL VCO Lock Range (Note 5.)	200		360	MHz
t_{pwi}		25		75	%
t_{pd}	Propagation Delay (Note 1.) CLKn to Q (Bypass) CLKn to Ext_FB (Locked (Note 2.))	1.7 –150	2.3 0	2.8 170	ns ps
t_r/t_f	Output Rise/Fall Time	200		800	ps
t_{skew}	Output Skew Within Bank All Outputs			70 100	ps
Δ_{pe}	Maximum Phase Error Deviation			TBD (Note 3.) TBD (Note 4.)	ps
$\Delta_{per/cycle}$	Rate of Change of Periods 75MHz Output (Note 1., 3.) 150MHz Output (Note 1., 3.) 75MHz Output (Note 1., 4.) 150MHz Output (Note 1., 4.)		20 10 200 100	50 25 400 200	ps/ cycle
t_{pw}	Output Duty Cycle	45		55	%
t_{jitter}	Cycle-to-Cycle Jitter, Standard Deviation (RMS) (Note 1.)			20	ps
t_{lock}	Maximum PLL Lock Time			10	ms

1. Guaranteed, not production tested.
2. Static phase offset between the selected reference clock and the feedback signal.
3. Specification holds for a clock switch between two signals no greater than 400ps out of phase. Delta period change per cycle is averaged over the clock switch excursion. (See Applications Information section on page 361 for more detail)
4. Specification holds for a clock switch between two signals no greater than $\pm\pi$ out of phase. Delta period change per cycle is averaged over the clock switch excursion.
5. The PLL will be unstable using a $\div 2$ output as the feedback. Either one of the $\div 4$ outputs (Qa0 or Qa1) should be used as the feedback signal.
6. PECL output termination is 50 ohms to $V_{CC} - 2.0\text{V}$.

PIN DESCRIPTIONS

Pin Name	I/O	Pin Definition
CLK0, $\overline{\text{CLK0}}$ CLK1, $\overline{\text{CLK1}}$	LVPECL Input LVPECL Input	Differential PLL clock reference (CLK0 pulldown, $\overline{\text{CLK0}}$ pullup) Differential PLL clock reference (CLK1 pulldown, $\overline{\text{CLK1}}$ pullup)
Ext_FB, $\overline{\text{Ext\_FB}}$	LVPECL Input	Differential PLL feedback clock (Ext_FB pulldown, $\overline{\text{Ext\_FB}}$ pullup)
Qa0:1, $\overline{\text{Qa0:1}}$	LVPECL Output	Differential 1x output pairs
Qb0:2, $\overline{\text{Qb0:2}}$	LVPECL Output	Differential 2x output pairs
Inp0bad	LVC MOS Output	Indicates detection of a bad input reference clock 0 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted
Inp1bad	LVC MOS Output	Indicates detection of a bad input reference clock 1 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted
Clk_Selected	LVC MOS Output	'0' if clock 0 is selected, '1' if clock 1 is selected
Alarm_Reset	LVC MOS Input	'0' will reset the input bad flags and align Clk_Selected with Sel_Clk. The input is "one-shotted" (50k Ω pullup)
Sel_Clk	LVC MOS Input	'0' selects CLK0, '1' selects CLK1 (50k Ω pulldown)
Manual_Override	LVC MOS Input	'1' disables internal clock switch circuitry (50k Ω pulldown)
PLL_En	LVC MOS Input	'0' bypasses selected input reference around the phase-locked loop (50k Ω pullup)
$\overline{\text{MR}}$	LVC MOS Input	'0' resets the internal dividers forcing Q outputs LOW. Asynchronous to the clock (50k Ω pullup)
VCCA	Power Supply	PLL power supply
VCC	Power Supply	Digital power supply
GNDA	Power Supply	PLL ground
GND	Power Supply	Digital ground

Applications Information

The MPC993 is a dual clock PLL with on-chip Intelligent Dynamic Clock Switch (IDCS) circuitry.

Definitions

primary clock: The input CLK selected by Sel_Clk.

secondary clock: The input CLK NOT selected by Sel_Clk.

PLL reference signal: The CLK selected as the PLL reference signal by Sel_Clk or IDCS. (IDCS can override Sel_Clk).

Status Functions

Clk_Selected: Clk_Selected (L) indicates CLK0 is selected as the PLL reference signal. Clk_Selected (H) indicates CLK1 is selected as the PLL reference signal.

INP_BAD: Latched (H) when it's CLK is stuck (H) or (L) for at least one Ext_FB period (Pos to Pos or Neg to Neg). Cleared (L) on assertion of Alarm_Reset.

Control Functions

Sel_Clk: Sel_Clk (L) selects CLK0 as the primary clock. Sel_Clk (H) selects CLK1 as the primary clock.

Alarm_Reset: Asserted by a negative edge. Generates a one-shot reset pulse that clears INPUT_BAD latches and Clk_Selected latch.

PLL_En: While (L), the PLL reference signal is substituted for the VCO output.

MR: While (L), internal dividers are held in reset which holds all Q outputs LOW.

Man Override (H)

(IDCS is disabled, PLL functions normally). PLL reference signal (as indicated by Clk_Selected) will always be the CLK selected by Sel_Clk. The status function INP_BAD is active in Man Override (H) and (L).

Man Override (L)

(IDCS is enabled, PLL functions enhanced). The first CLK to fail will latch it's INP_BAD (H) status flag and select the other input as the Clk_Selected for the PLL reference clock. Once latched, the Clk_Selected and INP_BAD remain latched until assertion of Alarm_Reset which clears all latches (INP_BADs are cleared and Clk_Selected = Sel_Clk). NOTE: If both CLKs are bad when Alarm_Reset is asserted, both INP_BADs will be

latched (H) after one Ext_FB period and Clk_Selected will be latched (L) indicating CLK0 is the PLL reference signal. While neither INP_BAD is latched (H), the Clk_Selected can be freely changed with Sel_Clk. Whenever a CLK switch occurs, (manually or by IDCS), following the next negative edge of the newly selected PLL reference signal, the next positive edge pair of Ext_FB and the newly selected PLL reference signal will slew to alignment.

To calculate the overall uncertainty between the input CLKs and the outputs from multiple MPC993's, the following procedure should be used. Assuming that the input CLKs to all MPC993's are exactly in phase, the total uncertainty will be the sum of the static phase offset, max I/O jitter, and output to output skew.

During a dynamic switch, the output phase between two devices may be increased for a short period of time. If the two input CLKs are 400ps out of phase, a dynamic switch of an MPC993 will result in an instantaneous phase change of 400ps to the PLL reference signal without a corresponding change in the output phase (due to the limited response of the PLL). As a result, the I/O phase of a device, undergoing this switch, will initially be 400ps and diminish as the PLL slews to its new phase alignment. This transient timing issue should be considered when analyzing the overall skew budget of a system.

Hot insertion and withdrawal

In PECL applications, a powered up driver will experience a low impedance path through an MPC993 input to its powered down VCC pins. In this case, a 100 ohm series resistance should be used in front of the input pins to limit the driver current. The resistor will have minimal impact on the rise and fall times of the input signals.

Acquiring Frequency Lock

1. While the MPC993 is receiving a valid CLK signal, assert Man_Override HIGH.
2. The PLL will phase and frequency lock within the specified lock time.
3. Apply a HIGH to LOW transition to Alarm_Reset to reset Input Bad flags.
4. De-assert Man_Override LOW to enable Intelligent Dynamic Clock Switch mode.

Intelligent Dynamic Clock Switch (IDCS) PLL Clock Driver

MPC9993



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A

3

Features:

- Fully Integrated PLL
- Intelligent Dynamic Clock Switch
- LVPECL Clock Outputs
- LVCMOS Control I/O
- 3.3V Operation
- 32-Lead LQFP Packaging

Functional Description

The MPC9993 Intelligent Dynamic Clock Switch (IDCS) circuit continuously monitors both input CLK signals. Upon detection of a failure (CLK stuck HIGH or LOW for at least 1 period), the INP_BAD for that CLK will be latched (H). If that CLK is the primary clock, the IDCS will switch to the good secondary clock and phase/frequency alignment will occur with minimal output phase disturbance. The typical phase bump caused by a failed clock is eliminated. (See Application Information section).

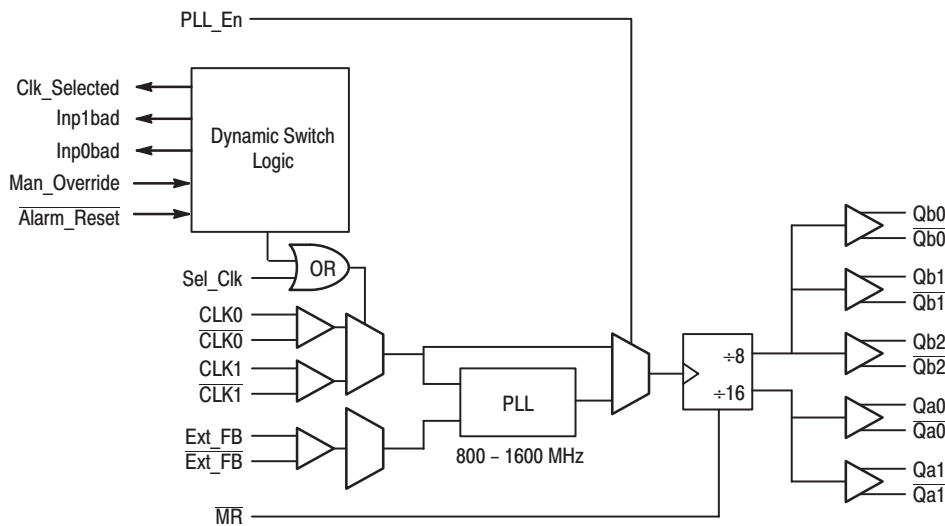


Figure 1. Block Diagram

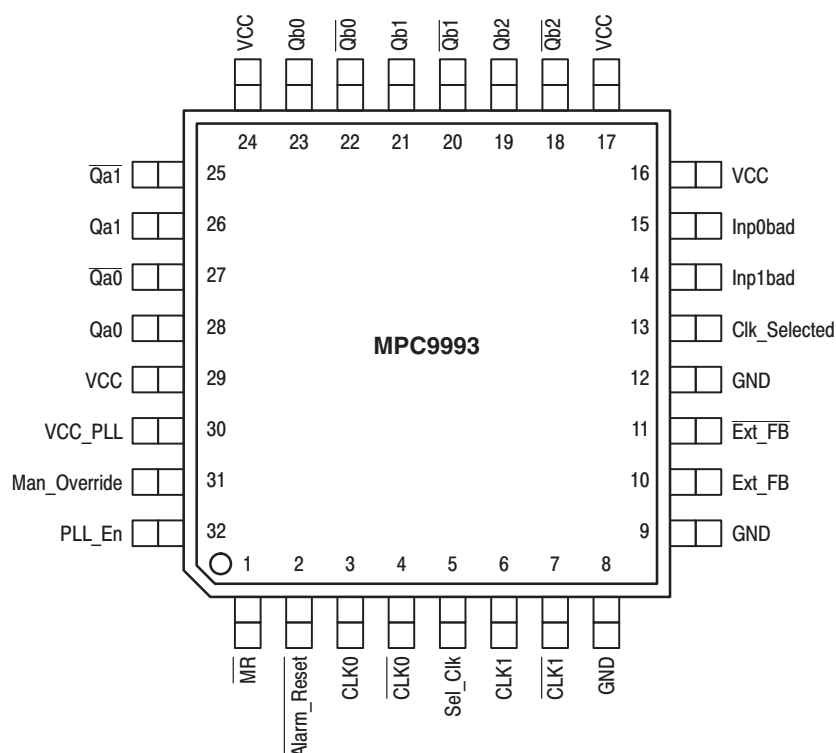


Figure 2. 32-Lead Pinout (Top View)

PIN DESCRIPTIONS

Pin Name	I/O	Pin Definition
CLK0, $\overline{\text{CLK0}}$ CLK1, $\overline{\text{CLK1}}$	LVPECL Input LVPECL Input	Differential PLL clock reference (CLK0 pulldown, $\overline{\text{CLK0}}$ pullup) Differential PLL clock reference (CLK1 pulldown, $\overline{\text{CLK1}}$ pullup)
Ext_FB, $\overline{\text{Ext\_FB}}$	LVPECL Input	Differential PLL feedback clock (Ext_FB pulldown, $\overline{\text{Ext\_FB}}$ pullup)
Qa0:1, $\overline{\text{Qa0:1}}$	LVPECL Output	Differential 1x output pairs
Qb0:2, $\overline{\text{Qb0:2}}$	LVPECL Output	Differential 2x output pairs
Inp0bad	LVC MOS Output	Indicates detection of a bad input reference clock 0 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted
Inp1bad	LVC MOS Output	Indicates detection of a bad input reference clock 1 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted
Clk_Selected	LVC MOS Output	'0' if clock 0 is selected, '1' if clock 1 is selected
Alarm_Reset	LVC MOS Input	'0' will reset the input bad flags and align Clk_Selected with Sel_Clk. The input is "one-shotted" (50k Ω pullup)
Sel_Clk	LVC MOS Input	'0' selects CLK0, '1' selects CLK1 (50k Ω pulldown)
Manual_Override	LVC MOS Input	'1' disables internal clock switch circuitry (50k Ω pulldown)
PLL_En	LVC MOS Input	'0' bypasses selected input reference around the phase-locked loop (50k Ω pullup)
$\overline{\text{MR}}$	LVC MOS Input	'0' resets the internal dividers forcing Q outputs LOW. Asynchronous to the clock (50k Ω pullup)
VCCA	Power Supply	PLL power supply
VCC	Power Supply	Digital power supply
GNDA	Power Supply	PLL ground
GND	Power Supply	Digital ground

Table 1. ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	3.9	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} +0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} +0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 2. GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output termination voltage		V _{CC} - 2		V	
MM	ESD Protection (Machine model)	175			V	
HBM	ESD Protection (Human body model)	1500			V	
CDM	ESD Protection (Charged device model)	1000			V	
LU	Latch-up immunity	100			mA	
C _{IN}	Input Capacitance		4.0		pF	Inputs
θ _{JA}	Thermal resistance junction to ambient JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ _{JC}	Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
T _J	Operating junction temperature ^a (continuous operation) MTBF = 9.1 years			110	°C	

a. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MPC9993 to be used in applications requiring industrial temperature range. It is recommended that users of the MPC9993 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 3. DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ$ to $+85^\circ\text{C}$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS control inputs ($\overline{\text{MR}}$, PLL_En, Sel_Clk, Man_Override, Alarm_Reset)						
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	
V_{IL}	Input Low Voltage			0.8	V	
I_{IN}	Input Current ^a			± 100	μA	$V_{IN}=V_{CC}$ or GND
LVCMOS control outputs (Clk_selected, Inp0bad, Inp1bad)						
V_{OH}	Output High Voltage	2.0			V	$I_{OH}=-24\text{ mA}$
V_{OL}	Output Low Voltage			0.55	V	$I_{OL}= 24\text{ mA}$
LVPECL clock inputs (CLK0, CLK1, Ext_FB) ^b						
V_{PP}	DC Differential Input Voltage ^c	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage ^d	$V_{CC}-1.8$		$V_{CC}-0.3$	V	Differential operation
I_{IN}	Input Current ^a			± 100	μA	$V_{IN}=V_{CC}$ or GND
LVPECL clock outputs (QA[1:0], QB[2:0])						
V_{OH}	Output High Voltage	$V_{CC}-1.20$	$V_{CC}-0.95$	$V_{CC}-0.70$	V	Termination 50Ω to V_{TT}
V_{OL}	Output Low Voltage	$V_{CC}-1.90$	$V_{CC}-1.75$	$V_{CC}-1.45$	V	Termination 50Ω to V_{TT}
Supply Current						
I_{GND}	Maximum Power Supply Current			180	mA	GND pins
I_{CC_PLL}	Maximum PLL Supply Current			15	mA	V_{CC_PLL} pin

a. Inputs have internal pull-up/pull-down resistors affecting the input current.

b. Clock inputs driven by differential LVPECL compatible signals.

c. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics.

d. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 4. AC Characteristics ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Reference Frequency +16 feedback	50		100	MHz	PLL locked
f_{VCO}	VCO Frequency Range ^b +16 feedback	800		1600	MHz	
f_{MAX}	Output Frequency QA[1:0] QB[2:0]	50 100		100 200	MHz MHz	PLL locked
f_{refDC}	Reference Input Duty Cycle	25		75	%	
t_{ϕ}	Propagation Delay SPO, static phase offset ^c CLK0, CLK1 to any Q	-2.0 0.9		+2.0 1.8	ns ns	PLL_EN=1 PLL_EN=0
V_{PP}	Differential input voltage ^d (peak-to-peak)	0.25		1.3	V	
V_{CMR}	Differential input crosspoint voltage ^e	$V_{CC}-1.7$		$V_{CC}-0.3$	V	
$t_{sk(O)}$	Output-to-output Skew within QA[2:0] or QB[1:0] within device			50 80	ps ps	
$\Delta_{per/cycle}$	Rate of change of period QA[1:0] ^f QB[2:0] ^f QA[1:0] ^g QB[2:0] ^g		20 10 200 100	50 25 400 200	ps ps ps ps	
DC	Output Duty Cycle	45	50	55	%	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter RMS (1 σ)			47	ps	
t_{LOCK}	Maximum PLL Lock Time			10	ms	
t_r, t_f	Output Rise/Fall Time	0.05		0.70	ns	20% to 80%

a. AC characteristics apply for parallel output termination of 50Ω to $V_{CC} - 2V$.

b. The input reference frequency must match the VCO lock range divided by the feedback divider ratio (FB): $f_{ref} = f_{VCO} \div FB$.

c. CLK0, CLK1 to Ext_FB.

d. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including SPO and device-to-device skew. Applicable to CLK0, CLK1 and Ext_FB.

e. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the SPO, device and part-to-part skew. Applicable to CLK0, CLK1 and Ext_FB.

f. Specification holds for a clock switch between two input signals (CLK0, CLK1) no greater than 400 ps out of phase. Delta period change per cycle is averaged over the clock switch excursion.

g. Specification holds for a clock switch between two input signals (CLK0, CLK1) at any phase difference ($\pm 180^\circ$). Delta period change per cycle is averaged over the clock switch excursion.

APPLICATIONS INFORMATION

The MPC9993 is a dual clock PLL with on-chip Intelligent Dynamic Clock Switch (IDCS) circuitry.

Definitions

primary clock: The input CLK selected by Sel_Clk.

secondary clock: The input CLK NOT selected by Sel_Clk.

PLL reference signal: The CLK selected as the PLL reference signal by Sel_Clk or IDCS. (IDCS can override Sel_Clk).

Status Functions

Clk_Selected: Clk_Selected (L) indicates CLK0 is selected as the PLL reference signal. Clk_Selected (H) indicates CLK1 is selected as the PLL reference signal.

INP_BAD: Latched (H) when it's CLK is stuck (H) or (L) for at least one Ext_FB period (Pos to Pos or Neg to Neg). Cleared (L) on assertion of Alarm_Reset.

Control Functions

Sel_Clk: Sel_Clk (L) selects CLK0 as the primary clock. Sel_Clk (H) selects CLK1 as the primary clock.

Alarm_Reset: Asserted by a negative edge. Generates a one-shot reset pulse that clears INPUT_BAD latches and Clk_Selected latch.

PLL_En: While (L), the PLL reference signal is substituted for the VCO output.

MR: While (L), internal dividers are held in reset which holds all Q outputs LOW.

Man Override (H)

(IDCS is disabled, PLL functions normally). PLL reference signal (as indicated by Clk_Selected) will always be the CLK selected by Sel_Clk. The status function INP_BAD is active in Man Override (H) and (L).

Man Override (L)

(IDCS is enabled, PLL functions enhanced). The first CLK to fail will latch it's INP_BAD (H) status flag and select the other input as the Clk_Selected for the PLL reference clock. Once latched, the Clk_Selected and INP_BAD remain latched until assertion of Alarm_Reset which clears all latches (INP_BADs are cleared and Clk_Selected = Sel_Clk). NOTE: If both CLKs are bad when Alarm_Reset is asserted, both INP_BADs will be latched (H) after one Ext_FB period and Clk_Selected will be

latched (L) indicating CLK0 is the PLL reference signal. While neither INP_BAD is latched (H), the Clk_Selected can be freely changed with Sel_Clk. Whenever a CLK switch occurs, (manually or by IDCS), following the next negative edge of the newly selected PLL reference signal, the next positive edge pair of Ext_FB and the newly selected PLL reference signal will slew to alignment.

To calculate the overall uncertainty between the input CLKs and the outputs from multiple MPC9993's, the following procedure should be used. Assuming that the input CLKs to all MPC9993's are exactly in phase, the total uncertainty will be the sum of the static phase offset, max I/O jitter, and output to output skew.

During a dynamic switch, the output phase between two devices may be increased for a short period of time. If the two input CLKs are 400ps out of phase, a dynamic switch of an MPC9993 will result in an instantaneous phase change of 400ps to the PLL reference signal without a corresponding change in the output phase (due to the limited response of the PLL). As a result, the I/O phase of a device, undergoing this switch, will initially be 400ps and diminish as the PLL slews to its new phase alignment. This transient timing issue should be considered when analyzing the overall skew budget of a system.

Hot insertion and withdrawal

In PECL applications, a powered up driver will experience a low impedance path through an MPC9993 input to its powered down VCC pins. In this case, a 100 ohm series resistance should be used in front of the input pins to limit the driver current. The resistor will have minimal impact on the rise and fall times of the input signals.

Acquiring Frequency Lock

1. While the MPC9993 is receiving a valid CLK signal, assert Man_Override HIGH.
2. The PLL will phase and frequency lock within the specified lock time.
3. Apply a HIGH to LOW transition to Alarm_Reset to reset Input Bad flags.
4. De-assert Man_Override LOW to enable Intelligent Dynamic Clock Switch mode.

Chapter Four

Clock Synthesizer Data Sheets

Clock Synthesizer Device Index

Device Number	Page
MC12429	370
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MC12439	388
MPC9229	399
MPC9230	408
MPC9239	417
MPC9259	426
MPC926508	434
MPC998	437
MPC9994	444

High Frequency Clock Synthesizer

The MC12429 is a general purpose synthesized clock source. Its internal VCO will operate over a range of frequencies from 200 to 400MHz. The differential PECL output can be configured to be the VCO frequency divided by 1, 2, 4, or 8. With the output configured to divide the VCO frequency by 1, and with a 16.000MHz external quartz crystal used to provide the reference frequency, the output frequency can be specified in 1MHz steps. The PLL loop filter is fully integrated so that no external components are required. The output frequency is configured using a parallel or serial interface.

- 25 to 400MHz Differential PECL Outputs
- ± 25 ps Peak-to-Peak Output Jitter
- Fully Integrated Phase-Locked Loop
- Minimal Frequency Over-Shoot
- Synthesized Architecture
- Serial 3-Wire Interface
- Parallel Interface for Power-Up
- Quartz Crystal Interface
- 28-Lead PLCC and 32-Lead LQFP Packages
- Operates from 3.3V or 5.0V Power Supply

Functional Description

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by 16 before being sent to the phase detector. With a 16MHz crystal, this provides a reference frequency of 1MHz. Although this data sheet illustrates functionality only for a 16MHz crystal, any crystal in the 10–25MHz range can be used.

The VCO within the PLL operates over a range of 200 to 400MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is also applied to the phase detector.

The phase detector and loop filter attempt to force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve loop lock.

The output of the VCO is also passed through an output divider before being sent to the PECL output driver. This output divider (N divider) is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle.

The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated in 50Ω to $V_{CC} - 2.0V$. The positive reference for the output driver and the internal logic is separated from the power supply for the phase-locked loop to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. Normally, on system reset, the $\overline{P\_LOAD}$ input is held LOW until sometime after power becomes valid. On the LOW-to-HIGH transition of $\overline{P\_LOAD}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs to reduce component count in the application of the chip.

The serial interface centers on a fourteen bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See the programming section for more information.

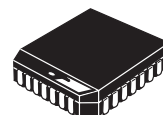
The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. See the programming section for more information.

Rev 7

MC12429

See Upgrade Product – MPC9229

HIGH FREQUENCY PLL CLOCK SYNTHESIZER



FN SUFFIX
28-LEAD PLCC PACKAGE
CASE 776



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A

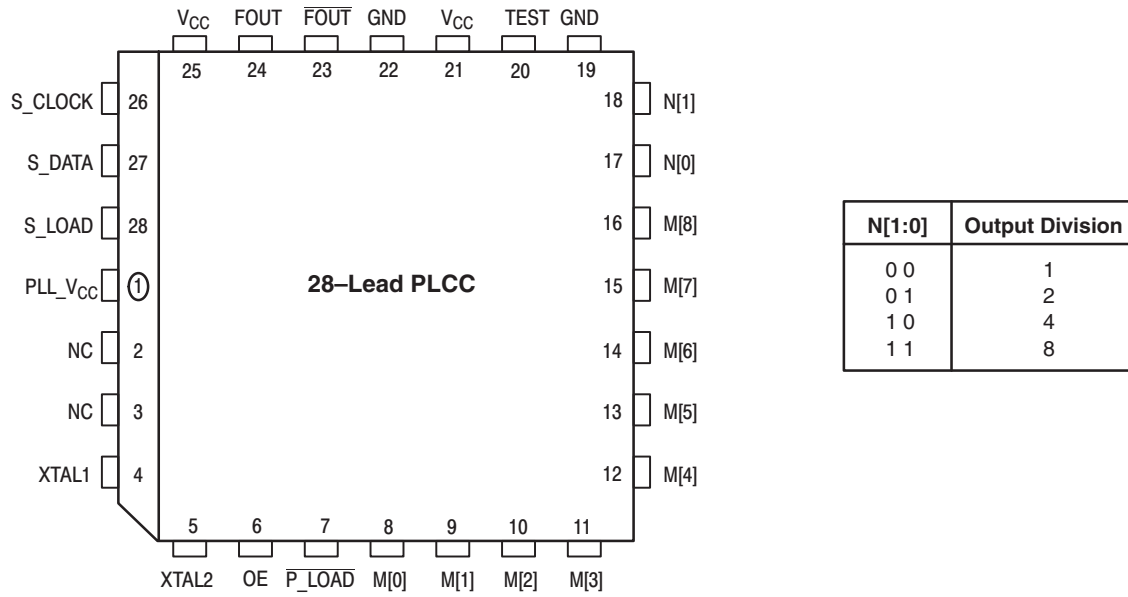


Figure 1. 28-Lead (Top View)

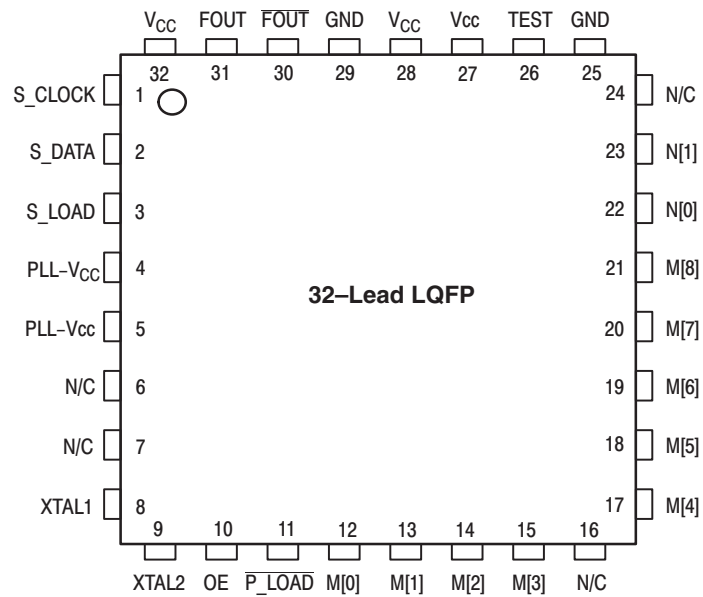


Figure 2. 32-Lead Pinout (Top View)

PIN DESCRIPTIONS

Pin Name	Function
Inputs	
XTAL1, XTAL2	These pins form an oscillator when connected to an external series-resonant crystal.
S_LOAD (Int. Pulldown)	This pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH, thus the data must be stable on the HIGH-to-LOW transition of S_LOAD for proper operation.
S_DATA (Int. Pulldown)	This pin acts as the data input to the serial configuration shift registers.
S_CLOCK (Int. Pulldown)	This pin serves to clock the serial configuration shift registers. Data from S_DATA is sampled on the rising edge.
P_LOAD (Int. Pullup)	This pin loads the configuration latches with the contents of the parallel inputs. The latches will be transparent when this signal is LOW, thus the parallel data must be stable on the LOW-to-HIGH transition of P_LOAD for proper operation. P_LOAD is state sensitive.
M[8:0] (Int. Pullup)	These pins are used to configure the PLL loop divider. They are sampled on the LOW-to-HIGH transition of P_LOAD. M[8] is the MSB, M[0] is the LSB.
N[1:0] (Int. Pullup)	These pins are used to configure the output divider modulus. They are sampled on the LOW-to-HIGH transition of P_LOAD.
OE (Int. Pullup)	Active HIGH Output Enable. The Enable is synchronous to eliminate possibility of runt pulse generation on the F _{OUT} output.
Outputs	
F _{OUT} , $\overline{F_{OUT}}$	These differential positive-referenced ECL signals (PECL) are the output of the synthesizer.
TEST	The function of this output is determined by the serial configuration bits T[2:0].
Power	
V _{CC}	This is the positive supply for the internal logic and the output buffer of the chip, and is connected to +3.3V or 5.0V (V _{CC} = PLL_V _{CC}). Current drain through V _{CC} ≈ 85mA.
PLL_V _{CC}	This is the positive supply for the PLL, and should be as noise-free as possible for low-jitter operation. This supply is connected to +3.3V or 5.0V (V _{CC} = PLL_V _{CC}). Current drain through PLL_V _{CC} ≈ 15mA.
GND	These pins are the negative supply for the chip and are normally all connected to ground.

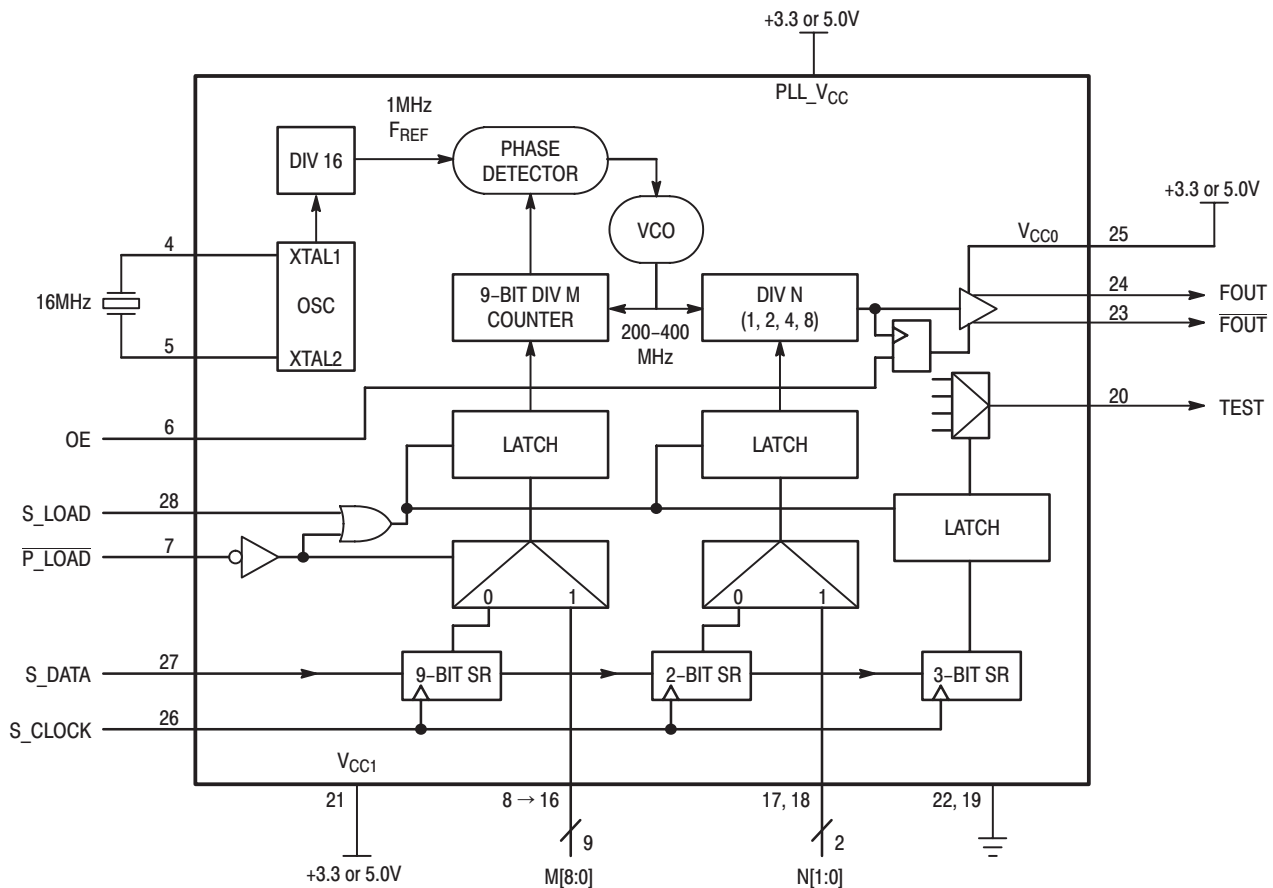


Figure 3. MC12429 Block Diagram (28-Lead PLCC Pinout)

PROGRAMMING INTERFACE

Programming the device amounts to properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can be represented by this formula:

$$F_{OUT} = (F_{XTAL} \div 16) \times M \div N \quad (1)$$

Where F_{XTAL} is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be $200 \leq M \leq 400$ for a 16MHz input reference.

Assuming that a 16MHz reference frequency is used the above equation reduces to:

$$F_{OUT} = M \div N$$

Substituting the four values for N (1, 2, 4, 8) yields:

TABLE A: Output Frequency Range

N	F _{OUT}	OUTPUT FREQUENCY RANGE
1	M	200 – 400 MHz
2	M / 2	100 – 200 MHz
4	M / 4	50 – 100 MHz
8	M / 8	25 – 50 MHz

From these ranges the user will establish the value of N required, then the value of M can be calculated based on the appropriate equation above. For example if an output frequency of 131MHz was desired the following steps would be taken to identify the appropriate M and N values. 131MHz falls within the frequency range set by an N value of 2 so $N[1:0] = 01$. For $N = 2$ $F_{OUT} = M \div 2$ and $M = 2 \times F_{OUT}$. Therefore $M = 131 \times 2 = 262$, so $M[8:0] = 10000110$. Following this same procedure a user can generate any whole frequency desired between 25 and 400MHz. Note that for $N > 2$ fractional values of F_{OUT} can be realized. The size of the programmable frequency steps (and thus the indicator of the fractional output frequencies achievable) will be equal to $F_{XTAL} \div 16 \div N$.

For input reference frequencies other than 16MHz the set of appropriate equations can be deduced from equation 1. For computer applications another useful frequency base would be 16.666MHz. From this reference one can generate a family of output frequencies at multiples of the 33.333MHz PCI clock. As an example to generate a 133.333MHz clock from a 16.666MHz reference the following M and N values would be used:

$$F_{OUT} = 16.666 \div 16 \times M \div N = 1.0416 \times M \div N$$

$$\text{Let } N = 2, \quad M = 133.3333 \div 1.0416 \times 2 = 256$$

The value for M falls within the constraints set for PLL stability, therefore $N[1:0] = 01$ and $M[8:0] = 10000000$. If the value for M

fell outside of the valid range a different N value would be selected to try to move M in the appropriate direction.

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the $\overline{P\_LOAD}$ signal such that a LOW to HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the $\overline{P\_LOAD}$ signal is LOW the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14 bit shift register. Note that the $\overline{P\_LOAD}$ signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 4 illustrates the timing diagram for both a parallel and a serial load of the MC12429 synthesizer.

M[8:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents FOUT, the CMOS output may not be able to toggle fast enough for some of the higher output frequencies. The T2, T1

and T0 control bits are preset to '000' when $\overline{P\_LOAD}$ is LOW so that the PECL FOUT outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MC12429 itself. However the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MC12429 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clock tree. Figure 5 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 250MHz or less. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 125MHz as the minimum divide ratio of the N counter is 2. Note that the M counter output on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.

T2	T1	T0	TEST (Pin 20)
0	0	0	SHIFT REGISTER OUT
0	0	1	HIGH
0	1	0	FREF
0	1	1	M COUNTER OUT
1	0	0	FOUT
1	0	1	LOW
1	1	0	MCNT
1	1	1	FOUT/4

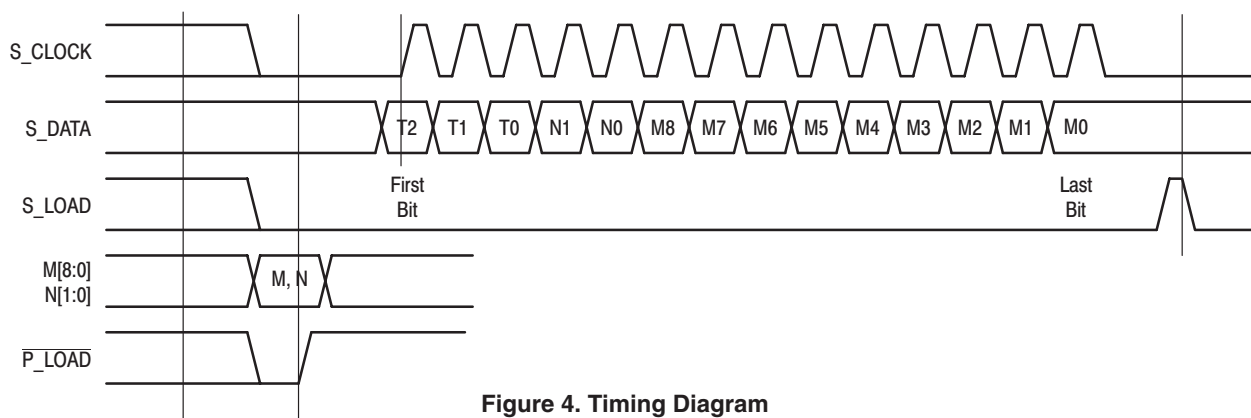
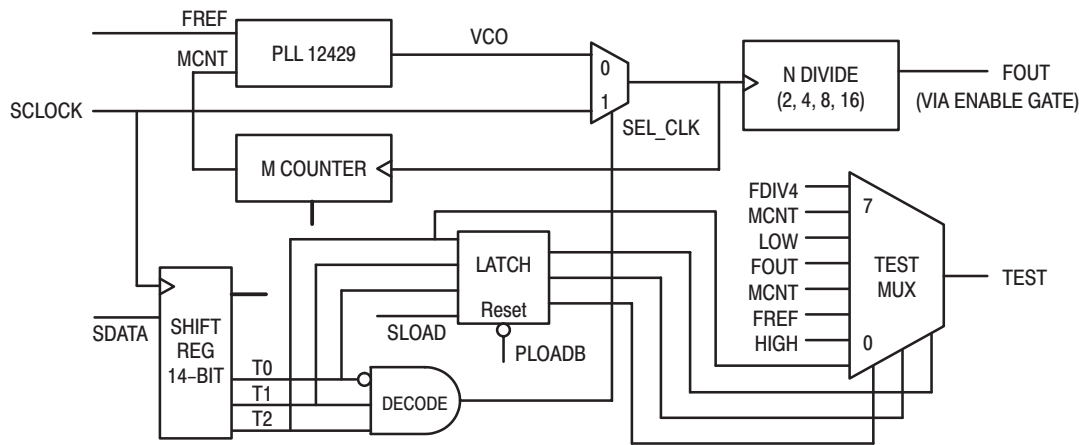


Figure 4. Timing Diagram



- T2=T1=1, T0=0: Test Mode (PLL bypass)
- SCLOCK is selected, MCNT is on TEST output, SCLOCK DIVIDE BY N is on FOUT pin

PLOADB acts as reset for test pin latch. When latch reset T2 data is shifted out TEST pin.

Figure 5. Serial Test Clock Block Diagram (PLL bypass)

4

DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$)

Symbol	Characteristic	0°C			25°C			70°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.2			2.2			2.2			V	
V_{IL}	Input LOW Voltage			0.8			0.8			0.8	V	
I_{IN}	Input Current			1.0			1.0			1.0	mA	
V_{OH}	Output HIGH Voltage TEST	2.5			2.5			2.5			V	$I_{OH} = -0.8mA$
V_{OL}	Output LOW Voltage TEST			0.4			0.4			0.4	V	$I_{OL} = 0.8mA$
V_{OH}	Output HIGH Voltage ¹ : FOUT, FOUT	2.28		2.60	2.32		2.49	2.38		2.565	V	$V_{CC0} = 3.3V^2$
V_{OL}	Output LOW Voltage ¹ : FOUT, FOUT	1.35		1.67	1.35		1.67	1.35		1.70	V	$V_{CC0} = 3.3V^2$
I_{CC}	Power Supply Current V_{CC} PLL_ V_{CC}		85 15	100 20		85 15	100 20		85 15	100 20	mA	

1. 50Ω to $V_{CC} - 2.0V$ termination.

2. Output levels will vary 1:1 with V_{CC0} variation.

DC CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$)

Symbol	Characteristic	0°C			25°C			70°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{IH}	Input HIGH Voltage	3.5			3.5			3.5			V	
V_{IL}	Input LOW Voltage			0.8			0.8			0.8	V	
I_{IN}	Input Current			1.0			1.0			1.0	mA	
V_{OH}	Output HIGH Voltage TEST	2.5			2.5			2.5			V	$I_{OH} = -0.8mA$
V_{OL}	Output LOW Voltage TEST			0.4			0.4			0.4	V	$I_{OL} = 0.8mA$
V_{OH}	Output HIGH Voltage ¹ : FOUT, FOUT	3.98		4.30	4.02		4.19	4.08		4.265	V	$V_{CC0} = 5.0V^2$
V_{OL}	Output LOW Voltage ¹ : FOUT, FOUT	3.05		3.37	3.05		3.37	3.05		3.40	V	$V_{CC0} = 5.0V^2$
I_{CC}	Power Supply Current V_{CC} PLL_ V_{CC}		85 15	100 20		85 15	100 20		85 15	100 20	mA	

1. 50Ω to $V_{CC} - 2.0V$ termination.

2. Output levels will vary 1:1 with V_{CC0} variation.

AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V}$ to $5.0\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Max	Unit	Condition
F_{MAXI}	Maximum Input Frequency S_CLOCK Xtal Oscillator	10	10 20	MHz	Note 3.
F_{MAXO}	Maximum Output Frequency VCO (Internal) FOUT	200 25	400 400	MHz	Note 4.
t_{LOCK}	Maximum PLL Lock Time		10	ms	
t_{jitter}	Period Deviation (Peak-to-Peak)		± 25	ps	Note 4., See Applications Section
t_s	Setup Time S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to $\overline{\text{P\_LOAD}}$	20 20 20		ns	
t_h	Hold Time S_DATA to S_CLOCK M, N to $\overline{\text{P\_LOAD}}$	20 20		ns	
tpw_{MIN}	Minimum Pulse Width S_LOAD $\overline{\text{P\_LOAD}}$	50 50		ns	Note 4.
t_r, t_f	Output Rise/Fall FOUT	300	800	ps	20%–80%, Note 4.

3. 10MHz is the maximum frequency to load the feedback device registers. S_CLOCK can be switched at higher frequencies when used as a test clock in TEST_MODE 6.
4. 50Ω to $V_{CC} - 2.0\text{V}$ pulldown.

APPLICATIONS INFORMATION

Using the On-Board Crystal Oscillator

The MC12429 features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MC12429 as possible to avoid any board level parasitics. To facilitate co-location surface mount crystals are recommended, but not required. Because the series resonant design is affected by capacitive loading on the xtal terminals loading variation introduced by crystals from different vendors could be a potential issue. For crystals with a higher shunt capacitance it may be required to place a resistance across the terminals to suppress the third harmonic. Although typically not required it is a good idea to layout the PCB with the provision of adding this external resistor. The resistor value will typically be between 500 and 1K Ω .

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately most crystals are characterized in a parallel resonant mode. Fortunately there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result a parallel resonant crystal can be used with the MC12429 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application this level of inaccuracy is immaterial. Table 1 below specifies the performance requirements of the crystals to be used with the MC12429.

Table 5. Recommended Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	± 75 ppm at 25°C
Frequency/Temperature Stability	± 150 pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80 Ω
Correlation Drive Level	100 μ W
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

Power Supply Filtering

The MC12429 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MC12429 provides separate power

supplies for the digital circuitry (V_{CC}) and the internal PLL (PLL_VCC) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the PLL_VCC pin for the MC12429.

Figure 6 illustrates a typical power supply filter scheme. The MC12429 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the PLL_VCC pin of the MC12429. From the data sheet the I_{PLL_VCC} current (the current sourced through the PLL_VCC pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the PLL_VCC pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 6 must have a resistance of 10–15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

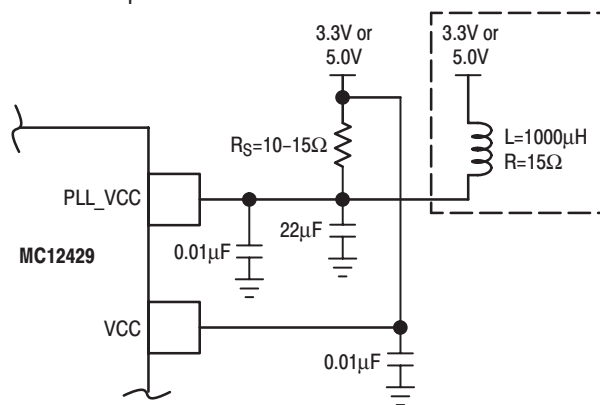


Figure 6. Power Supply Filter

A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. Figure 6 shows a 1000 μ H choke, this value choke will show a significant impedance at 10KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the PLL_VCC pin a low DC resistance inductor is required (less than 15 Ω). Generally the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering.

The MC12429 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 7 shows a representative board layout for the MC12429. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in

Figure 7 is the low impedance connections between VCC and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the 12429 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

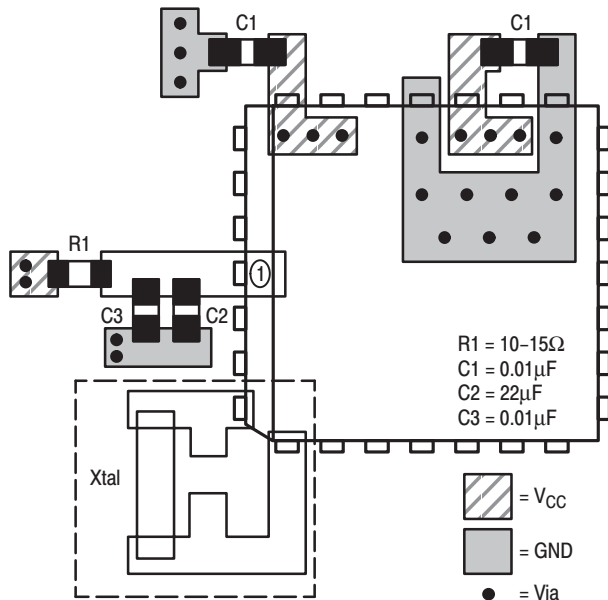


Figure 7. PCB Board Layout for MC12429 (28 PLCC)

Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator. Note the provisions for placing a resistor across the crystal oscillator terminals as discussed in the crystal oscillator section of this data sheet.

Although the MC12429 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Jitter Performance of the MC12429

The MC12429 exhibits long term and cycle-to-cycle jitter which rivals that of SAW based oscillators. This jitter perfor-

mance comes with the added flexibility one gets with a synthesizer over a fixed frequency oscillator.

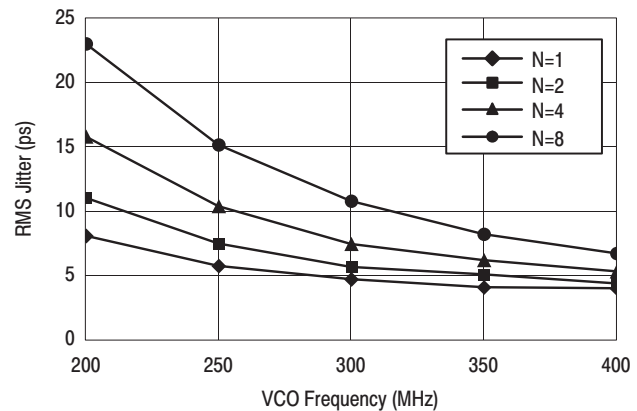


Figure 8. RMS PLL Jitter versus VCO Frequency

Figure 8 illustrates the RMS jitter performance of the MC12429 across its specified VCO frequency range. Note that the jitter is a function of both the output frequency as well as the VCO frequency, however the VCO frequency shows a much stronger dependence. The data presented has not been compensated for trigger jitter, this fact provides a measure of guardband to the reported data.

The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak-to-peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. All of the jitter data reported on the MC12429 was collected in this manner.

Figure 9 shows the jitter as a function of the output frequency. For the 12429 this information is probably of more importance. The flat line represents an RMS jitter value that corresponds to an 8 sigma ± 25 ps peak-to-peak long term period jitter. The graph shows that for output frequencies from 87.5 to 400MHz the jitter falls within the ± 25 ps peak-to-peak specification. The general trend is that as the output frequency is decreased the output edge jitter will increase.

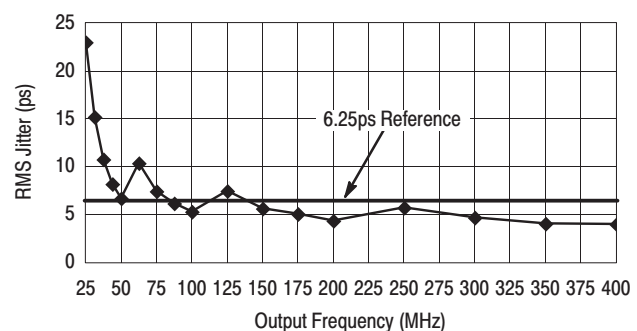


Figure 9. RMS Jitter versus Output Frequency

The jitter data presented should provide users with enough information to determine the effect on their overall timing budget. The jitter performance meets the needs of most system designs while adding the flexibility of frequency margining and field upgrades. These features are not available with a fixed frequency SAW oscillator.

High Frequency Clock Synthesizer

The MC12430 is a general purpose synthesized clock source. Its internal VCO will operate over a range of frequencies from 400 to 800 MHz. The differential PECL output can be configured to be the VCO frequency divided by 1, 2, 4 or 8. With the output configured to divide the VCO frequency by 2, and with a 16.000 MHz external quartz crystal used to provide the reference frequency, the output frequency can be specified in 1 MHz steps. The PLL loop filter is fully integrated so that no external components are required. The synthesizer output frequency is configured using a parallel or serial interface.

- 50 to 800 MHz Differential PECL Outputs
- ± 25 ps Peak-to-Peak Output Jitter
- Fully Integrated Phase-Locked Loop
- Minimal Frequency Over-Shoot
- Synthesized Architecture
- Serial 3-Wire Interface
- Parallel Interface for Power-Up
- Quartz Crystal Interface
- 28-Lead PLCC and 32-Lead LQFP Packages
- Operates from 3.3 V or 5.0V Power Supply

Functional Description

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by 16 before being sent to the phase detector. With a 16 MHz crystal, this provides a reference frequency of 1 MHz. Although this data sheet illustrates functionality only for a 16 MHz crystal, any crystal in the 10–20 MHz range can be used.

The VCO within the PLL operates over a range of 400 to 800 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is applied to the phase detector.

The phase detector and loop filter attempt to force the VCO output frequency to be $M \times 2$ times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve loop lock.

The output of the VCO is also passed through an output divider before being sent to the PECL output driver. This output divider (N divider) is configured through either the serial or the parallel interfaces and can provide one of four division ratios (1, 2, 4 or 8). This divider extends performance of the part while providing a 50% duty cycle.

The output driver is driven differentially from the output divider and is capable of driving a pair of transmission lines terminated in 50Ω to $V_{CC} - 2.0$ V. The positive reference for the output driver and the internal logic is separated from the power supply for the phase-locked loop to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the $M[8:0]$ and $N[1:0]$ inputs to configure the internal counters. Normally, on system reset, the $\overline{P\_LOAD}$ input is held LOW until sometime after power becomes valid. On the LOW-to-HIGH transition of $\overline{P\_LOAD}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the $M[8:0]$ and $N[1:0]$ inputs to reduce component count in the application of the chip.

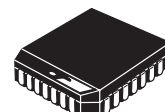
The serial interface centers on a fourteen bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See the programming section for more information.

The TEST output reflects various internal node values, and is controlled by the $T[2:0]$ bits in the serial data stream. See the programming section for more information.

MC12430

See Upgrade Product – MPC9230

**HIGH FREQUENCY PLL
CLOCK SYNTHESIZER**

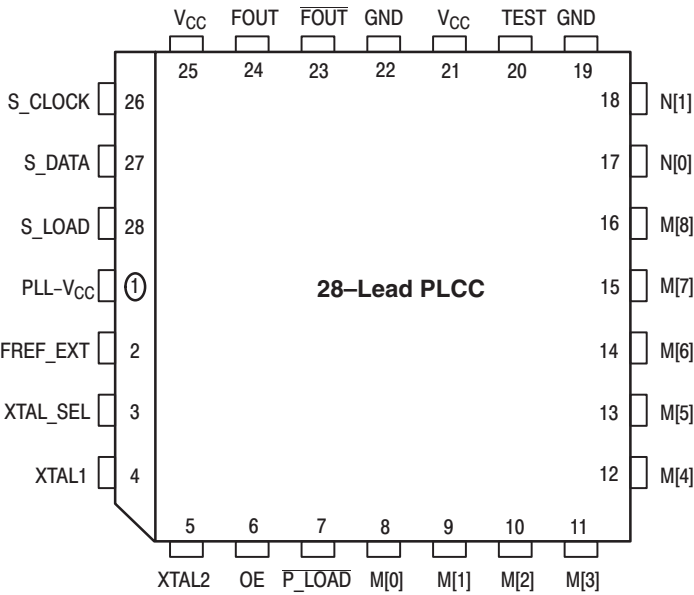


FN SUFFIX
28-LEAD PLCC PACKAGE
CASE 776



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A

4



N[1:0]	Output Division
0 0	2
0 1	4
1 0	8
1 1	1

Input	0	1
XTAL_SEL OE	FREF_EXT Disabled	XTAL Enabled

Figure 1. 28-Lead Pinout (Top View)

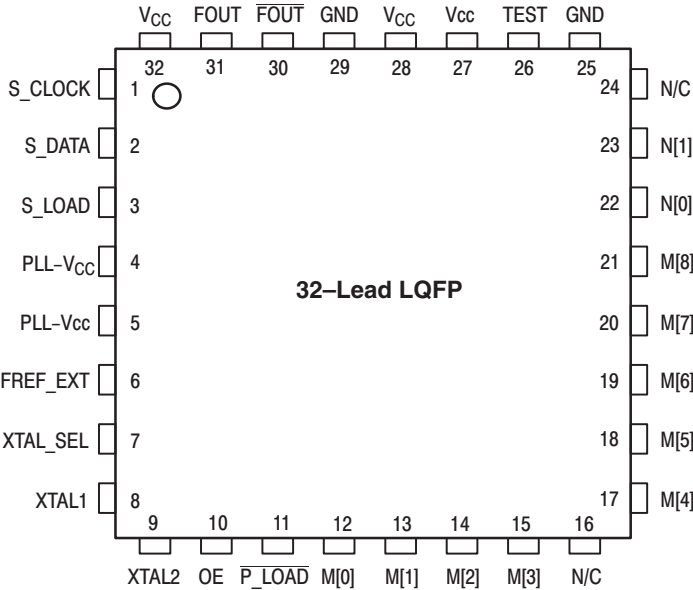


Figure 2. 32-Lead Pinout (Top View)

PIN DESCRIPTIONS

Pin Name	Function
Inputs	
XTAL1, XTAL2	These pins form an oscillator when connected to an external series–resonant crystal.
S_LOAD (Int. Pulldown)	This pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH, thus the data must be stable on the HIGH–to–LOW transition of S_LOAD for proper operation.
S_DATA (Int. Pulldown)	This pin acts as the data input to the serial configuration shift registers.
S_CLOCK (Int. Pulldown)	This pin serves to clock the serial configuration shift registers. Data from S_DATA is sampled on the rising edge.
P_LOAD (Int. Pullup)	This pin loads the configuration latches with the contents of the parallel inputs. The latches will be transparent when this signal is LOW, thus the parallel data must be stable on the LOW–to–HIGH transition of P_LOAD for proper operation. P_LOAD is state sensitive.
M[8:0] (Int. Pullup)	These pins are used to configure the PLL loop divider. They are sampled on the LOW–to–HIGH transition of P_LOAD. M[8] is the MSB, M[0] is the LSB.
N[1:0] (Int. Pullup)	These pins are used to configure the output divider modulus. They are sampled on the LOW–to–HIGH transition of P_LOAD.
OE (Int. Pullup)	Active HIGH Output Enable. The Enable is synchronous to eliminate possibility of runt pulse generation on the F _{OUT} output.
Outputs	
F _{OUT} , $\overline{F_{OUT}}$	These differential positive–referenced ECL signals (PECL) are the output of the synthesizer.
TEST	The function of this output is determined by the serial configuration bits T[2:0]. The output is single–ended ECL.
Power	
V _{CC}	This is the positive supply for the internal logic and the output buffer of the chip, and is connected to +3.3V or 5.0V (V _{CC} = PLL_V _{CC}). Current drain through V _{CC} ≈ 85 mA.
PLL_V _{CC}	This is the positive supply for the PLL, and should be as noise–free as possible for low–jitter operation. This supply is connected to +3.3V or 5.0V (V _{CC} = PLL_V _{CC}). Current drain through PLL_V _{CC} ≈ 15 mA.
GND	These pins are the negative supply for the chip and are normally all connected to ground.
Other	
FREF_EXT (Int. Pulldown)	LVC MOS/CMOS input which can be used as the PLL reference.
XTAL_SEL (Int. Pullup)	LVC MOS/CMOS input that selects between the crystal and the FREF_EXT source for the PLL reference signal. A HIGH selects the crystal input.

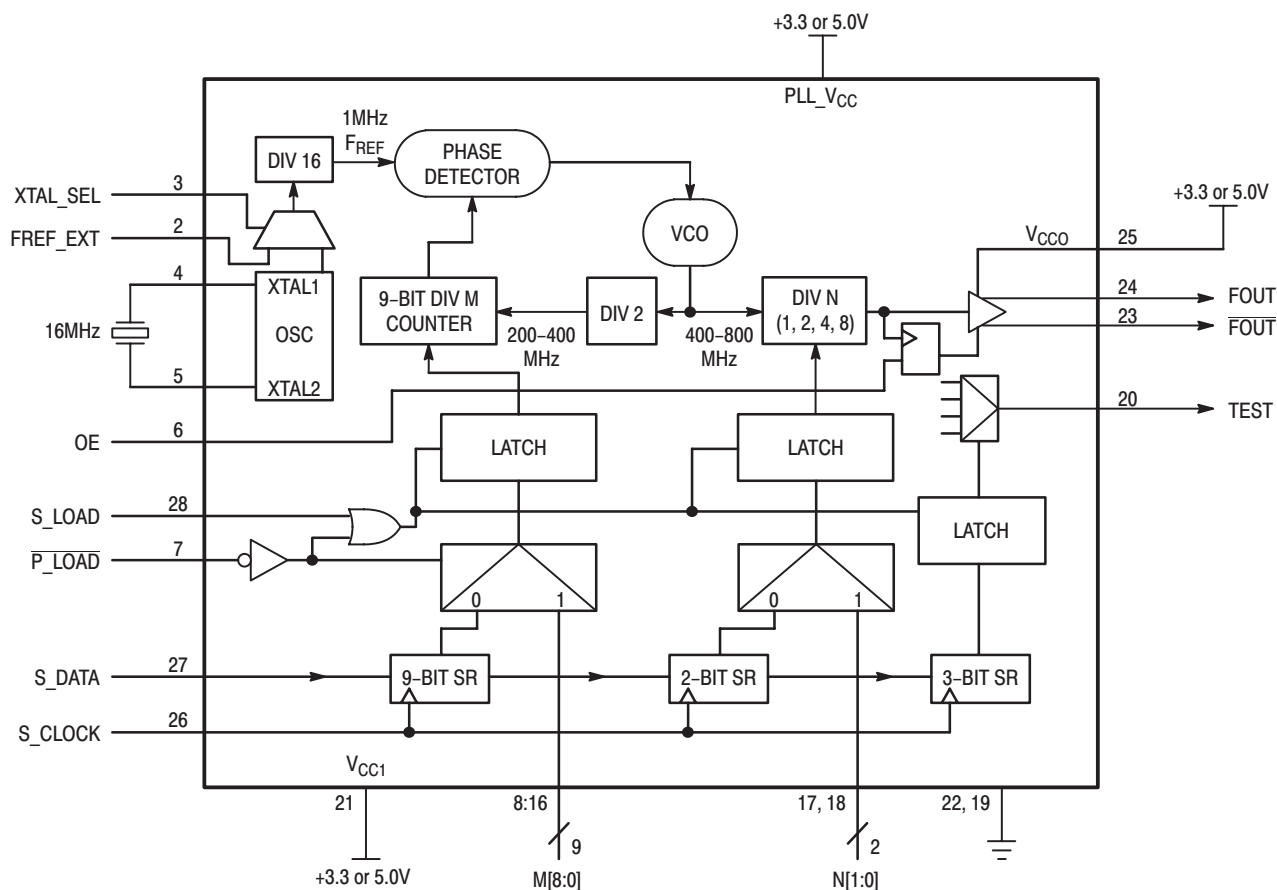


Figure 3. MC12430 Block Diagram (28-Lead PLCC Pinout)

PROGRAMMING INTERFACE

Programming the device amounts to properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can be represented by this formula:

$$F_{OUT} = (F_{XTAL} \div 16) \times M \times 2 \div N \quad (1)$$

Where F_{XTAL} is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be $200 \leq M \leq 400$ for any input reference.

Assuming that a 16 MHz reference frequency is used, the above equation reduces to:

$$F_{OUT} = 2 \times M \div N$$

Substituting the four values for N (1, 2, 4, 8) yields:

Output Frequency Range

N	FOUT	OUTPUT FREQUENCY RANGE
1	$2 \times M$	400 – 800 MHZ
2	M	200 – 400 MHZ
4	$M \div 2$	100 – 200 MHZ
8	$M \div 4$	50 – 100 MHZ

From these ranges, the user will establish the value of N required, then the value of M can be calculated based on the appropriate equation above. For example, if an output frequency of 131 MHz was desired, the following steps would be taken to identify the appropriate M and N values. 131MHz falls within the frequency range set by an N value of 4 so $N[1:0] = 01$. For $N = 4$, $F_{OUT} = M \div 2$ and $M = 2 \times F_{OUT}$. Therefore, $M = 131 \times 2 = 262$, so $M[8:0] = 100000110$. Following this same procedure, a user can generate any whole frequency desired between 50 and 800MHz. Note that for $N > 2$ fractional values of F_{OUT} can be realized. The size of the programmable frequency steps (and thus the indicator of the fractional output frequencies achievable) will be equal to $F_{XTAL} \div 8 \div N$.

For input reference frequencies other than 16 MHz, the set of appropriate equations can be deduced from equation 1. For computer applications, another useful frequency base would be 16.666 MHz. From this reference, one can generate a family of output frequencies at multiples of the 33.333 MHz PCI clock. As an example, to generate a 133.333 MHz clock from a 16.666 MHz reference, the following M and N values would be used:

$$F_{OUT} = 16.666 \div 16 \times M \times 2 \div N = 1.04166 \times M \times 2 \div N$$

$$\text{Let } N = 4, \quad M = 133.3333 \div 1.04166 \times 2 = 256$$

The value for M falls within the constraints set for PLL stability, therefore, $N[1:0] = 01$ and $M[8:0] = 10000000$. If the value for M fell outside of the valid range, a different N value would be selected to try to move M in the appropriate direction.

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the $\overline{P\_LOAD}$ signal such that a LOW to HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the $\overline{P\_LOAD}$ signal is LOW, the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port, the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14 bit shift register. Note that the $\overline{P\_LOAD}$ signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register, the most significant bit is loaded first (T2, N1 and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 4 illustrates the timing diagram for both a parallel and a serial load of the MC12430 synthesizer.

M[8:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. The T2, T1 and T0 control bits are preset to '000' when $\overline{P\_LOAD}$ is LOW so that the PECL FOUT outputs are as jitter-free as possible. Any active signal on the TEST output

pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MC12430 itself. However, the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MC12430 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clock tree. Figure 5 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level, the input frequency is limited to 250 MHz or less. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 250MHz as the minimum divide ratio of the N counter is 1. Note that the M counter output on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.

4

T2	T1	T0	TEST (Pin 20)
0	0	0	SHIFT REGISTER OUT
0	0	1	HIGH
0	1	0	FREF
0	1	1	M COUNTER OUT/2
1	0	0	FOUT
1	0	1	LOW
1	1	0	M COUNTER/2 in PLL Bypass Mode
1	1	1	FOUT/4

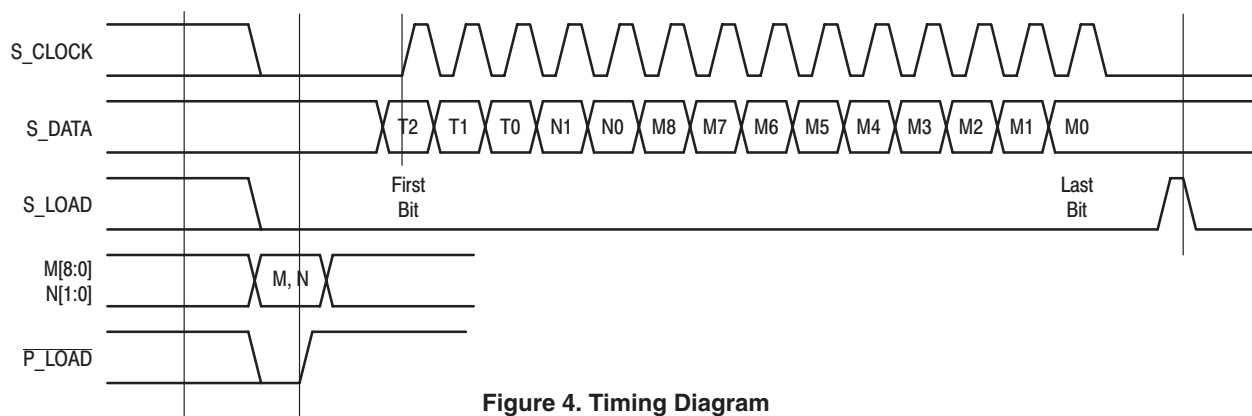
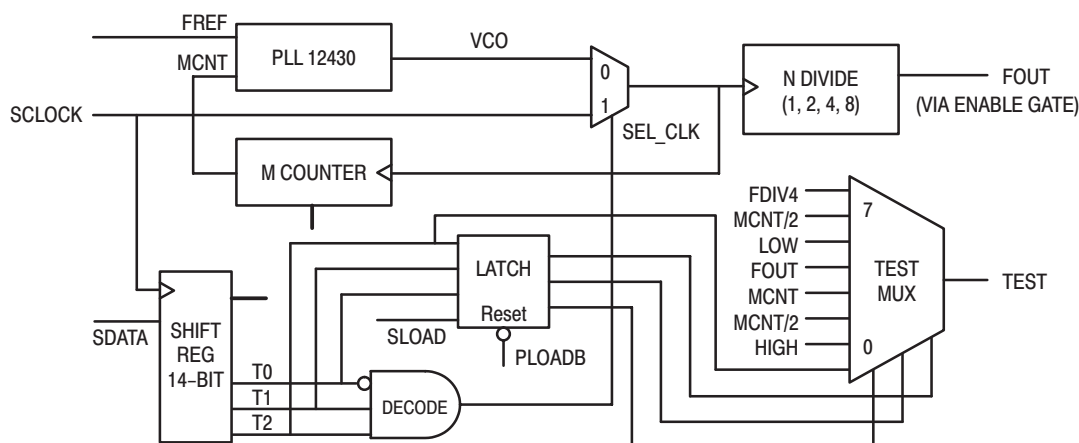


Figure 4. Timing Diagram



- T2=T1=1, T0=0: Test Mode (PLL Bypass)
 - SCLOCK is selected, MCNT/2 is on TEST output, SCLOCK DIVIDE BY N is on FOUT pin
- PLOADB acts as reset for test pin latch. When latch reset T2 data is shifted out TEST pin.

Figure 5. Serial Test Clock Block Diagram

4

DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$)

Symbol	Characteristic	0°C			25°C			70°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.2			2.2			2.2			V	
V_{IL}	Input LOW Voltage			0.8			0.8			0.8	V	
I_{IN}	Input Current			1.0			1.0			1.0	mA	
V_{OH}	Output HIGH Voltage TEST	2.5			2.5			2.5			V	$I_{OH} = -0.8mA$
V_{OL}	Output LOW Voltage TEST			0.4			0.4			0.4	V	$I_{OL} = 0.8mA$
V_{OH}	Output HIGH Voltage ¹ : FOUT, FOUT	2.28		2.60	2.32		2.49	2.38		2.565	V	$V_{CC0} = 3.3V^{2,3}$
V_{OL}	Output LOW Voltage ¹ : FOUT, FOUT	1.35		1.67	1.35		1.67	1.35		1.70	V	$V_{CC0} = 3.3V^{2,3}$
I_{CC}	Power Supply Current V_{CC} PLL_ V_{CC}		90 15	110 20		90 15	110 20		90 15	110 20	mA	

1. See applications information section for output level versus frequency information.

2. Output levels will vary 1:1 with V_{CC0} variation.3. 50 Ω to $V_{CC} - 2.0V$ termination.DC CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$)

Symbol	Characteristic	0°C			25°C			70°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{IH}	Input HIGH Voltage	3.5			3.5			3.5			V	
V_{IL}	Input LOW Voltage			0.8			0.8			0.8	V	
I_{IN}	Input Current			1.0			1.0			1.0	mA	
V_{OH}	Output HIGH Voltage TEST	2.5			2.5			2.5			V	$I_{OH} = -0.8mA$
V_{OL}	Output LOW Voltage TEST			0.4			0.4			0.4	V	$I_{OL} = 0.8mA$
V_{OH}	Output HIGH Voltage ¹ : FOUT, FOUT	3.98		4.30	4.02		4.19	4.08		4.265	V	$V_{CC0} = 5.0V^{2,3}$
V_{OL}	Output LOW Voltage ¹ : FOUT, FOUT	3.05		3.37	3.05		3.37	3.05		3.40	V	$V_{CC0} = 5.0V^{2,3}$
I_{CC}	Power Supply Current V_{CC} PLL_ V_{CC}		90 15	110 20		90 15	110 20		90 15	110 20	mA	

1. See applications information section for output level versus frequency information.

2. Output levels will vary 1:1 with V_{CC0} variation.3. 50 Ω to $V_{CC} - 2.0V$ termination.

AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V}$ to $5.0\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Max	Unit	Condition
F_{MAXI}	Maximum Input Frequency S_CLOCK Xtal Oscillator FREF_EXT	10 10	10 20 Note 2.	MHz	Note 1.
F_{MAXO}	Maximum Output Frequency VCO (Internal) FOUT	400 50	800 800	MHz	Note 4.
t_{LOCK}	Maximum PLL Lock Time		10	ms	
t_{jitter}	Period Deviation (Peak-to-Peak) Note 3.		± 25 ± 65	ps	N = 2, 4, 8; Note 4. N = 1; Note 4.
t_s	Setup Time S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to P_LOAD	20 20 20		ns	
t_h	Hold Time S_DATA to S_CLOCK M, N to P_LOAD	20 20		ns	
tpw_{MIN}	Minimum Pulse Width S_LOAD P_LOAD	50 50		ns	
t_r, t_f	Output Rise/Fall FOUT	300	800	ps	20%–80%; Note 4.

1. 10MHz is the maximum frequency to load the feedback divide registers. S_CLOCK can be switched at higher frequencies when used as a test clock in TEST_MODE 6.
2. Maximum frequency on FREF_EXT is a function of the internal M counter limitations. The phase detector can handle up to 100MHz on the input, but the M counter must remain in the valid range of $200 \leq M \leq 400$. See the Programming Interface section on page 382 of this data sheet for more details.
3. See Applications Information below for additional information.
4. 50Ω to $V_{CC} - 2.0\text{V}$ pull-down.

APPLICATIONS INFORMATION**Using the On-Board Crystal Oscillator**

The MC12430 features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MC12430 as possible to avoid any board level parasitics. To facilitate co-location surface mount crystals are recommended, but not required.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately, most crystals are characterized in a parallel resonant mode. Fortunately, there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result, a parallel resonant crystal can be used with the MC12430 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit

will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application, this level of inaccuracy is immaterial. Table 1 below specifies the performance requirements of the crystals to be used with the MC12430.

Table 1. Recommended Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	$\pm 75\text{ppm}$ at 25°C
Frequency/Temperature Stability	$\pm 150\text{ppm}$ 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7 pF
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100 μW
Aging	5 ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

Power Supply Filtering

The MC12430 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MC12430 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (PLL_VCC) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the PLL_VCC pin for the MC12430.

Figure 6 illustrates a typical power supply filter scheme. The MC12430 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the PLL_VCC pin of the MC12430. From the data sheet, the I_{PLL_VCC} current (the current sourced through the PLL_VCC pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0 V must be maintained on the PLL_VCC pin, very little DC voltage drop can be tolerated when a 3.3 V V_{CC} supply is used. The resistor shown in Figure 6 must have a resistance of 10–15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

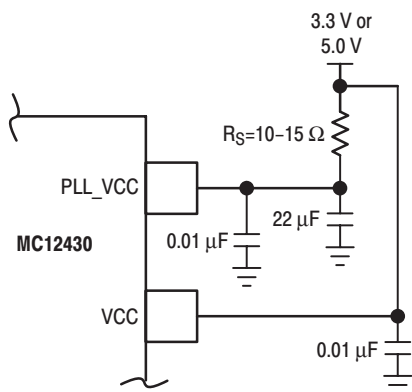


Figure 6. Power Supply Filter

A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000 μ H choke will show a significant impedance at 10 KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the PLL_VCC pin, a low DC resistance inductor is required (less than 15 Ω). Generally, the resistor/ca-

pacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering.

The MC12430 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 7 shows a representative board layout for the MC12430. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 7 is the low impedance connections between VCC and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the 12430 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

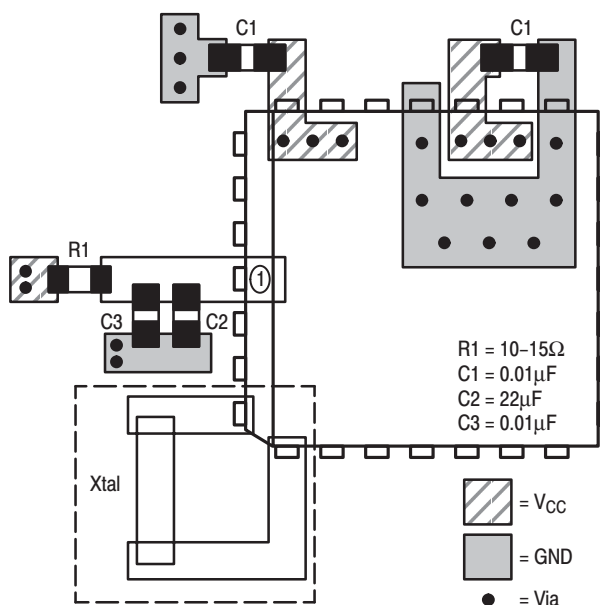


Figure 7. PCB Board Layout for MC12430 (28 PLCC)

Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator.

Although the MC12430 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Jitter Performance of the MC12430

The MC12430 exhibits long term and cycle-to-cycle jitter which rivals that of SAW based oscillators. This jitter performance comes with the added flexibility one gets with a synthesizer over a fixed frequency oscillator.

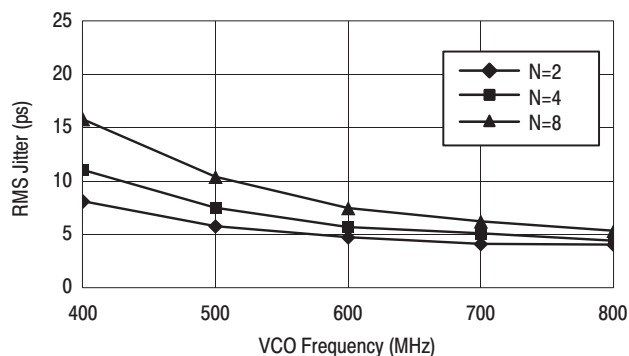


Figure 8. RMS PLL Jitter versus VCO Frequency

Figure 8 illustrates the RMS jitter performance of the MC12430 across its specified VCO frequency range. Note that the jitter is a function of both the output frequency as well as the VCO frequency, however the VCO frequency shows a much stronger dependence. The data presented has not been compensated for trigger jitter, this fact provides a measure of guardband to the reported data.

The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak-to-peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. The oscilloscope cannot collect adjacent pulses, rather it collects pulses from a very large sample of pulses.

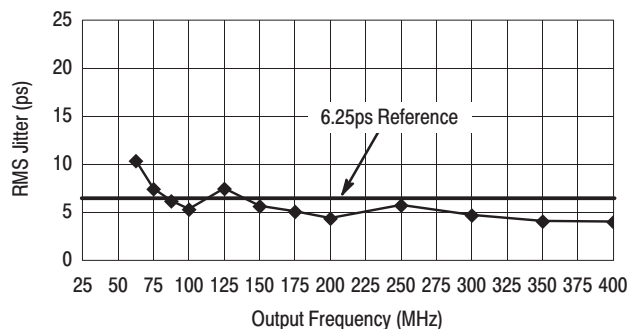


Figure 9. RMS Jitter versus Output Frequency

Figure 9 shows the jitter as a function of the output frequency. For the 12430, this information is probably of more importance. The flat line represents an RMS jitter value that corresponds to an 8 sigma ± 25 ps peak-to-peak long term period jitter. The graph shows that for output frequencies from 87.5 to

400 MHz the jitter falls within the ± 25 ps peak-to-peak specification. The general trend is that as the output frequency is decreased the output edge jitter will increase.

The jitter data from Figure 8 and Figure 9 do not include the performance of the 12430 when the output is in the divide by 1 mode. In divide by one mode, the MC12430 output jitter distribution is bimodal. Since a bimodal distribution cannot be accurately represented with an rms value, peak-to-peak values of jitter for the divide by one mode are presented.

Figure 10 shows the peak-to-peak jitter of the 12430 output in divide by one mode as a function of output frequency. Notice that as with the other modes the jitter improves with increasing frequency. The ± 65 ps shown in the data sheet table represents a conservative value of jitter, especially for the higher VCO, and thus output frequencies.

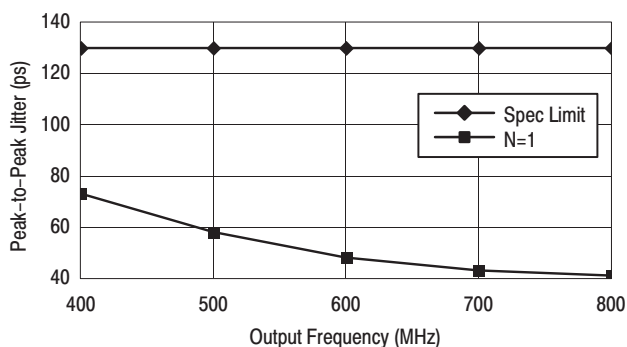


Figure 10. Peak-to-Peak Jitter versus Output Frequency

The jitter data presented should provide users with enough information to determine the effect on their overall timing budget. The jitter performance meets the needs of most system designs while adding the flexibility of frequency margining and field upgrades. These features are not available with a fixed frequency SAW oscillator.

Output Voltage Swing vs Frequency

In the divide by one mode, the output rise and fall times will limit the peak to peak output voltage swing. For a 400 MHz output, the peak to peak swing of the 12430 output will be approximately 700 mV. This swing will gradually degrade as the output frequency increases, at 800 MHz the output swing will be reduced to approximately 500 mV. For a worst case analysis, it would be safe to assume that the 12430 output will always generate at least a 500mV output swing. Note that most high speed ECL receivers require only a few hundred millivolt input swings for reliable operation. As a result, the output generated by the 12430 will, under all conditions, be sufficient for clocking standard ECL devices. Note that if a larger swing is required the MC12430 could drive a clock fanout buffer like the MC100EP111.

High Frequency Clock Synthesizer

The MC12439 is a general purpose synthesized clock source. Its internal VCO will operate over a range of frequencies from 400 to 800 MHz. The differential PECL output can be configured to be the VCO frequency divided by 1, 2, 4, or 8. With the output configured to divide the VCO frequency by 1, and with a 16.66 MHz external quartz crystal used to provide the reference frequency, the output frequency can be specified in 16.66MHz steps. The output frequency is configured using a parallel or serial interface.

- 50 to 800 MHz Differential PECL Outputs
- ± 25 ps Typical Peak-to-Peak Output Jitter
- Minimal Frequency Over-Shoot
- Synthesized Architecture
- Serial 3-Wire Interface
- Parallel Interface for Power-Up
- Quartz Crystal Interface
- 28-Lead PLCC Package
- Operates from 3.3 V or 5.0V Power Supply

Functional Description

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by 2 before being sent to the phase detector. With a 16.66 MHz crystal, this provides a reference frequency of 8.33 MHz. Although this data sheet illustrates functionality only for a 16 MHz and 16.66MHz crystal, any crystal in the 10–20 MHz range can be used. In addition to the crystal, an LVCMOS input can also be used as the PLL reference. The reference is selected via the XTAL_SEL input pin.

The VCO within the PLL operates over a range of 400 to 800 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is also applied to the phase detector.

The phase detector and loop filter attempt to force the VCO output frequency to be $2 \times M$ times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve loop lock.

The output of the VCO is also passed through an output divider before being sent to the PECL output driver. This output divider is configured through either the serial or the parallel interfaces and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle.

The output driver is driven differentially from the output divider and is capable of driving a pair of transmission lines terminated in 50Ω to $V_{CC} - 2.0$ V.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the $M[6:0]$ and $N[1:0]$ inputs to configure the internal counters. Normally, on system reset, the $\overline{P\_LOAD}$ input is held LOW until sometime after power becomes valid. On the LOW-to-HIGH transition of $\overline{P\_LOAD}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the $M[6:0]$ and $N[1:0]$ inputs to reduce component count in the application of the chip.

The serial interface centers on a twelve bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See the programming section for more information.

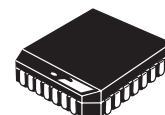
The TEST output reflects various internal node values and is controlled by the $T[2:0]$ bits in the serial data stream. See the programming section for more information.

The PWR_DOWN pin, when asserted, will synchronously divide the FOUT by 16. The power down sequence is clocked by the PLL reference clock, thereby causing the frequency reduction to happen relatively slowly. Upon de-assertion of the PWR_DOWN pin, the FOUT input will step back up to its programmed frequency in four discrete increments.

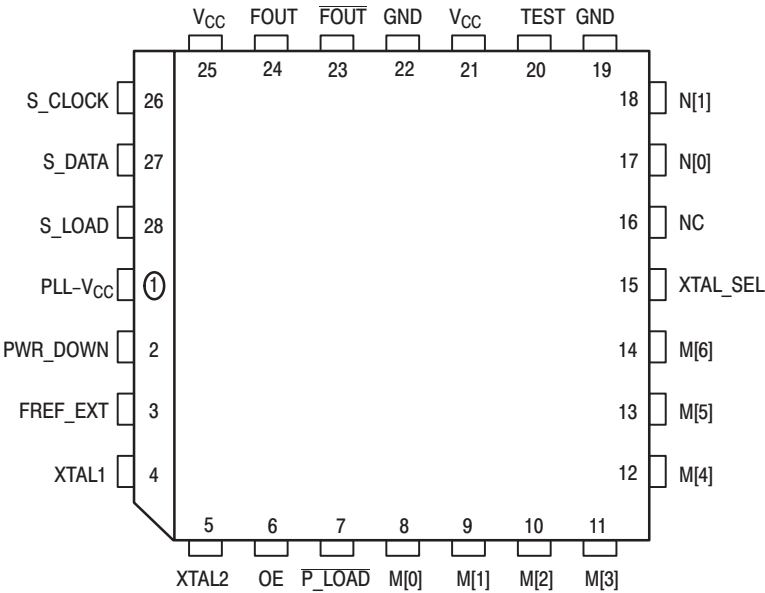
MC12439

See Upgrade Product – MPC9239

**HIGH FREQUENCY PLL
CLOCK SYNTHESIZER**



FN SUFFIX
28-LEAD PLCC PACKAGE
CASE 776



N[1:0]	Output Division
0 0	2
0 1	4
1 0	8
1 1	1

Input	0	1
PWR_DOWN	FOUT	FOUT/16
XTAL_SEL	FREF_EXT	XTAL
OE	Disabled	Enabled

28-Lead Pinout (Top View)

PIN DESCRIPTIONS

Pin Name	Type	Function
Inputs		
XTAL1, XTAL2	—	These pins form an oscillator when connected to an external series–resonant crystal.
S_LOAD	Int. Pulldown	This pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH, thus the data must be stable on the HIGH–to–LOW transition of S_LOAD for proper operation.
S_DATA	Int. Pulldown	This pin acts as the data input to the serial configuration shift registers.
S_CLOCK	Int. Pulldown	This pin serves to clock the serial configuration shift registers. Data from S_DATA is sampled on the rising edge.
P_LOAD	Int. Pullup	This pin loads the configuration latches with the contents of the parallel inputs. The latches will be transparent when this signal is LOW, thus the parallel data must be stable on the LOW–to–HIGH transition of P_LOAD for proper operation.
M[6:0]	Int. Pullup	These pins are used to configure the PLL loop divider. They are sampled on the LOW–to–HIGH transition of P_LOAD. M[6] is the MSB, M[0] is the LSB.
N[1:0]	Int. Pullup	These pins are used to configure the output divider modulus. They are sampled on the LOW–to–HIGH transition of P_LOAD. P_LOAD is state sensitive.
OE	Int. Pullup	Active HIGH Output Enable.
Outputs		
F _{OUT} , $\overline{F_{OUT}}$	—	These differential positive–referenced ECL signals (PECL) are the output of the synthesizer.
TEST	—	The function of this output is determined by the serial configuration bits T[2:0].
Power		
V _{CC}	—	This is the positive supply for the chip, and is connected to +3.3 V or 5.0 V (V _{CC} = PLL_V _{CC}).
PLL_V _{CC}	—	This is the positive supply for the PLL and should be as noise–free as possible for low–jitter operation. This supply is connected to +3.3 V or 5.0 V (V _{CC} = PLL_V _{CC}).
GND	—	These pins are the negative supply for the chip and are normally all connected to ground.
Other		
PWR_DOWN	Int. Pulldown	LVC MOS input that forces the FOUT output to synchronously reduce its frequency by a factor of 16.
FREF_EXT	Int. Pulldown	LVC MOS input which can be used as the PLL reference frequency.
XTAL_SEL	Int. Pullup	LVC MOS input that selects between the XTAL and FREF_EXT PLL reference inputs. A HIGH selects the XTAL input.

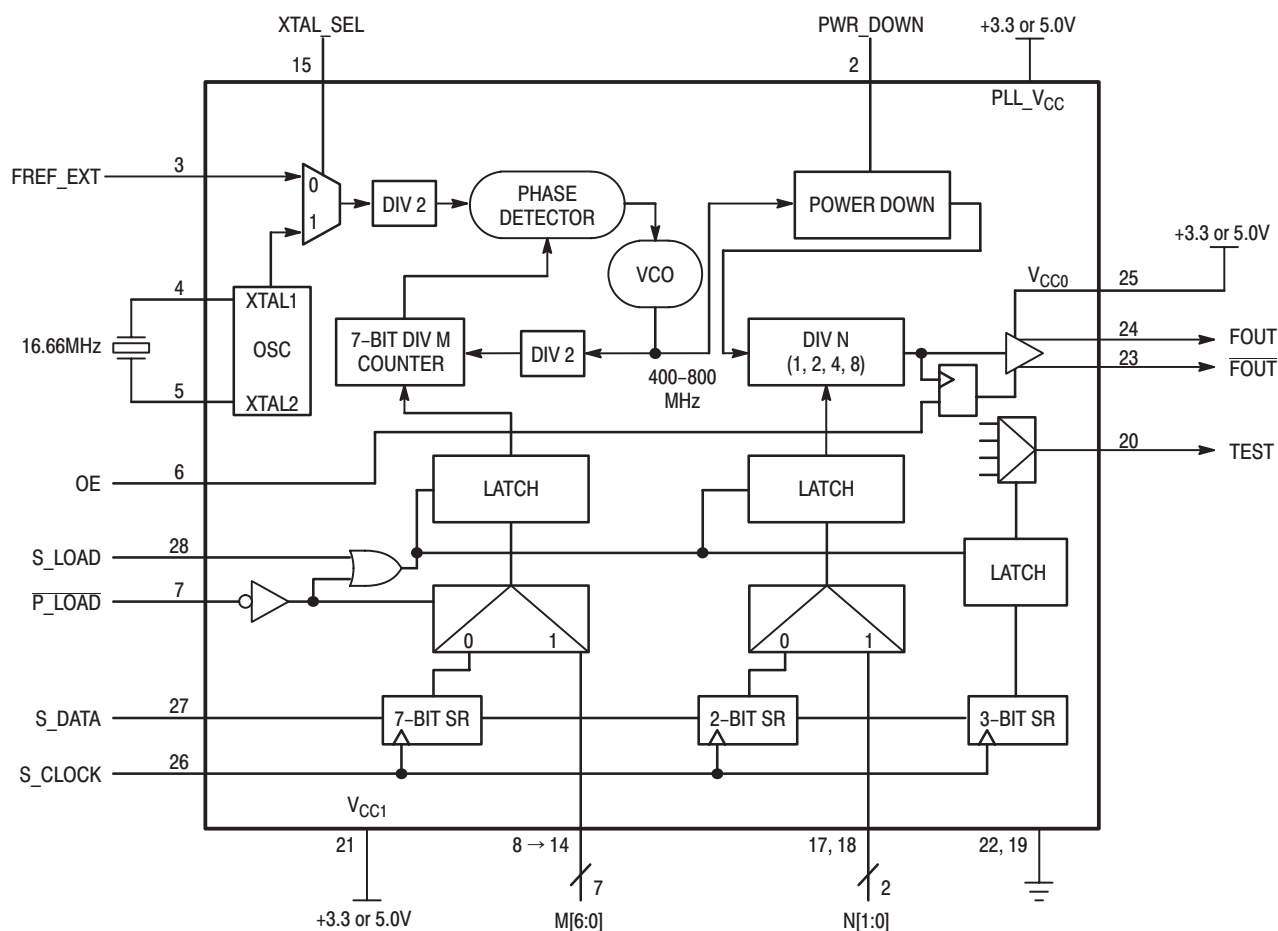


Figure 1. MC12439 Block Diagram

PROGRAMMING INTERFACE

Programming the device amounts to properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can be represented by this formula:

$$F_{OUT} = F_{XTAL} \times M \div N \quad (1)$$

Where F_{XTAL} is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be $25 \leq M \leq 50$ for a 16MHz input reference.

For input references other than 16MHz, the valid M values can be calculated from the valid VCO range of 400–800MHz.

Assuming that a 16MHz reference frequency is used, the above equation reduces to:

$$F_{OUT} = 16 \times M \div N$$

Substituting the four values for N (1, 2, 4, 8) yields:

Output Frequency Range

N	F _{OUT}	OUTPUT FREQUENCY RANGE
1	16 x M	400 – 800 MHz
2	8 x M	200 – 400 MHz
4	4 x M	100 – 200 MHz
8	2 x M	50 – 100 MHz

From these ranges, the user will establish the value of N required, then the value of M can be calculated based on the

appropriate equation above. For example, if an output frequency of 384MHz was desired, the following steps would be taken to identify the appropriate M and N values. 384 MHz falls within the frequency range set by an N value of 2, so $N[1:0] = 00$. For $N = 2$, $F_{OUT} = 8M$ and $M = F_{OUT} \div 8$. Therefore, $M = 384 \div 8 = 48$, so $M[8:0] = 0110000$.

For input reference frequencies other than 16MHz, the set of appropriate equations can be deduced from equation 1. For computer applications, another useful frequency base would be 16.666MHz. From this reference, one can generate a family of output frequencies at multiples of the 33.333 MHz PCI clock. As an example, to generate a 533.333MHz clock from a 16.666MHz reference, the following M and N values would be used:

$$F_{OUT} = 16.666 \times M \div N$$

$$\text{Let } N = 1, M = 533.333 \div 16.666 = 32$$

The value for M falls within the constraints set for PLL stability ($400 \div 16.666 \leq M \leq 800 \div 16.666$; $24 \leq M \leq 48$), therefore $N[1:0] = 11$ and $M[6:0] = 0100000$. If the value for M fell outside of the valid range, a different N value would be selected to try to move M in the appropriate direction.

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the $\overline{P\_LOAD}$ signal such that a LOW to HIGH transition will latch the information present on the $M[6:0]$ and $N[1:0]$ inputs into the M and N counters. When the $\overline{P\_LOAD}$ signal is LOW, the input latches will be transparent and any changes on the $M[6:0]$ and

N[1:0] inputs will affect the FOUT output pair. To use the serial port, the S_CLOCK signal samples the information on the S_DATA line and loads it into a 12 bit shift register. Note that the P_LOAD signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register, the most significant bit is loaded first (T2, N1 and M6). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 2 illustrates the timing diagram for both a parallel and a serial load of the MC12439 synthesizer.

M[6:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents FOUT, the CMOS output may not be able to toggle fast enough for some of the higher output frequencies. The T2, T1 and T0 control bits are preset to '000' when P_LOAD is LOW so that the PECL FOUT outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental effects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST

output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MC12439 itself. However the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110, the MC12439 is placed in PLL bypass mode. In this mode, the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode, the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clock tree. Figure 3 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level, the input frequency is limited to 250 MHz or less. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 250 MHz as the minimum divide ratio of the N counter is 1. Note that the M counter output on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.

T2	T1	T0	TEST (Pin 20)
0	0	0	SHIFT REGISTER OUT
0	0	1	HIGH
0	1	0	FREF
0	1	1	M COUNTER OUT/2
1	0	0	FOUT
1	0	1	LOW
1	1	0	M COUNTER/2 in PLL Bypass Mode
1	1	1	FOUT/4

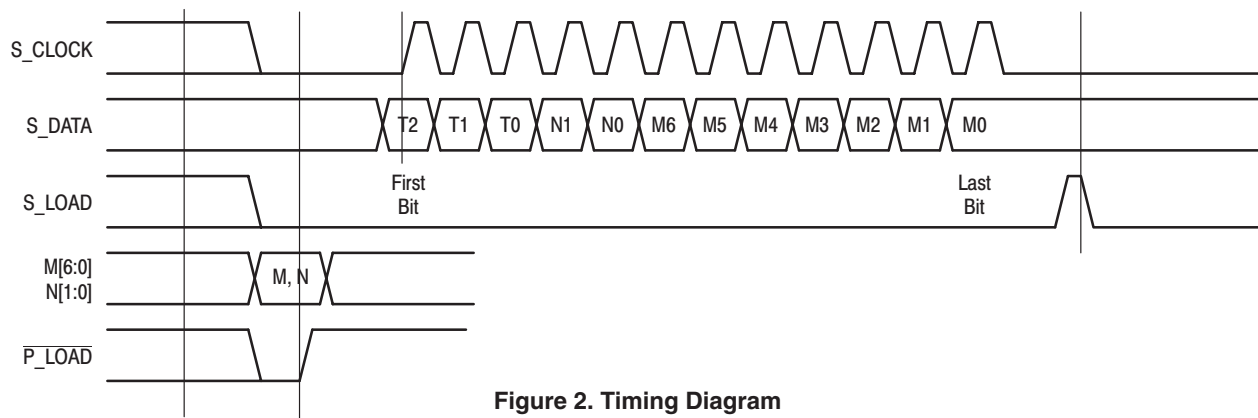


Figure 2. Timing Diagram

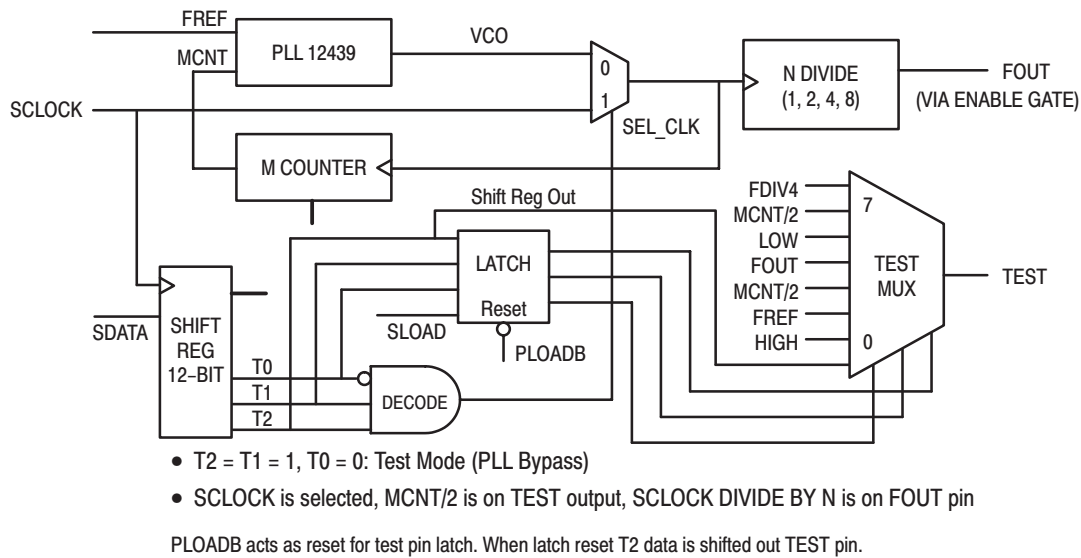


Figure 3. Serial Test Clock Block Diagram

DC CHARACTERISTICS ($V_{CC} = 3.3\text{ V} \pm 5\%$)

Symbol	Characteristic	0°C			25°C			70°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.0			2.0			2.0			V	
V_{IL}	Input LOW Voltage			0.8			0.8			0.8	V	
I_{IN}	Input Current			1.0			1.0			1.0	mA	
I_{OH}	Output HIGH Current ¹ : F_{OUT} , $\overline{F_{OUT}}$			50			50			50	mA	Continuous
V_{OH}	Output HIGH Voltage TEST	2.5			2.5			2.5			V	$I_{OH} = -0.8\text{mA}$
V_{OL}	Output LOW Voltage TEST			0.4			0.4			0.4	V	$I_{OL} = 0.8\text{mA}$
V_{OH}	Output HIGH Voltage ² : F_{OUT} , $\overline{F_{OUT}}$	2.28		2.60	2.32		2.49	2.38		2.565	V	$V_{CC0} = 3.3\text{V}^{3,4}$
V_{OL}	Output LOW Voltage ² : F_{OUT} , $\overline{F_{OUT}}$	1.35		1.67	1.35		1.67	1.35		1.70	V	$V_{CC0} = 3.3\text{V}^{3,4}$
I_{CC}	Power Supply Current V_{CC} PLL_ V_{CC}		90 15	110 20		90 15	110 20		90 15	110 20	mA	

1. Maximum I_{OH} spec implies the device can drive 25Ω impedance with the PECL outputs.
2. See Applications Information section for output level versus frequency information.
3. Output levels will vary 1:1 with V_{CC} variation.
4. 50Ω to $V_{CC} - 2.0\text{V}$ termination.

4

DC CHARACTERISTICS ($V_{CC} = 5.0\text{ V} \pm 5\%$)

Symbol	Characteristic	0°C			25°C			70°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{IH}	Input HIGH Voltage	3.5			3.5			3.5			V	
V_{IL}	Input LOW Voltage			0.8			0.8			0.8	V	
I_{IN}	Input Current			1.0			1.0			1.0	mA	
I_{OH}	Output HIGH Current ¹ : F_{OUT} , $\overline{F_{OUT}}$			50			50			50	mA	Continuous
V_{OH}	Output HIGH Voltage TEST	3.8			3.8			3.8			V	$I_{OH} = -0.8\text{ mA}$
V_{OL}	Output LOW Voltage TEST			0.4			0.4			0.4	V	$I_{OL} = 0.8\text{ mA}$
V_{OH}	Output HIGH Voltage ² : F_{OUT} , $\overline{F_{OUT}}$	3.98		4.30	4.02		4.19	4.08		4.265	V	$V_{CC0} = 5.0\text{ V}^{3,4}$
V_{OL}	Output LOW Voltage ² : F_{OUT} , $\overline{F_{OUT}}$	3.05		3.37	3.05		3.37	3.05		3.40	V	$V_{CC0} = 5.0\text{ V}^{3,4}$
I_{CC}	Power Supply Current V_{CC} PLL_ V_{CC}		90 15	110 20		90 15	110 20		90 15	110 20	mA	

1. Maximum I_{OH} spec implies the device can drive 25Ω impedance with the PECL outputs.
2. See applications information section for output level versus frequency information.
3. Output levels will vary 1:1 with V_{CC0} variation.
4. 50Ω to $V_{CC} - 2.0\text{V}$ termination.

AC CHARACTERISTICS ($T_A = 0$ to 70°C ; $V_{CC} = 3.3$ to $5.0\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Max	Unit	Condition
F_{MAXI}	Maximum Input Frequency S_CLOCK Xtal Oscillator FREF_EXT	10 10	10 20 Note 1.	MHz	
F_{MAXO}	Maximum Output Frequency VCO (Internal) FOUT	400 50	900 800	MHz	Note 3.
t_{LOCK}	Maximum PLL Lock Time	1	10	ms	
t_{jitter}	Period Deviation (Peak-to-Peak) (Note 2.)		± 25 ± 65	ps	N = 2,4,8; Note 3. N = 1; Note 3.
t_s	Setup Time S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to P_LOAD	20 20 20		ns	
t_h	Hold Time S_DATA to S_CLOCK M, N to P_LOAD	20 20		ns	
tpw_{MIN}	Minimum Pulse Width S_LOAD P_LOAD	50 50		ns	Note 3.
t_r, t_f	Output Rise/Fall Time	300	800	ps	Note 3.

1. Maximum frequency on FREF_EXT is a function of the internal M counter limitations. The phase detector can handle up to 100 MHz on the input, but the M counter must remain in the valid range of $25 \leq M \leq 50$. See the programming section in this data sheet for more details.
2. See Applications Information section for additional information.
3. $50\ \Omega$ to $V_{CC} - 2.0\text{V}$ pulldown.

APPLICATIONS INFORMATION

Using the On-Board Crystal Oscillator

The MC12439 features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs, the user is advised to mount the crystal as close to the MC12439 as possible to avoid any board level parasitics. To facilitate co-location, surface mount crystals are recommended but not required.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately, most crystals are characterized in a parallel resonant mode. Fortunately, there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result, a parallel resonant crystal can be used with the MC12439 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application, this level of inaccuracy is immaterial. Table 1 below specifies the performance requirements of the crystals to be used with the MC12439.

Table 1. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	± 75 ppm at 25°C
Frequency/Temperature Stability	± 150 pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7 pF
Equivalent Series Resistance (ESR)	50 to 80 Ω
Correlation Drive Level	100 μ W
Aging	5 ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

Power Supply Filtering

The MC12439 is a mixed analog/digital product, and as such, it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MC12439 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (PLL_VCC) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The

simplest form of isolation is a power supply filter on the PLL_VCC pin for the MC12439.

Figure 4 illustrates a typical power supply filter scheme. The MC12439 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the PLL_VCC pin of the MC12439. From the data sheet, the I_{PLL_VCC} current (the current sourced through the PLL_VCC pin) is typically 15mA (20 mA maximum), assuming that a minimum of 3.0 V must be maintained on the PLL_VCC pin very little DC voltage drop can be tolerated when a 3.3 V V_{CC} supply is used. The resistor shown in Figure 4 must have a resistance of 10–15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

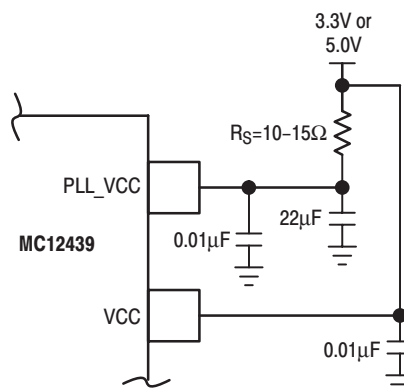


Figure 4. Power Supply Filter

A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000 μ H choke will show a significant impedance at 10 kHz frequencies and above. Because of the current draw and the voltage that must be maintained on the PLL_VCC pin, a low DC resistance inductor is required (less than 15 Ω). Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering.

The MC12439 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 5 shows a representative board layout for the MC12439. There exist many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 5 is the low impedance connections between V_{CC} and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the 12439 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the

leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

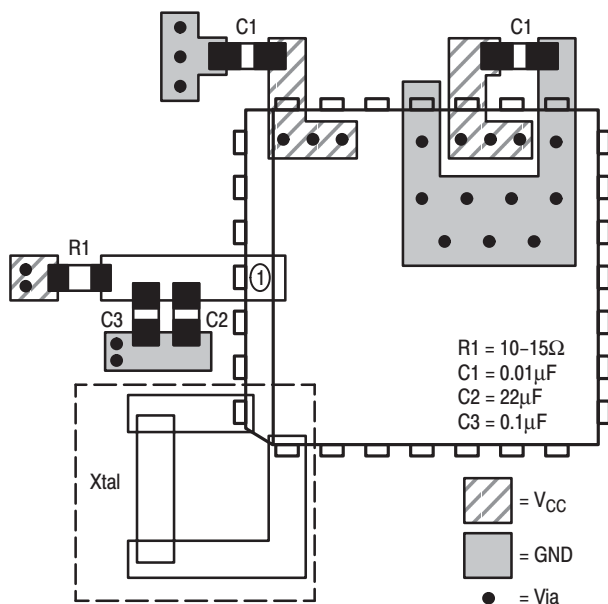


Figure 5. PCB Board Layout for MC12439

Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit, and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator.

Although the MC12439 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Jitter Performance of the MC12439

The MC12439 exhibits long term and cycle-to-cycle jitter which rivals that of SAW based oscillators. This jitter performance comes with the added flexibility one gets with a synthesizer over a fixed frequency oscillator.

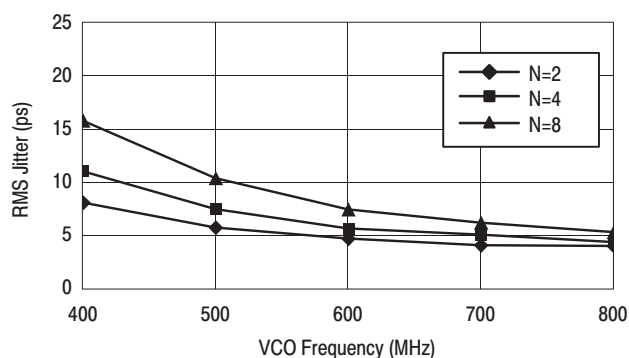


Figure 6. RMS PLL Jitter versus VCO Frequency

Figure 6 illustrates the RMS jitter performance of the MC12439 across its specified VCO frequency range. Note that the jitter is a function of both the output frequency as well as the VCO frequency, however the VCO frequency shows a much stronger dependence. The data presented has not been compensated for trigger jitter, this fact provides a measure of guardband to the reported data.

The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak-to-peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. The oscilloscope cannot collect adjacent pulses, rather it collects pulses from a very large sample of pulses.

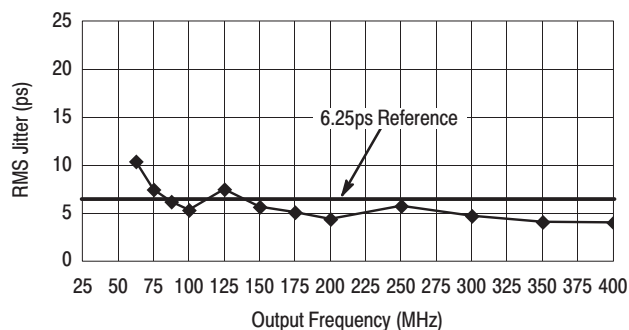


Figure 7. RMS Jitter versus Output Frequency

Figure 7 shows the jitter as a function of the output frequency. For the 12439, this information is probably of more importance. The flat line represents an RMS jitter value that corresponds to an 8 sigma ± 25 ps peak-to-peak long term period jitter. The graph shows that for output frequencies from 87.5 to 400 MHz the jitter falls within the ± 25 ps peak-to-peak specification. The general trend is that as the output frequency is decreased, the output edge jitter will increase.

The jitter data from Figure 6 does not include the performance of the 12439 when the output is in the divide by 1 mode. In divide by one mode, the MC12439 output jitter distribution is bimodal. Since a bimodal distribution cannot be accurately represented with an rms value, peak-to-peak values of jitter for the divide by one mode are presented.

Figure 8 shows the peak-to-peak jitter of the 12439 output in divide by one mode as a function of output frequency. Notice

that as with the other modes, the jitter improves with increasing frequency. The ± 65 ps shown in the data sheet table represents a conservative value of jitter, especially for the higher VCO, and thus output frequencies.

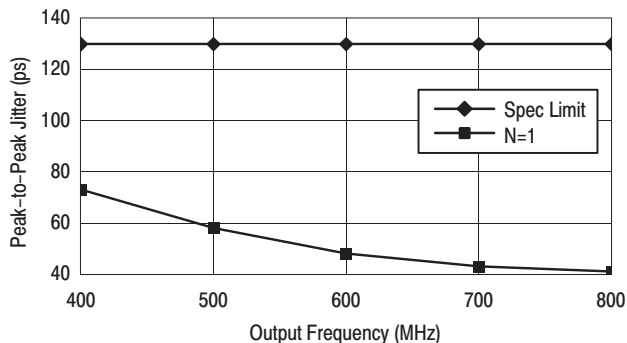


Figure 8. Peak-to-Peak Jitter versus Output Frequency

The jitter data presented should provide users with enough information to determine the effect on their overall timing budget. The jitter performance meets the needs of most system designs while adding the flexibility of frequency margining and field upgrades. These features are not available with a fixed frequency SAW oscillator.

Output Voltage Swing vs Frequency

In the divide by one mode, the output rise and fall times will limit the peak to peak output voltage swing. For a 400 MHz output, the peak to peak swing of the 12439 output will be approximately 700 mV. This swing will gradually degrade as the output frequency increases, at 800 MHz the output swing will be reduced to approximately 500 mV. For a worst case analysis, it would be safe to assume that the 12439 output will always generate at least a 400mV output swing. Note that most high speed ECL receivers require only a few hundred millivolt input swings for reliable operation. As a result, the output generated by the 12439 will, under all conditions, be sufficient for clocking standard ECL devices. Note that if a larger swing is desired, the MC12439 could drive the clock fanout buffer MC100EP111.

400 MHz Low Voltage PECL Clock Synthesizer

The MPC9229 is a 3.3V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking and computing applications. With output frequencies from 25 MHz to 400 MHz and the support of differential PECL output signals the device meets the needs of the most demanding clock applications.

Features

- 25 MHz to 400 MHz synthesized clock output signal
- Differential PECL output
- LVCMOS compatible control inputs
- On-chip crystal oscillator for reference frequency generation
- 3.3V power supply
- Fully integrated PLL
- Minimal frequency overshoot
- Serial 3-wire programming interface
- Parallel programming interface for power-up
- 32 lead LQFP and 28 PLCC packaging
- SiGe Technology
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MC12429

Functional Description

The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. The frequency of the internal crystal oscillator is divided by 16 and then multiplied by the PLL. The VCO within the PLL operates over a range of 800 to 1600 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The crystal oscillator frequency f_{XTAL} , the PLL feedback-divider M and the PLL post-divider N determine the output frequency.

The feedback path of the PLL is internal. The PLL adjusts the VCO output frequency to be 4-M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve phase lock. The PLL will be stable if the VCO frequency is within the specified VCO frequency range (800 to 1600 MHz). The M-value must be programmed by the serial or parallel interface.

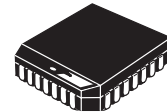
The PLL post-divider N is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle. The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated 50Ω to $V_{CC} - 2.0V$. The positive supply voltage for the internal PLL is separated from the power supply for the core logic and output drivers to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. It is recommended on system reset to hold the $\overline{P\_LOAD}$ input LOW until power becomes valid. On the LOW-to-HIGH transition of $\overline{P\_LOAD}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs prevent the LVCMOS compatible control inputs from floating.

The serial interface centers on a fourteen bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See the programming section for more information. The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. In order to minimize the PLL jitter, it is recommended to avoid active signal on the TEST output.

MPC9229

**400 MHZ LOW VOLTAGE
CLOCK SYNTHESIZER**



FN SUFFIX
28-LEAD PLCC PACKAGE
CASE 776



FA SUFFIX
32 LEAD LQFP PACKAGE
CASE 873A

4

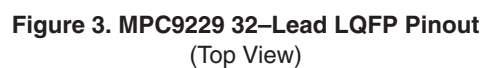
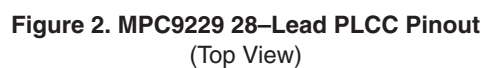


Table 1. Pin Configuration

Pin	I/O	Default	Type	Function
XTAL_IN, XTAL_OUT			Analog	Crystal oscillator interface
FOUT, FOUT	Output		LVPECL	Differential clock output
TEST	Output		LVC MOS	Test and device diagnosis output
S_LOAD	Input	0	LVC MOS	Serial configuration control input. This inputs controls the loading of the configuration latches with the contents of the shift register. The latches will be transparent when this signal is high, thus the data must be stable on the high-to-low transition.
P_LOAD	Input	1	LVC MOS	Parallel configuration control input. This input controls the loading of the configuration latches with the content of the parallel inputs (M and N). The latches will be transparent when this signal is low, thus the parallel data must be stable on the low-to-high transition of P_LOAD. P_LOAD is state sensitive
S_DATA	Input	0	LVC MOS	Serial configuration data input.
S_CLOCK	Input	0	LVC MOS	Serial configuration clock input.
M[0:8]	Input	1	LVC MOS	Parallel configuration for PLL feedback divider (M). M is sampled on the low-to-high transition of P_LOAD.
N[1:0]	Input	1	LVC MOS	Parallel configuration for Post-PLL divider (N). N is sampled on the low-to-high transition of P_LOAD
OE	Input	1	LVC MOS	Output enable (active high) The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the FOUT output. OE = L low stops FOUT in the logic low state (FOUT = L, FOUT = H)
GND	Supply	Supply	Ground	Negative power supply (GND)
VCC	Supply	Supply	VCC	Positive power supply for I/O and core. All VCC pins must be connected to the positive power supply for correct operation
VCC_PLL	Supply	Supply	VCC	PLL positive power supply (analog power supply)

4

Table 2. Output frequency range and PLL Post-divider N

N		Output division	Output frequency range
1	0		
0	0	1	200 - 400 MHz
0	1	2	100 - 200 MHz
1	0	4	50 - 100 MHz
1	1	8	25 - 50 MHz

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} - 2$		V	
MM	ESD protection (Machine Model)	200			V	
HBM	ESD protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	LQFP 32 Thermal resistance junction to ambient JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	LQFP 32 Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1

Table 4. Absolute Maximum Ratings^a

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.9	V	
V_{IN}	DC Input Voltage	-0.3	$V_{CC} + 0.3$	V	
V_{OUT}	DC Output Voltage	-0.3	$V_{CC} + 0.3$	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS control inputs (P_LOAD , S_LOAD , S_DATA , S_CLOCK , $M[0:8]$, $N[0:1]$, OE)						
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current ^a			±200	μA	$V_{IN} = V_{CC}$ or GND
Differential clock output F_{OUT}^b						
V_{OH}	Output High Voltage ^c	$V_{CC} - 1.02$		$V_{CC} - 0.74$	V	LVPECL
V_{OL}	Output Low Voltage ^c	$V_{CC} - 1.95$		$V_{CC} - 1.60$	V	LVPECL
Test and diagnosis output TEST						
V_{OH}	Output High Voltage ^c	2.0			V	$I_{OH} = -0.8$ mA
V_{OL}	Output Low Voltage ^c			0.55	V	$I_{OL} = 0.8$ mA
Supply current						
I_{CC_PLL}	Maximum PLL Supply Current			20	mA	V_{CC_PLL} Pins
I_{CC}	Maximum Supply Current			100	mA	All V_{CC} Pins

a. Inputs have pull-down resistors affecting the input current.

b. Outputs terminated 50Ω to $V_{TT} = V_{CC} - 2V$.

c. The MPC9229 TEST output levels are compatible to the MC12429 output levels.

Table 6. AC Characteristics ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{XTAL}	Crystal interface frequency range	10		20	MHz	
f_{VCO}	VCO frequency range ^b	800		1600	MHz	
f_{MAX}	Output Frequency	N = 00 (+1)	200	400	MHz	
		N = 01 (+2)	100	200	MHz	
		N = 10 (+4)	50	100	MHz	
		N = 11 (+8)	25	50	MHz	
DC	Output duty cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.05		0.3	ns	20% to 80%
f_{S_CLOCK}	Serial interface programming clock frequency ^c	0		10	MHz	
t_{P_MIN}	Minimum pulse width (S_LOAD, P_LOAD)	50			ns	
t_S	Setup Time	S_DATA to S_CLOCK	20		ns	
		S_CLOCK to S_LOAD	20		ns	
		M, N to P_LOAD	20		ns	
t_S	Hold Time	S_DATA to S_CLOCK	20		ns	
		M, N to P_LOAD	20		ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter	N = 00 (+1)		90	ps	
		N = 01 (+2)		130	ps	
		N = 10 (+4)		160	ps	
		N = 11 (+8)		190	ps	
$t_{JIT(PER)}$	Period Jitter	N = 00 (+1)		70	ps	
		N = 01 (+2)		120	ps	
		N = 10 (+4)		140	ps	
		N = 11 (+8)		170	ps	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

a AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b The input frequency f_{XTAL} and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \cdot M \div 4$.

c The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. See application section for more details.

Programming the MPC9229

Programming the MPC9229 amounts to properly configuring the internal PLL dividers to produce the desired synthesized frequency at the output. The output frequency can be represented by this formula:

$$f_{OUT} = (f_{XTAL} \div 16) \cdot (4 \cdot M) \div (4 \cdot N) \text{ or} \quad (1)$$

$$f_{OUT} = (f_{XTAL} \div 16) \cdot M \div N \quad (2)$$

where f_{XTAL} is the crystal frequency, M is the PLL feedback-divider and N is the PLL post-divider. The input frequency and the selection of the feedback divider M is limited by the VCO-frequency range. f_{XTAL} and M must be configured to

match the VCO frequency range of 800 to 1600 MHz in order to achieve stable PLL operation:

$$M_{MIN} = 4 \cdot f_{VCO,MIN} \div f_{XTAL} \text{ and} \quad (3)$$

$$M_{MAX} = 4 \cdot f_{VCO,MAX} \div f_{XTAL} \quad (4)$$

For instance, the use of a 16 MHz input frequency requires the configuration of the PLL feedback divider between M=200 and M = 400. Table 7 shows the usable VCO frequency and M divider range for other example input frequencies. Assuming that a 16 MHz input frequency is used, equation (2) reduces to:

$$f_{OUT} = M \div N \quad (5)$$

Table 7. MPC9229 Frequency Operating Range

M	M[8:0]	VCO frequency for an crystal interface frequency of						Output frequency for $f_{XTAL}=16$ MHz and for N =			
		10	12	14	16	18	20	1	2	4	16
160	010100000						800				
170	010101010						850				
180	010110100					810	900				
190	010111110					855	950				
200	011001000				800	900	1000	200	100	50	25
210	011010010				840	945	1050	210	105	52.5	26.25
220	011011100				880	990	1100	220	110	55	27.50
230	011100110			805	920	1035	1150	230	115	57.5	28.75
240	011110000			840	960	1080	1200	240	120	60	30
250	011111010			875	100	1125	1250	250	125	62.5	31.25
260	100000100			910	1040	1170	1300	260	130	65	32.50
270	100001110		810	945	1080	1215	1350	270	135	67.5	33.75
280	100011000		840	980	1120	1260	1400	280	140	70	35
290	100100010		870	1015	1160	1305	1450	290	145	72.5	36.25
300	100101100		900	1050	1200	1350	1500	300	150	75	37.5
310	100110110		930	1085	1240	1395	1550	310	155	77.5	38.75
320	101000000	800	960	1120	1280	1440	1600	320	160	80	40
330	101001010	825	990	1155	1320	1485		330	165	82.5	41.25
340	101010100	850	1020	1190	1360	1530		340	170	85	42.5
350	101011110	875	1050	1225	1400	1575		350	175	87.5	43.75
360	101101000	900	1080	1260	1440			360	180	90	45
370	101110010	925	1110	1295	1480			370	185	92.5	46.25
380	101111100	950	1140	1330	1520			380	190	95	47.5
390	110000110	975	1170	1365	1560			390	195	97.5	48.75
400	110010000	1000	1200	1400	1600			400	200	100	50
410	110011010	1025	1230	1435							
420	110100100	1050	1260	1470							
430	110101110	1075	1290	1505							
440	110111000	1100	1320	1540							
450	111000010	1125	1350	1575							
510	111111110	1275	1530								

Substituting N for the four available values for N (1, 2, 4, 8) yields:

Table 8. Output Frequency Range for $f_{XTAL} = 16$ MHz

N			F _{OUT}	F _{OUT} range	F _{OUT} step
1	0	Value			
0	0	1	M	200 - 400 MHz	1 MHz
0	1	2	M÷2	100 - 200 MHz	500 kHz
1	0	4	M÷4	50 - 100 MHz	250 kHz
1	1	8	M÷8	25 - 50 MHz	125 kHz

Example frequency calculation for an 16 MHz input frequency

If an output frequency of 131 MHz was desired the following steps would be taken to identify the appropriate M and N values. According to Table 8, 131 MHz falls in the frequency set by an value of 2 so N[1:0] = 01. For N = 2 the output frequency is F_{OUT} = M÷2 and M = F_{OUT} × 2. Therefore M = 2 × 131 = 262, so M[8:0] = 10000110. Following this procedure a user can generate any whole frequency between 25 MHz and 400 MHz. Note that for N > 2 fractional values of can be realized. The size of the programmable frequency steps (and thus the indicator of the fractional output frequencies achievable) will be equal to:

$$f_{STEP} = f_{XTAL} \div 16 \div N \quad (6)$$

Using the parallel and serial interface

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the $\overline{P\_LOAD}$ signal such that a LOW to HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the $\overline{P\_LOAD}$ signal is LOW the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14 bit shift register. Note that the $\overline{P\_LOAD}$ signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 4 illustrates the timing diagram for both a parallel and a serial load of the MPC9229 synthesizer. M[8:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

Using the test and diagnosis output TEST

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents F_{OUT}, the CMOS output is not able to toggle fast enough for higher output frequencies and should only be used for test and diagnosis. The T2, T1 and T0 control bits are preset to '000' when $\overline{P\_LOAD}$ is LOW so that the PECL FOUT outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin. Most of the signals available on the TEST output pin are useful only for performance verification of the MPC9229 itself. However the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MPC9229 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the F_{OUT} differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving F_{OUT} directly gives the user more control on the test clocks sent through the clock tree. Figure 6 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 200 MHz. This means the fastest the F_{OUT} pin can be toggled via the S_CLOCK is 100 MHz as the divide ratio of the Post-PLL divider is 2 (if N = 1). Note that the M counter output on the TEST output will not be a 50% duty cycle.

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Table 9. Test and Debug Configuration for TEST

T[2:0]			TEST output
T2	T1	T0	
0	0	0	14-bit shift register out ^a
0	0	1	Logic 1
0	1	0	$f_{XTAL} \div 16$
0	1	1	M-Counter out
1	0	0	FOUT
1	0	1	Logic 0
1	1	0	M-Counter out in PLL-bypass mode
1	1	1	FOUT ÷ 4

a. Clocked out at the rate of S_CLOCK

Table 10. Debug Configuration for PLL bypass^a

Output	Configuration
F _{OUT}	S_CLOCK ÷ N
TEST	M-Counter out ^b

a. T[2:0]=110. AC specifications do not apply in PLL bypass mode

b. clocked out at the rate of S_CLOCK÷(4·N)

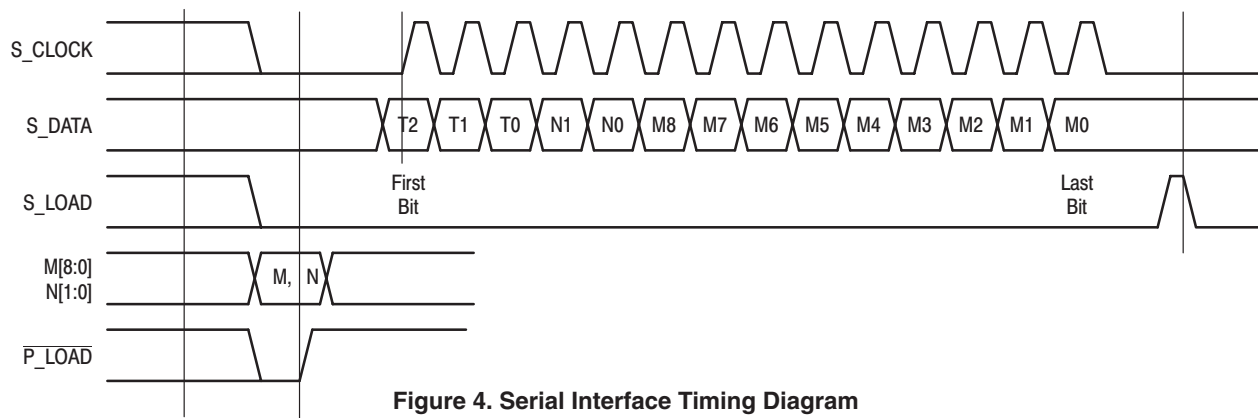


Figure 4. Serial Interface Timing Diagram

Power Supply Filtering

The MPC9229 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the VCC_PLL pin impacts the device characteristics. The MPC9229 provides separate power supplies for the digital circuitry (VCC) and the internal PLL (VCC_PLL) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCC_PLL pin for the MPC9229. Figure 5 illustrates a typical power supply filter scheme. The MPC9229 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the VCC supply and the MPC9229 pin of the MPC9229. From the data sheet, the VCC_PLL current (the current sourced through the VCC_PLL pin) is maximum 20 mA, assuming that a minimum of 2.835 V must be maintained on the VCC_PLL pin. The resistor shown in Figure 5 must have a resistance of 10-15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering. A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000 μ H choke will show a significant impedance at 10 kHz frequencies and above. Because of the current draw and the voltage that must be maintained on the VCC_PLL pin, a low DC resistance inductor is required (less than 15 Ω).

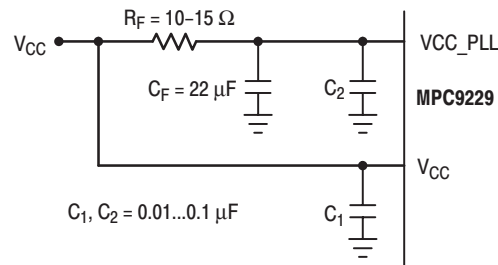


Figure 5. VCC_PLL Power Supply Filter

Layout Recommendations

The MPC9229 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 6 shows a representative board layout for the MPC9229. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 6 is the low impedance connections between VCC and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the MPC9229 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors. Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator. Although the MPC9229 has several design features to minimize the susceptibility to power

supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

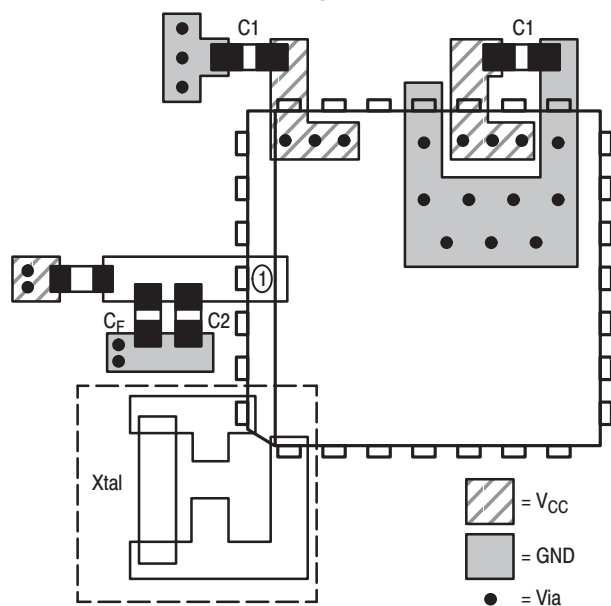


Figure 6. PCB Board Layout Recommendation for the PLCC28 Package

Using the On-Board Crystal Oscillator

The MPC9229 features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC9229 as possible to avoid any board level

parasitics. To facilitate co-location surface mount crystals are recommended, but not required. Because the series resonant design is affected by capacitive loading on the xtal terminals loading variation introduced by crystals from different vendors could be a potential issue. For crystals with a higher shunt capacitance it may be required to place a resistance across the terminals to suppress the third harmonic. Although typically not required it is a good idea to layout the PCB with the provision of adding this external resistor. The resistor value will typically be between 500 and 1K Ω .

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately most crystals are characterized in a parallel resonant mode. Fortunately there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result a parallel resonant crystal can be used with the MPC9229 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application this level of inaccuracy is immaterial. Table 11 below specifies the performance requirements of the crystals to be used with the MPC9229.

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Table 11. Recommended Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	± 75 ppm at 25°C
Frequency/Temperature Stability	± 150 pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80 Ω
Correlation Drive Level	100 μ W
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

800 MHz Low Voltage PECL Clock Synthesizer

The MPC9230 is a 3.3V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking and computing applications. With output frequencies from 50 MHz to 800 MHz and the support of differential PECL output signals the device meets the needs of the most demanding clock applications.

Features

- 50 MHz to 800 MHz synthesized clock output signal
- Differential PECL output
- LVCMOS compatible control inputs
- On-chip crystal oscillator for reference frequency generation
- Alternative LVCMOS compatible reference clock input
- 3.3V power supply
- Fully integrated PLL
- Minimal frequency overshoot
- Serial 3-wire programming interface
- Parallel programming interface for power-up
- 32 lead LQFP and 28 PLCC packaging
- SiGe Technology
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MC12430

Functional Description

The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. The frequency of the internal crystal oscillator is divided by 16 and then multiplied by the PLL. The VCO within the PLL operates over a range of 800 to 1600 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The crystal oscillator frequency f_{XTAL} , the PLL feedback-divider M and the PLL post-divider N determine the output frequency.

The feedback path of the PLL is internal. The PLL adjusts the VCO output frequency to be 8·M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve phase lock. The PLL will be stable if the VCO frequency is within the specified VCO frequency range (800 to 1600 MHz). The M-value must be programmed by the serial or parallel interface.

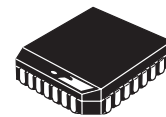
The PLL post-divider N is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle. The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated 50Ω to $V_{CC} - 2.0V$. The positive supply voltage for the internal PLL is separated from the power supply for the core logic and output drivers to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. It is recommended on system reset to hold the $\overline{P\_LOAD}$ input LOW until power becomes valid. On the LOW-to-HIGH transition of $\overline{P\_LOAD}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs prevent the LVCMOS compatible control inputs from floating.

The serial interface centers on a fourteen bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See the programming section for more information. The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. In order to minimize the PLL jitter, it is recommended to avoid active signal on the TEST output.

MPC9230

**800 MHZ LOW VOLTAGE
CLOCK SYNTHESIZER**



FN SUFFIX
28 LEAD PLCC PACKAGE
CASE 776



FA SUFFIX
32 LEAD LQFP PACKAGE
CASE 873A



Table 1. Pin Configuration

Pin	I/O	Default	Type	Function
XTAL_IN, XTAL_OUT			Analog	Crystal oscillator interface
FREF_EXT	Input	0	LVC MOS	Alternative PLL reference input
FOUT, $\overline{\text{FOUT}}$	Output		LVPECL	Differential clock output
TEST	Output		LVPECL	Test and device diagnosis output
XTAL_SEL	Input	1	LVC MOS	PLL reference select input
S_LOAD	Input	0	LVC MOS	Serial configuration control input. This input controls the loading of the configuration latches with the contents of the shift register. The latches will be transparent when this signal is high, thus the data must be stable on the high-to-low transition.
P_LOAD	Input	1	LVC MOS	Parallel configuration control input. This input controls the loading of the configuration latches with the content of the parallel inputs (M and N). The latches will be transparent when this signal is low, thus the parallel data must be stable on the low-to-high transition of P_LOAD. P_LOAD is state sensitive
S_DATA	Input	0	LVC MOS	Serial configuration data input.
S_CLOCK	Input	0	LVC MOS	Serial configuration clock input.
M[0:8]	Input	1	LVC MOS	Parallel configuration for PLL feedback divider (M). M is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$.
N[1:0]	Input	1	LVC MOS	Parallel configuration for Post-PLL divider (N). N is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$
OE	Input	1	LVC MOS	Output enable (active high) The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the FOUT output.
GND	Supply	Supply	Ground	Negative power supply (GND)
V _{CC}	Supply	Supply	V _{CC}	Positive power supply for I/O and core. All V _{CC} pins must be connected to the positive power supply for correct operation
VCC_PLL	Supply	Supply	V _{CC}	PLL positive power supply (analog power supply)

Table 2. Output frequency range and PLL Post-divider N

N		Output division	Output frequency range
1	0		
0	0	2	200 - 400 MHz
0	1	4	100 - 200 MHz
1	0	8	50 - 100 MHz
1	1	1	400 - 800 MHz

Table 3. Function Table

Input	0	1
XTAL_SEL	FREF_EXT	XTAL interface
OE	Outputs disabled, FOUT is stopped in the logic low state (FOUT = L, $\overline{\text{FOUT}}$ = H)	Outputs enabled

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		$V_{CC} - 2$		V	
MM	ESD protection (Machine model)	200			V	
HBM	ESD protection (Human body model)	2000			V	
LU	Latch-up immunity	200			mA	
C_{IN}	Input capacitance		4.0		pF	Inputs
θ_{JA}	LQFP 32 Thermal resistance junction to ambient JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	LQFP 32 Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1

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Table 5. Absolute Maximum Ratings^a

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	4.6	V	
V_{IN}	DC Input Voltage	-0.3	$V_{CC} + 0.3$	V	
V_{OUT}	DC Output Voltage	-0.3	$V_{CC} + 0.3$	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. DC Characteristics ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS control inputs (FREF_EXT, XTAL_SEL, P_LOAD, S_LOAD, S_DATA, S_CLOCK, M[0:8], N[0:1], OE)						
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current ^a			±200	μA	$V_{IN} = V_{CC}$ or GND
Differential clock output F_{OUT}^b						
V_{OH}	Output High Voltage	$V_{CC} - 1.02$		$V_{CC} - 0.74$	V	LVPECL
V_{OL}	Output Low Voltage	$V_{CC} - 1.95$		$V_{CC} - 1.60$	V	LVPECL
Test and diagnosis output TEST						
V_{OH}	Output High Voltage	$V_{CC} - 1.02$		$V_{CC} - 0.74$	V	LVPECL
V_{OL}	Output Low Voltage	$V_{CC} - 1.95$		$V_{CC} - 1.60$	V	LVPECL
Supply current						
I_{CC_PLL}	Maximum PLL Supply Current			20	mA	V_{CC_PLL} Pins
I_{CC}	Maximum Supply Current			110	mA	All V_{CC} Pins

a. Inputs have pull-down resistors affecting the input current.

b. Outputs terminated 50Ω to $V_{TT} = V_{CC} - 2V$.

Table 7. AC Characteristics ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{XTAL}	Crystal interface frequency range	10		20	MHz	
f_{REF}	FREF_EXT reference frequency range	10		$(f_{VCO,MAX} \div M) \cdot 4$ ^b	MHz	
f_{VCO}	VCO frequency range ^c	800		1600	MHz	
f_{MAX}	Output Frequency N = 11 ($\div 1$) N = 00 ($\div 2$) N = 01 ($\div 4$) N = 10 ($\div 8$)	400		800	MHz	
		200		400	MHz	
		100		200	MHz	
		50		100	MHz	
f_{S_CLOCK}	Serial interface programming clock frequency ^d	0		10	MHz	
$t_{P,MIN}$	Minimum pulse width (S_LOAD, P_LOAD)	50			ns	
DC	Output duty cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.05		0.3	ns	20% to 80%
t_s	Setup Time S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to P_LOAD	20			ns	
		20			ns	
		20			ns	
t_s	Hold Time S_DATA to S_CLOCK M, N to P_LOAD	20			ns	
		20			ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter N = 11 ($\div 1$) N = 00 ($\div 2$) N = 01 ($\div 4$) N = 10 ($\div 8$)			80	ps	
				90	ps	
				130	ps	
				160	ps	
$t_{JIT(PER)}$	Period Jitter N = 11 ($\div 1$) N = 00 ($\div 2$) N = 01 ($\div 4$) N = 10 ($\div 8$)			60	ps	
				70	ps	
				120	ps	
				140	ps	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

a AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b The maximum frequency on FREF_EXT is a function of the max. VCO frequency and the M counter. M should be higher than 160 for stable PLL operation.

c The input frequency f_{XTAL} and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \cdot M \div 4$.

d The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. See application section for more details.

Programming the MPC9230

Programming the MPC9230 amounts to properly configuring the internal PLL dividers to produce the desired synthesized frequency at the output. The output frequency can be represented by this formula:

$$f_{OUT} = (f_{XTAL} \div 16) \cdot (4 \cdot M) \div (2 \cdot N) \text{ or} \quad (1)$$

$$f_{OUT} = (f_{XTAL} \div 8) \cdot M \div N \quad (2)$$

where f_{XTAL} is the crystal frequency, M is the PLL feedback-divider and N is the PLL post-divider. The input frequency and the selection of the feedback divider M is limited by the VCO-frequency range. f_{XTAL} and M must be configured to

match the VCO frequency range of 800 to 1600 MHz in order to achieve stable PLL operation:

$$M_{MIN} = 4 \cdot f_{VCO,MIN} \div f_{XTAL} \text{ and} \quad (3)$$

$$M_{MAX} = 4 \cdot f_{VCO,MAX} \div f_{XTAL} \quad (4)$$

For instance, the use of a 16 MHz input frequency requires the configuration of the PLL feedback divider between M=200 and M = 400. Table 8 shows the usable VCO frequency and M divider range for other example input frequencies. Assuming that a 16 MHz input frequency is used, equation (2) reduces to:

$$f_{OUT} = 2 \cdot M \div N \quad (5)$$

Table 8. MPC9230 Frequency Operating Range

M	M[8:0]	VCO frequency for an crystal interface frequency of						Output frequency for $f_{XTAL}=16$ MHz and for N =			
		10	12	14	16	18	20	1	2	4	8
160	010100000						800				
170	010101010						850				
180	010110100					810	900				
190	010111110					855	950				
200	011001000				800	900	1000	400	200	100	50
210	011010010				840	945	1050	420	210	105	52.5
220	011011100				880	990	1100	440	220	110	55
230	011100110			805	920	1035	1150	460	230	115	57.5
240	011110000			840	960	1080	1200	480	240	120	60
250	011111010			875	100	1125	1250	500	250	125	62.5
260	100000100			910	1040	1170	1300	520	260	130	65
270	100001110		810	945	1080	1215	1350	540	270	135	67.5
280	100011000		840	980	1120	1260	1400	560	280	140	70
290	100100010		870	1015	1160	1305	1450	580	290	145	72.5
300	100101100		900	1050	1200	1350	1500	600	300	150	75
310	100110110		930	1085	1240	1395	1550	620	310	155	77.5
320	101000000	800	960	1120	1280	1440	1600	640	320	160	80
330	101001010	825	990	1155	1320	1485		660	330	165	82.5
340	101010100	850	1020	1190	1360	1530		680	340	170	85
350	101011110	875	1050	1225	1400	1575		700	350	175	87.5
370	101110010	925	1110	1295	1480			740	370	185	92.5
380	101111100	950	1140	1330	1520			760	380	190	95
390	110000110	975	1170	1365	1560			780	390	195	97.5
400	110010000	1000	1200	1400	1600			800	400	200	100
410	110011010	1025	1230	1435							
420	110100100	1050	1260	1470							
430	110101110	1075	1290	1505							
440	110111000	1100	1320	1540							
450	111000010	1125	1350	1575							
510	111111110	1275	1530								

Substituting N for the four available values for N (1, 2, 4, 8) yields:

Table 9. Output Frequency Range for $f_{XTAL} = 16$ MHz

N			F _{OUT}	F _{OUT} range	F _{OUT} step
1	0	Value			
0	0	2	M	200 - 400 MHz	1 MHz
0	1	4	M+2	100 - 200 MHz	500 kHz
1	0	8	M+4	50 - 100 MHz	250 kHz
1	1	1	2 · M	400 - 800 MHz	2 MHz

Example frequency calculation for an 16 MHz input frequency

If an output frequency of 131 MHz was desired the following steps would be taken to identify the appropriate M and N values. According to Table 9, 131 MHz falls in the frequency set by a value of 4 so N[1:0] = 01. For N = 4 the output frequency is $F_{OUT} = M + 2$ and $M = F_{OUT} \times 2$. Therefore $M = 2 \times 131 = 262$, so M[8:0] = 01000011. Following this procedure a user can generate any whole frequency between 50 MHz and 800 MHz. Note that for $N > 2$ fractional values of can be realized. The size of the programmable frequency steps (and thus the indicator of the fractional output frequencies achievable) will be equal to:

$$f_{STEP} = f_{XTAL} \div 8 \div N \quad (6)$$

Using the parallel and serial interface

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the $\overline{P\_LOAD}$ signal such that a LOW to HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the $\overline{P\_LOAD}$ signal is LOW the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14 bit shift register. Note that the $\overline{P\_LOAD}$ signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 4 illustrates the timing diagram for both a parallel and a serial load of the MPC9230 synthesizer. M[8:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

Using the test and diagnosis output TEST

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents FOUT, the LVPECL compatible TEST output is not able to toggle fast enough for higher output frequencies and should only be used for test and diagnosis. The T2, T1 and T0 control bits are preset to '000' when $\overline{P\_LOAD}$ is LOW so that the LVPECL compatible FOUT outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin. Most of the signals available on the TEST output pin are useful only for performance verification of the MPC9230 itself. However the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MPC9230 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clock tree. Table 10 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 200 MHz. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 50 MHz as the divide ratio of the Post-PLL divider is 4 (if N = 1). Note that the M counter output on the TEST output will not be a 50% duty cycle.

Table 10. Test and Debug Configuration for TEST

T[2:0]			TEST output
T2	T1	T0	
0	0	0	14-bit shift register out ^a
0	0	1	Logic 1
0	1	0	$f_{XTAL} \div 16$
0	1	1	M-Counter out
1	0	0	FOUT
1	0	1	Logic 0
1	1	0	M-Counter out in PLL-bypass mode
1	1	1	$FOUT \div 4$

a. Clocked out at the rate of S_CLOCK

Table 11. Debug Configuration for PLL bypass^a

Output	Configuration
FOUT	$S\_CLOCK \div N$
TEST	M-Counter out ^b

a. T[2:0]=110. AC specifications do not apply in PLL bypass mode

b. clocked out at the rate of $S\_CLOCK \div (2 \cdot N)$

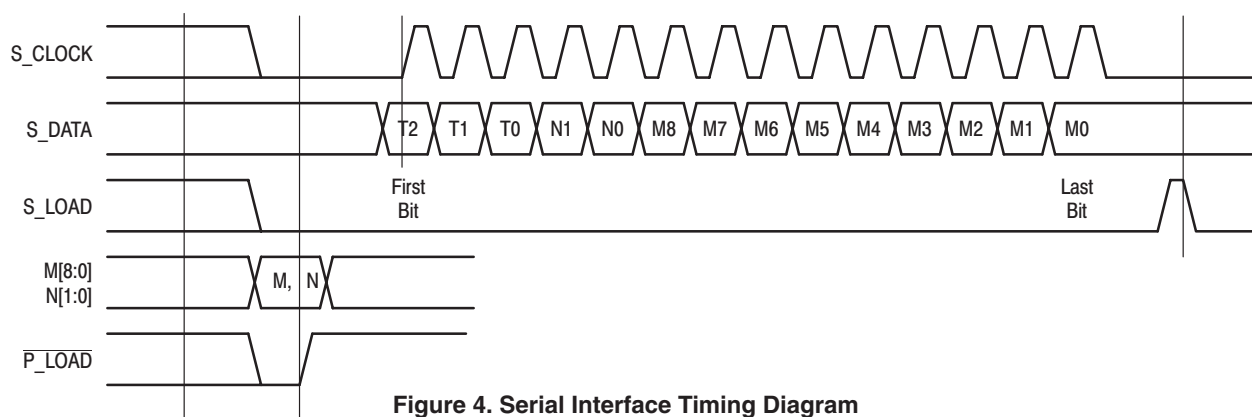


Figure 4. Serial Interface Timing Diagram

Power Supply Filtering

The MPC9230 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the VCC_PLL pin impacts the device characteristics. The MPC9230 provides separate power supplies for the digital circuitry (VCC) and the internal PLL (VCC_PLL) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCC_PLL pin for the MPC9230. Figure 5 illustrates a typical power supply filter scheme. The MPC9230 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the VCC supply and the MPC9230 pin of the MPC9230. From the data sheet, the VCC_PLL current (the current sourced through the VCC_PLL pin) is maximum 20 mA, assuming that a minimum of 2.835 V must be maintained on the VCC_PLL pin. The resistor shown in Figure 5 must have a resistance of 10-15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering. A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000 μ H choke will show a significant impedance at 10 kHz frequencies and above. Because of the current draw and the voltage that must be maintained on the VCC_PLL pin, a low DC resistance inductor is required (less than 15 Ω).

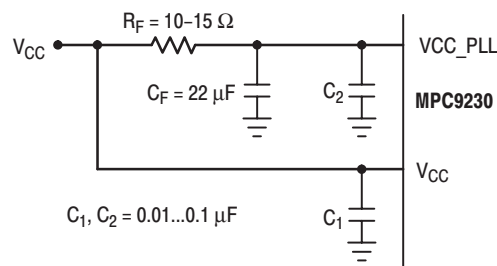


Figure 5. VCC_PLL Power Supply Filter

Layout Recommendations

The MPC9230 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 6 shows a representative board layout for the MPC9230. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 6 is the low impedance connections between VCC and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the MPC9230 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors. Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator. Although the MPC9230 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential

PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

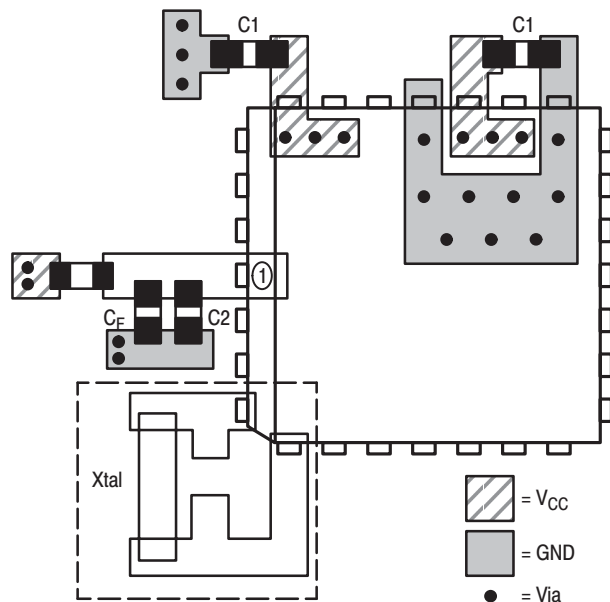


Figure 6. PCB Board Layout Recommendation for the PLCC28 Package

Using the On-Board Crystal Oscillator

The MPC9230 features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC9230 as possible to avoid any board level

parasitics. To facilitate co-location surface mount crystals are recommended, but not required. Because the series resonant design is affected by capacitive loading on the xtal terminals loading variation introduced by crystals from different vendors could be a potential issue. For crystals with a higher shunt capacitance it may be required to place a resistance across the terminals to suppress the third harmonic. Although typically not required it is a good idea to layout the PCB with the provision of adding this external resistor. The resistor value will typically be between 500 and 1K Ω .

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately most crystals are characterized in a parallel resonant mode. Fortunately there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result a parallel resonant crystal can be used with the MPC9230 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application this level of inaccuracy is immaterial. Table 12 below specifies the performance requirements of the crystals to be used with the MPC9230.

Table 12. Recommended Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	± 75 ppm at 25°C
Frequency/Temperature Stability	± 150 ppm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80 Ω
Correlation Drive Level	100 μ W
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

900 MHz Low Voltage LVPECL Clock Synthesizer

The MPC9239 is a 3.3V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking and computing applications. With output frequencies from 3.125 MHz to 900 MHz and the support of differential LVPECL output signals the device meets the needs of the most demanding clock applications.

Features

- 3.125 MHz to 900 MHz synthesized clock output signal
- Differential LVPECL output
- LVCMOS compatible control inputs
- On-chip crystal oscillator for reference frequency generation
- Alternative LVCMOS compatible reference input
- 3.3V power supply
- Fully integrated PLL
- Minimal frequency overshoot
- Serial 3-wire programming interface
- Parallel programming interface for power-up
- 28 PLCC and 32 LQFP packaging
- SiGe Technology
- Ambient temperature range 0°C to + 70°C
- Pin and function compatible to the MC12439

Functional Description

The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. The frequency of the internal crystal oscillator or external reference clock signal is multiplied by the PLL. The VCO within the PLL operates over a range of 800 to 1800 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The crystal oscillator frequency f_{XTAL} , the PLL feedback-divider M and the PLL post-divider N determine the output frequency.

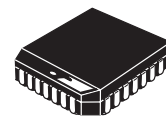
The feedback path of the PLL is internal. The PLL adjusts the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve phase lock. The PLL will be stable if the VCO frequency is within the specified VCO frequency range (800 to 1800 MHz). The M-value must be programmed by the serial or parallel interface.

The PLL post-divider N is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle. The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated 50Ω to $V_{CC} - 2.0V$. The positive supply voltage for the internal PLL is separated from the power supply for the core logic and output drivers to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[6:0] and N[1:0] inputs to configure the internal counters. It is recommended on system reset to hold the $\overline{P\_LOAD}$ input LOW until power becomes valid. On the LOW-to-HIGH transition of $\overline{P\_LOAD}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[6:0] and N[1:0] inputs prevent the LVCMOS compatible control inputs from floating. The serial interface centers on a twelve bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See the programming section for more information. The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. In order to minimize the PLL jitter, it is recommended to avoid active signal on the TEST output. The PWR_DOWN pin, when asserted, will synchronously divide the FOUT by 16. The power down sequence is clocked by the PLL reference clock, thereby causing the frequency reduction to happen relatively slowly. Upon de-assertion of the PWR_DOWN pin, the FOUT input will step back up to its programmed frequency in four discrete increments.

MPC9239

**900 MHZ LOW VOLTAGE
CLOCK SYNTHESIZER**



FN SUFFIX
28-LEAD PLCC PACKAGE
CASE 776



FA SUFFIX
32 LEAD LQFP PACKAGE
CASE 873A

4



Table 1. Pin Configuration

Pin	I/O	Default	Type	Function
XTAL_IN, XTAL_OUT			Analog	Crystal oscillator interface
FREF_EXT	Input	0	LVC MOS	Alternative PLL reference input
FOUT, $\overline{\text{FOUT}}$	Output		LVPECL	Differential clock output
TEST	Output		LVC MOS	Test and device diagnosis output
XTAL_SEL	Input	1	LVC MOS	PLL reference select input
PWR_DOWN	Input	0	LVC MOS	Configuration input for power down mode. Assertion (deassertion) of power down will decrease (increase) the output frequency by a ratio of 16 in 4 discrete steps. PWR_DOWN assertion (deassertion) is synchronous to the input reference clock.
S_LOAD	Input	0	LVC MOS	Serial configuration control input. This inputs controls the loading of the configuration latches with the contents of the shift register. The latches will be transparent when this signal is high, thus the data must be stable on the high-to-low transition.
$\overline{\text{P\_LOAD}}$	Input	1	LVC MOS	Parallel configuration control input. this input controls the loading of the configuration latches with the content of the parallel inputs (M and N). The latches will be transparent when this signal is low, thus the parallel data must be stable on the low-to-high transition of $\overline{\text{P\_LOAD}}$. $\overline{\text{P\_LOAD}}$ is state sensitive.
S_DATA	Input	0	LVC MOS	Serial configuration data input.
S_CLOCK	Input	0	LVC MOS	Serial configuration clock input.
M[0:6]	Input	1	LVC MOS	Parallel configuration for PLL feedback divider (M). M is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$.
N[1:0]	Input	1	LVC MOS	Parallel configuration for Post-PLL divider (N). N is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$.
OE	Input	1	LVC MOS	Output enable (active high) The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the FOUT output. OE = L low stops FOUT in the logic low state (FOUT = L, $\overline{\text{FOUT}}$ = H).
GND	Supply		Ground	Negative power supply (GND).
V _{CC}	Supply		V _{CC}	Positive power supply for I/O and core. All V _{CC} pins must be connected to the positive power supply for correct operation.
VCC_PLL	Supply		V _{CC}	PLL positive power supply (analog power supply).
NC				Do not connect

Table 2. Output frequency range and PLL Post-divider N

PWR_DOWN	N		VCO Output frequency division	FOUT frequency range
	1	0		
0	0	0	2	200 - 450 MHz
0	0	1	4	100 - 225 MHz
0	1	0	8	50 - 112.5 MHz
0	1	1	1	400 - 900 MHz
1	0	0	32	12.5 - 28.125 MHz
1	0	1	64	6.25 - 14.0625 MHz
1	1	0	128	3.125 - 7.03125 MHz
1	1	1	16	25 - 56.25 MHz

Table 3. FUNCTION TABLE

Input	0	1
XTAL_SEL	FREF_EXT	XTAL interface
OE	Outputs disabled. FOUT is stopped in the logic low state (FOUT = L, $\overline{\text{FOUT}}$ = H)	Outputs enabled
PWR_DOWN	Output divider ÷ 1	Output divider ÷ 16

Table 4. GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} - 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	LQFP 32 Thermal resistance junction to ambient JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	LQFP 32 Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1

Table 5. ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	4.6	V	
V_{IN}	DC Input Voltage	-0.3	$V_{CC} + 0.3$	V	
V_{OUT}	DC Output Voltage	-0.3	$V_{CC} + 0.3$	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	-65	125	°C	

^a Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS control inputs (FREF_EXT, PWR_DOWN, XTAL_SEL, P_LOAD, S_LOAD, S_DATA, S_CLOCK, M[0:8], N[0:1], OE)						
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current ^a			± 200	μA	$V_{IN} = V_{CC}$ or GND
Differential clock output FOUT ^b						
V_{OH}	Output High Voltage ^c	$V_{CC} - 1.02$		$V_{CC} - 0.74$	V	LVPECL
V_{OL}	Output Low Voltage ^c	$V_{CC} - 1.95$		$V_{CC} - 1.60$	V	LVPECL
Test and diagnosis output TEST						
V_{OH}	Output High Voltage	2.0			V	$I_{OH} = -0.8$ mA
V_{OL}	Output Low Voltage			0.55	V	$I_{OL} = 0.8$ mA
Supply current						
I_{CC_PLL}	Maximum PLL Supply Current			20	mA	V_{CC_PLL} Pins
I_{CC}	Maximum Supply Current		62	110	mA	All V_{CC} Pins

a. Inputs have pull-down resistors affecting the input current.

b. Outputs terminated 50Ω to $V_{TT} = V_{CC} - 2V$.

c. The MPC9239 FOUT output levels are compatible to the MC12439 output levels. The MPC9239 is capable of driving 25Ω loads.

Table 7. AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{XTAL}	Crystal interface frequency range	10		20	MHz	
f_{VCO}	VCO frequency range ^b	800		1800	MHz	
f_{MAX}	Output Frequency N = 11 (+1) N = 00 (+2) N = 01 (+4) N = 10 (+8)	400 200 100 50		900 450 225 112.5	MHz MHz MHz MHz	PWR_DOWN = 0
f_{S_CLOCK}	Serial interface programming clock frequency ^c	0		10	MHz	
t_{P_MIN}	Minimum pulse width (S_LOAD, P_LOAD)	50			ns	
DC	Output duty cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.05		0.3	ns	20% to 80%
t_S	Setup Time S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to P_LOAD	20 20 20			ns ns ns	
t_S	Hold Time S_DATA to S_CLOCK M, N to P_LOAD	20 20			ns ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter N = 11 (+1) N = 00 (+2) N = 01 (+4) N = 10 (+8)			60 90 120 160	ps ps ps ps	
$t_{JIT(PER)}$	Period Jitter N = 11 (+1) N = 00 (+2) N = 01 (+4) N = 10 (+8)			40 65 90 120	ps ps ps ps	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b. The input frequency f_{XTAL} and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \cdot 2 \cdot M$.

c. The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. See application section for more details.

Table 8. MPC9239 Frequency Operating Range (in MHz)

M	M[6:0]	VCO frequency for an crystal interface frequency of						Output frequency for $f_{XTAL}=16\text{ MHz}$ and for $N =$			
		10 MHz	12 MHz	14 MHz	16 MHz	18 MHz	20 MHz	1	2	4	8
20	0010100						800				
21	0010101						840				
22	0010110						880				
23	0010111					828	920				
24	0011000					864	960				
25	0011001				800	900	1000	400	200	100	50
26	0011010				832	936	1040	416	208	104	52
27	0011011				864	972	1080	432	216	108	54
28	0011100			812	896	1008	1120	448	224	112	56
29	0011101			840	928	1044	1160	464	232	116	58
30	0011110			875	960	1080	1200	480	240	120	60
31	0011111			868	992	1116	1240	496	248	124	62
32	0100000			896	1024	1152	1280	512	256	128	64
33	0100001			924	1056	1188	1320	528	264	132	66
34	0100010		816	952	1088	1224	1360	544	272	136	68
35	0100011		840	980	1120	1260	1400	560	280	140	70
36	0100100		864	1008	1152	1296	1440	576	288	144	72
37	0100101		888	1036	1184	1332	1480	592	296	148	74
38	0100110		912	1064	1216	1368	1520	608	304	152	76
39	0100111		936	1092	1248	1404	1560	624	312	156	78
40	0101000	800	960	1120	1280	1440	1600	640	320	160	80
41	0101001	820	984	1148	1312	1476	1640	656	328	164	82
42	0101010	840	1008	1176	1344	1512	1680	672	336	168	84
43	0101011	860	1032	1204	1376	1548	1720	688	344	172	86
44	0101100	880	1056	1232	1408	1584	1760	704	352	176	88
45	0101101	900	1080	1260	1440	1620	1800	720	360	180	90
46	0101110	920	1104	1288	1472	1656		736	368	184	92
47	0101111	940	1128	1316	1504	1692		752	376	188	94
48	0110000	960	1152	1344	1536	1728		768	384	192	96
49	0110001	980	1176	1372	1568	1764		784	392	196	98
50	0110010	1000	1200	1400	1600	1800		800	400	200	100
51	0110011	1020	1224	1428	1632			816	408	204	102
52	0110100	1040	1248	1456	1664			832	416	208	104
53	0110101	1060	1272	1484	1696			848	424	212	106
54	0110110	1080	1296	1512	1728			864	432	216	108
55	0110111	1100	1320	1540	1760			880	440	220	110
56	0111000	1120	1344	1568	1792			896	448	224	112
57	0111001	1140	1368	1596							
58	0111010	1160	1392	1624							
59	0111011	1180	1416	1652							
60	0111100	1200	1440	1680							
61	0111101	1220	1488	1736							
62	0111110	1260	1512	1764							
63	0111111	1260	1512	1764							
64	1000000	1280	1536	1792							
...		...	...	...							

Programming the MPC9239

Programming the MPC9239 amounts to properly configuring the internal PLL dividers to produce the desired synthesized frequency at the output. The output frequency can be represented by this formula:

$$f_{OUT} = (f_{XTAL} \div 2) \cdot (M \cdot 4) \div (N \cdot 2) \text{ or} \quad (1)$$

$$f_{OUT} = f_{XTAL} \cdot M \div N \quad (2)$$

where f_{XTAL} is the crystal frequency, M is the PLL feedback-divider and N is the PLL post-divider. The input frequency and the selection of the feedback divider M is limited by the VCO-frequency range. f_{XTAL} and M must be configured to match the VCO frequency range of 800 to 1800 MHz in order to achieve stable PLL operation:

$$M_{MIN} = f_{VCO,MIN} \div (2 \cdot f_{XTAL}) \text{ and} \quad (3)$$

$$M_{MAX} = f_{VCO,MAX} \div (2 \cdot f_{XTAL}) \quad (4)$$

For instance, the use of a 16 MHz input frequency requires the configuration of the PLL feedback divider between $M = 25$ and $M = 56$. Table 8 shows the usable VCO frequency and M divider range for other example input frequencies.

Assuming that a 16 MHz input frequency is used, equation (2) reduces to:

$$f_{OUT} = 16 M \div N \quad (5)$$

Substituting N for the four available values for N (1, 2, 4, 8) yields:

Table 9. Output Frequency Range for $f_{XTAL} = 16$ MHz

N			F _{OUT}	F _{OUT} range	F _{OUT} step
1	0	Value			
0	0	2	8-M	200-450 MHz	8 MHz
0	1	4	4-M	100-225 MHz	4 MHz
1	0	8	2-M	50-112.5 MHz	2 MHz
1	1	1	16-M	400-900 MHz	16 MHz

Example calculation for an 16 MHz input frequency

For example, if an output frequency of 384 MHz was desired, the following steps would be taken to identify the appropriate M and N values. 384 MHz falls within the frequency range set by an N value of 2, so $N[1:0]=00$. For $N = 2$, $F_{OUT} = 8 \cdot M$ and $M = F_{OUT} \div 8$. Therefore, $M = 384 \div 8 = 48$, so $M[6:0] = 0110000$. Following this procedure a user can generate any whole frequency between 50 MHz and 900 MHz. The size of the programmable frequency steps will be equal to:

$$f_{STEP} = f_{XTAL} \div N \quad (6)$$

Using the parallel and serial interface

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the $\overline{P\_LOAD}$ signal such that a LOW to HIGH transition will latch the information present on the $M[6:0]$ and $N[1:0]$ inputs into the M and N counters. When the $\overline{P\_LOAD}$ signal is LOW the input latches will be transparent and any changes on the $M[6:0]$ and $N[1:0]$ inputs will affect the FOUT output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 12 bit shift register. Note that the $\overline{P\_LOAD}$ signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two, and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M6). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 4 illustrates the timing diagram for both a parallel and a serial load of the MPC9239 synthesizer.

$M[6:0]$ and $N[1:0]$ are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

Using the test and diagnosis output TEST

The TEST output provides visibility for one of the several internal nodes as determined by the $T[2:0]$ bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents FOUT, the LVCMOS output is not able to toggle fast enough for higher output frequencies and should only be used for test and diagnosis.

The T2, T1 and T0 control bits are preset to '000' when $\overline{P\_LOAD}$ is LOW so that the PECL FOUT outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MPC9239 itself. However, the PLL bypass mode may be of interest at the board level for functional debug. When $T[2:0]$ is set to 110 the MPC9239 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clocktree shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 200 MHz. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 100 MHz as the divide ratio of the Post-PLL divider is 2 (if $N = 1$). Note that the M counter output on the TEST output will not be a 50% duty cycle.

Table 10. Test and Debug Configuration for TEST

T[2:0]			TEST output
T2	T1	T0	
0	0	0	12-bit shift register out ^a
0	0	1	Logic 1
0	1	0	$f_{XTAL} \div 2$
0	1	1	M-Counter out
1	0	0	FOUT
1	0	1	Logic 0
1	1	0	M-Counter out in PLL-bypass mode
1	1	1	$FOUT \div 4$

a. Clocked out at the rate of S_CLOCK

Table 11. Debug Configuration for PLL bypass^a

Output	Configuration
FOUT	$S\_CLOCK \div N$
TEST	M-Counter out ^b

- a. T[2:0] = 110. AC specifications do not apply in PLL bypass mode
- b. Clocked out at the rate of $S\_CLOCK \div (2 \cdot N)$

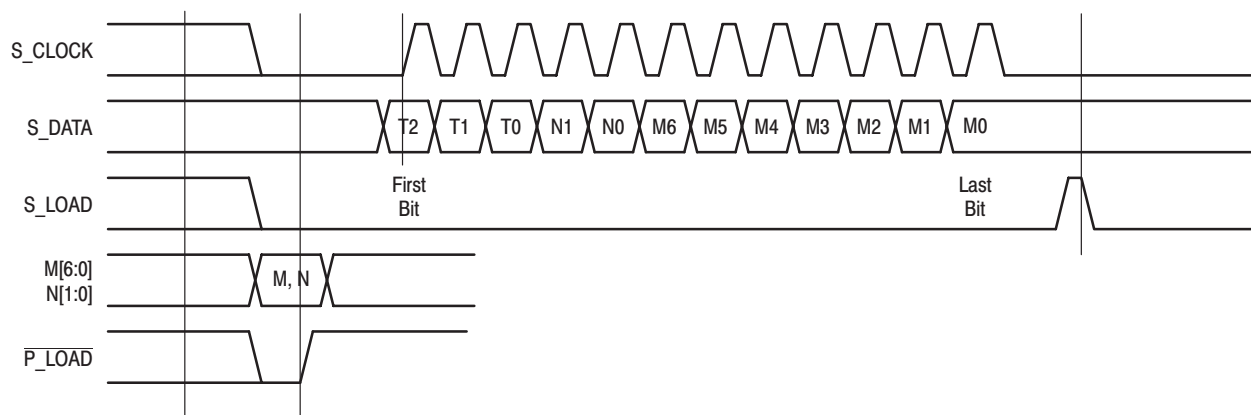


Figure 4. Serial Interface Timing Diagram

Power Supply Filtering

The MPC9239 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the VCC_PLL pin impacts the device characteristics. The MPC9239 provides separate power supplies for the digital circuitry (VCC) and the internal PLL (VCC_PLL) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCC_PLL pin for the MPC9239. Figure 5 illustrates a typical power supply filter scheme. The MPC9239 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the VCC supply and the MPC9239 pin of the MPC9239. From the data sheet, the VCC_PLL current (the current sourced through the VCC_PLL pin) is maximum 20 mA, assuming that a minimum of 2.835 V must be maintained on the VCC_PLL pin. The resistor shown in Figure 5 must have a resistance of 10-15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant

point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering. A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000 μ H choke will show a significant impedance at 10 kHz frequencies and above. Because of the current draw and the voltage that must be maintained on the VCC_PLL pin, a low DC resistance inductor is required (less than 15 Ω).

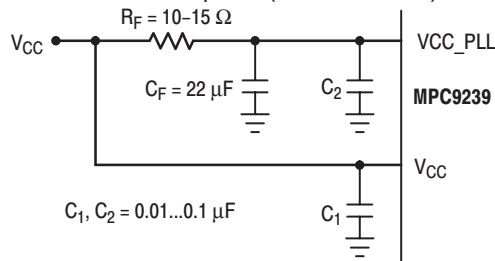


Figure 5. VCC_PLL Power Supply Filter

Layout Recommendations

The MPC9239 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 6 shows a representative board layout for the MPC9239. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure

6 is the low impedance connections between VCC and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the MPC9239 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors. Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator. Although the MPC9239 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

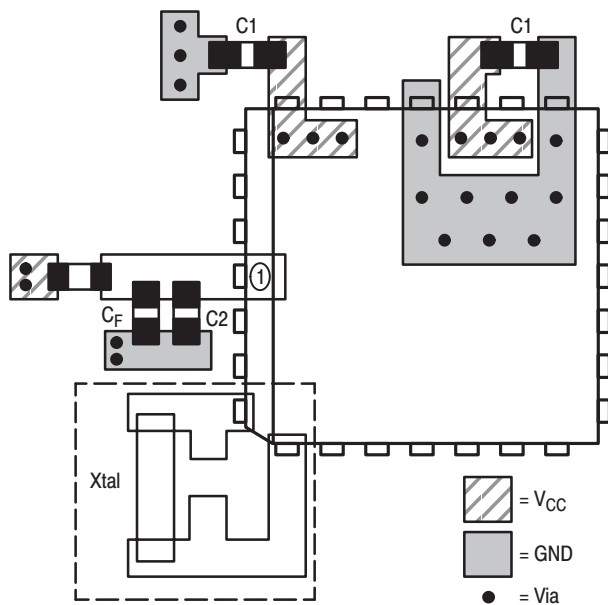


Figure 6. PCB Board Layout Recommendation for the PLCC28 Package

Using the On-Board Crystal Oscillator

The MPC9239 features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC9239 as possible to avoid any board level parasitics. To facilitate co-location surface mount crystals are recommended, but not required. Because the series resonant design is affected by capacitive loading on the xtal terminals loading variation introduced by crystals from different vendors could be a potential issue. For crystals with a higher shunt capacitance it may be required to place a resistance across the terminals to suppress the third harmonic. Although typically not required it is a good idea to layout the PCB with the provision of adding this external resistor. The resistor value will typically be between 500 and 1K Ω .

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately most crystals are characterized in a parallel resonant mode. Fortunately there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result a parallel resonant crystal can be used with the MPC9239 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application this level of inaccuracy is immaterial. Table 12 below specifies the performance requirements of the crystals to be used with the MPC9239.

Table 12. Recommended Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	± 75 ppm at 25°C
Frequency/Temperature Stability	± 150 ppm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80 Ω
Correlation Drive Level	100 μ W
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

Preliminary Information

900 MHz Low Voltage LVDS Clock Synthesizer

The MPC9259 is a 3.3V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking and computing applications. With output frequencies from 50 MHz to 900 MHz and the support of differential LVDS output signals the device meets the needs of the most demanding clock applications.

Features

- 50 MHz to 900 MHz synthesized clock output signal
- Differential LVDS output
- LVCMOS compatible control inputs
- On-chip crystal oscillator for reference frequency generation
- Alternative LVCMOS compatible reference input
- 3.3V power supply
- Fully integrated PLL
- Minimal frequency overshoot
- Serial 3-wire programming interface
- Parallel programming interface for power-up
- 32 Pin LQFP Package
- SiGe Technology
- Ambient temperature range 0°C to + 70°C

Functional Description

The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. The frequency of the internal crystal oscillator or external reference clock signal is multiplied by the PLL. The VCO within the PLL operates over a range of 800 to 1800 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The crystal oscillator frequency f_{XTAL} , the PLL feedback-divider M and the PLL post-divider N determine the output frequency.

The feedback path of the PLL is internal. The PLL adjusts the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve phase lock. The PLL will be stable if the VCO frequency is within the specified VCO frequency range (800 to 1800 MHz). The M-value must be programmed by the serial or parallel interface.

The PLL post-divider N is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[6:0] and N[1:0] inputs to configure the internal counters. It is recommended on system reset to hold the $\overline{P\_LOAD}$ input LOW until power becomes valid. On the LOW-to-HIGH transition of $\overline{P\_LOAD}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[6:0] and N[1:0] inputs prevent the LVCMOS compatible control inputs from floating. The serial interface centers on a twelve bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See the programming section for more information. The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. In order to minimize the PLL jitter, it is recommended to avoid active signal on the TEST output. The PWR_DOWN pin, when asserted, will synchronously divide the FOUT by 16. The power down sequence is clocked by the PLL reference clock, thereby causing the frequency reduction to happen relatively slowly. Upon de-assertion of the PWR_DOWN pin, the FOUT input will step back up to its programmed frequency in four discrete increments.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MPC9259

**900 MHZ LOW VOLTAGE
CLOCK SYNTHESIZER**



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A

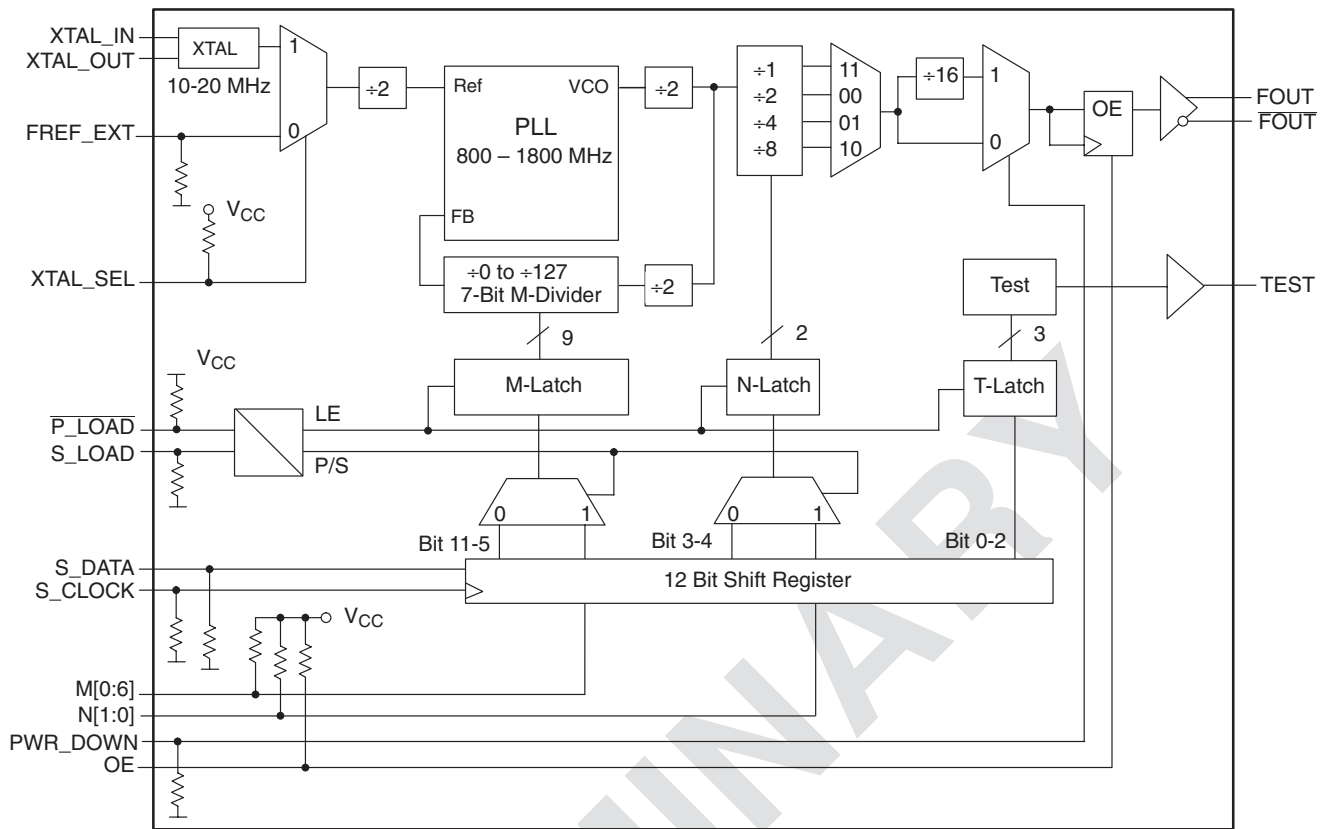


Figure 1. MPC9259 Logic Diagram

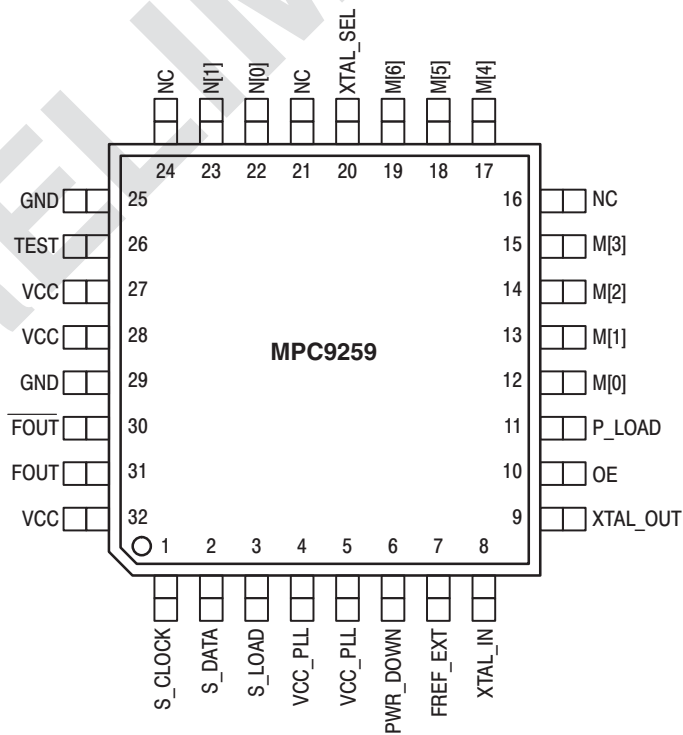
Figure 2. MPC9259 32-Lead LQFP Pinout
(Top View)

Table 1. Pin Configuration

Pin	I/O	Default	Type	Function
XTAL_IN, XTAL_OUT			Analog	Crystal oscillator interface
FREF_EXT	Input	0	LVC MOS	Alternative PLL reference input
FOUT, FOUT	Output		LVDS	Differential clock output
TEST	Output		LVC MOS	Test and device diagnosis output
XTAL_SEL	Input	1	LVC MOS	PLL reference select input
PWR_DOWN	Input	0	LVC MOS	Configuration input for power down mode. Assertion (deassertion) of power down will decrease (increase) the output frequency by a ratio of 16 in 4 discrete steps. PWR_DOWN assertion (deassertion) is synchronous to the input reference clock.
S_LOAD	Input	0	LVC MOS	Serial configuration control input. This inputs controls the loading of the configuration latches with the contents of the shift register. The latches will be transparent when this signal is high, thus the data must be stable on the high-to-low transition.
P_LOAD	Input	1	LVC MOS	Parallel configuration control input. this input controls the loading of the configuration latches with the content of the parallel inputs (M and N). The latches will be transparent when this signal is low, thus the parallel data must be stable on the low-to-high transition of P_LOAD. P_LOAD is state sensitive.
S_DATA	Input	0	LVC MOS	Serial configuration data input.
S_CLOCK	Input	0	LVC MOS	Serial configuration clock input.
M[0:6]	Input	1	LVC MOS	Parallel configuration for PLL feedback divider (M). M is sampled on the low-to-high transition of P_LOAD.
N[1:0]	Input	1	LVC MOS	Parallel configuration for Post-PLL divider (N). N is sampled on the low-to-high transition of P_LOAD
OE	Input	1	LVC MOS	Output enable (active high) The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the FOUT output. OE = L low stops FOUT in the logic low state (FOUT = L, FOUT = H).
GND	Supply		Ground	Negative power supply (GND).
V _{CC}	Supply		V _{CC}	Positive power supply for I/O and core. All V _{CC} pins must be connected to the positive power supply for correct operation.
V _{CC} _PLL	Supply		V _{CC}	PLL positive power supply (analog power supply).

Table 2. Output frequency range and PLL Post-divider N

PWR_DOWN	N		VCO Output frequency division	FOUT frequency range
	1	0		
0	0	0	2	200 - 450 MHz
0	0	1	4	100 - 225 MHz
0	1	0	8	50 - 112.5 MHz
0	1	1	1	400 - 900 MHz
1	0	0	32	12.5 - 28.125 MHz
1	0	1	64	6.25 - 14.0625 MHz
1	1	0	128	3.125 - 7.03125 MHz
1	1	1	16	25 - 56.25 MHz

Table 3. Function Table

Input	0	1
XTAL_SEL	FREF_EXT	XTAL interface
OE	Outputs disabled. FOUT is stopped in the logic low state (FOUT = L, $\overline{\text{FOUT}} = \text{H}$)	Outputs enabled
PWR_DOWN	Output divider $\div 1$	Output divider $\div 16$

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
MM	ESD protection (Machine model)	200			V	
HBM	ESD protection (Human body model)	2000			V	
LU	Latch-up immunity	200			mA	
C _{IN}	Input capacitance		4.0		pF	Inputs

Table 5. Absolute Maximum Ratings^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	3.9	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} + 0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} + 0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage temperature	-65	125	°C	

^a Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. DC Characteristics ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS control inputs (FREF_EXT, PWR_DOWN, XTAL_SEL, P_LOAD, S_LOAD, S_DATA, S_CLOCK, M[0:6], N[0:1], OE)						
V_{IH}	Input high voltage	2.0		$V_{CC} + 0.3$	V	LVCMOS
V_{IL}	Input low voltage			0.8	V	LVCMOS
I_{IN}	Input Current ^b			± 200	μA	$V_{IN} = V_{CC}$ or GND
Differential clock output FOUT						
V_{PP}	Output Differential Voltage (peak-to-peak)	250			mV	LVDS
V_{OS}	Output Offset Voltage	1125		1275	mV	LVDS
Test and diagnosis output TEST						
V_{OH}	Output High Voltage	2.0			V	$I_{OH} = -0.8\text{ mA}$
V_{OL}	Output Low Voltage			0.55	V	$I_{OL} = 0.8\text{ mA}$
Supply current						
I_{CC_PLL}	Maximum PLL Supply Current			20	mA	V_{CC_PLL} Pins
I_{CC}	Maximum Supply Current			110	mA	All V_{CC} Pins

- a. All AC characteristics are design targets and subject to change upon device characterization.
b. Inputs have pull-down resistors affecting the input current.

Table 7. AC Characteristics ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{XTAL}	Crystal interface frequency range	10		20	MHz	
f_{VCO}	VCO frequency range ^b	800		1800	MHz	
f_{MAX}	Output Frequency N = 11 (+1) N = 00 (+2) N = 01 (+4) N = 10 (+8)	400 200 100 50		900 450 225 112.5	MHz MHz MHz MHz	PWR_DOWN = 0
f_{S_CLOCK}	Serial interface programming clock frequency ^c	0		10	MHz	
$t_{p,MIN}$	Minimum pulse width (S_LOAD, P_LOAD)	50			ns	
DC	Output duty cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.05		TBD	ns	20% to 80%
t_S	Setup Time S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to P_LOAD	20 20 20			ns ns ns	
t_S	Hold Time S_DATA to S_CLOCK M, N to P_LOAD	20 20			ns ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter RMS (1 σ) ^d		TBD	TBD	ps	
$t_{JIT(PER)}$	Period Jitter RMS (1 σ)			± 25	ps	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

- a. All AC characteristics are design targets and subject to change upon device characterization.
b. The input frequency f_{XTAL} and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \cdot 2 \cdot M$.
c. The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. See application section for more details.
d. See application section for a jitter calculation for other confidence factors than 1 σ .

Table 8. MPC9259 Frequency Operating Range (in MHz)

M	M[6:0]	VCO frequency for an crystal interface frequency of						Output frequency for $f_{XTAL}=16\text{ MHz}$ and for $N =$			
		10 MHz	12 MHz	14 MHz	16 MHz	18 MHz	20 MHz	1	2	4	8
20	0010100						800				
21	0010101						840				
22	0010110						880				
23	0010111					828	920				
24	0011000					864	960				
25	0011001				800	900	1000	400	200	100	50
26	0011010				832	936	1040	416	208	104	52
27	0011011				864	972	1080	432	216	108	54
28	0011100			812	896	1008	1120	448	224	112	56
29	0011101			840	928	1044	1160	464	232	116	58
30	0011110			875	960	1080	1200	480	240	120	60
31	0011111			868	992	1116	1240	496	248	124	62
32	0100000			896	1024	1152	1280	512	256	128	64
33	0100001			924	1056	1188	1320	528	264	132	66
34	0100010		816	952	1088	1224	1360	544	272	136	68
35	0100011		840	980	1120	1260	1400	560	280	140	70
36	0100100		864	1008	1152	1296	1440	576	288	144	72
37	0100101		888	1036	1184	1332	1480	592	296	148	74
38	0100110		912	1064	1216	1368	1520	608	304	152	76
39	0100111		936	1092	1248	1404	1560	624	312	156	78
40	0101000	800	960	1120	1280	1440	1600	640	320	160	80
41	0101001	820	984	1148	1312	1476	1640	656	328	164	82
42	0101010	840	1008	1176	1344	1512	1680	672	336	168	84
43	0101011	860	1032	1204	1376	1548	1720	688	344	172	86
44	0101100	880	1056	1232	1408	1584	1760	704	352	176	88
45	0101101	900	1080	1260	1440	1620	1800	720	360	180	90
46	0101110	920	1104	1288	1472	1656		736	368	184	92
47	0101111	940	1128	1316	1504	1692		752	376	188	94
48	0110000	960	1152	1344	1536	1728		768	384	192	96
49	0110001	980	1176	1372	1568	1764		784	392	196	98
50	0110010	1000	1200	1400	1600	1800		800	400	200	100
51	0110011	1020	1224	1428	1632			816	408	204	102
52	0110100	1040	1248	1456	1664			832	416	208	104
53	0110101	1060	1272	1484	1696			848	424	212	106
54	0110110	1080	1296	1512	1728			864	432	216	108
55	0110111	1100	1320	1540	1760			880	440	220	110
56	0111000	1120	1344	1568	1792			896	448	224	112
57	0111001	1140	1368	1596							
58	0111010	1160	1392	1624							
59	0111011	1180	1416	1652							
60	0111100	1200	1440	1680							
61	0111101	1220	1488	1736							
62	0111110	1260	1512	1764							
63	0111111	1260	1512	1764							
64	1000000	1280	1536	1792							
...		...	...	...							

Programming the MPC9259

Programming the MPC9259 amounts to properly configuring the internal PLL dividers to produce the desired synthesized frequency at the output. The output frequency can be represented by this formula:

$$f_{OUT} = (f_{XTAL} \div 2) \cdot (M \cdot 4) \div (N \cdot 2) \text{ or} \quad (1)$$

$$f_{OUT} = f_{XTAL} \cdot M \div N \quad (2)$$

where f_{XTAL} is the crystal frequency, M is the PLL feedback-divider and N is the PLL post-divider. The input frequency and the selection of the feedback divider M is limited by the VCO-frequency range. f_{XTAL} and M must be configured to match the VCO frequency range of 800 to 1800 MHz in order to achieve stable PLL operation:

$$M_{MIN} = f_{VCO,MIN} \div (2 \cdot f_{XTAL}) \text{ and} \quad (3)$$

$$M_{MAX} = f_{VCO,MAX} \div (2 \cdot f_{XTAL}) \quad (4)$$

For instance, the use of a 16 MHz input frequency requires the configuration of the PLL feedback divider between $M = 25$ and $M = 56$. Table 8 shows the usable VCO frequency and M divider range for example input frequencies.

Assuming that a 16 MHz input frequency is used, equation (2) reduces to:

$$f_{OUT} = 16 M \div N \quad (5)$$

Substituting N for the four available values for N (1, 2, 4, 8) yields:

Table 9. Output Frequency Range for $f_{XTAL} = 16$ MHz

N			F _{OUT}	F _{OUT} range	F _{OUT} step
1	0	Value			
0	0	2	8-M	200-450 MHz	8 MHz
0	1	4	4-M	100-225 MHz	4 MHz
1	0	8	2-M	50-112.5 MHz	2 MHz
1	1	1	16-M	400-900 MHz	16 MHz

Example calculation for an 16 MHz input frequency

For example, if an output frequency of 384 MHz was desired, the following steps would be taken to identify the appropriate M and N values. 384 MHz falls within the frequency range set by an N value of 2, so $N[1:0]=00$. For $N = 2$, $F_{OUT} = 8 \cdot M$ and $M = F_{OUT} \div 8$. Therefore, $M = 384 \div 8 = 48$, so $M[6:0] = 0110000$. Following this procedure a user can generate any whole frequency between 50 MHz and 900 MHz. The size of the programmable frequency steps will be equal to:

$$f_{STEP} = f_{XTAL} \div N \quad (6)$$

Using the parallel and serial interface

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the $\overline{P\_LOAD}$ signal such that a LOW to HIGH transition will latch the information present on the $M[6:0]$ and $N[1:0]$ inputs into the M and N counters. When the $\overline{P\_LOAD}$ signal is LOW the input latches will be transparent and any changes on the $M[6:0]$ and $N[1:0]$ inputs will affect the FOUT output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 12 bit shift register. Note that the $\overline{P\_LOAD}$ signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two, and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M6). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 3 illustrates the timing diagram for both a parallel and a serial load of the MPC9259 synthesizer.

$M[6:0]$ and $N[1:0]$ are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

Using the test and diagnosis output TEST

The TEST output provides visibility for one of the several internal nodes as determined by the $T[2:0]$ bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents FOUT, the LVCMOS output is not able to toggle fast enough for higher output frequencies and should only be used for test and diagnosis.

The T2, T1 and T0 control bits are preset to '000' when $\overline{P\_LOAD}$ is LOW so that the PECL FOUT outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MPC9259 itself. However, the PLL bypass mode may be of interest at the board level for functional debug. When $T[2:0]$ is set to 110 the MPC9259 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clocktree shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 200 MHz. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 100 MHz as the divide ratio of the Post-PLL divider is 2 (if $N = 1$). Note that the M counter output on the TEST output will not be a 50% duty cycle.

Table 10. Test and Debug Configuration for TEST

T[2:0]			TEST output
T2	T1	T0	
0	0	0	12-bit shift register out ^a
0	0	1	Logic 1
0	1	0	$f_{XTAL} \div 2$
0	1	1	M-Counter out
1	0	0	FOUT
1	0	1	Logic 0
1	1	0	M-Counter out in PLL-bypass mode
1	1	1	$FOUT \div 4$

a. Clocked out at the rate of S_CLOCK

Table 11. Debug Configuration for PLL bypass^a

Output	Configuration
FOUT	$S\_CLOCK \div N$
TEST	M-Counter out ^b

- a. T[2:0] = 110. AC specifications do not apply in PLL bypass mode
b. Clocked out at the rate of $S\_CLOCK \div (2 \cdot N)$

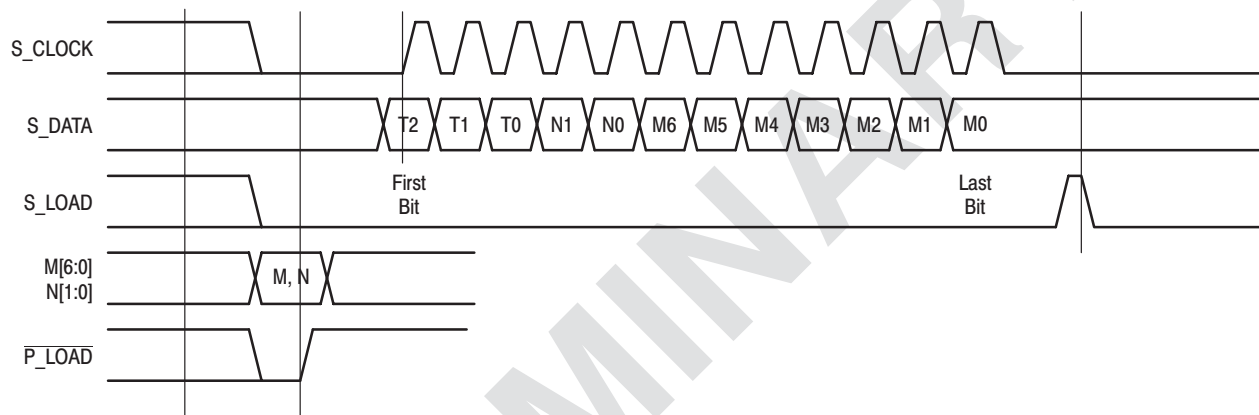


Figure 3. Serial Interface Timing Diagram

Power Supply Filtering

The MPC9259 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC9259 provides separate power supplies for the digital circuitry (VCC) and the internal PLL (VCC_PLL) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCC_PLL pin for the MPC9259. Figure 4 illustrates a typical power supply filter scheme. The MPC9259 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the VCC supply and the MPC9259 pin of the MPC9259. From the data sheet, the VCC_PLL current (the current sourced through the VCC_PLL pin) is typically TBD mA (TBD maximum), assuming that a minimum of 3.135V must be maintained on the VCC_PLL pin, very little DC voltage drop can be tolerated when a 3.3V VCC supply is used. The resistor shown in Figure 4 must have

a resistance of TBD Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering. A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000 μ H choke will show a significant impedance at 10 kHz frequencies and above. Because of the current draw and the voltage that must be maintained on the VCC_PLL pin, a low DC resistance inductor is required (less than TBD Ω).

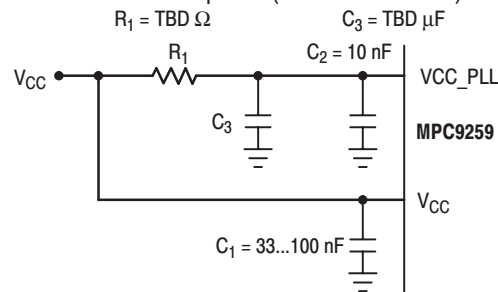


Figure 4. VCC_PLL Power Supply Filter

Product Preview Networking Clock Source

The MPC926508 is a low cost, low jitter, high performance clock synthesizer for networking applications. Using analog Phase-Locked Loop (PLL) techniques, the device accepts an input to produce multiple output clocks for networking chips, PCI devices, SDRAM, and ASICs. The MPC926508 outputs all have 0 ppm synthesis error.

Features

- Packaged in 20 pin narrow (150 mil) SSOP (QSOP)
- 25 or 125 MHz fundamental clock input or 25 MHz crystal input
- Two output clocks
- SDRAM frequencies of 100 and 133 MHz
- Zero ppm synthesis error in all clocks
- Full CMOS output swing with 25 mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- 3.3V operating voltage

MPC926508

NETWORKING CLOCK SOURCE



SD SUFFIX
20 LEAD SSOP
CASE 1461

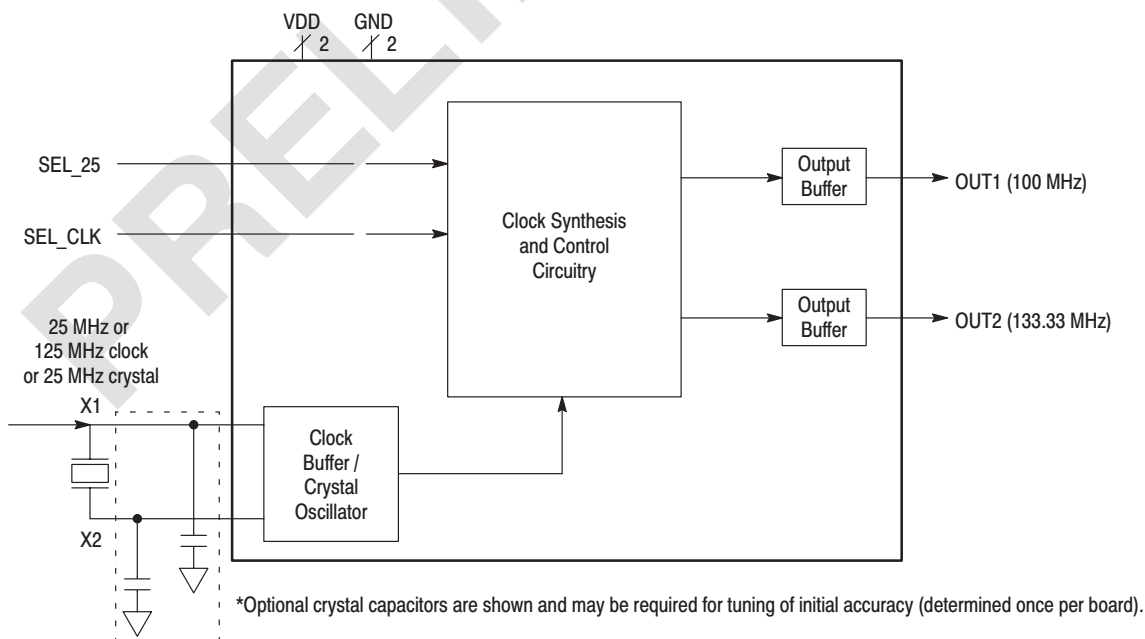


Figure 1. MPC926508 Block Diagram

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Table 1: FUNCTION TABLE

Control	Default	0	1
SEL_25	1	125	25
SEL_CLK	1	XTAL	REF_CLK

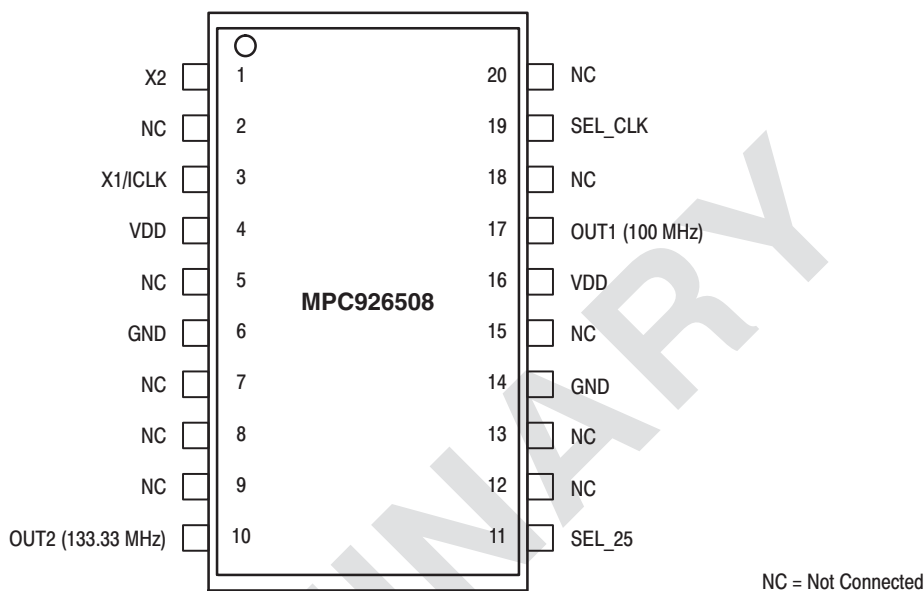


Figure 2. MPC926508 Pin Assignment

Table 2: PIN DESCRIPTION

Number	Name	Type	Description
1	X2	XO	Crystal connection. Connect to a crystal or leave unconnected for a clock input.
2	NC	—	Not Connected
3	X1/CLK	XI	Crystal connection. Connect to a fundamental crystal or clock input.
4	VDD	P	Connect to +3.3 V. Must be same as other VDD.
5	NC	—	Not Connected
6	GND	P	Connect to ground.
7	NC	—	Not Connected
8	NC	—	Not Connected
9	NC	—	Not Connected
10	OUT1 (133.33 MHz)	O	133.33 MHz Output
11	SEL_25	I	REF_CLK or XTAL Input Selection.
12	NC	—	Not Connected
13	NC	—	Not Connected
14	GND	P	Connect to ground.
15	NC	—	Not Connected
16	VDD	P	Connect to +3.3 V. Must be same as other VDD.
17	OUT2 (100 MHz)	O	100 MHz Output
18	NC	—	Not Connected
19	SEL_CLK	I	25 or 125 MHz REF_CLK Selection.
20	NC	—	Not Connected

Key: XI, XO = crystal connections; I = Input with internal pull-up resistor; O = Output; P = power supply connection.

Table 3: ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{DD}	Supply Voltage			4.5	V	Referenced to GND
	Inputs and Clock Outputs	−0.5		V _{DD} + 0.5	V	Referenced to GND
T _A	Ambient Operating Temperature	0		70	°C	
T _A	Ambient Operating Temperature, I version	−40		85	°C	Industrial temp
T _{SOL}	Soldering Temperature			260	°C	Max of 20 seconds
T _S	Storage Temperature	−65		150	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4: DC CHARACTERISTICS (V_{DD} = 3.3V ± 10%, T_A = −40°C to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{IH}	Input High Voltage X1 pin only all I type inputs	V _{DD} /2+1 2	V _{DD} /2		V V	
V _{IL}	Input Low Voltage X1 pin only all I type inputs		V _{DD} /2	V _{DD} /2−1 0.8	V V	
V _{OH}	Output High Voltage	2.4			V	I _{OH} = −25 mA
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 25 mA
V _{OH}	Output High Voltage, CMOS level	V _{DD} − 0.4			V	I _{OH} = −8 mA
I _{DD}	Operating Supply Current		35		mA	No Load
	Short Circuit Current		90		mA	Each Output
	Internal Pull-Up Resistor		200		kΩ	SEL_25, SEL_CLK

Table 5: AC CHARACTERISTICS (V_{DD} = 3.3V ± 10%, T_A = −40°C to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f _{REF}	Input Frequency	12	25	27	MHz	Crystal Oscillator
f _{REF}	Input Frequency		125		MHz	External Input
t _r	Output Clock Rise Time		1		ns	0.8 to 2.0V
t _f	Output Clock Fall Time		1		ns	2.0 to 0.8V
DCO	Output Clock Duty Cycle	40	50	60	%	At V _{DD} /2
	Frequency Error			0	ppm	All clocks
t _{JIT(CC)}	Jitter (Cycle-to-Cycle)		300		ps	Variation from mean

APPLICATIONS INFORMATION

External Components

The MPC926508 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01μF should be connected between each VDD and GND (pins 4 and 6, pins 16 and 14), as close to the MPC926508 as possible. A series termination resistor of 33 Ω may be used for each clock output. The crystal must be connected as close to

the chip as possible. The crystal should be a fundamental mode (do not use third overtone), parallel resonant. Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation, where C_L is the crystal load capacitance: Crystal caps (pF) = (C_L − 6) × 2. So for a crystal with 16 pF load capacitance, two 20 pF caps should be used.

Product Preview

HSTL Low Voltage Differential Clock

The MPC998 is a low voltage 3.3V, HSTL differential clock synthesizer. The clock is designed to support single and multiple processor systems requiring HSTL differential inputs. The MPC998 supports two differential HSTL output pairs that may be operated from 520 MHz to 840 MHz.

Features:

- 2 clock outputs: (PCLK0 and PCLK1), each fully selectable
- Fully integrated PLL
- Output frequencies from 520 MHz to 840 MHz
- HSTL outputs
- HSTL and LVPECL reference clocks
- 32 lead LQFP packaging

The fully integrated Phase Locked Loop multiplies the HSTL_CLK input or the PECL_CLK input frequency to the desired processor clock frequency.

The PLL may be bypassed for test purposes such that the PCLK outputs are fed directly from the HSTL_CLK or PECL_CLK input.

All outputs are HSTL. The PCLK outputs are capable of driving 25Ω to ground with at least 600mV p-p signals. The EXTFB_OUT is capable of driving 50Ω ground with at least a 600 mV p-p signal. For on-chip power reduction, the outputs are powered from 1.8V external supply. For zero delay applications the buffer can operate with either external or internal feedback.

MPC998

**HSTL LOW VOLTAGE
DIFFERENTIAL CLOCK
SYNTHESIZER FOR
520 – 840 MHZ**



FA SUFFIX
LQFP PACKAGE
CASE 873A

4

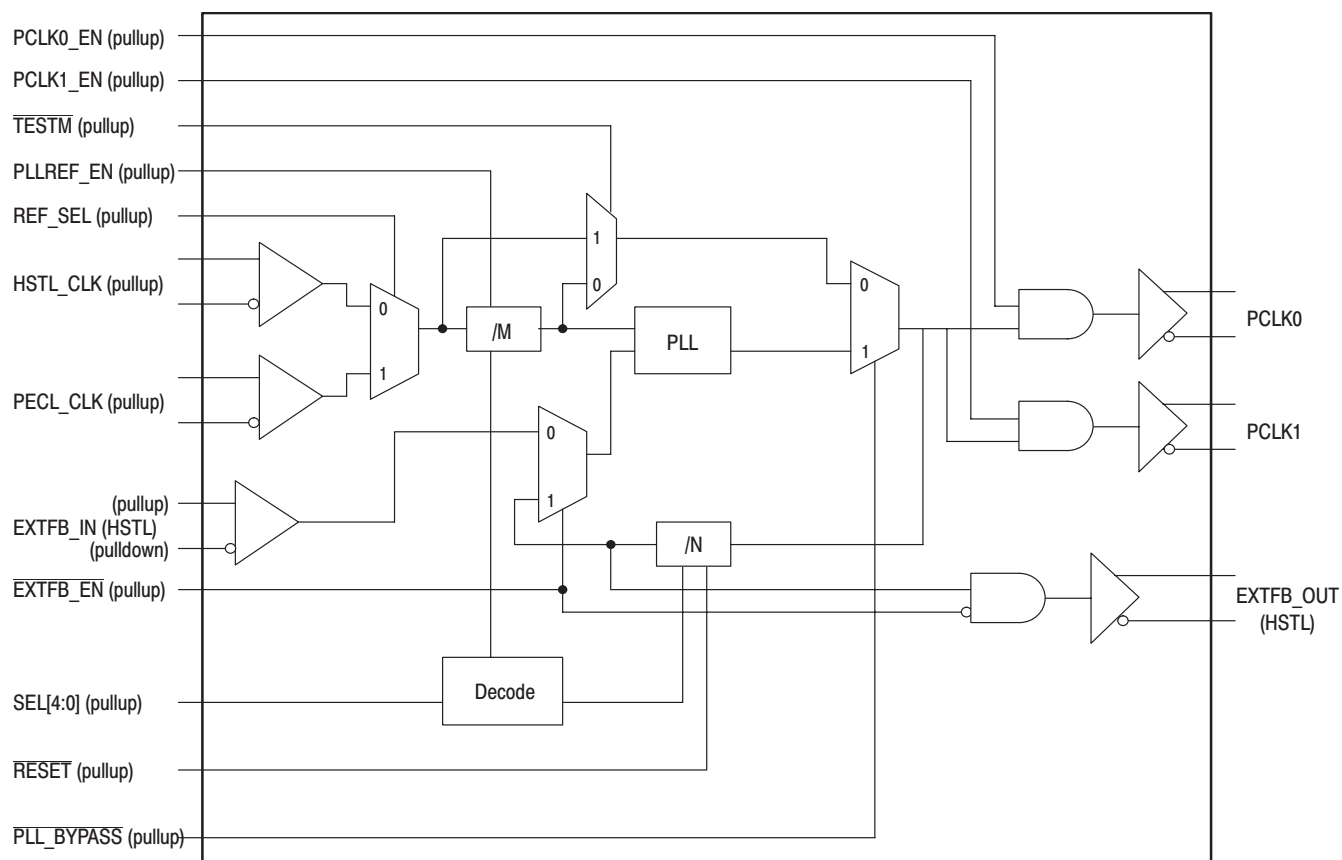


Figure 1. MPC998 Logic Diagram

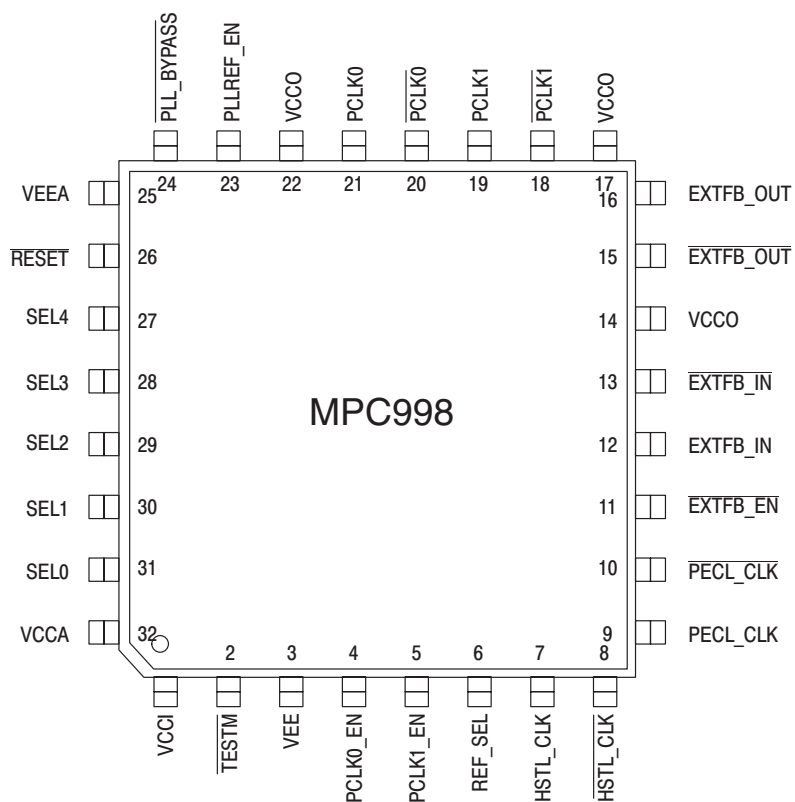


Figure 2. 32 Lead Package Pinout (Top View)

PIN CONFIGURATION

Pin #	Pin	I/O Type	Type	Description
1	VCCI	Power	Power Supply	3.3 V
2	TESTM	Input	LVC MOS	M divider test pins
3	VEE	Power (GND)	Ground	Digital GND
4	PCLK0_EN	Input	LVC MOS	PCLK0 enable
5	PCLK1_EN	Input	LVC MOS	PCLK1 enable
6	REF_SEL	Input	LVC MOS	Selects the PLL input reference clock
7	HSTL_CLK	Input	Differential HSTL	PLL reference clock input
8	HSTL_CLK	Input	Differential HSTL	PLL reference clock input
9	PECL_CLK	Input	Differential LVPECL	PLL reference clock input
10	PECL_CLK	Input	Differential LVPECL	PLL reference clock input
11	EXTFB_EN	Input	LVC MOS	External feedback enable
12	EXTFB_IN	Input	Differential HSTL	External feedback input
13	EXTFB_IN	Input	Differential HSTL	External feedback input
14	VCCO	Power	Power Supply	Output buffers power supply
15	EXTFB_OUT	Output	Differential HSTL	External feedback output clock
16	EXTFB_OUT	Output	Differential HSTL	External feedback output clock
17	VCCO	Power	Power Supply	Output buffers power supply
18	PCLK1	Output	Differential HSTL	Output clock 1
19	PCLK1	Output	Differential HSTL	Output clock 1
20	PCLK0	Output	Differential HSTL	Output clock 0
21	PCLK0	Output	Differential HSTL	Output clock 0
22	VCCO	Power	Power Supply	Output buffers power supply
23	PLLREF_EN	Input	LVC MOS	PLL reference enable
24	PLL_BYPASS	Input	LVC MOS	Input signal PLL bypass
25	VEEA	Power (GND)	Ground	Analog GND for PLL
26	RESET	Input	LVC MOS	PLL bypass reset (for test use)
27	SEL[4]	Input	LVC MOS	Selection of input and feedback frequency
28	SEL[3]	Input	LVC MOS	Selection of input and feedback frequency
29	SEL[2]	Input	LVC MOS	Selection of input and feedback frequency
30	SEL[1]	Input	LVC MOS	Selection of input and feedback frequency
31	SEL[0]	Input	LVC MOS	Selection of input and feedback frequency
32	VCCA	Power	Power Supply	3.3 V filtered for PLL (PLL power supply)

FREQUENCY SELECTION TABLE

SEL					Input Divide	Feedback Divide
4	3	2	1	0	M	N
0	0	0	0	0	5	24
0	0	0	0	1	5	25
0	0	0	1	0	5	26
0	0	0	1	1	5	27
0	0	1	0	0	5	28
0	0	1	0	1	5	29
0	0	1	1	0	5	30
0	0	1	1	1	5	31
0	1	0	0	0	5	32
0	1	0	0	1	5	33
0	1	0	1	0	5	34
0	1	0	1	1	5	35
0	1	1	0	0	5	36
0	1	1	0	1	5	37
0	1	1	1	0	5	38
0	1	1	1	1	5	39
1	0	0	0	0	5	40
1	0	0	0	1	5	41
1	0	0	1	0	5	42
1	0	0	1	1	5	43
1	0	1	0	0	5	44
1	0	1	0	1	5	45
1	0	1	1	0	5	46
1	0	1	1	1	5	47
1	1	0	0	0	5	48
1	1	0	0	1	5	49
1	1	0	1	0	5	50
1	1	0	1	1	5	51
1	1	1	0	0	5	52
1	1	1	0	1	5	53
1	1	1	1	0	5	54
1	1	1	1	1	5	55

FUNCTION TABLE (CONTROLS)

Control Pin	0	1
REF_SEL	HSTL_CLK	PECL_CLK
TESTM	M divider test mode enabled	Reference fed to Bypass mux
PLLREF_EN	Disable the input to the PLL and reset the M divider	Enable the input to the PLL
PLL_BYPASS	Outputs fed by input reference or M divider	Outputs fed by VCO
EXTFB_EN	External feedback enabled	Internal feedback enabled
PCLK0_EN	PCLK0 = low, $\overline{\text{PCLK0}}$ = high	PCLK0 = high, $\overline{\text{PCLK0}}$ = low
PCLK1_EN	PCLK1 = low, $\overline{\text{PCLK1}}$ = high	PCLK1 = high, $\overline{\text{PCLK1}}$ = low
RESET	Resets feedback N divider	Feedback enabled
SEL[4:0]	See Selection Frequency Table	

ABSOLUTE MAXIMUM RATINGS*

Symbol	Characteristics	Min	Max	Unit	Condition
VCC	Supply Voltage	-0.5	4.4	V	
VCCO	Output Supply Voltage	-0.5	4.4	V	
VIN	Input Voltage	-0.5	VCC+0.3	V	
IIN	Input Current	-1	1	mA	
TS	Storage temperature	-50	150	°C	

4

NOTE: Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC CHARACTERISTICS ($V_{CCA}=V_{CCI} = 3.3V \pm 5\%$, $V_{CCO} = 1.7$ to $2.1V$, $T_A = 0$ to 70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
VIH	Input high voltage	2.0		VCCI	V	LVC MOS
VIL	Input low voltage	0.0		0.8	V	LVC MOS
VCMR	Input high voltage ^a	1		VCCI - 0.3	V	LVPECL
VPP	Input low voltage ^a	0.5		1	V	LVPECL ^b
V _{IN} (dc)	DC input signal voltage	-0.3		1.45	V	HSTL ^c
V _{DIF} (dc)	DC differential input voltage	0.4		1.75	V	HSTL ^d
V _{CM} (dc)	DC common mode input voltage	0.4		1.0	V	HSTL ^e
VOH	Output High Voltage	V _X + 0.3	V _X + 0.5	1.4	V	HSTL ^{f,a}
VOL	Output Low Voltage	0.0	V _X - 0.5	V _X - 0.3	V	HSTL ^f
ICCI	Core Supply Current			140	mA	
ICCA	PLL Supply Current		15	20	mA	
ICCO	Output Supply Current		150		mA	Note ^g
Theta _{JA}	Junction to ambient thermal resistance		53		°C/W	Note ^h

a) DC levels will vary 1:1 with VCC.

b) VPP minimum and maximum required to maintain AC specifications. Actual device function will tolerate minimum VPP of 200mV.

c) V_{IN} (dc) specifies the maximum allowable dc excursion of each differential input.

d) V_{DIF} (dc) specifies the minimum input differential voltage ($V_{TR} - V_{CP}$) required for switching, where V_{TR} is the "true" input signal and V_{CP} is the "complement" input signal.

e) V_{CM}(dc) specifies the maximum allowable range of input signal crosspoint voltage

f) V_X is the differential output crosspoint voltage defined in the "AC CHARACTERISTICS" section

g) 2 PCLK into 25Ω and 1 EXTFB into 50Ω

h) Measured with 1.3M/s (250fpm) airflow

AC CHARACTERISTICS ($V_{CCA} = V_{CCI} = 3.3V \pm 5\%$, $V_{CCO} = 1.7V$ to $2.1V$, $T_A = 0$ to $70^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
fref	Input Frequency		100 - 125		MHz	
fMAX	Maximum Output Frequency	520		840	MHz	Note ^b
tsk(o)	Skew Error (PCLK)			35	ps	Note ^c
tjit(0)	Phase jitter (IO jitter)			output period / 2		Note ^c
tjit(cc)	Cycle-to-cycle jitter (full period)			5%		Note ^{c, e}
tjit(1/2per)	Cycle-to-cycle jitter (half period)			6%		Note ^{c, d}
V _{DIFout}	Differential Output pk-pk swing	0.6			V	For all HSTL output pairs
V _x	Differential output crosspoint voltage	0.68		0.9	V	For all HSTL output pairs
t _{lock}	Maximum PLL lock time			10	ms	

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- a) All PCLK outputs are terminated in 25Ω to ground, EXTFB_OUT is terminated in 50Ω to ground (applies to all measurements).
b) With PLL active but in bypass mode, fref Max is limited by input buffer; best performance is expected with PECL input.
c) Measured at differential pair crossover.
d) Reference to half PCLK period.
e) Reference to full PCLK period.

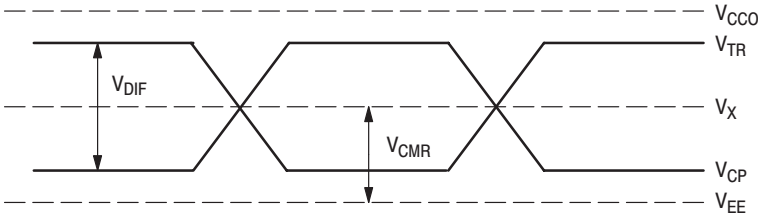


Figure 3. HSTL Differential Input Levels

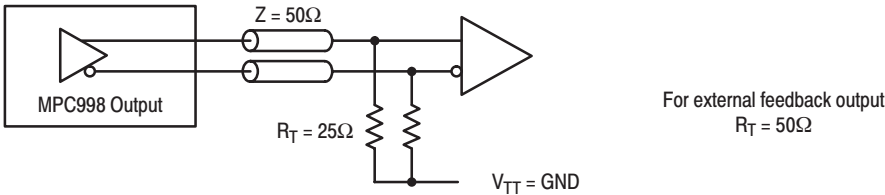


Figure 4. Output Termination and AC Test Reference

APPLICATIONS INFORMATION

Power Supply Filtering

The MPC998 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC998 provides separate power supplies for the output buffers (V_{CCO}) and the phase-locked loop (V_{CCA}) of the device.

The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC998. Figure 5 illustrates a typical power supply filter scheme. The MPC998 is most susceptible to noise with spectral content in the 10kHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the MPC998. From the data sheet the $I_{V_{CCA}}$ current (the current sourced through the V_{CCA} pin) is typically 15 mA (20 mA maximum), assuming that a minimum of 3.3V–5% must be maintained on the V_{CCA} pin. Very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 5 “Power Supply Filter” must have a resistance of 5-15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise

whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8-10 Ω resistor to avoid potential V_{CC} drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

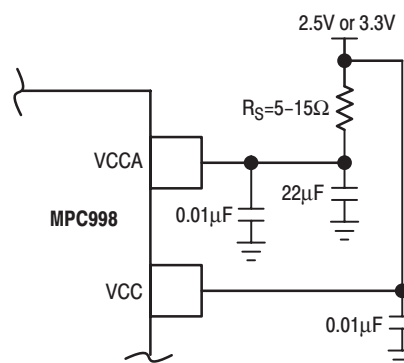


Figure 5. Power Supply Filter

Although the MPC998 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Product Preview

HSTL Low Voltage Differential Clock

The MPC9994 is a low voltage 3.3V, HSTL differential clock synthesizer. The clock is designed to support single and multiple processor systems requiring HSTL differential inputs. The MPC9994 supports two differential HSTL output pairs that may be operated from 340 MHz to 640 MHz.

Features:

- 2 clock outputs: (PCLK0 and PCLK1), each fully selectable
- Fully integrated PLL
- Output frequencies from 340 MHz to 640 MHz
- HSTL outputs
- HSTL and LVPECL reference clocks
- 32 lead LQFP packaging

The fully integrated Phase Locked Loop multiplies the HSTL_CLK input or the PECL_CLK input frequency to the desired processor clock frequency.

The PLL may be bypassed for test purposes such that the PCLK outputs are fed directly from the HSTL_CLK or PECL_CLK input.

All outputs are HSTL. The PCLK outputs are capable of driving 25Ω to ground with at least 600mV p-p signals. The EXTFB_OUT is capable of driving 50Ω ground with at least a 600 mV p-p signal. For on-chip power reduction, the outputs are powered from 1.8V external supply. For zero delay applications the buffer can operate with either external or internal feedback.

MPC9994

**HSTL LOW VOLTAGE
DIFFERENTIAL CLOCK
SYNTHESIZER FOR
340 – 640 MHZ**



**FA SUFFIX
LQFP PACKAGE
CASE 873A**

4

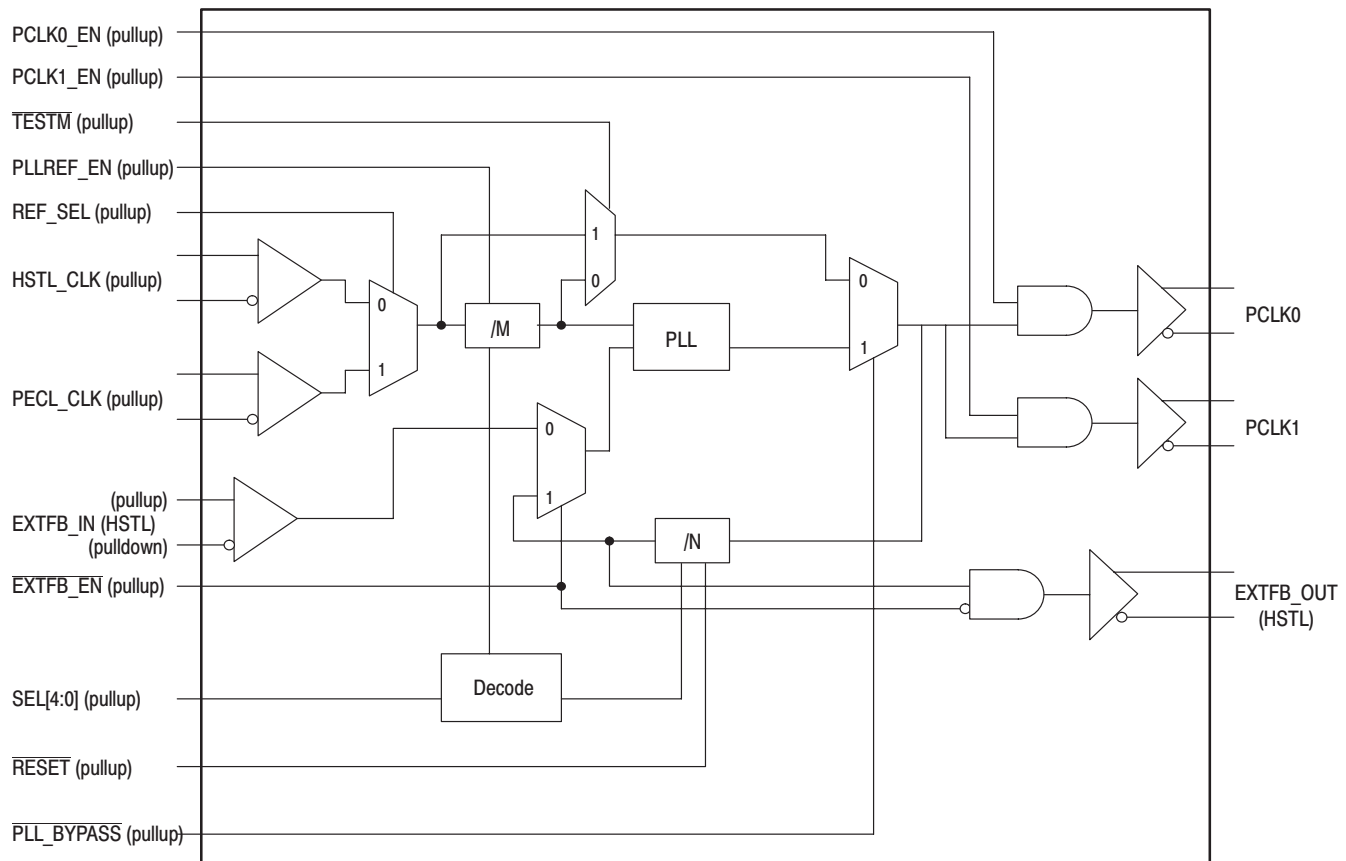


Figure 1. MPC9994 Logic Diagram

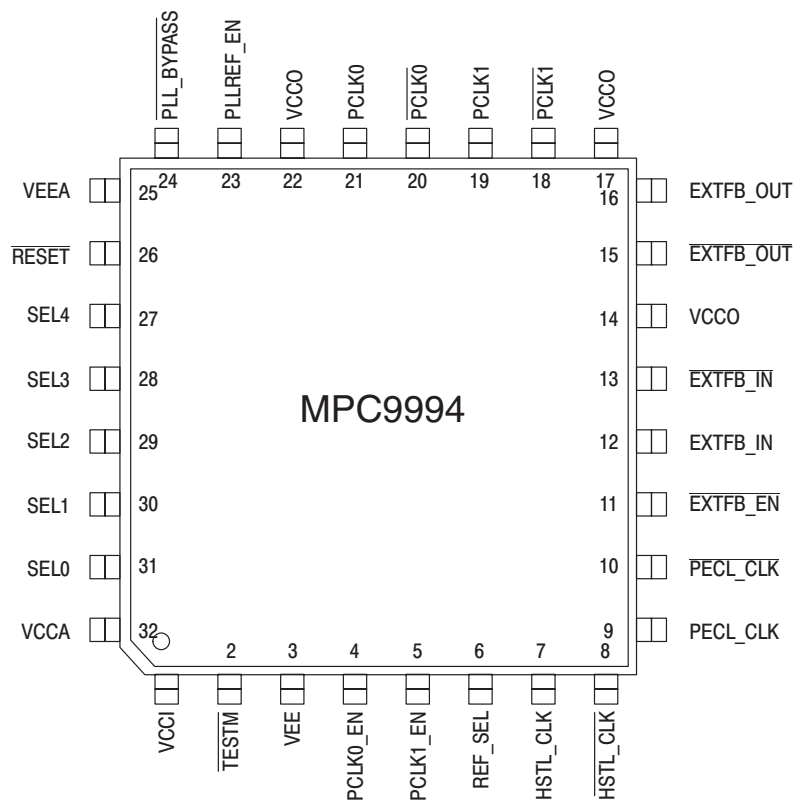


Figure 2. 32 Lead Package Pinout (Top View)

PIN CONFIGURATION

Pin #	Pin	I/O Type	Type	Description
1	VCCI	Power	Power Supply	3.3 V
2	TESTM	Input	LVC MOS	M divider test pins
3	VEE	Power (GND)	Ground	Digital GND
4	PCLK0_EN	Input	LVC MOS	PCLK0 enable
5	PCLK1_EN	Input	LVC MOS	PCLK1 enable
6	REF_SEL	Input	LVC MOS	Selects the PLL input reference clock
7	HSTL_CLK	Input	Differential HSTL	PLL reference clock input
8	HSTL_CLK	Input	Differential HSTL	PLL reference clock input
9	PECL_CLK	Input	Differential LVPECL	PLL reference clock input
10	PECL_CLK	Input	Differential LVPECL	PLL reference clock input
11	EXTFB_EN	Input	LVC MOS	External feedback enable
12	EXTFB_IN	Input	Differential HSTL	External feedback input
13	EXTFB_IN	Input	Differential HSTL	External feedback input
14	VCCO	Power	Power Supply	Output buffers power supply
15	EXTFB_OUT	Output	Differential HSTL	External feedback output clock
16	EXTFB_OUT	Output	Differential HSTL	External feedback output clock
17	VCCO	Power	Power Supply	Output buffers power supply
18	PCLK1	Output	Differential HSTL	Output clock 1
19	PCLK1	Output	Differential HSTL	Output clock 1
20	PCLK0	Output	Differential HSTL	Output clock 0
21	PCLK0	Output	Differential HSTL	Output clock 0
22	VCCO	Power	Power Supply	Output buffers power supply
23	PLLREF_EN	Input	LVC MOS	PLL reference enable
24	PLL_BYPASS	Input	LVC MOS	Input signal PLL bypass
25	VEEA	Power (GND)	Ground	Analog GND for PLL
26	RESET	Input	LVC MOS	PLL bypass reset (for test use)
27	SEL[4]	Input	LVC MOS	Selection of input and feedback frequency
28	SEL[3]	Input	LVC MOS	Selection of input and feedback frequency
29	SEL[2]	Input	LVC MOS	Selection of input and feedback frequency
30	SEL[1]	Input	LVC MOS	Selection of input and feedback frequency
31	SEL[0]	Input	LVC MOS	Selection of input and feedback frequency
32	VCCA	Power	Power Supply	3.3 V filtered for PLL (PLL power supply)

FREQUENCY SELECTION TABLE

SEL					Input Divide	Feedback Divide
4	3	2	1	0	M	N
0	0	0	0	0	5	16
0	0	0	0	1	5	17
0	0	0	1	0	5	18
0	0	0	1	1	5	19
0	0	1	0	0	5	20
0	0	1	0	1	5	21
0	0	1	1	0	5	22
0	0	1	1	1	5	23
0	1	0	0	0	5	24
0	1	0	0	1	5	25
0	1	0	1	0	5	26
0	1	0	1	1	5	27
0	1	1	0	0	5	28
0	1	1	0	1	5	29
0	1	1	1	0	5	30
0	1	1	1	1	5	31
1	0	0	0	0	5	32
1	0	0	0	1	5	33
1	0	0	1	0	5	34
1	0	0	1	1	5	35
1	0	1	0	0	5	36
1	0	1	0	1	5	37
1	0	1	1	0	5	38
1	0	1	1	1	5	39
1	1	0	0	0	5	40
1	1	0	0	1	5	41
1	1	0	1	0	5	42
1	1	0	1	1	5	43
1	1	1	0	0	5	44
1	1	1	0	1	5	45
1	1	1	1	0	5	46
1	1	1	1	1	5	47

FUNCTION TABLE (CONTROLS)

Control Pin	0	1
REF_SEL	HSTL_CLK	PECL_CLK
TESTM	M divider test mode enabled	Reference fed to Bypass mux
PLLREF_EN	Disable the input to the PLL and reset the M divider	Enable the input to the PLL
PLL_BYPASS	Outputs fed by input reference or M divider	Outputs fed by VCO
EXTFB_EN	External feedback enabled	Internal feedback enabled
PCLK0_EN	PCLK0 = low, $\overline{\text{PCLK0}}$ = high	PCLK0 = high, $\overline{\text{PCLK0}}$ = low
PCLK1_EN	PCLK1 = low, $\overline{\text{PCLK1}}$ = high	PCLK1 = high, $\overline{\text{PCLK1}}$ = low
RESET	Resets feedback N divider	Feedback enabled
SEL[4:0]	See Selection Frequency Table	

ABSOLUTE MAXIMUM RATINGS*

Symbol	Characteristics	Min	Max	Unit	Condition
VCC	Supply Voltage	-0.5	4.4	V	
VCCO	Output Supply Voltage	-0.5	4.4	V	
VIN	Input Voltage	-0.5	VCC+0.3	V	
IIN	Input Current	-1	1	mA	
TS	Storage temperature	-50	150	°C	

NOTE: Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC CHARACTERISTICS (VCCA=VCCI = 3.3V $\pm$ 5%, VCCO = 1.7 to 2.1V, TA = 0 to 70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
VIH	Input high voltage	2.0		VCCI	V	LVC MOS
VIL	Input low voltage	0.0		0.8	V	LVC MOS
VCMR	Input high voltage ^a	1		VCCI - 0.3	V	LVPECL
VPP	Input low voltage ^a	0.5		1	V	LVPECL ^b
V _{IN} (dc)	DC input signal voltage	-0.3		1.45	V	HSTL ^c
V _{DIF} (dc)	DC differential input voltage	0.4		1.75	V	HSTL ^d
V _{CM} (dc)	DC common mode input voltage	0.4		1.0	V	HSTL ^e
VOH	Output High Voltage	V _X + 0.3	V _X + 0.5	1.4	V	HSTL ^{f,a}
VOL	Output Low Voltage	0.0	V _X - 0.5	V _X - 0.3	V	HSTL ^f
ICCI	Core Supply Current			140	mA	
ICCA	PLL Supply Current		15	20	mA	
ICCO	Output Supply Current		150		mA	Note ^g
Theta _{JA}	Junction to ambient thermal resistance		53		°C/W	Note ^h

a) DC levels will vary 1:1 with VCC.

b) VPP minimum and maximum required to maintain AC specifications. Actual device function will tolerate minimum VPP of 200mV.

c) V_{IN} (dc) specifies the maximum allowable dc excursion of each differential input.

d) V_{DIF} (dc) specifies the minimum input differential voltage (V_{TR} - V_{CP}) required for switching, where V_{TR} is the "true" input signal and V_{CP} is the "complement" input signal.

e) V_{CM}(dc) specifies the maximum allowable range of input signal crosspoint voltage

f) V_X is the differential output crosspoint voltage defined in the "AC CHARACTERISTICS" section

g) 2 PCLK into 25Ω and 1 EXTFB into 50Ω

h) Measured with 1.3M/s (250fpm) airflow

AC CHARACTERISTICS ($V_{CCA} = V_{CCI} = 3.3V \pm 5\%$, $V_{CCO} = 1.7$ to $2.1V$, $T_A = 0$ to $70^{\circ}C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
fref	Input Frequency		100 - 125		MHz	
fMAX	Maximum Output Frequency	340		640	MHz	Note ^b
tsk(o)	Skew Error (PCLK)			35	ps	Note ^c
tjit(0)	Phase jitter (IO jitter)			output period / 2		Note ^c
tjit(cc)	Cycle-to-cycle jitter (full period)			5%		Note ^{c, e}
tjit(1/2per)	Cycle-to-cycle jitter (half period)			6%	Note ^d	Note ^{c, d}
V _{DIFout}	Differential Output pk-pk swing	0.6			V	For all HSTL output pairs
V _x	Differential output crosspoint voltage	0.68		0.9	V	For all HSTL output pairs
t _{lock}	Maximum PLL lock time			10	ms	

- a) All PCLK outputs are terminated in 25Ω to ground, EXTFB_OUT is terminated in 50Ω to ground (applies to all measurements).
b) With PLL active but in bypass mode, fref Max is limited by input buffer; best performance is expected with PECL input.
c) Measured at differential pair crossover.
d) Reference to half PCLK period.
e) Reference to full PCLK period.

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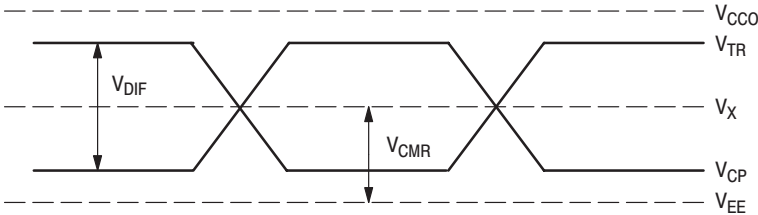


Figure 3. HSTL Differential Input Levels

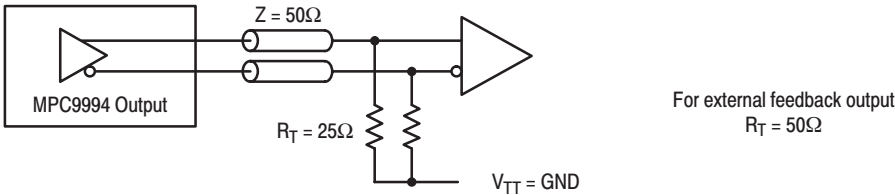


Figure 4. Output Termination and AC Test Reference

APPLICATIONS INFORMATION

Power Supply Filtering

The MPC9994 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC9994 provides separate power supplies for the output buffers (V_{CCO}) and the phase-locked loop (V_{CCA}) of the device.

The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC9994. Figure 5 illustrates a typical power supply filter scheme. The MPC9994 is most susceptible to noise with spectral content in the 10kHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the MPC9994. From the data sheet the $I_{V_{CCA}}$ current (the current sourced through the V_{CCA} pin) is typically 15 mA (20 mA maximum), assuming that a minimum of 3.3V–5% must be maintained on the V_{CCA} pin. Very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 5 “Power Supply Filter” must have a resistance of 5–15 Ω to meet the voltage drop criteria.. The RC filter pictured will provide a broadband filter with approximately 100:1 attenu-

ation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8–10 Ω resistor to avoid potential V_{CC} drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

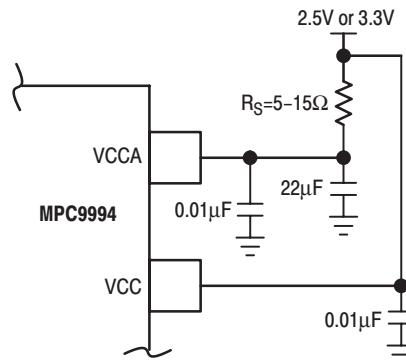


Figure 5. Power Supply Filter

Although the MPC9994 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Chapter Five

Zero–Delay Buffer Data Sheets

Zero–Delay Buffer Device Index

Device Number	Page
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MPC962305	496
MPC962308	502
MPC962309	496
MPC9653	509
MPC9658	518

Low Voltage PLL Clock Driver

The MPC953 is a 3.3V compatible, PLL based clock driver device targeted for high performance clock tree designs. With output frequencies of up to 110MHz and output skews of 150ps the MPC953 is ideal for the most demanding clock tree designs. The devices employ a fully differential PLL design to minimize cycle-to-cycle and phase jitter.

- Fully Integrated PLL
- Output Frequency up to 110MHz in PLL Mode
- Outputs Disable in High Impedance
- LQFP Packaging
- 100ps Cycle-to-Cycle Jitter

The MPC953 has a differential LVPECL reference input along with an external feedback input. These features make the MPC953 ideal for use as a zero delay, low skew fanout buffer. The device performance has been tuned and optimized for zero delay performance. The MR/OE input pin will reset the internal counters and tristate the output buffers when driven "high".

The MPC953 is fully 3.3V compatible and requires no external loop filter components. All control inputs accept LVCMOS or LVTTTL compatible levels while the outputs provide LVCMOS levels with the ability to drive terminated 50Ω transmission lines. For series terminated 50Ω lines, each of the MPC953 outputs can drive two traces giving the device an effective fanout of 1:18. The device is packaged in a 7x7mm 32-lead LQFP package to provide the optimum combination of board density and performance.

MPC953

See Upgrade Product – MPC9653

LOW VOLTAGE PLL CLOCK DRIVER



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A

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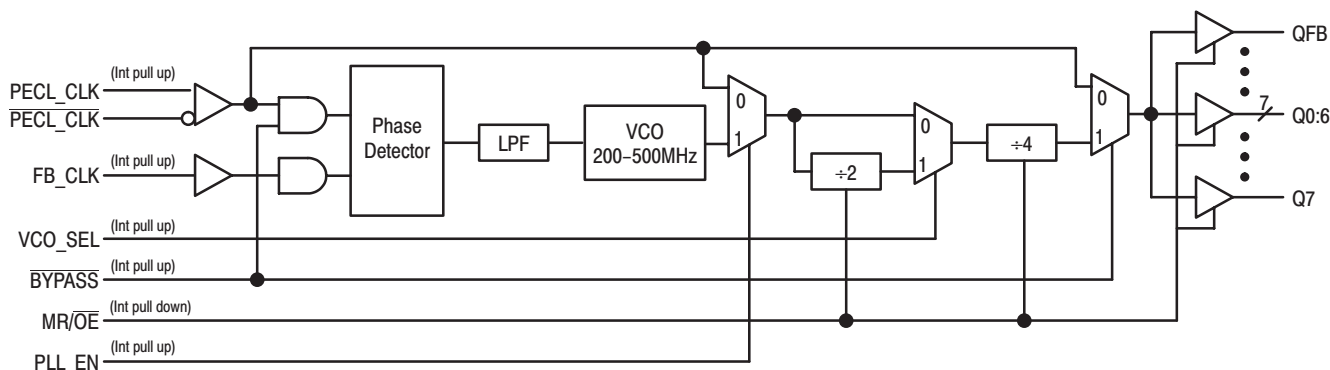


Figure 1. Logic Diagram

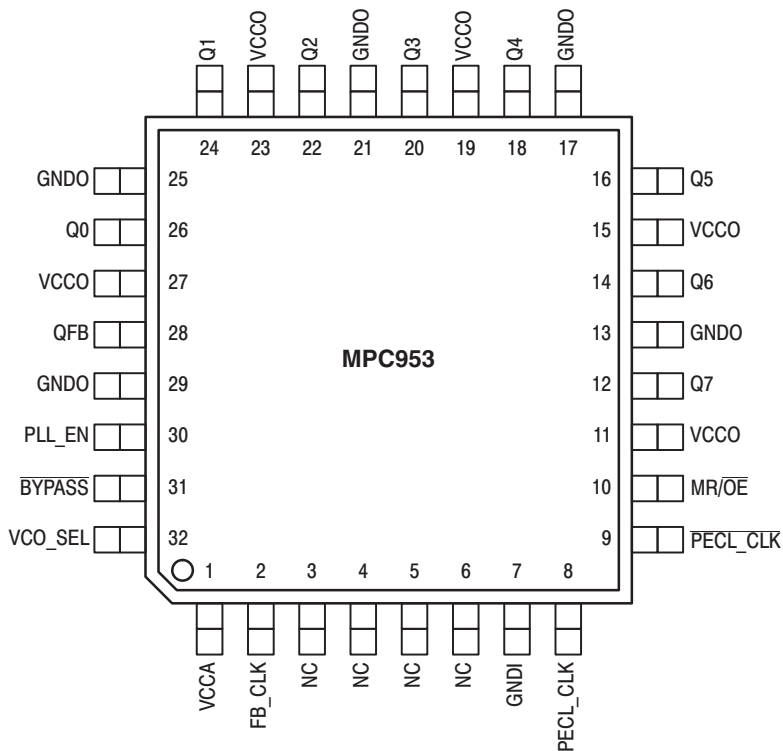


Figure 2. 32-Lead Pinout (Top View)

FUNCTION TABLES

BYPASS	Function
1	PLL Enabled
0	PLL Bypass
MR/OE	Function
1	Outputs Disabled
0	Outputs Enabled
VCO_SEL	Function
1	±2
0	±1
PLL_EN	Function
1	Select VCO
0	Select PECL_CLK

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	-0.3	4.6	V
V _I	Input Voltage	-0.3	V _{CC} + 0.3	V
I _{IN}	Input Current		±20	mA
T _{Stor}	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

THERMAL CHARACTERISTICS

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage LVCMS Inputs	2.0		3.6	V	
V_{IL}	Input LOW Voltage LVCMS Inputs			0.8	V	
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK	300		1000	mV	
V_{CMR}	Common Mode Range PECL_CLK	$V_{CC}-1.5$		$V_{CC}-0.6$	mV	Note 1.
V_{OH}	Output HIGH Voltage	$V_{CC}-0.6$			V	$I_{OH} = -20\text{mA}$, Note 2.
V_{OL}	Output LOW Voltage			0.6	V	$I_{OL} = 20\text{mA}$, Note 2.
I_{IN}	Input Current			± 120	μA	
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	Per Output
I_{CC}	Maximum Quiescent Supply Current			75	mA	All VCC Pins
I_{CCPLL}	Maximum PLL Supply Current		15	20	mA	VCCA Pin Only

- V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "HIGH" input is within the V_{CMR} range and the input swing lies within the V_{PP} specification.
- The MPC953 outputs can drive series or parallel terminated (50Ω to $V_{CC}/2$) 50Ω transmission lines on the incident edge (see Applications Info section).

PLL INPUT REFERENCE CHARACTERISTICS ($T_A = 0$ to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
f_{ref}	Reference Input Frequency	25	110	MHz	Note 3.
f_{refDC}	Reference Input Duty Cycle	25	75	%	

- Maximum and minimum input reference is limited by the VCO lock range and the feedback divider.

AC CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.8 to 2.0V, Note 6.
t_{pw}	Output Duty Cycle	45	50	55	%	Note 6.
$t_{sk(O)}$	Output-to-Output Skews			150	ps	Note 6.
f_{VCO}	PLL VCO Lock Range	200		500	MHz	Note 6.
f_{max}	Maximum Output Frequency PLL Mode PLL Mode Bypass Mode	25 50		62.5 110 200	MHz MHz MHz	VCO_SEL = '1' VCO_SEL = '0' Note 6.
$t_{pd(lock)}$	Input to FB_CLK Delay (with PLL Locked)	-75		125	ps	Note 4., 6.
$t_{pd(bypass)}$	Input to Q Delay Part-to-Part Delay	3		7 1.5	ns ns	PLL Bypassed Note 5., 6.
$t_{PLZ,HZ}$	Output Disable Time			7	ns	Note 6.
t_{PZL}	Output Enable Time			6	ns	Note 6.
t_{jitter}	Cycle-to-Cycle Jitter			100	ps	Note 6.
t_{lock}	Maximum PLL Lock Time			10	ms	

- $t_{pd(lock)}$ is input reference frequency dependent. The t_{pd} is specified at 50MHz ref, feedback $\div 8$. The t_{pd} does not include jitter.
- For a specified temperature and voltage, includes output skew.
- Termination of 50Ω to $V_{CC}/2$.

Power Supply Filtering

The MPC953 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC953 provides separate power supplies for the output buffers (VCCO) and the phase-locked loop (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC953.

Figure 3 illustrates a typical power supply filter scheme. The MPC953 is most susceptible to noise with spectral content in the 100KHz to 10MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the VCCA pin of the MPC953. From the data sheet the I_{VCCA} current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 3 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8–10Ω resistor to avoid potential V_{CC} drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

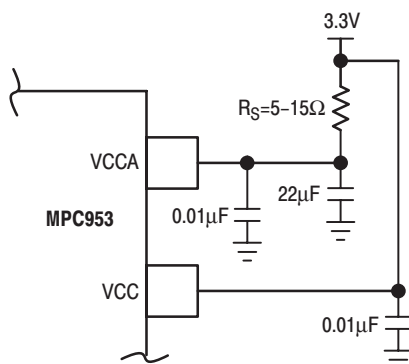


Figure 3. Power Supply Filter

Although the MPC953 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due

to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC953 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC953 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fan-out of the MPC953 clock driver is effectively doubled due to its capability to drive multiple lines.

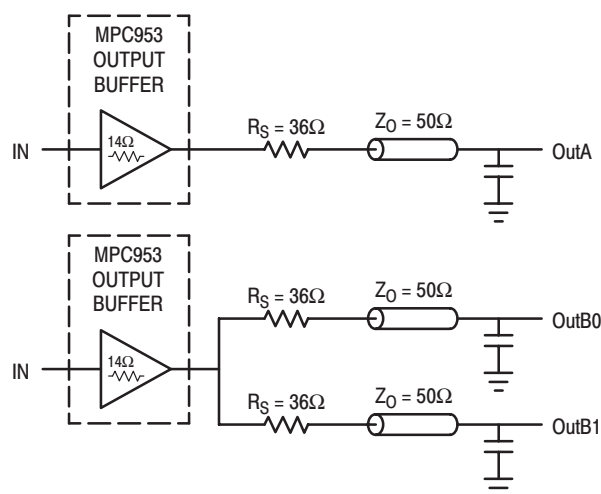


Figure 4. Single versus Dual Transmission Lines

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC953 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC953. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 / (R_S + R_o + Z_0))$$

$$Z_0 = 50\Omega \parallel 50\Omega$$

$$R_S = 36\Omega \parallel 36\Omega$$

$$R_o = 14\Omega$$

$$V_L = 3.0 (25 / (18 + 14 + 25)) = 3.0 (25 / 57) \\ = 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.62V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

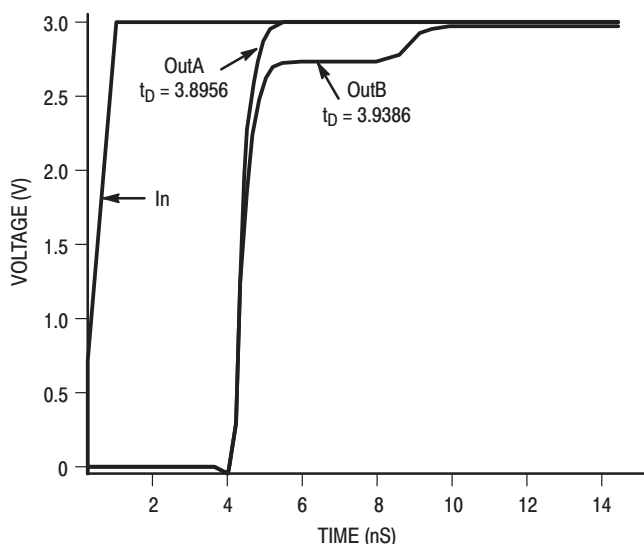


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

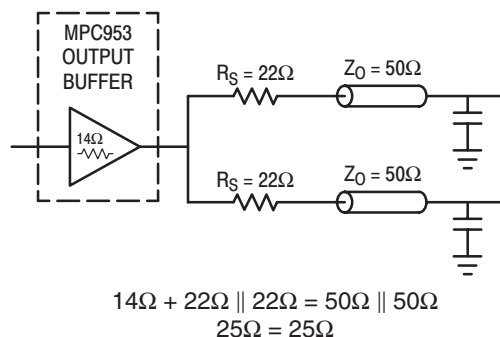


Figure 6. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Low Voltage PLL Clock Driver

The MPC954 is a 3.3V compatible, PLL based zero delay buffer targeted for high performance clock tree designs. With 11 outputs at frequencies of up to 100MHz and output skews of 200ps the MPC954 is ideal for the most demanding clock tree designs. The devices employ a fully differential PLL design to minimize cycle-to-cycle and phase jitter.

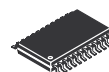
- Fully Integrated PLL
- Output Frequency up to 100MHz
- Outputs Disable in High Impedance
- TSSOP Packaging
- 50ps Cycle-to-Cycle Jitter Typical

The analog V_{CC} pin of the device also serves as a PLL bypass select pin. When driven low the V_{CCA} pin will route the REF_CLK input around the PLL directly to the outputs. The OE input is a logic enable for all of the outputs except QFB. A low on the OE pin forces Q0-Q9 to a logic low state.

The MPC954 is fully 3.3V compatible and requires no external loop filter components. All inputs accept LVCMOS or LVTTTL compatible levels while the outputs provide LVCMOS levels with the ability to drive terminated 50 Ω transmission lines. The output impedance of the MPC954 is $\approx 10\Omega$, therefore for series terminated 50 Ω lines, each of the MPC954 outputs can drive two traces giving the device an effective fanout of 1:22. The device is packaged in a 24-lead TSSOP package to provide the optimum combination of board density and performance.

MPC954

**LOW VOLTAGE
PLL ZERO DELAY BUFFER**



DT SUFFIX
24-LEAD TSSOP PACKAGE
CASE 948H

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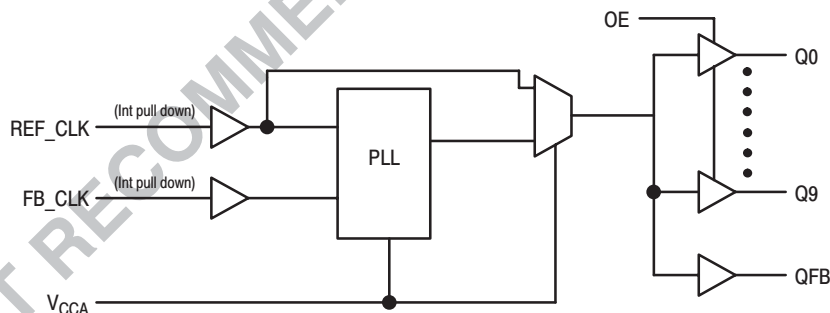
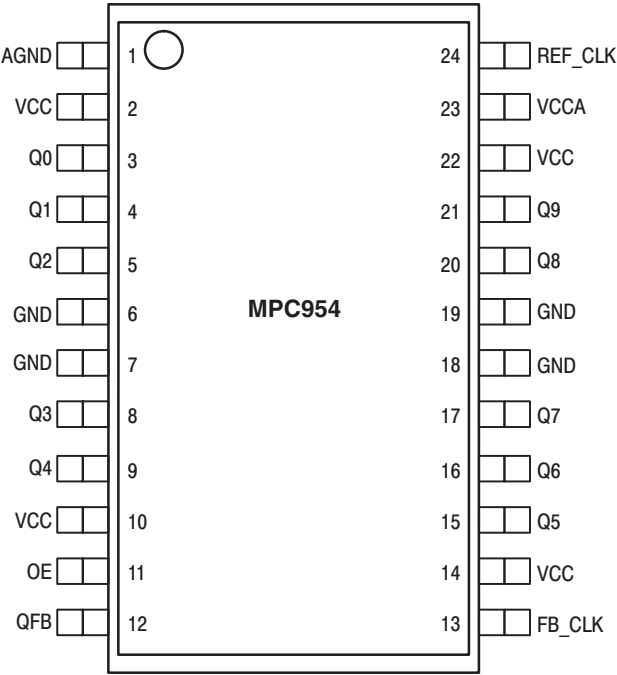


Figure 1. Block Diagram



FUNCTION TABLES

VCCA	Function
1	PLL Enabled
0	PLL Bypass
OE	Function
1	Q0 – Q9 Enabled
0	Q0 – Q9 Low

5

Figure 2. 24-Lead Pinout (Top View)

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	–0.3	4.6	V
V _I	Input Voltage	–0.3	V _{CC} + 0.3	V
I _{IN}	Input Current		±20	mA
T _{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

THERMAL CHARACTERISTICS

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage LVC MOS Inputs	2.0		3.6	V	
V_{IL}	Input LOW Voltage LVC MOS Inputs			0.8	V	
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -20\text{mA}$, Note 1.
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 20\text{mA}$, Note 1.
I_{IN}	Input Current			± 120	μA	Note 2.
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	Per Output
I_{CC}	Maximum Quiescent Supply Current		40		mA	All VCC Pins
I_{CCPLL}	Maximum PLL Supply Current		15		mA	VCCA Pin Only

1. The MPC954 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}/2$) transmission lines on the incident edge (see Applications Info section).
2. Inputs have pullup resistor which affect input current.

PLL INPUT REFERENCE CHARACTERISTICS ($T_A = 0$ to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
f_{ref}	Reference Input Frequency	50	100	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

AC CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time	0.3		1.5	ns	0.8 to 2.0V, (Note 1.)
t_{pw}	Output Duty Cycle	40	50	60	%	(Note 1.)
$t_{sk(O)}$	Output-to-Output Skews			300	ps	(Note 1.)
f_{max}	Maximum Output Frequency PLL Mode	50		100	MHz	(Note 1.)
$t_{pd(lock)}$	REF_CLK to FB_CLK Delay (with PLL Locked)	-300		0	ps	(Note 1.)
$t_{PLZ,HZ}$	Output Disable Time		7		ns	(Note 1.)
t_{PZL}	Output Enable Time		7		ns	(Note 1.)
t_{jitter}	Cycle-to-Cycle Jitter (Peak-to-Peak)		50		ps	(Note 1.)
t_{lock}	Maximum PLL Lock Time			10	ms	

1. Termination of 50Ω to $V_{CC}/2$.

Power Supply Filtering

The MPC954 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC954 provides separate power supplies for the output buffers (VCCO) and the phase-locked loop (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC954.

Figure 3 illustrates a typical power supply filter scheme. The MPC954 is most susceptible to noise with spectral content in the 1KHz to 10MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the VCCA pin of the MPC954. From the data sheet the I_{VCCA} current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 3 must have a resistance of 10–15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8–10 Ω resistor to avoid potential V_{CC} drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

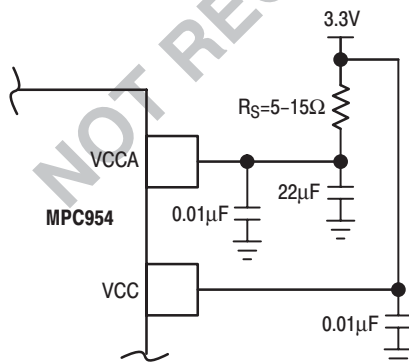


Figure 3. Power Supply Filter

Although the MPC954 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be ap-

plications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC954 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC954 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fan-out of the MPC954 clock driver is effectively doubled due to its capability to drive multiple lines.

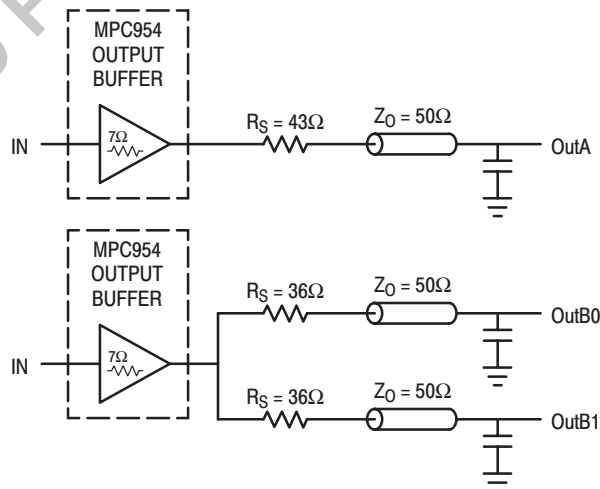


Figure 4. Single versus Dual Transmission Lines

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC954 output buffers is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC954. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_o / (R_s + R_o + Z_o))$$

$$Z_o = 50\Omega \parallel 50\Omega$$

$$R_s = 43\Omega \parallel 43\Omega$$

$$R_o = 7\Omega$$

$$V_L = 3.0 (25 / (21.5 + 7 + 25)) = 3.0 (25 / 53.5) \\ = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.80V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

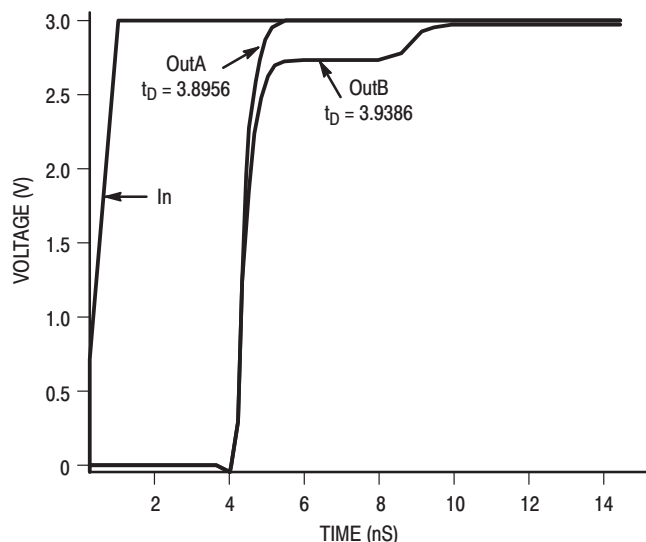


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

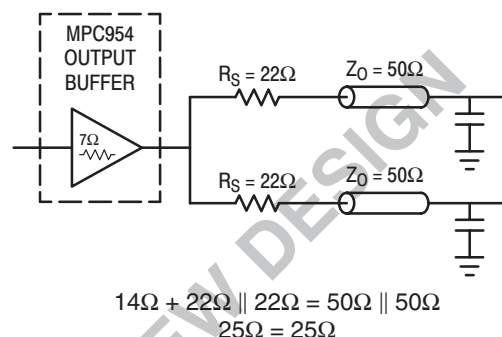


Figure 6. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Low Voltage PLL Clock Driver

The MPC958 is a 3.3V compatible, PLL based clock driver device targeted for high performance clock tree designs. With output frequencies of up to 200MHz and output skews of 200ps the MPC958 is ideal for the most demanding clock tree designs. The devices employ a fully differential PLL design to minimize cycle-to-cycle and phase jitter.

- Fully Integrated PLL
- Output Frequency up to 200MHz
- Outputs Disable in High Impedance
- LQFP Packaging
- 100ps Cycle-to-Cycle Jitter

The MPC958 has a differential LVPECL reference input along with an external feedback input. These features make the MPC958 ideal for use as a zero delay, low skew fanout buffer. The device performance has been tuned and optimized for zero delay performance. The MR/OE input pin will tristate the output buffers when driven "high".

The MPC958 is fully 3.3V compatible and requires no external loop filter components. All control inputs accept LVCMOS or LVTTTL compatible levels while the outputs provide LVCMOS levels with the ability to drive terminated 50Ω transmission lines. For series terminated 50Ω lines, each of the MPC958 outputs can drive two traces giving the device an effective fanout of 1:22. The device is packaged in a 7x7mm 32-lead LQFP package to provide the optimum combination of board density and performance.

MPC958

See Upgrade Product – MPC9658

LOW VOLTAGE PLL CLOCK DRIVER



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A

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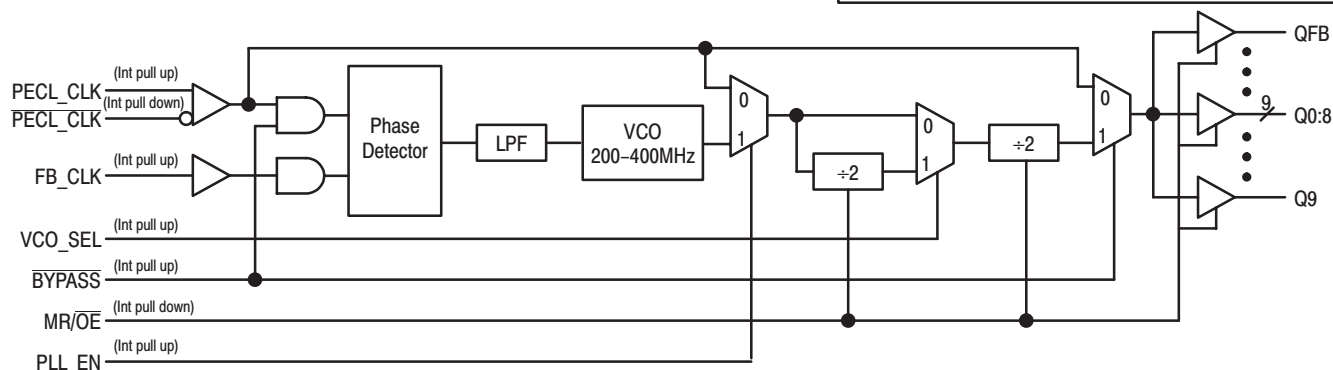


Figure 1. Logic Diagram

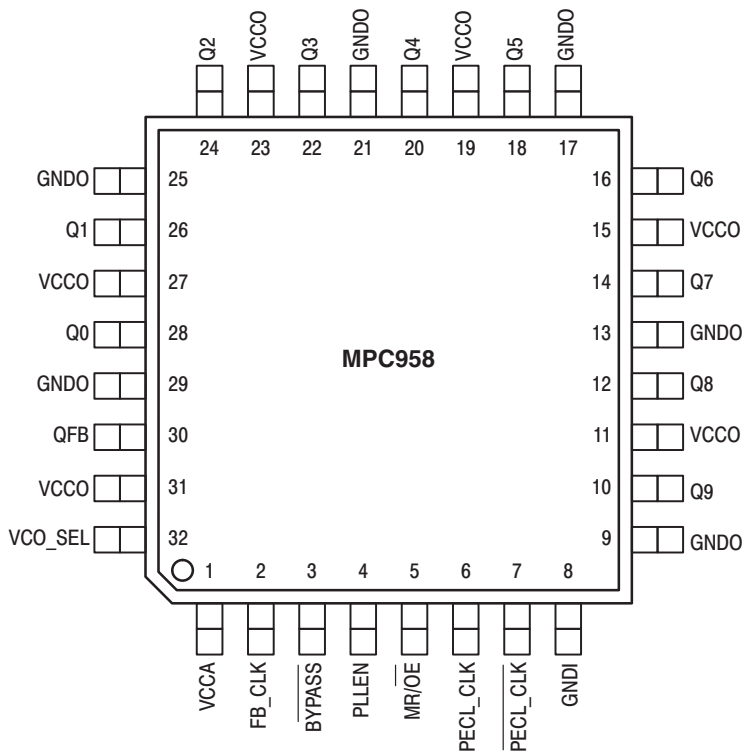


Figure 2. 32-Lead Pinout (Top View)

FUNCTION TABLES

BYPASS	Function
1	PLL Enabled
0	PLL Bypass
MR/OE	Function
1	Outputs Disabled
0	Outputs Enabled
VCO_SEL	Function
1	±2
0	±1
PLL_EN	Function
1	Select VCO
0	Select PECL_CLK

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ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	−0.3	4.6	V
V _I	Input Voltage	−0.3	V _{CC} + 0.3	V
I _{IN}	Input Current		±20	mA
T _{Stor}	Storage Temperature Range	−40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

THERMAL CHARACTERISTICS

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage LVC MOS Inputs	2.0		3.6	V	
V_{IL}	Input LOW Voltage LVC MOS Inputs			0.8	V	
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK	300		1000	mV	
V_{CMR}	Common Mode Range PECL_CLK	1.0		3.0	V	Note 1.
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -20\text{mA}$, Note 2.
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 20\text{mA}$, Note 2.
I_{IN}	Input Current			± 120	μA	
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	Per Output
I_{CC}	Maximum Quiescent Supply Current			75	mA	All VCC Pins
I_{CCPLL}	Maximum PLL Supply Current		15	20	mA	VCCA Pin Only

1. V_{CMR} is the center of the differential input signal. Normal operation is obtained when the input crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} specification.
2. The MPC958 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}/2$) transmission lines on the incident edge (see Applications Info section).

PLL INPUT REFERENCE CHARACTERISTICS ($T_A = 0$ to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
f_{ref}	Reference Input Frequency	Note 1.	Note 1.	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

3. Maximum and minimum input reference is limited by the VCO lock range and the feedback divider.

AC CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time	0.10		1.0	ns	0.8 to 2.0V Note 1.
t_{pw}	Output Duty Cycle PLL Mode	$t_{cycle}/2 - 400$		$t_{cycle}/2 + 400$	ps	Note 1.
$t_{sk(O)}$	Output-to-Output Skews (Relative to QFB)			200	ps	Note 1.
f_{VCO}	PLL VCO Lock Range	200		400	MHz	
f_{max}	Maximum Output Frequency (Note 1.) PLL Mode PLL Mode Bypass Mode	50 100		100 200 200	MHz	VCO_SEL = '1' VCO_SEL = '0'
$t_{pd(lock)}$	Input to Ext_FB Delay (with PLL Locked @ 100MHz)	-70		130	ps	Note 1.
$t_{pd(bypass)}$	Input to Q Delay	3.0		7.0	ns	PLL Bypassed
$t_{PLZ,HZ}$	Output Disable Time			7	ns	
t_{PZL}	Output Enable Time			6	ns	
t_{jitter}	Cycle-to-Cycle Jitter (Peak-to-Peak)			100	ps	Note 1.
t_{lock}	Maximum PLL Lock Time			10	ms	

4. Termination of 50Ω to $V_{CC}/2$.

Power Supply Filtering

The MPC958 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC958 provides a separate power supply for the phase-locked loop (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC958.

Figure 3 illustrates a typical power supply filter scheme. The MPC958 is most susceptible to noise with spectral content in the 1kHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the VCCA pin of the MPC958. From the data sheet the I_{VCCA} current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 3 must have a resistance of 10–15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20kHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8–10 Ω resistor to avoid potential V_{CC} drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

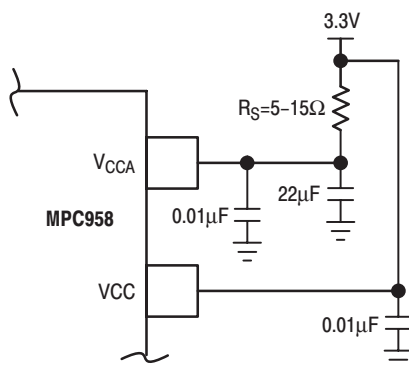


Figure 3. Power Supply Filter

Although the MPC958 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter

schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC958 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC958 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fan-out of the MPC958 clock driver is effectively doubled due to its capability to drive multiple lines.

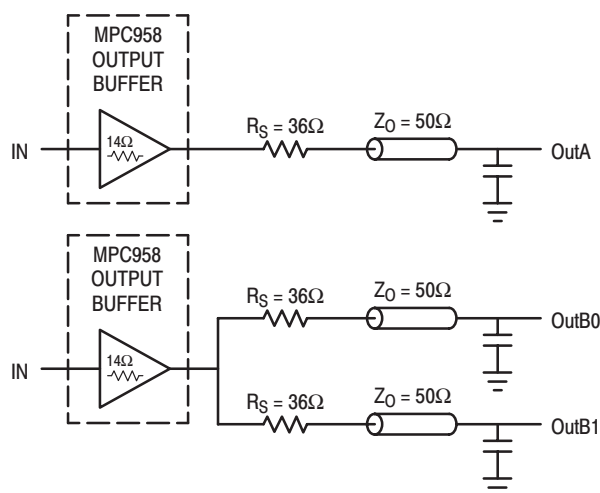


Figure 4. Single versus Dual Transmission Lines

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC958 output buffers is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC958. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 / (R_S + R_o + Z_0))$$

$$Z_0 = 50\Omega \parallel 50\Omega$$

$$R_S = 36\Omega \parallel 36\Omega$$

$$R_o = 14\Omega$$

$$V_L = 3.0 (25 / (18 + 14 + 25)) = 3.0 (25 / 57) \\ = 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.62V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

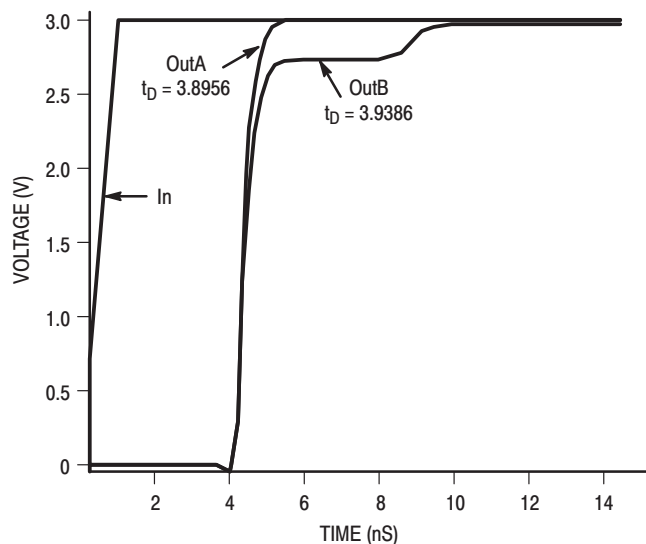


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

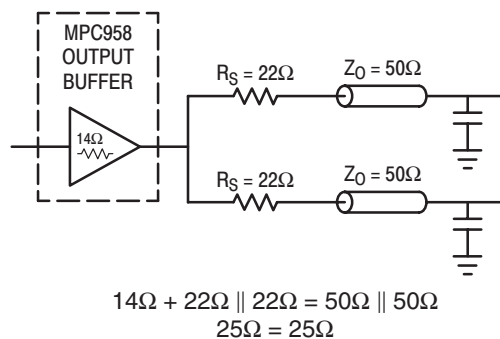


Figure 6. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Product Preview

1:10 LVCMOS Zero Delay Clock Buffer

The MPC9608 is a 2.5V and 3.3V compatible, 1:10 PLL based zero-delay buffer. With a very wide frequency range and low output skews the MPC9608 is targeted for high performance and mid-range clock tree designs.

Features

- 1:10 outputs LVCMOS zero-delay buffer
- Single 3.3V or 2.5V supply
- 150 ps maximum output skew¹
- ± 100 ps static phase offset (SPO)¹
- Supports a clock I/O frequency range of 12.5 to 200 MHz
- Selectable divide-by-two for one output bank
- Synchronous output enable control (CLK_STOP)
- Output tristate control (output high impedance)
- PLL bypass mode for low frequency system test purpose
- Supports networking, telecommunications and computer applications
- Supports a variety of microprocessors and controllers
- Compatible to PowerQuicc I and II
- Ambient Temperature Range -40°C to $+85^{\circ}\text{C}$

Functional Description

The MPC9608 uses an internal PLL and an external feedback path to lock its low-skew clock output phase to the reference clock phase, providing virtually zero propagation delay. This enables nested clock designs with near-zero insertion delay. Designs using the MPC9608 as PLL fan-out buffer will show significantly lower clock skew than clock distributions developed from traditional fanout buffers. The device offers one reference clock input and two banks of 5 outputs for clock fanout. The input frequency and phase is reproduced by the PLL and provided at the outputs. A selectable frequency divider sets the bank B outputs to generate either an identical copy of the bank A clocks or one half of the bank A clock frequency. Both output banks remain synchronized to the input reference for both bank B configurations.

Outputs are only disabled or enabled when the outputs are already in logic low state (CLK_STOP). For system test and diagnosis, the MPC9608 outputs can also be set to high-impedance state by connecting $\overline{\text{OE}}$ to logic high level. Additionally, the device provides a PLL bypass mode for low frequency test purpose. In PLL bypass mode, the minimum frequency and static phase offset specification do not apply.

CLK_STOP and $\overline{\text{OE}}$ do not affect the PLL feedback output (QFB) and down stream clocks can be disabled without the internal PLL losing lock.

The MPC9608 is fully 2.5V or 3.3V compatible and requires no external components for the internal PLL. All inputs accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated $50\ \Omega$ transmission lines on the incident edge. For series terminated transmission lines, each of the MPC9608 outputs can drive one or two traces giving the devices an effective fanout of 1:20. The device is packaged in a $7\times 7\ \text{mm}^2$ 32-lead LQFP package.

MPC9608

**LOW VOLTAGE 3.3V/2.5V
LVCMOS 1:10 ZERO-DELAY
CLOCK BUFFER**



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A

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1. Final AC specifications pending final device characterization.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

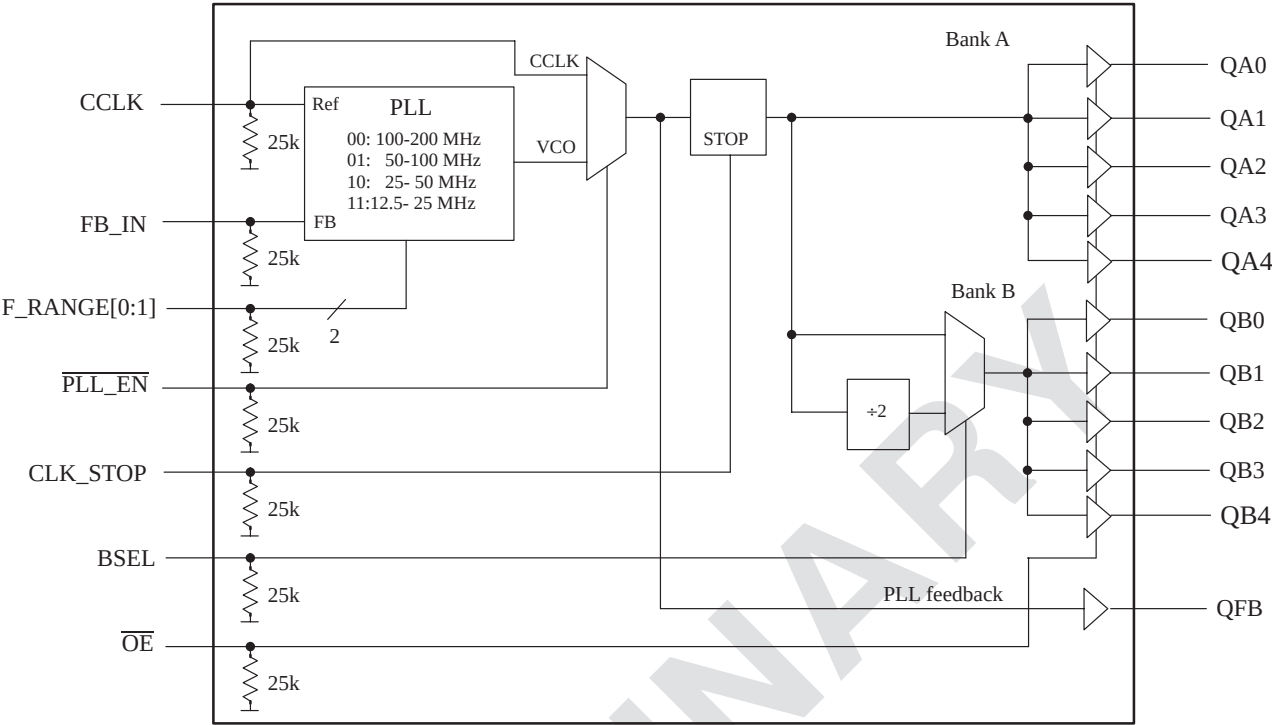


Figure 1. MPC9608 Logic Diagram

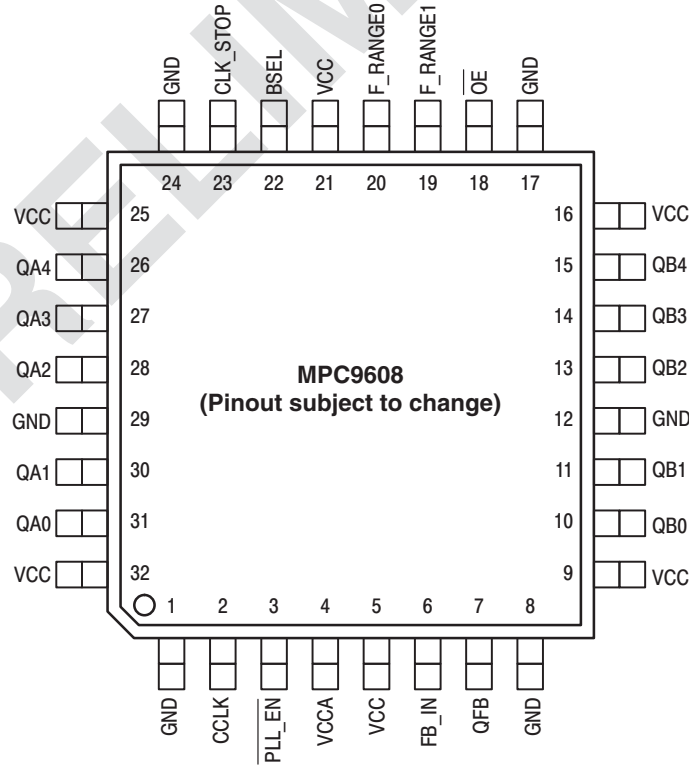


Figure 2. MPC9608 32-Lead Package Pinout (Top View)

TABLE 1: PIN CONFIGURATION

Pin	I/O	Type	Function
CCLK	Input	LVC MOS	PLL reference clock signal
FB_IN	Input	LVC MOS	PLL feedback signal input, connect to a QFB output
F_RANGE[0:1]	Input	LVC MOS	PLL frequency range select
BSEL	Input	LVC MOS	Frequency divider select for bank B outputs
PLL_EN	Input	LVC MOS	PLL enable/disable
$\overline{OE}$	Input	LVC MOS	Output enable/disable (high-impedance tristate)
CLK_STOP	Input	LVC MOS	Synchronous clock enable/stop
QA0-4, QB0-4	Output	LVC MOS	Clock outputs
QFB	Output	LVC MOS	PLL feedback signal output. Connect to FB_IN
GND	Supply	Ground	Negative power supply
VCCA	Supply	VCC	PLL positive power supply (analog power supply). The MPC9608 requires an external RC filter for the analog power supply pin VCCA. Please see applications section for details.
VCC	Supply	VCC	Positive power supply for I/O and core

TABLE 2: FUNCTION TABLE

Control	Default	0	1
F_RANGE[0:1]	00	PLL frequency range. See Table 3 "Clock frequency configuration for QFB connected to FB_IN"	
BSEL	0	$f_{QB0-4} = f_{QA0-4}$	$f_{QB0-4} = f_{QA0-4} \div 2$
CLK_STOP	0	Outputs enabled	Outputs synchronously stopped in logic low state
$\overline{OE}$	0	Outputs enabled (active)	Outputs disabled (high-impedance state), independent on CLK_STOP. Applying $\overline{OE}=1$ and PLL_EN=1 resets the device. The PLL feedback output QFB is not affected by $\overline{OE}$.
PLL_EN	0	Normal operation mode with PLL enabled.	Test mode with PLL disabled. CCLK is substituted for the internal VCO output. MPC9608 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable. Applying $\overline{OE}=1$ and PLL_EN=1 resets the device.

TABLE 3: Clock Frequency Configuration for QFB connected to FB_IN

F_RANGE[0]	F_RANGE[1]	BSEL	f_{REF} (CCLK) range [MHz]	QA0-QA4		QB0-B4		QFB
				Ratio	f_{QA0-4} [MHz]	Ratio	f_{QB0-4} [MHz]	
0	0	0	100.0—200.0	f_{REF}	100.0—200.0	f_{REF}	100.0—200.0	f_{REF}
0	0	1				$f_{REF} \div 2$	50.0—25.0	f_{REF}
0	1	0	50.0—100.0	f_{REF}	50.0—100.0	f_{REF}	50.0—100.0	f_{REF}
0	1	1				$f_{REF} \div 2$	25.0—50.0	f_{REF}
1	0	0	25.0—50.0	f_{REF}	25.0—50.0	f_{REF}	25.0—50.0	f_{REF}
1	0	1				$f_{REF} \div 2$	12.5—25.0	f_{REF}
1	1	0	12.5—25.0	f_{REF}	12.5—25	f_{REF}	12.5—25.0	f_{REF}
1	1	1				$f_{REF} \div 2$	50.0—100	f_{REF}

TABLE 4: GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		$V_{CC} \div 2$		V	
MM	ESD protection (Machine model)	200			V	
HBM	ESD protection (Human body model)	2000			V	
LU	Latch-up immunity	200			mA	
C_{PD}	Power dissipation capacitance		10		pF	Per output
C_{IN}	Input capacitance		4.0		pF	Inputs

TABLE 5: ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.6	V	
V_{IN}	DC Input Voltage	-0.3	$V_{CC}+0.3$	V	
V_{OUT}	DC Output Voltage	-0.3	$V_{CC}+0.3$	V	
I_{IN}	DC Input Current		± 20	mA	
I_{OUT}	DC Output Current		± 50	mA	
T_S	Storage temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

TABLE 6: DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input Low Voltage			0.8	V	LVC MOS
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -24 \text{ mA}^a$
V_{OL}	Output Low Voltage			0.55 0.30	V V	$I_{OL} = 24 \text{ mA}$ $I_{OL} = 12 \text{ mA}$
Z_{OUT}	Output Impedance		14 - 17		Ω	
I_{IN}	Input Current ^b			± 200	μA	$V_{IN} = V_{CC}$ or GND
I_{CCA}	Maximum PLL Supply Current		3.0	5.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins

a. The MPC9608 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines.

b. Inputs have pull-down resistors affecting the input current.

TABLE 7: AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)^{a b}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input reference frequency in PLL mode ^c F_RANGE = 00 F_RANGE = 01 F_RANGE = 10 F_RANGE = 11 Input reference frequency in PLL bypass mode ^d	100 50 25 12.5 0		200 100 50 25 TBD	MHz MHz MHz MHz MHz	
f_{MAX}	Output Frequency ^e F_RANGE = 00 F_RANGE = 01 F_RANGE = 10 F_RANGE = 11	100 50 25 12.5		200 100 50 25	MHz MHz MHz MHz	BSEL = 0 BSEL = 0 BSEL = 0 BSEL = 0
f_{refDC}	Reference Input Duty Cycle	25		75	%	
t_r, t_f	CCLK Input Rise/Fall Time			1.0	ns	0.8 to 2.0V
$t_{(\phi)}$	Propagation Delay (static phase offset) CCLK to FB_IN F_RANGE = 00 F_RANGE = 01 F_RANGE = 10 F_RANGE = 11		± 100		ps	PLL locked
$t_{sk(o)}$	Output-to-Output Skew ^f			150	ps	
DC	Output Duty Cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter RMS (1 σ) ^g		15		ps	BSEL = 0
$t_{JIT(PER)}$	Period Jitter RMS (1 σ)		10		ps	BSEL = 0
$t_{JIT(\phi)}$	I/O Phase Jitter RMS (1 σ)		TBD		ps	BSEL = 0
t_s	Setup time, CLK_STOP to CCLK	100			ps	
t_h	Hold time, CCLK to CLK_STOP	100			ps	
BW	PLL closed loop bandwidth ^h F_RANGE = 00 F_RANGE = 01 F_RANGE = 10 F_RANGE = 11			TBD TBD TBD TBD	kHz kHz kHz kHz	
t_{LOCK}	Maximum PLL Lock Time		10		ms	

a. All AC characteristics are design targets and subject to change upon device characterization.

b. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

c. PLL mode requires $PLL\_EN = 0$ to enable the PLL and zero-delay operation.

d. In bypass mode, the MPC9608 divides the input reference clock.

e. Applies for bank A and for bank B if BSEL = 0. If BSEL = 1, the min. and max. output frequency of bank B must be divided by two.

f. See application section for part-to-part skew calculation.

g. See application section for a jitter calculation for other confidence factors than 1 σ .

h. -3 dB point of PLL transfer characteristics.

TABLE 8: DC CHARACTERISTICS ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	1.7		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input Low Voltage	-0.3		0.7	V	LVC MOS
V_{OH}	Output High Voltage	1.8			V	$I_{OH} = -15 \text{ mA}^a$
V_{OL}	Output Low Voltage			0.6	V	$I_{OL} = 15 \text{ mA}$
Z_{OUT}	Output Impedance		17 - 20		Ω	
I_{IN}	Input Current			± 200	μA	$V_{IN} = V_{CC}$ or GND
I_{CCA}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins

a. The MPC9608 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

TABLE 9: AC CHARACTERISTICS ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)^{a b}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input reference frequency in PLL mode ^c F_RANGE = 00 F_RANGE = 01 F_RANGE = 10 F_RANGE = 11 Input reference frequency in PLL bypass mode ^d	100 50 25 12.5 0		200 100 50 25 TBD	MHz MHz MHz MHz MHz	
f_{MAX}	Output Frequency ^e F_RANGE = 00 F_RANGE = 01 F_RANGE = 10 F_RANGE = 11	100 50 25 12.5		200 100 50 25	MHz MHz MHz MHz	BSEL = 0 BSEL = 0 BSEL = 0 BSEL = 0
f_{refDC}	Reference Input Duty Cycle	25		75	%	
t_r, t_f	CCLK Input Rise/Fall Time			1.0	ns	0.7 to 1.7V
$t_{(\phi)}$	Propagation Delay (static phase offset) CCLK to FB_IN F_RANGE = 00 F_RANGE = 01 F_RANGE = 10 F_RANGE = 11		± 100		ps	PLL locked
$t_{sk(o)}$	Output-to-Output Skew ^f			150	ps	
DC	Output Duty Cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.6 to 1.8V
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter RMS (1 σ) ^g		15		ps	BSEL = 0
$t_{JIT(PER)}$	Period Jitter RMS (1 σ)		10		ps	BSEL = 0
$t_{JIT(\phi)}$	I/O Phase Jitter RMS (1 σ)		TBD		ps	BSEL = 0
t_S	Setup time, CLK_STOP to CCLK	100			ps	
t_H	Hold time, CCLK to CLK_STOP	100			ps	
BW	PLL closed loop bandwidth ^h F_RANGE = 00 F_RANGE = 01 F_RANGE = 10 F_RANGE = 11			TBD TBD TBD TBD	kHz kHz kHz kHz	
t_{LOCK}	Maximum PLL Lock Time		10		ms	

a. All AC characteristics are design targets and subject to change upon device characterization.

b. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

c. PLL mode requires $PLL\_EN = 0$ to enable the PLL and zero-delay operation.

d. In bypass mode, the MPC9608 divides the input reference clock.

e. Applies for bank A and for bank B if BSEL = 0. If BSEL = 1, the min. and max. output frequency of bank B must be divided by two.

f. See application section for part-to-part skew calculation.

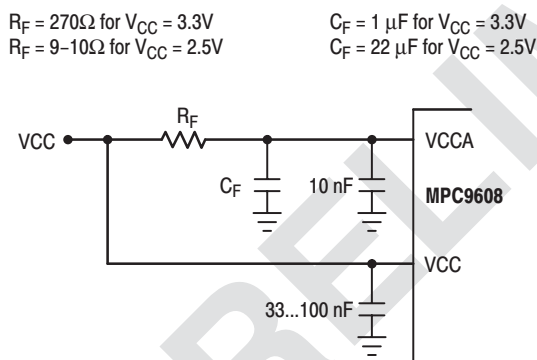
g. See application section for a jitter calculation for other confidence factors than 1 σ .

h. -3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Power Supply Filtering

The MPC9608 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9608 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC9608. Figure 3 illustrates a typical power supply filter scheme. The MPC9608 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F . From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V ($V_{CC}=3.3V$ or $V_{CC}=2.5V$) must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 3 "V_{CCA} Power Supply Filter" must have a resistance of 270Ω ($V_{CC}=3.3V$) or 9-10Ω ($V_{CC}=2.5V$) to meet the voltage drop criteria.

Figure 3. V_{CCA} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3 "V_{CCA} Power Supply Filter", the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9608 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is

being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9608 in zero-delay applications

Nested clock trees are typical applications for the MPC9608. Designs using the MPC9608 as LVCMOS PLL fan-out buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fan-out buffers. The external feedback option of the MPC9608 clock driver allows for its use as a zero delay buffer. By using the QFB output as a feedback to the PLL the propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of part-to-part skew

The MPC9608 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9608 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD, LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consists of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

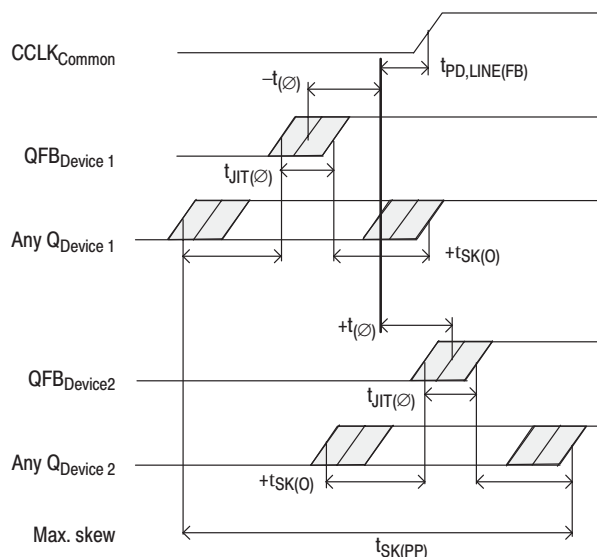


Figure 4. MPC9608 max. device-to-device skew

Due to the statistical nature of I/O jitter a RMS value (1σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 10.

Table 10: Confidence Factor CF

CF	Probability of clock edge within the distribution
$\pm 1\sigma$	0.68268948
$\pm 2\sigma$	0.95449988
$\pm 3\sigma$	0.99730007
$\pm 4\sigma$	0.99993663
$\pm 5\sigma$	0.99999943
$\pm 6\sigma$	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% ($\pm 3\sigma$) is assumed, resulting in a worst case timing uncertainty from input to any output of -295 ps¹ relative to CCLK:

$$t_{SK(PP)} = [-100ps...100ps] + [-150ps...150ps] + [(15ps \cdot -3)...(15ps \cdot 3)] + t_{PD, LINE(FB)}$$

$$t_{SK(PP)} = [-295ps...295ps] + t_{PD, LINE(FB)}$$

Due to the frequency dependence of I/O jitter, Figure 5 "Max. I/O Jitter versus frequency" can be used for a more precise timing performance analysis.

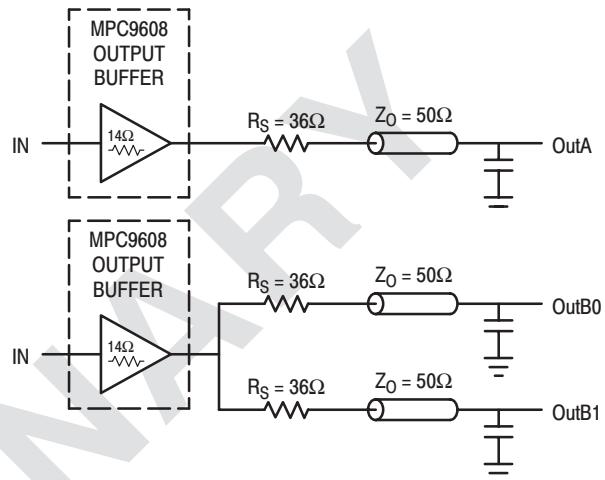
TBD

Figure 5. Max. I/O Jitter versus frequency

Driving Transmission Lines

The MPC9608 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC} \pm 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9608 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 6 "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9608 clock driver is effectively doubled due to its capability to drive multiple lines.

**Figure 6. Single versus Dual Transmission Lines**

The waveform plots in Figure 7 "Single versus Dual Line Termination Waveforms" show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9608 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9608. The output waveform in Figure 7 "Single versus Dual Line Termination Waveforms" shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned} V_L &= V_S (Z_0 \div (R_S + R_0 + Z_0)) \\ Z_0 &= 50\Omega \parallel 50\Omega \\ R_S &= 36\Omega \parallel 36\Omega \\ R_0 &= 14\Omega \\ V_L &= 3.0 (25 \div (18 + 17 + 25)) \\ &= 1.31V \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

1. Skew data are design targets and pending device specifications.

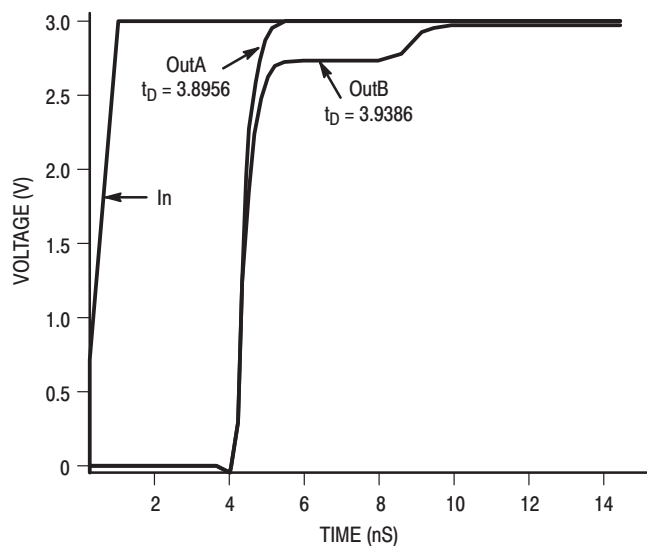


Figure 7. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be

uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 8 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

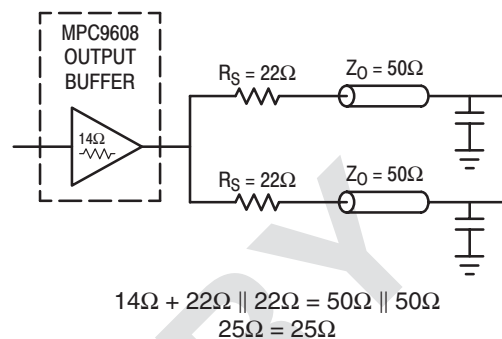
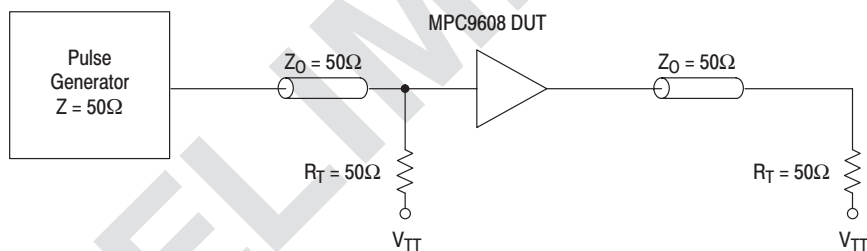
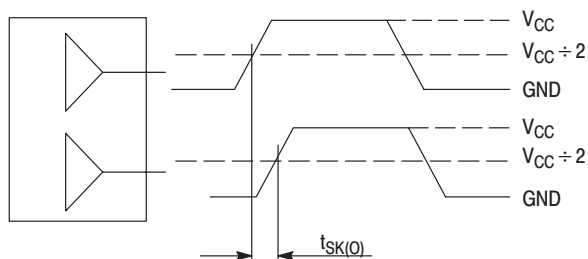


Figure 8. Optimized Dual Line Termination

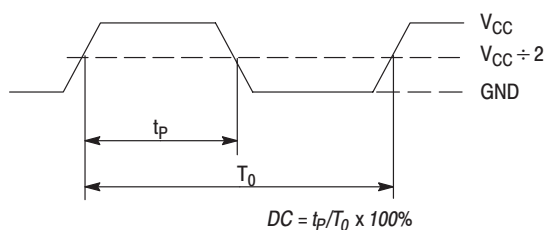
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Figure 9. CCLK MPC9608 AC test reference for $V_{CC} = 3.3V$ and $V_{CC} = 2.5V$



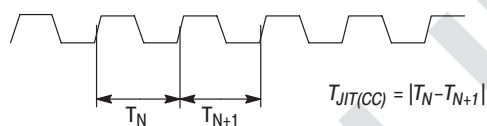
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 10. Output-to-output Skew $t_{SK(O)}$



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 12. Output Duty Cycle (DC)



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 14. Cycle-to-cycle Jitter

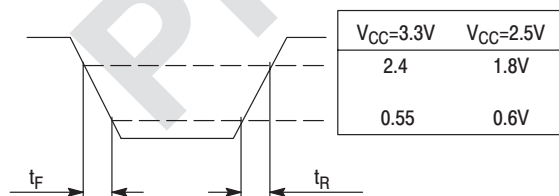


Figure 16. Output Transition Time Test Reference

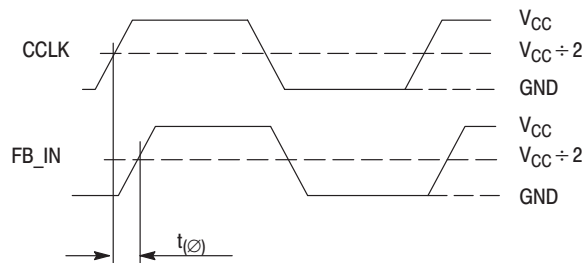
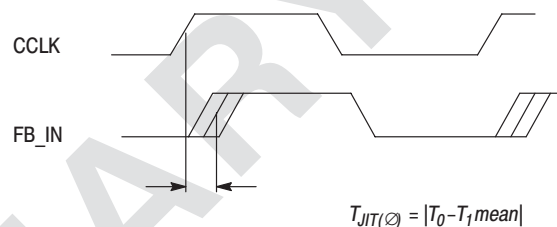
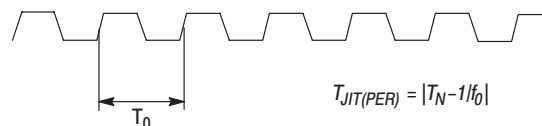


Figure 11. Propagation delay (t_{PD} , static phase offset) test reference



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 13. I/O Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 15. Period Jitter

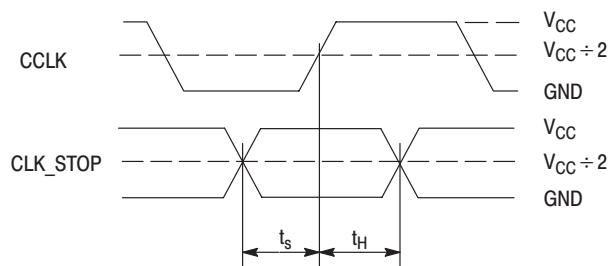


Figure 17. Setup and Hold Time (t_s , t_h) Test Reference

Low Voltage Zero Delay Buffer

The MPC961 is a 2.5V or 3.3V compatible, 1:18 PLL based zero delay buffer. With output frequencies of up to 200MHz, output skews of 150ps the device meets the needs of the most demanding clock tree applications.

- Fully Integrated PLL
- Up to 200MHz I/O Frequency
- LVCMOS Outputs
- Outputs Disable in High Impedance
- LVCMOS Reference Clock Options
- LQFP Packaging
- $\pm 50\text{ps}$ Cycle–Cycle Jitter
- 150ps Output Skews

The MPC961 is offered with two different input configurations. The MPC961C offers an LVCMOS reference clock while the MPC961P offers an LVPECL reference clock.

When pulled high the $\overline{\text{OE}}$ pin will force all of the outputs (except QFB) into a high impedance state. Because the $\overline{\text{OE}}$ pin does not affect the QFB output, down stream clocks can be disabled without the internal PLL losing lock.

The MPC961 is fully 2.5V or 3.3V compatible and requires no external loop filter components. All control inputs accept LVCMOS compatible levels and the outputs provide low impedance LVCMOS outputs capable of driving terminated 50Ω transmission lines. For series terminated lines the MPC961 can drive two lines per output giving the device an effective fanout of 1:36. The device is packaged in a 32 lead LQFP.

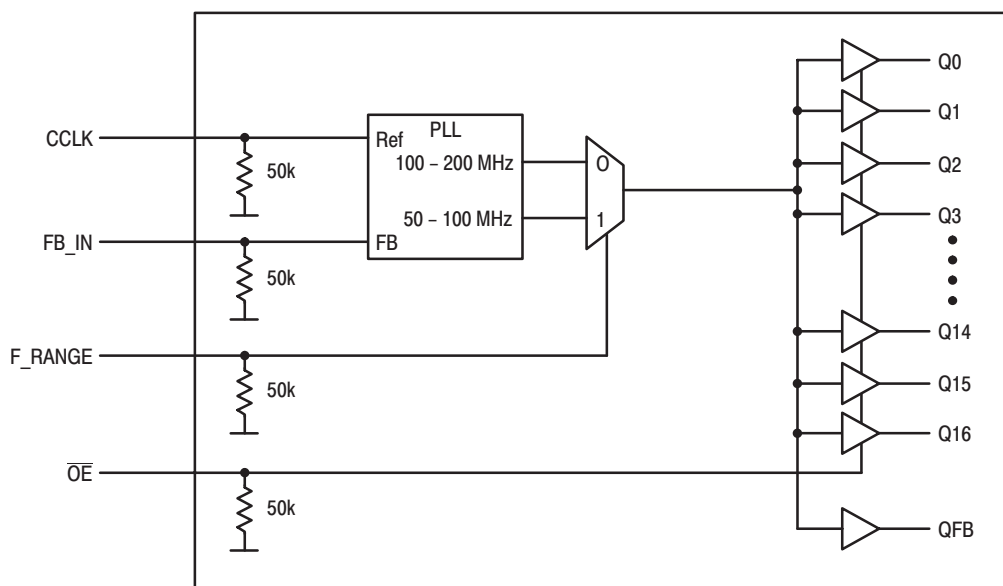
MPC961C

**LOW VOLTAGE
ZERO DELAY BUFFER**



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A

5



The MPC961C requires an external RC filter for the analog power supply pin V_{CCA} . Please see applications section for details.

Figure 1. MPC961C Logic Diagram

Rev 1

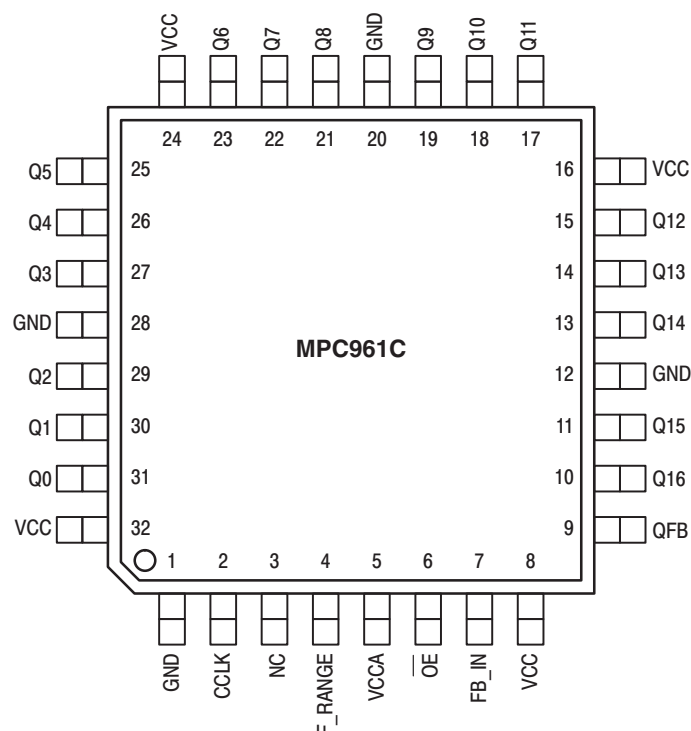


Figure 2. 32-Lead Pinout (Top View)

Table 1: PIN CONFIGURATIONS

Pin	I/O	Type	Function
CCLK	Input	LVC MOS	PLL reference clock signal
FB_IN	Input	LVC MOS	PLL feedback signal input, connect to a QFB output
F_RANGE	Input	LVC MOS	PLL frequency range select
OE	Input	LVC MOS	Output enable/disable
Q0 - Q16	Output	LVC MOS	Clock outputs
QFB	Output	LVC MOS	PLL feedback signal output, connect to a FB_IN
GND	Supply	Ground	Negative power supply
VCCA	Supply	VCC	PLL positive power supply (analog power supply). The MPC961C requires an external RC filter for the analog power supply pin VCCA. Please see applications section for details.
VCC	Supply	VCC	Positive power supply for I/O and core
NC			Not connected

Table 2: FUNCTION TABLE

Control	Default	0	1
F_RANGE	0	PLL high frequency range. MPC961C input reference and output clock frequency range is 100 – 200 MHz	PLL low frequency range. MPC961C input reference and output clock frequency range is 50 – 100 MHz
OE	0	Outputs enabled	Outputs disabled (high-impedance state)

Table 3: ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	3.6	V
V_{IN}	DC Input Voltage	-0.3	$V_{CC} + 0.3$	V
V_{OUT}	DC Output Voltage	-0.3	$V_{CC} + 0.3$	V
I_{IN}	DC Input Current		± 20	mA
I_{OUT}	DC Output Current		± 50	mA
T_S	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 4: DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ$ to 85°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input LOW Voltage	-0.3		0.8	V	LVC MOS
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -20\text{mA}^a$
V_{OL}	Output LOW Voltage			0.55	V	$I_{OL} = 20\text{mA}^a$
Z_{OUT}	Output Impedance		14	20	Ω	
I_{IN}	Input Current			± 120	μA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		8.0	10	pF	Per Output
I_{CCA}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current				mA	All VCC Pins
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	

a. The MPC961C is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up two 50Ω series terminated transmission lines.

Table 5: AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ$ to 85°C)^a

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{max}	Maximum Output Frequency F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{refDC}	Reference Input Duty Cycle	25		75	%	
t_r, t_f	TCLK Input Rise/Fall Time			3.0	ns	0.8 to 2.0V
$t(\phi)$	Propagation Delay (static phase offset) CCLK to FB_IN	-80		120	ps	PLL locked
$t_{sk(O)}$	Output-to-Output Skew ^b		90	150	ps	
DC_O	Output Duty Cycle F_RANGE = 0 F_RANGE = 1	42 45	50 50	55 55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ,HZ}$	Output Disable Time			10	ns	
$t_{PZL,LZ}$	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter RMS (1 σ) ^c			15	ps	
$t_{JIT(PER)}$	Period Jitter RMS (1 σ)		7.0	10	ps	
$t_{JIT(\phi)}$	I/O Phase Jitter RMS (1 σ)			15	ns	
t_{lock}	Maximum PLL Lock Time			10	ms	

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT}

b. See applications section for part-to-part skew calculation

c. See applications section for calculation for other confidence factors than 1 σ

Table 6: DC CHARACTERISTICS ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	1.7		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input LOW Voltage	-0.3		0.7	V	LVC MOS
V_{OH}	Output HIGH Voltage	1.8			V	$I_{OH} = -15mA^a$
V_{OL}	Output LOW Voltage			0.6	V	$I_{OL} = 15mA^a$
Z_{OUT}	Output Impedance		18	26	Ω	
I_{IN}	Input Current			± 120	μA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		8.0	10	pF	Per Output
I_{CCA}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current				mA	All VCC Pins
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	

a. The MPC961C is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up two 50 Ω series terminated transmission lines.

Table 7: AC CHARACTERISTICS ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)^a

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{max}	Maximum Output Frequency F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{refDC}	Reference Input Duty Cycle	25		75	%	
t_r, t_f	TCLK Input Rise/Fall Time			3.0	ns	0.7 to 1.7V
$t_{(\varnothing)}$	Propagation Delay (static phase offset) CCLK to FB_IN	-80		120	ps	PLL locked
$t_{sk(O)}$	Output-to-Output Skew ^b		90	150	ps	
DCO	Output Duty Cycle F_RANGE = 0 F_RANGE = 1	40 45	50 50	60 55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.6 to 1.8V
$t_{PLZ,HZ}$	Output Disable Time			10	ns	
$t_{PZL,LZ}$	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter RMS (1 σ) ^c			15	ps	
$t_{JIT(PER)}$	Period Jitter RMS (1 σ)		7.0	10	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter RMS (1 σ)			15	ns	
t_{lock}	Maximum PLL Lock Time			10	ms	

a. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}

b. See applications section for part-to-part skew calculation

c. See applications section for calculation for other confidence factors than 1 σ

Power Supply Filtering

The MPC961C is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC961C provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC961C.

Figure 3 illustrates a typical power supply filter scheme. The MPC961C is most susceptible to noise with spectral content in the 10kHz to 10MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the MPC961C. From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 2mA (5mA maximum), assuming that a minimum of 2.375V ($V_{CC} = 3.3V$ or $V_{CC} = 2.5V$) must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 3 must have a resistance of 270 Ω ($V_{CC} = 3.3V$) or 5 to 15 Ω ($V_{CC} = 2.5V$) to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20kHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

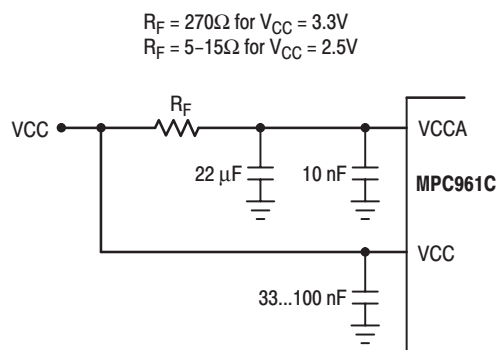


Figure 3. Power Supply Filter

Although the MPC961C has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC961C clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 15 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091.

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC961C clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fan-out of the MPC961C clock driver is effectively doubled due to its capability to drive multiple lines.

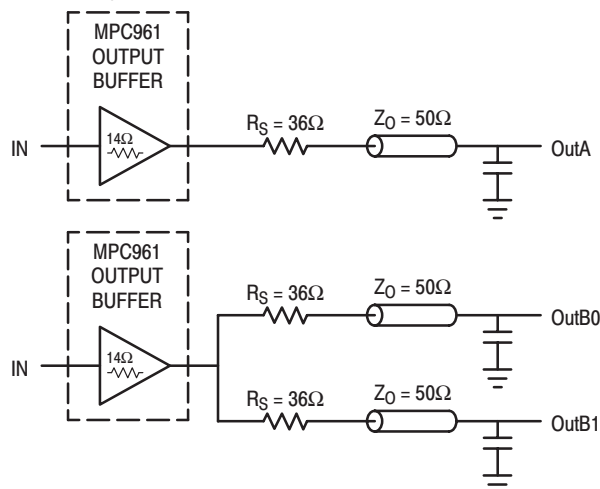


Figure 4. Single versus Dual Transmission Lines

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC961C output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC961C. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned}
 V_L &= V_S (Z_o / (R_s + R_o + Z_o)) \\
 Z_o &= 50\Omega \parallel 50\Omega \\
 R_s &= 36\Omega \parallel 36\Omega \\
 R_o &= 14\Omega \\
 V_L &= 3.0 (25 / (18 + 14 + 25) = 3.0 (25 / 57) \\
 &= 1.31V
 \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.62V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

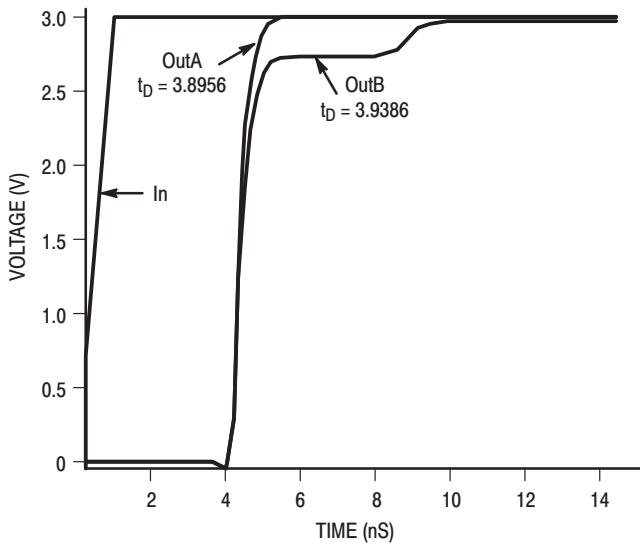


Figure 5. Single versus Dual Waveforms

5

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

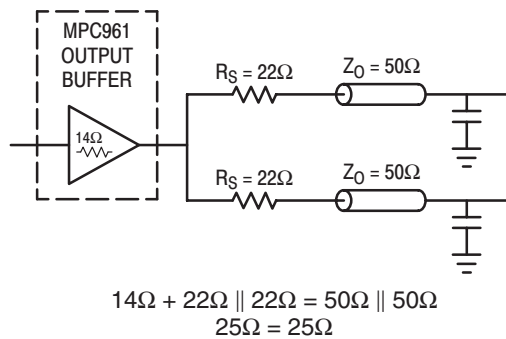


Figure 6. Optimized Dual Line Termination

SPICE level and IBIS output buffer models are available for engineers who want to simulate their specific interconnect schemes.

Using the MPC961C in zero-delay applications

Nested clock trees are typical applications for the MPC961C. Designs using the MPC961C as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC961C clock driver allows for its use as a zero delay buffer. By using the QFB output as a feedback to the PLL the propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of part-to-part skew

The MPC961C zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC961C are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\emptyset)} + t_{SK(O)} + t_{PD, LINE(FB)} + t_{JIT(\emptyset)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

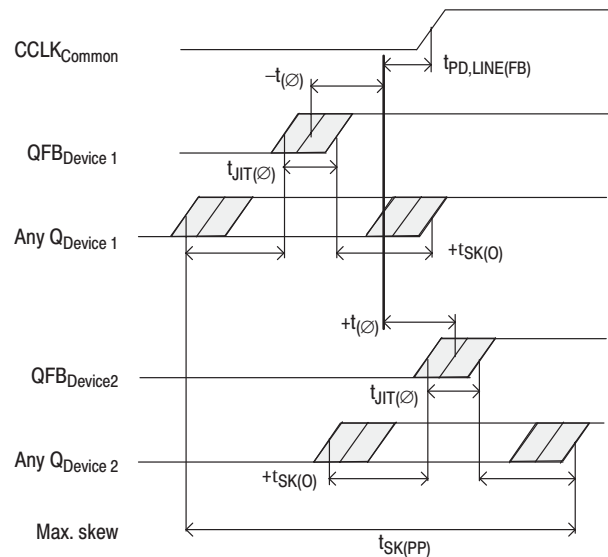


Figure 7. MPC961C max. device-to-device skew

Due to the statistical nature of I/O jitter a rms value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

Table 8: Confidence Factor CF

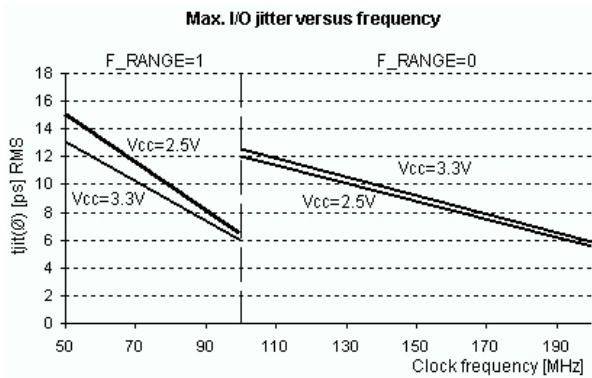
CF	Probability of clock edge within the distribution
$\pm 1\sigma$	0.68268948
$\pm 2\sigma$	0.95449988
$\pm 3\sigma$	0.99730007
$\pm 4\sigma$	0.99993663
$\pm 5\sigma$	0.99999943
$\pm 6\sigma$	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% ($\pm 3\sigma$) is assumed, resulting in a worst case timing uncertainty from input to any output of -275 ps to 315 ps relative to CCLK:

$$t_{SK(PP)} = [-80ps...120ps] + [-150ps...150ps] + [(15ps \cdot -3)...(15ps \cdot 3)] + t_{PD, LINE(FB)}$$

$$t_{SK(PP)} = [-275ps...315ps] + t_{PD, LINE(FB)}$$

Due to the frequency dependence of the I/O jitter, Figure 8 “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis.

**Figure 8. Max. I/O Jitter versus frequency**

Power Consumption of the MPC961C and Thermal Management

The MPC961C AC specification is guaranteed for the entire operating frequency range up to 200 MHz. The MPC961C power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage,

output loading, ambient temperature, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the MPC961C die junction temperature and the associated device reliability. For a complete analysis of power consumption as a function of operating conditions and associated long term device reliability please refer to the application note AN1545. According the AN1545, the long-term device reliability is a function of the die junction temperature:

Table 9: Die junction temperature and MTBF

Junction temperature (°C)	MTBF (Years)
100	20.4
110	9.1
120	4.2
130	2.0

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the MPC961C needs to be controlled and the thermal impedance of the board/package should be optimized. The power dissipated in the MPC961C is represented in equation 1.

Where I_{CCQ} is the static current consumption of the MPC961C, C_{PD} is the power dissipation capacitance per output, $(M)\Sigma C_L$ represents the external capacitive output load, N is the number of active outputs (N is always 27 in case of the MPC961C). The MPC961C supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore, ΣC_L is zero for controlled transmission line systems and can be eliminated from equation 1. Using parallel termination output termination results in equation 2 for power dissipation.

In equation 2, P stands for the number of outputs with a parallel or thevenin termination, V_{OL} , I_{OL} , V_{OH} and I_{OH} are a function of the output termination technique and DC_Q is the clock signal duty cycle. If transmission lines are used ΣC_L is zero in equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature T_J as a function of the power consumption.

$$P_{TOT} = \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_M C_L \right) \right] \cdot V_{CC} \quad \text{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_M C_L \right) \right] + \sum_P \left[DC_Q \cdot I_{OH} \cdot (V_{CC} - V_{OH}) + (1 - DC_Q) \cdot I_{OL} \cdot V_{OL} \right] \quad \text{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \quad \text{Equation 3}$$

$$f_{CLOCK,MAX} = \frac{1}{C_{PD} \cdot N \cdot V_{CC}^2} \cdot \left[\frac{T_{J,MAX} - T_A}{R_{thja}} - (I_{CCQ} \cdot V_{CC}) \right] \quad \text{Equation 4}$$

Where R_{thja} is the thermal impedance of the package (junction to ambient) and T_A is the ambient temperature. According to Table 9, the junction temperature can be used to estimate the long-term device reliability. Further, combining equation 1 and equation 2 results in a maximum operating frequency for the MPC961C in a series terminated transmission line system.

Table 10: Thermal package impedance of the 32ld LQFP

Convection, LFPM	R_{thja} (1P2S board), K/W
Still air	80
100 lfpm	70
200 lfpm	61
300 lfpm	57
400 lfpm	56
500 lfpm	55

$T_{J,MAX}$ should be selected according to the MTBF system requirements and Table 9. R_{thja} can be derived from Table 10. The R_{thja} represent data based on 1S2P boards, using 2S2P boards will result in a lower thermal impedance than indicated below.

If the calculated maximum frequency is below 200 MHz, it becomes the upper clock speed limit for the given application conditions. The following two derating charts describe the safe frequency operation range for the MPC961C. The charts were calculated for a maximum tolerable die junction temperature of 110°C, corresponding to an estimated MTBF of 9.1 years, a supply voltage of 3.3V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made. There are no operating frequency limitations if a 2.5V power supply or the system specifications allow for a MTBF of 4 years (corresponding to a max. junction temperature of 120°C).

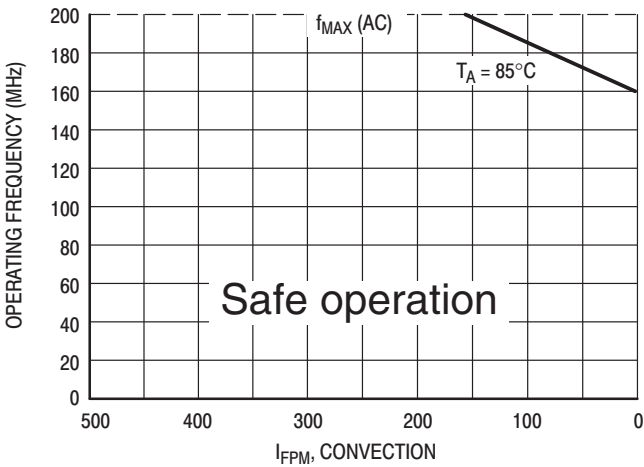


Figure 9. Maximum MPC961C frequency, $V_{CC} = 3.3V$, MTBF 9.1 years, driving series terminated transmission lines

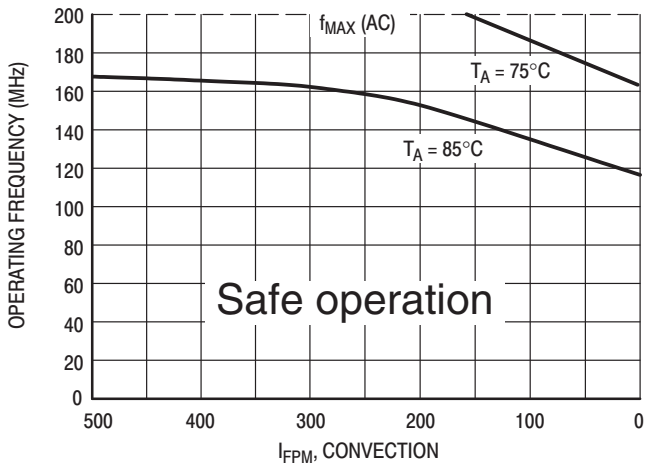


Figure 10. Maximum MPC961C frequency, $V_{CC} = 3.3V$, MTBF 9.1 years, 4 pF load per line

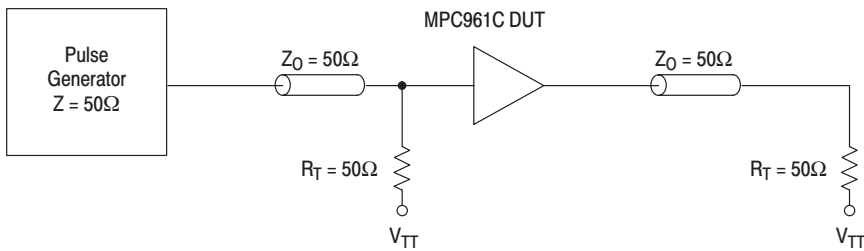
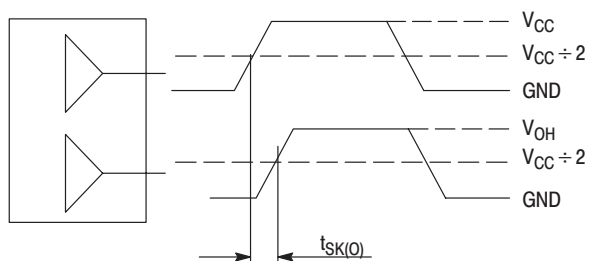
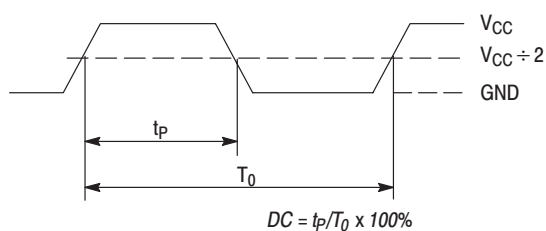


Figure 11. TCLK MPC961C AC test reference for $V_{CC} = 3.3V$ and $V_{CC} = 2.5V$



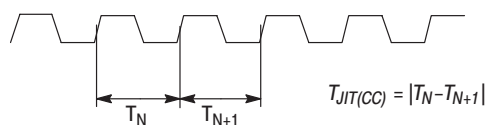
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 12. Output-to-output Skew $t_{SK(O)}$



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 14. Output Duty Cycle (DC)



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 16. Cycle-to-cycle Jitter

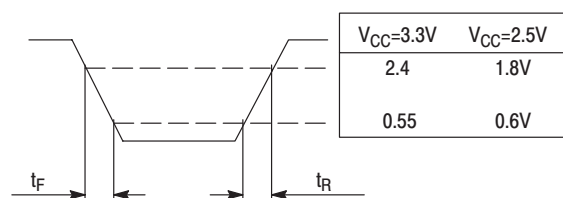


Figure 18. Output Transition Time Test Reference

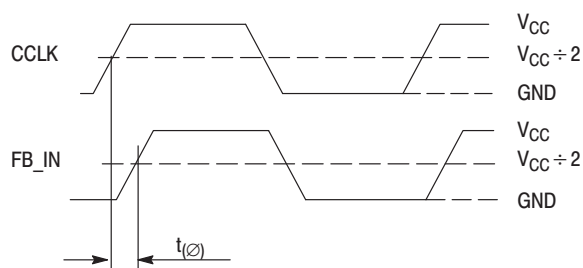
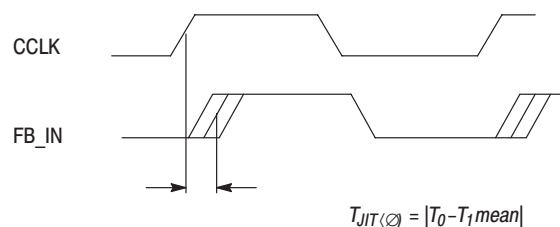
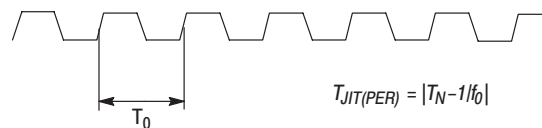


Figure 13. Propagation delay (t_{PD} , static phase offset) test reference



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 15. I/O Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 17. Period Jitter

Low Voltage Zero Delay Buffer

The MPC961 is a 2.5V or 3.3V compatible, 1:18 PLL based zero delay buffer. With output frequencies of up to 200MHz, output skews of 150ps the device meets the needs of the most demanding clock tree applications.

- Fully Integrated PLL
- Up to 200MHz I/O Frequency
- LVCMOS Outputs
- Outputs Disable in High Impedance
- LVPECL Reference Clock Options
- LQFP Packaging
- $\pm 50\text{ps}$ Cycle–Cycle Jitter
- 150ps Output Skews

The MPC961 is offered with two different input configurations. The MPC961C offers an LVCMOS reference clock while the MPC961P offers an LVPECL reference clock.

When pulled high the $\overline{\text{OE}}$ pin will force all of the outputs (except QFB) into a high impedance state. Because the $\overline{\text{OE}}$ pin does not affect the QFB output, down stream clocks can be disabled without the internal PLL losing lock.

The MPC961 is fully 2.5V or 3.3V compatible and requires no external loop filter components. All control inputs accept LVCMOS compatible levels and the outputs provide low impedance LVCMOS outputs capable of driving terminated 50Ω transmission lines. For series terminated lines the MPC961 can drive two lines per output giving the device an effective fanout of 1:36. The device is packaged in a 32 lead LQFP package to provide the optimum combination of board density and performance.

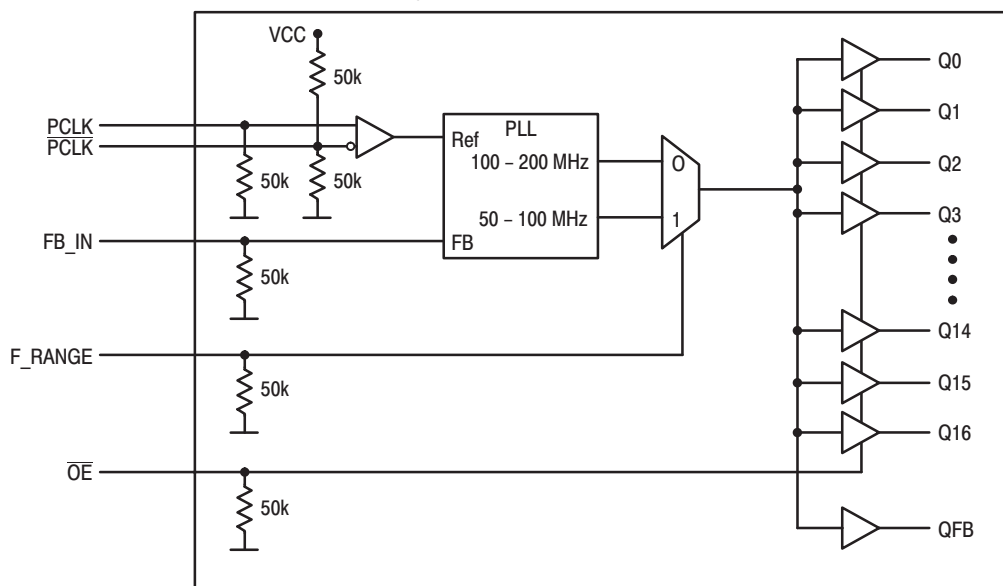
MPC961P

**LOW VOLTAGE
ZERO DELAY BUFFER**



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A

5



The MPC961P requires an external RC filter for the analog power supply pin V_{CCA} . Please see applications section for details.

Figure 1. MPC961P Logic Diagram

Rev 2

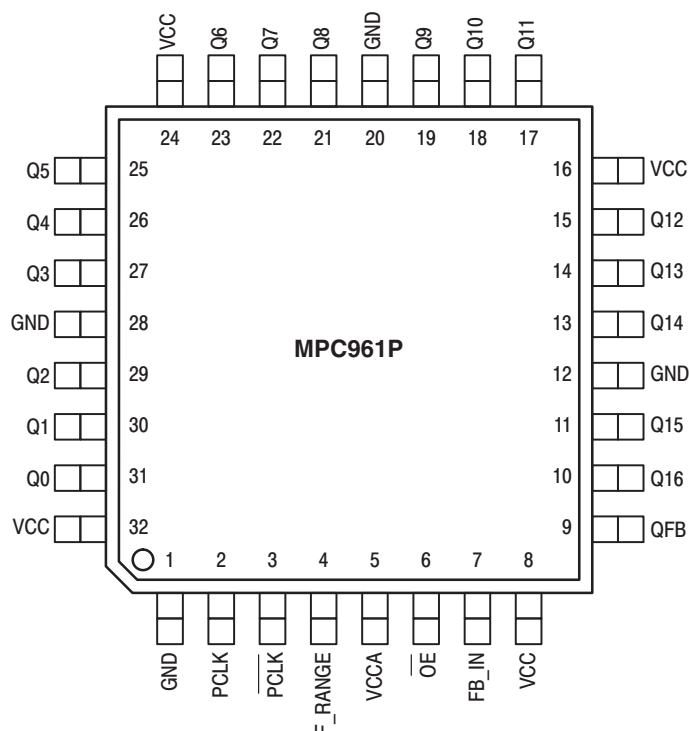


Figure 2. 32-Lead Pinout (Top View)

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Table 1: PIN CONFIGURATIONS

Pin	I/O	Type	Function
PCLK, $\overline{\text{PCLK}}$	Input	LVC MOS	PLL reference clock signal
FB_IN	Input	LVC MOS	PLL feedback signal input, connect to a QFB output
F_RANGE	Input	LVC MOS	PLL frequency range select
$\overline{\text{OE}}$	Input	LVC MOS	Output enable/disable
Q0 - Q16	Output	LVC MOS	Clock outputs
QFB	Output	LVC MOS	PLL feedback signal output, connect to a FB_IN
GND	Supply	Ground	Negative power supply
VCCA	Supply	VCC	PLL positive power supply (analog power supply). The MPC961P requires an external RC filter for the analog power supply pin VCCA. Please see applications section for details.
VCC	Supply	VCC	Positive power supply for I/O and core

Table 2: FUNCTION TABLE

Control	Default	0	1
F_RANGE	0	PLL high frequency range. MPC961P input reference and output clock frequency range is 100 – 200 MHz	PLL low frequency range. MPC961P input reference and output clock frequency range is 50 – 100 MHz
$\overline{\text{OE}}$	0	Outputs enabled	Outputs disabled (high-impedance state)

Table 3: ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	3.6	V
V_{IN}	DC Input Voltage	-0.3	$V_{CC} + 0.3$	V
V_{OUT}	DC Output Voltage	-0.3	$V_{CC} + 0.3$	V
I_{IN}	DC Input Current		± 20	mA
I_{OUT}	DC Output Current		± 50	mA
T_S	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 4: DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ$ to 85°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input LOW Voltage	-0.3		0.8	V	LVC MOS
V_{PP}	Peak-to-peak input voltage ^a PECL_CLK, $\overline{\text{PECL\_CLK}}$	500		1000	mV	LVPECL
V_{CMR}	Common Mode Range ^a PECL_CLK, $\overline{\text{PECL\_CLK}}$	1.2		$V_{CC} - 0.8$	V	LVPECL
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -20\text{mA}^b$
V_{OL}	Output LOW Voltage			0.55	V	$I_{OL} = 20\text{mA}^b$
Z_{OUT}	Output Impedance		14	20	Ω	
I_{IN}	Input Current			± 120	μA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		8.0	10	pF	Per Output
I_{CCA}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current				mA	All VCC Pins
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	

a. Exceeding the specified V_{CMR}/V_{PP} window results in a t_{PD} changes of approx. 250 ps.

b. The MPC961P is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up two 50Ω series terminated transmission lines.

Table 5: AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)^a

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{max}	Maximum Output Frequency F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{refDC}	Reference Input Duty Cycle	25		75	%	
$t_{(\varnothing)}$	Propagation Delay ^b (static phase offset) PECL_CLK to FB_IN	-50		225	ps	PLL locked
$t_{sk(O)}$	Output-to-Output Skew ^c		90	150	ps	
DC _O	Output Duty Cycle F_RANGE = 0 F_RANGE = 1	42 45	50 50	55 55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ,HZ}$	Output Disable Time			10	ns	
$t_{PZL,LZ}$	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter RMS (1 σ) ^d			15	ps	
$t_{JIT(PEP)}$	Period Jitter RMS (1 σ)		7.0	10	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter RMS (1 σ) F_RANGE = 0 F_RANGE = 1			$0.0015 \cdot T$ $0.0010 \cdot T$	ns	T = Clock Signal Period
t_{lock}	Maximum PLL Lock Time			10	ms	

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT}

b. t_{PD} applies for $V_{CMR} = V_{CC} - 1.3V$ and $V_{PP} = 800mV$

c. See applications section for part-to-part skew calculation

d. See applications section for calculation for other confidence factors than 1 σ

Table 6: DC CHARACTERISTICS ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	1.7		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input LOW Voltage	-0.3		0.7	V	LVC MOS
V_{PP}	Peak-to-peak input voltage ^a PECL_CLK, PECL_CLK	500		1000	mV	LVPECL
V_{CMR}	Common Mode Range ^a PECL_CLK, PECL_CLK	1.2		$V_{CC} - 0.7$	V	LVPECL
V_{OH}	Output HIGH Voltage	1.8			V	$I_{OH} = -15mA^b$
V_{OL}	Output LOW Voltage			0.6	V	$I_{OL} = 15mA^b$
Z_{OUT}	Output Impedance		18	26	Ω	
I_{IN}	Input Current			± 120	μA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		8.0	10	pF	Per Output
I_{CCA}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current				mA	All VCC Pins
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	

a. Exceeding the specified V_{CMR}/V_{PP} window results in a t_{PD} changes < 250 ps.

b. The MPC961P is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up two 50Ω series terminated transmission lines.

Table 7: AC CHARACTERISTICS ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)^a

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{max}	Maximum Output Frequency F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{refDC}	Reference Input Duty Cycle	25		75	%	
$t_{(\phi)}$	Propagation Delay ^b (static phase offset) PCLK to FB_IN	-50		175	ps	PLL locked
$t_{sk(O)}$	Output-to-Output Skew ^c		90	150	ps	
DC _O	Output Duty Cycle F_RANGE = 0 F_RANGE = 1	40 45	50 50	60 55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.6 to 1.8V
$t_{PLZ,HZ}$	Output Disable Time			10	ns	
$t_{PZL,LZ}$	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter RMS (1 σ) ^d			15	ps	
$t_{JIT(PER)}$	Period Jitter RMS (1 σ)		7.0	10	ps	
$t_{JIT(\phi)}$	I/O Phase Jitter RMS (1 σ) F_RANGE = 0 F_RANGE = 1			$0.0015 \cdot T$ $0.0010 \cdot T$	ns	T = Clock Signal Period
t_{lock}	Maximum PLL Lock Time			10	ms	

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT}

b. t_{PD} applies for $V_{CMR} = V_{CC} - 1.3V$ and $V_{PP} = 800mV$

c. See applications section for part-to-part skew calculation

d. See applications section for calculation for other confidence factors than 1 σ

Power Supply Filtering

The MPC961P is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC961P provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC961P.

Figure 3 illustrates a typical power supply filter scheme. The MPC961P is most susceptible to noise with spectral content in the 10kHz to 5MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the MPC961P. From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 2mA (5mA maximum), assuming that a minimum of 2.375V ($V_{CC} = 3.3V$ or $V_{CC} = 2.5V$) must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 3 must have a resistance of 270 Ω ($V_{CC} = 3.3V$) or 5 to 15 Ω ($V_{CC} = 2.5V$) to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20kHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

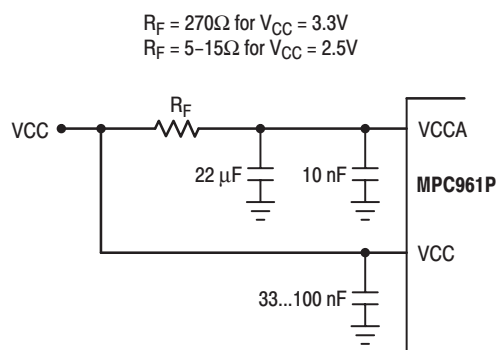


Figure 3. Power Supply Filter

Although the MPC961P has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC961P clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 15 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091.

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC961P clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fan-out of the MPC961P clock driver is effectively doubled due to its capability to drive multiple lines.

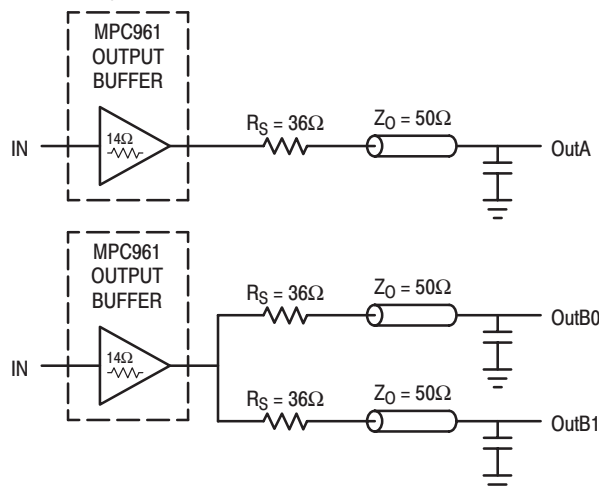


Figure 4. Single versus Dual Transmission Lines

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC961P output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC961P. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned}
 V_L &= V_S (Z_o / (R_s + R_o + Z_o)) \\
 Z_o &= 50\Omega \parallel 50\Omega \\
 R_s &= 36\Omega \parallel 36\Omega \\
 R_o &= 14\Omega \\
 V_L &= 3.0 (25 / (18 + 14 + 25)) = 3.0 (25 / 57) \\
 &= 1.31V
 \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.62V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

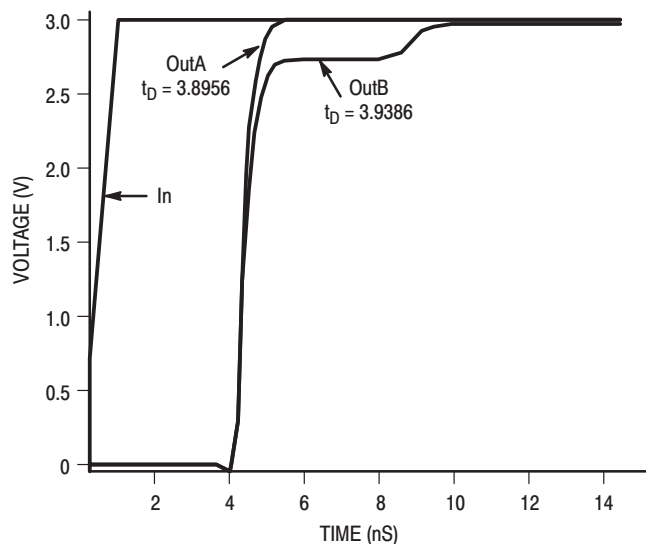


Figure 5. Single versus Dual Waveforms

5

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

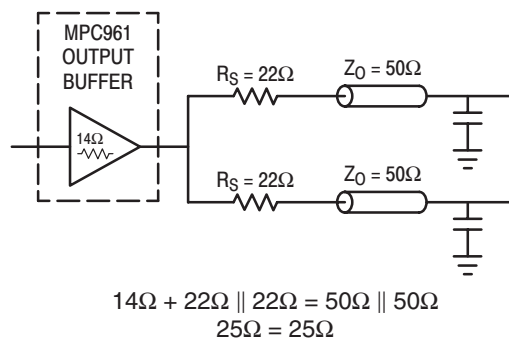


Figure 6. Optimized Dual Line Termination

SPICE level and IBIS output buffer models are available for engineers who want to simulate their specific interconnect schemes.

Using the MPC961P in zero-delay applications

Nested clock trees are typical applications for the MPC961P. Designs using the MPC961P as LVCMOS PLL fan-out buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fan-out buffers. The external feedback option of the MPC961P clock driver allows for its use as a zero delay buffer. By using the QFB output as a feedback to the PLL the propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of part-to-part skew

The MPC961P zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC961P are connected together, the maximum overall timing uncertainty from the common PCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD, LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

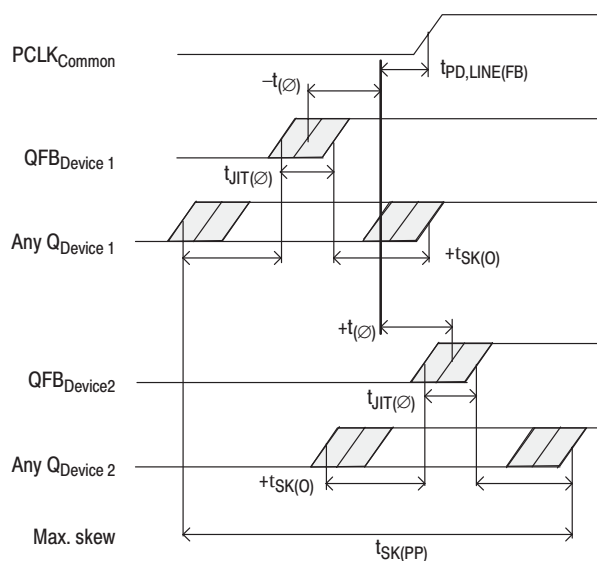


Figure 7. MPC961P max. device-to-device skew

Due to the statistical nature of I/O jitter a rms value (1σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

Table 8: Confidence Factor CF

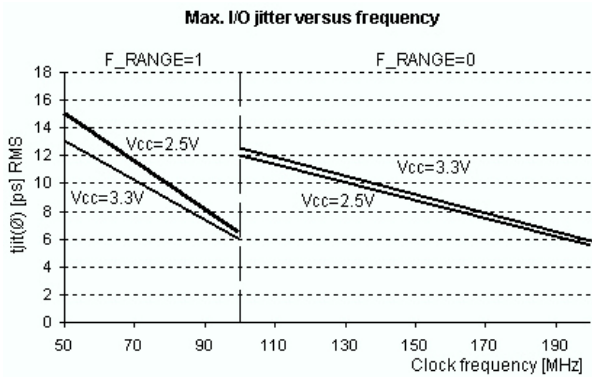
CF	Probability of clock edge within the distribution
$\pm 1\sigma$	0.68268948
$\pm 2\sigma$	0.95449988
$\pm 3\sigma$	0.99730007
$\pm 4\sigma$	0.99993663
$\pm 5\sigma$	0.99999943
$\pm 6\sigma$	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% ($\pm 3\sigma$) is assumed, resulting in a worst case timing uncertainty from input to any output of -236 ps to 361 ps relative to PCLK ($f=125$ MHz, $V_{CC}=2.5$ V):

$$t_{SK(PP)} = [-50ps...175ps] + [-150ps...150ps] + [(12ps \cdot -3)...(12ps \cdot 3)] + t_{PD, LINE(FB)}$$

$$t_{SK(PP)} = [-236ps...361ps] + t_{PD, LINE(FB)}$$

Due to the frequency dependence of the I/O jitter, Figure 8 “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis.

**Figure 8. Max. I/O Jitter versus frequency**

Power Consumption of the MPC961P and Thermal Management

The MPC961P AC specification is guaranteed for the entire operating frequency range up to 200 MHz. The MPC961P power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperature, vertical convection and

thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the MPC961P die junction temperature and the associated device reliability. For a complete analysis of power consumption as a function of operating conditions and associated long term device reliability please refer to the application note AN1545. According the AN1545, the long-term device reliability is a function of the die junction temperature:

Table 9: Die junction temperature and MTBF

Junction temperature (°C)	MTBF (Years)
100	20.4
110	9.1
120	4.2
130	2.0

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the MPC961P needs to be controlled and the thermal impedance of the board/package should be optimized. The power dissipated in the MPC961P is represented in equation 1.

Where I_{CCQ} is the static current consumption of the MPC961P, C_{PD} is the power dissipation capacitance per output, $(M)\Sigma C_L$ represents the external capacitive output load, N is the number of active outputs (N is always 27 in case of the MPC961P). The MPC961P supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore, ΣC_L is zero for controlled transmission line systems and can be eliminated from equation 1. Using parallel termination output termination results in equation 2 for power dissipation.

In equation 2, P stands for the number of outputs with a parallel or thevenin termination, V_{OL} , I_{OL} , V_{OH} and I_{OH} are a function of the output termination technique and DC_Q is the clock signal duty cycle. If transmission lines are used ΣC_L is zero in equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature T_J as a function of the power consumption.

$$P_{TOT} = \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_M C_L \right) \right] \cdot V_{CC} \quad \text{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_M C_L \right) \right] + \sum_P [DC_Q \cdot I_{OH} \cdot (V_{CC} - V_{OH}) + (1 - DC_Q) \cdot I_{OL} \cdot V_{OL}] \quad \text{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \quad \text{Equation 3}$$

$$f_{CLOCK,MAX} = \frac{1}{C_{PD} \cdot N \cdot V_{CC}^2} \cdot \left[\frac{T_{J,MAX} - T_A}{R_{thja}} - (I_{CCQ} \cdot V_{CC}) \right] \quad \text{Equation 4}$$

Where R_{thja} is the thermal impedance of the package (junction to ambient) and T_A is the ambient temperature. According to Table 9, the junction temperature can be used to estimate the long-term device reliability. Further, combining equation 1 and equation 2 results in a maximum operating frequency for the MPC961P in a series terminated transmission line system.

Table 10: Thermal package impedance of the 32ld LQFP

Convection, LFPM	R_{thja} (1P2S board), K/W
Still air	80
100 lfpm	70
200 lfpm	61
300 lfpm	57
400 lfpm	56
500 lfpm	55

$T_{J,MAX}$ should be selected according to the MTBF system requirements and Table 9. R_{thja} can be derived from Table 10. The R_{thja} represent data based on 1S2P boards, using 2S2P boards will result in a lower thermal impedance than indicated below.

If the calculated maximum frequency is below 200 MHz, it becomes the upper clock speed limit for the given application conditions. The following two derating charts describe the safe frequency operation range for the MPC961P. The charts were calculated for a maximum tolerable die junction temperature of 110°C, corresponding to an estimated MTBF of 9.1 years, a supply voltage of 3.3V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made. There are no operating frequency limitations if a 2.5V power supply or the system specifications allow for a MTBF of 4 years (corresponding to a max. junction temperature of 120°C).

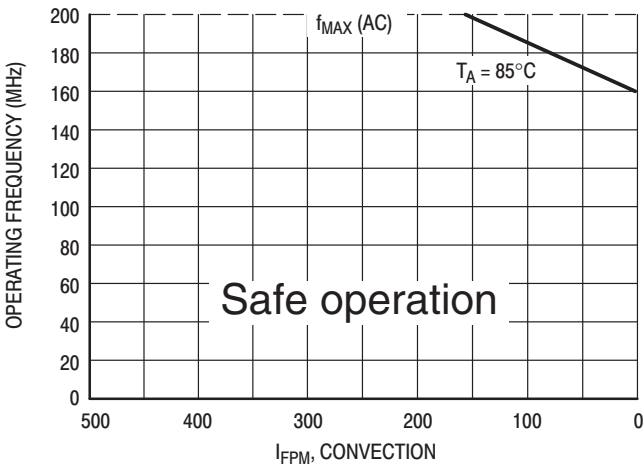


Figure 9. Maximum MPC961P frequency, $V_{CC} = 3.3V$, MTBF 9.1 years, driving series terminated transmission lines

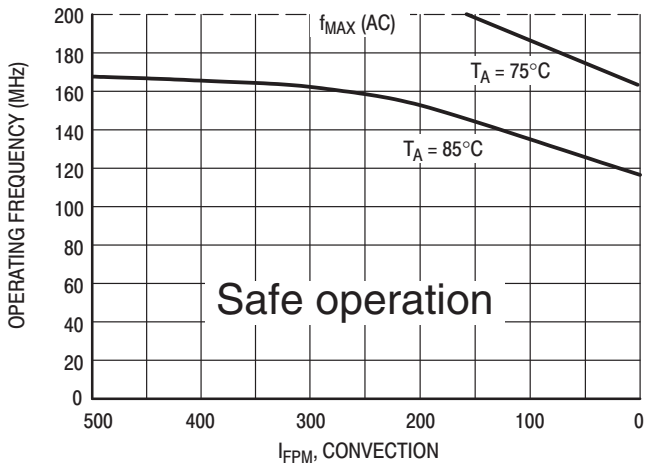


Figure 10. Maximum MPC961P frequency, $V_{CC} = 3.3V$, MTBF 9.1 years, 4 pF load per line

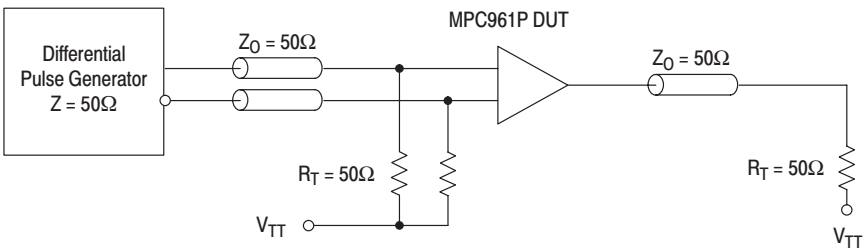


Figure 11. TCLK MPC961P AC test reference for $V_{CC} = 3.3V$ and $V_{CC} = 2.5V$

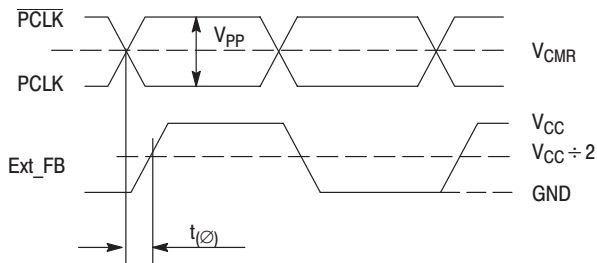


Figure 12. Propagation delay (t_{ϕ}), static phase offset) test reference

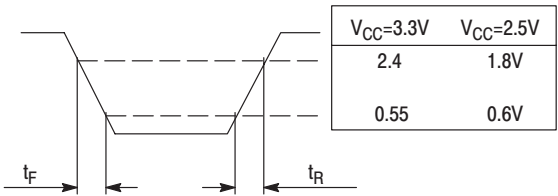
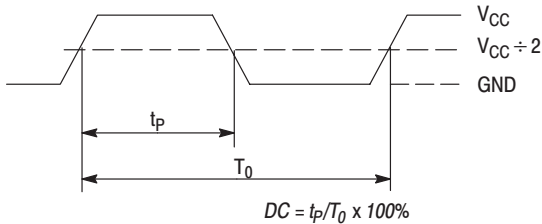
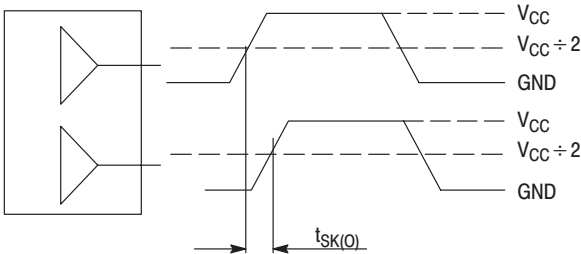


Figure 13. Output Transition Time Test Reference



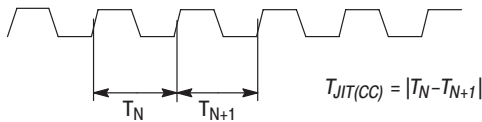
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 14. Output Duty Cycle (DC)



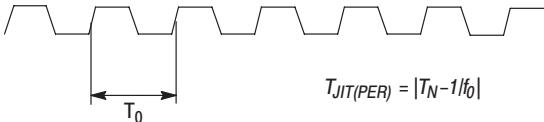
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 15. Output-to-output Skew $t_{SK(O)}$



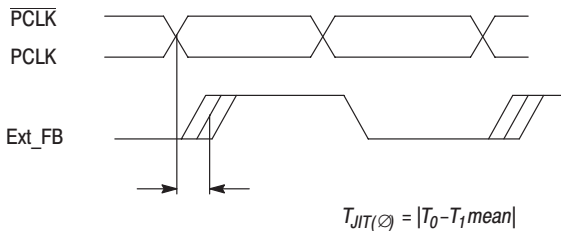
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 16. Cycle-to-cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 17. Period Jitter



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 18. I/O Jitter

Low-Cost 3.3V Zero Delay Buffer

The MPC962309 is a zero delay buffer designed to distribute high-speed clocks. Available in a 16-pin SOIC or TSSOP package, the device accepts one reference input and drives nine low-skew clocks. The MPC962305 is the 8-pin version of the MPC962309 which drives five outputs with one reference input. The -1H versions of these devices have higher drive than the -1 devices and can operate up to 100/133 MHz frequencies. These parts have on-chip PLLs which lock to an input clock presented on the REF pin. The PLL feedback is on-chip and is obtained from the CLOCKOUT pad.

Features

- 1:5 LVCMOS zero-delay buffer (MPC962305)
- 1:9 LVCMOS zero-delay buffer (MPC962309)
- Zero input-output propagation delay
- Multiple low-skew outputs
 - 250 ps max output-output skew
 - 700 ps max device-device skew
- Supports a clock I/O frequency range of 10MHz to 133MHz, compatible with CPU and PCI bus frequencies
- Low jitter, 200 ps max cycle-cycle, and compatible with Pentium®-based systems
- Test Mode to bypass PLL (MPC962309 only. See "Select Input Decoding" on page 2)
- 8-pin SOIC or 8-pin TSSOP package (MPC962305); 16-pin SOIC or 16-pin TSSOP package (MPC962309)
- Single 3.3V supply
- Ambient temperature range: -40°C to +85°C
- Compatible with the CY2305, CY23S05, CY2309, CY23S09
- Spread spectrum compatible

Functional Description

The MPC962309 has two banks of four outputs each, which can be controlled by the Select Inputs as shown in the "Select Input Decoding" table. Bank B can be tri-stated if all of the outputs are not required. Select inputs also allow the input clock to be directly applied to the outputs for chip and system testing purposes.

The MPC962305 and MPC962309 PLLs enter a power down state when there are no rising edges on the REF input. During this state, all of the outputs are in tristate, the PLL is turned off, and there is less than 25.0 μ A of current draw for the device. The PLL shuts down in one additional case as shown in the "Select Input Decoding" table.

Multiple MPC962305 and MPC962309 devices can accept the same input clock and distribute it throughout the system. In this situation, the difference between the output skews of two devices will be less than 700 ps.

All outputs have less than 200 ps of cycle-cycle jitter. The input-to-output propagation delay on both devices is guaranteed to be less than 350 ps and the output-to-output skew is guaranteed to be less than 250 ps.

The MPC962305 and MPC962309 are available in two/three different configurations, as shown on the ordering information page. The MPC962305-1/MPC962309-1 are the base parts. High drive versions of those devices, MPC962305-1H and MPC962309-1H, are available to provide faster rise and fall times of the base device.

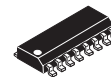
MPC962305 MPC962309



D SUFFIX
8 LEAD SOIC PACKAGE
CASE 751



DT SUFFIX
8 LEAD TSSOP PACKAGE
CASE 948J

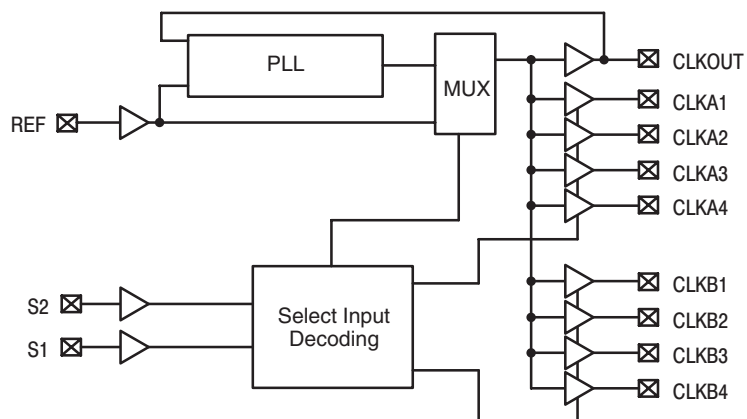


D SUFFIX
16 LEAD SOIC PACKAGE
CASE 751B



DT SUFFIX
16 LEAD TSSOP PACKAGE
CASE 948F

Block Diagram



Pin Configuration

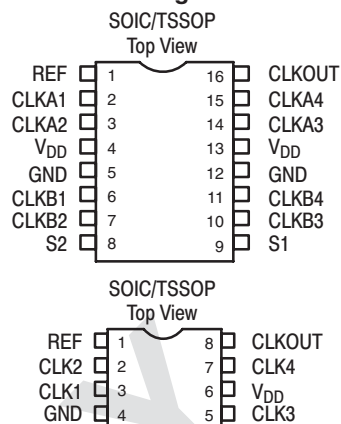


Table 1. Pin Description for MPC962309

Pin	Signal	Description
1	REF ^[1]	Input reference frequency, 5V–tolerant input
2	CLKA1 ^[2]	Buffered clock output, Bank A
3	CLKA2 ^[2]	Buffered clock output, Bank A
4	V _{DD}	3.3V supply
5	GND	Ground
6	CLKB1 ^[2]	Buffered clock output, Bank B
7	CLKB2 ^[2]	Buffered clock output, Bank B
8	S2 ^[3]	Select input, bit 2
9	S1 ^[3]	Select input, bit 1
10	CLKB3 ^[2]	Buffered clock output, Bank B
11	CLKB4 ^[2]	Buffered clock output, Bank B
12	GND	Ground
13	V _{DD}	3.3V supply
14	CLKA3 ^[2]	Buffered clock output, Bank A
15	CLKA4 ^[2]	Buffered clock output, Bank A
16	CLKOUT ^[2]	Buffered output, internal feedback on this pin

Table 2. Pin Description for MPC962305

Pin	Signal	Description
1	REF ^[1]	Input reference frequency, 5V–tolerant input
2	CLK2 ^[2]	Buffered clock output
3	CLK1 ^[2]	Buffered clock output
4	GND	Ground
5	CLK3 ^[2]	Buffered clock output
6	V _{DD}	3.3V supply
7	CLK4 ^[2]	Buffered clock output
8	CLKOUT ^[2]	Buffered clock output, internal feedback on this pin

NOTE:

- 1 Weak pull–down.
- 2 Weak pull–down on all outputs.
- 3 Weak pull–ups on these inputs.

Table 3. Select Input Decoding for MPC962309

S2	S1	CLOCK A1–A4	CLOCK B1–B4	CLKOUT ^[4]	Output Source	PLL Shutdown
0	0	Three–State	Three–State	Driven	PLL	N
0	1	Driven	Three–State	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

NOTE:

- 4 This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and output.

Table 4. Maximum Ratings

Characteristics	Value	Unit
Supply Voltage to Ground Potential	–0.5 to +4.6	V
DC Input Voltage (Except Ref)	–0.5 to $V_{DD}+0.5$	V
DC Input Voltage REF	–0.5 to 5.5	V
Storage Temperature	–65 to +150	°C
Junction Temperature	150	°C
Static Discharge Voltage (per MIL–STD–883, Method 3015)	>2000	V

Table 5. Operating Conditions for MPC962305–XX and MPC962309–XX Industrial Temperature Devices

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	–40	85	°C
C_L	Load Capacitance, below 100 MHz		30	pF
C_L	Load Capacitance, from 100 MHz to 133 MHz		10	pF
C_{IN}	Input Capacitance		7	pF

Table 6. Electrical Characteristics for MPC962305–XX and MPC962309–XX Industrial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage ^[5]			0.8	V
V_{IH}	Input HIGH Voltage ^[5]		2.0		V
I_{IL}	Input LOW Current	$V_{IN} = 0V$		50.0	μA
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$		100.0	μA
V_{OL}	Output LOW Voltage	$I_{OL} = 8\text{ mA (–1)}$ $I_{OH} = 12\text{ mA (–1H)}$		0.4	V
V_{OH}	Output HIGH Voltage	$I_{OH} = –8\text{ mA (–1)}$ $I_{OL} = –12\text{ mA (–1H)}$	2.4		V
I_{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz		25.0	μA
I_{DD}	Supply Current	Unloaded outputs at 66.67 MHz, SEL inputs at V_{DD}		35.0	mA

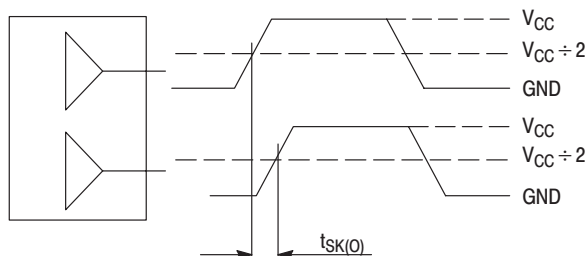
Table 7. Switching Characteristics for MPC962305–1 and MPC962309–1 Industrial Temperature Devices^[6]

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
t ₁	Output Frequency	30-pF load 10-pF load	10 10		100 133.33	MHz MHz
	Duty Cycle = t ₂ ÷ t ₁	Measured at 1.4V, F _{OUT} = 66.67 MHz	40.0	50.0	60.0	%
t ₃	Rise Time	Measured between 0.8V and 2.0V			2.50	ns
t ₄	Fall Time	Measured between 0.8V and 2.0V			2.50	ns
t ₅	Output to Output Skew	All outputs equally loaded			250	ps
t _{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at V _{DD} /2		0	±350	ps
t _{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at V _{DD} /2. Measured in PLL Bypass Mode, MPC962309 device only.	1	5	8.7	ns
t ₇	Device to Device Skew	Measured at V _{DD} /2 on the CLKOUT pins of devices		0	700	ps
t _J	Cycle to Cycle Jitter	Measured at 66.67 MHz, loaded outputs			200	ps
t _{LOCK}	PLL Lock Time	Stable power supply, valid clock presented on REF pin			1.0	ms

Table 8. Switching Characteristics for MPC962305–1H and MPC962309–1H Industrial Temperature Devices^[6]

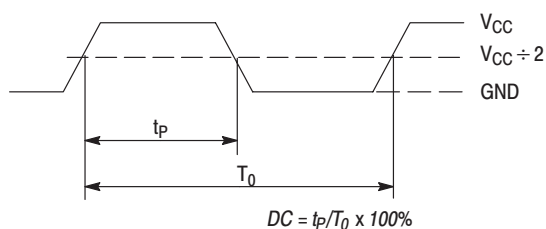
Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
t ₁	Output Frequency	30-pF load 10-pF load	10 10		100 133.33	MHz MHz
	Duty Cycle = t ₂ ÷ t ₁	Measured at 1.4V, F _{OUT} = 66.67 MHz	40.0	50.0	60.0	%
	Duty Cycle = t ₂ ÷ t ₁	Measured at 1.4V, F _{OUT} < 50 MHz	45.0	50.0	55.0	%
t ₃	Rise Time	Measured between 0.8V and 2.0V			1.50	ns
t ₄	Fall Time	Measured between 0.8V and 2.0V			1.50	ns
t ₅	Output to Output Skew	All outputs equally loaded			250	ps
t _{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at V _{DD} /2		0	±350	ps
t _{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at V _{DD} /2. Measured in PLL Bypass Mode, MPC962309 device only.	1	5	8.7	ns
t ₇	Device to Device Skew	Measured at V _{DD} /2 on the CLKOUT pins of devices		0	700	ps
t ₈	Output Slew Rate	Measured between 0.8V and 2.0V using Test Circuit #2	1			V/ns
t _J	Cycle to Cycle Jitter	Measured at 66.67 MHz, loaded outputs			200	ps
t _{LOCK}	PLL Lock Time	Stable power supply, valid clock presented on REF pin			1.0	ms

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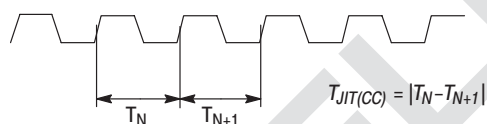
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 1. Output-to-output Skew $t_{SK(O)}$



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 3. Output Duty Cycle (DC)



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 5. Cycle-to-cycle Jitter

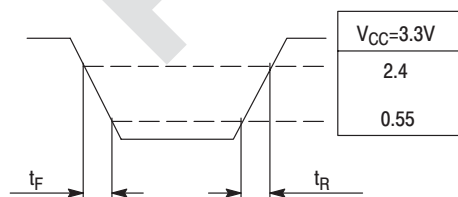


Figure 7. Output Transition Time Test Reference

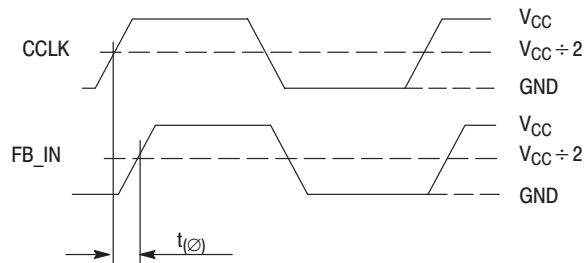
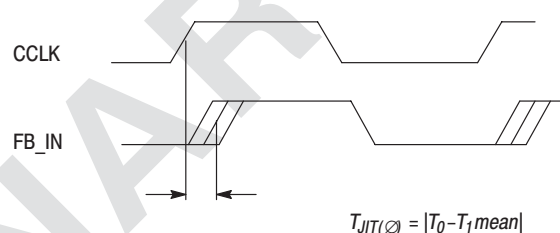
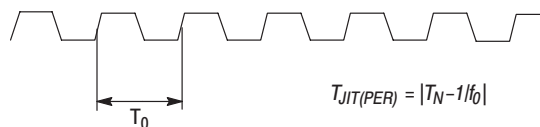


Figure 2. Propagation delay (t_{PD} , static phase offset) test reference



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 4. I/O Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 6. Period Jitter

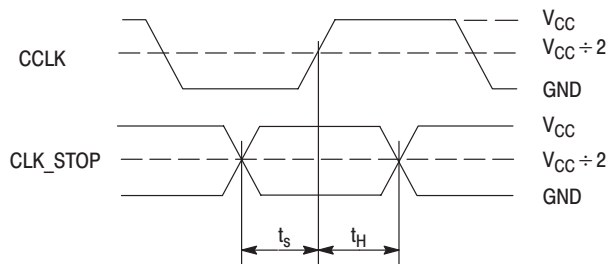
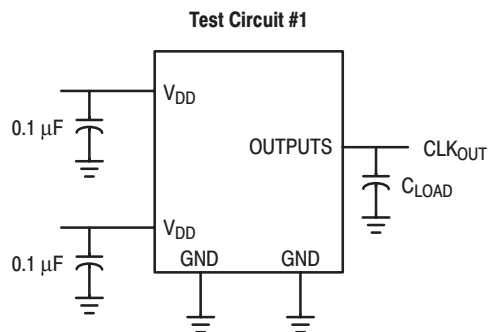
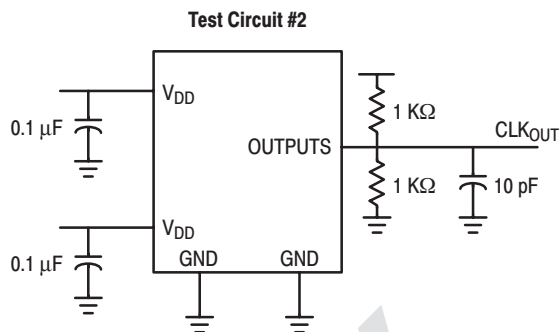


Figure 8. Setup and Hold Time (t_s , t_h) Test Reference

Test Circuit for all parameters except t_b Test Circuit for t_b , Output slew rate on -1H, -5 device**Table 9. Ordering Information**

Ordering Code	Package Type
MPC962305D-1	8-pin 150-mil SOIC
MPC962305D-1R2	8-pin 150-mil SOIC-Tape and Reel
MPC962305D-1H	8-pin 150-mil SOIC
MPC962305D-1HR2	8-pin 150-mil SOIC-Tape and Reel
MPC962305DT-1H	8-pin 150-mil TSSOP
MPC962305DT-1HR2	8-pin 150-mil TSSOP-Tape and Reel
MPC962309D-1	16-pin 150-mil SOIC
MPC962309D-1R2	16-pin 150-mil SOIC-Tape and Reel
MPC962309D-1H	16-pin 150-mil SOIC
MPC962309D-1HR2	16-pin 150-mil SOIC-Tape and Reel
MPC962309DT-1H	16-pin 4.4-mm TSSOP
MPC962309DT-1HR2	16-pin 4.4-mm TSSOP-Tape and Reel

3.3V Zero Delay Buffer

The MPC962308 is a 3.3V Zero Delay Buffer designed to distribute high-speed clocks in PC, workstation, datacom, telecom and other high-performance applications. The MPC962308 uses an internal PLL and an external feedback path to lock its low-skew clock output phase to the reference clock phase, providing virtually zero propagation delay. The input-to-output skew is guaranteed to be less than 250 ps and output-to-output skew is guaranteed to be less than 200 ps.

Features

- 1:8 outputs LVCMOS zero-delay buffer
- Zero input-output propagation delay, adjustable by the capacitive load on FBK input
- Multiple Configurations, See "Available MPC962308 Configurations" table
- Multiple low-skew outputs
 - 200 ps max output-output skew
 - 700 ps max device-device skew
 - Two banks of four outputs, output tristate control by two select inputs
- Supports a clock I/O frequency range of 10MHz to 133MHz
- Low jitter, 200 ps max cycle-cycle (–1, –1H, –4, –5H)
- ± 250 ps static phase offset (SPO)
- 16-pin SOIC package or 16-pin TSSOP package
- Single 3.3V supply
- Ambient temperature range: –40°C to +85°C
- Compatible with the CY2308 and CY23S08
- Spread spectrum compatible

Functional Description

The MPC962308 has two banks of four outputs each which can be controlled by the select inputs as shown in the table "Selected Input Decoding." Bank B can be tristated if all of the outputs are not required. The select inputs also allow the input clock to be directly applied to the output for chip and system testing purposes. The MPC962308 PLL enters a power down state when there are no rising edges on the REF input. During this state, all of the outputs are in tristate and there is less than 50 μ A of current draw. The PLL shuts down in two additional cases explained in the "Select Input Decoding" table.

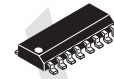
Multiple MPC962308 devices can accept and distribute the same input clock throughout the system. In this situation, the difference between the output skews of two devices will be less than 700 ps.

The MPC962308 is available in five different configurations as shown in the "Available MPC962308 Configurations" table. In the MPC962308–1, the reference frequency is reproduced by the PLL and provided at the outputs. A high drive version of this configuration, the MPC962308–1H, is available to provide faster rise and fall times of the device.

The MPC962308–2 provides 2X and 1X the reference frequency at the output banks. In addition, the MPC962308–3 provides 4X and 2X the reference frequency at the output banks. The output banks driving the feedback will determine the different configurations of the above devices. The MPC962308–4 provides outputs 2X the reference frequency. The MPC962308–5H is a high drive version with outputs of REF/2.

The MPC962308 is fully 3.3V compatible and requires no external components for the internal PLL. All inputs accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines on the incident edge. Depending on the configuration, the device is offered in a 16-lead SOIC or 16-lead TSSOP package.

MPC962308

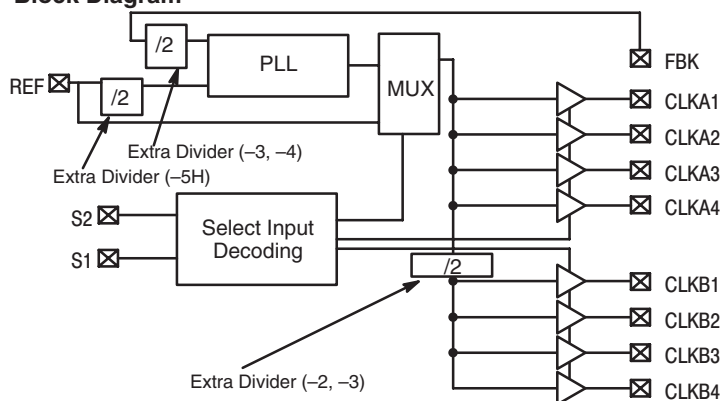


D SUFFIX
16 LEAD SOIC PACKAGE
CASE 751B



DT SUFFIX
16 LEAD TSSOP PACKAGE
CASE 948F

Block Diagram



Pin Configuration

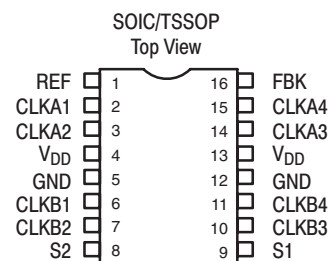


Table 1. Select Input Decoding

S2	S1	CLOCK A1–A4	CLOCK B1–B4	Output Source	PLL Shutdown
0	0	Three–State	Three–State	PLL	Y
0	1	Driven	Three–State	PLL	N
1	0	Driven	Driven	Reference	Y
1	1	Driven	Driven	PLL	N

Table 2. Available MPC962308 Configurations

Device	Feedback From	Bank A Frequency	Bank B Frequency
MPC962308–1	Bank A or Bank B	Reference	Reference
MPC962308–1H	Bank A or Bank B	Reference	Reference
MPC962308–2	Bank A	Reference	Reference/2
MPC962308–2	Bank B	2 X Reference	Reference
MPC962308–3	Bank A	2 X Reference	Reference or Reference ^[1]
MPC962308–3	Bank B	4 X Reference	2 X Reference
MPC962308–4	Bank A or Bank B	2 X Reference	2 X Reference
MPC962308–5H	Bank A or Bank B	Reference /2	Reference /2

NOTE:

1 Output phase is indeterminant (0° or 180° from input clock). If phase integrity is required, use the MPC962308–2.

Table 3. Pin Description

Pin	Signal	Description
1	REF ^[2]	Input reference frequency, 5V tolerant input
2	CLKA1 ^[3]	Clock output, Bank A
3	CLKA2 ^[3]	Clock output, Bank A
4	VDD	3.3V supply
5	GND	Ground
6	CLKB1 ^[3]	Clock output, Bank B
7	CLKB2 ^[3]	Clock output, Bank B
8	S2 ^[4]	Select input, bit 2
9	S1 ^[4]	Select input, bit 1
10	CLKB3 ^[3]	Clock output, Bank B
11	CLKB4 ^[3]	Clock output, Bank B
12	GND	Ground
13	VDD	3.3V supply
14	CLKA3 ^[3]	Clock output, Bank A
15	CLKA4 ^[3]	Clock output, Bank A
16	FBK	PLL feedback input

NOTE:

2 Weak pull-down.

3 Weak pull-down on all outputs.

4 Weak pull-ups on these inputs.

5

Table 4. Maximum Ratings

Characteristics	Value	Unit
Supply Voltage to Ground Potential	−0.5 to +4.6	V
DC Input Voltage (Except Ref)	−0.5 to $V_{DD}+0.5$	V
DC Input Voltage REF	−0.5 to 5.5	V
Storage Temperature	−65 to +150	°C
Junction	150	°C
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2000	V

Table 5. Operating Conditions for MPC962308–XX Industrial Temperature Devices

Parameter	Description	Min.	Max.	Unit
V _{DD}	Supply Voltage	3.0	3.6	V
T _A	Operating Temperature (Ambient Temperature)	–40	85	°C
C _L	Load Capacitance, below 100 MHz		30	pF
	Load Capacitance, from 100 MHz to 133 MHz		15	pF
C _{IN}	Input Capacitance ^[5]		7	pF

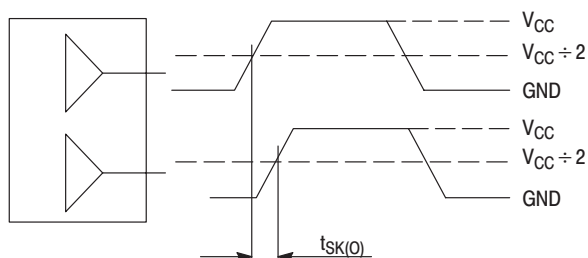
Table 6. Electrical Characteristics for MPC962308–XX Industrial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Unit
V _{IL}	Input LOW Voltage			0.8	V
V _{IH}	Input HIGH Voltage		2.0		V
I _{IL}	Input LOW Current	V _{IN} = 0V		50.0	μA
I _{IH}	Input HIGH Current	V _{IN} = V _{DD}		100.0	μA
V _{OL}	Output LOW Voltage	I _{OL} = 8 mA (–1, –2, –3, –4) I _{OL} = 12 mA (–1H, –5H)		0.4	V
V _{OH}	Output HIGH Voltage	I _{OH} = –8 mA (–1, –2, –3, –4) I _{OH} = –12 mA (–1H, –5H)	2.4 V	2.4	V
I _{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz		25.0	μA
I _{DD}	Supply Current	Unloaded outputs, 100 MHz, Select inputs at V _{DD} or GND		45.0	mA
				70(–1H, –5H)	mA
		Unloaded outputs, 66–MHz REF (–1, –2, –3, –4)		35.0	mA
		Unloaded outputs, 66–MHz REF (–1, –2, –3, –4)		20.0	mA

Table 7. Switching Characteristics for MPC962308–XX Industrial Temperature Devices^[6]

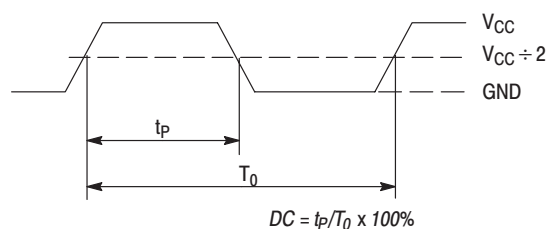
Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
t ₁	Output Frequency	30-pF load, All devices	10		100	MHz
t ₁	Output Frequency	20-pF load, –1H, –5H devices ^[7]	10		133.3	MHz
t ₁	Output Frequency	15-pF load, –1, –2, –3, –4 devices	10		133.3	MHz
	Duty Cycle = t ₂ ÷ t ₁ (–1, –2, –3, –4, –1H, –5H)	Measured at 1.4V, F _{OUT} = 66.66 MHz 30-pF load	40.0	50.0	60.0	%
	Duty Cycle = t ₂ ÷ t ₁ (–1, –2, –3, –4, –1H, –5H)	Measured at 1.4V, F _{OUT} < 50.0 MHz 15-pF load	45.0	50.0	55.0	%
t ₃	Rise Time (–1, –2, –3, –4)	Measured between 0.8V and 2.0V, 30-pF load			2.50	ns
t ₃	Rise Time (–1, –2, –3, –4)	Measured between 0.8V and 2.0V, 15-pF load			1.50	ns
t ₃	Rise Time (–1H, –5H)	Measured between 0.8V and 2.0V, 30-pF load			1.50	ns
t ₄	Fall Time (–1, –2, –3, –4)	Measured between 0.8V and 2.0V, 30-pF load			2.50	ns
t ₄	Fall Time (–1, –2, –3, –4)	Measured between 0.8V and 2.0V, 15-pF load			1.50	ns
t ₄	Fall Time (–1H, –5H)	Measured between 0.8V and 2.0V, 30-pF load			1.25	ns
t ₅	Output to Output Skew on same Bank (–1, –2, –3, –4)	All outputs equally loaded			200	ps
	Output to Output Skew (–1H, –5H)	All outputs equally loaded			200	ps
	Output Bank A to Output Bank B Skew (–1, –4, –5H)	All outputs equally loaded			200	ps
	Output Bank A to Output Bank B Skew (–2, –3)	All outputs equally loaded			400	ps
t ₆	Delay, REF Rising Edge to FBK Rising Edge	Measured at V _{DD} /2		0	± 250	ps
t ₇	Device to Device Skew	Measured at V _{DD} /2 on the FBK pins of devices		0	700	ps
t ₈	Output Slew Rate	Measured between 0.8V and 2.0V on –1H, –5H device using Test Circuit # 2	1			V/ns
t _J	Cycle to Cycle Jitter (–1, –1H, –4, –5H)	Measured at 66.67 MHz, loaded outputs, 15-pF load			200	ps
		Measured at 66.67 MHz, loaded outputs, 30-pF load			200	ps
		Measured at 133.3 MHz, loaded outputs, 15 pF load			100	ps
t _J	Cycle to Cycle Jitter (–2, –3)	Measured at 66.67 MHz, loaded outputs 30-pF load			400	ps
		Measured at 66.67 MHz, loaded outputs 15-pF load			400	ps
t _{LOCK}	PLL Lock Time	Stable power supply, valid clocks presented on REF and FBK pins			1.0	ms

APPLICATIONS INFORMATION



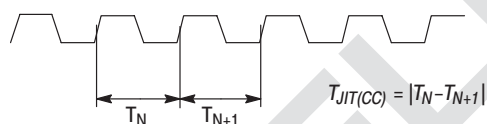
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 1. Output-to-output Skew $t_{SK(O)}$



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 3. Output Duty Cycle (DC)



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 5. Cycle-to-cycle Jitter

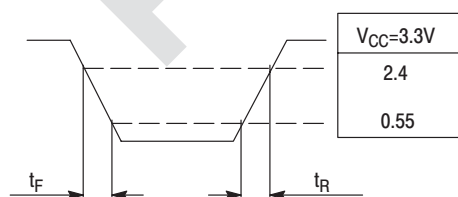


Figure 7. Output Transition Time Test Reference

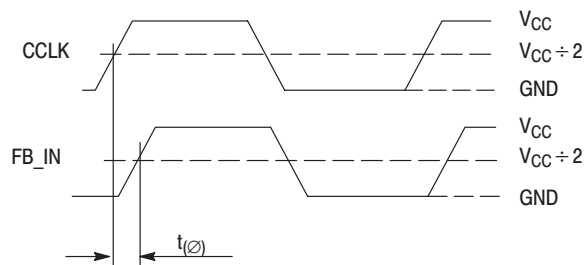
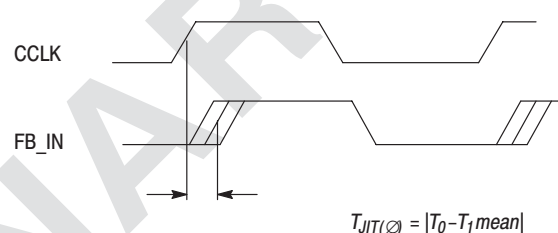
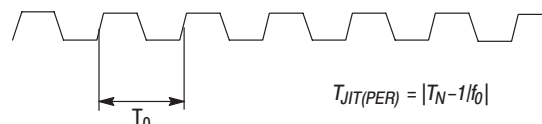


Figure 2. Propagation delay (t_{PD} , static phase offset) test reference



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 4. I/O Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 6. Period Jitter

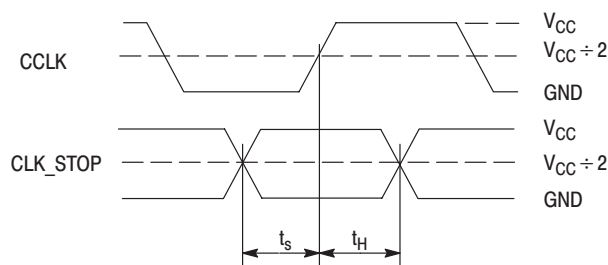
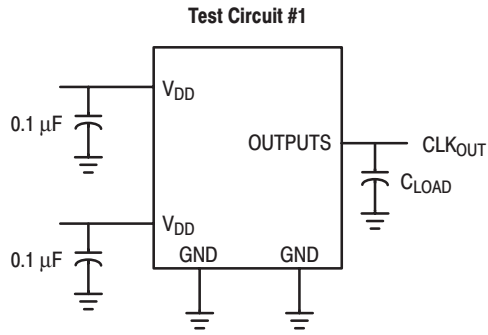
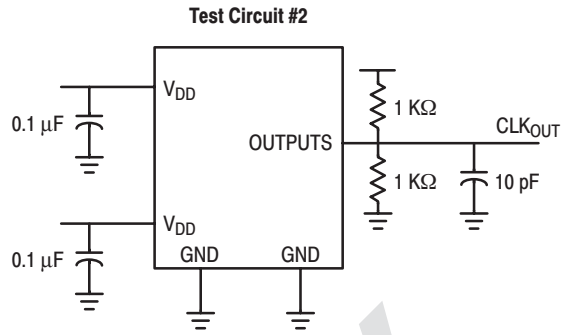


Figure 8. Setup and Hold Time (t_s , t_h) Test Reference



Test Circuit for all parameters except t_b



Test Circuit for t_b , Output slew rate on -1H, -5 device

Ordering Information (Available)

Ordering Code	Package Name	Package Type
MPC962308D-1	D16	16-pin 150-mil SOIC
MPC962308D-1R2	D16	16-pin 150-mil SOIC – Tape and Reel
MPC962308D-1H	D16	16-pin 150-mil SOIC
MPC962308D-1HR2	D16	16-pin 150-mil SOIC – Tape and Reel
MPC962308DT-1H	DT16	16-pin 150-mil TSSOP
MPC962308DT-1HR2	DT16	16-pin 150-mil TSSOP – Tape and Reel
MPC962308D-2	D16	16-pin 150-mil SOIC
MPC962308D-2R2	D16	16-pin 150-mil SOIC – Tape and Reel

Ordering Information (Planned)

Ordering Code	Package Name	Package Type
MPC962308D-3	D16	16-pin 150-mil SOIC
MPC962308D-3R2	D16	16-pin 150-mil SOIC – Tape and Reel
MPC962308D-4	D16	16-pin 150-mil SOIC
MPC962308D-4R2	D16	16-pin 150-mil SOIC – Tape and Reel
MPC962308D-5H	D16	16-pin 150-mil SOIC
MPC962308D-5HR2	D16	16-pin 150-mil SOIC – Tape and Reel
MPC962308DT-5H	DT16	16-pin 150-mil TSSOP
MPC962308DT-5HR2	DT16	16-pin 150-mil TSSOP – Tape and Reel

3.3V 1:8 LVCMOS PLL Clock Generator

The MPC9653 is a 3.3V compatible, 1:8 PLL based clock generator and zero-delay buffer targeted for high performance low-skew clock distribution in mid-range to high-performance telecom, networking and computing applications. With output frequencies up to 125 MHz and output skews less than 150 ps the device meets the needs of the most demanding clock applications.

Features

- 1:8 PLL based low-voltage clock generator
- Supports zero-delay operation
- 3.3V power supply
- Generates clock signals up to 125 MHz
- Maximum output skew of 150 ps
- Differential LVPECL reference clock input
- External PLL feedback
- Drives up to 16 clock lines
- 32 lead LQFP packaging
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MPC953

Functional Description

The MPC9653 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9653 requires the connection of the QFB output to the feedback input to close the PLL feedback path (external feedback). With the PLL locked, the output frequency is equal to the reference frequency of the device and VCO_SEL selects the operating frequency range of 25 to 62.5 MHz or 50 to 125 MHz. The two available post-PLL dividers selected by VCO_SEL (divide-by-4 or divide-by-8) and the reference clock frequency determine the VCO frequency. Both must be selected to match the VCO frequency range. The internal VCO of the MPC9653 is running at either 4x or 8x of the reference clock frequency.

The MPC9653 has a differential LVPECL reference input along with an external feedback input. The device is ideal for use as a zero delay, low skew fanout buffer. The device performance has been tuned and optimized for zero delay performance.

The PLL_EN and BYPASS controls select the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is bypassing the PLL and routed either to the output dividers or directly to the outputs. The PLL bypass configurations are fully static and the minimum clock frequency specification and all other PLL characteristics do not apply. The outputs can be disabled (high-impedance) and the device reset by asserting the MR/ÖE pin. Asserting MR/ÖE also causes the PLL to loose lock due to missing feedback signal presence at FB_IN. Deasserting MR/ÖE will enable the outputs and close the phase locked loop, enabling the PLL to recover to normal operation.

The MPC9653 is fully 3.3V compatible and requires no external loop filter components. The inputs (except PCLK) accept LVCMOS except signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9653 outputs can drive one or two traces giving the devices an effective fanout of 1:16. The device is packaged in a 7x7 mm² 32-lead LQFP package.

MPC9653

**LOW VOLTAGE
3.3V LVCMOS 1:8
PLL CLOCK GENERATOR**



FA SUFFIX
32 LEAD LQFP PACKAGE
CASE 873A

5

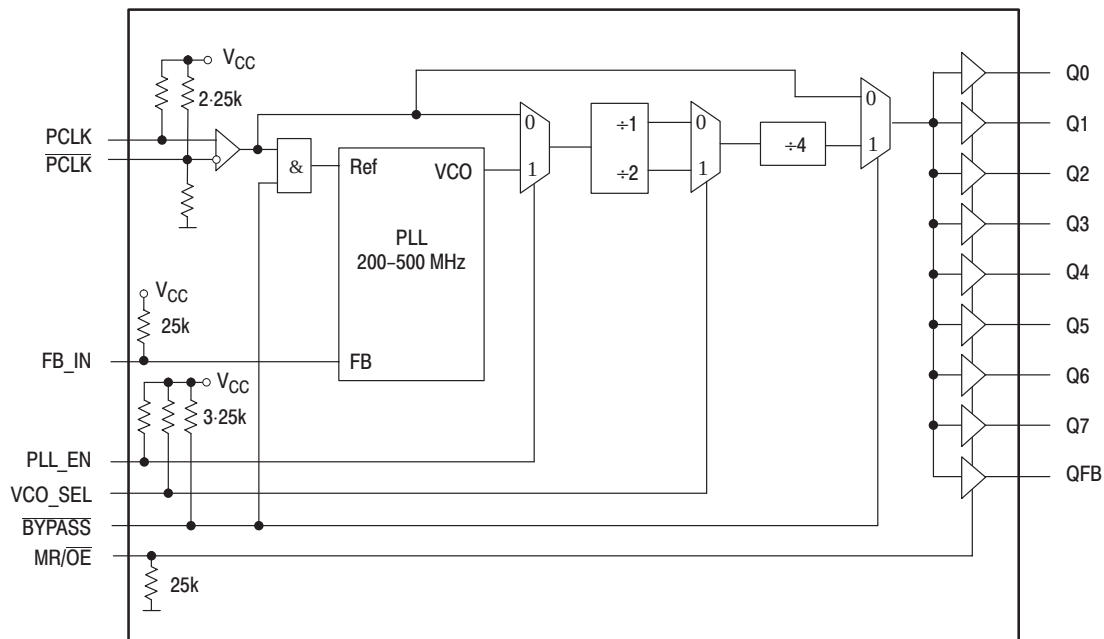


Figure 1. MPC9653 Logic Diagram

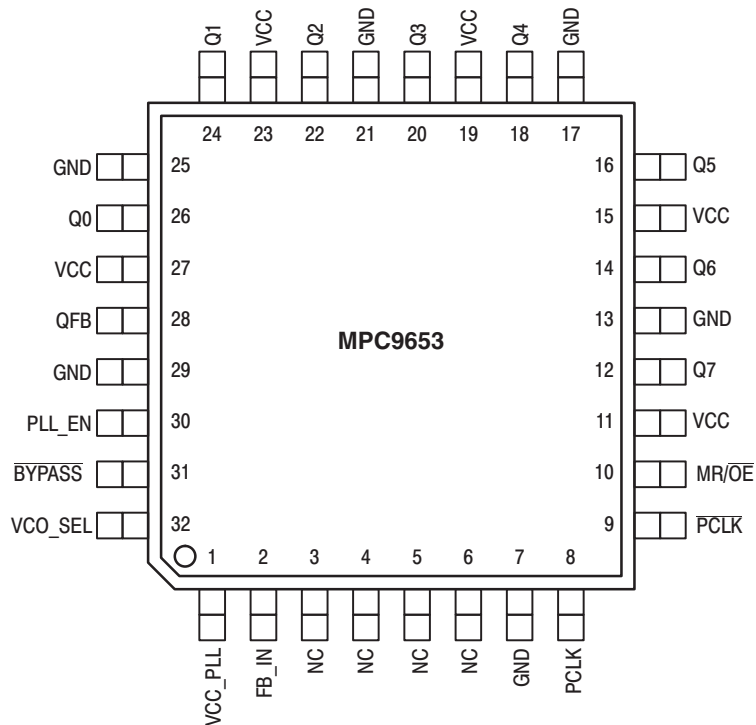


Figure 2. MPC9653 32-Lead Package Pinout (Top View)

Table 1: PIN CONFIGURATION

Pin	I/O	Type	Function
PCLK, PCLK	Input	LVPECL	PECL reference clock signal
FB_IN	Input	LVC MOS	PLL feedback signal input, connect to QFB
VCO_SEL	Input	LVC MOS	Operating frequency range select
BYPASS	Input	LVC MOS	PLL and output divider bypass select
PLL_EN	Input	LVC MOS	PLL enable/disable
MR/ÖE	Input	LVC MOS	Output enable/disable (high-impedance tristate) and device reset
Q0-7	Output	LVC MOS	Clock outputs
QFB	Output	LVC MOS	Clock output for PLL feedback, connect to FB_IN
GND	Supply	Ground	Negative power supply (GND)
VCC_PLL	Supply	VCC	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin VCC_PLL. Please see applications section for details.
VCC	Supply	VCC	Positive power supply for I/O and core. All VCC pins must be connected to the positive power supply for correct operation

Table 2: FUNCTION TABLE

Control	Default	0	1
PLL_EN	1	Test mode with PLL bypassed. The reference clock (PCLK) is substituted for the internal VCO output. MPC9653 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Selects the VCO output ^a
BYPASS	1	Test mode with PLL and output dividers bypassed. The reference clock (PCLK) is directly routed to the outputs. MPC9653 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Selects the output dividers.
VCO_SEL	1	$VCO \div 1$ (High frequency range). $f_{REF} = f_{Q0-7} = 4 \cdot f_{VCO}$	$VCO \div 2$ (Low output range). $f_{REF} = f_{Q0-7} = 8 \cdot f_{VCO}$
MR/ÖE	0	Outputs enabled (active)	Outputs disabled (high-impedance state) and reset of the device. During reset the PLL feedback loop is open. The VCO is tied to its lowest frequency. The length of the reset pulse should be greater than one reference clock cycle (PCLK).

a. PLL operation requires BYPASS=1 and PLL_EN=1.

Table 3: GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 4: ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.9	V	
V_{IN}	DC Input Voltage	-0.3	$V_{CC}+0.3$	V	
V_{OUT}	DC Output Voltage	-0.3	$V_{CC}+0.3$	V	
I_{IN}	DC Input Current		± 20	mA	
I_{OUT}	DC Output Current		± 50	mA	
T_S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5: DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	2.0		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input low voltage			0.8	V	LVC MOS
V_{PP}	Peak-to-peak input voltage (PCLK)	300			mV	LVPECL
V_{CMR}^a	Common Mode Range (PCLK)	1.0		$V_{CC}-0.6$	V	LVPECL
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -24\text{ mA}^b$
V_{OL}	Output Low Voltage			0.55 0.30	V V	$I_{OL} = 24\text{ mA}$ $I_{OL} = 12\text{ mA}$
Z_{OUT}	Output impedance		14 - 17		Ω	
I_{IN}	Input Current ^c			± 200	μA	$V_{IN} = V_{CC}$ or GND
I_{CC_PLL}	Maximum PLL Supply Current		5.0	10	mA	V_{CC_PLL} Pin
I_{CCQ}^d	Maximum Quiescent Supply Current			10	mA	All V_{CC} Pins

- a V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
- b The MPC9653 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines. The MPC9653 meets the V_{OH} and V_{OL} specification of the MPC953 ($V_{OH} > V_{CC}-0.6V$ at $I_{OH} = -20\text{mA}$ and $V_{OL} > 0.6V$ at $I_{OL} = 20\text{mA}$).
- c Inputs have pull-down or pull-up resistors affecting the input current.
- d OE/MR=1 (outputs in high-impedance state).

Table 6: AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{REF}	Input reference frequency +4 feedback ^b	50		125	MHz	PLL locked
	PLL mode, external feedback +8 feedback ^c	25		62.5	MHz	PLL locked
	Input reference frequency in PLL bypass mode ^d	0		200	MHz	
f_{VCO}	VCO lock frequency range ^e	200		500	MHz	
f_{MAX}	Output Frequency	+4 feedback ^b	50	125	MHz	PLL locked
		+8 feedback ^c	25	62.5	MHz	PLL locked
V_{PP}	Peak-to-peak input voltage PCLK	450		1000	mV	LVPECL
V_{CMRf}	Common Mode Range PCLK	1.2		$V_{CC}-0.75$	V	LVPECL
$t_{PW,MIN}$	Input Reference Pulse Width ^g	2			ns	
$t_{(\phi)}$	Propagation Delay (static phase offset) ^h PCLK to FB_IN	-75		125	ps	PLL locked
t_{PD}	Propagation Delay PLL and divider bypass ($\overline{BYPASS}=0$), PCLK to Q0-7 PLL disable ($\overline{BYPASS}=1$ and $PLL\_EN=0$), PCLK to Q0-7	1.2		3.3	ns	
		3.0		7.0	ns	
$t_{sk(O)}$	Output-to-output Skew ⁱ			150	ps	
$t_{sk(PP)}$	Device-to-device Skew in PLL and divider bypass ^j			1.5	ns	$\overline{BYPASS}=0$
DC	Output duty cycle	45	50	55	%	PLL locked
t_R, t_F	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time			7.0	ns	
$t_{PZL, LZ}$	Output Enable Time			6.0	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter			100	ps	
$t_{JIT(PER)}$	Period Jitter			100	ps	
$t_{JIT(\phi)}$	I/O Phase Jitter ^k RMS (1 σ)			25	ps	
BW	PLL closed loop bandwidth ^l PLL mode, external feedback	÷ 4 feedback ^b ÷ 8 feedback ^c		0.8 – 4	MHz	
				0.5 – 1.3	MHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

a AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b +4 PLL feedback (high frequency range) requires $VCO\_SEL=0$, $PLL\_EN=1$, $\overline{BYPASS}=1$ and $MR/\overline{OE}=0$.

c +8 PLL feedback (low frequency range) requires $VCO\_SEL=1$, $PLL\_EN=1$, $\overline{BYPASS}=1$ and $MR/\overline{OE}=0$.

d In bypass mode, the MPC9653 divides the input reference clock.

e The input frequency f_{REF} must match the VCO frequency range divided by the feedback divider ratio FB: $f_{REF} = f_{VCO} \div FB$.

f V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\phi)}$.

g Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF,MAX} = 100\% - DC_{REF,MIN}$.
E.g. at $f_{REF}=100$ MHz the input duty cycle range is $20\% < DC < 80\%$.

h Valid for $f_{REF}=50$ MHz and $FB=+8$ ($VCO\_SEL=1$). For other reference frequencies: $t_{(\phi)}$ [ps] = $50 \text{ ps} \pm (1 + (120 \cdot f_{REF}))$.

i See application section for part-to-part skew calculation in PLL zero-delay mode.

j For a specified temperature and voltage, includes output skew.

k I/O phase jitter is reference frequency dependent. See application section for details.

l -3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Programming the MPC9653

The MPC9653 supports output clock frequencies from 25 to 125 MHz. Two different feedback divider configurations can be used to achieve the desired frequency operation range. The feedback divider (VCO_SEL) should be used to situate the VCO in the frequency lock range between 200 and 500 MHz

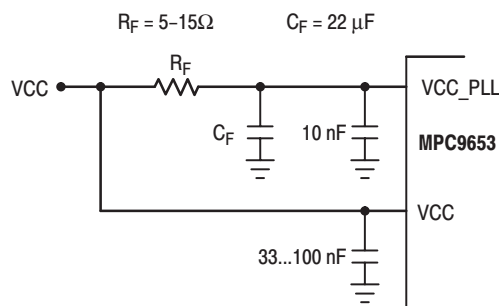
for stable and optimal operation. Two operating frequency ranges are supported: 25 to 62.5 MHz and 50 to 125 MHz. Table 9 illustrates the configurations supported by the MPC9653. PLL zero-delay is supported if BYPASS=1, PLL_EN=1 and the input frequency is within the specified PLL reference frequency range.

Table 9: MPC9653 Configurations (QFB connected to FB_IN)

BYPASS	PLL_EN	VCO_SEL	Operation	Frequency		
				Ratio	Output range (f _{Q0-7})	VCO
0	X	X	Test mode: PLL and divider bypass	f _{Q0-7} = f _{REF}	0-200 MHz	n/a
1	0	0	Test mode: PLL bypass	f _{Q0-7} = f _{REF} ÷ 4	0-50 MHz	n/a
1	0	1	Test mode: PLL bypass	f _{Q0-7} = f _{REF} ÷ 8	0-25 MHz	n/a
1	1	0	PLL mode (high frequency range)	f _{Q0-7} = f _{REF}	50 to 125 MHz	f _{VCO} = f _{REF} · 4
1	1	1	PLL mode (low frequency range)	f _{Q0-7} = f _{REF}	25 to 62.5 MHz	f _{VCO} = f _{REF} · 8

Power Supply Filtering

The MPC9653 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC9653 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA_PLL} pin for the MPC9653. Figure 3 illustrates a typical power supply filter scheme. The MPC9653 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CCA} current (the current sourced through the V_{CCA_PLL} pin) is typically 5 mA (10 mA maximum), assuming that a minimum of 2.985V must be maintained on the V_{CCA_PLL} pin.

Figure 3. V_{CCA_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3 “V_{CCA_PLL} Power Supply Filter”, the filter cut-off frequency is around 4 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9653 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9653 in zero-delay applications

Nested clock trees are typical applications for the MPC9653. Designs using the MPC9653 as LVCMOS PLL fan-out buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fan-out buffers. The external feedback option of the MPC9653 clock driver allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device (the propagation delay through the device is virtually eliminated). The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of part-to-part skew

The MPC9653 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9653 are connected together, the maximum overall timing uncertainty from the common PCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD, LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

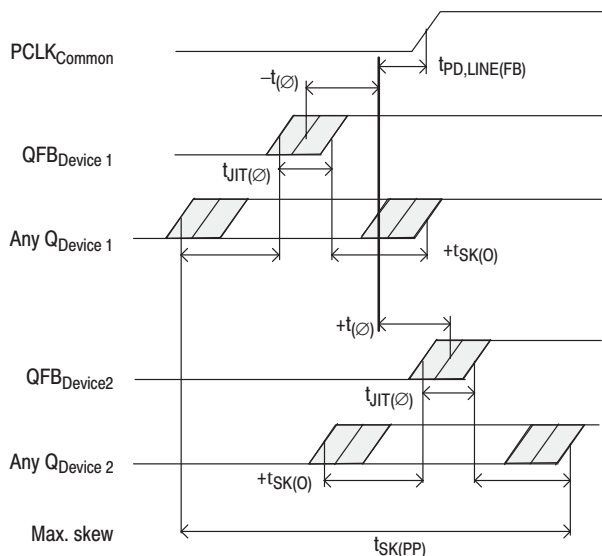


Figure 4. MPC9653 max. device-to-device skew

Due to the statistical nature of I/O jitter a RMS value (1σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 10.

Table 10: Confidence Factor CF

CF	Probability of clock edge within the distribution
$\pm 1\sigma$	0.68268948
$\pm 2\sigma$	0.95449988
$\pm 3\sigma$	0.99730007
$\pm 4\sigma$	0.99993663
$\pm 5\sigma$	0.99999943
$\pm 6\sigma$	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% ($\pm 3\sigma$) is assumed, resulting in a worst case timing uncertainty from input to any output of -197 ps to 297 ps (at 125 MHz reference frequency) relative to PCLK:

$$t_{SK(PP)} = [-17ps...117ps] + [-150ps...150ps] + [(10ps \cdot -3)...(10ps \cdot 3)] + t_{PD, LINE(FB)}$$

$$t_{SK(PP)} = [-197ps...297ps] + t_{PD, LINE(FB)}$$

Due to the frequency dependence of the I/O jitter, Figure 5 “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis.

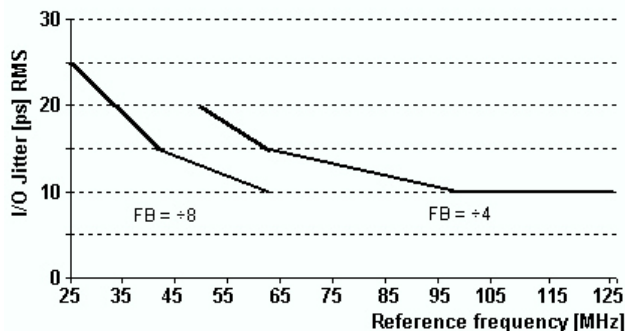


Figure 5. Max. I/O Jitter versus frequency

Driving Transmission Lines

The MPC9653 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC} \pm 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9653 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 6 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9653 clock driver is effectively doubled due to its capability to drive multiple lines.

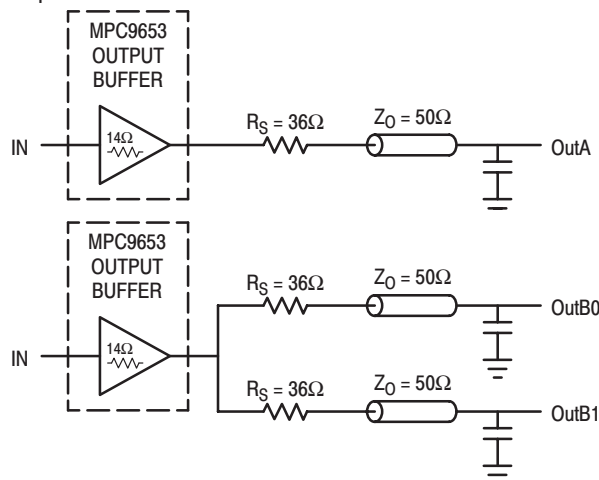


Figure 6. Single versus Dual Transmission Lines

The waveform plots in Figure 7 “Single versus Dual Line Termination Waveforms” show the simulation results of an out-

put driving a single line versus two lines. In both cases the drive capability of the MPC9653 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9653. The output waveform in Figure 7 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned} V_L &= V_S (Z_0 \div (R_S + R_0 + Z_0)) \\ Z_0 &= 50\Omega \parallel 50\Omega \\ R_S &= 36\Omega \parallel 36\Omega \\ R_0 &= 14\Omega \\ V_L &= 3.0 (25 \div (18 + 14 + 25)) \\ &= 1.31V \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

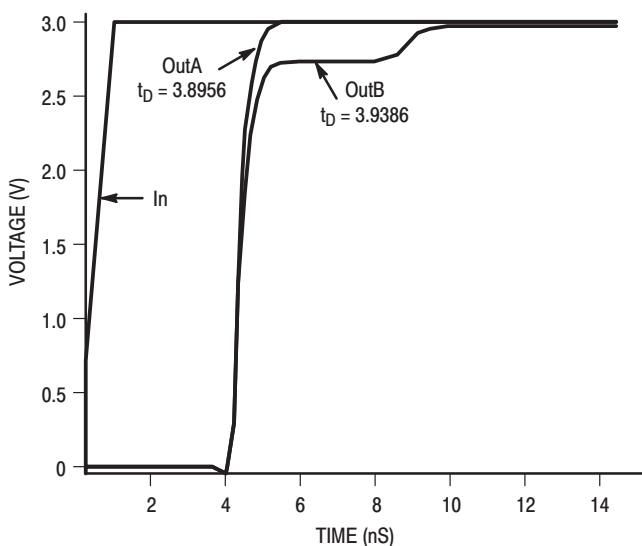


Figure 7. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 8 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

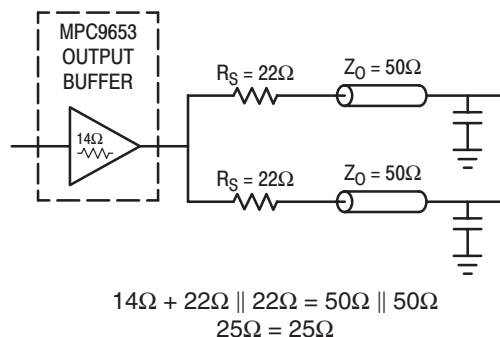


Figure 8. Optimized Dual Line Termination

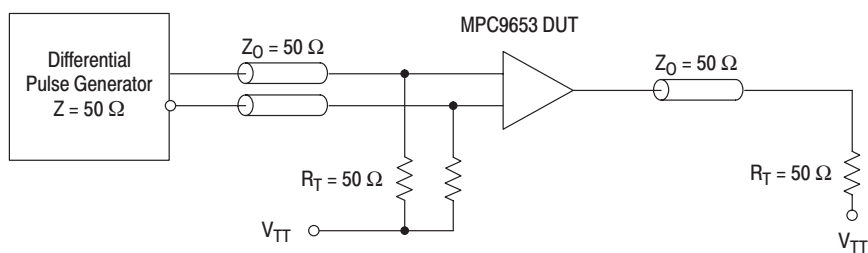
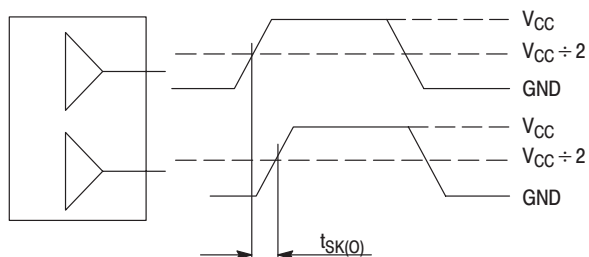
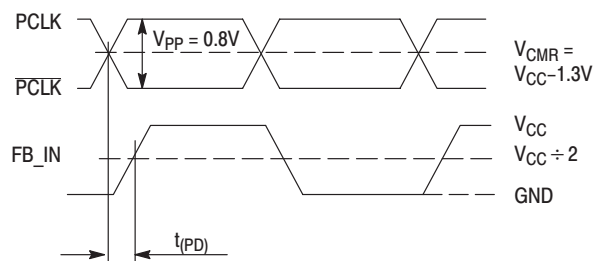
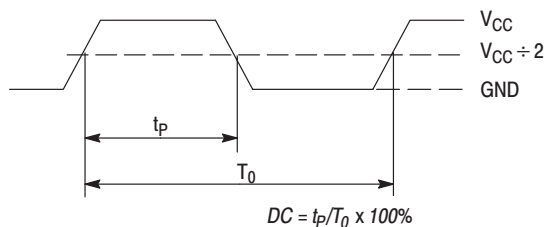


Figure 9. PCLK MPC9653 AC test reference

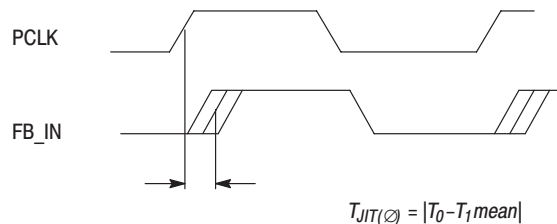


The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 10. Output-to-output Skew $t_{SK(O)}$ Figure 11. Propagation delay (t_{PD}), static phase offset) test reference

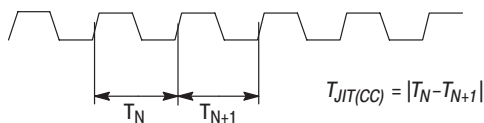
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 12. Output Duty Cycle (DC)



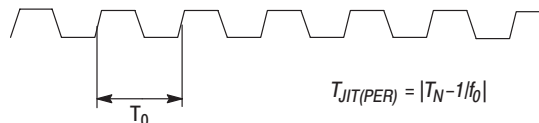
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 13. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 14. Cycle-to-cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 15. Period Jitter

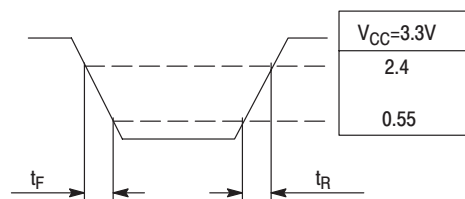


Figure 16. Output Transition Time Test Reference

3.3V 1:10 LVCMOS PLL Clock Generator

The MPC9658 is a 3.3V compatible, 1:10 PLL based clock generator and zero-delay buffer targeted for high performance low-skew clock distribution in mid-range to high-performance telecom, networking and computing applications. With output frequencies up to 250 MHz and output skews less than 120 ps the device meets the needs of the most demanding clock applications. The MPC9658 is specified for the temperature range of 0°C to +70°C.

Features

- 1:10 PLL based low-voltage clock generator
- Supports zero-delay operation
- 3.3V power supply
- Generates clock signals up to 250 MHz
- Maximum output skew of 120 ps
- Differential LVPECL reference clock input
- External PLL feedback
- Drives up to 20 clock lines
- 32 lead LQFP packaging
- Pin and function compatible to the MPC958

Functional Description

The MPC9658 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9658 requires the connection of the QFB output to the feedback input to close the PLL feedback path (external feedback). With the PLL locked, the output frequency is equal to the reference frequency of the device and VCO_SEL selects the operating frequency range of 50 to 125 MHz or 100 to 250 MHz. The two available post-PLL dividers selected by VCO_SEL (divide-by-2 or divide-by-4) and the reference clock frequency determine the VCO frequency. Both must be selected to match the VCO frequency range. The internal VCO of the MPC9658 is running at either 2x or 4x of the reference clock frequency.

The MPC9658 has a differential LVPECL reference input along with an external feedback input. The MPC9658 is ideal for use as a zero delay, low skew fanout buffer. The device performance has been tuned and optimized for zero delay performance.

The PLL_EN and BYPASS controls select the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is bypassing the PLL and routed either to the output dividers or directly to the outputs. The PLL bypass configurations are fully static and the minimum clock frequency specification and all other PLL characteristics do not apply. The outputs can be disabled (high-impedance) and the device reset by asserting the MR/ÖE pin. Asserting MR/ÖE also causes the PLL to loose lock due to missing feedback signal presence at FB_IN. Deasserting MR/ÖE will enable the outputs and close the phase locked loop, enabling the PLL to recover to normal operation.

The MPC9658 is fully 3.3V compatible and requires no external loop filter components. The inputs (except PCLK) accept LVCMOS except signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9658 outputs can drive one or two traces giving the devices an effective fanout of 1:16. The device is packaged in a 7x7 mm² 32-lead LQFP package.

MPC9658

**LOW VOLTAGE
3.3V LVCMOS 1:10
PLL CLOCK GENERATOR**



FA SUFFIX
32 LEAD LQFP PACKAGE
CASE 873A

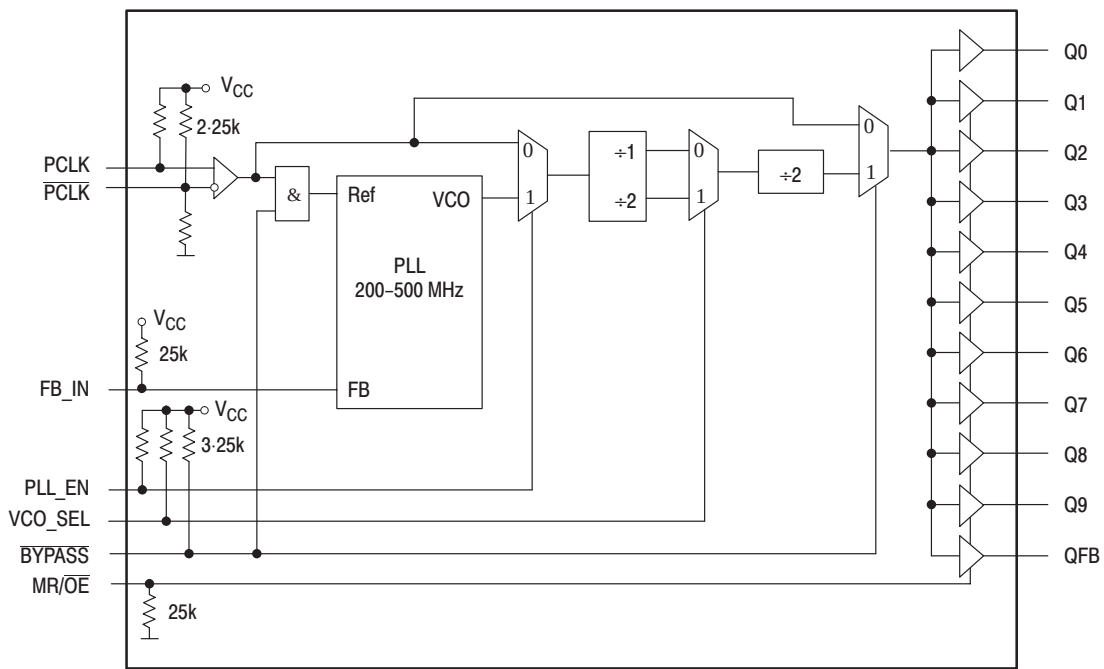


Figure 1. MPC9658 Logic Diagram

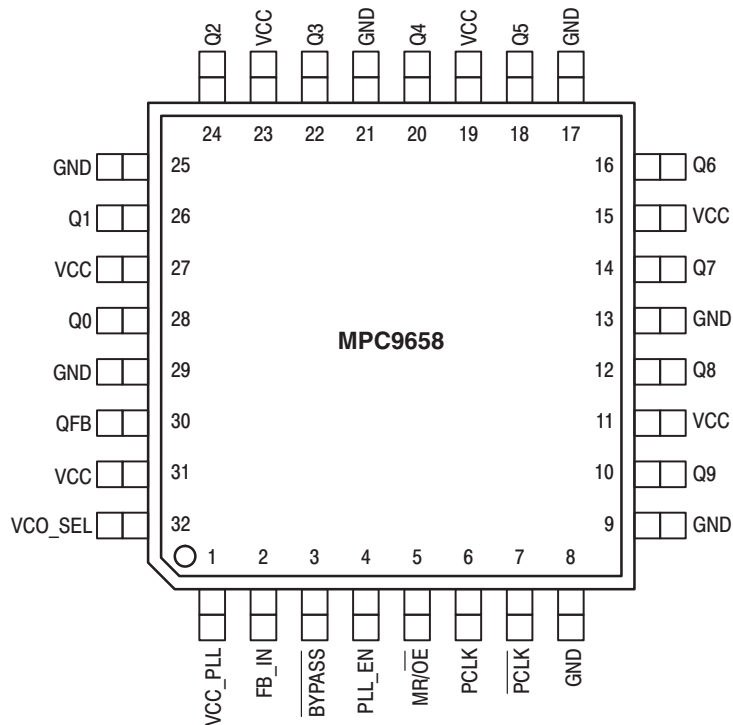


Figure 2. MPC9658 32-Lead Package Pinout (Top View)

Table 1. PIN CONFIGURATION

Pin	I/O	Type	Function
PCLK, PCLK	Input	LVPECL	PECL reference clock signal
FB_IN	Input	LVC MOS	PLL feedback signal input, connect to QFB
VCO_SEL	Input	LVC MOS	Operating frequency range select
BYPASS	Input	LVC MOS	PLL and output divider bypass select
PLL_EN	Input	LVC MOS	PLL enable/disable
MR/OE	Input	LVC MOS	Output enable/disable (high-impedance tristate) and device reset
Q0-9	Output	LVC MOS	Clock outputs
QFB	Output	LVC MOS	Clock output for PLL feedback, connect to FB_IN
GND	Supply	Ground	Negative power supply (GND)
VCC_PLL	Supply	VCC	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin VCC_PLL. Please see applications section for details.
VCC	Supply	VCC	Positive power supply for I/O and core. All VCC pins must be connected to the positive power supply for correct operation

Table 2. FUNCTION TABLE

Control	Default	0	1
PLL_EN	1	Test mode with PLL bypassed. The reference clock (PCLK) is substituted for the internal VCO output. MPC9658 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Selects the VCO output ^a
BYPASS	1	Test mode with PLL and output dividers bypassed. The reference clock (PCLK) is directly routed to the outputs. MPC9658 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Selects the output dividers.
VCO_SEL	1	VCO ÷ 1 (High frequency range). $f_{REF} = f_{Q0-9} = 2 \cdot f_{VCO}$	VCO ÷ 2 (Low frequency range). $f_{REF} = f_{Q0-9} = 4 \cdot f_{VCO}$
MR/OE	0	Outputs enabled (active)	Outputs disabled (high-impedance state) and reset of the device. During reset the PLL feedback loop is open. The VCO is tied to its lowest frequency. The length of the reset pulse should be greater than one reference clock cycle (PCLK).

a. PLL operation requires BYPASS=1 and PLL_EN=1.

Table 3. ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	3.9	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} +0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} +0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	LQFP 32 Thermal resistance junction to ambient JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	LQFP 32 Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1

Table 5. DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{PP}	Peak-to-Peak Input Voltage (PCLK)	250			mV	LVPECL
V_{CMR}^a	Common Mode Range (PCLK)	1.0		$V_{CC}-0.6$	V	LVPECL
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -24\text{ mA}^b$
V_{OL}	Output Low Voltage ^c			0.55	V	$I_{OL} = 24\text{ mA}$
				0.30	V	$I_{OL} = 12\text{ mA}$
Z_{OUT}	Output Impedance		14 - 17		Ω	
I_{IN}	Input Current ^d			± 200	μA	$V_{IN} = V_{CC}$ or GND
I_{CC_PLL}	Maximum PLL Supply Current		12	20	mA	V_{CC_PLL} Pin
I_{CCQ}	Maximum Quiescent Supply Current		13	20	mA	All V_{CC} Pins

a V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.

b The MPC9658 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines.

c The MPC9658 output levels are compatible to the MPC958 output levels.

d Inputs have pull-down resistors affecting the input current.

Table 6. AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input reference frequency	100		250	MHz	PLL locked
	PLL mode, external feedback	50		125	MHz	PLL locked
	Input reference frequency in PLL bypass mode ^d	0		250	MHz	
f_{VCO}	VCO lock frequency range ^e	200		500	MHz	
f_{MAX}	Output Frequency	100		250	MHz	PLL locked
		50		125	MHz	PLL locked
V_{PP}	Peak-to-peak input voltage (PCLK)	500		1000	mV	LVPECL
V_{CMR}^f	Common Mode Range (PCLK)	1.2		$V_{CC}-0.9$	V	LVPECL
$t_{PW,MIN}$	Input Reference Pulse Width ^g	2.0			ns	
$t_{(\varnothing)}$	Propagation Delay (static phase offset)	PCLK to FB_IN $f_{REF}=100$ MHz any frequency	-70 -125	+80 +125	ps ps	PLL locked
t_{PD}	Propagation Delay (PLL and divider bypass)	PCLK to Q0-9	1.0	4.0	ns	
$t_{sk(O)}$	Output-to-output Skew ^h			120	ps	
DC	Output Duty Cycle ⁱ	$(T/2)-400$	$T/2$	$(T/2)+400$	ps	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time			7.0	ns	
$t_{PZL, LZ}$	Output Enable Time			6.0	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter			80	ps	
$t_{JIT(PER)}$	Period Jitter			80	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter	$f_{VCO}=500$ MHz and $\div 2$ feedback, RMS (1σ) ^j $f_{VCO}=500$ MHz and $\div 4$ feedback, RMS (1σ)		5.5	ps	
				6.5	ps	
BW	PLL closed loop bandwidth ^k	$\div 2$ feedback ^c $\div 4$ feedback ^d	6-20		MHz	
			2-8		MHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

a AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b $\div 2$ PLL feedback (high frequency range) requires $VCO\_SEL=0$, $PLL\_EN=1$, $BYPASS=1$ and $MR/\overline{OE}=0$.

c $\div 4$ PLL feedback (low frequency range) requires $VCO\_SEL=1$, $PLL\_EN=1$, $BYPASS=1$ and $MR/\overline{OE}=0$.

d In bypass mode, the MPC9658 divides the input reference clock.

e The input frequency f_{ref} must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.

f V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\varnothing)}$.

g Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF,MAX} = 100\% - DC_{REF,MIN}$.

h See application section for part-to-part skew calculation in PLL zero-delay mode.

i Output duty cycle is $DC = (0.5 \pm 400 \text{ ps} \cdot f_{OUT}) \cdot 100\%$. E.g. the DC range at $f_{OUT}=100\text{MHz}$ is $46\% < DC < 54\%$. T = output period.

j See application section for a jitter calculation for other confidence factors than 1σ and a characteristic for other VCO frequencies.

k -3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Programming the MPC9658

The MPC9658 supports output clock frequencies from 50 to 250 MHz. Two different feedback divider configurations can be used to achieve the desired frequency operation range. The feedback divider (VCO_SEL) should be used to situate the VCO in the frequency lock range between 200 and 500 MHz

for stable and optimal operation. Two operating frequency ranges are supported: 50 to 125 MHz and 100 to 250 MHz. Table 7 illustrates the configurations supported by the MPC9658. PLL zero-delay is supported if $BYPASS=1$, $PLL\_EN=1$ and the input frequency is within the specified PLL reference frequency range.

Table 7. MPC9658 Configurations (QFB connected to FB_IN)

BYPASS	PLL_EN	VCO_SEL	Operation	Frequency		
				Ratio	Output range (f _{Q0-9})	VCO
0	X	X	Test mode: PLL and divider bypass	$f_{Q0-9} = f_{REF}$	0-250 MHz	n/a
1	0	0	Test mode: PLL bypass	$f_{Q0-9} = f_{REF} \div 2$	0-125 MHz	n/a
1	0	1	Test mode: PLL bypass	$f_{Q0-9} = f_{REF} \div 4$	0-62.5 MHz	n/a
1	1	0	PLL mode (high frequency range)	$f_{Q0-9} = f_{REF}$	100 to 250 MHz	$f_{VCO} = f_{REF} \cdot 2$
1	1	1	PLL mode (low frequency range)	$f_{Q0-9} = f_{REF}$	50 to 125 MHz	$f_{VCO} = f_{REF} \cdot 4$

Power Supply Filtering

The MPC9658 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC9658 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9658. Figure 3 illustrates a typical power supply filter scheme. The MPC9658 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F . From the data sheet the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 12 mA (20 mA maximum), assuming that a minimum of 2.835V must be maintained on the V_{CC_PLL} pin.

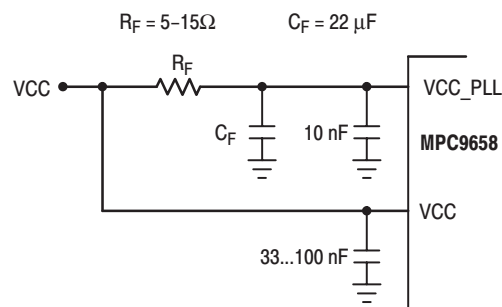


Figure 3. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3 “ V_{CC_PLL} Power Supply Filter”, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9658 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9658 in zero-delay applications

Nested clock trees are typical applications for the MPC9658. Designs using the MPC9658 as LVCMOS PLL fan-out buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fan-out buffers. The external feedback option of the MPC9658 clock driver allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device (the propagation delay through the device is virtually eliminated). The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of part-to-part skew

The MPC9658 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9658 are connected together, the maximum overall timing uncertainty from the common PCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD, LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

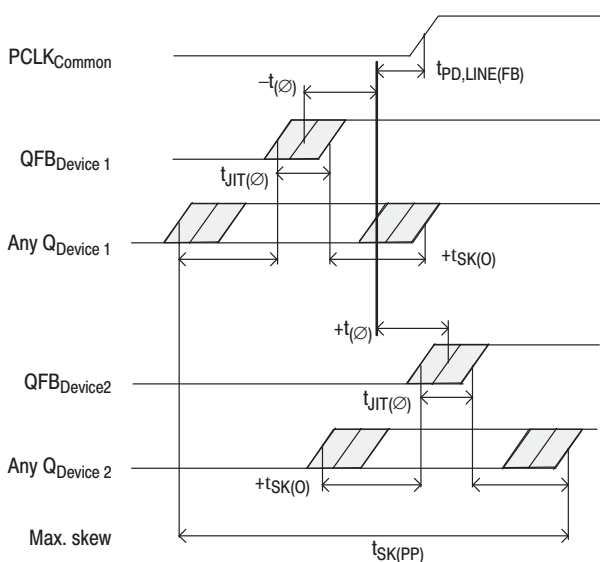


Figure 4. MPC9658 max. device-to-device skew

Due to the statistical nature of I/O jitter a RMS value (1σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

Table 8. Confidence Factor CF

CF	Probability of clock edge within the distribution
$\pm 1\sigma$	0.68268948
$\pm 2\sigma$	0.95449988
$\pm 3\sigma$	0.99730007
$\pm 4\sigma$	0.99993663
$\pm 5\sigma$	0.99999943
$\pm 6\sigma$	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% ($\pm 3\sigma$) is assumed, resulting in a worst case timing uncertainty from input to any output of -214 ps to 224 ps relative to PCLK ($f_{REF} = 100\text{ MHz}$, $FB = \pm 4$, $t_{jit(\varnothing)} = 8\text{ ps RMS}$ at $f_{VCO} = 400\text{ MHz}$):

$$t_{SK(PP)} = [-70\text{ps}...80\text{ps}] + [-120\text{ps}...120\text{ps}] + [(8\text{ps} \cdot -3)...(8\text{ps} \cdot 3)] + t_{PD, LINE(FB)}$$

$$t_{SK(PP)} = [-214\text{ps}...224\text{ps}] + t_{PD, LINE(FB)}$$

Due to the frequency dependence of the I/O jitter, figure 5 can be used for a more precise timing performance analysis.

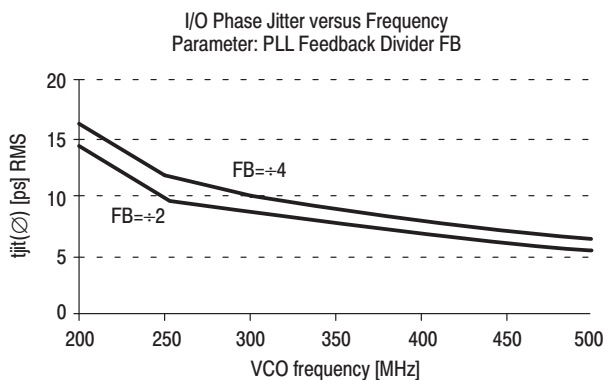


Figure 5. Max. I/O Jitter versus frequency

Driving Transmission Lines

The MPC9658 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC} \pm 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9658 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 6 "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in

parallel. When taken to its extreme the fanout of the MPC9658 clock driver is effectively doubled due to its capability to drive multiple lines.

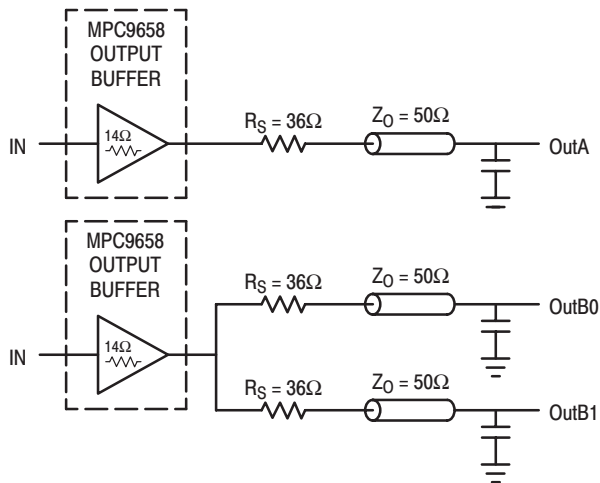


Figure 6. Single versus Dual Transmission Lines

The waveform plots in Figure 7 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9658 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9658. The output waveform in Figure 7 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned} V_L &= V_S (Z_0 \div (R_S + R_0 + Z_0)) \\ Z_0 &= 50\Omega \parallel 50\Omega \\ R_S &= 36\Omega \parallel 36\Omega \\ R_0 &= 14\Omega \\ V_L &= 3.0 (25 \div (18 + 14 + 25)) \\ &= 1.31V \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

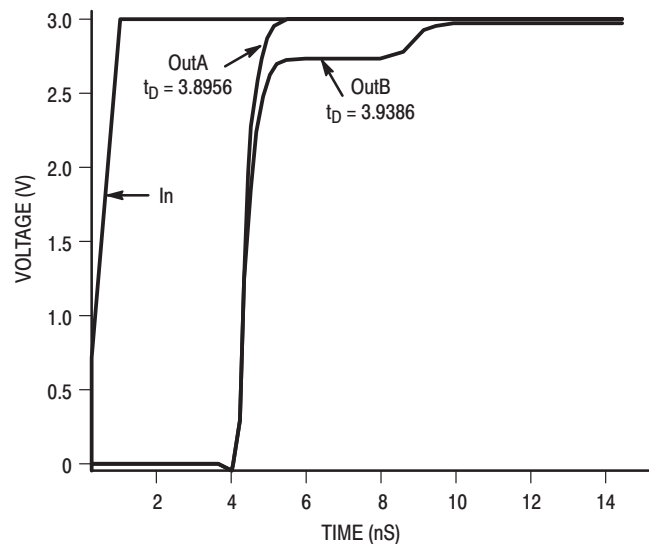


Figure 7. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 8 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

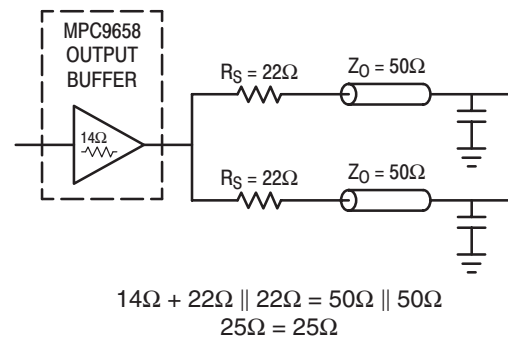


Figure 8. Optimized Dual Line Termination

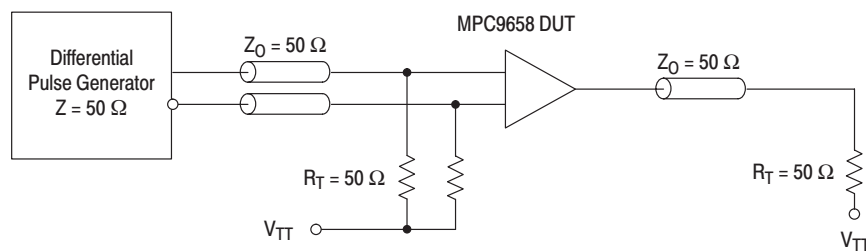
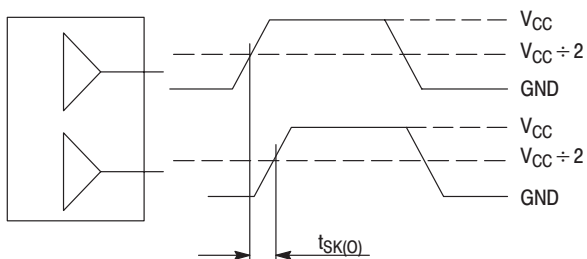
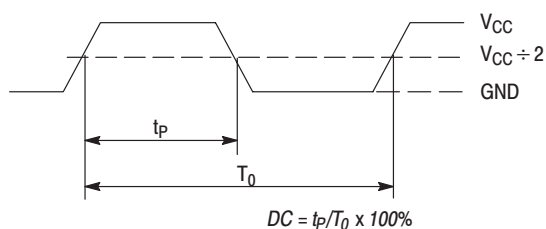


Figure 9. PCLK MPC9658 AC test reference



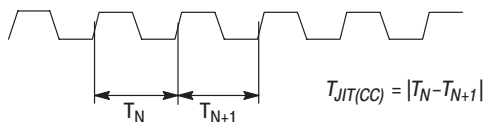
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 10. Output-to-output Skew $t_{SK(O)}$



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 12. Output Duty Cycle (DC)



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 14. Cycle-to-cycle Jitter

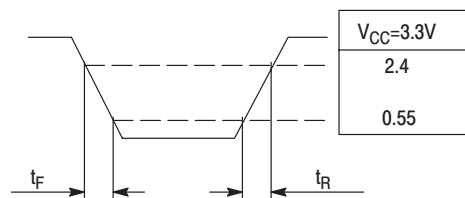


Figure 16. Output Transition Time Test Reference

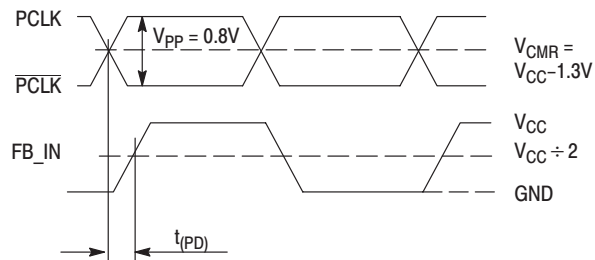
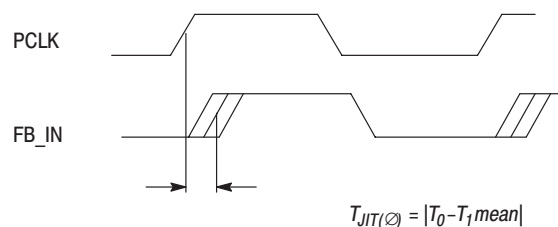
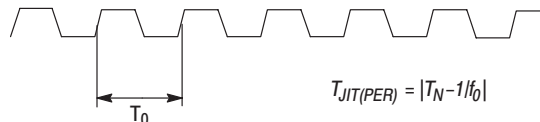


Figure 11. Propagation delay (t_{PD}), static phase offset) test reference



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 13. I/O Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 15. Period Jitter

Chapter Six

LVCMOS Fanout Buffer Data Sheets

LVCMOS Fanout Buffer Device Index

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1:6 PCI Clock Generator/ Fanout Buffer

The MPC905 is a six output clock generation device targeted to provide the clocks required in a 3.3V or 5.0V PCI environment. The device operates from a 3.3V supply and can interface to either a TTL input or an external crystal. The inputs to the device can be driven with 5.0V when the V_{CC} is at 3.3V. The outputs of the MPC905 meet all of the specifications of the PCI standard.

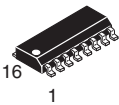
- Six Low Skew Outputs
- Synchronous Output Enables for Power Management
- Low Voltage Operation
- XTAL Oscillator Interface
- 16-Lead SOIC Package
- 5.0V Tolerant Enable Inputs

The MPC905 device is targeted for PCI bus or processor bus environments with up to 12 clock loads. Each of the six outputs on the MPC905 can drive two series terminated 50 Ω transmission lines. This capability effectively makes the MPC905 a 1:12 fanout buffer.

The MPC905 offers two synchronous enable inputs to allow users flexibility in developing power management features for their designs. Both enable signals are active HIGH inputs. A logic '0' on the Enable1 will pull outputs 0 to 4 into the logic '0' state. A logic '1' on the Enable1 input will result in outputs 0 to 4 to be toggling. A logic '0' on Enable2 will cause output BLK5 to a logic '0' state, whereas a logic '1' on Enable2 will cause output BLK5 to toggle. The oscillator remains on.

MPC905

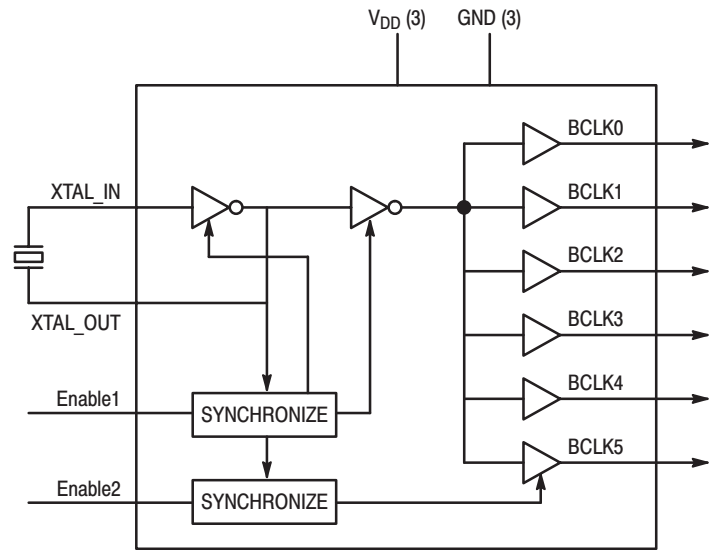
1:6 PCI CLOCK GENERATOR/ FANOUT BUFFER



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B

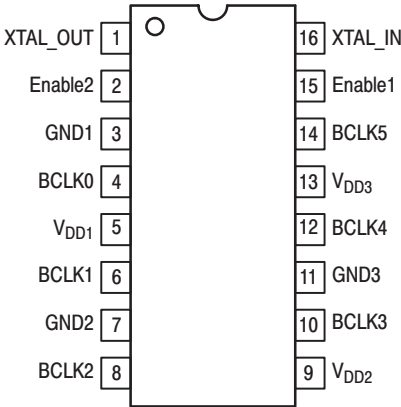
6

The Enable2 input can be used to disable any high power device for system power savings during periods of inactivity. Both enable inputs are synchronized internal to the chip so that the output disabling will happen only when the outputs are already LOW. This feature guarantees no runt pulses will be generated during enabling and disabling.



Rev 2

Pinout: 16-Lead Plastic Package (Top View)



PIN CONFIGURATIONS

Pin	I/O	Type	Function
XTAL_IN, XTAL_OUT	Input	Analog	Crystal Oscillator Terminals
Enable1, Enable2	Input	LVC MOS	Output Enable
BCLK0 – BCLK5	Output	LVC MOS	Clock Outputs
V _{DD}		Supply	Positive Power Supply
GND		Supply	Negative Power Supply

FUNCTION TABLE

ENABLE1	ENABLE2	Outputs 0 to 4	Output 5	OSC (On/Off)
0	0	Low	Low	ON
0	1	Low	Toggling	ON
1	0	Toggling	Low	ON
1	1	Toggling	Toggling	ON

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V _{DD}	Supply Voltage	–0.5	4.6	V
V _{IN}	Input Voltage	–0.5	V _{CC} + 0.5	V
T _{oper}	Operating Temperature Range	0	+70	°C
T _{stg}	Storage Temperature Range	–65	+150	°C
T _{sol}	Soldering Temperature Range (10 Sec)		+260	°C
T _j	Junction Temperature Range		+125	°C
ESD	Static Discharge Voltage	1500		V
I _{Latch}	Latch Up Current	50		mA

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
T _A	Ambient Temperature Range	0	70	°C
V _{CC}	Positive Supply Voltage (Functional Range)	3.0	3.6	V
t _{DCin}	T _{high} (at XTAL_IN Input) T _{low} (at XTAL_IN Input)	0.44T ¹ 0.44T ¹	0.56T ¹ 0.56T ¹	T = Period

1. When using External Source for reference, requirement to meet PCI clock duty cycle requirement on the output.

DC CHARACTERISTICS (T_A = 0–70°C; V_{DD} = 3.3V ±0.3V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V _{IH}	High Level Input Voltage	2.0		5.5 ²	V	
V _{IL}	Low Level Input Voltage			0.8	V	
V _{OH}	High Level Output Voltage	2.4			V	I _{OH} = –36mA ¹
V _{OL}	Low Level Output Voltage			0.4	V	I _{OL} = 36mA ¹
I _{IH}	Input High Current			2.5 ²	μA	
I _{IL}	Input Low Current			2.5	μA	
I _{CC}	Power Supply Current		20 37 78	45 95	μA mA mA	DC 33MHz 66MHz
C _{IN}	Input Capacitance			9.0 4.5	pF	XTAL_IN Others

- The MPC905 can drive 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to V_{TT} = V_{CC}/2. Alternately, the device drives up to two 50Ω series terminated transmission lines per output.
- XTAL_IN input will sink up to 10mA when driven to 5.5V. There are no reliability concerns associated with the condition. Note that the Enable1 input must be a logic HIGH. Do not take the Enable1 input to a logic LOW with >V_{CC} volts on the XTAL_IN input.

AC CHARACTERISTICS ($T_A = 0-70^{\circ}\text{C}$; $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Operating Frequency Using External Crystal Using External Clock Source	– DC		50 100	MHz	
t_{pw}	Output Pulse Width HIGH (Above 2.0V) LOW (Below 0.8V) HIGH (Above 2.0V) LOW (Below 0.8V)	$0.40T^1$ $0.40T^1$ $0.45T^2$ $0.45T^2$		$0.60T^1$ $0.60T^1$ $0.55T^2$ $0.55T^2$		$T = \text{Periods}$
t_{per}	Output Period	$T - 400\text{ps}$				$T = \text{Desired Period}$
t_{os}	Output-to-Output Skew Rising Edges Falling Edges			400 500	ps	
t_r, t_f	Rise/Fall Times (Slew Rate)	1		4	V/ns	Series Terminated Transmission Lines
t_{EN}	Enable Time Enable1 Enable2			5 4	ms Cycles	
t_{DIS}	Disable Time Enable1 Enable2			4 4	Cycles	
A_{osc}	XTAL_IN to XTAL_OUT Oscillator Gain	6			db	
Phase	Loop Phase Shift Modulo $360^{\circ} +$	30			Degrees	

1. Assuming input duty cycle specs from Recommended Operating Conditions table are met.
2. Assuming external crystal or 50% duty cycle external reference is used.

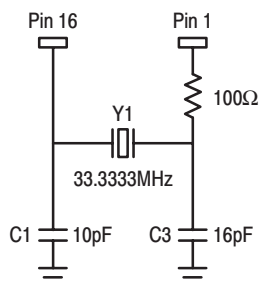


Figure 1. Crystal Oscillator Interface
(Fundamental)

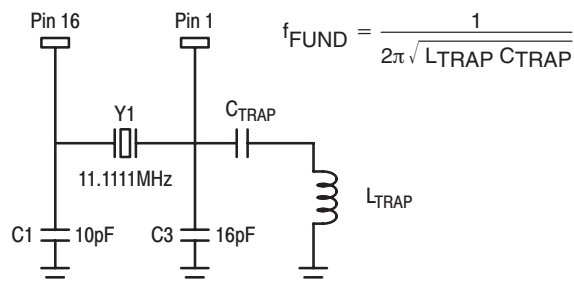


Figure 2. Crystal Oscillator Interface
(3rd Overtone)

Table 1. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Parallel Resonance*
Frequency Tolerance	$\pm 75\text{ppm}$ at 25°C
Frequency/Temperature Stability	$\pm 150\text{ppm}$ 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	$100\mu\text{W}$
Aging	5ppm/Yr (First 3 Years)

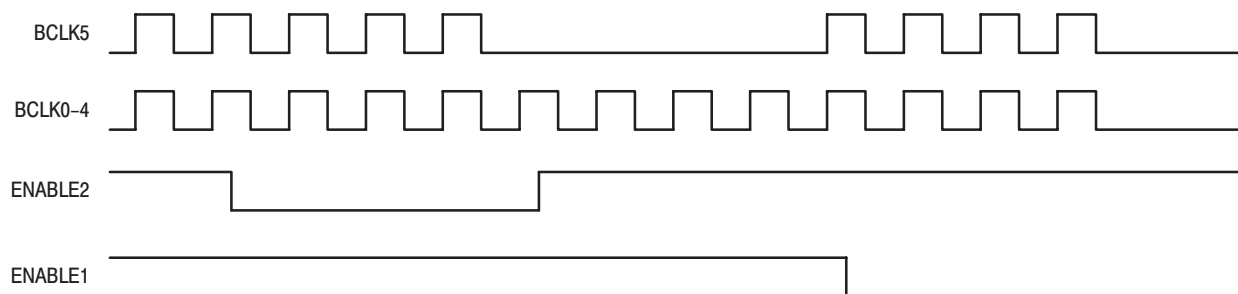


Figure 3. Enable Timing Diagram

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC905 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC905 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fan-out of the MPC905 clock driver is effectively doubled due to its capability to drive multiple lines.

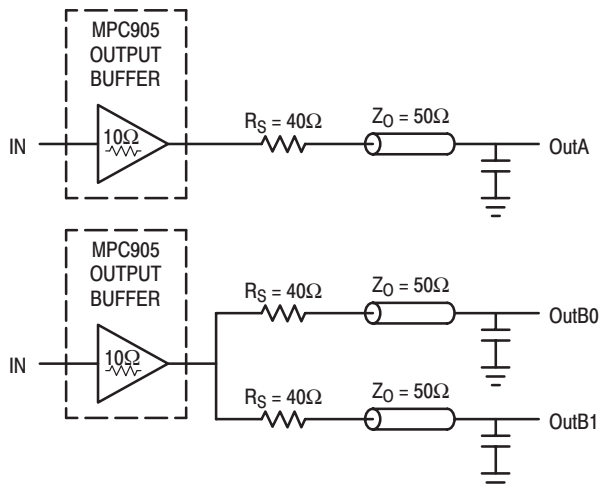


Figure 4. Single versus Dual Transmission Lines

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC905 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 40Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_o / R_s + R_o + Z_o) = 3.0 (25/55) = 1.36V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.73V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

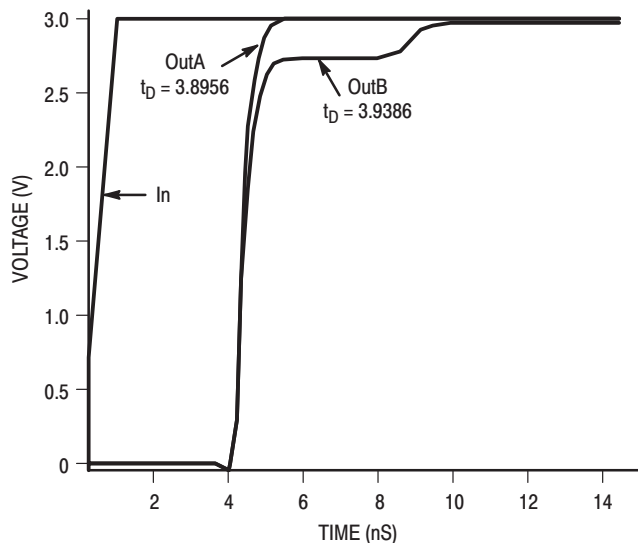


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

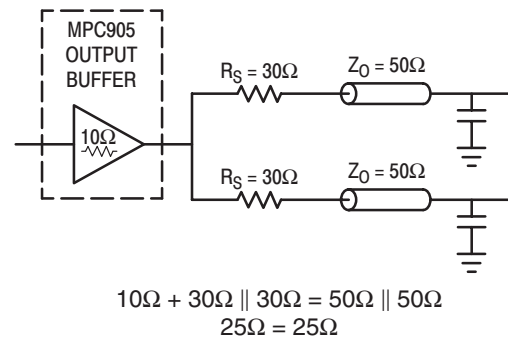


Figure 6. Optimized Dual Line Termination

Low Voltage 1:18 Clock Distribution Chip

The MPC940L is a 1:18 low voltage clock distribution chip with 2.5V or 3.3V LVCMOS output capabilities. The device features the capability to select either a differential LVPECL or an LVCMOS compatible input. The 18 outputs are 2.5V or 3.3V LVCMOS compatible and feature the drive strength to drive 50Ω series or parallel terminated transmission lines. With output-to-output skews of 150ps, the MPC940L is ideal as a clock distribution chip for the most demanding of synchronous systems. The 2.5V outputs also make the device ideal for supplying clocks for a high performance microprocessor based design. For a similar device at a lower price/performance point the reader is referred to the MPC9109.

- LVPECL or LVCMOS Clock Input
- 2.5V LVCMOS Outputs for Pentium II Microprocessor Support
- 150ps Maximum Output-to-Output Skew
- Maximum Output Frequency of 250MHz
- 32-Lead LQFP Packaging
- Dual or Single Supply Device:
 - Dual V_{CC} Supply Voltage, 3.3V Core and 2.5V Output
 - Single 3.3V V_{CC} Supply Voltage for 3.3V Outputs
 - Single 2.5V V_{CC} Supply Voltage for 2.5V I/O

With a low output impedance ($\approx 20\Omega$), in both the HIGH and LOW logic states, the output buffers of the MPC940L are ideal for driving series terminated transmission lines. With a 20Ω output impedance the 940L has the capability of driving two series terminated lines from each output. This gives the device an effective fanout of 1:36. If a lower output impedance is desired please see the MPC942 data sheet.

The differential LVPECL inputs of the MPC940L allow the device to interface directly with a LVPECL fanout buffer like the MC100EP111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used to provide for a test clock interface as well as the primary system clock. A logic HIGH on the LVCMOS_CLK_Sel pin will select the LVCMOS level clock input. All inputs of the MPC940L have internal pullup/pulldown resistor so they can be left open if unused.

The MPC940L is a single or dual supply device. The device power supply offers a high degree of flexibility. The device can operate with a 3.3V core and 3.3V output, a 3.3V core and 2.5V outputs as well as a 2.5V core and 2.5V outputs. The 32-lead LQFP package was chosen to optimize performance, board space and cost of the device. The 32-lead LQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

MPC940L

**LOW VOLTAGE
1:18 CLOCK
DISTRIBUTION CHIP**



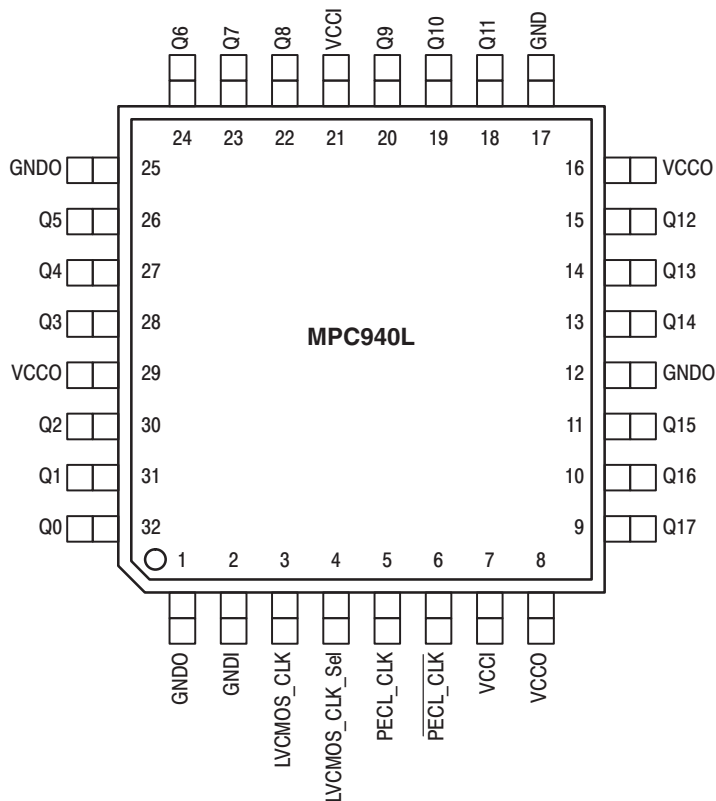
FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A

6

LOGIC DIAGRAM



Pinout: 32-Lead TQFP (Top View)



FUNCTION TABLE

LVC MOS_CLK_Sel	Input
0	PECL_CLK
1	LVC MOS_CLK

POWER SUPPLY VOLTAGES

Supply Pin	Voltage Level
VCCI	2.5V or 3.3V ± 5%
VCCO	2.5V or 3.3V ± 5%

PIN CONFIGURATIONS

Pin	I/O	Type	Function
PECL_CLK PECL_CLK	Input	LVPECL	Reference Clock Input
LVC MOS_CLK	Input	LVC MOS	Alternative Reference Clock Input
LVC MOS_CLK_SEL	Input	LVC MOS	Selects Clock Source
Q0–Q17	Output	LVC MOS	Clock Outputs
VCCO		Supply	Output Positive Power Supply
VCCI		Supply	Core Positive Power Supply
GNDO		Supply	Output Negative Power Supply
GNDI		Supply	Core Negative Power Supply

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	3.6	V
V_I	Input Voltage	-0.3	$V_{DD} + 0.3$	V
I_{IN}	Input Current		± 20	mA
T_{Stor}	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CCI} = 3.3\text{V} \pm 5\%$; $V_{CCO} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage CMOS_CLK	2.4		V_{CCI}	V	
V_{IL}	Input LOW Voltage CMOS_CLK			0.8	V	
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK	500		1000	mV	
V_{CMR}	Common Mode Range PECL_CLK	$V_{CC} - 1.4$		$V_{CC} - 0.6$	V	
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -20\text{mA}$
V_{OL}	Output LOW Voltage			0.5	V	$I_{OH} = 20\text{mA}$
I_{IN}	Input Current			± 200	μA	
C_{IN}	Input Capacitance		4.0		pF	
C_{pd}	Power Dissipation Capacitance		10		pF	per output
Z_{OUT}	Output Impedance	18	23	28	Ω	
I_{CC}	Maximum Quiescent Supply Current		0.5	1.0	mA	

AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CCI} = 3.3\text{V} \pm 5\%$; $V_{CCO} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency			250	MHz	
t_{PLH}	Propagation Delay PECL_CLK $\leq 150\text{MHz}$ CMOS_CLK $\leq 150\text{MHz}$	2.0 1.8	2.7 2.5	3.4 3.0	ns	Note 1.
t_{PLH}	Propagation Delay PECL_CLK $> 150\text{MHz}$ CMOS_CLK $> 150\text{MHz}$	2.0 1.8	2.9 2.4	3.7 3.2	ns	
$t_{sk(o)}$	Output-to-Output Skew PECL_CLK CMOS_CLK			150 150	ps	Note 1.
$t_{sk(pp)}$	Part-to-Part Skew PECL_CLK $< 150\text{MHz}$ CMOS_CLK $< 150\text{MHz}$			1.4 1.2	ns	Notes 1., 2.
$t_{sk(pp)}$	Part-to-Part Skew PECL_CLK $> 150\text{MHz}$ CMOS_CLK $> 150\text{MHz}$			1.7 1.4	ns	Notes 1., 2.
$t_{sk(pp)}$	Part-to-Part Skew PECL_CLK CMOS_CLK			850 750	ps	Notes 1., 3.
DC	Output Duty Cycle $f_{CLK} < 134\text{ MHz}$ $f_{CLK} \leq 250\text{ MHz}$	45 40	50 50	55 60	% %	Input DC = 50% Input DC = 50%
t_r, t_f	Output Rise/Fall Time	0.3		1.1	ns	0.5 – 2.4 V

1. Tested using standard input levels, Production tested @ 150MHz.

2. Across temperature and voltage ranges, Includes output skew.

3. For a specific temperature and voltage, Includes output skew.

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CCI} = 3.3\text{V} \pm 5\%$; $V_{CCO} = 2.5\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage CMOS_CLK	2.4		V_{CCI}	V	
V_{IL}	Input LOW Voltage CMOS_CLK			0.8	V	
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK	500		1000	mV	
V_{CMR}	Common Mode Range PECL_CLK	$V_{CC} - 1.4$		$V_{CC} - 0.6$	V	
V_{OH}	Output HIGH Voltage	1.8			V	$I_{OH} = -20\text{mA}$
V_{OL}	Output LOW Voltage			0.5	V	$I_{OH} = 20\text{mA}$
I_{IN}	Input Current			± 200	μA	
C_{IN}	Input Capacitance		4.0		pF	
C_{pd}	Power Dissipation Capacitance		10		pF	per output
Z_{OUT}	Output Impedance		23		Ω	
I_{CC}	Maximum Quiescent Supply Current		0.5	1.0	mA	

AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CCI} = 3.3\text{V} \pm 5\%$; $V_{CCO} = 2.5\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency			250	MHz	
t_{PLH}	Propagation Delay PECL_CLK $\leq 150\text{MHz}$ CMOS_CLK $\leq 150\text{MHz}$	2.0 1.7	2.8 2.5	3.5 3.0	ns	Note 1.
t_{PLH}	Propagation Delay PECL_CLK $> 150\text{MHz}$ CMOS_CLK $> 150\text{MHz}$	2.0 1.8	2.9 2.5	3.8 3.3	ns	
$t_{sk(o)}$	Output-to-Output Skew PECL_CLK CMOS_CLK			150 150	ps	Note 1.
$t_{sk(pp)}$	Part-to-Part Skew PECL_CLK $< 150\text{MHz}$ CMOS_CLK $< 150\text{MHz}$			1.5 1.3	ns	Notes 1., 2.
$t_{sk(pp)}$	Part-to-Part Skew PECL_CLK $> 150\text{MHz}$ CMOS_CLK $> 150\text{MHz}$			1.8 1.5	ns	Notes 1., 2.
$t_{sk(pp)}$	Part-to-Part Skew PECL_CLK CMOS_CLK			850 750	ps	Notes 1., 3.
DC	Output Duty Cycle $f_{CLK} < 134\text{ MHz}$ $f_{CLK} \leq 250\text{ MHz}$	45 40	50 50	55 60	% %	Input DC = 50% Input DC = 50%
t_r, t_f	Output Rise/Fall Time	0.3		1.2	ns	0.5 – 1.8 V

1. Tested using standard input levels, Production tested @ 150MHz.
2. Across temperature and voltage ranges, Includes output skew.
3. For a specific temperature and voltage, Includes output skew.

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CCI} = 2.5\text{V} \pm 5\%$; $V_{CCO} = 2.5\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage CMOS_CLK	2.0		V_{CCI}	V	
V_{IL}	Input LOW Voltage CMOS_CLK			0.8	V	
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK	500		1000	mV	
V_{CMR}	Common Mode Range PECL_CLK	$V_{CC}-1.0$		$V_{CC}-0.6$	V	
V_{OH}	Output HIGH Voltage	1.8			V	$I_{OH} = -12\text{mA}$
V_{OL}	Output LOW Voltage			0.5	V	$I_{OH} = 12\text{mA}$
I_{IN}	Input Current			± 200	μA	
C_{IN}	Input Capacitance		4.0		pF	
C_{pd}	Power Dissipation Capacitance		10		pF	per output
Z_{OUT}	Output Impedance	18	23	28	Ω	
I_{CC}	Maximum Quiescent Supply Current		0.5	1.0	mA	

AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CCI} = 2.5\text{V} \pm 5\%$; $V_{CCO} = 2.5\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency			200	MHz	
t_{PLH}	Propagation Delay PECL_CLK $\leq 150\text{MHz}$ CMOS_CLK $\leq 150\text{MHz}$	2.6 2.3	4.0 3.1	5.2 4.0	ns	Note 1.
t_{PLH}	Propagation Delay PECL_CLK $> 150\text{MHz}$ CMOS_CLK $> 150\text{MHz}$	2.8 2.3	3.8 3.1	5.0 4.0	ns	
$t_{sk(o)}$	Output-to-Output Skew PECL_CLK CMOS_CLK			200 200	ps	Note 1.
$t_{sk(pp)}$	Part-to-Part Skew PECL_CLK $< 150\text{MHz}$ CMOS_CLK $< 150\text{MHz}$			2.6 1.7	ns	Notes 1., 2.
$t_{sk(pp)}$	Part-to-Part Skew PECL_CLK $> 150\text{MHz}$ CMOS_CLK $> 150\text{MHz}$			2.2 1.7	ns	Notes 1., 2.
$t_{sk(pp)}$	Part-to-Part Skew PECL_CLK CMOS_CLK			1.2 1.0	ns	Notes 1., 3.
DC	Output Duty Cycle $f_{CLK} < 134\text{ MHz}$ $f_{CLK} \leq 250\text{ MHz}$	45 40	50 50	55 60	% %	Input DC = 50% Input DC = 50%
t_r, t_f	Output Rise/Fall Time	0.3		1.2	ns	0.5 – 1.8 V

1. Tested using standard input levels, Production tested @ 150MHz.
2. Across temperature and voltage ranges, Includes output skew.
3. For a specific temperature and voltage, Includes output skew.

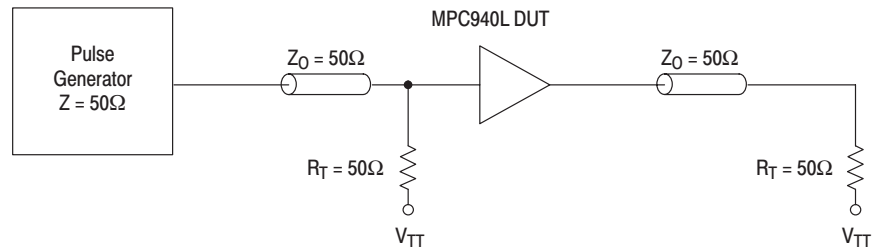


Figure 1. LVC MOS_CLK MPC940L AC test reference for $V_{CC} = 3.3V$ and $V_{CC} = 2.5V$

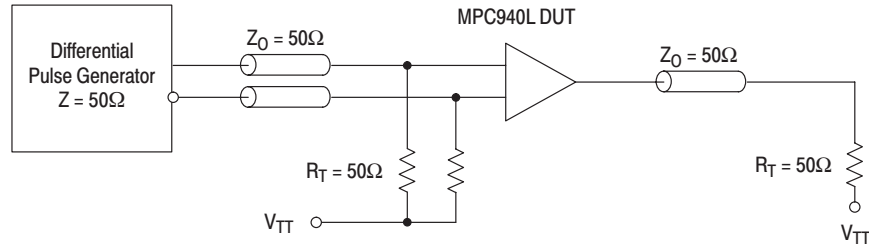


Figure 2. PECL_CLK MPC940L AC test reference for $V_{CC} = 3.3V$ and $V_{CC} = 2.5V$

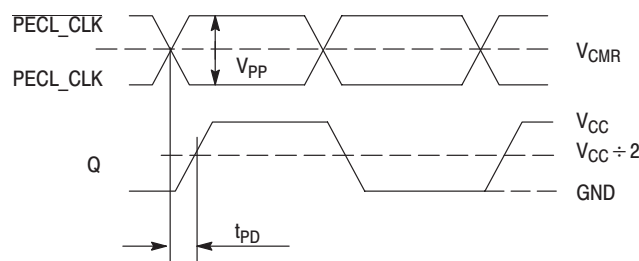


Figure 3. Propagation delay (t_{pD}) test reference

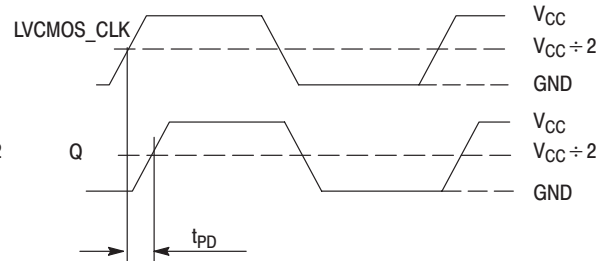
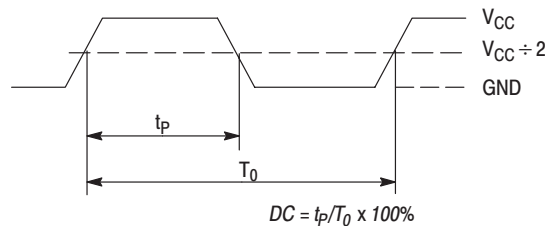
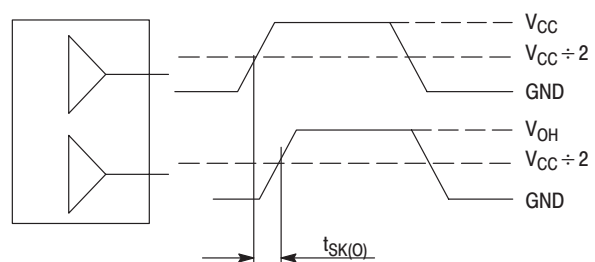


Figure 4. LVC MOS Propagation delay (t_{pD}) test reference



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 5. Output Duty Cycle (DC)



The pin-to-pin skew is defined as the worst case difference in propagation delay between any two similar delay path within a single device

Figure 6. Output-to-output Skew $t_{SK(O)}$

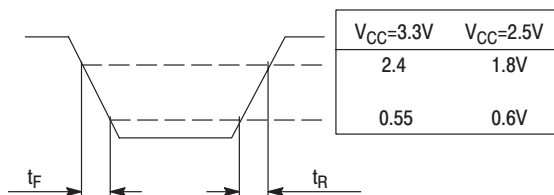


Figure 7. Output Transition Time Test Reference

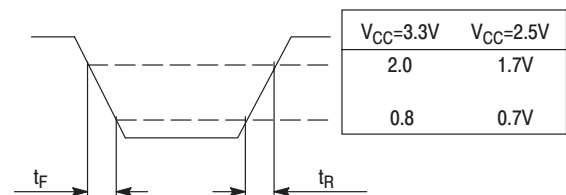


Figure 8. Input Transition Time Test Reference

Low Voltage 1:27 Clock Distribution Chip

The MPC941 is a 1:27 low voltage clock distribution chip. The device features the capability to select either a differential LVPECL or an LVCMOS compatible input. The 27 outputs are LVCMOS compatible and feature the drive strength to drive 50Ω series or parallel terminated transmission lines. With output-to-output skews of 250ps, the MPC941 is ideal as a clock distribution chip for the most demanding of synchronous systems. For a similar product with a smaller number of outputs, please consult the MPC940 data sheet.

- LVPECL or LVCMOS Clock Input
- 250ps Maximum Output-to-Output Skew
- Drives Up to 54 Independent Clock Lines
- Maximum Output Frequency of 250MHz
- High Impedance Output Enable
- Extended Temperature Range: -40°C to +85°C
- 48-Lead LQFP Packaging
- 3.3V or 2.5V V_{CC} Supply Voltage

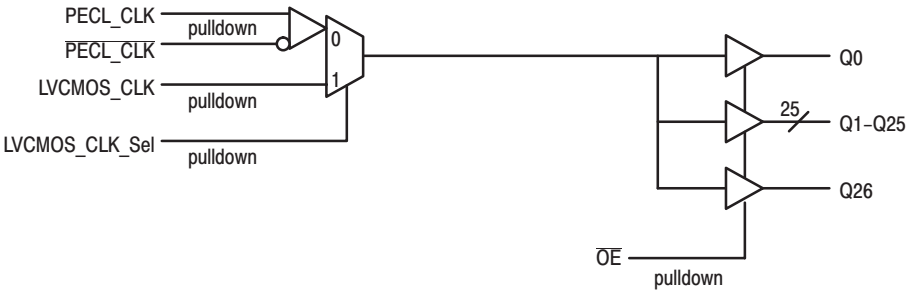
With a low output impedance, in both the HIGH and LOW logic states, the output buffers of the MPC941 are ideal for driving series terminated transmission lines. More specifically, each of the 27 MPC941 outputs can drive two series terminated 50Ω transmission lines. With this capability, the MPC941 has an effective fanout of 1:54. With this level of fanout, the MPC941 provides enough copies of low skew clocks for most high performance synchronous systems.

The differential LVPECL inputs of the MPC941 allow the device to interface directly with an LVPECL fanout buffer like the MC100EP111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used as a test clock interface as well as the primary system clock. A logic HIGH on the LVCMOS_CLK_Sel pin will select the LVCMOS level clock input.

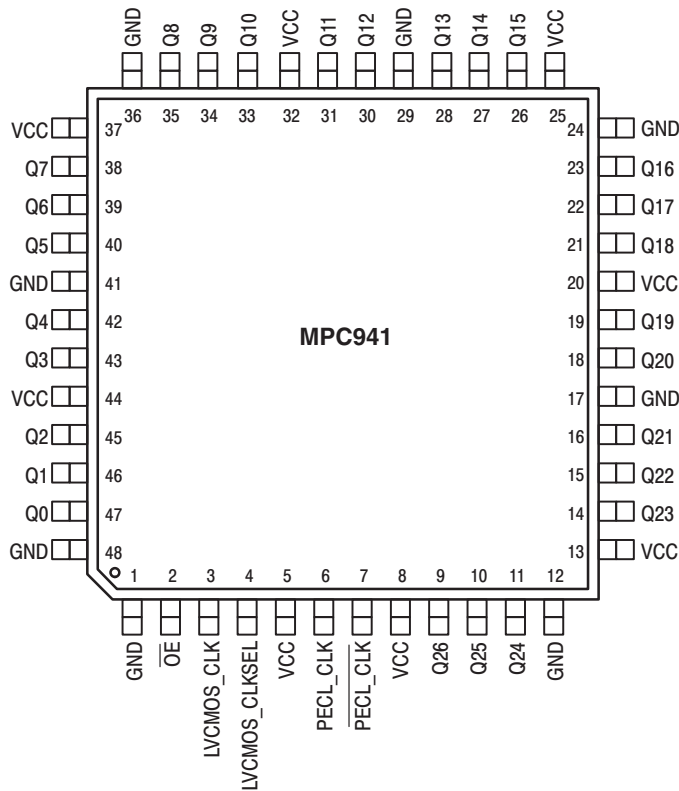
The MPC941 is fully 3.3V and 2.5V compatible. The 48-lead LQFP package was chosen to optimize performance, board space and cost of the device. The 48-lead LQFP has a 7x7mm body size.

MPC941**LOW VOLTAGE 3.3V/2.5V
1:27 CLOCK
DISTRIBUTION CHIP****FA SUFFIX**
48-LEAD LQFP PACKAGE
CASE 932**6**

LOGIC DIAGRAM



Pinout: 48-Lead QFP (Top View)



FUNCTION TABLE

LVCOS_CLK_Sel	Input
0	PECL_CLK
1	LVCOS_CLK

Table 1: PIN CONFIGURATIONS

Pin	I/O	Type	Function
PECL_CLK, PECL_CLK	Input	LVPECL	LVPECL differential reference clock inputs
LVCOS_CLK	Input	LVCOS	Alternative reference clock input
LVCOS_CLK_Sel	Input	LVCOS	Input reference clock select
OE	Input	LVCOS	Output tristate control
GND		Supply	Negative voltage supply output bank (GND)
VCC		Supply	Positive voltage supply
Q0 - Q26	Output	LVCOS	Clock outputs

Table 2: ABSOLUTE MAXIMUM RATINGS*

Symbol	Characteristics	Min	Max	Unit
V _{CC}	Supply Voltage	-0.3	3.6	V
V _{IN}	DC Input Voltage	-0.3	V _{CC} +0.3	V
V _{OUT}	DC Output Voltage	-0.3	V _{CC} +0.3	V
I _{IN}	DC Input Current		±20	mA
I _{OUT}	DC Output Current		±50	mA
T _S	Storage temperature	-40	125	°C

* Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 3: DC CHARACTERISTICS (V_{CC} = 3.3V ± 5%, T_A = -40 to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{IH}	Input high voltage LVC MOS_CLK	2.0		V _{CC} + 0.3	V	LVC MOS
V _{IL}	Input low voltage LVC MOS_CLK	-0.3		0.8	V	LVC MOS
I _{IN}	Input current			±120 ^a	μA	
V _{PP}	Peak-to-peak input voltage PECL_CLK, PECL_CLK	500			mV	LVPECL
V _{CMR}	Common Mode Range PECL_CLK, PECL_CLK	1.2		V _{CC} -0.8	V	LVPECL
V _{OH}	Output High Voltage	2.4			V	I _{OH} =-24 mA ^b
V _{OL}	Output Low Voltage			0.55 0.40	V V	I _{OL} = 24mA ^b I _{OL} =12mA
I _{OZ}	Output tristate leakage current			100	μA	
Z _{OUT}	Output impedance		14 - 17		Ω	
C _{PD}	Power Dissipation Capacitance		7-8	10	pF	Per Output
C _{IN}	Input capacitance		4.0		pF	
I _{CCQ}	Maximum Quiescent Supply Current			5	mA	All V _{CC} Pins
V _{TT}	Output termination voltage		V _{CC} +2		V	

a. Input pull-up / pull-down resistors influence input current.

b. The MPC941 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

Table 4: AC CHARACTERISTICS (V_{CC} = 3.3V ± 5%, T_A = -40 to +85°C)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f _{MAX}	Maximum Output Frequency	0		250 ^b	MHz	
t _r , t _f	LVC MOS_CLK Input Rise/Fall Time			1.0 ^c	ns	0.8 to 2.0V
t _{PLH} t _{PHL}	Propagation delay PECL_CLK to any Q LVC MOS_CLK to any Q	1.2 0.9	1.8 1.5	2.6 2.3	ns ns	
t _{PLZ} , HZ	Output Disable Time				ns	
t _{PZL} , LZ	Output Enable Time				ns	
t _{sk(O)}	Output-to-output Skew PECL_CLK to any Q LVC MOS_CLK to any Q		125 125	250 250	ps	
t _{sk(PP)}	Device-to-device Skew PECL_CLK to any Q LVC MOS_CLK to any Q			1000 1000	ps ps	For a given T _A and V _{CC} , any Q
t _{sk(PP)}	Device-to-device Skew PECL_CLK to any Q LVC MOS_CLK to any Q			1400 1400	ps ps	For any T _A , V _{CC} and Q
DC _Q	Output Duty Cycle PECL_CLK to any Q LVC MOS_CLK to any Q	45 45	50 50	60 55	% %	DC _{REF} = 50% DC _{REF} = 50%
t _r , t _f	Output Rise/Fall Time	0.2		1.0	ns	0.55 to 2.4V

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.

b. AC characteristics are guaranteed up to f_{max}. Please refer to applications section for information on power consumption versus operating frequency and thermal management.

c. Fast input signal transition times are required to maintain part-to-part skew specification. If part-to-part skew is not critical to the application, signal transition times smaller than 3 ns can be applied to the MPC941.

Table 5: DC CHARACTERISTICS ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40$ to $+85^\circ\text{C}$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage LVC MOS_CLK	1.7		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input low voltage LVC MOS_CLK	-0.3		0.7	V	LVC MOS
I_{IN}	Input current			$\pm 120^a$	μA	
V_{PP}	Peak-to-peak input voltage PECL_CLK, PECL_CLK	500			mV	LVPECL
V_{CMR}	Common Mode Range PECL_CLK, PECL_CLK	1.1		$V_{CC}-0.7$	V	LVPECL
V_{OH}	Output High Voltage	1.8			V	$I_{OH} = -15 \text{ mA}^b$
V_{OL}	Output Low Voltage			0.6	V	$I_{OL} = 15 \text{ mA}^b$
I_{OZ}	Output tristate leakage current			100	μA	
Z_{OUT}	Output impedance		18 – 20		Ω	
C_{PD}	Power Dissipation Capacitance		7–8	10	pF	Per Output
C_{IN}	Input capacitance		4.0		pF	
I_{CCQ}	Maximum Quiescent Supply Current			5	mA	All V_{CC} Pins
V_{TT}	Output termination voltage		$V_{CC}+2$		V	

a. Input pull-up / pull-down resistors influence input current.

b. The MPC941 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines.

Table 6: AC CHARACTERISTICS ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40$ to $+85^\circ\text{C}$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{MAX}	Maximum Output Frequency	0		250 ^b	MHz	
t_r, t_f	LVC MOS_CLK Input Rise/Fall Time			1.0 ^c	ns	0.7 to 1.7V
t_{PLH}	Propagation delay PECL_CLK to any Q	1.3	2.1	2.9	ns	
t_{PHL}	LVC MOS_CLK to any Q	1.0	1.8	2.6	ns	
$t_{PLZ, HZ}$	Output Disable Time				ns	
$t_{PZL, LZ}$	Output Enable Time				ns	
$t_{sk(O)}$	Output-to-output Skew PECL_CLK to any Q LVC MOS_CLK to any Q		125 125	250 250	ps	
$t_{sk(PP)}$	Device-to-device Skew PECL_CLK to any Q LVC MOS_CLK to any Q			1200 1200	ps ps	For a given T_A and V_{CC} , any Q
$t_{sk(PP)}$	Device-to-device Skew PECL_CLK to any Q LVC MOS_CLK to any Q			1600 1600	ps ps	For any T_A , V_{CC} and Q
DC_Q	Output Duty Cycle PECL_CLK to any Q LVC MOS_CLK to any Q	45 45	50 50	60 55	% %	$DC_{REF} = 50\%$ $DC_{REF} = 50\%$
t_r, t_f	Output Rise/Fall Time	0.2		1.0	ns	0.6 to 1.6V

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b. AC characteristics are guaranteed up to f_{max} . Please refer to the applications section for information on power consumption versus operating frequency and thermal management.

c. Fast input signal transition times are required to maintain part-to-part skew specification. If part-to-part skew is not critical to the application, signal transition times smaller than 3 ns can be applied to the MPC941.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC941 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $VCC/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC941 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 1 "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC941 clock driver is effectively doubled due to its capability to drive multiple lines.

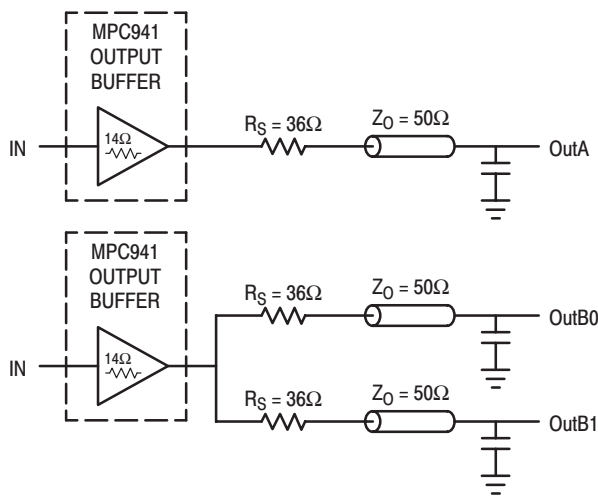


Figure 1. Single versus Dual Transmission Lines

The waveform plots of Figure 2 "Single versus Dual Waveforms" show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC941 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC941. The output waveform in Figure 2 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the

output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 / (R_S + R_o + Z_0))$$

$$Z_0 = 50\Omega \parallel 50\Omega$$

$$R_S = 36\Omega \parallel 36\Omega$$

$$R_o = 14\Omega$$

$$V_L = 3.0 (25 / (18 + 14 + 25)) = 3.0 (25 / 57) = 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

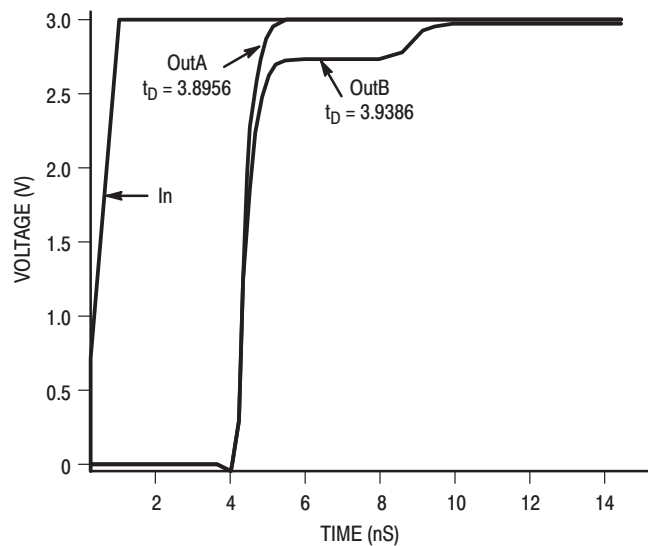


Figure 2. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 3 "Optimized Dual Line Termination" should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

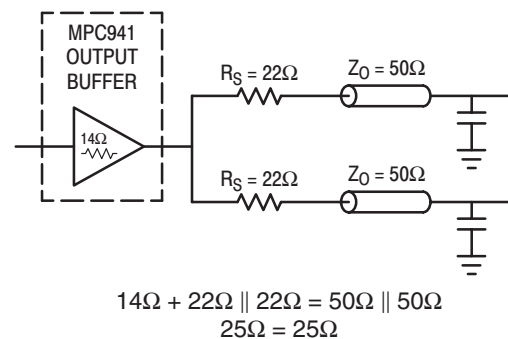


Figure 3. Optimized Dual Line Termination

Power Consumption of the MPC941 and Thermal Management

The MPC941 AC specification is guaranteed for the entire operating frequency range up to 250 MHz. The MPC941 power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperature, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the MPC941 die junction temperature and the associated device reliability. For a complete analysis of power consumption as a function of operating conditions and associated long term device reliability please refer to the application note AN1545. According the AN1545, the long-term device reliability is a function of the die junction temperature:

Table 7: Die junction temperature and MTBF

Junction temperature (°C)	MTBF (Years)
100	20.4
110	9.1
120	4.2
130	2.0

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the MPC941 needs to be controlled and the thermal impedance of the board/package should be optimized. The power dissipated in the MPC941 is represented in equation 1.

Where I_{CCQ} is the static current consumption of the MPC941, C_{PD} is the power dissipation capacitance per output, $(M)\Sigma C_L$ represents the external capacitive output load, N is the number of active outputs (N is always 27 in case of the MPC941). The MPC941 supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore, ΣC_L is zero for controlled transmission line systems and can be eliminated from equation 1. Using parallel termination output termination results in equation 2 for power dissipation.

$$P_{TOT} = \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_M C_L \right) \right] \cdot V_{CC} \quad \text{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_M C_L \right) \right] + \sum_P [DC_Q \cdot I_{OH} \cdot (V_{CC} - V_{OH}) + (1 - DC_Q) \cdot I_{OL} \cdot V_{OL}] \quad \text{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \quad \text{Equation 3}$$

$$f_{CLOCK,MAX} = \frac{1}{C_{PD} \cdot N \cdot V_{CC}^2} \cdot \left[\frac{T_{J,MAX} - T_A}{R_{thja}} - (I_{CCQ} \cdot V_{CC}) \right] \quad \text{Equation 4}$$

In equation 2, P stands for the number of outputs with a parallel or thevenin termination, V_{OL} , I_{OL} , V_{OH} and I_{OH} are a function of the output termination technique and DC_Q is the clock signal duty cycle. If transmission lines are used ΣC_L is zero in equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature T_J as a function of the power consumption.

Where R_{thja} is the thermal impedance of the package (junction to ambient) and T_A is the ambient temperature. According to Table 7, the junction temperature can be used to estimate the long-term device reliability. Further, combining equation 1 and equation 2 results in a maximum operating frequency for the MPC941 in a series terminated transmission line system.

$T_{J,MAX}$ should be selected according to the MTBF system requirements and Table 7. R_{thja} can be derived from Table 8. The R_{thja} represent data based on 1S2P boards, using 2S2P boards will result in a lower thermal impedance than indicated below.

Table 8: Thermal package impedance of the 48ld LQFP

Convection, LFPM	R_{thja} (1P2S board), K/W
Still air	78
100 lfpm	68
200 lfpm	59
300 lfpm	56
400 lfpm	54
500 lfpm	53

If the calculated maximum frequency is below 250 MHz, it becomes the upper clock speed limit for the given application conditions. The following eight derating charts describe the safe frequency operation range for the MPC941. The charts were calculated for a maximum tolerable die junction temperature of 110°C (120°C), corresponding to a estimated MTBF of 9.1 years (4 years), a supply voltage of either 3.3V or 2.5V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made.

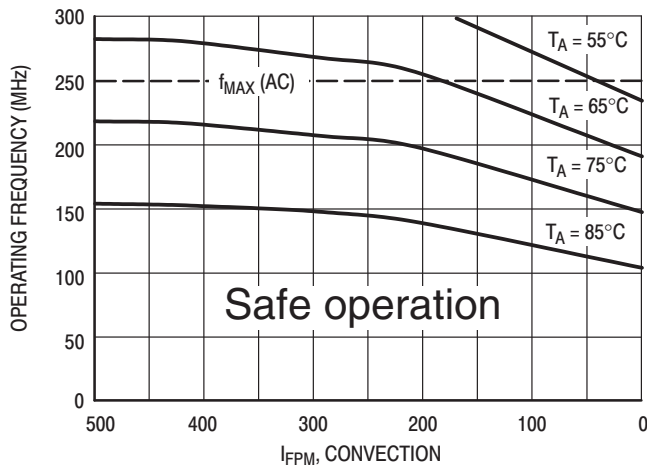


Figure 4. Maximum MPC941 frequency, $V_{CC} = 3.3V$, MTBF 9.1 years, driving series terminated transmission lines

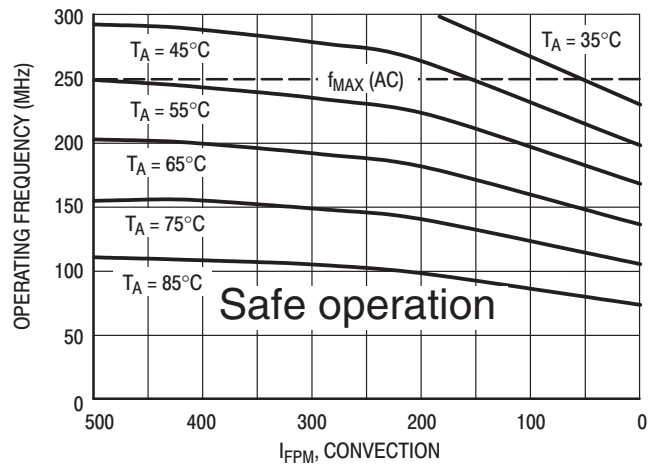


Figure 5. Maximum MPC941 frequency, $V_{CC} = 3.3V$, MTBF 9.1 years, 4 pF load per line

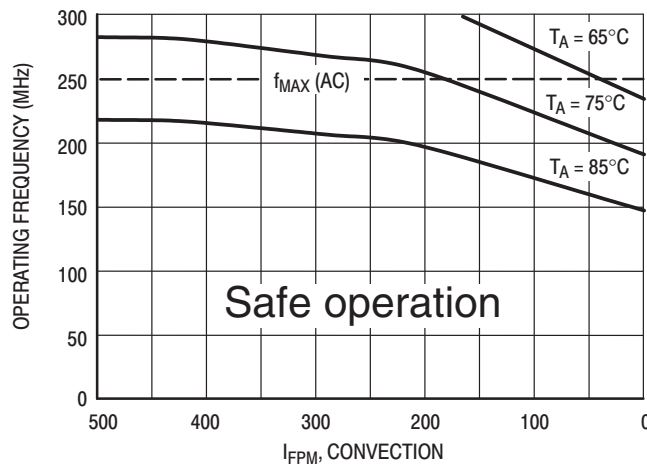


Figure 6. Maximum MPC941 frequency, $V_{CC} = 3.3V$, MTBF 4 years, driving series terminated transmission lines

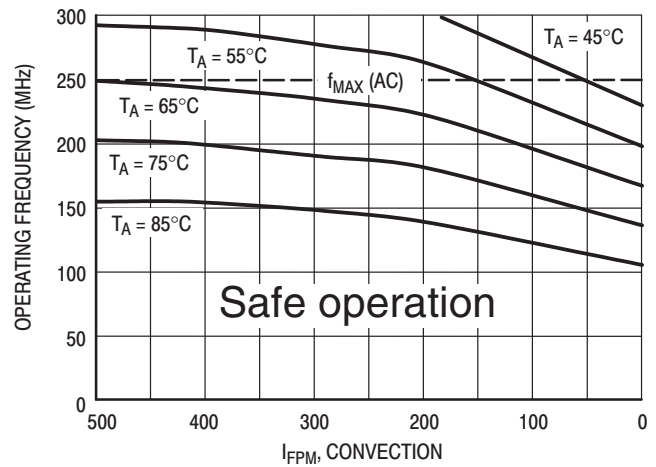


Figure 7. Maximum MPC941 frequency, $V_{CC} = 3.3V$, MTBF 4 years, 4 pF load per line

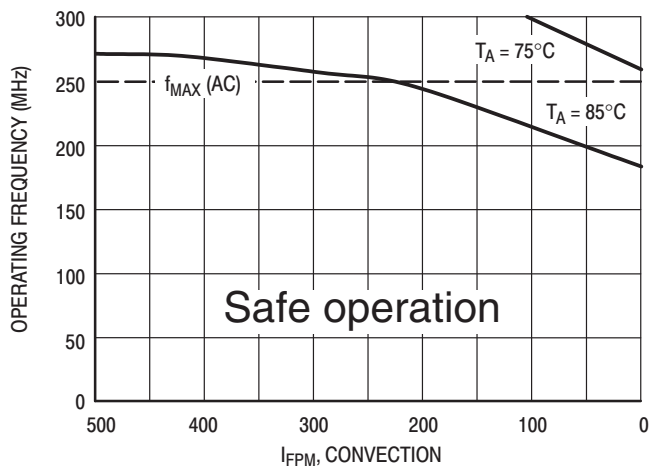


Figure 8. Maximum MPC941 frequency, $V_{CC} = 2.5V$, MTBF 9.1 years, driving series terminated transmission lines

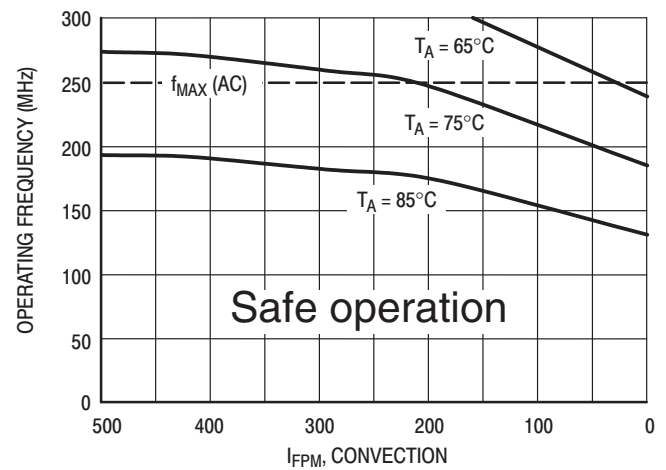


Figure 9. Maximum MPC941 frequency, $V_{CC} = 2.5V$, MTBF 9.1 years, 4 pF load per line

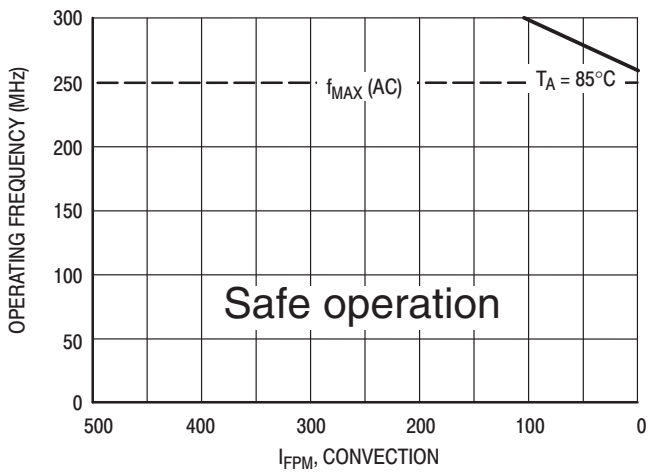


Figure 10. Maximum MPC941 frequency, $V_{CC} = 2.5V$, MTBF 4 years, driving series terminated transmission lines

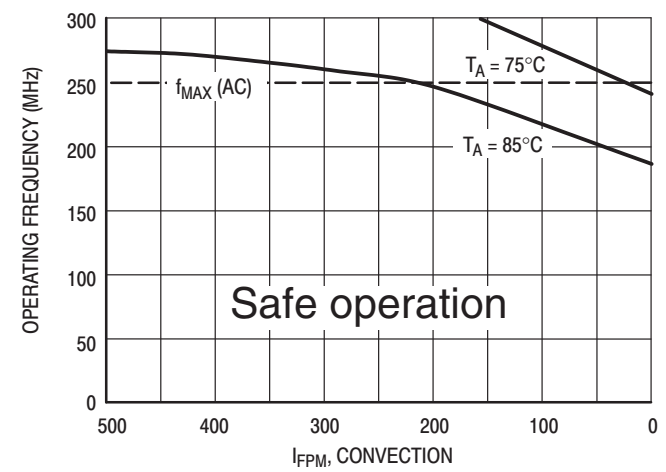


Figure 11. Maximum MPC941 frequency, $V_{CC} = 2.5V$, MTBF 4 years, 4 pF load per line

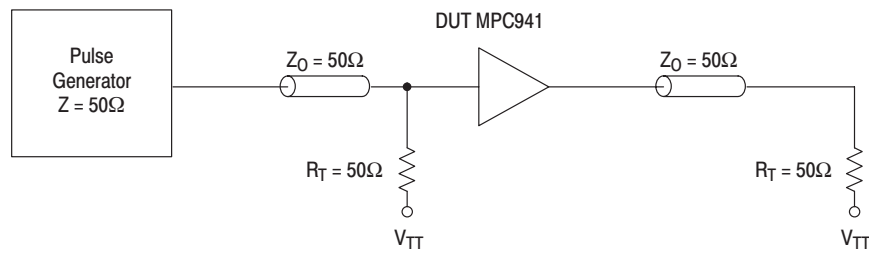


Figure 12. LVC MOS_CLK MPC941 AC test reference for $V_{CC} = 3.3V$ and $V_{CC} = 2.5V$

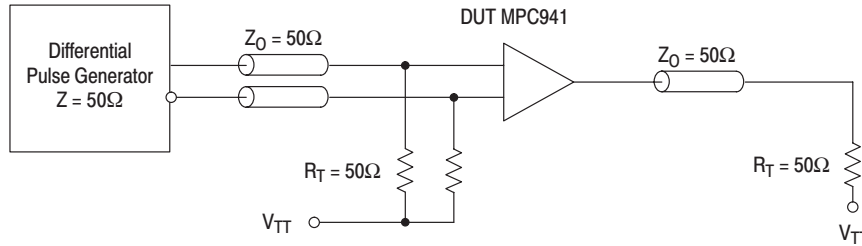


Figure 13. PECL_CLK MPC941 AC test reference for $V_{CC} = 3.3V$ and $V_{CC} = 2.5V$

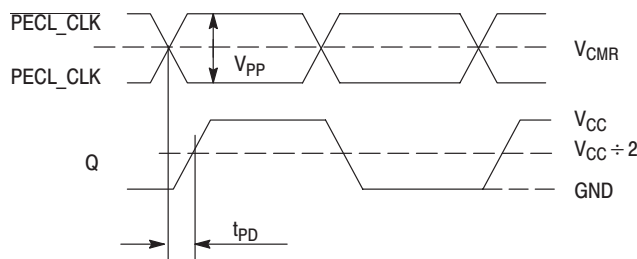


Figure 14. LVPECL Propagation delay (t_{pD}) test reference

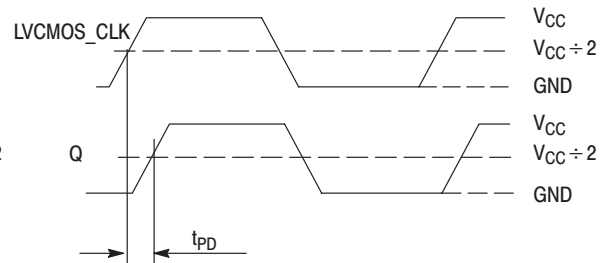
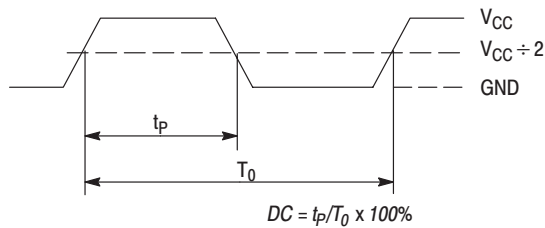


Figure 15. LVC MOS Propagation delay (t_{pD}) test reference



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 16. Output Duty Cycle (DC)

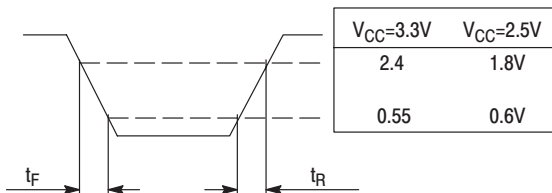


Figure 18. Output Transition Time Test Reference

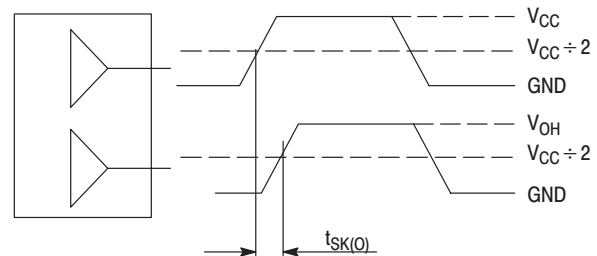


Figure 17. Output-to-output Skew $t_{SK(O)}$

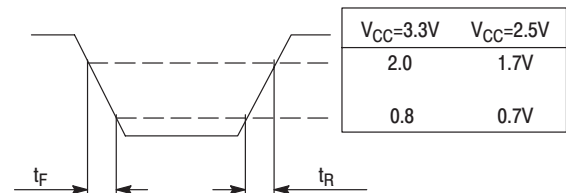


Figure 19. Input Transition Time Test Reference

Low Voltage 1:18 Clock Distribution Chip

The MPC942 is a 1:18 low voltage clock distribution chip with 2.5V or 3.3V LVCMOS output capabilities. The device is offered in two versions; the MPC942C has an LVCMOS input clock while the MPC942P has a LVPECL input clock. The 18 outputs are 2.5V or 3.3V LVCMOS compatible and feature the drive strength to drive 50 Ω series or parallel terminated transmission lines. With output-to-output skews of 200ps, the MPC942 is ideal as a clock distribution chip for the most demanding of synchronous systems. The 2.5V outputs also make the device ideal for supplying clocks for a high performance Pentium II™ microprocessor based design.

- LVCMOS/LVTTL Clock Input
- 2.5V LVCMOS Outputs for Pentium II Microprocessor Support
- 150ps Maximum Targeted Output-to-Output Skew
- Maximum Output Frequency of 250MHz @ 3.3 V_{CC}
- 32-Lead TQFP Packaging
- Single 3.3V or 2.5V Supply

With a low output impedance ($\approx 12\Omega$), in both the HIGH and LOW logic states, the output buffers of the MPC942 are ideal for driving series terminated transmission lines. With an output impedance of 12 Ω the MPC942 can drive two series terminated transmission lines from each output. This capability gives the MPC942 an effective fanout of 1:36. The MPC942 provides enough copies of low skew clocks for most high performance synchronous systems.

The LVCMOS/LVTTL input of the MPC942C provides a more standard LVCMOS interface. The OE pins will place the outputs into a high impedance state. The OE pin has an internal pullup resistor.

The MPC942 is a single supply device. The V_{CC} power pins require either 2.5V or 3.3V. The 32-lead TQFP package was chosen to optimize performance, board space and cost of the device. The 32-lead TQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

MPC942C

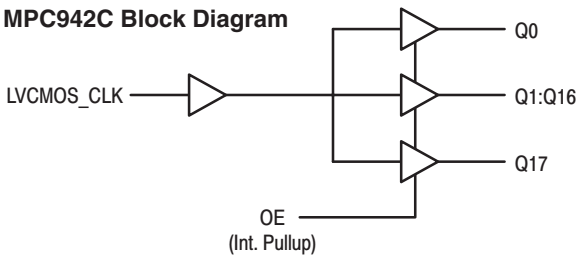
**LOW VOLTAGE
1:18 CLOCK
DISTRIBUTION CHIP**



**FA SUFFIX
32-LEAD TQFP PACKAGE
CASE 873A**

LOGIC DIAGRAM

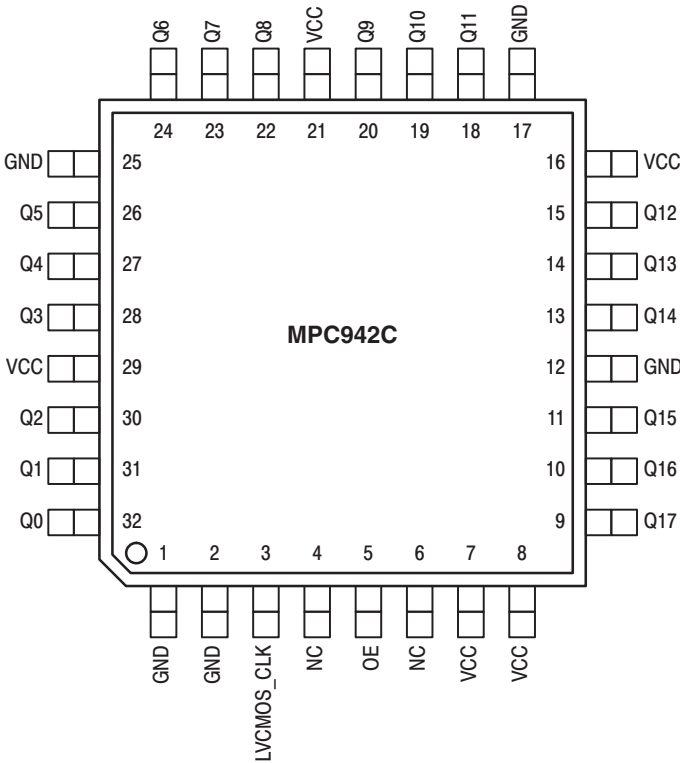
MPC942C Block Diagram



FUNCTION TABLE

OE	Output
0	HIGH IMPEDANCE
1	OUTPUTS ENABLED

Pinout: 32-Lead (Top View)



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	-0.3	3.6	V
V _I	Input Voltage	-0.3	V _{CC} + 0.3	V
I _{IN}	Input Current		±20	mA
T _{Stor}	Storage Temperature Range	-40	125	°C

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CCI} = 2.5\text{V} \pm 5\%$, $V_{CCO} = 2.5\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		V_{CCI}	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.0			V	$I_{OH} = -16\text{ mA}$
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 16\text{ mA}$
I_{IN}	Input Current			± 200	μA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		14		pF	Per Output
Z_{OUT}	Output Impedance		12		Ω	
I_{CC}	Maximum Quiescent Supply Current		0.5		mA	

AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CCI} = 2.5\text{V} \pm 5\%$, $V_{CCO} = 2.5\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Frequency			200	MHz	
t_{PLH}	Propagation Delay	1.5		2.8	ns	
$t_{sk(o)}$	Output-to-Output Skew			200	ps	
$t_{sk(pr)}$	Part-to-Part Skew			1.3	ns	Notes 1, 2
$t_{sk(pr)}$	Part-to-Part Skew			600	ps	Notes 1, 3
d_t	Duty Cycle	45		55	%	
t_r, t_f	Output Rise/Fall Time	0.2		1.0	ns	

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CCI} = 3.3\text{V} \pm 5\%$, $V_{CCO} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.4		V_{CCI}	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -20\text{ mA}$
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 20\text{ mA}$
I_{IN}	Input Current			± 200	μA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		14		pF	Per Output
Z_{OUT}	Output Impedance		12		Ω	
I_{CC}	Maximum Quiescent Supply Current		0.5		mA	

AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CCI} = 3.3\text{V} \pm 5\%$, $V_{CCO} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Frequency			250	MHz	
t_{PLH}	Propagation Delay	1.3		2.3	ns	Note 1
$t_{sk(o)}$	Output-to-Output Skew			200	ps	
$t_{sk(pr)}$	Part-to-Part Skew			1.0	ns	Notes 1, 2
$t_{sk(pr)}$	Part-to-Part Skew			500	ps	Notes 1, 3
d_t	Duty Cycle	45		55	%	
t_r, t_f	Output Rise/Fall Time	0.2		1.0	ns	

1. Tested using standard input levels, production tested @ 133 MHz.
2. Across temperature and voltage ranges, includes output skew.
3. For a specific temperature and voltage, includes output skew.

Low Voltage 1:18 Clock Distribution Chip

The MPC942 is a 1:18 low voltage clock distribution chip with 2.5V or 3.3V LVCMOS output capabilities. The device is offered in two versions; the MPC942C has an LVCMOS input clock while the MPC942P has a LVPECL input clock. The 18 outputs are 2.5V or 3.3V LVCMOS compatible and feature the drive strength to drive 50 Ω series or parallel terminated transmission lines. With output-to-output skews of 200ps, the MPC942 is ideal as a clock distribution chip for the most demanding of synchronous systems. The 2.5V outputs also make the device ideal for supplying clocks for a high performance Pentium II™ microprocessor based design.

- LVPECL Clock Input
- 2.5V LVCMOS Outputs for Pentium II Microprocessor Support
- 200ps Maximum Targeted Output-to-Output Skew
- Maximum Output Frequency of 250MHz @ 3.3 V_{CC}
- 32-Lead LQFP Packaging
- Single 3.3V or 2.5V Supply

With a low output impedance ($\approx 12\Omega$), in both the HIGH and LOW logic states, the output buffers of the MPC942 are ideal for driving series terminated transmission lines. With an output impedance of 12 Ω the MPC942 can drive two series terminated transmission lines from each output. This capability gives the MPC942 an effective fanout of 1:36. The MPC942 provides enough copies of low skew clocks for most high performance synchronous systems.

The differential LVPECL inputs of the MPC942P allow the device to interface directly with a LVPECL fanout buffer like the MC100EP111 to build very wide clock fanout trees or to couple to a high frequency clock source. The OE pins will place the outputs into a high impedance state. The OE pin has an internal pullup resistor.

The MPC942 is a single supply device. The V_{CC} power pins require either 2.5V or 3.3V. The 32-lead LQFP package was chosen to optimize performance, board space and cost of the device. The 32-lead LQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

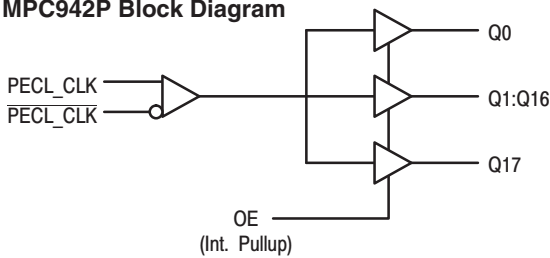
MPC942P**LOW VOLTAGE
1:18 CLOCK
DISTRIBUTION CHIP****FA SUFFIX**
32-LEAD LQFP PACKAGE
CASE 873A**6**

Pentium II is a trademark of Intel Corporation.

Rev 1

LOGIC DIAGRAM

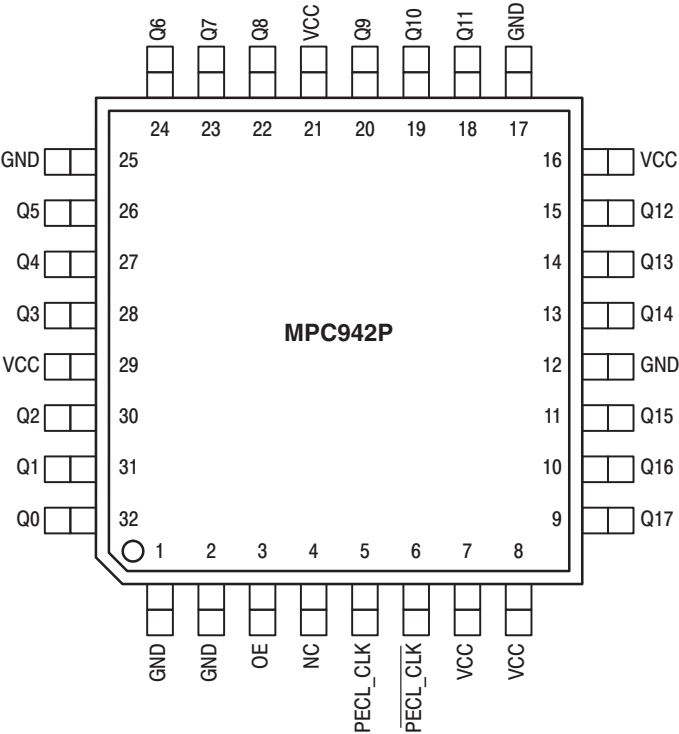
MPC942P Block Diagram



FUNCTION TABLE

OE	Output
0	HIGH IMPEDANCE
1	OUTPUTS ENABLED

Pinout: 32-Lead (Top View)



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	3.6	V
V_I	Input Voltage	-0.3	$V_{CC} + 0.3$	V
I_{IN}	Input Current		± 20	mA
T_{Stor}	Storage Temperature Range	-40	125	$^{\circ}C$

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 2.5\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{PP}	Input Swing PECL_CLK	0.6		1.0	V	
V_X	Input Crosspoint PECL_CLK	$V_{CC}-1.0$		$V_{CC}-0.6$	V	
V_{OH}	Output HIGH Voltage	2.0			V	$I_{OH} = -16\text{ mA}$
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 16\text{ mA}$
I_{IN}	Input Current			± 200	μA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		14		pF	Per Output
Z_{OUT}	Output Impedance		12		Ω	
I_{CC}	Maximum Quiescent Supply Current		0.5	5.0	mA	

AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 2.5\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Frequency			200	MHz	
t_{PLH}	Propagation Delay	1.8		4.0	ns	
t_{PHL}	Propagation Delay	2.0		4.3	ns	
$t_{sk(o)}$	Output-to-Output Skew			200	ps	
$t_{sk(pr)}$	Part-to-Part Skew			2.2	ns	Note 2
$t_{sk(pr)}$	Part-to-Part Skew			1.3	ps	Note 1
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	

1. For a specific temperature and voltage, includes output skew.
2. Across temperature and voltage ranges, includes output skew.

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.4		V_{CC}	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{PP}	Input Swing PECL_CLK	0.6		1.0	V	
V_X	Input Crosspoint PECL_CLK	$V_{CC}-1.0$		$V_{CC}-0.6$	V	
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -20\text{ mA}$
V_{OL}	Output LOW Voltage			0.6	V	$I_{OL} = 20\text{ mA}$
I_{IN}	Input Current			± 200	μA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		14		pF	Per Output
Z_{OUT}	Output Impedance		12		Ω	
I_{CC}	Maximum Quiescent Supply Current		0.5	5.0	mA	

AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Frequency			250	MHz	
t_{PLH}	Propagation Delay	1.5		3.2	ns	
t_{PHL}	Propagation Delay	1.5		3.6	ns	
$t_{sk(o)}$	Output-to-Output Skew			200	ps	
$t_{sk(pr)}$	Part-to-Part Skew			1.7	ns	Note 2
$t_{sk(pr)}$	Part-to-Part Skew			1.0	ps	Note 1
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	

1. For a specific temperature and voltage, includes output skew.
2. Across temperature and voltage ranges, includes output skew.

2.5V and 3.3V LVC MOS Clock Fanout Buffer

The MPC9443 is a 2.5V and 3.3V compatible 1:16 clock distribution buffer designed for low-voltage high-performance telecom, networking and computing applications. The device supports 3.3V, 2.5V and dual supply voltage (mixed-voltage) applications. The MPC9443 offers 16 low-skew outputs which are divided into 4 individually configurable banks. Each output bank can be individually supplied by 2.5V or 3.3V, individually set to run at 1X or 1/2X of the input clock frequency or be disabled (logic low output state). Two selectable LVPECL compatible inputs support differential clock distribution systems. In addition, one selectable LVC MOS input is provided for LVC MOS clock distribution systems. The MPC9443 is specified for the extended temperature range of -40 to $+85^{\circ}\text{C}$.

Features

- Configurable 16 outputs LVC MOS clock distribution buffer
- Compatible to single, dual and mixed 3.3V/2.5V voltage supply
- Output clock frequency up to 350 MHz
- Designed for high-performance telecom, networking and computer applications
- Supports applications requiring clock redundancy
- Max. output skew of 250 ps (125 ps within one bank)
- Selectable output configurations per output bank
- Individually per-bank high-impedance tristate
- Output disable (stop in logic low state) control
- 48 ld LQFP package
- Ambient operating temperature range of -40 to 85°C

Functional Description

The MPC9443 is a full static design supporting clock frequencies up to 350 MHz. The signals are generated and retimed on-chip to ensure minimal skew between the four output banks.

Two independent LVPECL compatible clock inputs are available. This feature supports redundant differential clock sources. In addition, the MPC9443 supports single-ended LVC MOS clock distribution systems. Each of the four output banks can be individually supplied by 2.5V or 3.3V, supporting mixed voltage applications. The FSELx pins choose between division of the input reference frequency by one or two. The frequency divider can be set individually for each output bank. The MPC9443 output banks are in high-impedance state by deasserting the $\overline{\text{OE}}_{\text{N}}$ pins. Asserting $\overline{\text{OE}}_{\text{N}}$ will enable output banks. Please see the Output High-Impedance Control table on page 558 for details. The outputs can be synchronously stopped (logic low state). The outputs provide LVC MOS compatible levels with the capability to drive terminated $50\ \Omega$ transmission lines. For series terminated transmission lines, each of the MPC9443 outputs can drive one or two traces giving the devices an effective fanout of 1:32 at $V_{\text{CC}} = 3.3\text{V}$. The device is packaged in a $7 \times 7\ \text{mm}^2$ 48-lead LQFP package.

MPC9443

**LOW VOLTAGE SUPPLY 2.5V
AND 3.3V LVC MOS CLOCK
FANOUT BUFFER**



FA SUFFIX
48-LEAD LQFP PACKAGE
CASE 932

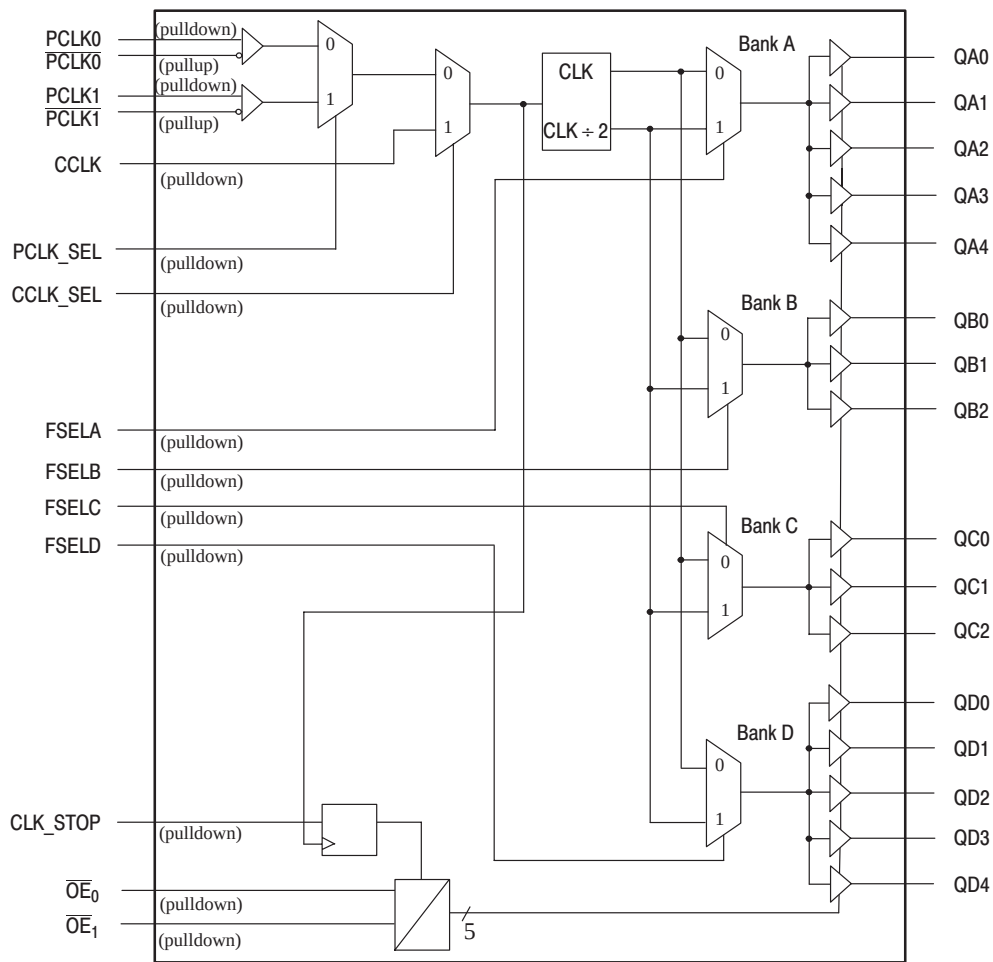


Figure 1. MPC9443 Logic Diagram

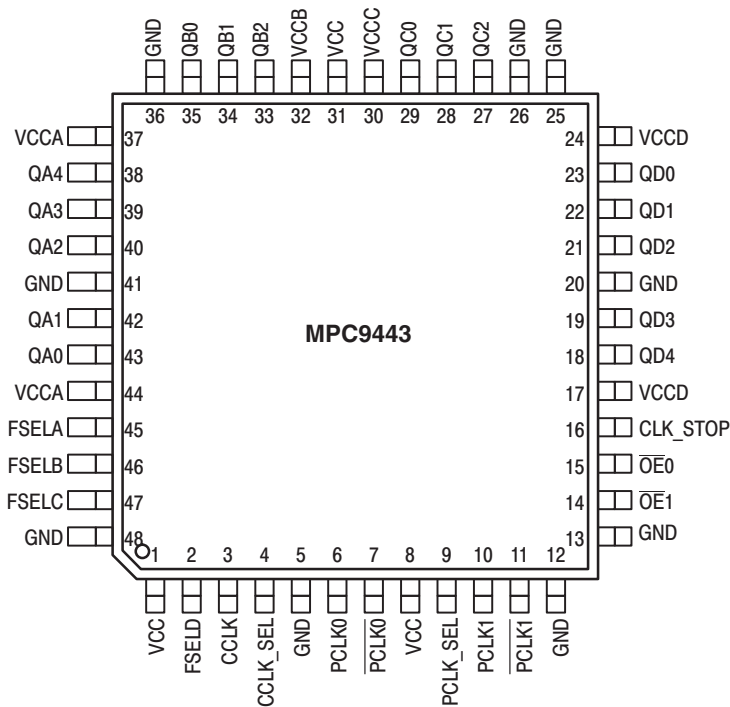


Figure 2. 48-Lead Package Pinout (Top View)

Table 1: Pin Configuration

Pin	I/O	Type	Function
CCLK	Input	LVC MOS	LVC MOS clock inputs
PCLK0, PCLK0	Input	LVC MOS	LVPECL differential clock input
PCLK1, PCLK1	Input	LVC MOS	LVPECL differential clock input
FSEL _A , FSEL _B , FSEL _C , FSEL _D	Input	LVC MOS	Output bank divide select input
CCLK_SEL	Input	LVC MOS	LVC MOS/LVPECL clock input select
PCLK_SEL	Input	LVC MOS	PCLK0/PCLK1 clock input select
$\overline{OE}_0$, $\overline{OE}_1$	Input	LVC MOS	Output tristate control
CLK_STOP	Input	LVC MOS	Synchronous output enable/disable (clock stop) control
GND		Supply	Negative voltage supply
V _{CCA} , V _{CCB} , V _{CCC} , V _{CCD}		Supply	Positive voltage supply output bank (VCC)
V _{CC}		Supply	Positive voltage supply core (VCC)
QA0 to QA4	Output	LVC MOS	Bank A outputs
QB0 to QB2	Output	LVC MOS	Bank B outputs
QC0 to QC2	Output	LVC MOS	Bank C outputs
QD0 to QD4	Output	LVC MOS	Bank D outputs

Table 2: Supported Single and Dual Supply Configurations

Supply voltage configuration	V _{CC} ^a	V _{CCA} ^b	V _{CCB} ^c	V _{CCC} ^d	V _{CCD} ^e	GND
3.3V supply	3.3V	3.3V	3.3V	3.3V	3.3V	0 V
Mixed mode supply	3.3V	3.3V or 2.5V	3.3V or 2.5V	3.3V or 2.5V	3.3V or 2.5V	0 V
2.5V supply	2.5V	2.5V	2.5V	2.5V	2.5V	0 V

a. V_{CC} is the positive power supply of the device core and input circuitry. V_{CC} voltage defines the input threshold and levels

b. V_{CCA} is the positive power supply of the bank A outputs. V_{CCA} voltage defines bank A output levels

c. V_{CCB} is the positive power supply of the bank B outputs. V_{CCB} voltage defines bank B output levels

d. V_{CCC} is the positive power supply of the bank C outputs. V_{CCC} voltage defines bank C output levels

e. V_{CCD} is the positive power supply of the bank D outputs. V_{CCD} voltage defines bank D output levels

6

Table 3: Function Table (Controls)

Control	Default	0	1
CCLK_SEL	0	PCLK or PCLK1 active (LVPECL clock mode)	CCLK active (LVC MOS clock mode)
PCLK_SEL	0	PCLK0 active, PCLK1 inactive	PCLK1 active, PCLK0 inactive
FSEL _A	0	f _{QA0:4} = f _{REF}	f _{QA0:4} = f _{REF} ÷ 2
FSEL _B	0	f _{QB0:2} = f _{REF}	f _{QB0:2} = f _{REF} ÷ 2
FSEL _C	0	f _{QC0:2} = f _{REF}	f _{QC0:2} = f _{REF} ÷ 2
FSEL _D	0	f _{QD0:4} = f _{REF}	f _{QD0:4} = f _{REF} ÷ 2
CLK_STOP	0	Normal operation	Outputs are synchronously disabled (stopped) in logic low state
$\overline{OE}_0$, $\overline{OE}_1$	00	Asynchronous output enable control. See Table 4. $\overline{OE}_N$	

Table 4: Output High-Impedance Control ($\overline{OE}_N$)^a

$\overline{OE}_0$	$\overline{OE}_1$	QA0 to QA4	QB0 to QB2	QC0 to QC2	QD0 to QD4	Total number of enabled outputs
0	0	Enabled	Enabled	Enabled	Enabled	16
0	1	Enabled	Disabled (tristate)	Disabled (tristate)	Enabled	10
1	0	Enabled	Enabled	Disabled (tristate)	Disabled (tristate)	8
1	1	Disabled (tristate)	Disabled (tristate)	Disabled (tristate)	Disabled (tristate)	0

a. $\overline{OE}_N$ will tristate (high impedance) output banks independent on the logic state of the output and the status of CLK_STOP.

Table 5: Absolute Maximum Ratings^a

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.6	V	
V_{IN}	DC Input Voltage	-0.3	$V_{CC}+0.3$	V	
V_{OUT}	DC Output Voltage	-0.3	$V_{CC}+0.3$	V	
I_{IN}	DC Input Current		± 20	mA	
I_{OUT}	DC Output Current		± 50	mA	
T_S	Storage temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 6: General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		$V_{CC} \div 2$		V	
MM	ESD protection (Machine model)	200			V	
HBM	ESD protection (Human body model)	2000			V	
LU	Latch-up immunity	200			mA	
C_{PD}	Power dissipation capacitance		10		pF	Per output
C_{IN}	Input capacitance		4.0		pF	

Table 7: DC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = V_{CCD} = 3.3V \pm 5\%$, $T_A = -40$ to $+85^\circ\text{C}$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input Low Voltage	-0.3		0.8	V	LVC MOS
V_{PP}	Peak-to-peak Input Voltage PCLK0, 1	250			mV	LVPECL
V_{CMR}^a	Common Mode Range PCLK0, 1	1.1		$V_{CC}-0.6$	V	LVPECL
I_{IN}	Input Current ^b			200	μA	$V_{IN}=\text{GND}$ or $V_{IN}=V_{CC}$
V_{OH}	Output High Voltage	2.4			V	$I_{OH}=-24\text{ mA}^c$
V_{OL}	Output Low Voltage			0.55 0.30	V V	$I_{OL}=24\text{ mA}^c$ $I_{OL}=12\text{ mA}$
Z_{OUT}	Output Impedance		19		Ω	
I_{CCQ}^d	Maximum Quiescent Supply Current			2.0	mA	All V_{CC} Pins

- a. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
- b. Input pull-up / pull-down resistors influence input current.
- c. The MPC9443 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines (for $V_{CC}=3.3V$) or one 50Ω series terminated transmission line (for $V_{CC}=2.5V$).
- d. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 8: AC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = V_{CCD} = 3.3V \pm 5\%$, $T_A = -40$ to $+85^\circ\text{C}$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	0		350	MHz	
f_{MAX}	Maximum Output Frequency	+1 output +2 output	0 0	350 175	MHz MHz	FSELx=0 FSELx=1
V_{PP}	Peak-to-peak Input Voltage PCLK0,1	500		1000	mV	LVPECL
V_{CMR}^b	Common Mode Range PCLK0,1	1.3		$V_{CC}-0.8$	V	LVPECL
t_{P_REF}	Reference Input Pulse Width	1.4			ns	
t_r, t_f	CCLK Input Rise/Fall Time			1.0 ^c	ns	0.8 to 2.0V
t_{PLH}	Propagation Delay PCLK0,1 to any Q	2.5		5.0	ns	
t_{PHL}	Propagation Delay PCLK0,1 to any Q	2.4		5.2	ns	
t_{PLH}	Propagation Delay CCLK to any Q	2.1		4.2	ns	
t_{PHL}	Propagation Delay CCLK to any Q	1.9		4.6	ns	
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
t_S, t_H	Setup, hold time (reference clock to CLK_STOP)	500			ps	
$t_{sk(LH, HL)}$	Output-to-output Skew ^d			125 225 250	ps ps ps	Within one bank Any output, same output divider Any output, any output divider
$t_{sk(PP)}$	Device-to-device Skew (LH) ^e			2.5 2.1	ns ns	Using PCLK0,1 Using CCLK
	Device-to-device Skew (LH, HL) ^f			2.8 2.7	ns ns	Using PCLK0,1 Using CCLK
$t_{SK(P)}$	Output pulse skew ^g			300 400	ps ps	$DC_{REF} = 50\%$
DC_Q	Output Duty Cycle				%	
	$f_Q < 140\text{ MHz}$ and using CCLK	45	50	55	%	
	$f_Q < 250\text{ MHz}$ and using PCLK0,1	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V

- a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
- b. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification.
- c. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
- d. $t_{sk(LH, HL)}$ includes both device skew referenced to the rising output edge and device skew referenced to the falling output edge.
- e. Device-to-device skew referenced to the rising output edge.
- f. Device-to-device skew referenced to the rising output edge or referenced to the falling output edge.
- g. Output pulse skew is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.

Table 9: DC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = V_{CCD} = 2.5V \pm 5\%$, $T_A = -40$ to $+85^\circ\text{C}$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	1.7		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input Low Voltage	-0.3		0.7	V	LVC MOS
V_{PP}	Peak-to-peak Input Voltage PCLK0,1	250			mV	LVPECL
V_{CMRA}	Common Mode Range PCLK0,1	1.1		$V_{CC}-0.7$	V	LVPECL
I_{IN}	Input Current ^b			200	μA	$V_{IN}=\text{GND}$ or $V_{IN}=V_{CC}$
V_{OH}	Output High Voltage	1.8			V	$I_{OH} = -15\text{ mA}^c$
V_{OL}	Output Low Voltage			0.6	V	$I_{OL} = 15\text{ mA}^c$
Z_{OUT}	Output Impedance		22		Ω	
I_{CCQ}^d	Maximum Quiescent Supply Current			2.0	mA	All V_{CC} Pins

- a. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
- b. Input pull-up / pull-down resistors influence input current.
- c. The MPC9443 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives one 50Ω series terminated transmission lines at $V_{CC}=2.5V$.
- d. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 10: AC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = V_{CCD} = 2.5 \pm 5\%$, $T_A = -40$ to $+85^\circ\text{C}$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	0		350	MHz	
f_{MAX}	Maximum Output Frequency	± 1 output ± 2 output	0 0	350 175	MHz MHz	FSELx=0 FSELx=1
V_{PP}	Peak-to-peak input voltage PCLK0,1	500		1000	mV	LVPECL
V_{CMR}^b	Common Mode Range PCLK0,1	1.1		$V_{CC}-0.7$	V	LVPECL
$t_{P, REF}$	Reference Input Pulse Width	1.4			ns	
t_r, t_f	CCLK Input Rise/Fall Time			1.0 ^c	ns	0.8 to 2.0V
t_{PLH} t_{PHL} t_{PLH} t_{PHL}	Propagation delay PCLK0,1 to any Q PCLK0,1 to any Q CCLK to any Q CCLK to any Q	2.8 2.7 2.2 2.1		6.0 6.2 5.3 5.5	ns ns ns ns	
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
t_S, t_H	Setup, hold time (reference clock to CLK_STOP)	500			ps	
$t_{sk(LH, HL)}$	Output-to-output Skew ^d Within one bank Any output, same output divider Any output, any output divider			125 225 250	ps ps ps	
$t_{sk(PP)}$	Device-to-device Skew (LH) ^e Using PCLK0,1 Using CCLK Device-to-device Skew (LH, HL) ^f Using PCLK0,1 Using CCLK			3.2 3.1 3.5 3.4	ns ns ns ns	
$t_{SK(p)}$	Output pulse skew ^g Using PCLK0,1 Using CCLK			300 400	ps ps	$DC_{REF} = 50\%$
DC_Q	Output Duty Cycle $f_Q < 140\text{ MHz}$ and using CCLK $f_Q < 250\text{ MHz}$ and using PCLK0,1	45 45	50 50	55 55	% %	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.6 to 1.8V

- a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
- b. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification.
- c. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
- d. $t_{sk(LH, HL)}$ includes both device skew referenced to the rising output edge and device skew referenced to the falling output edge.
- e. Device-to-device skew referenced to the rising output edge.
- f. Device-to-device skew referenced to the rising output edge or referenced to the falling output edge.
- g. Output pulse skew is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.

Table 11: DC Characteristics(V_{CC} = 3.3V ± 5%, any V_{CCA,B,C,D} = 2.5V ± 5% or 3.3V ± 5% (mixed), T_A = -40 to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{IH}	Input high voltage	2.0		V _{CC} + 0.3	V	LVC MOS
V _{IL}	Input low voltage	-0.3		0.8	V	LVC MOS
I _{IN}	Input current ^a			200	μA	
V _{OH}	Output High Voltage 2.5V output 3.3V output	1.7 2.0			V	I _{OH} = -15 mA ^b I _{OH} = -24 mA ^b
V _{OL}	Output Low Voltage 2.5V output 3.3V output			0.6 0.55	V	I _{OL} = 15 mA ^b I _{OL} = 24 mA ^b
V _{PP}	Peak-to-peak input voltage PCLK0,1	250			mV	LVPECL
V _{CMR} ^c	Common Mode Range PCLK0,1	1.1		V _{CC} -0.6	V	LVPECL
Z _{OUT}	Output impedance 2.5V output 3.3V output		22 19		Ω Ω	
C _{PD}	Power Dissipation Capacitance		10		pF	Per Output
I _{CCQ} ^d	Maximum Quiescent Supply Current			2.0	mA	All V _{CC} Pins

- a. Input pull-up / pull-down resistors influence input current.
- b. The MPC9443 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines (for V_{CC}=3.3V) or one 50Ω series terminated transmission line (for V_{CC}=2.5V).
- c. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
- d. ICCQ is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 12: AC Characteristics(V_{CC} = 3.3V ± 5%, any V_{CCA,B,C,D} = 2.5V ± 5% or 3.3V ± 5% (mixed), T_A = -40 to +85°C)^{a b}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
t _{sk(LH, HL)}	Output-to-output Skew ^c Any output, same output divider Any output, any output divider			275 350	ps ps	
t _{sk(PP)}	Device-to-device Skew	See 3.3V AC table				
t _{PLH, HL}	Propagation Delay	See 3.3V AC table				
t _{SK(P)}	Output pulse skew ^d Using PCLK0,1 Using CCLK			400 500	ps ps	DC _{REF} = 50%
DC _Q	Output Duty Cycle f _Q < 140 MHz and using CCLK f _Q < 250 MHz and using PCLK0,1	45 45	50 50	55 55	% %	

- a. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
- b. This table only specifies AC parameter in mixed voltage supply conditions that vary from the corresponding AC tables. All other parameters, see the 3.3V (for 3.3V outputs) or 2.5V AC table (for 2.5V outputs).
- c. t_{sk(LH, HL)} includes both device skew referenced to the rising output edge and device skew referenced to the falling output edge.
- d. Output pulse skew is the absolute difference of the propagation delay times: |t_{pLH} - t_{pHL}|.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC9443 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines at $V_{CC} = 3.3V$. For more information on transmission lines the reader is referred to application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}+2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9443 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9443 clock driver is effectively doubled due to its capability to drive multiple lines (at $V_{CC} = 3.3V$).

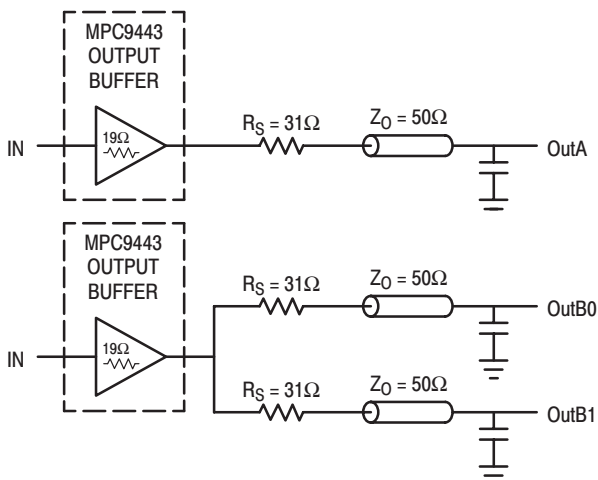


Figure 3. Single versus Dual Transmission Lines

The waveform plots in Figure 4 "Single versus Dual Line Termination Waveforms" show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9443 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9443. The output waveform in Figure 4 "Single versus Dual Line Termination Waveforms" shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 31Ω se-

ries resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned} V_L &= V_S (Z_0 \div (R_S + R_0 + Z_0)) \\ Z_0 &= 50\Omega \parallel 50\Omega \\ R_S &= 31\Omega \parallel 31\Omega \\ R_0 &= 19\Omega \\ V_L &= 3.0 (25 \div (15.5 + 19 + 25)) \\ &= 1.26V \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.52V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

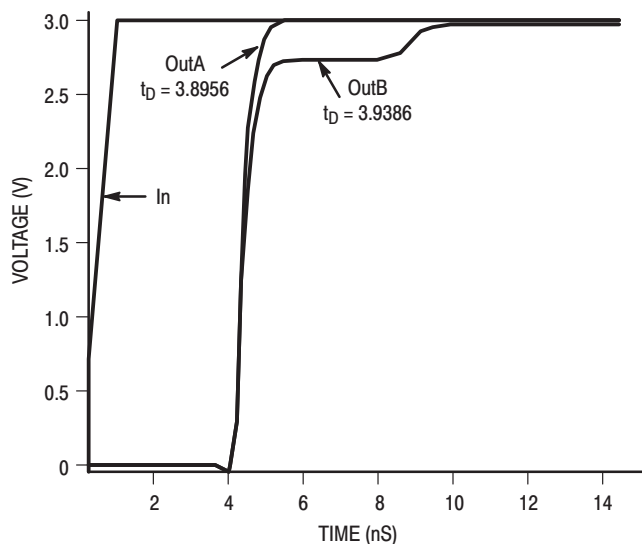


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 "Optimized Dual Line Termination" should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

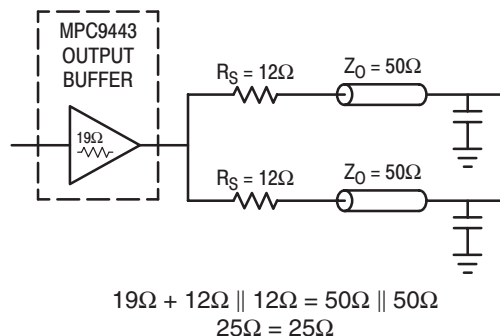


Figure 5. Optimized Dual Line Termination

Power Consumption of the MPC9443 and Thermal Management

The MPC9443 AC specification is guaranteed for the entire operating frequency range up to 350 MHz. The MPC9443 power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperature, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the MPC9443 die junction temperature and the associated device reliability. For a complete analysis of power consumption as a function of operating conditions and associated long term device reliability please refer to the application note AN1545. According to the AN1545, the long-term device reliability is a function of the die junction temperature:

Table 13: Die junction temperature and MTBF

Junction temperature (°C)	MTBF (Years)
100	20.4
110	9.1
120	4.2
130	2.0

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the MPC9443 needs to be controlled and the thermal impedance of the board/package should be optimized. The power dissipated in the MPC9443 is represented in equation 1.

Where I_{CCQ} is the static current consumption of the MPC9443, C_{PD} is the power dissipation capacitance per output, $(M)\Sigma C_L$ represents the external capacitive output load, N is the number of active outputs (N is always 16 in case of the MPC9443). The MPC9443 supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore, ΣC_L is zero for controlled transmission line systems and can be eliminated from equation 1. Using parallel termination output termination results in equation 2 for power dissipation.

$$P_{TOT} = \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_M C_L \right) \right] \cdot V_{CC} \quad \text{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_M C_L \right) \right] + \sum_P [DC_Q \cdot I_{OH} \cdot (V_{CC} - V_{OH}) + (1 - DC_Q) \cdot I_{OL} \cdot V_{OL}] \quad \text{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \quad \text{Equation 3}$$

$$f_{CLOCK,MAX} = \frac{1}{C_{PD} \cdot N \cdot V_{CC}^2} \cdot \left[\frac{T_{J,MAX} - T_A}{R_{thja}} - (I_{CCQ} \cdot V_{CC}) \right] \quad \text{Equation 4}$$

In equation 2, P stands for the number of outputs with a parallel or thevenin termination, V_{OL} , I_{OL} , V_{OH} and I_{OH} are a function of the output termination technique and DC_Q is the clock signal duty cycle. If transmission lines are used ΣC_L is zero in equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature T_J as a function of the power consumption.

Where R_{thja} is the thermal impedance of the package (junction to ambient) and T_A is the ambient temperature. According to Table 13, the junction temperature can be used to estimate the long-term device reliability. Further, combining equation 1 and equation 2 results in a maximum operating frequency for the MPC9443 in a series terminated transmission line system.

$T_{J,MAX}$ should be selected according to the MTBF system requirements and Table 13. R_{thja} can be derived from Table 14. The R_{thja} represent data based on 1S2P boards, using 2S2P boards will result in a lower thermal impedance than indicated below.

Table 14: Thermal package impedance of the 48ld LQFP

Convection, LFPM	R_{thja} (1P2S board), K/W	R_{thja} (2P2S board), K/W
Still air	69	53
100 lfpm		
200 lfpm	64	50
300 lfpm		
400 lfpm		
500 lfpm		

If the calculated maximum frequency is below 250 MHz, it becomes the upper clock speed limit for the given application conditions. The following eight derating charts describe the safe frequency operation range for the MPC9443. The charts were calculated for a maximum tolerable die junction temperature of 110°C (120°C), corresponding to an estimated MTBF of 9.1 years (4 years), a supply voltage of 3.3V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made.

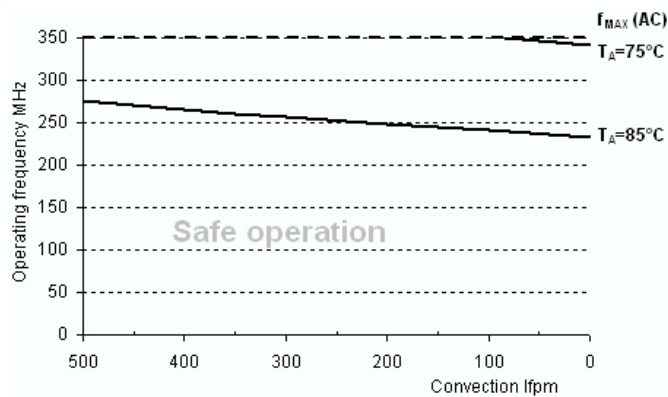


Figure 6. Maximum MPC9443 frequency, $V_{CC} = 3.3V$, MTBF 9.1 years, driving series terminated transmission lines

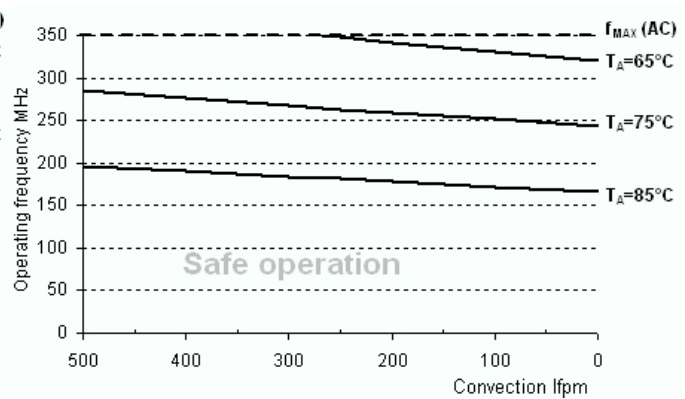


Figure 7. Maximum MPC9443 frequency, $V_{CC} = 3.3V$, MTBF 9.1 years, 4 pF load per line

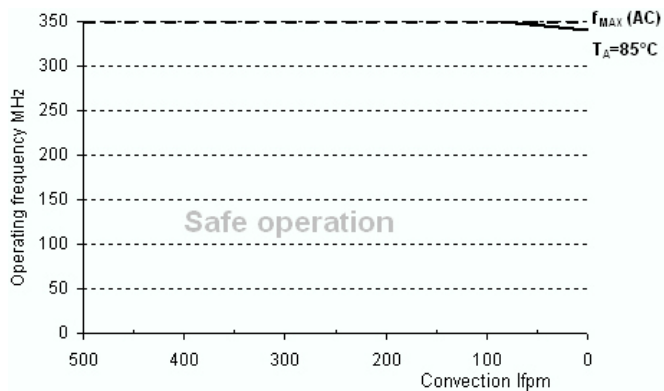


Figure 8. Maximum MPC9443 frequency, $V_{CC} = 3.3V$, MTBF 4 years, driving series terminated transmission lines

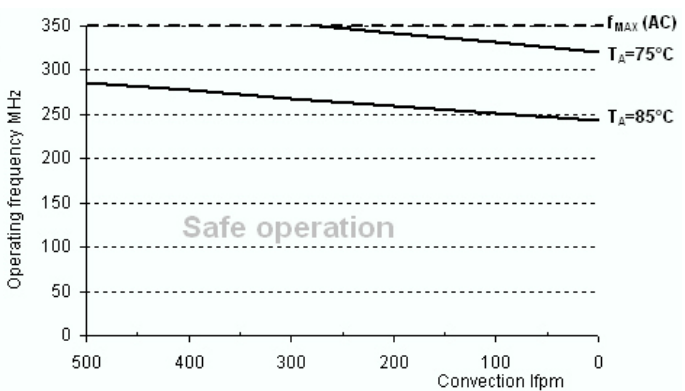


Figure 9. Maximum MPC9443 frequency, $V_{CC} = 3.3V$, MTBF 4 years, 4 pF load per line

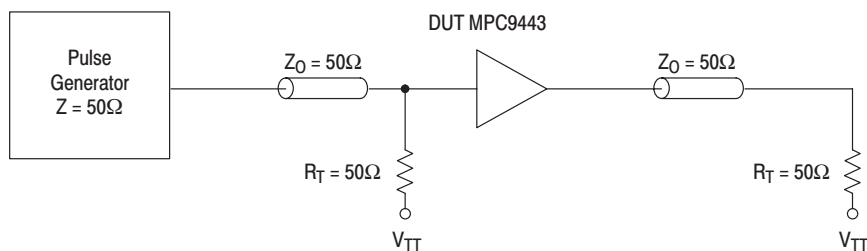


Figure 10. CCLK MPC9443 AC test reference for $V_{CC} = 3.3V$ and $V_{CC} = 2.5V$

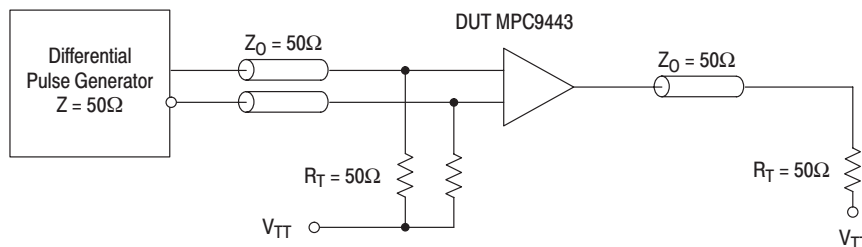


Figure 11. PCLK MPC9443 AC test reference

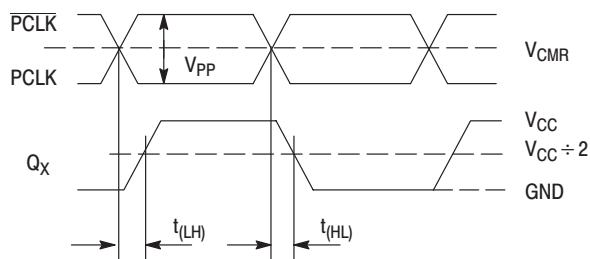


Figure 12. Propagation delay (t_{PD}) test reference

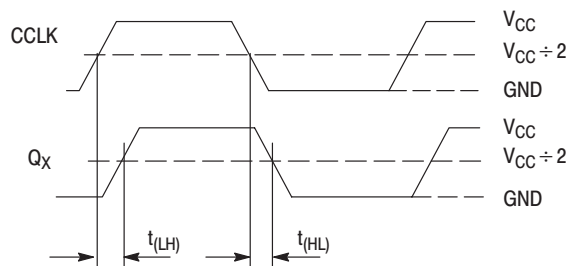


Figure 13. Propagation delay (t_{PD}) test reference

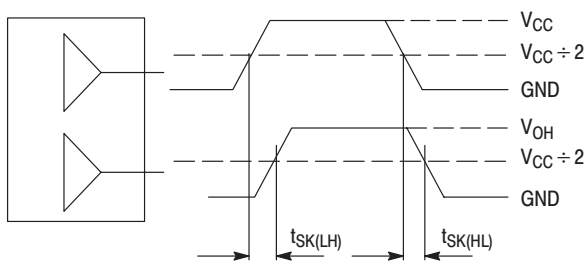
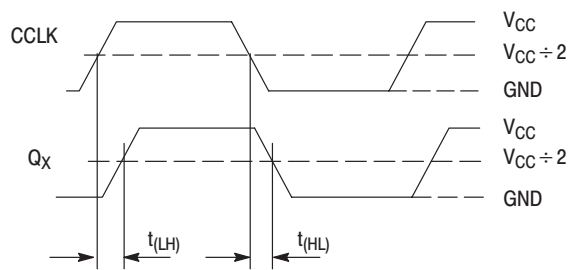


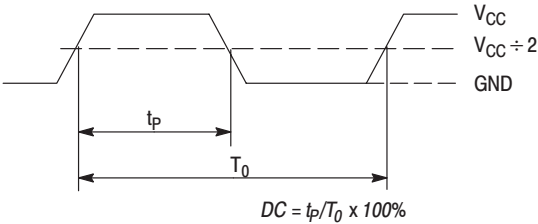
Figure 14. Output-to-output Skew $t_{SK(LH, HL)}$

The pin-to-pin skew is defined as the worst case difference in propagation delay between any two similar delay paths within a single device



$$t_{SK(P)} = |t_{PLH} - t_{PHL}|$$

Figure 15. Output Pulse Skew $t_{SK(P)}$ test reference



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 16. Output Duty Cycle (DC)

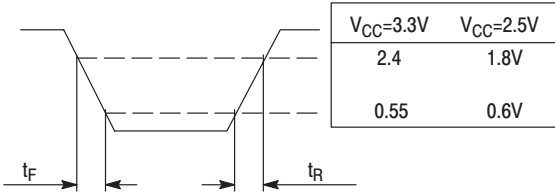
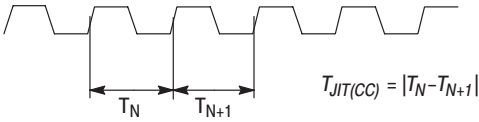


Figure 17. Output Transition Time test reference



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 18. Cycle-to-cycle Jitter

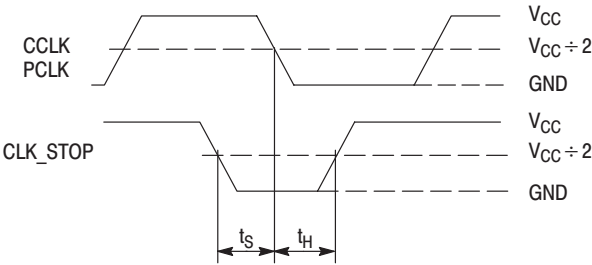


Figure 19. Setup and hold time (t_S , t_H) test reference

2.5V and 3.3V LVCMOS Clock Fanout Buffer

The MPC9446 is a 2.5V and 3.3V compatible 1:10 clock distribution buffer designed for low-voltage mid-range to high-performance telecom, networking and computing applications. Both 3.3V, 2.5V and dual supply voltages are supported for mixed-voltage applications. The MPC9446 offers 10 low-skew outputs and 2 selectable inputs for clock redundancy. The outputs are configurable and support 1:1 and 1:2 output to input frequency ratios. The MPC9446 is specified for the extended temperature range of -40°C to 85°C.

Features

- Configurable 10 outputs LVCMOS clock distribution buffer
- Compatible to single, dual and mixed 3.3V/2.5V voltage supply
- Wide range output clock frequency up to 250 MHz
- Designed for mid-range to high-performance telecom, networking and computer applications
- Supports applications requiring clock redundancy
- Max. output skew of 200 ps (150 ps within one bank)
- Selectable output configurations per output bank
- Tristable outputs
- 32 ld LQFP package
- Ambient operating temperature range of -40 to 85°C

Functional Description

The MPC9446 is a full static fanout buffer design supporting clock frequencies up to 250 MHz. The signals are generated and retimed on-chip to ensure minimal skew between the three output banks. Two independent LVCMOS compatible clock inputs are available. This feature supports redundant clock sources or the addition of a test clock into the system design. Each of the three output banks can be individually supplied by 2.5V or 3.3V supporting mixed voltage applications. The FSELx pins choose between division of the input reference frequency by one or two. The frequency divider can be set individually for each of the three output banks. The MPC9446 can be reset and the outputs are disabled by deasserting the MR/ $\overline{OE}$ pin (logic high state). Asserting MR/ $\overline{OE}$ will enable the outputs.

All inputs accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. Please consult the MPC9456 specification for a 1:10 mixed voltage buffer with LVPECL compatible inputs. For series terminated transmission lines, each of the MPC9446 outputs can drive one or two traces giving the devices an effective fanout of 1:20. The device is packaged in a 7x7 mm² 32-lead LQFP package.

MPC9446**LOW VOLTAGE SINGLE OR
DUAL SUPPLY 2.5V AND 3.3V
LVCMOS CLOCK
DISTRIBUTION BUFFER****FA SUFFIX**
LQFP PACKAGE
CASE 873A**6**

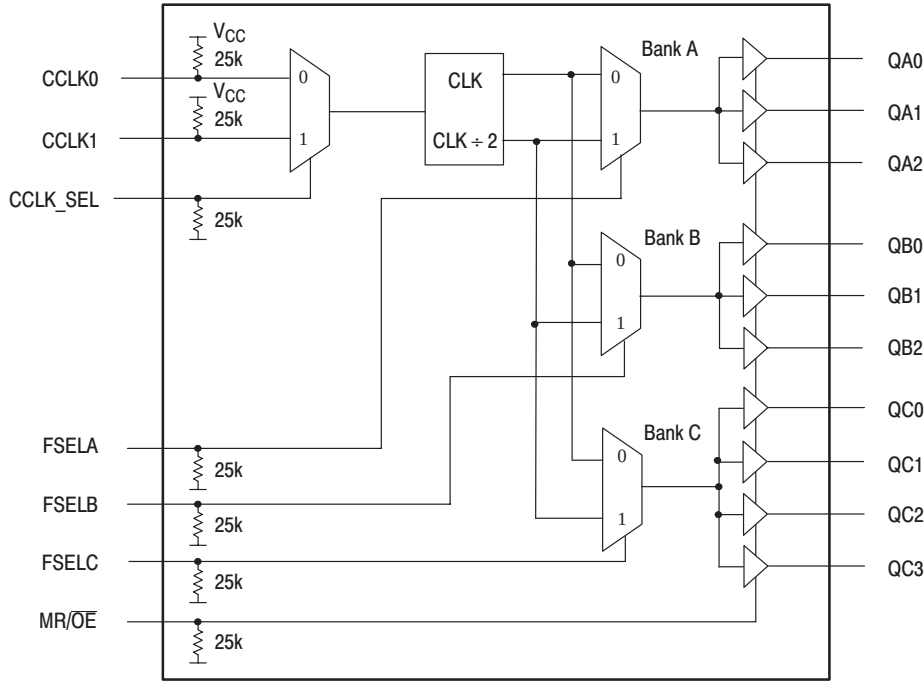


Figure 1. MPC9446 Logic Diagram

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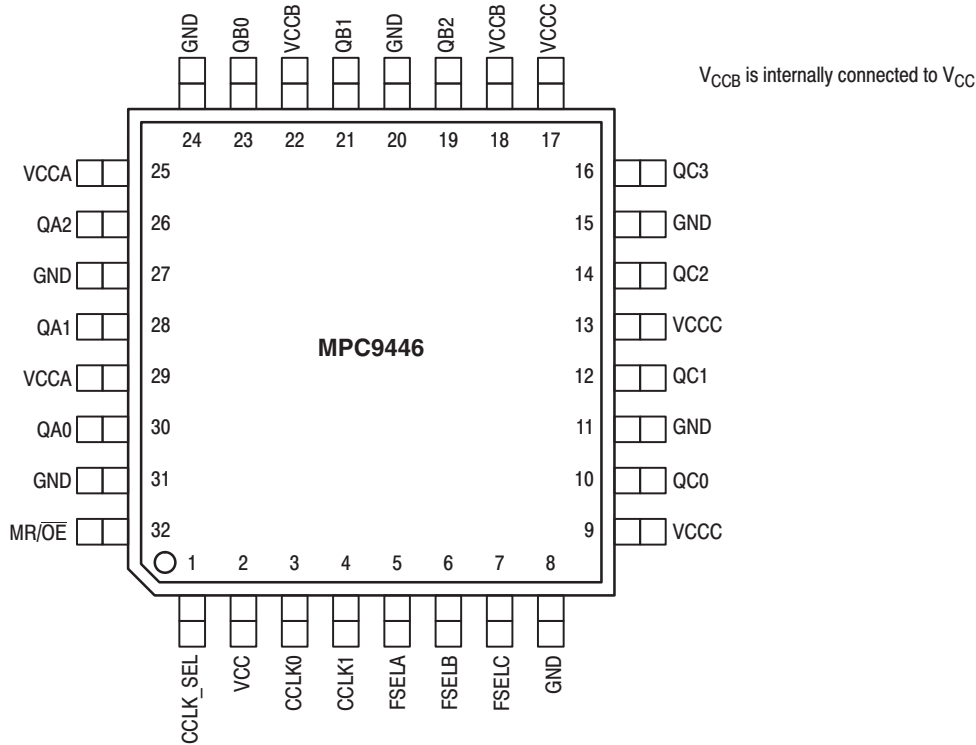


Figure 2. Pinout: 32-Lead Package Pinout (Top View)

Table 1: Pin Configuration

Pin	I/O	Type	Function
CCLK0,1	Input	LVC MOS	LVC MOS clock inputs
FSELA, FSELB, FSELC	Input	LVC MOS	Output bank divide select input
MR/ $\overline{OE}$	Input	LVC MOS	Internal reset and output (high impedance) control
GND		Supply	Negative voltage supply (GND)
VCCA, VCCB*, VCCC		Supply	Positive voltage supply for output banks
VCC		Supply	Positive voltage supply for core (VCC)
QA0 - QA2	Output	LVC MOS	Bank A outputs
QB0 - QB2	Output	LVC MOS	Bank B outputs
QC0 - QC3	Output	LVC MOS	Bank C outputs

* VCCB is internally connected to VCC.

Table 2: Supported Single and Dual Supply Configurations

Supply voltage configuration	V _{CC} ^a	V _{CCA} ^b	V _{CCB} ^c	V _{CCC} ^d	GND
3.3V	3.3V	3.3V	3.3V	3.3V	0V
Mixed voltage supply	3.3V	3.3V or 2.5V	3.3V	3.3V or 2.5V	0 V
2.5V	2.5V	2.5V	2.5V	2.5V	0 V

- a. V_{CC} is the positive power supply of the device core and input circuitry. V_{CC} voltage defines the input threshold and levels
b. V_{CCA} is the positive power supply of the bank A outputs. V_{CCA} voltage defines bank A output levels
c. V_{CCB} is the positive power supply of the bank B outputs. V_{CCB} voltage defines bank B output levels. V_{CCB} is internally connected to V_{CC}.
d. V_{CCC} is the positive power supply of the bank C outputs. V_{CCC} voltage defines bank C output levels

Table 3: Function Table (Controls)

Control	Default	0	1
CCLK_SEL	0	CCLK0	CCLK1
FSELA	0	f _{QA0:2} = f _{REF}	f _{QA0:2} = f _{REF} + 2
FSELB	0	f _{QB0:2} = f _{REF}	f _{QB0:2} = f _{REF} + 2
FSELC	0	f _{QC0:3} = f _{REF}	f _{QC0:3} = f _{REF} + 2
MR/ $\overline{OE}$	0	Outputs enabled	Internal reset Outputs disabled (tristate)

Table 4: Absolute Maximum Ratings^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	3.6	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} +0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} +0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage temperature	-65	125	°C	

- a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 5: General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output Termination Voltage		V _{CC} + 2		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C _{PD}	Power Dissipation Capacitance		10		pF	Per output
C _{IN}	Input Capacitance		4.0		pF	

Table 6: DC CHARACTERISTICS ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Sym- bol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input Low Voltage	-0.3		0.8	V	LVC MOS
I_{IN}	Input Current ^a			200	μA	$V_{IN} = \text{GND}$ or $V_{IN} = V_{CC}$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -24 \text{ mA}^b$
V_{OL}	Output Low Voltage			0.55 0.30	V V	$I_{OL} = 24 \text{ mA}^b$ $I_{OL} = 12 \text{ mA}$
Z_{OUT}	Output Impedance		14 - 17		Ω	
I_{CCQ}^c	Maximum Quiescent Supply Current			2.0	mA	All V_{CC} Pins

a. Input pull-up / pull-down resistors influence input current.

b. The MPC9446 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines.

c. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 7: AC CHARACTERISTICS ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	0		250 ^b	MHz	
f_{MAX}	Maximum Output Frequency	+1 output 0 +2 output 0		250 ^b 125	MHz MHz	FSELx=0 FSELx=1
$t_{P, REF}$	Reference Input Pulse Width	1.4			ns	
t_r, t_f	CCLK Input Rise/Fall Time			1.0 ^c	ns	0.8 to 2.0V
t_{PLH} t_{PHL}	Propagation delay	CCLK0,1 to any Q 2.2 CCLK0,1 to any Q 2.2	2.8 2.8	4.45 4.2	ns ns	
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
$t_{sk(O)}$	Output-to-output Skew	Within one bank Any output bank, same output divider Any output, Any output divider		150 200 350	ps ps ps	
$t_{sk(PP)}$	Device-to-device Skew			2.25	ns	
$t_{SK(P)}$	Output pulse skew ^d			200	ps	
DCQ	Output Duty Cycle	+1 output 47 +2 output 45	50 50	53 55	% %	DC _{REF} = 50% DC _{REF} = 25%-75%
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b. The MPC9446 is functional up to an input and output clock frequency of 350 MHz and is characterized up to 250 MHz.

c. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.

d. Output pulse skew is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.

Table 8: DC CHARACTERISTICS ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Sym- bol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	1.7		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input Low Voltage	-0.3		0.7	V	LVC MOS
V_{OH}	Output High Voltage	1.8			V	$I_{OH} = -15\text{ mA}^a$
V_{OL}	Output Low Voltage			0.6	V	$I_{OL} = 15\text{ mA}$
Z_{OUT}	Output Impedance		17 - 20 ^b		Ω	
I_{IN}	Input Current ^b			± 200	μA	$V_{IN} = \text{GND}$ or $V_{IN} = V_{CC}$
I_{CCQ}^c	Maximum Quiescent Supply Current			2.0	mA	All V_{CC} Pins

- a. The MPC9446 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.
- b. Input pull-up / pull-down resistors influence input current.
- c. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 9: AC CHARACTERISTICS ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)^{a b}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	0		250 ^c	MHz	
f_{MAX}	Maximum Output Frequency	+1 output 0 +2 output 0		250 ^b 125	MHz MHz	FSELx=0 FSELx=1
$t_{P, REF}$	Reference Input Pulse Width	1.4			ns	
t_r, t_f	CCLK Input Rise/Fall Time			1.0 ^d	ns	0.7 to 1.7V
t_{PLH} t_{PHL}	Propagation delay CCLK0,1 to any Q CCLK0,1 to any Q	2.6 2.6		5.6 5.5	ns ns	
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
$t_{sk(O)}$	Output-to-output Skew Within one bank Any output bank, same output divider Any output, Any output divider			150 200 350	ps ps ps	
$t_{sk(PP)}$	Device-to-device Skew			3.0	ns	
$t_{SK(P)}$	Output pulse skew ^e			200	ps	
DC_Q	Output Duty Cycle	+1 or +2 output 45	50	55	%	$DC_{REF} = 50\%$
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.6 to 1.8V

- a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
- b. AC specifications are design targets, final specification is pending device characterization.
- c. The MPC9446 is functional up to an input and output clock frequency of 350 MHz and is characterized up to 250 MHz.
- d. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
- e. Output pulse skew is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.

Table 10: AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $V_{CCA}, V_{CCB}, V_{CCC} = 2.5V \pm 5\%$ or $3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)^{a b}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
$t_{sk(O)}$	Output-to-output Skew Within one bank Any output bank, same output divider Any output, Any output divider			150 250 350	ps ps ps	
$t_{sk(PP)}$	Device-to-device Skew			2.5	ns	
$t_{PLH, HL}$	Propagation delay CCLK0,1 to any Q	See 3.3V table				
$t_{SK(P)}$	Output pulse skew ^c			250	ps	
DC_Q	Output Duty Cycle	+1 or +2 output 45	50	55	%	$DC_{REF} = 50\%$

- a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
- b. For all other AC specifications, refer to 2.5V or 3.3V tables according to the supply voltage of the output bank.
- c. Output pulse skew is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC9446 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC} \div 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9446 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9446 clock driver is effectively doubled due to its capability to drive multiple lines.

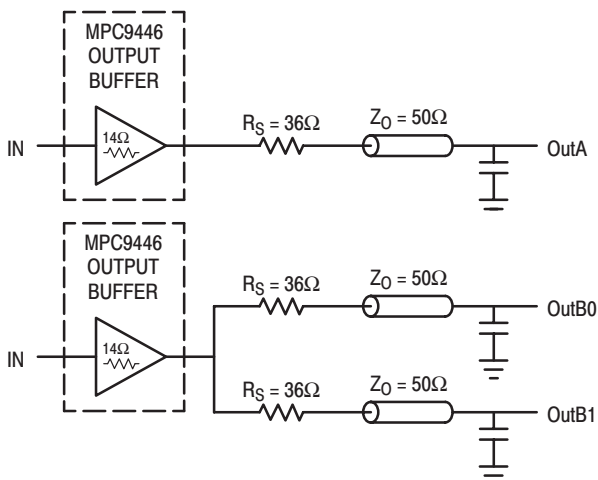


Figure 3. Single versus Dual Transmission Lines

The waveform plots in Figure 4 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9446 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9446. The output waveform in Figure 4 “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω se-

ries resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned} V_L &= V_S (Z_0 \div (R_S + R_0 + Z_0)) \\ Z_0 &= 50\Omega \parallel 50\Omega \\ R_S &= 36\Omega \parallel 36\Omega \\ R_0 &= 14\Omega \\ V_L &= 3.0 (25 \div (18 + 14 + 25)) \\ &= 1.31V \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

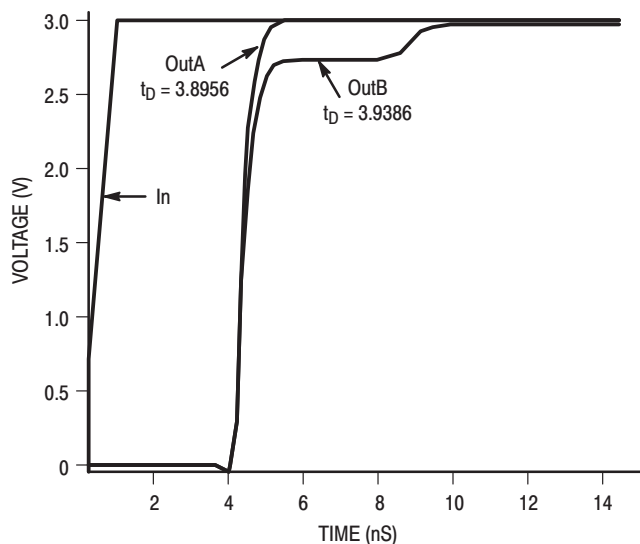


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

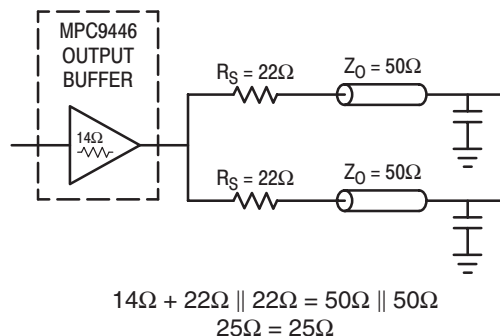


Figure 5. Optimized Dual Line Termination

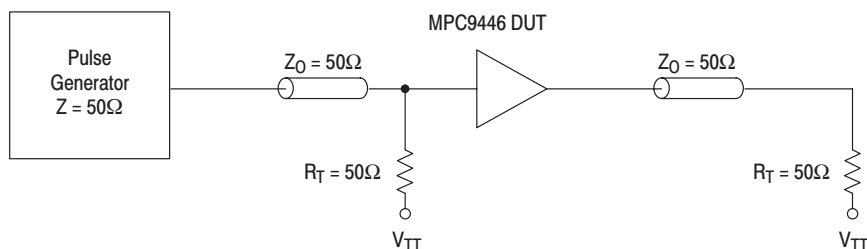


Figure 6. CCLK0,1 MPC9446 AC test reference for $V_{CC} = 3.3V$ and $V_{CC} = 2.5V$

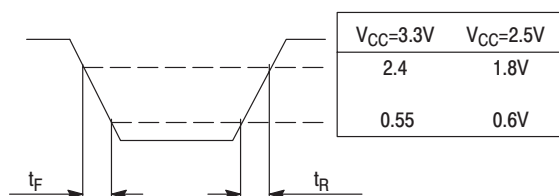


Figure 7. Output Transition Time Test Reference

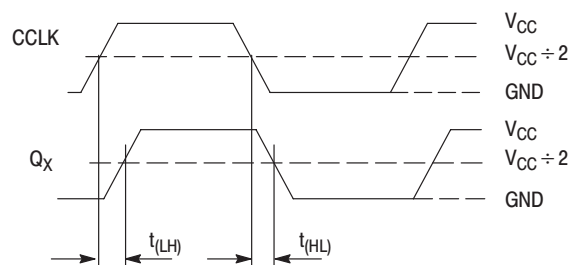
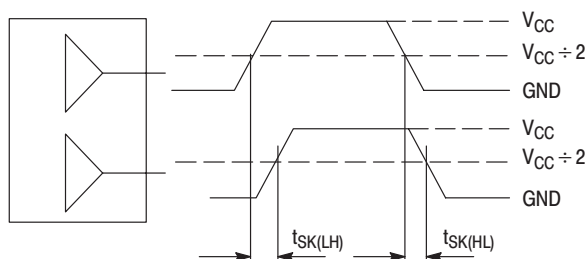
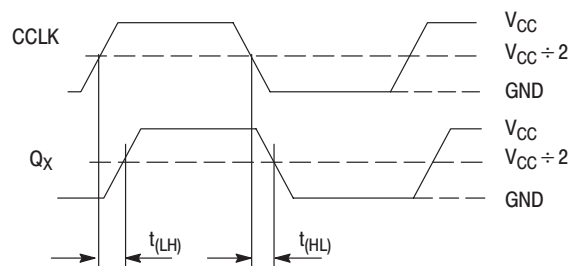


Figure 8. Propagation delay (t_{pD}) test reference



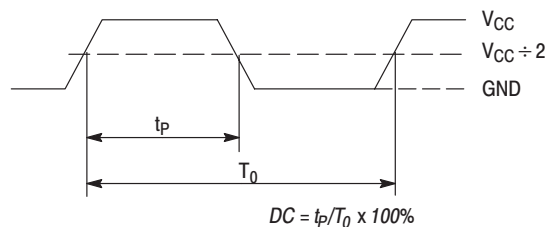
The pin-to-pin skew is defined as the worst case difference in propagation delay between any two similar delay paths within a single device

Figure 9. Output-to-output Skew $t_{SK(LH, HL)}$



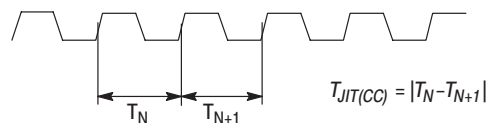
$$t_{SK(P)} = |t_{PLH} - t_{PHL}|$$

Figure 10. Output Pulse Skew ($t_{SK(P)}$) test reference



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 11. Output Duty Cycle (DC)



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 12. Cycle-to-cycle Jitter

3.3V/2.5V 1:9 LVCMOS Clock Fanout Buffer

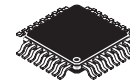
The MPC9447 is a 3.3V or 2.5V compatible, 1:9 clock fanout buffer targeted for high performance clock tree applications. With output frequencies up to 350 MHz and output skews less than 150 ps, the device meets the needs of most demanding clock applications.

Features

- 9 LVCMOS Compatible Clock Outputs
- 2 Selectable, LVCMOS Compatible Inputs
- Maximum Clock Frequency of 350 MHz
- Maximum Clock Skew of 150 ps
- Synchronous Output Stop in Logic Low State Eliminates Output Runt Pulses
- High-Impedance Output Control
- 3.3V or 2.5V Power Supply
- Drives up to 18 Series Terminated Clock Lines
- Ambient Temperature Range -40°C to $+85^{\circ}\text{C}$
- 32 Lead LQFP Packaging
- Supports Clock Distribution in Networking, Telecommunications, and Computer Applications
- Pin and Function Compatible to MPC947

MPC9447

**LOW VOLTAGE
3.3 V/2.5 V LVCMOS 1:9
CLOCK FANOUT BUFFER**



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A

6

Functional Description

MPC9447 is specifically designed to distribute LVCMOS compatible clock signals up to a frequency of 350 MHz. Each output provides a precise copy of the input signal with a near zero skew. The outputs buffers support driving of 50Ω terminated transmission lines on the incident edge: each is capable of driving either one parallel terminated or two series terminated transmission lines.

Two selectable independent LVCMOS compatible clock inputs are available, providing support of redundant clock source systems. The MPC9447 CLK_STOP control is synchronous to the falling edge of the input clock. It allows the start and stop of the output clock signal only in a logic low state, thus eliminating potential output runt pulses. Applying the OE control will force the outputs into high-impedance mode.

All inputs have an internal pull-up or pull-down resistor preventing unused and open inputs from floating. The device supports a 2.5V or 3.3V power supply and an ambient temperature range of -40°C to $+85^{\circ}\text{C}$. The MPC9447 is pin and function compatible but performance-enhanced to the MPC947.

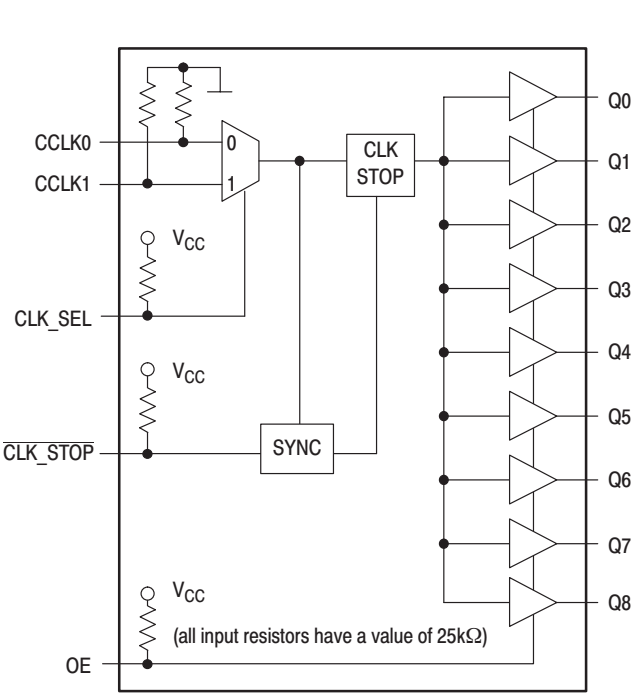


Figure 1. Logic Diagram

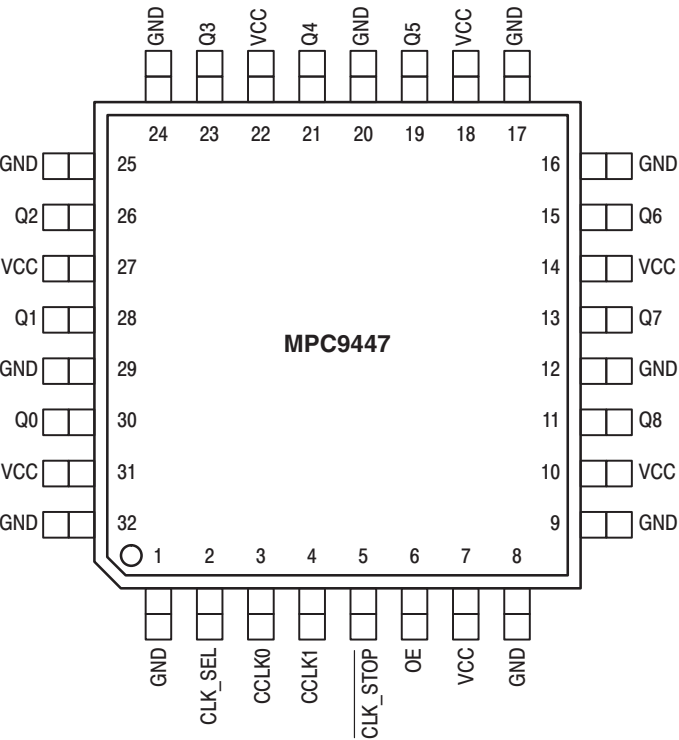


Figure 2. 32-Lead Pinout (Top View)

Table 1. Function Table

Control	Default	0	1
CLK_SEL	1	CLK0 input selected	CLK1 input selected
OE	1	Outputs disabled (high-impedance state) ^a	Outputs enabled
CLK_STOP	1	Outputs synchronously stopped in logic low state	Outputs active

a. OE = 0 will high-impedance tristate all outputs independent on CLK_STOP

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Table 2. Pin Configuration

Pin	I/O	Type	Function
CCLK0	Input	LVC MOS	Clock signal input
CCLK1	Input	LVC MOS	Alternative clock signal input
CLK_SEL	Input	LVC MOS	Clock input select
CLK_STOP	Input	LVC MOS	Clock output enable/disable
OE	Input	LVC MOS	Output enable/disable (high-impedance tristate)
Q0–8	Output	LVC MOS	Clock outputs
GND	Supply	Ground	Negative power supply (GND)
VCC	Supply	VCC	Positive power supply for I/O and core. All VCC pins must be connected to the positive power supply for correct operation

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output termination voltage		V _{CC} ÷ 2		V	
MM	ESD protection (Machine model)	200			V	
HBM	ESD protection (Human body model)	2000			V	
LU	Latch-up immunity	200			mA	
C _{PD}	Power dissipation capacitance		10		pF	Per output
C _{IN}	Input capacitance		4.0		pF	Inputs

Table 4. Absolute Maximum Ratings^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	3.9	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} + 0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} + 0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 40°C to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{IH}	Input High Voltage	2.0		V _{CC} + 0.3	V	LVC MOS
V _{IL}	Input Low Voltage	-0.3		0.8	V	LVC MOS
V _{OH}	Output High Voltage	2.4			V	I _{OH} = -24 mA ^a
V _{OL}	Output Low Voltage			0.55 0.30	V V	I _{OL} = 24 mA I _{OL} = 12 mA
Z _{OUT}	Output Impedance		17		Ω	
I _{IN}	Input Current ^b			±300	μA	V _{IN} = V _{CC} or GND
I _{CCQ}	Maximum Quiescent Supply Current ^c			2.0	mA	All V _{CC} Pins

- a. The MPC9447 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines (for V_{CC}=3.3V).
b. Inputs have pull-down or pull-up resistors affecting the input current.
c. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

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Table 6. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = -40°C to +85°C)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f _{ref}	Input Frequency	0		350	MHz	
f _{max}	Output Frequency	0		350	MHz	
f _{P,REF}	Reference Input Pulse Width	1.4			ns	
t _r , t _f	CCLK0, CCLK1 Input Rise/Fall Time			1.0 ^b	ns	0.8 to 2.0V
t _{PLH/HL}	Propagation Delay CCLK0 or CCLK1 to any Q	1.3		3.3	ns	
t _{PLZ, HZ}	Output Disable Time			11	ns	
t _{PZL, ZH}	Output Enable Time			11	ns	
t _S	Setup Time CCLK0 or CCLK1 to CLK_STOP ^c	0.0			ns	
t _H	Hold Time CCLK0 or CCLK1 to CLK_STOP ^c	1.0			ns	
t _{sk(O)}	Output-to-Output Skew			150	ps	
t _{sk(PP)}	Device-to-Device Skew			2.0	ns	
t _{SK(P)}	Output Pulse Skew ^d			300	ps	DC _{REF} = 50%
DC _Q	Output Duty Cycle f _Q < 170 MHz	45	50	55	%	
t _r , t _f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
t _{JIT(CC)}	Cycle-to-cycle jitter RMS (1 σ)		TBD		ps	

- a. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
b. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
c. Setup and hold times are referenced to the falling edge of the selected clock signal input.
d. Output pulse skew is the absolute difference of the propagation delay times: | t_{PLH} - t_{PHL} |.

Table 7. DC Characteristics ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	1.7		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input Low Voltage	-0.3		0.7	V	LVC MOS
V_{OH}	Output High Voltage	1.8			V	$I_{OH} = -15\text{ mA}^a$
V_{OL}	Output Low Voltage			0.6	V	$I_{OL} = 15\text{ mA}$
Z_{OUT}	Output Impedance		19		Ω	
I_{IN}	Input Current ^b			± 300	μA	$V_{IN} = V_{CC}$ or GND
I_{CCQ}	Maximum Quiescent Supply Current ^c			2.0	mA	All V_{CC} Pins

a. The MPC9447 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives one 50Ω series terminated transmission lines per output ($V_{CC}=2.5V$).

b. Inputs have pull-down or pull-up resistors affecting the input current.

c. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 8. AC Characteristics ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	0		350	MHz	
f_{max}	Output frequency	0		350	MHz	
$t_{P,REF}$	Reference Input Pulse Width	1.4			ns	
t_r, t_f	CCLK0, CCLK1 Input Rise/Fall Time			1.0 ^b	ns	0.7 to 1.7V
$t_{PLH/HL}$	Propagation Delay CCLK0 or CCLK1 to any Q	1.7		4.4	ns	
$t_{PLZ, HZ}$	Output Disable Time			11	ns	
$t_{PZL, ZH}$	Output Enable Time			11	ns	
t_S	Setup Time CCLK0 or CCLK1 to CLK_STOP ^c	0.0			ns	
t_H	Hold Time CCLK0 or CCLK1 to CLK_STOP ^c	1.0			ns	
$t_{sk(O)}$	Output-to-Output Skew			150	ps	
$t_{sk(PP)}$	Device-to-Device Skew			2.7	ns	
$t_{sk(P)}$	Output Pulse Skew ^d			200	ps	$DC_{REF} = 50\%$
DC_Q	Output Duty Cycle $f_Q < 350\text{ MHz}$	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.6 to 1.8V
$t_{JIT(CC)}$	Cycle-to-cycle jitter RMS (1 σ)		TBD		ps	

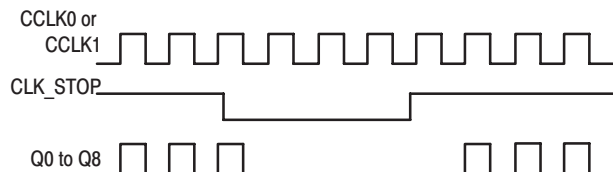
a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.

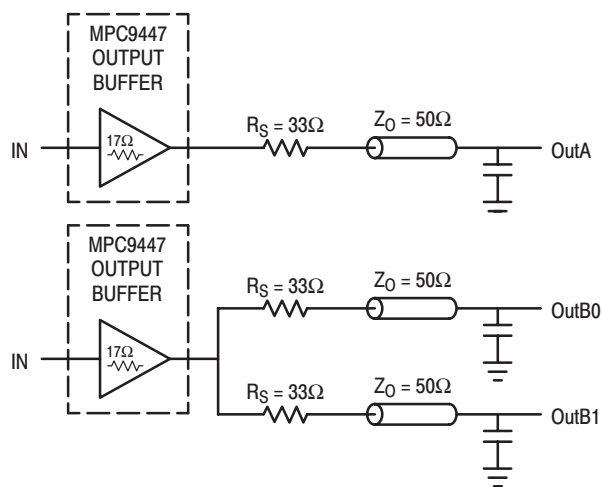
c. Setup and hold times are referenced to the falling edge of the selected clock signal input.

d. Output pulse skew is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$

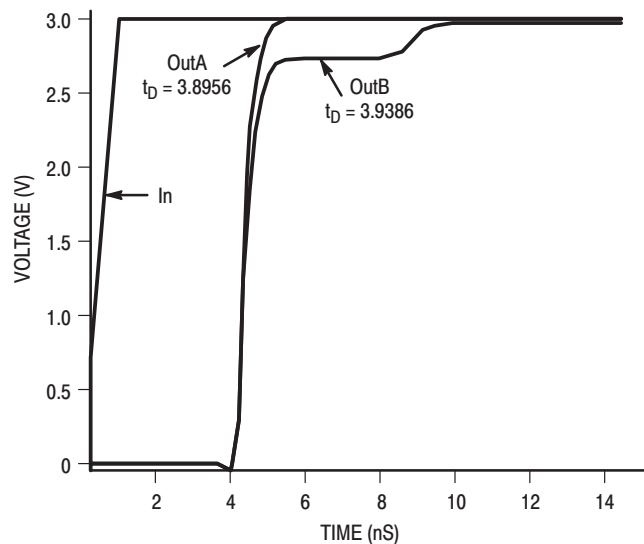
APPLICATION INFORMATION

Figure 3. Output Clock Stop (CLK_STOP) Timing Diagram**Driving Transmission Lines**

The MPC9447 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of 17Ω ($V_{CC}=3.3V$), the outputs can drive either parallel or series terminated transmission lines. For more information on transmission lines, the reader is referred to Motorola application note AN1091. In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}+2$.

**Figure 4. Single versus Dual Transmission Lines**

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9447 clock driver. For the series terminated case, however, there is no DC current draw; thus, the outputs can drive multiple series terminated lines. Figure 4 “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fanout of the MPC9447 clock driver is effectively doubled due to its capability to drive multiple lines at $V_{CC}=3.3V$.

**Figure 5. Single versus Dual Line Termination Waveforms**

The waveform plots in Figure 5 “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases, the drive capability of the MPC9447 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9447. The output waveform in Figure 5 “Single versus Dual Line Termination Waveforms” shows a step in the waveform; this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 33Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned}
 V_L &= V_S (Z_0 \div (R_S + R_0 + Z_0)) \\
 Z_0 &= 50\Omega \parallel 50\Omega \\
 R_S &= 33\Omega \parallel 33\Omega \\
 R_0 &= 17\Omega \\
 V_L &= 3.0 (25 \div (16.5 + 17 + 25)) \\
 &= 1.28V
 \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

Since this step is well above the threshold region it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in Figure 6 “Optimized Dual Line Termination” should be used. In this case, the series terminating resistors are reduced

such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

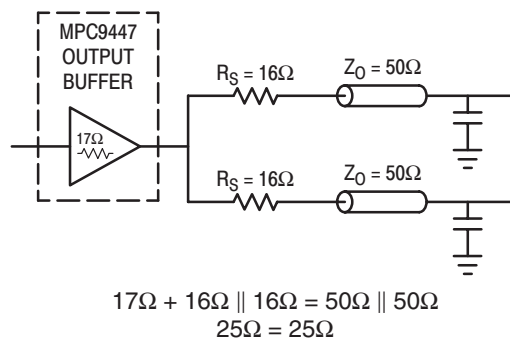


Figure 6. Optimized Dual Line Termination

The Following Figures Illustrate the Measurement Reference for the MPC9447 Clock Driver Circuit

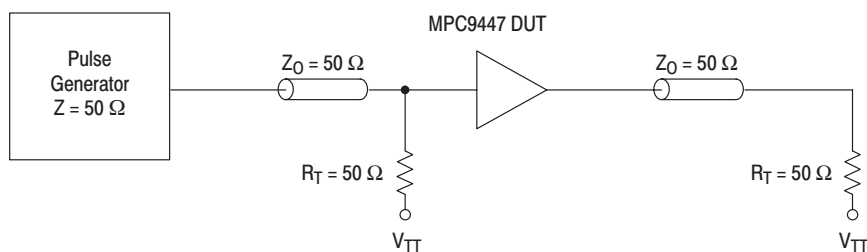


Figure 7. CCLK MPC9447 AC Test Reference for $V_{CC} = 3.3V$ and $V_{CC} = 2.5V$

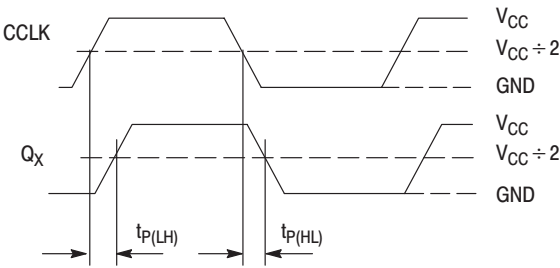
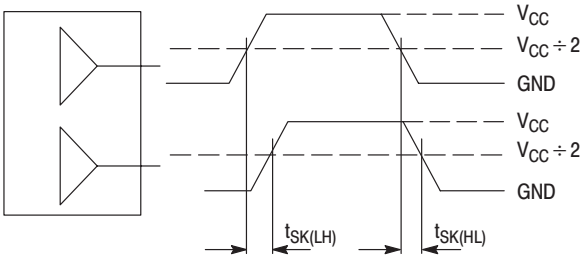
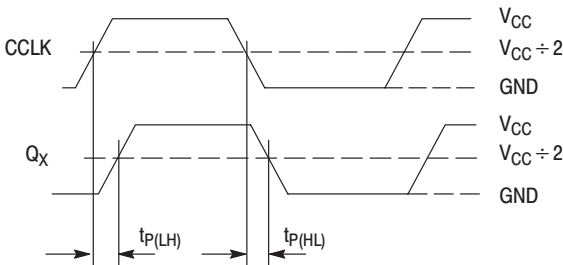


Figure 8. Propagation Delay (t_{PD}) Test Reference



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

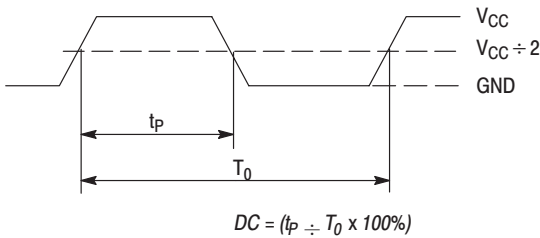
Figure 9. Output-to-Output Skew $t_{SK(LH, HL)}$



$$t_{SK(P)} = |t_{PLH} - t_{PHL}|$$

Figure 10. Output Pulse Skew ($t_{SK(P)}$) Test Reference

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The time from the output controlled edge to the non-controlled edge, divided by the time between output controlled edges, expressed as a percentage

Figure 11. Output Duty Cycle (DC)

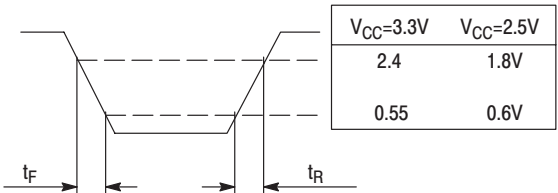
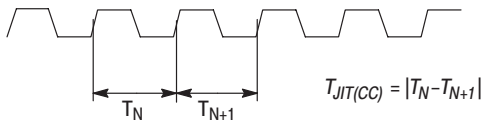


Figure 12. Output Transition Time Test Reference



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 13. Cycle-to-Cycle Jitter

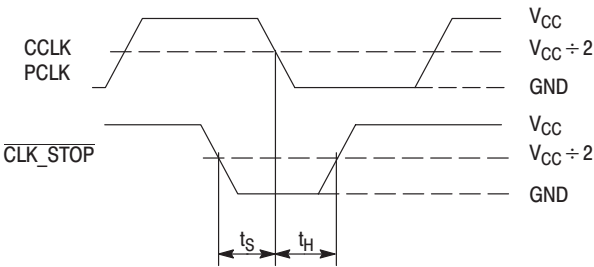


Figure 14. Setup and Hold Time (t_s, t_H) Test Reference

3.3V/2.5V LVCMOS 1:12 Clock Fanout Buffer

The MPC9448 is a 3.3V or 2.5V compatible, 1:12 clock fanout buffer targeted for high performance clock tree applications. With output frequencies up to 350 MHz and output skews less than 150 ps, the device meets the needs of most demanding clock applications.

- 12 LVCMOS compatible clock outputs
- Selectable LVCMOS and differential LVPECL compatible clock inputs
- Maximum clock frequency of 350 MHz
- Maximum clock skew of 150 ps
- Synchronous output stop in logic low state eliminates output runt pulses
- High-impedance output control
- 3.3V or 2.5V power supply
- Drives up to 24 series terminated clock lines
- Ambient temperature range -40°C to $+85^{\circ}\text{C}$
- 32-Lead LQFP packaging
- Supports clock distribution in networking, telecommunication and computing applications
- Pin and function compatible to MPC948

Functional Description

The MPC9448 is specifically designed to distribute LVCMOS compatible clock signals up to a frequency of 350 MHz. Each output provides a precise copy of the input signal with a near zero skew. The outputs buffers support driving of 50Ω terminated transmission lines on the incident edge: each output is capable of driving either one parallel terminated or two series terminated transmission lines.

Two selectable, independent clock inputs are available, providing support of LVCMOS and differential LVPECL clock distribution systems. The MPC9448 CLK_STOP control is synchronous to the falling edge of the input clock. It allows the start and stop of the output clock signal only in a logic low state, thus eliminating potential output runt pulses. Applying the OE control will force the outputs into high-impedance mode.

All inputs have an internal pull-up or pull-down resistor preventing unused and open inputs from floating. The device supports a 2.5V or 3.3V power supply and an ambient temperature range of -40°C to $+85^{\circ}\text{C}$. The MPC9448 is pin and function compatible but performance-enhanced to the MPC948.

MPC9448

LOW VOLTAGE
3.3V/2.5V LVCMOS 1:12
CLOCK FANOUT BUFFER



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A

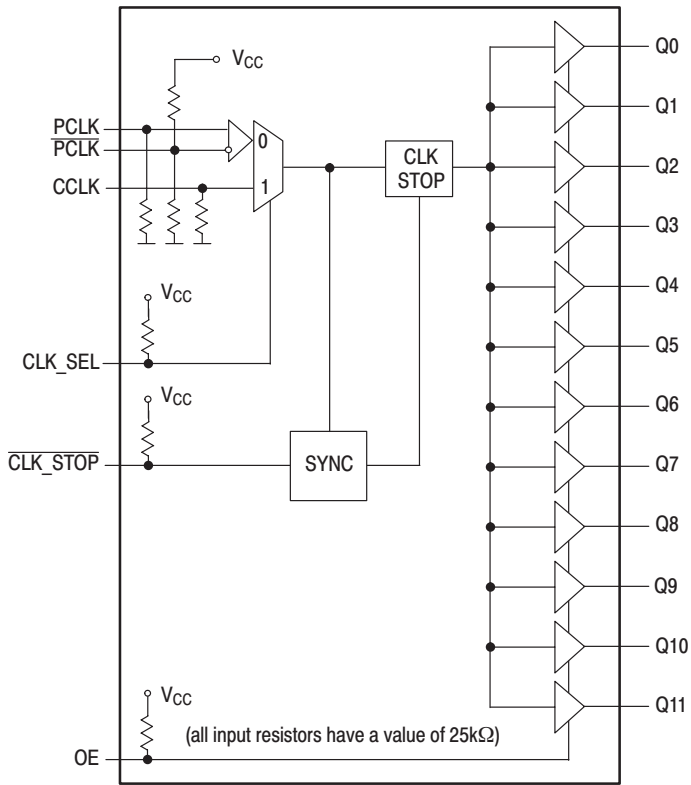


Figure 1. Logic Diagram

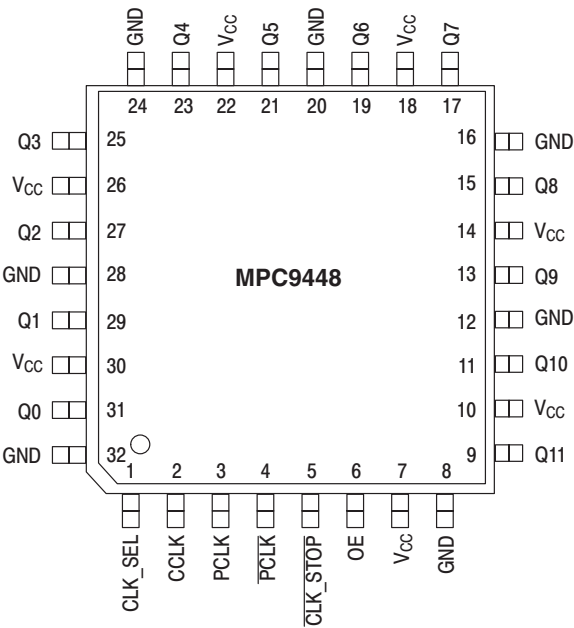


Figure 2. 32-Lead Package Pinout (Top View)

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Table 1: FUNCTION TABLE

Control	Default	0	1
CLK_SEL	1	PECL differential input selected	CCLK input selected
OE	1	Outputs disabled (high-impedance state) ¹	Outputs enabled
CLK_STOP	1	Outputs synchronously stopped in logic low state	Outputs active

3. OE=0 will high-impedance tristate all outputs independent on CLK_STOP.

Table 2: PIN CONFIGURATION

Pin	I/O	Type	Function
PCLK, PCLK	Input	LVPECL	Clock signal input
CCLK	Input	LVC MOS	Alternative clock signal input
CLK_SEL	Input	LVC MOS	Clock input select
CLK_STOP	Input	LVC MOS	Clock output enable/disable
OE	Input	LVC MOS	Output enable/disable (high-impedance tristate)
Q0–11	Output	LVC MOS	Clock outputs
GND	Supply	Ground	Negative power supply (GND)
VCC	Supply	VCC	Positive power supply for I/O and core. All VCC pins must be connected to the positive power supply for correct operation

Table 3: ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	3.9	V
V_{IN}	DC Input Voltage	-0.3	$V_{CC} + 0.3$	V
V_{OUT}	DC Output Voltage	-0.3	$V_{CC} + 0.3$	V
I_{IN}	DC Input Current		± 20	mA
I_{OUT}	DC Output Current		± 50	mA
T_{Stor}	Storage Temperature Range	-65	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 4: GENERAL SPECIFICATIONS

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per Output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 5: DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		$V_{CC} + 0.3$	V	LVCMOS
V_{IL}	Input LOW Voltage	-0.3		0.8	V	LVCMOS
V_{PP}	Peak-to-Peak Input Voltage PCLK	250			mV	LVPECL
V_{CMR}^a	Common Mode Range PCLK	1.1		$V_{CC} - 0.6$	V	LVPECL
I_{IN}	Input Current ^b			300	μA	$V_{IN} = V_{CC}$ or GND
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -24\text{mA}^c$
V_{OL}	Output LOW Voltage			0.55 0.30	V V	$I_{OL} = 24\text{mA}^c$ $I_{OL} = 12\text{mA}$
Z_{OUT}	Output Impedance		17		Ω	
I_{CCQ}^d	Maximum Quiescent Supply Current			2.0	mA	All V_{CC} Pins

- a. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
- b. Input pull-up / pull-down resistors influence input current.
- c. The MPC9448 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines (for $V_{CC}=3.3V$) or one 50Ω series terminated transmission line (for $V_{CC}=2.5V$).
- d. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 6: AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	0		350	MHz	
f_{MAX}	Maximum Output Frequency	0		350	MHz	
V_{PP}	Peak-to-peak input voltage PCLK	400		1000	mV	LVPECL
V_{CMR}^b	Common Mode Range PCLK	1.3		$V_{CC}-0.8$	V	LVPECL
$t_{P, REF}$	Reference Input Pulse Width	1.4			ns	
t_r, t_f	CCLK Input Rise/Fall Time			1.0 ^c	ns	0.8 to 2.0V
$t_{PLH/HL}$	Propagation delay PCLK to any Q	1.6		3.6	ns	
$t_{PLH/HL}$	Propagation delay CCLK to any Q	1.3		3.3	ns	
$t_{PLZ, HZ}$	Output Disable Time			11	ns	
$t_{PZL, LZ}$	Output Enable Time			11	ns	
t_S	Setup time CCLK to $\overline{CLK\_STOP}$	0.0			ns	
	PCLK to $\overline{CLK\_STOP}$	0.0			ns	
t_H	Hold time CCLK to $\overline{CLK\_STOP}$	1.0			ns	
	PCLK to $\overline{CLK\_STOP}$	1.5			ns	
$t_{sk(O)}$	Output-to-output Skew			150	ps	
$t_{sk(PP)}$	Device-to-device Skew PCLK or CCLK to any Q			2.0	ns	
$t_{sk(P)}$	Output pulse skew ^d Using CCLK			300	ps	
	Using PCLK			400	ps	
DC_Q	Output Duty Cycle $f_Q < 170$ MHz	45	50	55	%	$DC_{REF} = 50\%$
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts $t_{PLH/HL}$ and $t_{sk(PP)}$.

c. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.

d. Output pulse skew is the absolute difference of the propagation delay times: $|t_{pLH} - t_{pHL}|$.

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Table 7: DC CHARACTERISTICS ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	1.7		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input low voltage	-0.3		0.7	V	LVC MOS
V_{PP}	Peak-to-peak input voltage PCLK	250			mV	LVPECL
V_{CMR}^a	Common Mode Range PCLK	1.0		$V_{CC}-0.7$	V	LVPECL
I_{IN}	Input current ^b			300	μA	$V_{IN}=GND$ or $V_{IN}=V_{CC}$
V_{OH}	Output High Voltage	1.8			V	$I_{OH} = -15$ mA ^c
V_{OL}	Output Low Voltage			0.6	V	$I_{OL} = 15$ mA ^c
Z_{OUT}	Output impedance		19		Ω	
I_{CCQd}	Maximum Quiescent Supply Current			2.0	mA	All V_{CC} Pins

a. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.

b. Input pull-up / pull-down resistors influence input current.

c. The MPC9448 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives one 50Ω series terminated transmission lines at $V_{CC}=2.5V$.

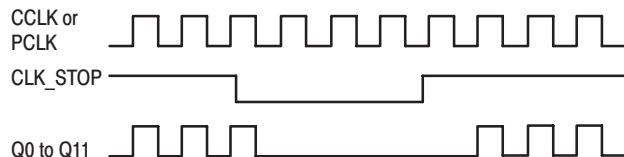
d. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 8: AC CHARACTERISTICS ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$)^a

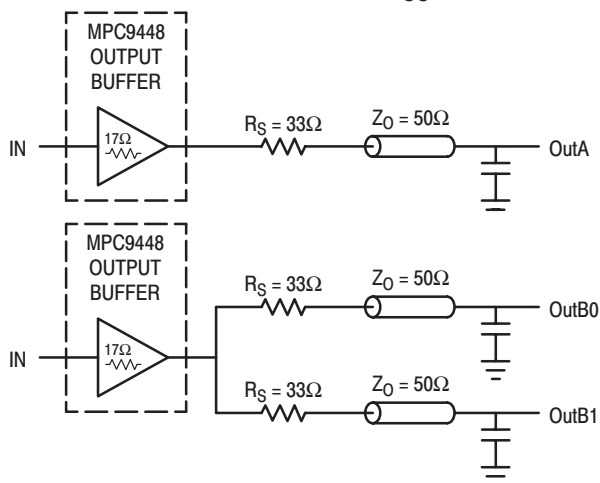
Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	0		350	MHz	
f_{MAX}	Maximum Output Frequency	0		350	MHz	
V_{PP}	Peak-to-peak input voltage PCLK	400		1000	mV	LVPECL
V_{CMR}^b	Common Mode Range PCLK	1.2		$V_{CC}-0.8$	V	LVPECL
$t_{P, REF}$	Reference Input Pulse Width	1.4			ns	
t_r, t_f	CCLK Input Rise/Fall Time			1.0 ^c	ns	0.8 to 2.0V
$t_{PLH/HL}$ $t_{PLH/HL}$	Propagation delay PCLK to any Q CCLK to any Q	1.5 1.7		4.2 4.4	ns ns	
$t_{PLZ, HZ}$	Output Disable Time			11	ns	
$t_{PZL, LZ}$	Output Enable Time			11	ns	
t_S	Setup time CCLK to CLK_STOP PCLK to CLK_STOP	0.0 0.0			ns ns	
t_H	Hold time CCLK to CLK_STOP PCLK to CLK_STOP	1.0 1.5			ns ns	
$t_{sk(O)}$	Output-to-output Skew			150	ps	
$t_{sk(PP)}$	Device-to-device Skew PCLK or CCLK to any Q			2.7	ns	
$t_{SK(p)}$	Output pulse skew ^d Using CCLK Using PCLK			200 300	ps ps	
DC_Q	Output Duty Cycle $f_Q < 350$ MHz and using CCLK $f_Q < 200$ MHz and using PCLK	45 45	50 50	55 55	% %	$DC_{REF} = 50\%$
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.6 to 1.8V

- a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
- b. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts $t_{PLH/HL}$ and $t_{SK(PP)}$.
- c. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
- d. Output pulse skew is the absolute difference of the propagation delay times: $|t_{pLH} - t_{pHL}|$.

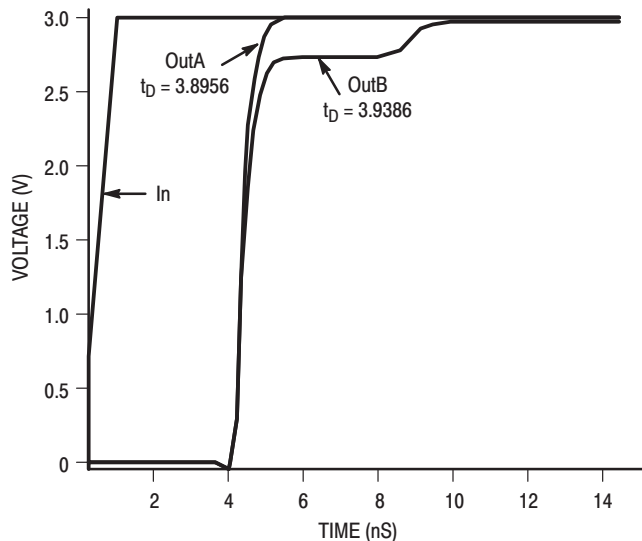
APPLICATIONS INFORMATION

Figure 3. Output Clock Stop (CLK_STOP) Timing Diagram**Driving Transmission Lines**

The MPC9448 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of 17Ω ($V_{CC}=3.3V$), the outputs can drive either parallel or series terminated transmission lines. For more information on transmission lines, the reader is referred to Motorola application note AN1091. In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}/2$.

**Figure 4. Single versus Dual Transmission Lines**

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9448 clock driver. For the series terminated case, however, there is no DC current draw; thus, the outputs can drive multiple series terminated lines. Figure 4 "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fanout of the MPC9448 clock driver is effectively doubled due to its capability to drive multiple lines at $V_{CC}=3.3V$.

**Figure 5. Single versus Dual Line Termination Waveforms**

The waveform plots in Figure 5 "Single versus Dual Line Termination Waveforms" show the simulation results of an output driving a single line versus two lines. In both cases, the drive capability of the MPC9448 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9448. The output waveform in Figure 5 "Single versus Dual Line Termination Waveforms" shows a step in the waveform; this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 33Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned}
 V_L &= V_S (Z_0 / (R_S + R_0 + Z_0)) \\
 Z_0 &= 50\Omega \parallel 50\Omega \\
 R_S &= 33\Omega \parallel 33\Omega \\
 R_0 &= 17\Omega \\
 V_L &= 3.0 (25 / (16.5 + 17 + 25)) \\
 &= 1.28V
 \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

Since this step is well above the threshold region it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in Figure 6 “Optimized Dual Line Termination” should be used. In this case, the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

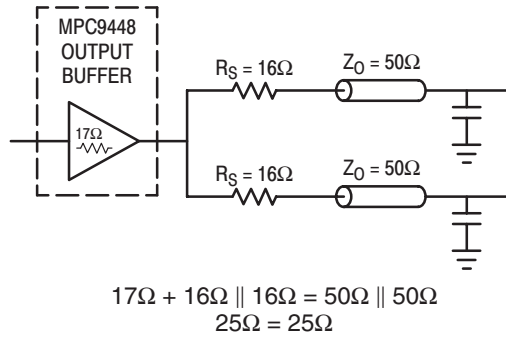


Figure 6. Optimized Dual Line Termination

Power Consumption of the MPC9448 and Thermal Management

The MPC9448 AC specification is guaranteed for the entire operating frequency range up to 350 MHz. The MPC9448 power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperature, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the MPC9448 die junction temperature and the associated device reliability. For a complete analysis of power consumption as a function of operating conditions and associated long term device reliability please refer to the application note AN1545. According to the AN1545, the long-term device reliability is a function of the die junction temperature:

$$P_{TOT} = \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_M C_L \right) \right] \cdot V_{CC} \quad \text{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_M C_L \right) \right] + \sum_P \left[DC_Q \cdot I_{OH} \cdot (V_{CC} - V_{OH}) + (1 - DC_Q) \cdot I_{OL} \cdot V_{OL} \right] \quad \text{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \quad \text{Equation 3}$$

$$f_{CLOCK,MAX} = \frac{1}{C_{PD} \cdot N \cdot V_{CC}^2} \cdot \left[\frac{T_{J,MAX} - T_A}{R_{thja}} - (I_{CCQ} \cdot V_{CC}) \right] \quad \text{Equation 4}$$

Table 9: Die junction temperature and MTBF

Junction temperature (°C)	MTBF (Years)
100	20.4
110	9.1
120	4.2
130	2.0

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the MPC9448 needs to be controlled and the thermal impedance of the board/package should be optimized. The power dissipated in the MPC9448 is represented in equation 1.

Where I_{CCQ} is the static current consumption of the MPC9448, C_{PD} is the power dissipation capacitance per output, $(M)\Sigma C_L$ represents the external capacitive output load, N is the number of active outputs (N is always 12 in case of the MPC9448). The MPC9448 supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore, ΣC_L is zero for controlled transmission line systems and can be eliminated from equation 1. Using parallel termination output termination results in equation 2 for power dissipation.

In equation 2, P stands for the number of outputs with a parallel or thevenin termination, V_{OL} , I_{OL} , V_{OH} and I_{OH} are a function of the output termination technique and DC_Q is the clock signal duty cycle. If transmission lines are used ΣC_L is zero in equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature T_J as a function of the power consumption.

Where R_{thja} is the thermal impedance of the package (junction to ambient) and T_A is the ambient temperature. According to Table 9, the junction temperature can be used to estimate the long-term device reliability. Further, combining equation 1 and equation 2 results in a maximum operating frequency for the MPC9448 in a series terminated transmission line system, equation 4.

$T_{J,MAX}$ should be selected according to the MTBF system requirements and Table 9. R_{thja} can be derived from Table 10. The R_{thja} represent data based on 1S2P boards, using 2S2P boards will result in a lower thermal impedance than indicated below.

Table 10: Thermal package impedance of the 32ld LQFP

Convection, LFPM	R_{thja} (1P2S board), °C/W	R_{thja} (2P2S board), °C/W
Still air	86	61
100 lfpm	76	56
200 lfpm	71	54
300 lfpm	68	53
400 lfpm	66	52
500 lfpm	60	49

If the calculated maximum frequency is below 350 MHz, it becomes the upper clock speed limit for the given application conditions. The following eight derating charts describe the safe frequency operation range for the MPC9448. The charts were calculated for a maximum tolerable die junction temperature of 110°C (120°C), corresponding to an estimated MTBF of 9.1 years (4 years), a supply voltage of 3.3V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made.

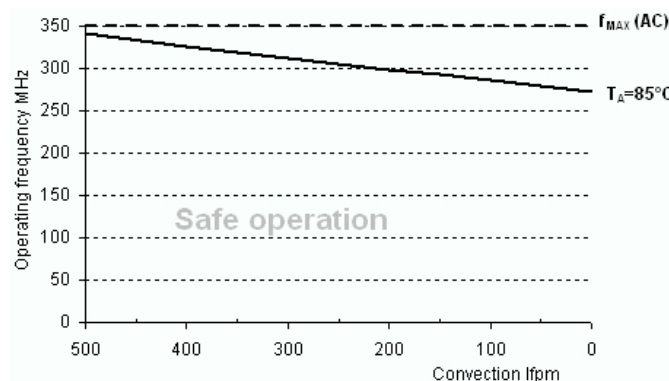


Figure 7. Maximum MPC9448 frequency, $V_{CC} = 3.3V$, MTBF 9.1 years, driving series terminated transmission lines, 2s2p board

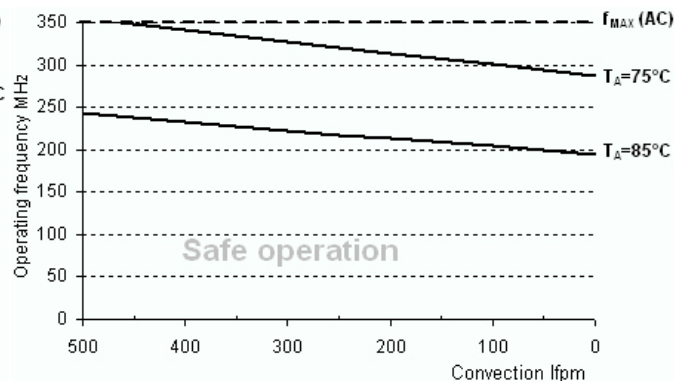


Figure 8. Maximum MPC9448 frequency, $V_{CC} = 3.3V$, MTBF 9.1 years, 4 pF load per line, 2s2p board



Figure 9. No maximum frequency limitation for $V_{CC} = 3.3V$, MTBF 4 years, driving series terminated transmission lines, 2s2p board



Figure 10. Maximum MPC9448 frequency, $V_{CC} = 3.3V$, MTBF 4 years, 4 pF load per line, 2s2p board

The Following Figures Illustrate the Measurement Reference for the MPC9448 Clock Driver Circuit

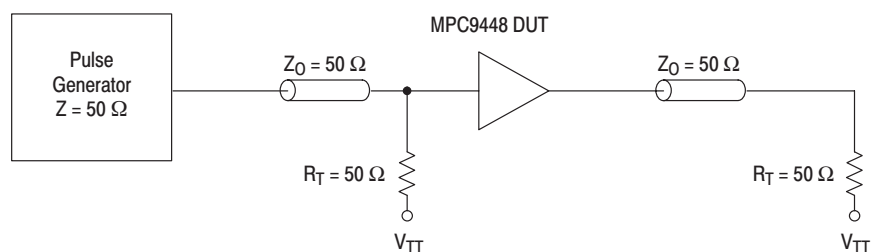


Figure 11. CCLK MPC9448 AC Test Reference for $V_{CC} = 3.3V$ and $V_{CC} = 2.5V$

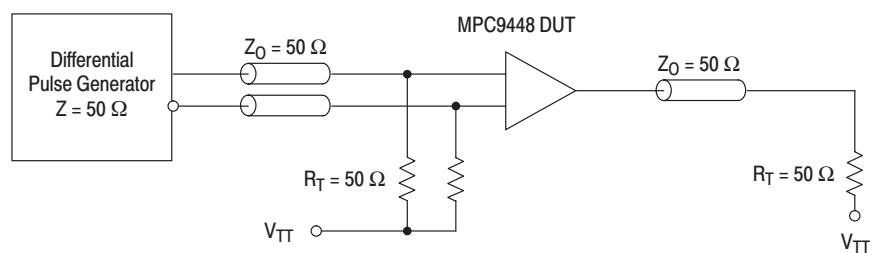
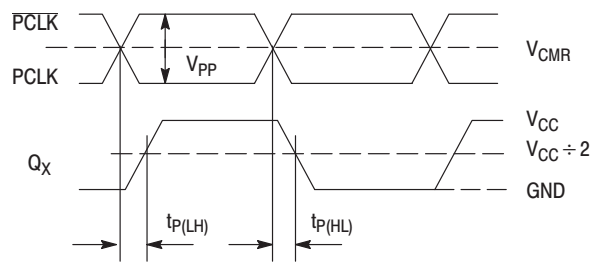
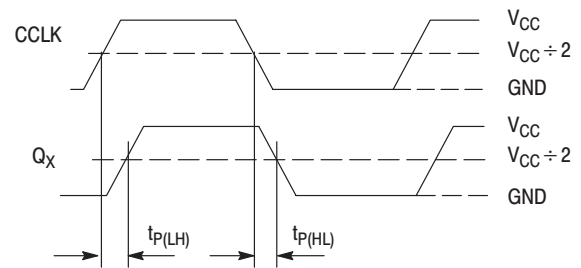
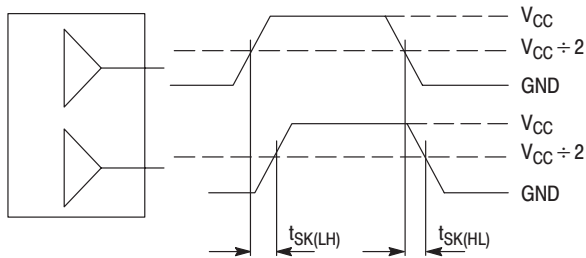
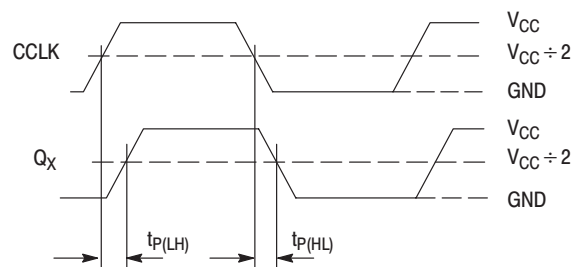


Figure 12. PCLK MPC9448 AC Test Reference

Figure 13. Propagation Delay (t_{PD}) Test ReferenceFigure 14. Propagation Delay (t_{PD}) Test Reference

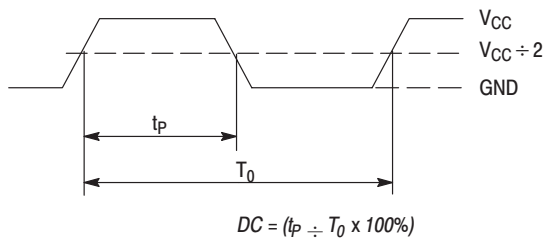
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 15. Output-to-Output Skew $t_{SK(LH, HL)}$ 

$$t_{SK(P)} = |t_{PLH} - t_{PHL}|$$

Figure 16. Output Pulse Skew ($t_{SK(P)}$) Test Reference

6



$$DC = (t_p \div T_0 \times 100\%)$$

The time from the output controlled edge to the non-controlled edge, divided by the time between output controlled edges, expressed as a percentage

Figure 17. Output Duty Cycle (DC)

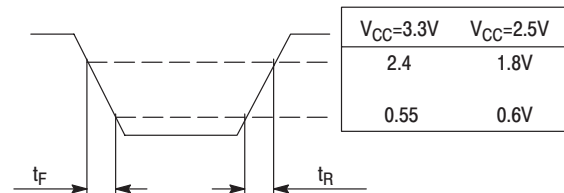
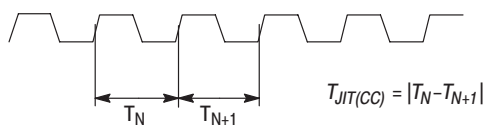
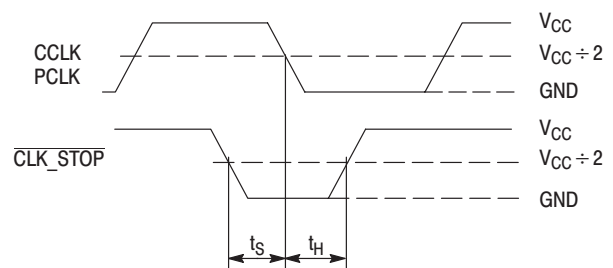


Figure 18. Output Transition Time Test Reference



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 19. Cycle-to-Cycle Jitter

Figure 20. Setup and Hold Time (t_S , t_H) Test Reference

3.3V/2.5V 1:15 PECL/LVCMOS Clock Fanout Buffer

The MPC9449 is a 3.3V or 2.5V compatible, 1:15 clock fanout buffer targeted for high performance clock tree applications. With output frequencies up to 200 MHz and output skews less than 200 ps the device meets the needs of the most demanding clock applications.

Features

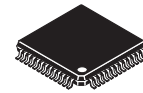
- 15 LVCMOS compatible clock outputs
- Two selectable LVCMOS and one differential LVPECL compatible clock inputs
- Selectable output frequency divider (divide-by-one and divide-by-two)
- Maximum clock frequency of 200 MHz
- Maximum clock skew of 200 ps
- High-impedance output control
- 3.3V or 2.5V power supply
- Drives up to 30 series terminated clock lines
- Ambient temperature range -40°C to $+85^{\circ}\text{C}$
- 52 lead LQFP packaging
- Supports clock distribution in networking, telecommunication and computing applications
- Pin and function compatible to MPC949

Functional Description

The MPC9449 is specifically designed to distribute LVCMOS compatible clock signals up to a frequency of 200 MHz. The device has 15 identical outputs, organized in 4 output banks. Each output bank provides a retimed or frequency divided copy of the input signal with a near zero skew. The output buffer supports driving of 50Ω terminated transmission lines on the incident edge: each output is capable of driving either one parallel terminated or two series terminated transmission lines.

Two selectable LVCMOS compatible clock inputs are available. This feature supports redundant differential clock sources. In addition, the MPC9449 accepts one differential PECL clock signal. The DSELx pins choose between division of the input reference frequency by one or two. The frequency divider can be set individually for each of the four output banks. Applying the OE control will force the outputs into high-impedance mode.

All inputs have an internal pull-up or pull-down resistor preventing unused and open inputs from floating. The device supports a 2.5V or 3.3V power supply and an ambient temperature range of -40°C to $+85^{\circ}\text{C}$. The MPC9449 is pin and function compatible but performance-enhanced to the MPC949. The device is packaged in a 52-lead LQFP package.

MPC9449**3.3V/2.5V 1:15
PECL/LVCMOS
CLOCK FANOUT BUFFER****FA SUFFIX**
52 LEAD LQFP PACKAGE
CASE 848D**6**

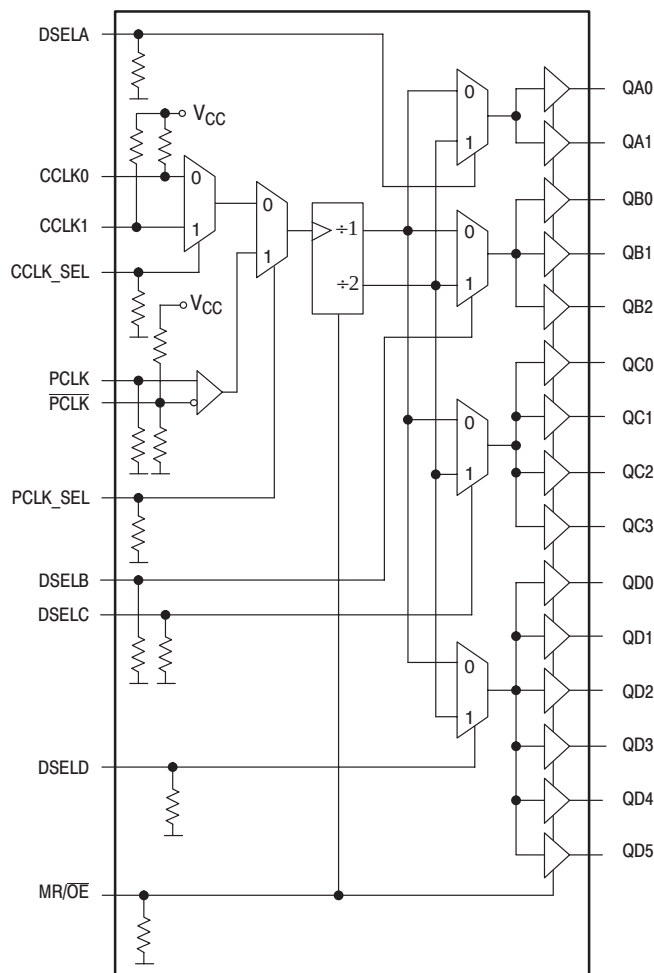


Figure 1. MPC9449 Logic Diagram

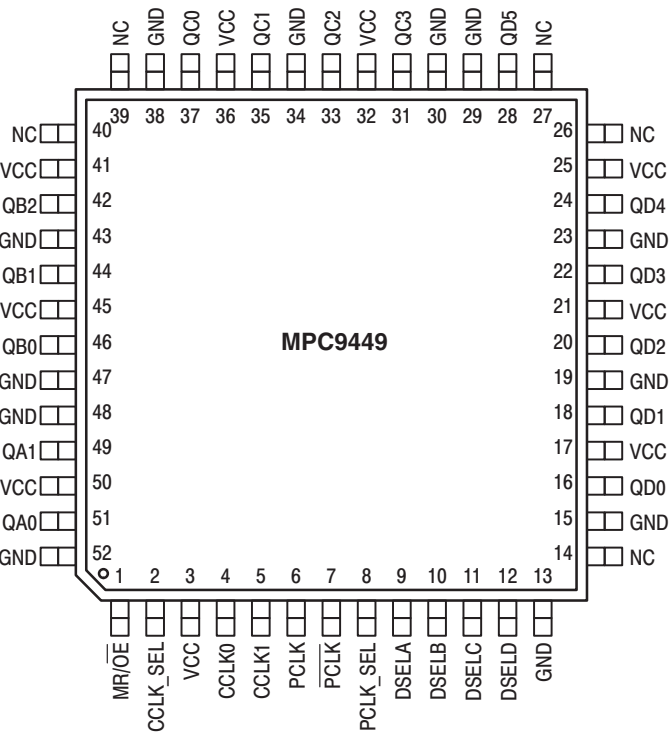


Figure 2. MPC9449 52-Lead Package Pinout (Top View)

Table 1: FUNCTION TABLE

Control	Default	0	1
PCLK_SEL	0	LVC MOS clock input selected (CCLK0 or CCLK1)	PCLK differential input selected
CCLK_SEL	0	CCLK0 selected	CCLK1 selected
DSELA, DSELB, DSELC, DSELD	0 0 0 0	+1	+2
MR/OE	1	Outputs enabled	Outputs disabled (high impedance)

Table 2: PIN CONFIGURATION

Pin	I/O	Type	Function
PCLK, PCLK	Input	LVPECL	Differential LVPECL clock input
CCLK0, CCLK1	Input	LVC MOS	LVC MOS clock inputs
PCLK_SEL	Input	LVC MOS	LVPECL clock input select
CCLK_SEL	Input	LVC MOS	LVC MOS clock input select
DSELA, DSELB, DSELC, DSELD	Input	LVC MOS	Clock divider selection
MR/OE	Input	LVC MOS	Output enable/disable (high-impedance tristate)
QA0-1, QB0-2, QC0-3, QD0-5	Output	LVC MOS	Clock outputs
GND	Supply	Ground	Negative power supply (GND)
VCC	Supply	VCC	Positive power supply for I/O and core. All VCC pins must be connected to the positive power supply for correct operation

Table 3: GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		12		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 4: ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.8	V	
V_{IN}	DC Input Voltage	-0.3	$V_{CC}+0.3$	V	
V_{OUT}	DC Output Voltage	-0.3	$V_{CC}+0.3$	V	
I_{IN}	DC Input Current		± 20	mA	
I_{OUT}	DC Output Current		± 50	mA	
T_S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5: DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	2.0		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input low voltage			0.8	V	LVC MOS
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -24 \text{ mA}^a$
V_{PP}	Peak-to-peak input voltage PCLK, $\overline{\text{PCLK}}$	250			mV	LVPECL
V_{CMR}^b	Common Mode Range PCLK, $\overline{\text{PCLK}}$	1.0		$V_{CC} - 0.6$	V	LVPECL
V_{OL}	Output Low Voltage			0.55 0.30	V V	$I_{OL} = 24 \text{ mA}$ $I_{OL} = 12 \text{ mA}$
Z_{OUT}	Output impedance		14 - 17		Ω	
I_{IN}	Input Current			± 200	μA	$V_{IN} = V_{CC}$ or GND
I_{CCQ}	Maximum Quiescent Supply Current			10	mA	All V_{CC} Pins

- a The MPC9449 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines.
- b V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.

Table 6: AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{PP}	Peak-to-peak input voltage PCLK, $\overline{\text{PCLK}}$	400		1000	mV	LVPECL
V_{CMR}^c	Common Mode Range PCLK, $\overline{\text{PCLK}}$	1.0		$V_{CC} - 0.6$	V	LVPECL
f_{max}	Output frequency	0		200	MHz	
f_{ref}	Input Frequency	0		200	MHz	
$t_{P, REF}$	Reference Input Pulse Width	1.5			ns	
t_r, t_f	CCLK0, CCLK1 Input Rise/Fall Time			1.0	ns	0.8 to 2.0V
$t_{sk(O)}$	Output-to-output Skew Qa outputs Qb outputs Qc outputs Qd outputs same frequency different frequencies All outputs All outputs			50 50 50 100 200 300	ps ps ps ps ps ps	
$t_{sk(PP)}$	Device-to-device Skew		2.5		ns	
$t_{sk(P)}$	Output Pulse Skew			250	ps	$DC_{REF} = 50\%$
$t_{PLH, HL}$	Propagation delay CCLK0 or CCLK1 to any Q PCLK to any Q	1.0 1.0	3.0 3.0	5.0 5.0	ns ns	
$t_{PLZ, HZ}$	Output Disable Time OE to any Q			11	ns	
$t_{PZL, LZ}$	Output Enable Time OE to any Q			11	ns	
t_r, t_f	Output Rise/Fall Time ^c	0.1		1.0	ns	0.55 to 2.4V
$t_{JIT(CC)}$	Cycle-to-cycle jitter RMS (1 σ)		TBD		ps	

- a AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
- b V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts propagation delay.
- c An input rise/fall time greater than that specified may be used, but AC characteristics are not guaranteed under such a condition.

Table 7: DC CHARACTERISTICS ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	1.7		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input low voltage	-0.3		0.7	V	LVC MOS
V_{PP}	Peak-to-peak input voltage PCLK, PCLK	250			mV	LVPECL
V_{CMR}^a	Common Mode Range PCLK, PCLK	1.0		$V_{CC}-0.6$	V	LVPECL
V_{OH}	Output High Voltage	1.8			V	$I_{OH} = -15\text{ mA}^b$
V_{OL}	Output Low Voltage			0.6	V	$I_{OL} = 15\text{ mA}$
Z_{OUT}	Output impedance		17 - 20		Ω	
I_{IN}	Input Current ^c			± 200	μA	$V_{IN} = V_{CC}$ or GND
I_{CC}	Maximum Quiescent Supply Current			10	mA	All V_{CC} Pins

a V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.

b The MPC9449 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} .

c Inputs have pull-down or pull-up resistors affecting the input current.

Table 8: AC CHARACTERISTICS ($V_{CC} = 2.5V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{PP}	Peak-to-peak input voltage PCLK, PCLK	400		1000	mV	LVPECL
V_{CMR}^b	Common Mode Range PCLK, PCLK	1.2		$V_{CC}-0.6$	V	LVPECL
f_{max}	Output frequency	0		200	MHz	
f_{ref}	Input Frequency	0		200	MHz	
$t_{P, REF}$	Reference Input Pulse Width	1.5			ns	
t_r, t_f	CCLK Input Rise/Fall Time			1.0	ns	0.7 to 1.7V
$t_{sk(O)}$	Output-to-output Skew Qa outputs Qb outputs Qc outputs Qd outputs same frequency different frequencies All outputs			50 50 50 100 200 300	ps ps ps ps ps ps	
$t_{sk(PP)}$	Device-to-device Skew		5.0		ns	
$t_{SK(P)}$	Output Pulse Skew			350	ps	$DC_{REF} = 50\%$
$t_{PLH, HL}$	Propagation delay CCLK0 or CCLK1 to any Q PCLK to any Q	1.0 1.0	3.5 3.5	7.0 7.0	ns ns	
$t_{PLZ, HZ}$	Output Disable Time OE to any Q			11	ns	
$t_{PZL, LZ}$	Output Enable Time OE to any Q			11	ns	
t_r, t_f	Output Rise/Fall Time ^c	0.1		1.0	ns	0.6 to 1.8V
$t_{JIT(CC)}$	Cycle-to-cycle jitter RMS (1 σ)		TBD		ps	

a AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts propagation delay.

c An input rise/fall time greater than that specified may be used, but AC characteristics are not guaranteed under such a condition.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC9449 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}+2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9449 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9449 clock driver is effectively doubled due to its capability to drive multiple lines.

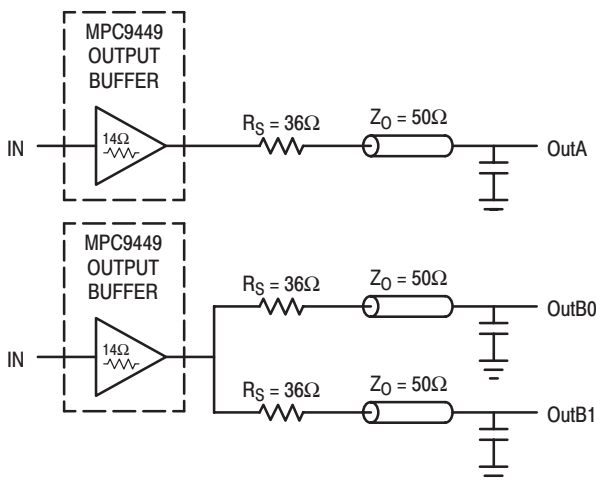


Figure 3. Single versus Dual Transmission Lines

The waveform plots in Figure 4 "Single versus Dual Line Termination Waveforms" show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9449 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9449. The output waveform in Figure 4 "Single versus Dual Line Termination Waveforms" shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the

parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$

$$Z_0 = 50\Omega \parallel 50\Omega$$

$$R_S = 36\Omega \parallel 36\Omega$$

$$R_0 = 14\Omega$$

$$V_L = 3.0 (25 \div (18 + 17 + 25))$$

$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

1. Final skew data pending specification.

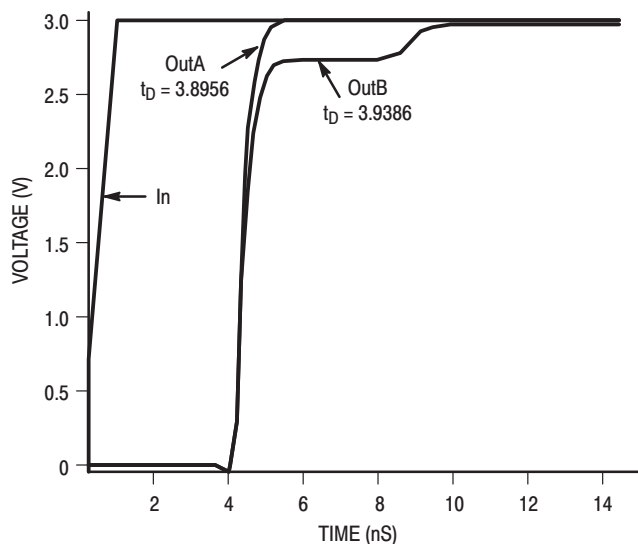


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 "Optimized Dual Line Termination" should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

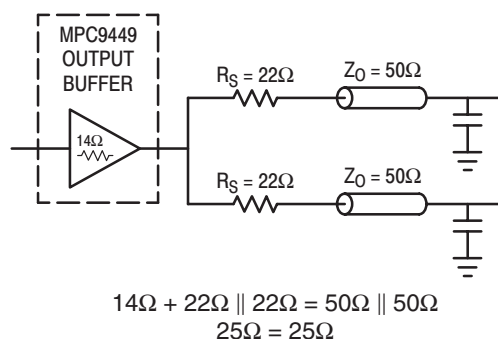


Figure 5. Optimized Dual Line Termination

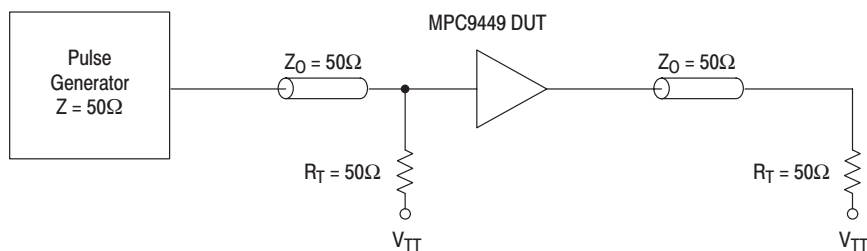


Figure 6. CCLK MPC9449 AC test reference for $V_{CC} = 3.3V$ and $V_{CC} = 2.5V$

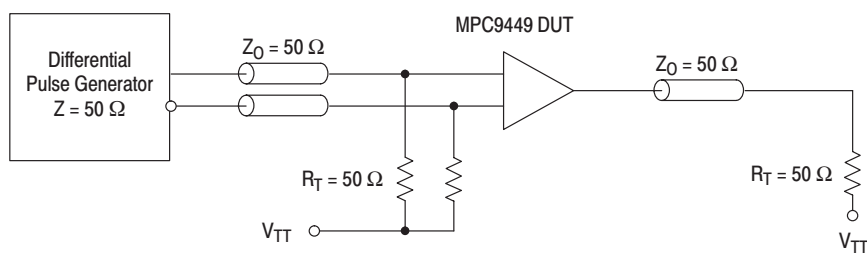
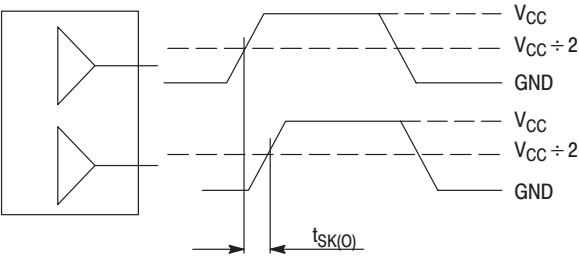


Figure 7. PCLK MPC9449 AC test reference



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 8. Output-to-output Skew $t_{SK(O)}$

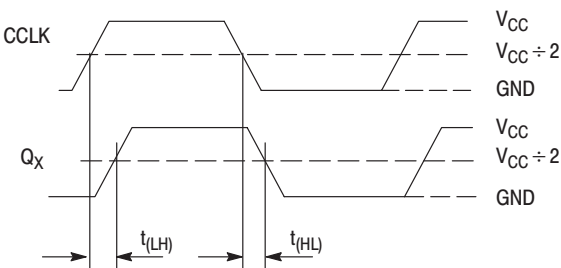


Figure 9. Propagation delay (t_{PD}) test reference

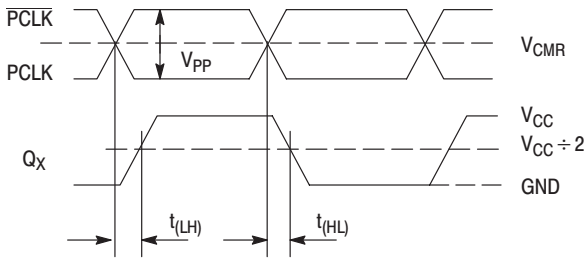
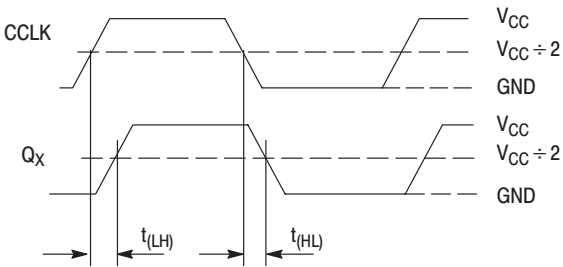


Figure 10. Propagation delay (t_{PD}) test reference



$$t_{SK(P)} = |t_{PLH} - t_{PHL}|$$

Figure 11. Output Pulse Skew $t_{SK(P)}$ test reference

6

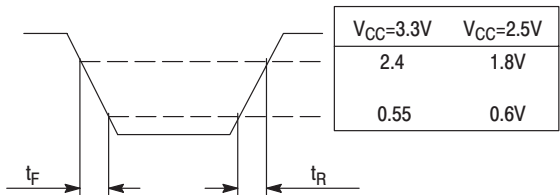
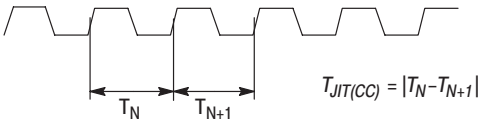


Figure 12. Output Transition Time Test Reference



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 13. Cycle-to-cycle Jitter

2.5V and 3.3V LVC MOS Clock Fanout Buffer

The MPC9456 is a 2.5V and 3.3V compatible 1:10 clock distribution buffer designed for low-voltage mid-range to high-performance telecom, networking and computing applications. Both 3.3V, 2.5V and dual supply voltages are supported for mixed-voltage applications. The MPC9456 offers 10 low-skew outputs and a differential LVPECL clock input. The outputs are configurable and support 1:1 and 1:2 output to input frequency ratios. The MPC9456 is specified for the extended temperature range of -40 to 85°C.

Features

- Configurable 10 outputs LVC MOS clock distribution buffer
- Compatible to single, dual and mixed 3.3V/2.5V voltage supply
- Wide range output clock frequency up to 250 MHz
- Designed for mid-range to high-performance telecom, networking and computer applications
- Supports high-performance differential clocking applications
- Max. output skew of 200 ps (150 ps within one bank)
- Selectable output configurations per output bank
- Tristable outputs
- 32 ld LQFP package
- Ambient operating temperature range of -40 to 85°C

Functional Description

The MPC9456 is a full static design supporting clock frequencies up to 250 MHz. The signals are generated and retimed on-chip to ensure minimal skew between the three output banks.

Each of the three output banks can be individually supplied by 2.5V or 3.3V supporting mixed voltage applications. The FSELx pins choose between division of the input reference frequency by one or two. The frequency divider can be set individually for each of the three output banks. The MPC9456 can be reset and the outputs are disabled by deasserting the MR/ $\overline{OE}$ pin (logic high state). Asserting MR/ $\overline{OE}$ will enable the outputs.

All control inputs accept LVC MOS signals while the outputs provide LVC MOS compatible levels with the capability to drive terminated 50 Ω transmission lines. The clock input is low voltage PECL compatible for differential clock distribution support. Please consult the MPC9446 specification for a full CMOS compatible device. For series terminated transmission lines, each of the MPC9456 outputs can drive one or two traces giving the devices an effective fanout of 1:20. The device is packaged in a 7x7 mm² 32-lead LQFP package.

MPC9456**LOW VOLTAGE SINGLE OR
DUAL SUPPLY 2.5V AND 3.3V
LVC MOS CLOCK
DISTRIBUTION BUFFER****FA SUFFIX**
LQFP PACKAGE
CASE 873A

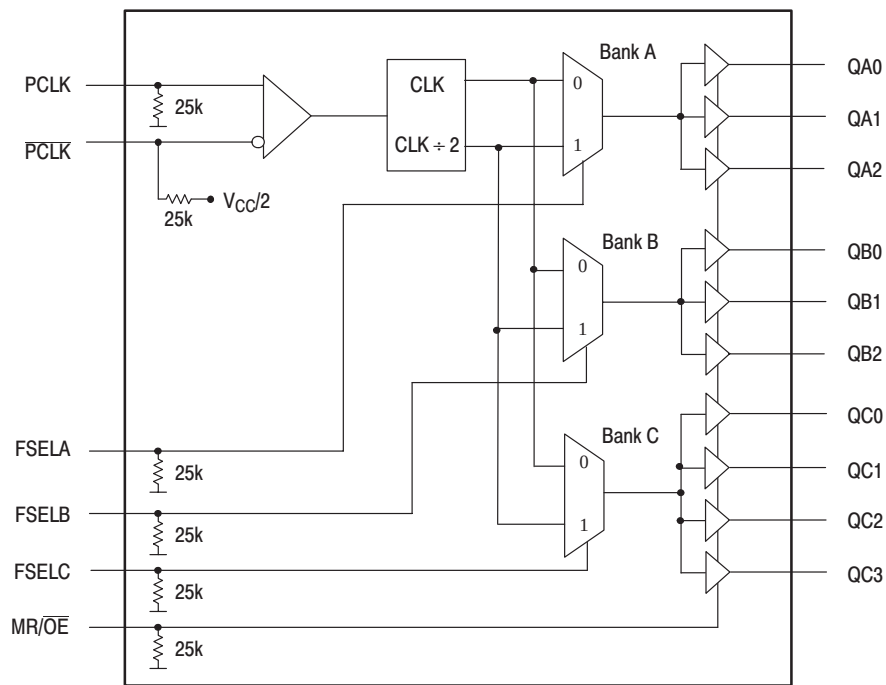


Figure 1. MPC9456 Logic Diagram

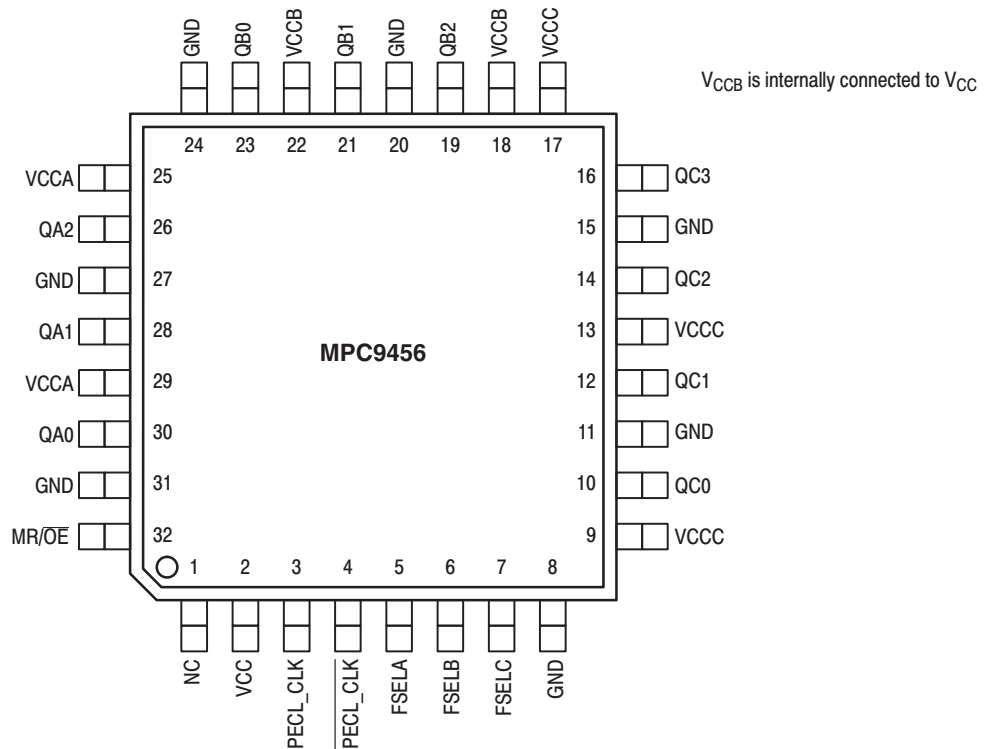


Figure 2. Pinout: 32-Lead Package Pinout (Top View)

Table 1: Pin Configuration

Pin	I/O	Type	Function
PECL_CLK, PECL_CLK	Input	LVPECL	Differential clock reference Low voltage positive ECL input
FSEL _A , FSEL _B , FSEL _C	Input	LVC MOS	Output bank divide select input
MR/ $\overline{OE}$	Input	LVC MOS	Internal reset and output tristate control
GND		Supply	Negative voltage supply output bank (GND)
V _{CCA} , V _{CCB} [*] , V _{CCC}		Supply	Positive voltage supply for output banks
V _{CC}		Supply	Positive voltage supply core (VCC)
QA0 - QA2	Output	LVC MOS	Bank A outputs
QB0 - QB2	Output	LVC MOS	Bank B outputs
QC0 - QC3	Output	LVC MOS	Bank C outputs

* V_{CCB} is internally connected to V_{CC}.

Table 2: Supported Single and Dual Supply Configurations

Supply voltage configuration	V _{CC} ^a	V _{CCA} ^b	V _{CCB} ^c	V _{CCC} ^d	GND
3.3V	3.3V	3.3V	3.3V	3.3V	0V
Mixed voltage supply	3.3V	3.3V or 2.5V	3.3V	3.3V or 2.5V	0 V
2.5V	2.5V	2.5V	2.5V	2.5V	0 V

a. V_{CC} is the positive power supply of the device core and input circuitry. V_{CC} voltage defines the input threshold and levels

b. V_{CCA} is the positive power supply of the bank A outputs. V_{CCA} voltage defines bank A output levels

c. V_{CCB} is the positive power supply of the bank B outputs. V_{CCB} voltage defines bank B output levels. V_{CCB} is internally connected to V_{CC}.

d. V_{CCC} is the positive power supply of the bank C outputs. V_{CCC} voltage defines bank C output levels

Table 3: Function Table (Controls)

Control	Default	0	1
FSELA	0	f _{QA0:2} = f _{REF}	f _{QA0:2} = f _{REF} ÷ 2
FSELB	0	f _{QB0:2} = f _{REF}	f _{QB0:2} = f _{REF} ÷ 2
FSELC	0	f _{QC0:3} = f _{REF}	f _{QC0:3} = f _{REF} ÷ 2
MR/ $\overline{OE}$	0	Outputs enabled	Internal reset Outputs disabled (tristate)

Table 4: Absolute Maximum Ratings^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	4.6	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} +0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} +0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage temperature	-40	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 5: General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output Termination Voltage		V _{CC} ÷ 2		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C _{PD}	Power Dissipation Capacitance		10		pF	Per output
C _{IN}	Input Capacitance		4.0		pF	

Table 6: DC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 3.3V \pm 5\%$, $T_A = -40$ to $+85^\circ\text{C}$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	2.0		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input low voltage	-0.3		0.8	V	LVC MOS
V_{PP}	Peak-to-peak input voltage	PCLK	250		mV	LVPECL
$V_{CMR\Delta}$	Common Mode Range	PCLK	1.1	$V_{CC}-0.6$	V	LVPECL
I_{IN}	Input current ^b			200	μA	$V_{IN}=\text{GND}$ or $V_{IN}=V_{CC}$
V_{OH}	Output High Voltage	2.4			V	$I_{OH}=-24\text{ mA}^c$
V_{OL}	Output Low Voltage			0.55 0.30	V V	$I_{OL}=24\text{ mA}^b$ $I_{OL}=12\text{ mA}$
Z_{OUT}	Output impedance		14 - 17		Ω	
I_{CCQ}^d	Maximum Quiescent Supply Current			2.0	mA	All V_{CC} Pins

- a. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
- b. Input pull-up / pull-down resistors influence input current.
- c. The MPC9456 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50Ω series terminated transmission lines.
- d. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 7: AC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 3.3V \pm 5\%$, $T_A = -40$ to $+85^\circ\text{C}$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	0		250 ^b	MHz	
f_{MAX}	Maximum Output Frequency	+1 output +2 output	0 0	250 ^b 125	MHz MHz	$FSELx=0$ $FSELx=1$
V_{PP}	Peak-to-peak input voltage	PCLK	500	1000	mV	LVPECL
$V_{CMR\Delta}$	Common Mode Range	PCLK	1.3	$V_{CC}-0.8$	V	LVPECL
$t_{P, REF}$	Reference Input Pulse Width	1.4			ns	
t_r, t_f	PCLK Input Rise/Fall Time			1.0 ^d	ns	0.8 to 2.0V
t_{PLH} t_{PHL}	Propagation delay	CCLK to any Q CCLK to any Q	2.2 2.2	4.45 4.2	ns ns	
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
$t_{sk(O)}$	Output-to-output Skew	Within one bank Any output bank, same output divider Any output, Any output divider		150 200 350	ps ps ps	
$t_{sk(PP)}$	Device-to-device Skew			2.25	ns	
$t_{SK(P)}$	Output pulse skew ^e			200	ps	
DC_Q	Output Duty Cycle	+1 output +2 output	47 45	53 55	% %	$DC_{REF} = 50\%$ $DC_{REF} = 25\%-75\%$
t_r, t_f	Output Rise/Fall Time		0.1	1.0	ns	0.55 to 2.4V

- a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
- b. The MPC9456 is functional up to an input and output clock frequency of 350 MHz and is characterized up to 250 MHz.
- c. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification.
- d. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
- e. Output pulse skew is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.

Table 8: DC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 2.5V \pm 5\%$, $T_A = -40$ to $+85^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	1.7		$V_{CC} + 0.3$	V	LVC MOS
V_{IL}	Input low voltage	-0.3		0.7	V	LVC MOS
V_{PP}	Peak-to-peak input voltage PCLK	250			mV	LVPECL
V_{CMRA}	Common Mode Range PCLK	1.1		$V_{CC}-0.7$	V	LVPECL
V_{OH}	Output High Voltage	1.8			V	$I_{OH} = -15\text{ mA}^b$
V_{OL}	Output Low Voltage			0.6	V	$I_{OL} = 15\text{ mA}$
Z_{OUT}	Output impedance		17 - 20 ^b		Ω	
I_{IN}	Input current ^c			± 200	μA	$V_{IN} = GND$ or $V_{IN} = V_{CC}$
I_{CCQd}	Maximum Quiescent Supply Current			2.0	mA	All V_{CC} Pins

- a. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
- b. The MPC9456 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT} . Alternatively, the device drives up to two 50 Ω series terminated transmission lines per output.
- c. Input pull-up / pull-down resistors influence input current.
- d. ICCQ is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 9: AC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 2.5V \pm 5\%$, $T_A = -40$ to $+85^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	0		250 ^b	MHz	
f_{MAX}	Maximum Output Frequency +1 output +2 output	0 0		250 ^b 125	MHz MHz	FSELx=0 FSELx=1
V_{PP}	Peak-to-peak input voltage PCLK	500		1000	mV	LVPECL
V_{CMRC}	Common Mode Range PCLK	1.1		$V_{CC}-0.7$	V	LVPECL
$t_{P, REF}$	Reference Input Pulse Width	1.4			ns	
t_r, t_f	PCLK Input Rise/Fall Time			1.0 ^d	ns	0.7 to 1.7V
t_{PLH} t_{PHL}	Propagation delay PCLK to any Q PCLK to any Q	2.6 2.6		5.6 5.5	ns ns	
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
$t_{sk(O)}$	Output-to-output Skew Within one bank Any output bank, same output divider Any output, Any output divider			150 200 350	ps ps ps	
$t_{sk(PP)}$	Device-to-device Skew			3.0	ns	
$t_{SK(P)}$	Output pulse skew ^e			200	ps	
DC_Q	Output Duty Cycle +1 or +2 output	45	50	55	%	$DC_{REF} = 50\%$
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.6 to 1.8V

- a. AC characteristics apply for parallel output termination of 50 Ω to V_{TT} .
- b. The MPC9456 is functional up to an input and output clock frequency of 350 MHz and is characterized up to 250 MHz.
- c. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification.
- d. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
- e. Output pulse skew is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.

Table 10: AC Characteristics ($V_{CC} = 3.3V \pm 5\%$, $V_{CCA} = V_{CCB} = V_{CCC} = 2.5V \pm 5\%$ or $3.3V \pm 5\%$, $T_A = -40$ to $+85^\circ\text{C}$)^{a b}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
$t_{sk(O)}$	Output-to-output Skew Within one bank Any output bank, same output divider Any output, Any output divider			150 250 350	ps ps ps	
$t_{sk(PP)}$	Device-to-device Skew			2.5	ns	
$t_{PLH,HL}$	Propagation delay PCLK to any Q	See 3.3V table				
$t_{SK(P)}$	Output pulse skew ^c			250	ps	
DC_Q	Output Duty Cycle +1 or +2 output	45	50	55	%	$DC_{REF} = 50\%$

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b. For all other AC specifications, refer to 2.5V or 3.3V tables according to the supply voltage of the output bank.

c. Output pulse skew is the absolute difference of the propagation delay times: $|t_{pLH} - t_{pHL}|$.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC9456 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}+2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9456 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9456 clock driver is effectively doubled due to its capability to drive multiple lines.

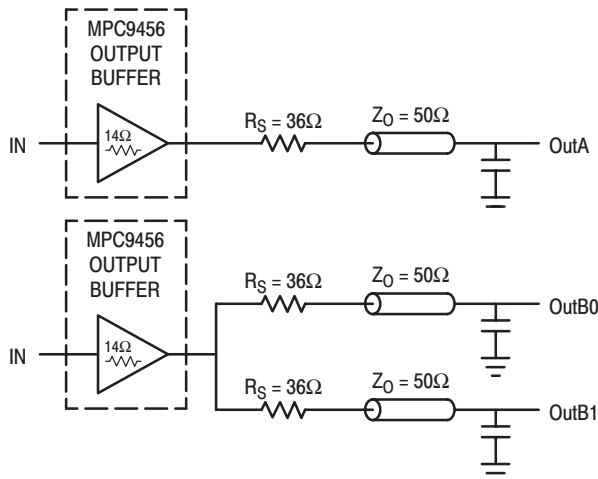


Figure 3. Single versus Dual Transmission Lines

The waveform plots in Figure 4 "Single versus Dual Line Termination Waveforms" show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9456 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9456. The output waveform in Figure 4 "Single versus Dual Line Termination Waveforms" shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω se-

ries resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$\begin{aligned} V_L &= V_S (Z_0 \div (R_S + R_0 + Z_0)) \\ Z_0 &= 50\Omega \parallel 50\Omega \\ R_S &= 36\Omega \parallel 36\Omega \\ R_0 &= 14\Omega \\ V_L &= 3.0 (25 \div (18 + 14 + 25)) \\ &= 1.31V \end{aligned}$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

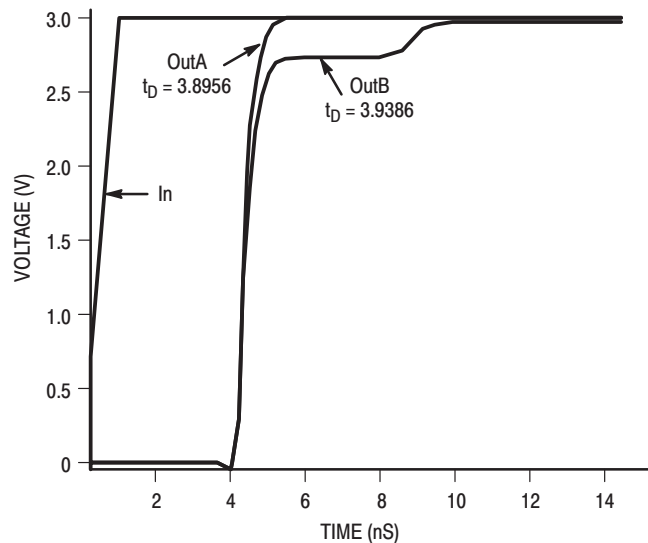


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 "Optimized Dual Line Termination" should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

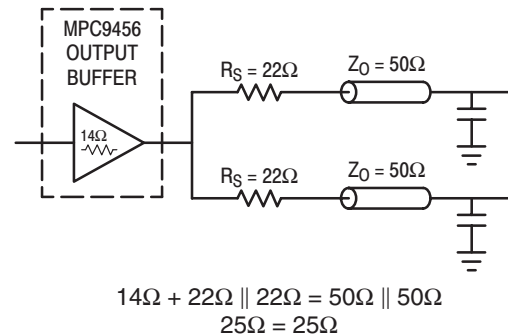


Figure 5. Optimized Dual Line Termination

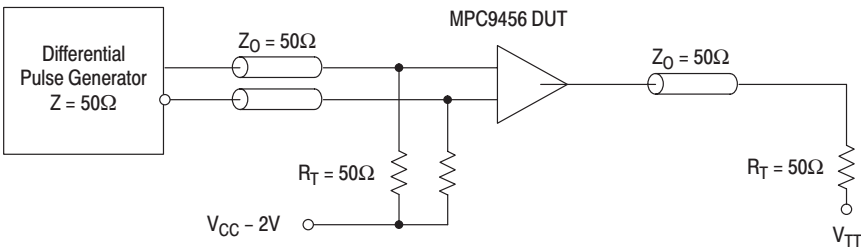


Figure 6. PCLK MPC9456 AC test reference for $V_{CC} = 3.3V$ and $V_{CC} = 2.5V$

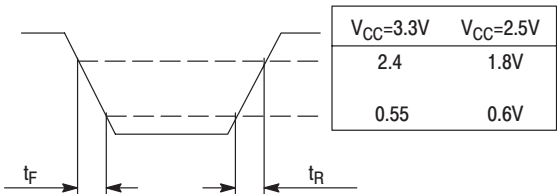


Figure 7. Output Transition Time Test Reference

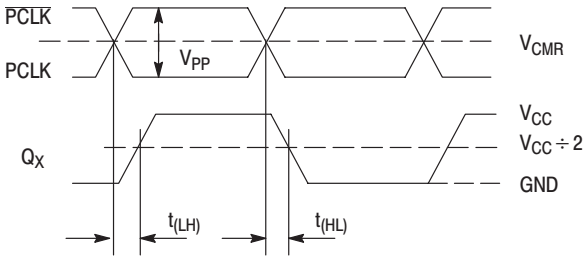
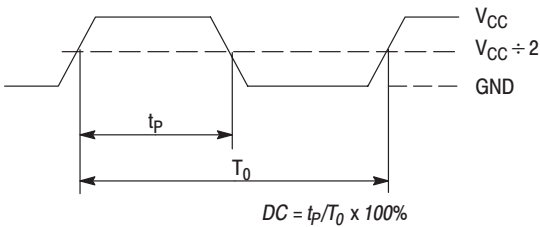
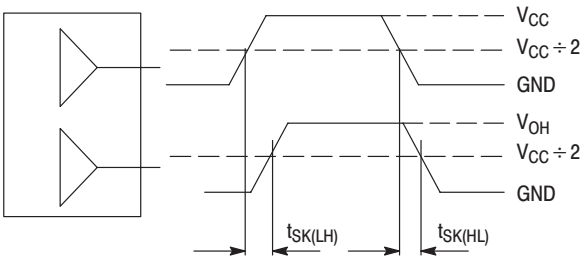


Figure 8. Propagation delay (t_{pD}) test reference



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 9. Output Duty Cycle (DC)



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 10. Output-to-output Skew $t_{SK(O)}$

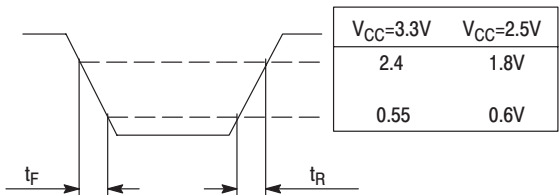


Figure 11. Output Transition Time test reference

Low Voltage 1:10 CMOS Clock Driver

The MPC946 is a low voltage CMOS, 1:10 clock buffer. The 10 outputs can be configured into a standard fanout buffer or into 1X and 1/2X combinations. The ten outputs were designed and optimized to drive 50Ω series or parallel terminated transmission lines. With output to output skews of 350ps the MPC946 is an ideal clock distribution chip for synchronous systems which need a tight level of skew from a large number of outputs. For a similar product with more outputs consult the MPC949 data sheet.

- 2 Selectable LVCMOS/LVTTL Clock Inputs
- 350ps Output to Output Skew
- Drives up to 20 Series Terminated Independent Clock Lines
- Maximum Input/Output Frequency of 150MHz
- Tristatable Outputs
- 32-Lead LQFP Packaging
- 3.3V VCC Supply

With an output impedance of approximately 7Ω, in both the HIGH and the LOW logic states, the output buffers of the MPC946 are ideal for driving series terminated transmission lines. More specifically each of the 10 MPC946 outputs can drive two series terminated transmission lines. With this capability, the MPC946 has an effective fanout of 1:20 in applications using point-to-point distribution schemes.

The MPC946 has the capability of generating 1X and 1/2X signals from a 1X source. The design is fully static, the signals are generated and retimed inside the chip to ensure minimal skew between the 1X and 1/2X signals. The device features selectability to allow the user to select the ratio of 1X outputs to 1/2X outputs.

Two independent LVCMOS/LVTTL compatible clock inputs are available. Designers can take advantage of this feature to provide redundant clock sources or the addition of a test clock into the system design. With the TCLK_Sel input pulled HIGH the TCLK1 input is selected.

All of the control inputs are LVCMOS/LVTTL compatible. The Dsel pins choose between 1X and 1/2X outputs. A LOW on the Dsel pins will select the 1X output. The MR/Tristate input will reset the internal flip flops and tristate the outputs when it is forced HIGH.

The MPC946 is fully 3.3V compatible. The 32-lead LQFP package was chosen to optimize performance, board space and cost of the device. The 32-lead LQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

MPC946

See Upgrade Product – MPC9446

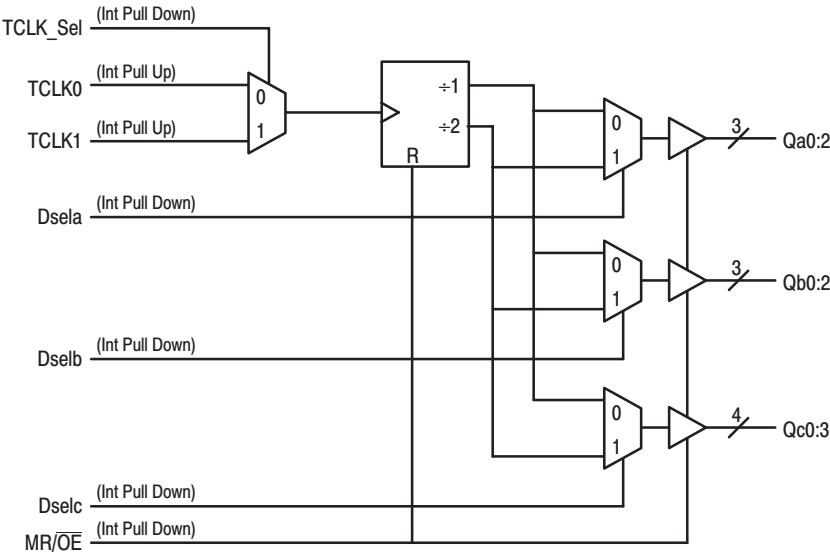
LOW VOLTAGE 1:10 CMOS CLOCK DRIVER



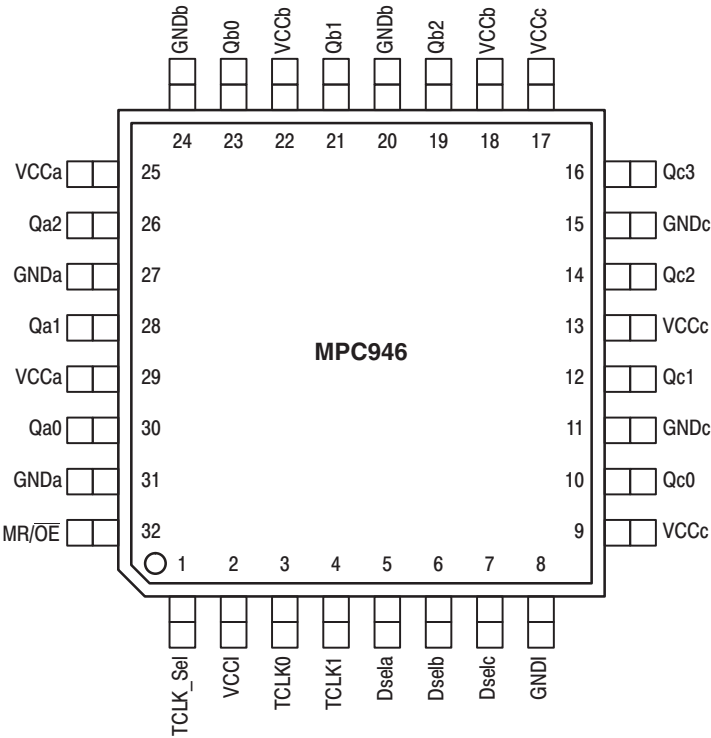
FA SUFFIX
LQFP PACKAGE
CASE 873A

6

LOGIC DIAGRAM



Pinout: 32-Lead TQFP (Top View)



FUNCTION TABLES

TCLK_Sel	Input
0	TCLK0
1	TCLK1

Dselx	Outputs
0	1x
1	1/2x

MR/OE	Outputs
0	Enabled
1	Hi-Z

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	4.6	V
V_I	Input Voltage	-0.3	$V_{DD} + 0.3$	V
I_{IN}	Input Current (CMOS Inputs)		± 20	mA
T_{Stor}	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		3.6	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.5			V	$I_{OH} = -20\text{mA}^1$
V_{OL}	Output LOW Voltage			0.4	V	$I_{OL} = 20\text{mA}^1$
I_{IN}	Input Current			± 120	μA	Note 2.
I_{CC}	Maximum Quiescent Supply Current		70	85	mA	
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	Per Output

- The MPC946 can drive 50Ω transmission lines on the incident edge. Each output can drive one 50Ω parallel terminated transmission line to the termination voltage of $V_{TT} = V_{CC}/2$. Alternately, the device drives up to two 50Ω series terminated transmission lines.
- I_{IN} current is a result of internal pull-up/pull-down resistors.

AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency	150			MHz	Note 1.
t_{PLH} , t_{PHL}	Propagation Delay TCLK to Q	5.0 4.5	8.0 7.5	12.0 11.5	ns	Note 1., 3.
$t_{sk(o)}$	Output-to-Output Skew Same Frequency Outputs Different Frequency Outputs Same Frequency Outputs Different Frequency Outputs			350 350 350 450	ps	Note 1., 3. $F_{max} < 100\text{MHz}$ $F_{max} < 100\text{MHz}$ $F_{max} > 100\text{MHz}$ $F_{max} > 100\text{MHz}$
$t_{sk(pp)}$	Part-to-Part Skew		2.0	4.5	ns	Note 2.
t_{PZL} , t_{PZH}	Output Enable Time		3	11	ns	Note 3.
t_{PLZ} , t_{PHZ}	Output Disable Time		3	11	ns	Note 3.
t_r , t_f	Output Rise/Fall Time	0.1	0.5	1.0	ns	0.8V to 2.0V, Note 3.

- Driving 50Ω transmission lines.
- Part-to-part skew at a given temperature and voltage.
- Termination is 50Ω to $V_{CC}/2$.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC946 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $VCC/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC946 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 1 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fan-out of the MPC946 clock driver is effectively doubled due to its capability to drive multiple lines.

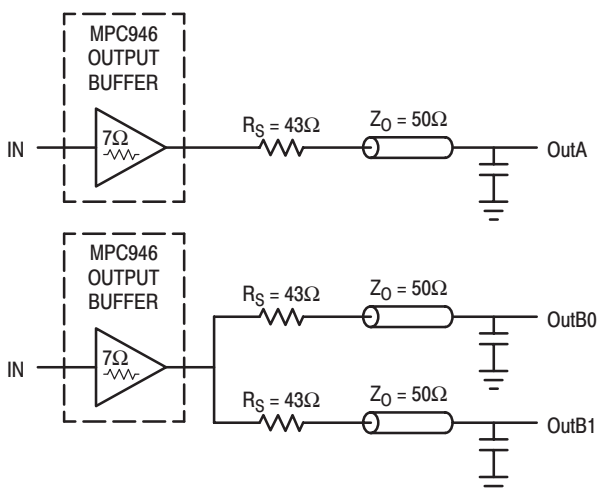


Figure 1. Single versus Dual Transmission Lines

The waveform plots of Figure 2 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC946 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC946. The output waveform in Figure 2 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_o / R_s + R_o + Z_o) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

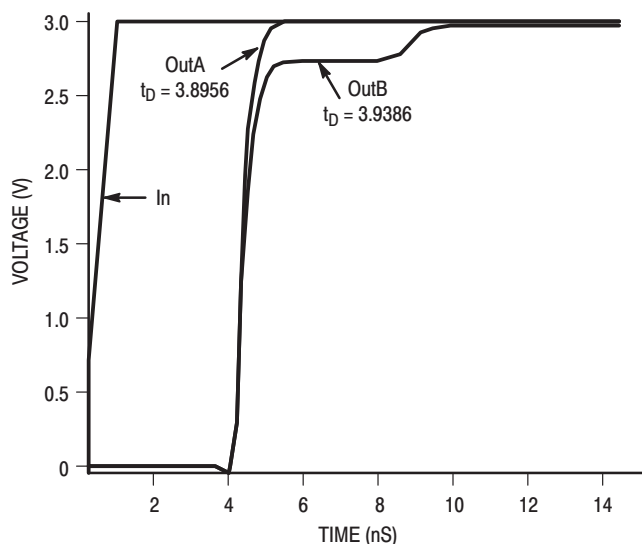


Figure 2. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 3 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

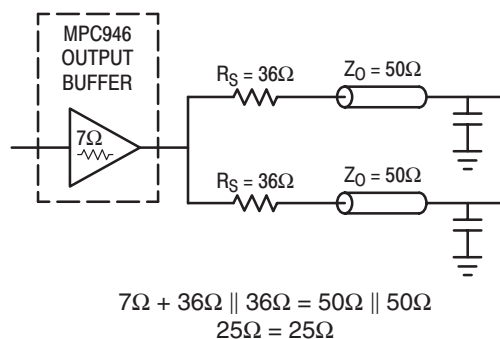


Figure 3. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Low Voltage 1:9 Clock Distribution Chip

The MPC947 is a 1:9 low voltage clock distribution chip. The device features the capability to select between two LVTTTL compatible inputs and fans the signal out to 9 LVCMOS or LVTTTL compatible outputs. These 9 outputs were designed and optimized to drive 50Ω series terminated transmission lines. With output-to-output skews of 500ps, the MPC947 is ideal as a clock distribution chip for synchronous systems which need a tight level of skew at a relatively low cost. For a similar product targeted at a higher price/performance point, consult the MPC948 data sheet.

- 2 Selectable LVCMOS/LVTTTL Clock Inputs
- 500ps Maximum Output-to-Output Skew
- Drives Up to 18 Independent Clock Lines
- Maximum Output Frequency of 110MHz
- Synchronous Output Enable
- Tristatable Outputs
- 32-Lead LQFP Packaging
- 3.3V V_{CC} Supply Voltage

With an output impedance of approximately 7Ω, in both the HIGH and LOW logic states, the output buffers of the MPC947 are ideal for driving series terminated transmission lines. More specifically, each of the 9 MPC947 outputs can drive two series terminated 50Ω transmission lines. With this capability, the MPC947 has an effective fanout of 1:18 in applications using point-to-point distribution schemes. With this level of fanout, the MPC947 provides enough copies of low skew clocks for high performance synchronous systems, including use as a clock distribution chip for the L2 cache of a PowerPC 620 based system.

Two independent LVCMOS/LVTTTL compatible clock inputs are available. Designers can take advantage of this feature to provide redundant clock sources or the addition of a test clock into the system design. With the select input pulled HIGH, the TTL_CLK1 input will be selected.

All of the control inputs are LVCMOS/LVTTTL compatible. The MPC947 provides a synchronous output enable control to allow for starting and stopping of the output clocks. A logic high on the Sync_OE pin will enable all of the outputs. Because this control is synchronized to the input clock, potential output glitching or runt pulse generation is eliminated. In addition, for board level test, the outputs can be tristated via the tristate control pin. A logic LOW applied to the Tristate input will force all of the outputs into high impedance. Note that all of the MPC947 inputs have internal pullup resistors.

The MPC947 is fully 3.3V compatible. The 32-lead LQFP package was chosen to optimize performance, board space and cost of the device. The 32-lead LQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

MPC947

**LOW VOLTAGE
1:9 CLOCK
DISTRIBUTION CHIP**



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A

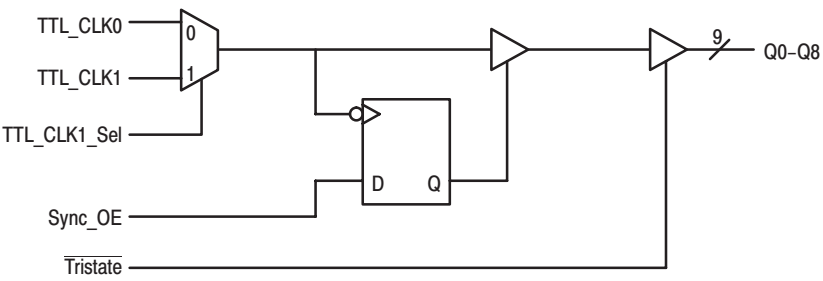


Figure 1. Logic Diagram

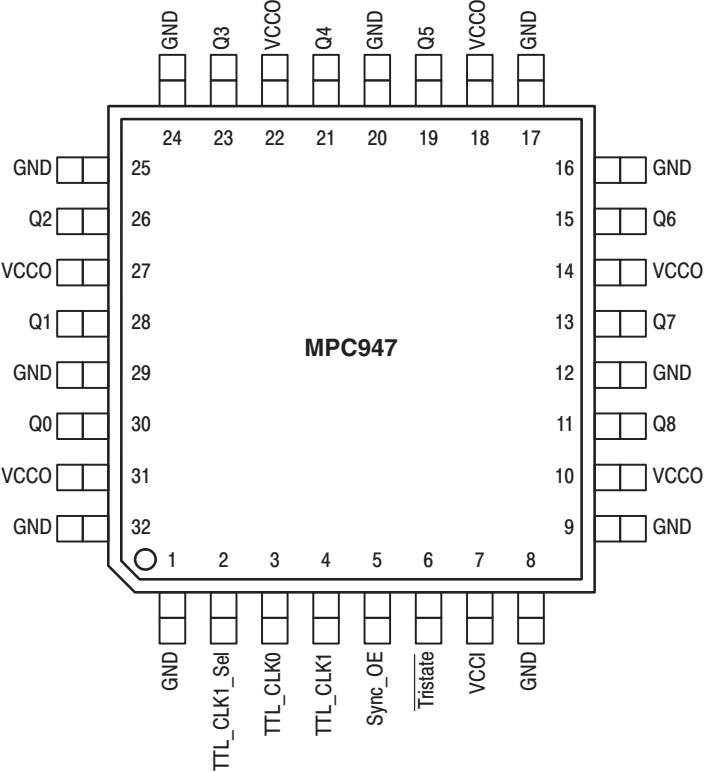


Figure 2. 32-Lead Pinout (Top View)

FUNCTION TABLES

TTL_CLK1_Sel	Input
0	TTL_CLK0
1	TTL_CLK1
Sync_OE	Outputs
0	Disabled
1	Enabled
Tristate	Outputs
0	Tristate
1	Enabled

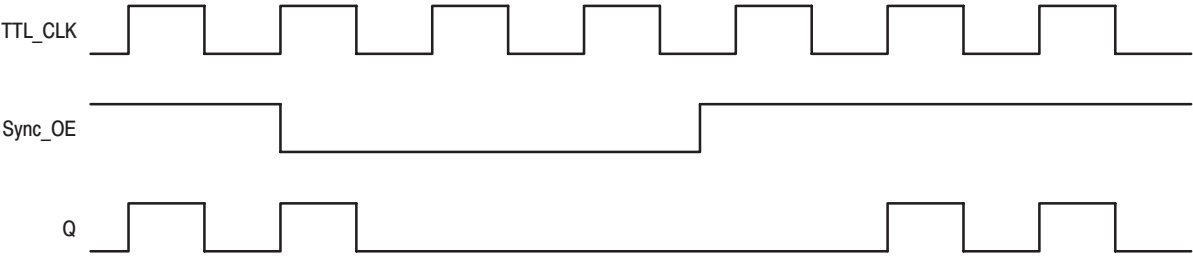


Figure 3. Sync_OE Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	4.6	V
V_I	Input Voltage	-0.3	$V_{DD} + 0.3$	V
I_{IN}	Input Current (CMOS Inputs)		± 20	mA
T_{Stor}	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		3.6	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.5			V	$I_{OH} = -20\text{mA}$ (Note 1.)
V_{OL}	Output LOW Voltage			0.4	V	$I_{OL} = 20\text{mA}$ (Note 1.)
I_{IN}	Input Current			-100	μA	Note 2.
I_{CC}	Maximum Quiescent Supply Current		21	28	mA	
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	Per Output

1. The MPC947 can drive 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to $V_{TT} = V_{CC}/2$. Alternately, the device drives up to two 50Ω series terminated transmission lines per output.
2. I_{IN} current is a result of internal pull-up resistors.

AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency	110			MHz	Note 3.
t_{pd}	Propagation Delay $TCLK$ to Q	4.75		9.25	ns	Note 3.
$t_{sk(o)}$	Output-to-Output Skew			500	ps	Note 3.
$t_{sk(pr)}$	Part-to-Part Skew			2.0	ns	Notes 3., 4.
t_{pwo}	Output Pulse Width	$t_{CYCLE}/2 - 800$		$t_{CYCLE}/2 + 800$	ps	Note 3., Measured at $V_{CC}/2$
t_s	Setup Time $Sync\_OE$ to Input Clk	0.0			ns	Notes 3., 5.
t_h	Hold Time Input Clk to $Sync\_OE$	1.0			ns	Notes 3., 5.
t_{PZL}, t_{PZH}	Output Enable Time			11	ns	
t_{PLZ}, t_{PHZ}	Output Disable Time			11	ns	
t_r, t_f	Output Rise/Fall Time	0.2		1.0	ns	0.8V to 2.0V

3. Driving 50Ω terminated to $V_{CC}/2$.
4. Part-to-part skew at a given temperature and voltage.
5. Setup and Hold times are relative to the falling edge of the input clock.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC947 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $VCC/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC947 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fan-out of the MPC947 clock driver is effectively doubled due to its capability to drive multiple lines.

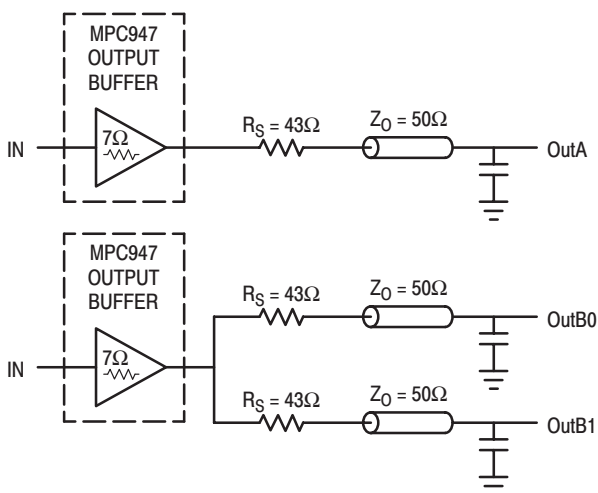


Figure 4. Single versus Dual Transmission Lines

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC947 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC947. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_o / R_s + R_o + Z_o) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

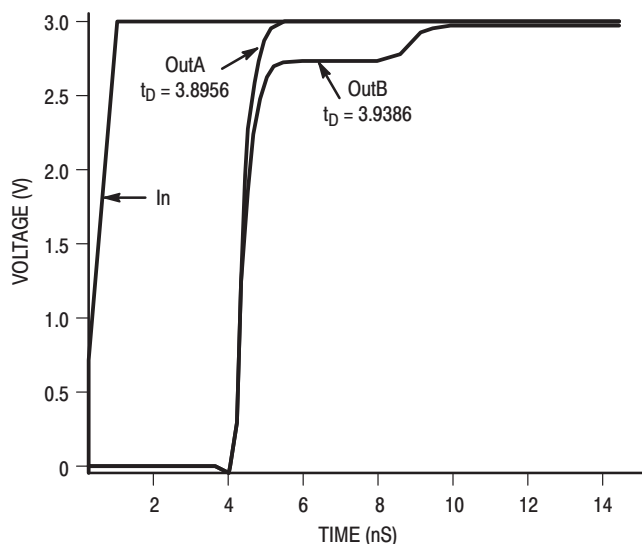


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

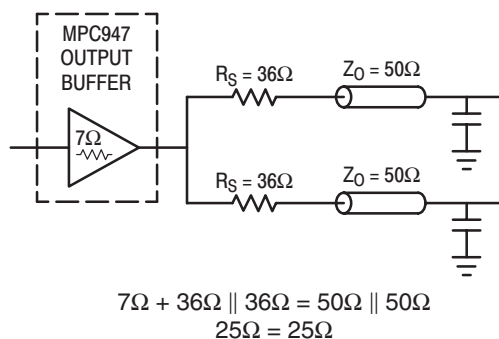


Figure 6. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Low Voltage 1:12 Clock Distribution Chip

The MPC948 is a 1:12 low voltage clock distribution chip. The device features the capability to select either a differential LVPECL or a LVTTTL compatible input. The 12 outputs are LVCMOS or LVTTTL compatible and feature the drive strength to drive 50Ω series terminated transmission lines. With output-to-output skews of 350ps, the MPC948 is ideal as a clock distribution chip for the most demanding of synchronous systems. For a similar product targeted at a lower price/performance point, please consult the MPC947 data sheet.

- Clock Distribution for PowerPC™ 620 L2 Cache
- LVPECL or LVCMOS/LVTTTL Clock Input
- 350ps Maximum Output-to-Output Skew
- Drives Up to 24 Independent Clock Lines
- Maximum Output Frequency of 150MHz
- Synchronous Output Enable
- Tristatable Outputs
- 32-Lead LQFP Packaging
- 3.3V V_{CC} Supply Voltage

With an output impedance of approximately 7Ω, in both the HIGH and LOW logic states, the output buffers of the MPC948 are ideal for driving series terminated transmission lines. More specifically, each of the 12 MPC948 outputs can drive two series terminated 50Ω transmission lines. With this capability, the MPC948 has an effective fanout of 1:24 in applications where each line drives a single load. With this level of fanout, the MPC948 provides enough copies of low skew clocks for high performance synchronous systems, including use as a clock distribution chip for the L2 cache of a PowerPC 620 based system.

The differential LVPECL inputs of the MPC948 allow the device to interface directly with a LVPECL fanout buffer like the MC100LVE111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS/LVTTTL input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used to provide for a test clock interface as well as the primary system clock. A logic HIGH on the TTL_CLK_Sel pin will select the TTL level clock input.

All of the control inputs are LVCMOS/LVTTTL compatible. The MPC948 provides a synchronous output enable control to allow for starting and stopping of the output clocks. A logic high on the Sync_OE pin will enable all of the outputs. Because this control is synchronized to the input clock, potential output glitching or runt pulse generation is eliminated. In addition, for board level test, the outputs can be tristated via the tristate control pin. A logic LOW applied to the Tristate input will force all of the outputs into high impedance. Note that all of the MPC948 inputs have internal pullup resistors.

The MPC948 is fully 3.3V compatible. The 32-lead LQFP package was chosen to optimize performance, board space and cost of the device. The 32-lead LQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

MPC948

LOW VOLTAGE 1:12 CLOCK DISTRIBUTION CHIP



FA SUFFIX
 32-LEAD LQFP PACKAGE
 CASE 873A

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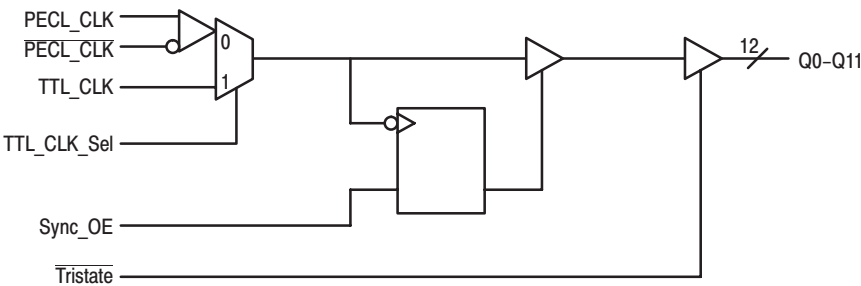


Figure 1. Logic Diagram

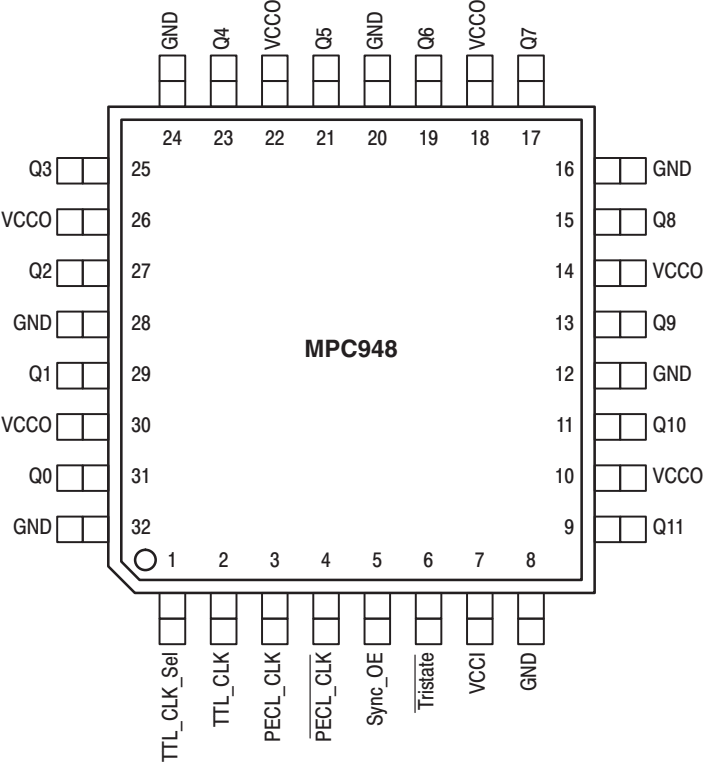


Figure 2. 32-Lead Pinout (Top View)

FUNCTION TABLES

TTL_CLK_Sel	Input
0	PECL_CLK
1	TTL_CLK

Sync_OE	Outputs
0	Disabled
1	Enabled

Tristate	Outputs
0	Tristate
1	Enabled

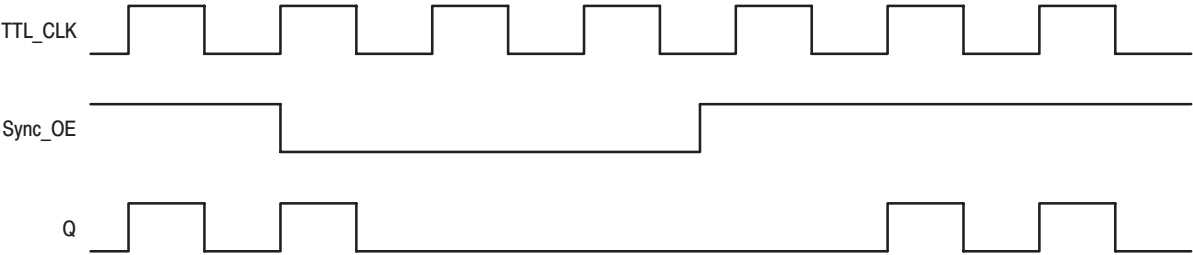


Figure 3. Sync_OE Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	4.6	V
V_I	Input Voltage	-0.3	$V_{DD} + 0.3$	V
I_{IN}	Input Current		± 20	mA
T_{Stor}	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage PECL_CLK Other	2.135 2.0		2.42 3.60	V	Single Ended Spec
V_{IL}	Input LOW Voltage PECL_CLK Other	1.49		1.825 0.8	V	Single Ended Spec
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK	300		1000	mV	
V_{CMR}	Common Mode Range PECL_CLK	$V_{CC} - 2.0$		$V_{CC} - 0.6$	V	Note 1.
V_{OH}	Output HIGH Voltage	2.5			V	$I_{OH} = -20\text{mA}$ (Note 2.)
V_{OL}	Output LOW Voltage			0.4	V	$I_{OL} = 20\text{mA}$ (Note 2.)
I_{IN}	Input Current			± 100	μA	Note 3.
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	Per Output
I_{CC}	Maximum Quiescent Supply Current		22	30	mA	

- V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "HIGH" input is within the V_{CMR} range and the input swing lies within the V_{PP} specification.
- The MPC948 can drive 50Ω transmission lines on the incident edge. Each output can drive one 50Ω parallel terminated transmission line to the termination voltage of $V_{TT} = V_{CC}/2$. Alternately, the device drives up to two 50Ω series terminated transmission lines.
- Inputs have pull-up resistors which affect input current, PECL_CLK has a pull-down resistor.

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AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Assumes 50% input duty cycle)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency	150			MHz	Note 4.
t_{pd}	Propagation Delay PECL_CLK to Q TTL_CLK to Q	4.0 4.4		8.0 8.9	ns	Note 4.
$t_{sk(o)}$	Output-to-Output Skew			350	ps	Note 4.
$t_{sk(pr)}$	Part-to-Part Skew PECL_CLK to Q TTL_CLK to Q			1.5 2.0	ns	Notes 4., 5.
t_{pwo}	Output Pulse Width	$t_{CYCLE}/2 - 800$		$t_{CYCLE}/2 + 800$	ps	Notes 4., 6. Measured at $V_{CC}/2$
t_s	Setup Time Sync_OE to PECL_CLK Sync_OE to TTL_CLK	1.0 0.0			ns	Notes 4., 7.
t_h	Hold Time PECL_CLK to Sync_OE TTL_CLK to Sync_OE	0.0 1.0			ns	Notes 4., 7.
t_{PZL}, t_{PZH}	Output Enable Time	3		11	ns	
t_{PLZ}, t_{PHZ}	Output Disable Time	3		11	ns	
t_r, t_f	Output Rise/Fall Time	0.20		1.0	ns	0.8V to 2.0V

- Driving 50Ω transmission lines.
- Part-to-part skew at a given temperature and voltage.
- Assumes 50% input duty cycle.
- Setup and Hold times are relative to the falling edge of the input clock.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC948 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $VCC/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC948 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fan-out of the MPC948 clock driver is effectively doubled due to its capability to drive multiple lines.

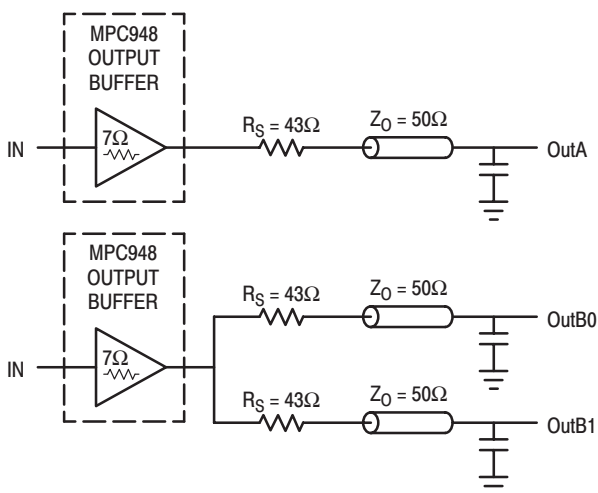


Figure 4. Single versus Dual Transmission Lines

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC948 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC948. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S \left(\frac{Z_o}{R_s + R_o + Z_o} \right) = 3.0 \left(\frac{25}{53.5} \right) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

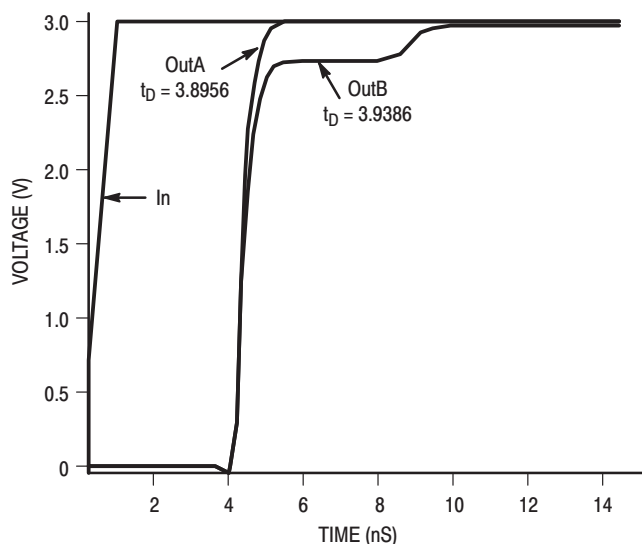


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

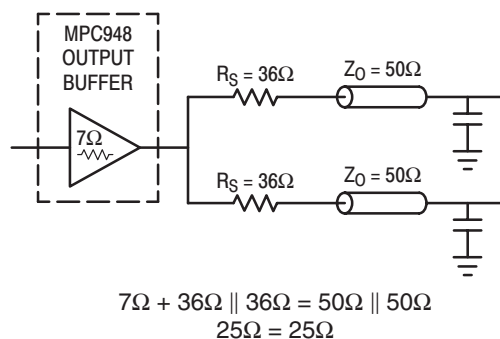


Figure 6. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Low Voltage 1:15 PECL to CMOS Clock Driver

The MPC949 is a low voltage CMOS, 15 output clock buffer. The 15 outputs can be configured into a standard fanout buffer or into 1X and 1/2X combinations. The device features a low voltage PECL input, in addition to its LVCMOS/LVTTL inputs, to allow it to be incorporated into larger clock trees which utilize low skew PECL devices (see the MC100EP111 data sheet) in the lower branches of the tree. The fifteen outputs were designed and optimized to drive 50Ω series or parallel terminated transmission lines. With output to output skews of 350ps the MPC949 is an ideal clock distribution chip for synchronous systems which need a tight level of skew from a large number of outputs. For a similar product with a smaller fanout and package consult the MPC946 data sheet.

- Low Voltage PECL Clock Input
- 2 Selectable LVCMOS/LVTTL Clock Inputs
- 350ps Maximum Output to Output Skew
- Drives up to 30 Independent Clock Lines
- Maximum Output Frequency of 160MHz
- High Impedance Output Enable
- 52-Lead LQFP Packaging
- 3.3V V_{CC} Supply

With an output impedance of approximately 7Ω, in both the HIGH and the LOW logic states, the output buffers of the MPC949 are ideal for driving series terminated transmission lines. More specifically each of the 15 MPC949 outputs can drive two series terminated transmission lines. With this capability, the MPC949 has an effective fanout of 1:30 in applications using point-to-point distribution schemes.

The MPC949 has the capability of generating 1X and 1/2X signals from a 1X source. The design is fully static, the signals are generated and retimed inside the chip to ensure minimal skew between the 1X and 1/2X signals. The device features selectability to allow the user to select the ratio of 1X outputs to 1/2X outputs.

Two independent LVCMOS/LVTTL compatible clock inputs are available. Designers can take advantage of this feature to provide redundant clock sources or the addition of a test clock into the system design. With the TCLK_Sel input pulled HIGH the TCLK1 input is selected. The PCLK_Sel input will select the PECL input clock when driven HIGH.

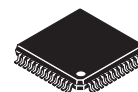
All of the control inputs are LVCMOS/LVTTL compatible. The Dsel pins choose between 1X and 1/2X outputs. A LOW on the Dsel pins will select the 1X output. The MR/ŌE input will reset the internal flip flops and tristate the outputs when it is forced HIGH.

The MPC949 is fully 3.3V compatible. The 52 lead LQFP package was chosen to optimize performance, board space and cost of the device. The 52-lead LQFP has a 10x10mm body size with a 0.65mm pin spacing.

MPC949

See Upgrade Product – MPC9449

LOW VOLTAGE 1:15 PECL TO LVCMOS CLOCK DRIVER



FA SUFFIX
52-LEAD LQFP PACKAGE
CASE 848D

Figure 1. Logic Diagram

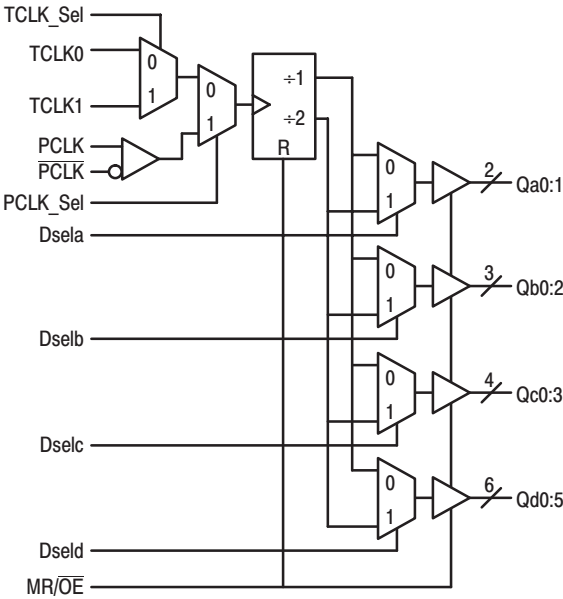
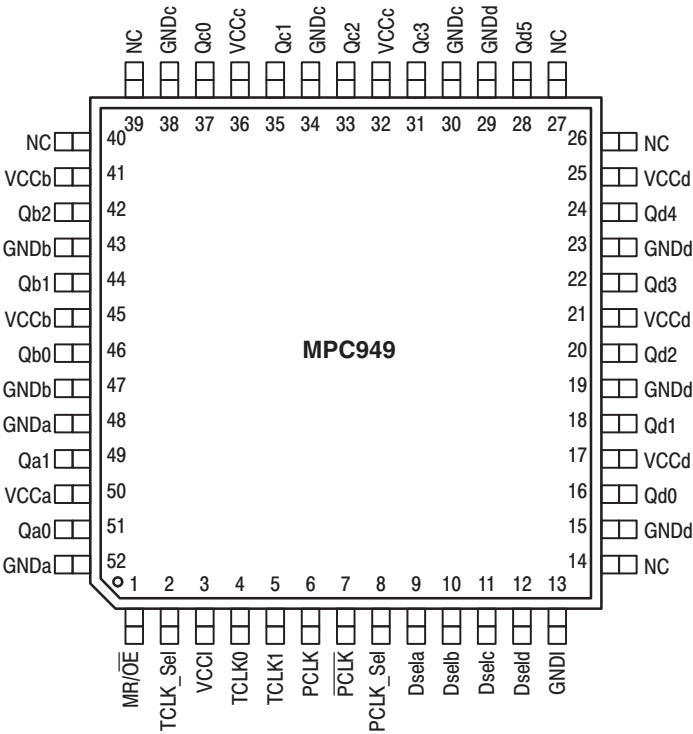


Figure 2. 52-Lead Pinout (Top View)



6

FUNCTION TABLE

Input	0	1
TCLK_Sel	TCLK0	TCLK1
PCLK_Sel	TCLKn	PCLK
Dseln	$\div 1$	$\div 2$
MR/OE	Enabled	Hi-Z

PIN DESCRIPTION

Pin Name	Function
TCLK_Sel (Int Pulldown)	Select pin to choose TCKL0 or TCLK1
TCLK0:1 (Int Pullup)	LVC MOS/LVTTL clock inputs
PCLK (Int Pulldown)	True PECL clock input
$\overline{\text{PCLK}}$ (Int Pullup)	Complement PECL clock input
Dseln (Int Pulldown)	1x or 1/2x input divide select pins
MR/OE (Int Pulldown)	Internal reset and output tristate control pin
PCLK_Sel (Int Pulldown)	Select Pin to choose TCLK or PCLK

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	4.6	V
V_I	Input Voltage	-0.3	$V_{DD} + 0.3$	V
I_{IN}	Input Current	TBD	TBD	mA
T_{Stor}	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage (Except PECL_CLK)	2.0		3.60	V	
V_{IL}	Input LOW Voltage (Except PECL_CLK)			0.8	V	
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK	300		1000	mV	
V_{CMR}	Common Mode Range PECL_CLK	$V_{CC} - 2.0$		$V_{CC} - 0.6$	V	Note 1.
V_{OH}	Output HIGH Voltage	2.5			V	$I_{OH} = -20\text{mA}$ (Note 2.)
V_{OL}	Output LOW Voltage			0.4	V	$I_{OL} = 20\text{mA}$ (Note 2.)
I_{IN}	Input Current			± 120	μA	Note 3.
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	Per Output
I_{CC}	Maximum Quiescent Supply Current		70	85	mA	

1. V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "HIGH" input is within the V_{CMR} range and the input swing lies within the V_{PP} specification.
2. The MPC949 can drive 50Ω transmission lines on the incident edge. Each output can drive one 50Ω parallel terminated transmission line to the termination voltage of $V_{TT} = V_{CC}/2$. Alternately, the device drives up to two 50Ω series terminated transmission lines.
3. Inputs have pull-up/pull-down resistors which affect input current.

AC CHARACTERISTICS ($T_A = 0^\circ$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency	160			MHz	Note 4.
t_{PLH}	Propagation Delay PECL_CLK to Q TTL_CLK to Q	4.0 4.2	6.5 7.5	9.0 10.6	ns	Note 4.
t_{PHL}	Propagation Delay PECL_CLK to Q TTL_CLK to Q	3.8 4.0	6.2 7.2	8.6 10.5	ns	Note 4.
$t_{sk(o)}$	Output-to-Output Skew		300	350	ps	Note 4.
$t_{sk(pp)}$	Part-to-Part Skew PECL_CLK to Q TTL_CLK to Q		1.5 2.0	2.75 4.0	ns	Note 5.
t_{PZL}, t_{PZH}	Output Enable Time		3	11	ns	Note 4.
t_{PLZ}, t_{PHZ}	Output Disable Time		3	11	ns	Note 4.
t_r, t_f	Output Rise/Fall Time	0.10		1.0	ns	0.8V to 2.0V

4. Driving 50Ω transmission lines terminated to $V_{CC}/2$.
5. Part-to-part skew at a given temperature and voltage.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC949 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $VCC/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC949 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fan-out of the MPC949 clock driver is effectively doubled due to its capability to drive multiple lines.

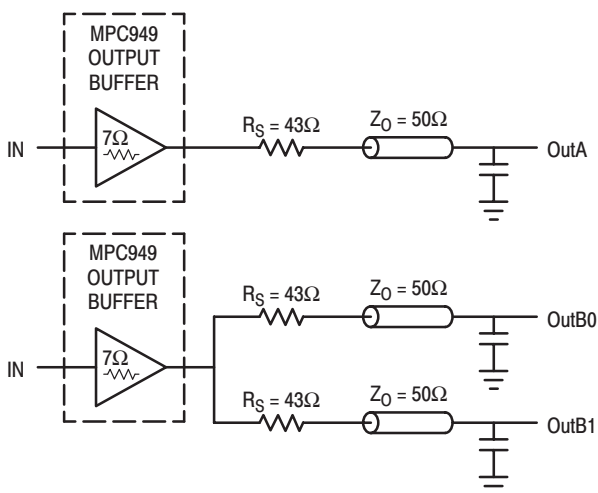


Figure 3. Single versus Dual Transmission Lines

The waveform plots of Figure 4 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC949 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC949. The output waveform in Figure 4 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_o / R_s + R_o + Z_o) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

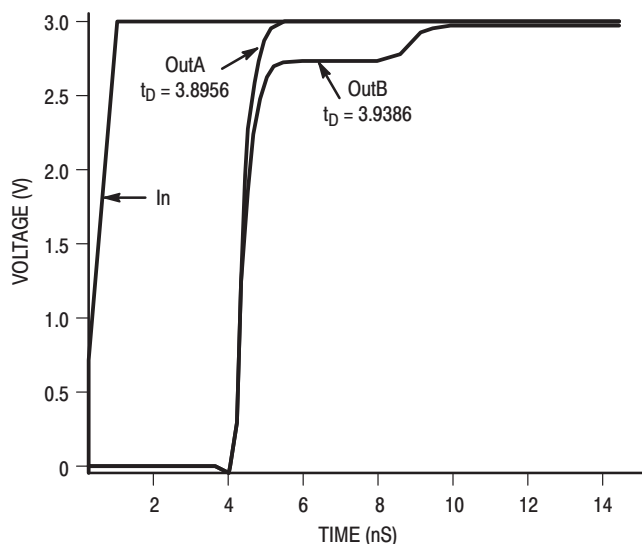


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

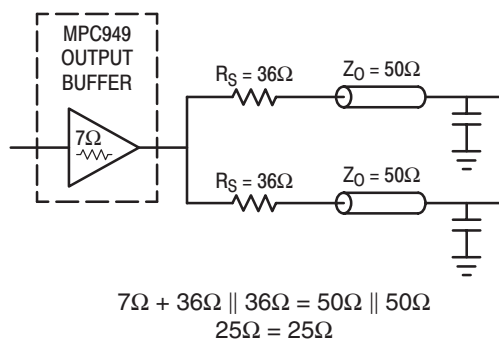


Figure 5. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Chapter Seven

Differential Fanout Buffer Data Sheets

Differential Fanout Buffer Device Index

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Low-Voltage 1:10 Differential ECL/PECL/HSTL Clock Driver

The MC100EP111 is a low skew 1-to-10 differential driver, designed with clock distribution in mind. It accepts two clock sources into an input multiplexer. The ECL/PECL input signals can be either differential or single-ended if the V_{BB} output is used. HSTL inputs can be used when the EP111 is operating under PECL conditions. The selected signal is fanned out to 10 identical differential outputs.

- 100ps Part-to-Part Skew typical
- 35ps Output-to-Output Skew typical
- Differential Design
- V_{BB} Output
- Low Voltage V_{EE} Range of -2.25 to -3.8V for ECL
- Low Voltage V_{CC} Range of +2.25 to +3.8V for PECL and HSTL
- 75k Ω Input Pulldown Resistors
- ECL/PECL Outputs

The EP111 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate-to-gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50 Ω , even if only one side is being used. In most applications, all ten differential pairs will be used and therefore terminated. In the case where fewer than ten pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The MC100EP111, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the EP111 to be used for high performance clock distribution in +3.3V or +2.5V systems. Designers can take advantage of the EP111's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using PECL, designers should refer to Motorola Application Note AN1406/D.

The MC100EP111 may be driven single-endedly utilizing the V_{BB} bias output with the $\overline{CLK0}$ input. If a single-ended signal is to be used, the V_{BB} pin should be connected to the $\overline{CLK0}$ input and bypassed to ground via a 0.01 μ F capacitor. The V_{BB} output can only source/sink 0.2mA; therefore, it should be used as a switching reference for the MC100EP111 only. Part-to-Part Skew specifications are not guaranteed when driving the MC100EP111 single-endedly.

Rev 1

MC100EP111

See Upgrade Product – MC100ES6111

LOW-VOLTAGE 1:10 DIFFERENTIAL ECL/PECL/HSTL CLOCK DRIVER



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A

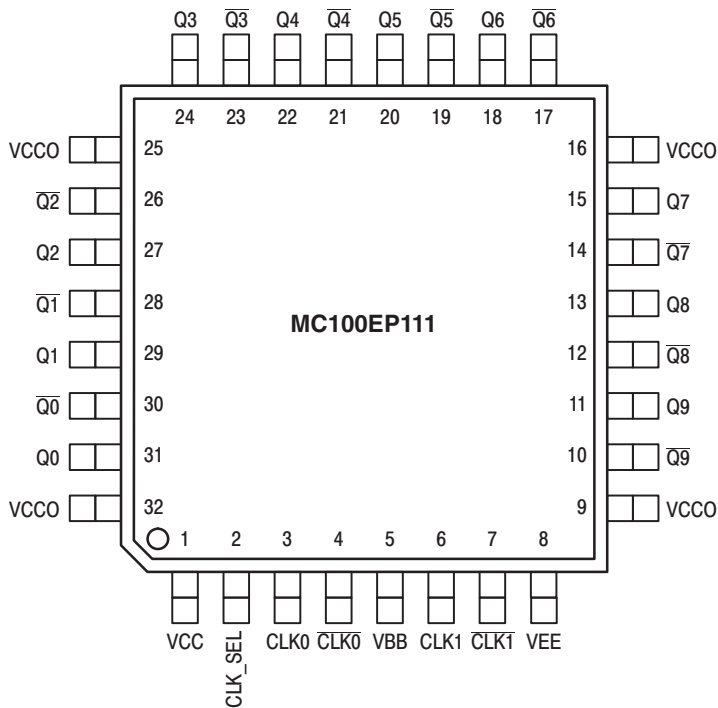


Figure 1. 32-Lead TQFP Pinout
(Top View)

PIN NAMES

Pins	Function
CLK0, $\overline{\text{CLK0}}$	Differential ECL/PECL Input Pair
CLK1, $\overline{\text{CLK1}}$	Differential HSTL Input Pair
Q0:9, $\overline{\text{Q0:9}}$	Differential PECL Outputs
CLK_SEL	Active Clock Select Input
VBB	V _{BB} Output

FUNCTION

CLK_SEL	Active Input
0	CLK0, $\overline{\text{CLK0}}$
1	CLK1, $\overline{\text{CLK1}}$

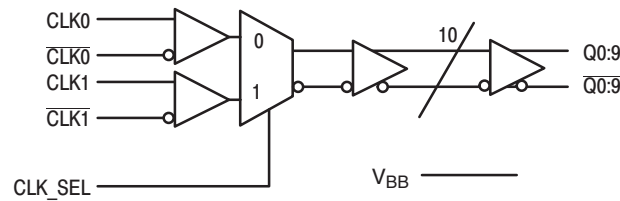


Figure 2. Logic Symbol

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	-0.3	4.6	V
V _I	Input Voltage	-0.3	V _{CC} + 0.3	V
I _{IN}	Input Current		±20	mA
T _{Stor}	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

THERMAL CHARACTERISTICS

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

DC CHARACTERISTICS

Vsupply : VCC=VCC0 = 0.0 volts, VEE = -2.25 to -3.80 volts

Symbol	Characteristic	-40°C			25°C			70°C			Unit	Condition
IEE	Internal supply current	45		85	60		95	65		105	mA	Absolute value of current
ICC	Output and Internal supply current	270		360	290		380	300		380	mA	All outputs terminated 50Ω to VCC=-2.0V
IIN	Input current			150			150			150	μA	Includes pullup/pulldown resistors
VBB	Internally generated bias voltage	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V	for VEE= -3.0 to -3.8 volts
VBB	Internally generated bias voltage	-1.38		-1.16	-1.38		-1.16	-1.38		-1.16	V	for VEE= -2.25 to -2.75 volts
VIH	Input HIGH voltage (CLK_SEL)	-1.165		-0.880	-1.165		-0.880	-1.165		-0.880	V	Difference of input $\approx$ VIH - VIL ¹ Cross point of input $\approx$ average (VIH,VIL)
VIL	Input LOW voltage (CLK_SEL)	-1.810		-1.475	-1.810		-1.475	-1.810		-1.475	V	
VPP	Input amplitude (CLK0,CLK0)	0.5		1.3	0.5		1.3	0.5		1.3	V	
VCMR	Common mode voltage (CLK0,CLK0)	VEE+1.0		-0.3	VEE+1.0		-0.3	VEE+1.0		-0.3	V	
VOH	Output HIGH voltage	-1.30		-0.95				-1.20		-0.90	mV	IOH = -30 mA
VOL	Output LOW voltage	-1.85		-1.40				-1.90		-1.50		IOL = -5 mA
VOUTpp	Differential output swing	350						500				

DC CHARACTERISTICS

Vsupply : VCC=VCC0 = 2.25 to 3.80 volts, VEE = 0.0 volts

Symbol	Characteristic	-40°C			25°C			70°C			Unit	Condition
IEE	Internal supply current	45		85	60		95	65		105	mA	Absolute value of current
ICC	Output and Internal supply current	270		360	290		380	300		380	mA	All outputs terminated 50Ω to VCC=-2.0V
IIN	Input current			150			150			150	μA	Includes pullup/pulldown resistors
VBB	Internally generated bias voltage	VCC-1.38		VCC-1.26	VCC-1.38		VCC-1.26	VCC-1.38		VCC-1.26	V	for VCC= 3.0 to 3.8 volts
VBB	Internally generated bias voltage	VCC-1.38		VCC-1.16	VCC-1.38		VCC-1.16	VCC-1.38		VCC-1.16	V	for VCC= 2.25 to 2.75 volts
VIH	Input HIGH voltage (CLK_SEL)	VCC-1.165		VCC-0.880	VCC-1.165		VCC-0.880	VCC-1.165		VCC-0.880	V	Difference of input $\approx$ VIH - VIL ¹ Cross point of input $\approx$ average (VIH,VIL)
VIL	Input LOW voltage (CLK_SEL)	VCC-1.810		VCC-1.475	VCC-1.810		VCC-1.475	VCC-1.810		VCC-1.475	V	
VPP	Input amplitude (CLK0,CLK0)	0.5		1.3	0.5		1.3	0.5		1.3	V	
VCMR	Common mode voltage (CLK0,CLK0)	1		VCC-0.3	1		VCC-0.3	1		VCC-0.3	V	
Vdif	Differential input voltage (CLK1,CLK1)	0.4		1.9	0.4		1.9	0.4		1.9	V	Difference of input $\approx$ VIH - VIL
Vx	Input crossover voltage (CLK1,CLK1)	0.68		0.9	0.68		0.9	0.68		0.9	V	Cross point of input $\approx$ average (VIH,VIL)

DC CHARACTERISTICSV_{supply} : VCC=VCC0 = 2.25 to 3.80 volts, VEE = 0.0 volts

VOH	Output HIGH voltage	VCC–1.30	VCC–0.95		VCC–1.20	VCC–0.90		IOH = –30 mA
VOL	Output LOW voltage	VCC–1.85	VCC–1.40		VCC–1.90	VCC–1.50		IOL = –5 mA
VOUTpp	Differential output swing	350			500		mV	
Note 1. VPP minimum and maximum required to maintain AC specifications. Actual device function will tolerate minimum VPP of 100 mV.								

AC CHARACTERISTICS – PECL InputV_{supply} : VCC=VCC0 = 2.25 to 3.80 volts, VEE = 0.0 volts –OR–

VCC=VCC0 = 0.0 volts, VEE = –2.25 to –3.80 volts

Symbol	Characteristic	–40°C			25°C			70°C			Unit	Condition
		Min	typ	Max	Min	typ	Max	Min	typ	Max		
Tpd	Differential propagation delay											Nominal (single input condition) VPP = 0.650V, VCMR = VCC–0.800V Note 2
	CLK0, $\overline{\text{CLK0}}$ to all Q0, $\overline{\text{Q0}}$ thru Q9, $\overline{\text{Q9}}$	350		500	380		530	450		600	ps	
Tsk(part)	Part to part skew			150			150			150	ps	
Tsk(output)	Output to output skew for given part		35	70		30	65		30	60	ps	Note 2
Tpd	Differential propagation delay											Note 2
	CLK0, $\overline{\text{CLK0}}$ to all Q0, $\overline{\text{Q0}}$ thru Q9, $\overline{\text{Q9}}$	280		600	300		620	370		700	ps	
Tsk(part)	Part to part skew			320			320			330	ps	
Tsk(output)	Output to output skew for given part		35	70		30	65		30	60	ps	Note 2
Fmax	Maximum frequency			1500			1500			1500	MHz	Functional to 1.5 GHz Timing specifications apply up to 1.0 GHz
Tr / Tf	Output rise and fall times (20%, 80%)	100		300	100		300	100		300	ps	All outputs terminated 500Ω to VCC–2.0V

AC CHARACTERISTICS – HSTL Input

Vsupply : VCC=VCC0 = 2.25 to 3.8 volts, VEE = 0.0 volts

Symbol	Characteristic	–40°C			25°C			70°C			Unit	Condition
		Min	typ	Max	Min	typ	Max	Min	typ	Max		
Tpd	Differential propagation delay											Nominal (single input condition) Vdif = 1.000V, Vx = VEE+0.750V Note 2
	CLK1,CLK1 to all Q0,Q0 thru Q9,Q9	380		530	420		570	500		650	ps	
Tsk(part)	Part to part skew			150			150			150	ps	
Tsk(output)	Output to output skew for given part		35	70		30	65		30	60	ps	Note 2
Tpd	Differential propagation delay											All input conditions (full input range) Note 2
	CLK1,CLK1 to all Q0,Q0 thru Q9,Q9	300		600	350		650	430		750	ps	
Tsk(part)	Part to part skew			300			300			320	ps	
Tsk(output)	Output to output skew for given part		35	70		30	65		30	60	ps	Note 2
Fmax	Maximum frequency			250			250			250	MHz	Functional to 250 MHz Timing specifications apply up to 250 MHz
Tr / Tf	Output rise and fall times (20%, 80%)	100		300	100		300	100		300	ps	All outputs terminated 500Ω to VCC–2.0V
Note 2. For operation with 2.5 volt supply, the output termination is 50Ω to VEE. For operation at 3.3 volt supply, the output termination is 50Ω to VCC–2v.												

Low-Voltage 1:5 Dual Differential ECL/PECL Clock Driver

The MC100EP210 is a low skew 1-to-5 dual differential driver, designed with clock distribution in mind. The input signals can be either differential or single-ended if the V_{BB} output is used. The signal is fanned out to 5 identical differential outputs.

- 150ps Part-to-Part Skew typical
- 35ps Output-to-Output Skew typical
- Differential Design
- V_{BB} Output
- Voltage and Temperature Compensated Outputs
- Low Voltage V_{EE} Range of -2.25 to $-3.8V$
- $75k\Omega$ Input Pulldown Resistors

The EP210 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate-to-gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω , even if only one side is being used. In most applications, all ten differential pairs will be used and therefore terminated. In the case where fewer than ten pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The MC100EP210, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the EP210 to be used for high performance clock distribution in $+3.3V$ or $+2.5V$ systems. Designers can take advantage of the EP210's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using PECL, designers should refer to Motorola Application Note AN1406/D.

The MC100EP210 may be driven single-endedly utilizing the V_{BB} bias output with the $\overline{CLKA}$ or $\overline{CLKB}$ input. If a single-ended signal is to be used, the V_{BB} pin should be connected to the $\overline{CLKA}$ or $\overline{CLKB}$ input and bypassed to ground via a $0.01 \mu F$ capacitor. The V_{BB} output can only source/sink $0.3mA$; therefore, it should be used as a switching reference for the MC100EP210 only. Part-to-Part Skew specifications are not guaranteed when driving the MC100EP210 single-endedly.

MC100EP210

See Upgrade Product – MC100ES6210

LOW-VOLTAGE 1:5 DUAL DIFFERENTIAL ECL/PECL CLOCK DRIVER



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A

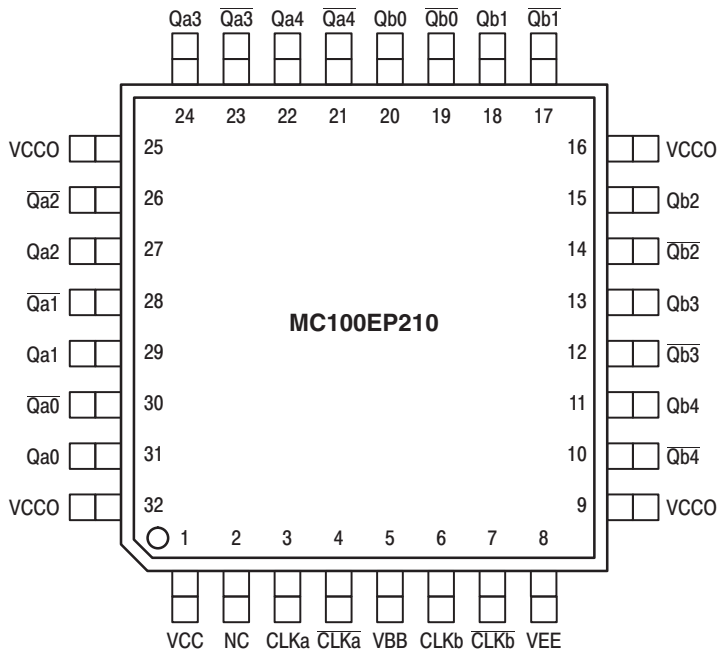


Figure 1. 32-Lead TQFP Pinout
(Top View)

PIN NAMES

Pins	Function
CLKn, CLKn	Differential Input Pairs
Qn0:4, Qn0:4	Differential Outputs
VBB	V _{BB} Output

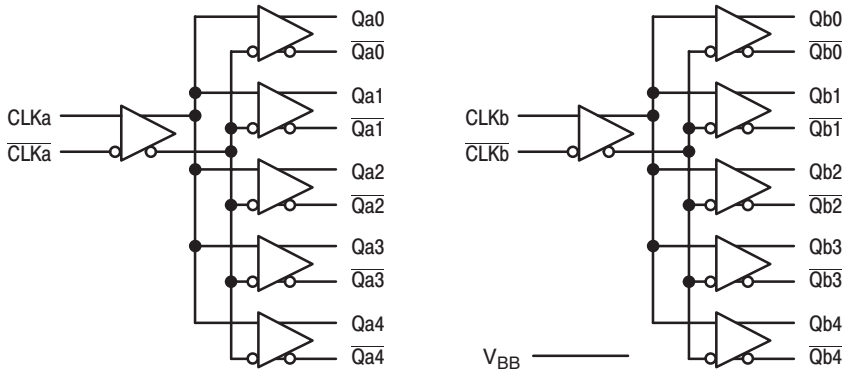


Figure 2. Logic Symbol

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	-0.3	4.6	V
V _I	Input Voltage	-0.3	V _{CC} + 0.3	V
I _{IN}	Input Current		±20	mA
T _{Stor}	Storage Temperature Range	-40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

THERMAL CHARACTERISTICS

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

DC CHARACTERISTICS

Vsupply : VCC=VCC0 = 0.0 volts, VEE = -2.25 to -3.80 volts

Symbol	Characteristic	-40°C		25°C		70°C		Unit	Condition
Min	typ	Max	Min	typ	Max	Min	typ	Max	
IEE	Internal supply current	20		75		20		75	
ICC	Output and Internal supply current	270		360		270		380	
IIN	Input current			150				150	
VBB	Internally generated bias voltage	-1.38		-1.26		-1.38		-1.26	
VBB	Internally generated bias voltage	-1.38		-1.16		-1.38		-1.16	
VPP	Input amplitude	0.5		1.3		0.5		1.3	
VCMR	Common mode voltage	VEE+1.0		-0.3		VEE+1.0		-0.3	
VOH	Output HIGH voltage	-1.30		-0.95		-1.20		-0.90	
VOL	Output LOW voltage	-1.85		-1.40		-1.90		-1.50	
VOUtp	Differential output swing	350				500			

DC CHARACTERISTICS

Vsupply : VCC=VCC0 = 2.25 to 3.80 volts, VEE = 0.0 volts

Symbol	Characteristic	-40°C		25°C		70°C		Unit	Condition
Min	typ	Max	Min	typ	Max	Min	typ	Max	
IEE	Internal supply current	20		75		30		85	
ICC	Output and Internal supply current	270		360		270		380	
IIN	Input current			150				150	
VBB	Internally generated bias voltage	VCC-1.38		VCC-1.26		VCC-1.38		VCC-1.26	
VBB	Internally generated bias voltage	VCC-1.38		VCC-1.16		VCC-1.38		VCC-1.16	
VPP	Input amplitude	0.5		1.3		0.5		1.3	
VCMR	Common mode voltage	1		VCC-0.3		1		VCC-0.3	
VOH	Output HIGH voltage	VCC-1.30		VCC-0.95		VCC-1.20		VCC-0.90	
VOL	Output LOW voltage	VCC-1.85		VCC-1.40		VCC-1.90		VCC-1.50	
VOUtp	Differential output swing	350				500			

Note 1. VPP minimum and maximum required to maintain AC specifications. Actual device function will tolerate minimum VPP of 100 mV.

AC CHARACTERISTICS

Vsupply : VCC=VCC0 = 2.25 to 3.80 volts, VEE = 0.0 volts – OR – VCC=VCC0 = 0.0 volts, VEE = –2.25 to –3.80 volts

Symbol	Characteristic	–40°C			25°C			70°C			Unit	Condition
		Min	typ	Max	Min	typ	Max	Min	typ	Max		
Tpd	Differential propagation delay CLK, $\overline{\text{CLK}}$ to all $\overline{\text{Q0}}, \overline{\text{Q0}}$ thru Q4, $\overline{\text{Q4}}$	270		420	300		450	380		530	ps	Nominal (single input condition) VPP = 0.650V, VCMR = VCC–0.800V Applies to 500 MHz reference. Note 2
Tsk(part)	Part to part skew			150			150			150	ps	At single frequency. Note 2
Tsk(output)	Output to output skew for given part		15	50		15	50		15	50	ps	Note 2
Tpd	Differential propagation delay CLK, $\overline{\text{CLK}}$ to all $\overline{\text{Q0}}, \overline{\text{Q0}}$ thru Q4, $\overline{\text{Q4}}$	220		520	250		550	320		620	ps	All input conditions Note 2
Tsk(part)	Part to part skew			300			300			300	ps	Note 2
Tsk(output)	Output to output skew for given part		15	50		15	50		15	50	ps	Note 2
Fmax	Maximum frequency			1500			1500			1500	MHz	Functional to 1.5 GHz Timing specifications apply up to 1.0 GHz
Tr / Tf	Output rise and fall times (20%, 80%)	100		300	100		300	100		300	ps	Note 2

Note 2. For operation with 2.5 volt supply, the output termination is 50Ω to VEE. For operation at 3.3 volt supply, the output termination is 50Ω to VCC–2v.

Low-Voltage Dual 1:10 Differential ECL/PECL Clock Driver

The MC100EP220 is a dual low skew 1-to-10 differential driver, designed with clock distribution in mind. The V_{BB} output provides a DC threshold bias for single ended sources. The V_{BB} can be connected to the true input or the complementary input, the latter will produce an inverted output. If used, the V_{BB} output should be bypassed to ground.

- 225ps Max. Part-to-Part Skew
- 60ps Output-to-Output Skew
- Differential Design
- V_{BB} Output
- Voltage and Temperature Compensated Outputs
- Low Voltage V_{EE} Range of -2.375 to $-3.8V$
- $65k\Omega$ Input Pulldown Resistors

The EP220 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate-to-gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

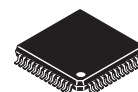
To ensure that the tight skew specification is met it is necessary that both pairs of the differential outputs are terminated into 50Ω , even if only one side is being used. In applications which do not use all of the outputs, it is best to leave unused pairs open to minimize power consumption in the device.

The MC100EP220, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the EP220 to be used for high performance clock distribution in $+3.3V$ or $+2.5V$ systems. Designers can take advantage of the EP220's performance to distribute low skew clocks across the backplane. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using PECL, designers should refer to Motorola Application Note AN1406/D.

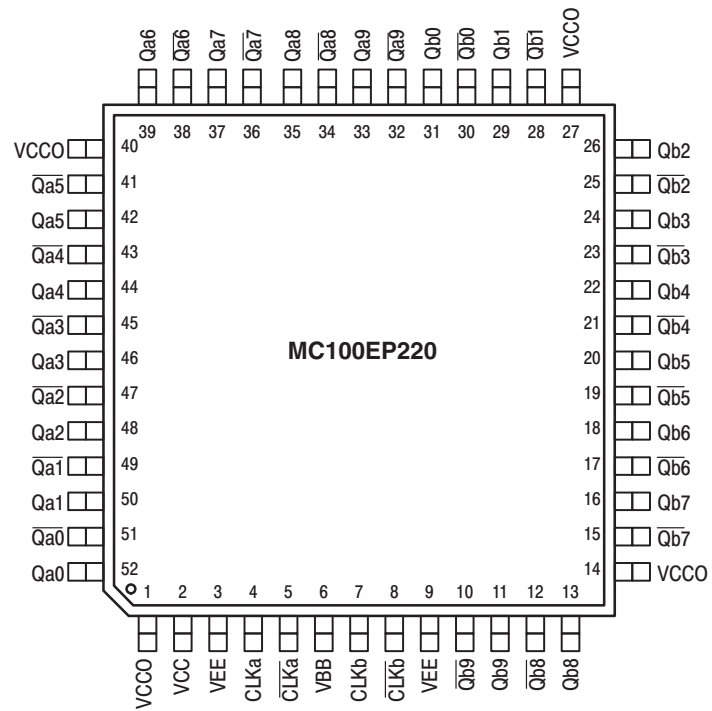
MC100EP220

See Upgrade Product – MC100ES6220

LOW-VOLTAGE DUAL 1:10 DIFFERENTIAL ECL/PECL CLOCK DRIVER



TB SUFFIX
52-LEAD LQFP PACKAGE
EXPOSED PAD
CASE 1336



Pinout: 52-Lead LQFP
(Top View)

LOGIC SYMBOL

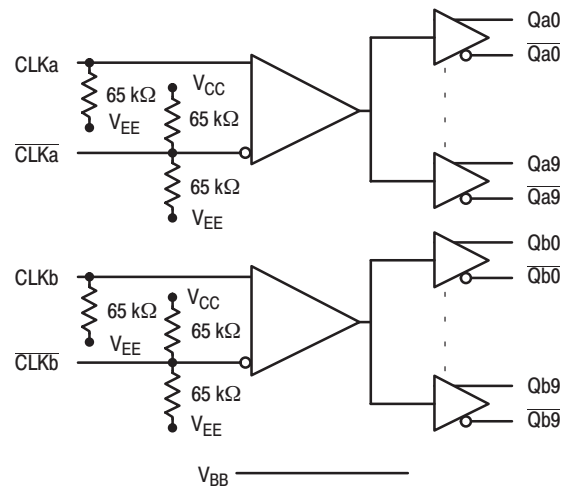


Table 1: PIN CONFIGURATION

Pin	I/O	Type	Function
CLKA, $\overline{\text{CLKA}}$	Input	ECL/LVPECL	Differential reference clock signal input for fanout buffer A
CLKB, $\overline{\text{CLKB}}$	Input	ECL/LVPECL	Differential reference clock signal input for fanout buffer B
Q[0-19], $\overline{\text{Q}}[0-19]$	Output	LVPECL	Differential clock outputs
VEE ^a	Supply		Negative power supply
V _{CC} , V _{CCO}	Supply		Positive power supply. All V _{CC} and V _{CCO} pins must be connected to the positive power supply for correct DC and AC operation
V _{BB}	Output		DC bias output for single ended input operation

- a. In ECL mode (negative power supply mode), VEE is either -3.3V or -2.5V and VCC is connected to GND (0V).
 In PECL mode (positive power supply mode), VEE is connected to GND (0V) and VCC is either +3.3V or +2.5V.
 In both modes, the input and output levels are referenced to the most positive supply (VCC).

Table 2: ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	4.6	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} +0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} +0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage temperature	-65	125	°C	

- a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3: GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output termination voltage		V _{CC} - 2 ^a		V	
MM	ESD Protection (Machine model)	75			V	
HBM	ESD Protection (Human body model)	1500			V	
CDM	ESD Protection (Charged device model)	500			V	
LU	Latch-up immunity	200			mA	
C _{IN}			4.0		pF	Inputs
θ _{JA}	Thermal resistance junction to ambient	See application information ^b				
θ _{JC}	Thermal resistance junction to case	See application information				

- a. Output termination voltage V_{TT} = 0V for V_{CC}=2.5V operation is supported but the power consumption of the device will increase.
 b. Proper thermal management is critical for reliable system operation. This especially true for high-fanout and high drive capability products. Thermal package information and exposed pad land pattern design recommendations are available in the applications section of this data-sheet. In addition, the means of calculating die power consumption, the corresponding die temperature and the relationship to long-term reliability is addressed in the Motorola application note AN1545. Thermal modeling is recommended for the MC100EP220.

Table 4: PECL DC Characteristics ($V_{CCO} = V_{CC} = 2.375V$ to $3.8V$, $V_{EE} = GND$)

Symbol	Characteristics	T _A = -40°C		T _A = 25°C		T _A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
Clock input pair CLKA, $\overline{CLKA}$, CLKB, $\overline{CLKB}$ (LVPECL differential signals)									
V _{PP}	Differential input voltage ^a V _{CC} =3.3V V _{CC} =2.5V	0.10 0.15		0.10 0.15		0.10 0.15		V V	
V _{CMR}	Differential cross point voltage ^b CLKA, CLKB	1.0	V _{CC} -0.4	1.0	V _{CC} -0.4	1.0	V _{CC} -0.4	V	
All inputs (LVPECL single ended signals)									
V _{IH}	Input high voltage	V _{CC} -1.14		V _{CC} -1.14		V _{CC} -1.14		V	
V _{IL}	Input low voltage		V _{CC} -1.46		V _{CC} -1.46		V _{CC} -1.46	V	
I _{IH}	Input Current		150		150		150	μA	V _{IN} = V _{CC} to V _{EE}
LVPECL clock outputs (Q0-19, $\overline{Q0-19}$)									
V _{OH}	Output High Voltage	V _{CC} -1.20	V _{CC} -0.82	V _{CC} -1.15	V _{CC} -0.82	V _{CC} -1.15	V _{CC} -0.82	V	I _{OH} = -30mA ^c
V _{OL}	Output Low Voltage	V _{CC} -1.90	V _{CC} -1.40	V _{CC} -1.90	V _{CC} -1.40	V _{CC} -1.9	V _{CC} -1.40	V	I _{OL} = -5mA ^c
Supply current and V _{BB}									
I _{EE}	Max. Supply Current		190		190		190	mA	V _{EE} pin
I _{CC}	Max. Supply Current ^d		750		750		750	mA	V _{CC} pins
V _{BB}	Output reference voltage ^e	V _{CC} -1.36	V _{CC} -1.24	V _{CC} -1.36	V _{CC} -1.24	V _{CC} -1.36	V _{CC} -1.24	V	

a. V_{PP} is the minimum differential input voltage swing required to maintain device functionality.

b. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

c. Equivalent to an output termination of 50Ω to V_{TT} .

d. I_{CC} includes current through the output resistors (all outputs terminated 50Ω to V_{TT}).

e. V_{BB} output can be used to bias the complementary input when the device is used with single ended clock signals. V_{BB} can sink max. 0.3 mA DC current.

Table 5: ECL DC Characteristics ($V_{CC} = V_{CCO} = GND$, $V_{EE} = -3.8V$ to $-2.375V$)

Symbol	Characteristics	T _A = -40°C		T _A = 25°C		T _A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
Clock input pair CLKA, $\overline{CLKA}$, CLKB, $\overline{CLKB}$ for ECL differential signals									
V _{PP}	Differential input voltage ^a V _{EE} =-3.3V V _{EE} =-2.5V	0.10 0.15		0.10 0.15		0.10 0.15		V V	
V _{CMR}	Differential cross point voltage ^b	V _{EE} +1.0	-0.4	V _{EE} +1.0	-0.4	V _{EE} +1.0	-0.4	V	
All inputs ECL single ended signals									
V _{IH}	Input high voltage	-1.14		-1.14		-1.14		V	
V _{IL}	Input low voltage		-1.46		-1.46		-1.46	V	
I _{IH}	Input Current		150		150		150	μA	V _{IN} = V _{EE} to V _{CC}
LVPECL clock outputs (Q0-19, $\overline{Q0-19}$)									
V _{OH}	Output High Voltage	-1.20	-0.82	-1.15	-0.82	-1.15	-0.82	V	I _{OH} = -30 mA ^c
V _{OL}	Output Low Voltage	-1.90	-1.40	-1.90	-1.40	-1.90	-1.40	V	I _{OL} = -5 mA ^c
Supply current and V _{BB}									
I _{EE}	Max. Supply Current		190		190		190	mA	V _{EE} pin
I _{CC}	Max. Supply Current ^d		750		750		750	mA	V _{CC} Pins
V _{BB}	Output reference voltage ^e	-1.36	-1.24	-1.36	-1.24	-1.36	-1.24	V	

a. V_{PP} is the minimum differential input voltage swing required to maintain device functionality.

b. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

c. Equivalent to an output termination of 50Ω to V_{TT} .

d. I_{CC} includes current through the output resistors (all outputs terminated 50Ω to V_{TT}).

e. V_{BB} output can be used to bias the complementary input when the device is used with single ended clock signals. V_{BB} can sink max. 0.3 mA DC current.

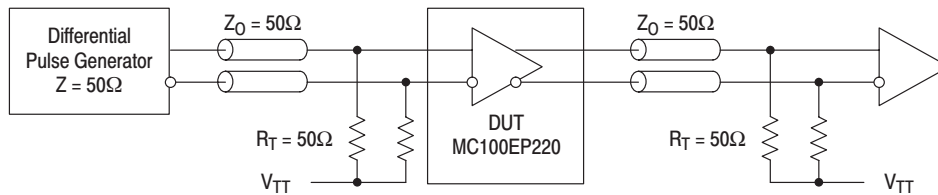
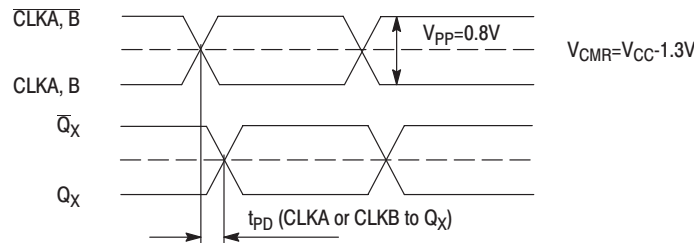
Table 6: PECL/ECL AC Characteristics^a ($V_{CC} = V_{CCO} = 2.375V$ to $3.8V$, $V_{EE} = GND$) or ($V_{EE} = -3.8V$ to $-2.375V$, $V_{CC} = V_{CCO} = GND$)

Symbol	Characteristics	T _A = -40°C			T _A = 25°C			T _A = 85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Clock input pair CLKA, $\overline{CLKA}$, CLKB, $\overline{CLKB}$ for PECL differential signals												
V _{PP}	Differential input voltage ^b (peak-to-peak)	0.4		1.0	0.4		1.0	0.4		1.0	V	
V _{CMR}	Differential cross point voltage ^c	1.0		V _{CC} -0.4	1.0		V _{CC} -0.4	1.0		V _{CC} -0.4	V	
f _{CLK}	Input Frequency (PECL)	0		1.0	0		1.0	0		1.0	GHz	
Clock input pair CLKA, $\overline{CLKA}$, CLKB, $\overline{CLKB}$ for ECL differential signals												
V _{PP}	Differential input voltage (peak-to-peak)	0.4		1.0	0.4		1.0	0.4		1.0	V	
V _{CMR}	Differential cross point voltage	V _{EE} +1.0		-0.4	V _{EE} +1.0		-0.4	V _{EE} +1.0		-0.4	V	
f _{CLK}	Input Frequency (ECL)	0		1.0	0		1.0	0		1.0	GHz	
PECL/ECL clock outputs (Q0-19, $\overline{Q0-19}$)												
t _{PD}	Propagation Delay CLKA or CLKB to Qx	300	400	500	350	450	550	425	535	650	ps	
V _{O(P-P)}	Differential output voltage (peak-to-peak)	450	700		500	700		500	700		mV	
t _{sk(O)}	Output-to-output skew (within device)		35	60		35	60		35	60	ps	Diff.
t _{sk(PP)}	Output-to-output skew (part-to-part)			200			200			225	ps	Diff.
t _{JIT(CC)}	Output cycle-to-cycle jitter (RMS)			TBD			TBD			TBD	ps	
DC _O	Positive output pulse width	t _p – 50	t _p	t _p + 50	t _p – 50	t _p	t _p + 50	t _p – 50	t _p	t _p + 50	ps	t _p input positive pulse width
t _r t _f	Output Rise/Fall Time	100		500	100		500	100		500	ps	20% to 80%

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b. V_{PP} (AC) is the minimum differential input voltage swing required to maintain AC characteristics including t_{pd} and device-to-device skew.

c. V_{CMR} (AC) is the crosspoint of the differential input signal. AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay and part-to-part skew.

**Figure 1. MC100EP220 AC test reference****Figure 2. MC100EP220 AC reference measurement waveform**

APPLICATIONS INFORMATION

Using the thermally enhanced package of the MC100EP220

The MC100EP220 uses a thermally enhanced exposed pad (EP) 52 lead LQFP package. The package is molded so that the leadframe is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance that supports the power consumption of the MC100EP220 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100EP220. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is the absolute minimum requirement for MC100EP220 applications on multi-layer boards. The recommended thermal land design comprises a 5 x 5 thermal via array as shown in Figure 3 "Recommended thermal land pattern", providing an efficient heat removal path.

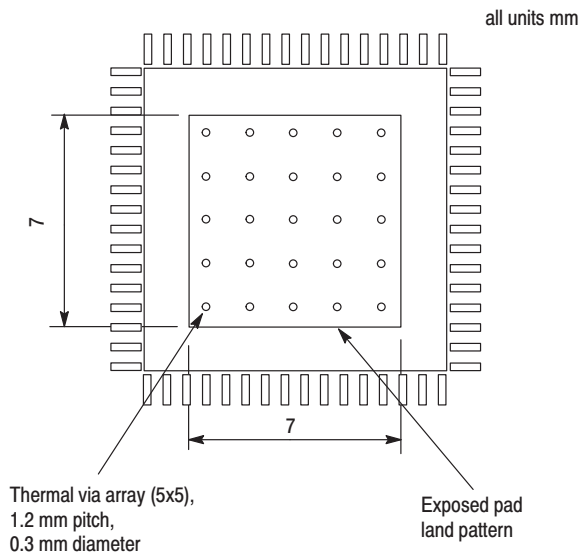


Figure 3. Recommended thermal land pattern

The via diameter is should be approx. 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. Figure 4 "Recommended solder mask openings" shows a recommend solder mask opening with respect to the recommended 5 x 5 thermal via

array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as shown in Figure 4. For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

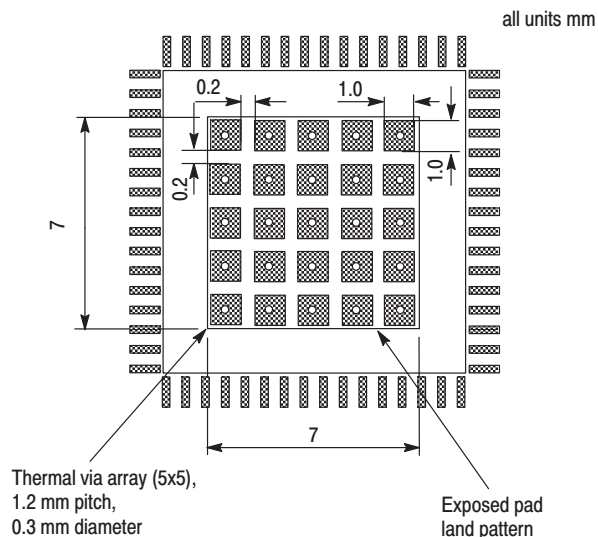


Figure 4. Recommended solder mask openings

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided. For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

Table 7: Thermal Resistance^a

Convection-LFPM	R _{THJA} ^b °C/W	R _{THJA} ^c °C/W	R _{THJC} ^d °C/W	R _{THJB} ^e °C/W
Natural	57.1	24.9	15.8	9.7
100	50.0	21.3		
200	46.9	20.0		
400	43.4	18.7		
800	38.6	16.9		

- Thermal data pattern with a 3 x 3 thermal via array on 2S2P boards (based on empirical results)
- Junction to ambient, single layer test board, per JESD51-6
- Junction to ambient, four conductor layer test board (2S2P), per JES51-6
- Junction to case, per MIL-SPEC 883E, method 1012.1
- Junction to board, four conductor layer test board (2S2P) per JESD 51-8

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100EP220 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.

Low-Voltage 1:20 Differential ECL/PECL Clock Driver

The MC100EP221 is a low skew 1-to-20 differential driver, designed with clock distribution in mind. It accepts two clock sources into an input multiplexer. The input signals can be either differential or single-ended if the V_{BB} output is used. The selected signal is fanned out to 20 identical differential outputs.

- 270ps max. Part-to-Part Skew
- 50ps max. Output-to-Output Skew
- Differential Design
- V_{BB} Output
- Voltage and Temperature Compensated Outputs
- Supports 3.3V and 2.5V, ECL and PECL Operation
- Supports HSTL and PECL Clock Systems

The EP221 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate-to-gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

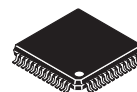
To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω , even if only one side is being used. In most applications, all ten differential pairs will be used and therefore terminated. In the case where fewer than ten pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The MC100EP221, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the EP221 to be used for high performance clock distribution in +3.3V or +2.5V systems. Designers can take advantage of the EP221's performance to distribute low skew clocks across the backplane. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies.

MC100EP221

See Upgrade Product – MC100ES6221

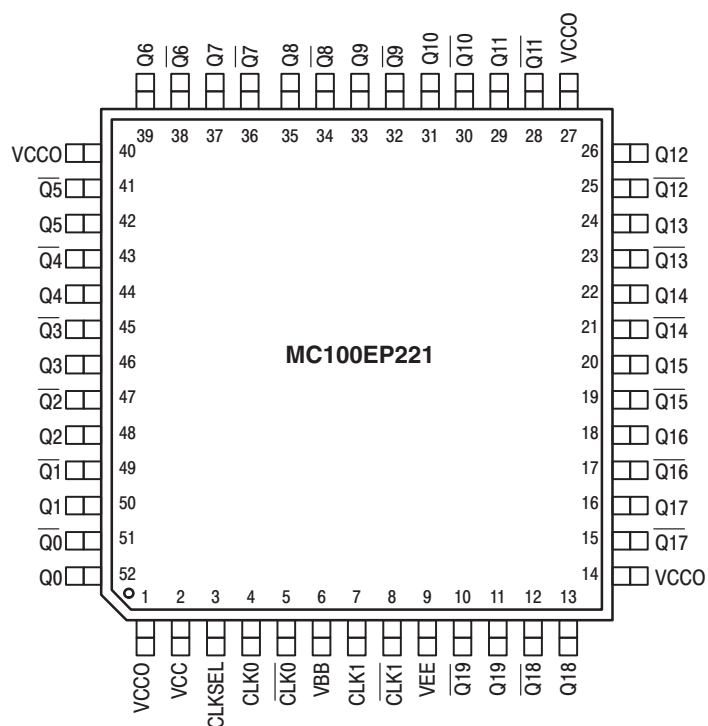
LOW-VOLTAGE 1:20 DIFFERENTIAL ECL/PECL CLOCK DRIVER



TB SUFFIX
52-LEAD LQFP PACKAGE
EXPOSED PAD
CASE 1336

6

Pinout: 52-Lead LQFP
(Top View)



FUNCTION

CLK_SEL	Active Input
0	CLK0, $\overline{\text{CLK0}}$
1	CLK1, $\overline{\text{CLK1}}$

LOGIC SYMBOL

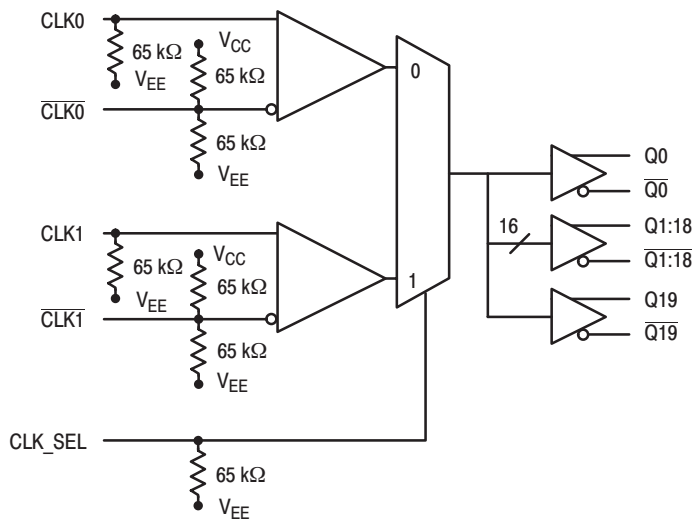


Table 1: PIN CONFIGURATION

Pin	I/O	Type	Function
CLK0, $\overline{\text{CLK0}}$	Input	ECL/LVPECL	Differential reference clock signal input
CLK1, $\overline{\text{CLK1}}$	Input	ECL/LVPECL or HSTL	Alternative differential reference clock signal input
CLK_SEL	Input	LVPECL	Output frequency divider select
Q[0-19], $\overline{\text{Q}}[0-19]$	Output	LVPECL	Differential clock outputs
VEE ^a	Supply		Negative power supply
V _{CC} , V _{CCO}	Supply		Positive power supply. All V _{CC} and V _{CCO} pins must be connected to the positive power supply for correct DC and AC operation
VBB	Output		DC bias output for single ended input operation

- a. In ECL mode (negative power supply mode), VEE is either -3.3V or -2.5V and VCC is connected to GND (0V).
 In PECL mode (positive power supply mode), VEE is connected to GND (0V) and VCC is either +3.3V or +2.5V.
 In both modes, the input and output levels are referenced to the most positive supply (VCC).

Table 2: ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	4.6	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} +0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} +0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage temperature	-65	125	°C	

- a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3: GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output termination voltage		V _{CC} - 2 ^a		V	
MM	ESD Protection (Machine model)	75			V	
HBM	ESD Protection (Human body model)	1500			V	
CDM	ESD Protection (Charged device model)	500			V	
LU	Latch-up immunity	200			mA	
C _{IN}			4.0		pF	Inputs
θ _{JA}	Thermal resistance junction to ambient	See application information ^b				
θ _{JC}	Thermal resistance junction to case	See application information				

- a. Output termination voltage V_{TT} = 0V for V_{CC}=2.5V operation is supported but the power consumption of the device will increase.
 b. Proper thermal management is critical for reliable system operation. This especially true for high-fanout and high drive capability products. Thermal package information and exposed pad land pattern design recommendations are available in the applications section of this data-sheet. In addition, the means of calculating die power consumption, the corresponding die temperature and the relationship to long-term reliability is addressed in the Motorola application note AN1545. Thermal modeling is recommended for the MC100EP221.

Table 4: PECL and HSTL DC Characteristics ($V_{CC0} = V_{CC} = 2.375V$ to $3.8V$, $V_{EE} = GND$)

Symbol	Characteristics	T _A = -40°C		T _A = 25°C		T _A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
Clock input pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}^a$ (LVPECL differential signals)									
V _{PP}	Differential input voltage ^b V _{CC} =3.3V V _{CC} =2.5V	0.10 0.15		0.10 0.15		0.10 0.15		V V	
V _{CMR}	Differential cross point voltage ^c CLK0 CLK1	1.0 0.1	V _{CC} -0.4 V _{CC} -1.0	1.0 0.1	V _{CC} -0.4 V _{CC} -1.0	1.0 0.1	V _{CC} -0.4 V _{CC} -1.0	V V	
Clock input pair CLK1, $\overline{CLK1}^d$ (HSTL differential signals)									
V _{DIF}	Differential input voltage ^e V _{CC} =3.3V V _{CC} =2.5V	0.4 0.4	1.0 1.0	0.4 0.4	1.0 1.0	0.4 0.4	1.0 1.0	V V	
V _X	Differential cross point voltage ^f	0.68	0.9	0.68	0.9	0.68	0.9	V	
V _{IH}	Input high voltage	V _X +0.2	V _X +0.5	V _X +0.2	V _X +0.5	V _X +0.2	V _X +0.5	V	
V _{IL}	Input low voltage	V _X -0.5	V _X -0.2	V _X -0.5	V _X -0.2	V _X -0.5	V _X -0.2	V	
All inputs (LVPECL single ended signals)									
V _{IH}	Input high voltage	V _{CC} -1.165	V _{CC} -0.880	V _{CC} -1.165	V _{CC} -0.880	V _{CC} -1.165	V _{CC} -0.880	V	
V _{IL}	Input low voltage	V _{CC} -1.810	V _{CC} -1.480	V _{CC} -1.810	V _{CC} -1.480	V _{CC} -1.810	V _{CC} -1.480	V	
I _{IH}	Input Current		150		150		150	μA	V _{IN} = V _{CC} to V _{EE}
LVPECL clock outputs (Q0-19, $\overline{Q0-19}$)									
V _{OH}	Output High Voltage	V _{CC} -1.20	V _{CC} -0.82	V _{CC} -1.15	V _{CC} -0.82	V _{CC} -1.15	V _{CC} -0.82	V	I _{OH} = -30mA ^g
V _{OL}	Output Low Voltage	V _{CC} -1.90	V _{CC} -1.40	V _{CC} -1.90	V _{CC} -1.40	V _{CC} -1.9	V _{CC} -1.40	V	I _{OL} = -5mA ^g
Supply current and V _{BB}									
I _{EE}	Max. Supply Current		190		190		190	mA	V _{EE} pin
I _{CC}	Max. Supply Current ^h		750		750		750	mA	V _{CC} pins
V _{BB}	Output reference voltage ⁱ V _{CC} =3.3V V _{CC} =2.5V	V _{CC} -1.35 V _{CC} -1.35	V _{CC} -1.24 V _{CC} -1.24	V _{CC} -1.35 V _{CC} -1.35	V _{CC} -1.24 V _{CC} -1.22	V _{CC} -1.35 V _{CC} -1.35	V _{CC} -1.24 V _{CC} -1.22	V V	

- a. The input pairs CLK0, CLK1 are compatible to differential signaling standards. CLK0 is compatible to LVPECL signals and CLK1 meets both HSTL and LVPECL differential signal specifications. The difference between CLK0 and CLK1 is the differential input threshold voltage (V_{CMR}).
- b. V_{PP} is the minimum differential input voltage swing required to maintain device functionality.
- c. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
- d. Clock inputs driven by differential HSTL compatible signals. Only applicable to CLK1, $\overline{CLK1}$.
- e. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality. Only applicable to CLK1, $\overline{CLK1}$.
- f. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
- g. Equivalent to an output termination of 50Ω to V_{TT} .
- h. I_{CC} includes current through the output resistors (all outputs terminated 50Ω to V_{TT}).
- i. V_{BB} output can be used to bias the complementary input when the device is used with single ended clock signals. V_{BB} can sink max. 0.3 mA DC current.

Table 5: ECL DC Characteristics ($V_{CC} = V_{CCO} = \text{GND}$, $V_{EE} = -3.8\text{V}$ to -2.375V)

Symbol	Characteristics	T _A = -40°C		T _A = 25°C		T _A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
Clock input pair CLK0, $\overline{\text{CLK0}}$, CLK1, $\overline{\text{CLK1}}$ ^a for ECL differential signals									
V _{PP}	Differential input voltage ^b V _{EE} =-3.3V V _{EE} =-2.5V	0.10 0.15		0.10 0.15		0.10 0.15		V V	
V _{CMR}	Differential cross point voltage ^c CLK0 CLK1	V _{EE} +1.0 V _{EE} +0.1	-0.4 -1.0	V _{EE} +1.0 V _{EE} +0.1	-0.4 -1.0	V _{EE} +1.0 V _{EE} +0.1	-0.4 -1.0	V V	
All inputs ECL single ended signals									
V _{IH}	Input high voltage	-1.165	-0.880	-1.165	-0.880	-1.165	-0.880	V	
V _{IL}	Input low voltage	-1.810	-1.480	-1.810	-1.480	-1.810	-1.480	V	
I _{IH}	Input Current		150		150		150	μA	V _{IN} = V _{EE} to V _{CC}
LVPECL clock outputs (Q0-19, $\overline{\text{Q0-19}}$)									
V _{OH}	Output High Voltage	-1.20	-0.82	-1.20	-0.82	-1.20	-0.82	V	I _{OH} = -30 mA ^d
V _{OL}	Output Low Voltage	-1.90	-1.40	-1.90	-1.40	-1.90	-1.40	V	I _{OL} = -5 mA ^d
Supply current and V _{BB}									
I _{EE}	Max. Supply Current		190		190		190	mA	V _{EE} pin
I _{CC}	Max. Supply Current ^e		750		750		750	mA	V _{CC} Pins
V _{BB}	Output reference voltage ^f V _{EE} =-3.3V V _{EE} =-2.5V	-1.35 -1.35	-1.24 -1.24	-1.35 -1.35	-1.24 -1.22	-1.35 -1.35	-1.24 -1.22	V V	

- a. The input pairs CLK0, CLK1 are compatible to differential signaling standards such as ECL. The difference between CLK0 and CLK1 is the differential input threshold voltage (V_{CMR}).
- b. V_{PP} is the minimum differential input voltage swing required to maintain device functionality.
- c. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
- d. Equivalent to an output termination of 50Ω to V_{TT} .
- e. I_{CC} includes current through the output resistors (all outputs terminated 50Ω to V_{TT}).
- f. V_{BB} output can be used to bias the complementary input when the device is used with single ended clock signals. V_{BB} can sink max. 0.3 mA DC current.

Table 6: PECL/ECL/HSTL AC Characteristics^a ($V_{CC} = V_{CCO} = 2.375V$ to $3.8V$, $V_{EE} = GND$) or ($V_{EE} = -3.8V$ to $-2.375V$, $V_{CC} = V_{CCO} = GND$)

Symbol	Characteristics	T _A = -40°C			T _A = 25°C			T _A = 85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Clock input pair CLK0, $\overline{\text{CLK0}}$, CLK1, $\overline{\text{CLK1}}$ ^b for PECL differential signals												
V _{PP}	Differential input voltage ^c (peak-to-peak)	0.5		1.0	0.5		1.0	0.5		1.0	V	
V _{CMR}	Differential cross point voltage ^d CLK0 CLK1	1.0 0.3		V _{CC} -0.4 V _{CC} -1.3	1.0 0.3		V _{CC} -0.4 V _{CC} -1.3	1.0 0.3		V _{CC} -0.4 V _{CC} -1.3	V V	
f _{CLK}	Input Frequency (PECL)	0		1.0			1.0			1.0	GHz	
Clock input pair CLK0, $\overline{\text{CLK0}}$, CLK1, $\overline{\text{CLK1}}$ for ECL differential signals												
V _{PP}	Differential input voltage (peak-to-peak)	0.5		1.0	0.5		1.0	0.5		1.0	V	
V _{CMR}	Differential cross point voltage CLK0 CLK1	V _{EE} +1.0 V _{EE} +0.3		-0.4 -1.3	V _{EE} +1.0 V _{EE} +0.3		-0.4 -1.3	V _{EE} +1.0 V _{EE} +0.3		-0.4 -1.3	V V	
f _{CLK}	Input Frequency (ECL)	0		1.0			1.0			1.0	GHz	
Clock input pair CLK1, $\overline{\text{CLK1}}$ for HSTL differential signals												
V _{DIF}	Differential input voltage ^e (peak-to-peak) CLK1	0.4		1.0	0.5		1.0	0.5		1.0	V	
V _X	Differential cross point voltage ^f CLK1	0.68		0.9	0.68		0.9	0.68		0.9	V	
f _{CLK}	Input Frequency (HSTL)	0		1.0			1.0			1.0	GHz	
PECL/ECL clock outputs (Q0-19, $\overline{\text{Q0-19}}$)												
t _{PD}	Propagation Delay CLK ₀ to Qx CLK ₁ to Qx	350 370	460 500	600 640	390 440	520 570	660 710	480 530	630 680	750 800	ps ps	Diff. Diff.
V _{O(P-P)}	Differential output voltage (peak-to-peak) f _O < 50 MHz f _O < 0.8 GHz f _O < 1.0 GHz	450 400 375			550 500 400			550 500 400			mV mV mV	
t _{sk(O)}	Output-to-output skew (within device)		30	50		30	50		30	50	ps	Diff.
t _{sk(PP)}	Output-to-output skew (part-to-part)			270			270			270	ps	Diff.
t _{JIT(CC)}	Output cycle-to-cycle jitter (RMS)			TBD			TBD			TBD	ps	
DC _O	Output duty cycle	49.5	50	50.5	49.5	50	50.5	49.5	50	50.5	%	DC _{fref} = 50%
t _r , t _f	Output Rise/Fall Time	100		500	100		500	100		500	ps	20% to 80%

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b. The input pairs CLK0, CLK1 are compatible to differential signaling standards such as ECL. The difference between CLK0 and CLK1 is the differential input threshold voltage (V_{CMR}).

c. V_{PP} (AC) is the minimum differential input voltage swing required to maintain AC characteristics including t_{pd} and device-to-device skew.

d. V_{CMR} (AC) is the crosspoint of the differential input signal. AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay and part-to-part skew.

e. V_{DIF} (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics. Only applicable to CLK1.

f. V_X (AC) is the crosspoint of the differential HSTL input signal. AC operation is obtained when the crosspoint is within the V_X (AC) range and the input swing lies within the V_{DIF} (AC) specification. Violation of V_X (AC) or V_{DIF} (AC) impacts the device propagation delay and part-to-part skew.

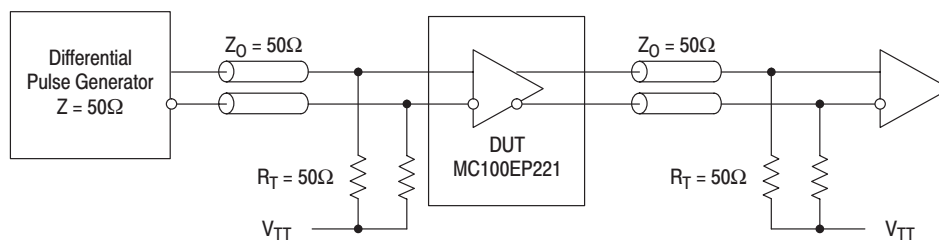


Figure 1. MC100EP221 AC test reference

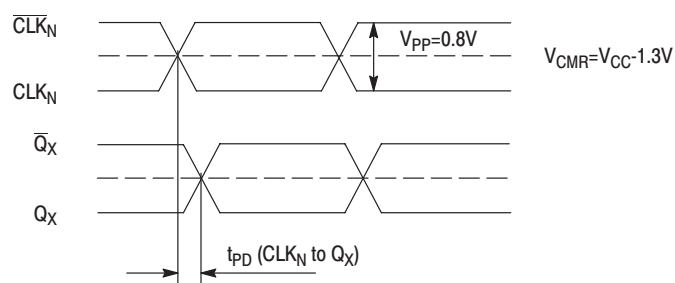


Figure 2. MC100EP221 AC reference measurement waveform

APPLICATIONS INFORMATION

Using the thermally enhanced package of the MC100EP221

The MC100EP221 uses a thermally enhanced exposed pad (EP) 52 lead LQFP package. The package is molded so that the leadframe is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance that supports the power consumption of the MC100EP221 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100EP221. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is the absolute minimum requirement for MC100EP221 applications on multi-layer boards. The recommended thermal land design comprises a 5 x 5 thermal via array as shown in Figure 3 "Recommended thermal land pattern", providing an efficient heat removal path.

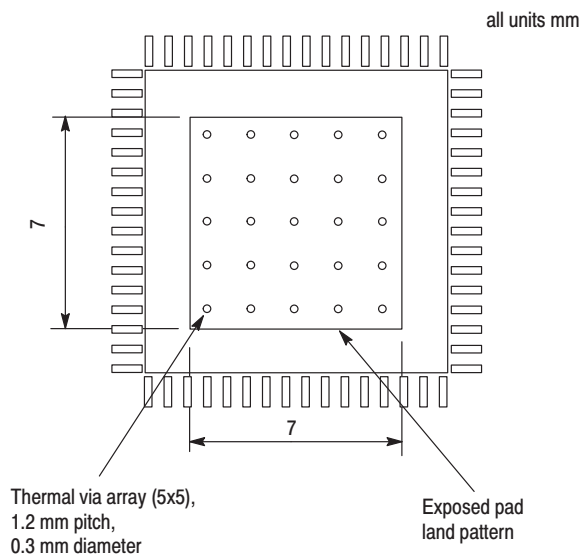


Figure 3. Recommended thermal land pattern

The via diameter is should be approx. 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. Figure 4 "Recommended solder mask openings" shows a recommend solder mask opening with respect to the recommended 5 x 5 thermal via

array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as shown in Figure 4. For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

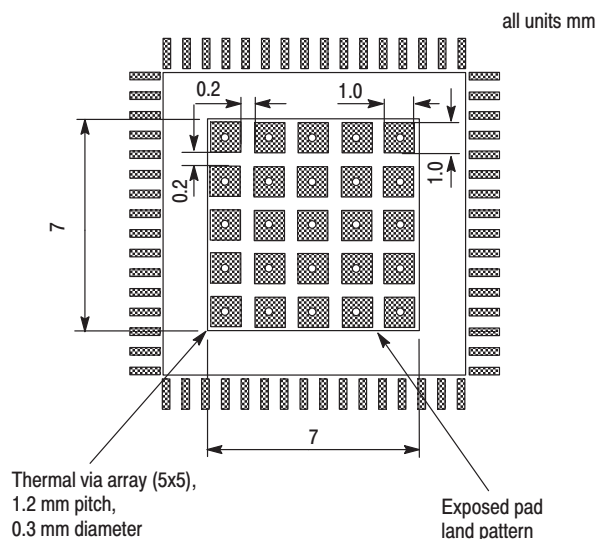


Figure 4. Recommended solder mask openings

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided. For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

Table 7: Thermal Resistance^a

Convection-LFPM	R_{THJA}^b °C/W	R_{THJA}^c °C/W	R_{THJC}^d °C/W	R_{THJB}^e °C/W
Natural	57.1	24.9	15.8	9.7
100	50.0	21.3		
200	46.9	20.0		
400	43.4	18.7		
800	38.6	16.9		

- Thermal data pattern with a 3 x 3 thermal via array on 2S2P boards (based on empirical results)
- Junction to ambient, single layer test board, per JESD51-6
- Junction to ambient, four conductor layer test board (2S2P), per JES51-6
- Junction to case, per MIL-SPEC 883E, method 1012.1
- Junction to board, four conductor layer test board (2S2P) per JESD 51-8

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100EP221 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.

Low Voltage ECL/PECL 1:15 Clock Driver

The MC100EP222 is a low voltage, low skew 1:15 differential $\div 1$ and $\div 2$ ECL/PECL clock distribution buffer. The MC100EP222 has been designed and optimized for 2.5 V and 3.3 V systems. Target applications for this clock driver are high performance clock distribution systems for computer, networking and telecommunication systems.

Features:

- 15 differential ECL outputs (4 output banks)
- 2 selectable differential ECL inputs
- Selectable 1:1 or 1:2 frequency outputs
- Operates from a -2.5, -3.3 V (ECL) or 2.5, 3.3 V (PECL) power supply
- Extended temperature operating range of -40 to +85 deg C

The MC100EP222 device characteristics allows low-skew clock distribution of differential and single-ended LVECL/LVPECL signals. Typical applications for the MC100EP222 are primary clock distribution systems on backplanes of high-performance computer, networking and telecommunication systems.

The MC100EP222 can be operated from a 3.3 V or 2.5 V positive supply (PECL mode) without the requirement of a negative supply line. Each of the four output banks of two, three, four and six differential clock output pairs may be independently configured to distribute the input frequency or $\div 2$ of the input frequency. The FSELA, FSELB, FSELC, FSELD and CLK_SEL are asynchronous control inputs. Any changes of the control inputs require a MR pulse for resynchronization of the $\div 2$ outputs. For the functionality of the MR control input, "Timing Diagram" on page 648.

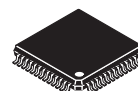
Each of the CLK0, CLK1 inputs can be used differential or single-ended. For single-ended signals, connect the bypassed V_{BB} output reference to the unused input of the pair.

The MC100EP222 guarantees low output-to-output skew of 40 (70) ps and device-to-device skew of max. 350 ps. To ensure low skew clock signals in the application, both sides of any differential output pair need to be terminated identically, even if only one side is used. When fewer than all fifteen pairs are used, identical termination of all output pairs on the same package side is recommended. If no outputs on a side are used, it is recommended to leave all of these outputs open and unterminated. This will maintain minimum output skew.

MC100EP222

See Upgrade Product – MC100ES6222

LOW VOLTAGE 3.3 V/2.5 V 1:15 DIFFERENTIAL ECL/PECL CLOCK DRIVER



TB SUFFIX
52-LEAD LQFP PACKAGE
EXPOSED PAD
CASE 1336

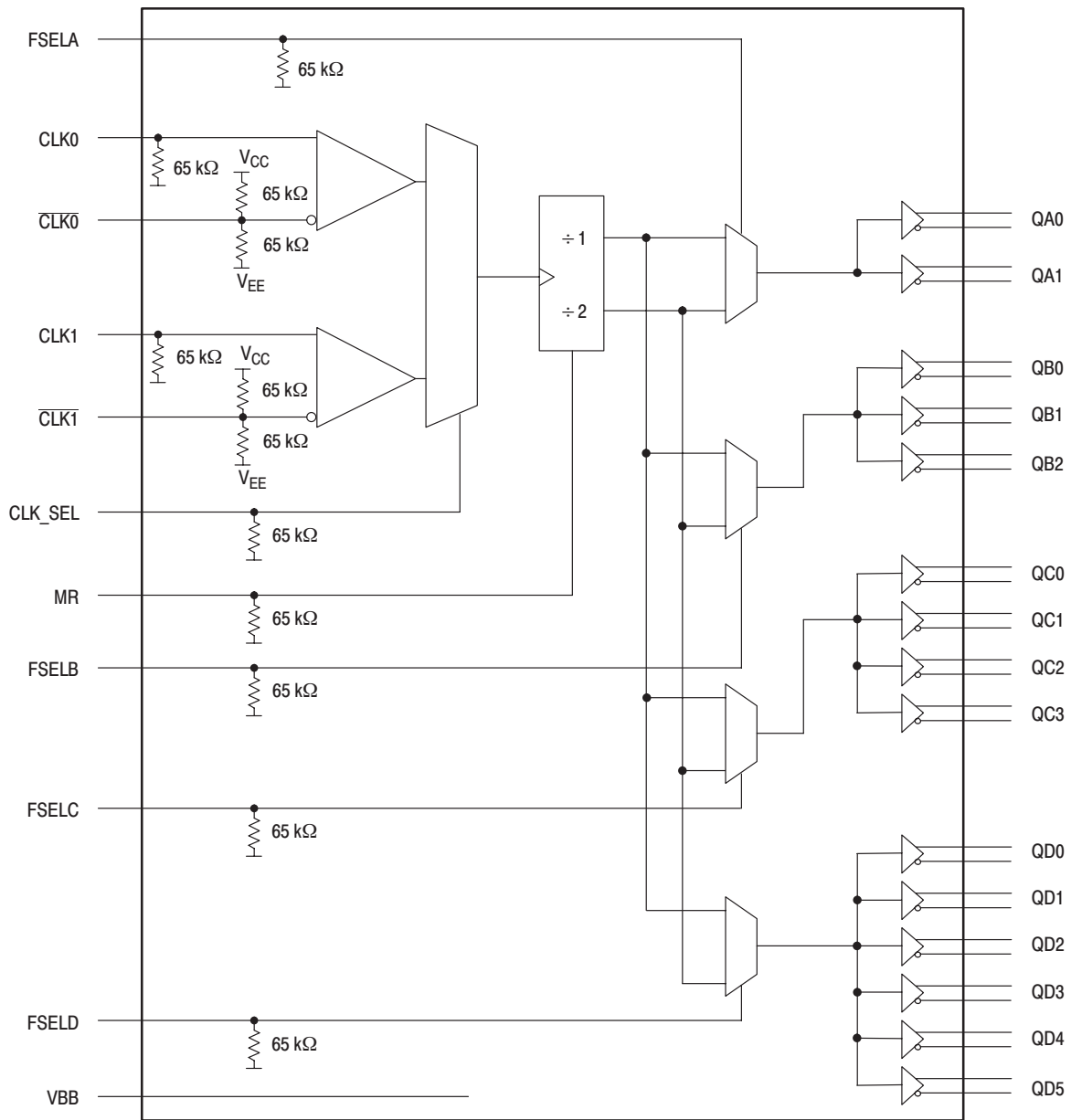


Figure 1. MC100EP222 Logic Diagram

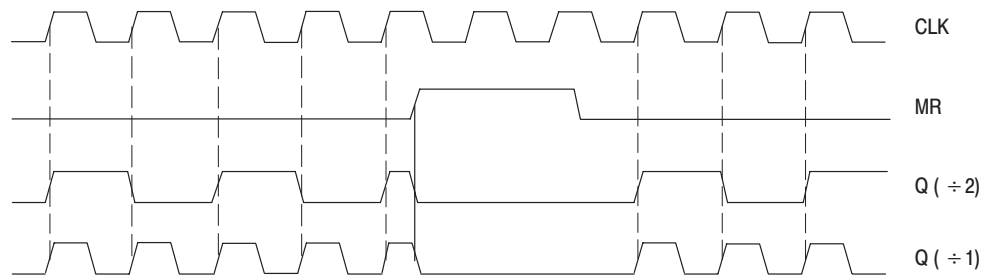


Figure 2. MC100EP222 Function Diagram

Figure 3. 52 Lead Package Pinout (Top View)

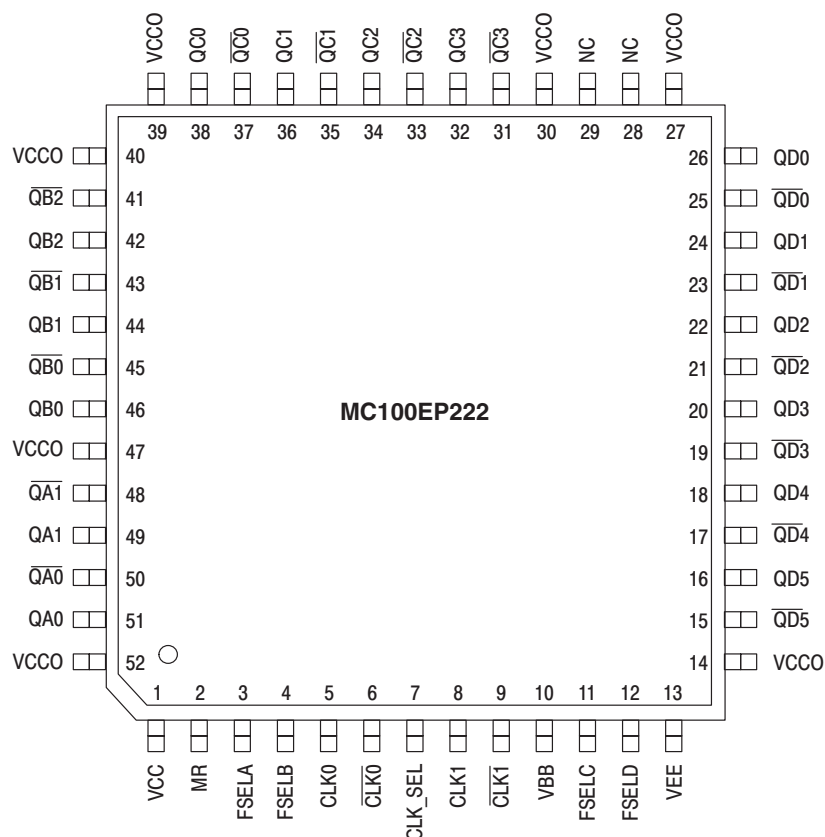


Table 1: FUNCTION TABLE

Control Pin	0	1
FSELA (asynchronous)	÷ 1	÷ 2
FSELB (asynchronous)	÷ 1	÷ 2
FSELC (asynchronous)	÷ 1	÷ 2
FSELD (asynchronous)	÷ 1	÷ 2
CLK_SEL (asynchronous)	CLK0	CLK1
MR (asynchronous)	Active	Reset

Table 2: PIN CONFIGURATION

Pin	I/O	Type	Description
CLK0, $\overline{\text{CLK0}}$	Input	ECL/PECL	Differential reference clock signal input
CLK1, $\overline{\text{CLK1}}$	Input	ECL/PECL	Alternative differential reference clock signal input
CLK_SEL	Input	ECL/PECL	Clock input select
QAn, $\overline{\text{QAn}}$	Output	ECL/PECL	Bank A differential outputs
QBn, $\overline{\text{QBn}}$	Output	ECL/PECL	Bank B differential outputs
QCn, $\overline{\text{QCn}}$	Output	ECL/PECL	Bank C differential outputs
QDn, $\overline{\text{QDn}}$	Output	ECL/PECL	Bank D differential outputs
FSELA	Input	ECL/PECL	Selection of bank A output frequency
FSELB	Input	ECL/PECL	Selection of bank B output frequency
FSELC	Input	ECL/PECL	Selection of bank C output frequency
FSELD	Input	ECL/PECL	Selection of bank D output frequency
MR	Input	ECL/PECL	Reset
VBB	Output		DC bias output for single ended input operation
VEE ^a	Supply		Negative power supply
V _{CC} , V _{CCO}	Supply		Positive power supply. All V _{CC} and V _{CCO} pins must be connected to the positive power supply for correct DC and AC operation

- a. In ECL mode (negative power supply mode), VEE is either -3.3V or -2.5V and VCC is connected to GND (0V).
 In PECL mode (positive power supply mode), VEE is connected to GND (0V) and VCC is either +3.3V or +2.5V.
 In both modes, the input and output levels are referenced to the most positive supply.

Table 3: ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	4.6	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} +0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} +0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage temperature	-65	125	°C	

- a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4: GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output termination voltage		V _{CC} - 2 ^a		V	
MM	ESD Protection (Machine model)	75			V	
HBM	ESD Protection (Human body model)	1500			V	
CDM	ESD Protection (Charged device model)	500			V	
LU	Latch-up immunity	200			mA	
C _{IN}			4.0		pF	Inputs
θ _{JA}	Thermal resistance junction to ambient	See application information ^b				
θ _{JC}	Thermal resistance junction to case	See application information				

- a. Output termination voltage V_{TT} = 0V for V_{CC}=2.5V operation is supported but the power consumption of the device will increase
 b. Proper thermal management is critical for reliable system operation. This especially true for high-fanout and high drive capability products. Thermal package information and exposed pad land pattern design recommendations are available in the applications section of this datasheet. In addition, the means of calculating die power consumption, the corresponding die temperature and the relationship to long-term reliability is addressed in the Motorola application note AN1545. Thermal modeling is recommended for the MC100EP222.

Table 5: PECL DC Characteristics ($V_{CC0} = V_{CC} = 2.375\text{ V to }3.8\text{ V}$, $V_{EE} = \text{GND}$)

Symbol	Characteristics	T _A = -40°C		T _A = 25°C		T _A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
Clock input pairs CLK0, $\overline{\text{CLK0}}$, CLK1, $\overline{\text{CLK1}}$ (LVPECL differential signals)									
V _{PP}	Differential input voltage ^a V _{CC} =3.3 V V _{CC} =2.5 V	0.10 0.15		0.10 0.15		0.10 0.15		V V	
V _{CMR}	Differential cross point voltage ^b CLK0,CLK1	1.0	V _{CC} -0.4	1.0	V _{CC} -0.4	1.0	V _{CC} -0.4	V	
I _{IH}	Input Current		150		150		150	μA	V _{IN} = V _{CC} to V _{EE}
Control inputs (LVPECL single ended)									
V _{IH}	Input high voltage	V _{CC} -1.165	V _{CC} -0.880	V _{CC} -1.165	V _{CC} -0.880	V _{CC} -1.165	V _{CC} -0.880	V	
V _{IL}	Input low voltage	V _{CC} -1.810	V _{CC} -1.480	V _{CC} -1.810	V _{CC} -1.480	V _{CC} -1.810	V _{CC} -1.480	V	
I _{IH}	Input Current		150		150		150	μA	V _{IN} = V _{CC} to V _{EE}
LVPECL clock outputs (QAn, $\overline{\text{QAn}}$, QBn, $\overline{\text{QBn}}$, QCn, $\overline{\text{QCn}}$, QDn, $\overline{\text{QDn}}$)									
V _{OH}	Output High Voltage	V _{CC} -1.20	V _{CC} -0.82	V _{CC} -1.15	V _{CC} -0.82	V _{CC} -1.15	V _{CC} -0.82	V	I _{OH} = -30mA ^c
V _{OL}	Output Low Voltage	V _{CC} -1.90	V _{CC} -1.40	V _{CC} -1.90	V _{CC} -1.40	V _{CC} -1.9	V _{CC} -1.40	V	I _{OL} = -5mA ^c
Supply current and V _{BB}									
I _{EE}	Max. Supply Current		190		190		190	mA	V _{EE} pin
I _{CC}	Max. Supply Current ^d		675		675		675	mA	V _{CC} pins
V _{BB}	Output reference voltage ^e V _{CC} =3.3 V V _{CC} =2.5 V	V _{CC} -1.35 V _{CC} -1.35	V _{CC} -1.24 V _{CC} -1.24	V _{CC} -1.35 V _{CC} -1.35	V _{CC} -1.24 V _{CC} -1.22	V _{CC} -1.35 V _{CC} -1.35	V _{CC} -1.24 V _{CC} -1.22	V V	

a. V_{PP} is the minimum differential input voltage swing required to maintain device functionality.

b. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

c. Equivalent to an output termination of 50Ω to V_{TT} .

d. I_{CC} includes current through the output resistors (all outputs terminated 50Ω to V_{TT}).

e. V_{BB} output can be used to bias the complementary input when the device is used with single ended clock signals. V_{BB} can sink max. 0.3 mA DC current.

Table 6: ECL DC Characteristics ($V_{CC} = V_{CCO} = \text{GND}$, $V_{EE} = -3.8 \text{ V}$ to -2.375 V)

Symbol	Characteristics	T _A = -40°C		T _A = 25°C		T _A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
Clock input pairs CLK0, $\overline{\text{CLK0}}$, CLK1, $\overline{\text{CLK1}}$ (ECL differential signals)									
V _{PP}	Differential input voltage ^a V _{EE} =-3.3 V V _{EE} =-2.5 V	0.10 0.15		0.10 0.15		0.10 0.15		V V	
V _{CMR}	Differential cross point voltage ^b CLK0,CLK1	V _{EE} +1.0	-0.4	V _{EE} +1.0	-0.4	V _{EE} +1.0	-0.4	V	
I _{IH}	Input Current		150		150		150	μA	V _{IN} = V _{EE} to V _{CC}
All inputs ECL single ended signals									
V _{IH}	Input high voltage	-1.165	-0.880	-1.165	-0.880	-1.165	-0.880	V	
V _{IL}	Input low voltage	-1.810	-1.480	-1.810	-1.480	-1.810	-1.480	V	
I _{IH}	Input Current		150		150		150	μA	V _{IN} = V _{EE} to V _{CC}
LVPECL clock outputs (Q0-19, $\overline{\text{Q0-19}}$)									
V _{OH}	Output High Voltage	-1.20	-0.82	-1.20	-0.82	-1.20	-0.82	V	I _{OH} = -30 mA ^c
V _{OL}	Output Low Voltage	-1.90	-1.40	-1.90	-1.40	-1.90	-1.40	V	I _{OL} = -5 mA ^c
Supply current and V _{BB}									
I _{EE}	Max. Supply Current		190		190		190	mA	V _{EE} pin
I _{CC}	Max. Supply Current ^d		750		750		750	mA	V _{CC} Pins
V _{BB}	Output reference voltage ^e V _{EE} =-3.3 V V _{EE} =-2.5 V	-1.35 -1.35	-1.24 -1.24	-1.35 -1.35	-1.24 -1.22	-1.35 -1.35	-1.24 -1.22	V V	

- a. V_{PP} is the minimum differential input voltage swing required to maintain device functionality.
- b. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
- c. Equivalent to an output termination of 50Ω to V_{TT} .
- d. I_{CC} includes current through the output resistors (all outputs terminated 50Ω to V_{TT}).
- e. V_{BB} output can be used to bias the complementary input when the device is used with single ended clock signals. V_{BB} can sink max. 0.3 mA DC current.

Table 7: ECL AC Characteristics^a ($V_{CC} = V_{CCO} = 2.375 \text{ V to } 3.8 \text{ V}$, $V_{EE} = \text{GND}$) or ($V_{EE} = -3.8 \text{ V to } -2.375 \text{ V}$, $V_{CC} = V_{CCO} = \text{GND}$)

Symbol	Characteristics	T _A = -40°C			T _A = 25°C			T _A = 85°C			Unit	Condi- tion
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Clock input pair CLK0, $\overline{\text{CLK0}}$, CLK1, $\overline{\text{CLK1}}$ (PECL/ECL differential signals)												
V _{PP}	Differential input voltage ^b (peak-to-peak) CLK0, CLK1	0.5		1.0	0.5		1.0	0.5		1.0	V	
V _{CMR}	Differential cross point voltage ^c											
	PECL mode CLK0, CLK1	V _{EE} +1.0		-0.4	V _{EE} +1.0		-0.4	V _{EE} +1.0		-0.4	V	
	ECL mode CLK0, CLK1	1.0		V _{CC} -0.4	1.0		V _{CC} -0.4	1.0		V _{CC} -0.4	V	
f _{CLK}	Input Frequency	0		1.0	0		1.0	0		1.0	GHz	
PECL/ECL clock outputs (QAn, $\overline{\text{QAn}}$, QBn, $\overline{\text{QBn}}$, QCn, $\overline{\text{QCn}}$, QDn, $\overline{\text{QDn}}$)												
t _{PD}	Propagation Delay CLK _N to Qx MR to Qx	560	730	910 TBD	640	790	940 TBD	740	890	1040 TBD	ps ps	Diff.
V _{O(P-P)}	Differential output voltage (peak-to-peak) f _O < 100 MHz	450			550			550			mV	
	f _O < 0.5 GHz	400			500			500			mV	
	f _O < 1.0 GHz	375			400			400			mV	
t _{sk(O)}	Output-to-output skew within											Diff.
	- QA[0:1]			40			40			40	ps	
	- QB[0:2]			40			40			40	ps	
	- QC[0:3]			70			70			70	ps	
	- QD[0:5]			40			40			40	ps	
	- QA _N , QB _N , QD _N (single freq.)			60			60			60	ps	
	- all outputs (single freq.)			120			120			120	ps	
	- QA _N , QB _N , QD _N (multiple freq.)			130			130			130	ps	
- all outputs (multiple freq.)			150			150			150	ps		
t _{sk(PP)}	Output-to-output skew (part-to-part)			350			300			300	ps	Diff.
t _{JIT(CC)}	Output cycle-to-cycle jitter (RMS)			TBD			TBD			TBD	ps	
DC _O	Output duty cycle	49.5	50	50.5	49.5	50	50.5	49.5	50	50.5	%	DC _{ref} = 50%
t _r , t _f	Output Rise/Fall Time	100		500	100		500	100		500	ps	20% to 80%

- a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
- b. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including t_{pd} and device-to-device skew.
- c. V_{CMR} (AC) is the crosspoint of the differential input signal. AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay and part-to-part skew.

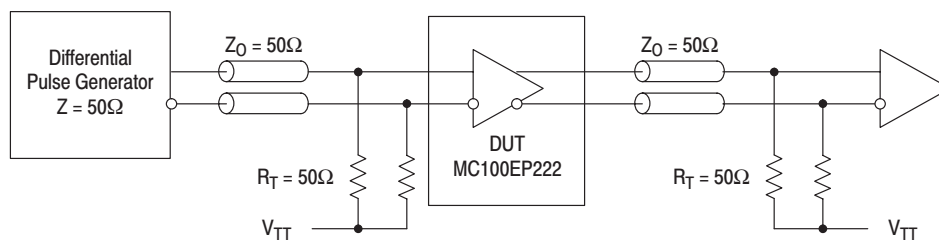
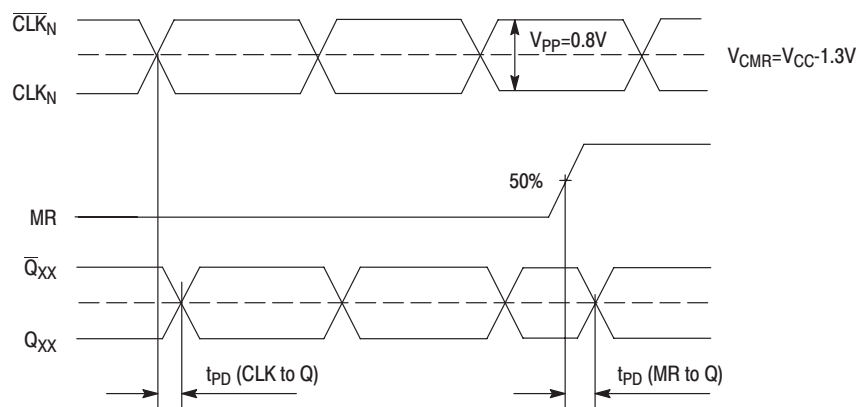


Figure 4. MC100EP222 AC test reference

Figure 5. MC100EP222 t_{PD} / AC reference measurement waveform

APPLICATIONS INFORMATION

Using the thermally enhanced package of the MC100EP222

The MC100EP222 uses a thermally enhanced exposed pad (EP) 52 lead LQFP package. The package is molded so that the leadframe is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance that supports the power consumption of the MC100EP222 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100EP222. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is the absolute minimum requirement for MC100EP222 applications on multi-layer boards. The recommended thermal land design comprises a 5 x 5 thermal via array as shown in Figure 6 "Recommended thermal land pattern", providing an efficient heat removal path.

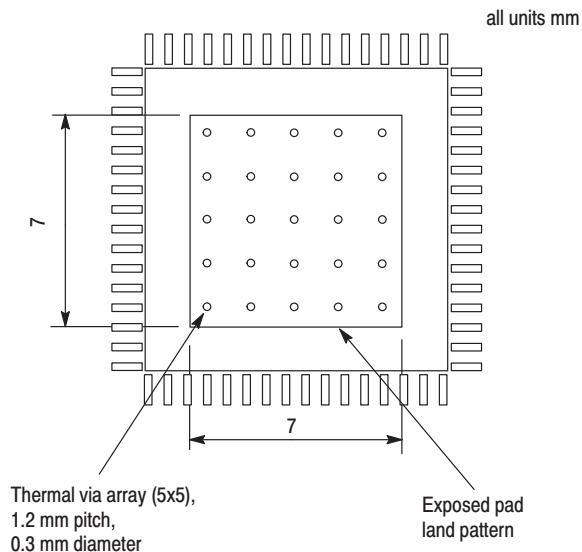


Figure 6. Recommended thermal land pattern

The via diameter is should be approx. 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. Figure 7 "Recommended solder mask openings" shows a recommend solder mask opening with respect to the recommended 5 x 5 thermal via

array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as shown in Figure 7 For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

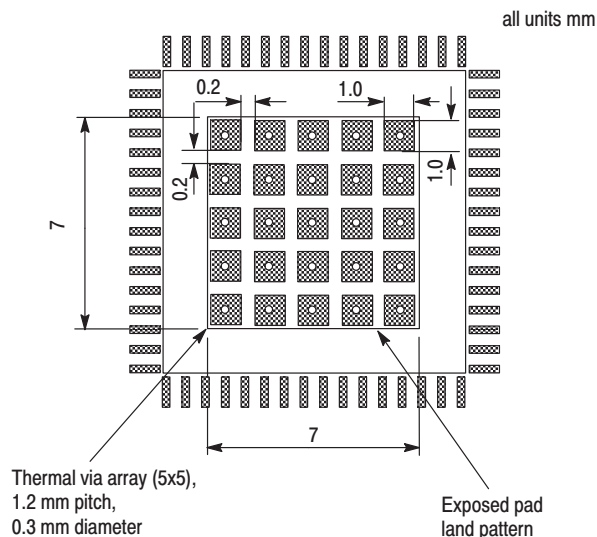


Figure 7. Recommended solder mask openings

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided. For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

Table 8: Thermal Resistance^a

Convection-LFPM	R_{THJA}^b °C/W	R_{THJA}^c °C/W	R_{THJC}^d °C/W	R_{THJB}^e °C/W
Natural	57.1	24.9	15.8	9.7
100	50.0	21.3		
200	46.9	20.0		
400	43.4	18.7		
800	38.6	16.9		

- Thermal data pattern with a 3 x 3 thermal via array on 2S2P boards (based on empirical results)
- Junction to ambient, single layer test board, per JESD51-6
- Junction to ambient, four conductor layer test board (2S2P), per JES51-6
- Junction to case, per MIL-SPEC 883E, method 1012.1
- Junction to board, four conductor layer test board (2S2P) per JESD 51-8

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100EP222 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.

Product Preview

Low-Voltage 1:22 Differential PECL/HSTL Clock Driver

The MC100EP223 is a low skew 1-to-22 differential driver, designed with clock distribution in mind. It accepts two clock sources into an input multiplexer. The selected signal is fanned out to 22 identical differential outputs.

- 200ps Part-to-Part Skew
- 50ps Output-to-Output Skew
- Differential Design
- Open Emitter HSTL Compatible Outputs
- 3.3V V_{CC}
- Both PECL and HSTL Inputs
- 75k Ω Input Pulldown Resistors
- Thermally Enhanced 64 lead Exposed Pad LQFP

The EP223 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate-to-gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

The EP223 HSTL outputs are not realized in the conventional manner. To minimize part-to-part and output-to-output skew, the HSTL compatible output levels are generated with an open emitter architecture. The outputs are pulled down with 50 Ω to ground, rather than the typical 50 Ω to V_{DDQ} pullup of a "standard" HSTL output. Because the HSTL outputs are pulled to ground, the EP223 does not utilize the V_{DDQ} supply of the HSTL standard. The output levels are derived from V_{CC} .

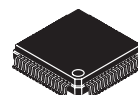
In the case of an asynchronous control, there is a chance of generating a 'run' clock pulse when the device is enabled/disabled. To avoid this, the output enable (OE) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50 Ω , even if only one side is being used. In most applications, all 22 differential pairs will be used and therefore terminated. In the case where fewer than 22 pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

MC100EP223

See Upgrade Product – MC100ES6223

LOW-VOLTAGE 1:22 DIFFERENTIAL PECL/HSTL CLOCK DRIVER



TC SUFFIX
64-LEAD LQFP PACKAGE
CASE 840K

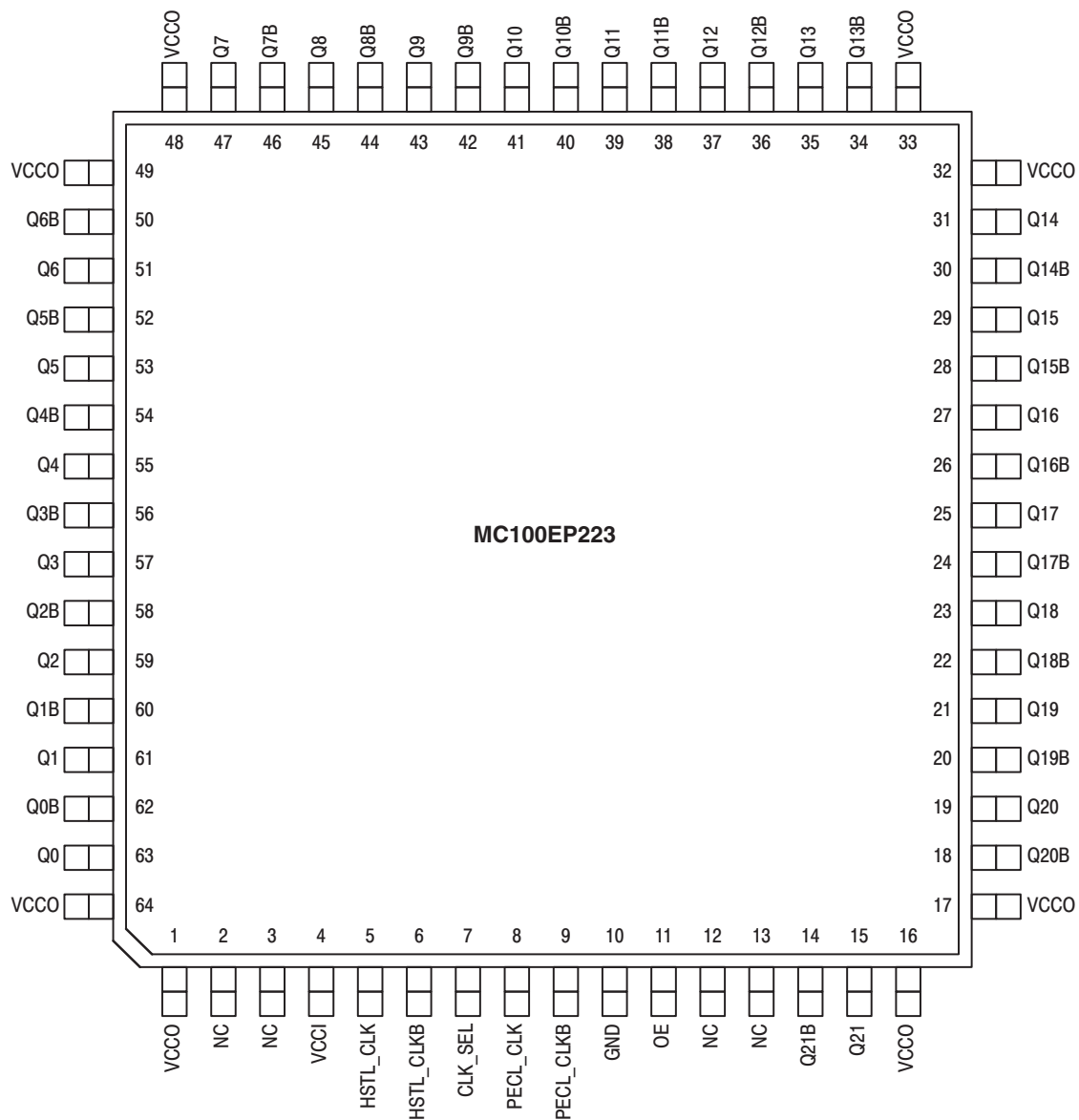


Figure 1. 64-Lead Pinout (Top View)

PIN NAMES

Pins	Function
HSTL_CLK, HSTL_CLKB	Differential HSTL Inputs
PECL_CLK, PECL_CLKB	Differential PECL Inputs
Q0:21, Q0B:21B	Differential HSTL Outputs
CLK_SEL	Active Clock Select Input
OE	Output Enable
GND	Ground
VCCI	Core VCC
VCCO	I/O VCC

FUNCTION

OE	CLK_SEL	Q0:21, Q0B:21B
0	0	Q = Low, QB = High
0	1	Q = Low, QB = High
1	0	HSTL_CLK, HSTL_CLKB
1	1	PECL_CLK, PECL_CLKB

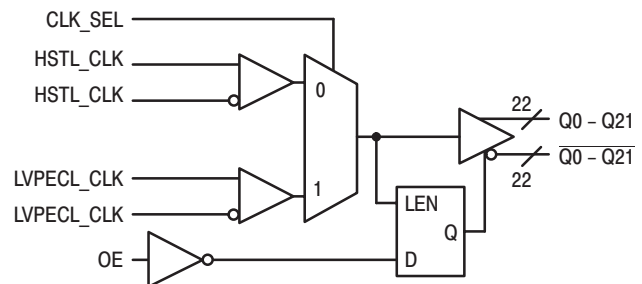


Figure 2. Logic Symbol

SIGNAL GROUPS

Level	Direction	Signal
HSTL	Input	HSTL_CLK, HSTL_CLKB
HSTL	Output	Q0:21, Q0B:21B
LVPECL	Input	PECL_CLK, PECL_CLKB
LVCMOS/LVTTL	Input	CLK_SEL, OE

HSTL DC CHARACTERISTICS

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage				1.0						V
V _{OL}	Output LOW Voltage						0.4				V
V _{IH}	Input HIGH Voltage				V _{CC} +0.1		1.6				V
V _{IL}	Input LOW Voltage				−0.3		V _{CC} −0.1				V
V _{CC}	Input Crossover Voltage				0.68		0.9				V

PECL DC CHARACTERISTICS

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{IH}	Input HIGH Voltage (Note 1.)	2.135		2.420	2.135		2.420	2.135		2.420	V
V _{IL}	Input LOW Voltage (Note 1.)	1.490		1.825	1.490		1.825	1.490		1.825	V
I _{IH}	Input HIGH Current			150			150			150	μA

1. These values are for V_{CC} = 3.3V. Level specifications vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{EE} = GND, V_{CC} = V_{CC(min)} to V_{CC(max)})

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _{PLH} , t _{PHL}	Propagation Delay to Output IN (Differential)		1.0			1.0			1.0		ns
t _{skew}	Within–Device Skew Part–to–Part Skew (Diff)			50 200			50 200			50 200	ps
f _{max}	Maximum Input Frequency			250			250			250	MHz
V _{PP}	Minimum Input Swing PECL_CLK		600			600			600		mV
V _{CMR}	Common Mode Range PECL_CLK										V
t _r , t _f	Output Rise/Fall Time (20–80%)	300		600	300		600	300		600	ps

Power Supply Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
V _{CCI}	Core V _{CC}	3.0	3.3	3.6	V
V _{CCO}	I/O V _{CC}	1.6	1.8	2.0	V
I _{CC}	Power Supply Current				mA
I _{EE}	Power Supply Current				mA

APPLICATIONS INFORMATION

Using the thermally enhanced package of the MC100EP223

The MC100EP223 uses a thermally enhanced 64 lead LQFP package. This package provides the low thermal impedance that supports the power consumption of the MC100EP223 high-speed bipolar integrated circuit and eases the power management task for the system design. An exposed pad at the bottom of the package establishes thermal conductivity from the package to the printed circuit board. In order to take advantage of the enhanced thermal capabilities of this package, it is recommended to solder the exposed pad of the package to the printed circuit board. The attachment process for exposed pad package is the same as for any standard surface mount package. Vias are recommended from the pad on the board down to an appropriate plane in the board that is capable of distributing the heat. In order to supply enough solder paste to fill those vias and not starve the solder joints, it may be required to stencil print solder paste onto the printed circuit pad. This pad should match the dimensions of the exposed pad. The dimensions of the exposed pad are shown on the package outline in this specification. For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

Thermal Resistance

Convection LFPM	R _{THJA} ^a °C/W	R _{THJA} ^b °C/W	R _{THJC} ^c °C/W	R _{THJB} ^d °C/W
Natural	57.1	24.9	15.8	9.7
100	50.0	21.3		
200	46.9	20.0		
400	43.4	18.7		
800	38.6	16.9		

- a. Junction to ambient, single layer test board, per JESD51-6
- b. Junction to ambient, four conductor layer test board (2S2P), per JES51-6
- c. Junction to case, per MIL-SPEC 883E, method 1012.1
- d. Junction to board, four conductor layer test board (2S2P) per JESD 51-8

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100EP223 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals.

Preliminary Information

2.5V / 3.3V ECL 1:2

Differential Fanout Buffer

The MC100ES6011 is a differential 1:2 fanout buffer. The device is pin and functionally equivalent to the LVEP11 device. With AC performance the same as the LVEP11 device, the ES6011 is ideal for applications requiring lower voltage. Single-ended CLK input operation is limited to a $V_{CC} \geq 3.0$ V in PECL mode, or $V_{EE} \leq -3.0$ V in ECL mode.

The 100ES Series contains temperature compensation.

Features

- 240 ps Typical Propagation Delay
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range: $V_{CC} = 2.375$ V to 3.8 V with $V_{EE} = 0$ V
- ECL Mode Operating Range: $V_{CC} = 0$ V with $V_{EE} = -2.375$ V to -3.8 V
- Open Input Default State
- Q Output Will Default LOW with Inputs Open or at V_{EE}
- LVDS Input Compatible

MC100ES6011



D SUFFIX
8 LEAD SOIC PACKAGE
CASE 751



DT SUFFIX
8 LEAD TSSOP PACKAGE
CASE TBD

ORDERING INFORMATION

Device	Package
MC100ES6011D	SO-8
MC100ES6011DR2	SO-8
MC100ES6011DT	TSSOP-8
MC100ES6011DTR2	TSSOP-8

PIN DESCRIPTION

PIN	FUNCTION
D^* , $\bar{D}^{**}$	ECL Data Inputs
$Q0$, $\bar{Q}0$, $Q1$, $\bar{Q}1$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

* Pins will default LOW when left open.

** Pins will default to $0.572 V_{CC}/2$ when left open.

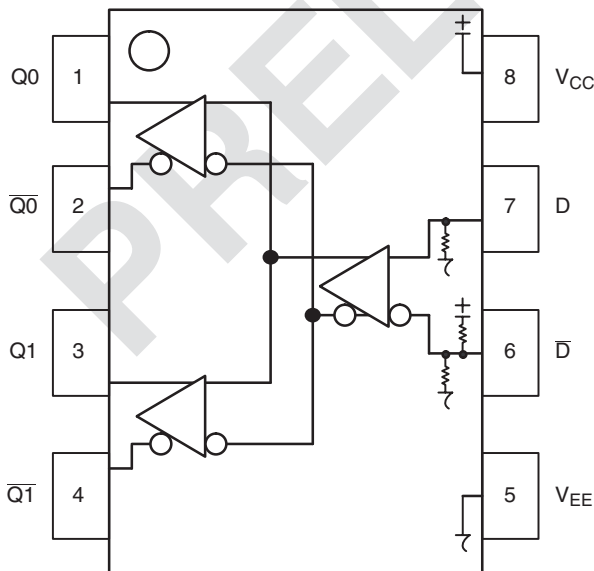


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 1. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 k Ω
Internal Input Pullup Resistor		56 k Ω
ESD Protection	Human Body Model	> 2 kV
	Machine Model	> 200 V
	Charged Device Model	> 1500 kV
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

Table 2. MAXIMUM RATINGS^a

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		4.6	V
V _{EE}	ECL Mode Power Supply	V _{CC} = 0 V		−4.6	V
V _I	PECL Mode Input Voltage ECL Mode Input Voltage	V _{EE} = 0 V	V _I ≤ V _{CC}	4.6	V
		V _{CC} = 0 V	V _I ≥ V _{EE}	−4.6	V
I _{out}	Output Current	Continuous Surge		50	mA
				100	mA
T _A	Operating Temperature Range			−40 to +85	°C
T _{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM	8 SOIC	TBD	°C/W
		500 LFPM	8 SOIC	TBD	°C/W
		0 LFPM	8 TSSOP	TBD	°C/W
		500 LFPM	8 TSSOP	TBD	°C/W

a Maximum Ratings are those values beyond which device damage may occur.

Table 3. DC CHARACTERISTICS, PECL (V_{CC} = 2.5 V $\pm$ 5%, V_{EE} = 0 V)

Symbol	Characteristic	−40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current		15			15		mA
V _{OH}	Output HIGH Voltage ^a	1415	1495	1620	1475	1545	1620	mV
V _{OL}	Output LOW Voltage ^a	670	805	945	690	795	880	mV
V _{IH}	Input HIGH Voltage (Single Ended)	1335		1620	1335		1620	mV
V _{IL}	Input LOW Voltage (Single Ended)	690		1025	690		1025	mV
V _{PP}	Differential Input Voltage ^b	0.12		1.3	0.12		1.3	V
V _{CMR}	Differential Cross Point Voltage ^c	1.0		V _{CC} −0.8	1.0		V _{CC} −0.8	V
I _{IH}	Input HIGH Current			150			150	μ A
I _{IL}	Input LOW Current	D	0.5		0.5			μ A
		$\bar{D}$	−150		−150			

NOTE: ES6011 circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

a Output termination voltage V_{TT} = 0V for V_{CC} = 2.5V operation is supported but the power consumption of the device will increase.

b V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.

c V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 4. DC CHARACTERISTICS, PECL ($V_{CC} = 3.3 \text{ V} \pm 5\%$, $V_{EE} = 0 \text{ V}$)

Symbol	Characteristic	-40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		15			15		mA
V_{OH}	Output HIGH Voltage ^a	2215	2295	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage ^a	1470	1605	1745	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	mV
V_{PP}	Differential Input Voltage ^b	0.12		1.3	0.12		1.3	V
V_{CMR}	Differential Cross Point Voltage ^c	1.0		$V_{CC}-0.8$	1.0		$V_{CC}-0.8$	V
I_{IH}	Input HIGH Current			150			150	μA
I_{IL}	Input LOW Current	$\begin{matrix} D \\ \bar{D} \end{matrix}$ 0.5 -150			$\begin{matrix} D \\ \bar{D} \end{matrix}$ 0.5 -150			μA

NOTE: ES6011 circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lpm is maintained.

a All loading with 50 ohms to $V_{CC}-2.0$ volts.

b V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.

c V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 5. DC CHARACTERISTICS, ECL ($V_{CC} = 0 \text{ V}$; $V_{EE} = -3.8 \text{ V}$ to -2.375 V)

Symbol	Characteristic	-40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		15			15		mA
V_{OH}	Output HIGH Voltage ^a	-1085	-1005	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage ^a	-1830	-1695	-1555	-1810	-1705	-1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage (Single Ended)	-1810		-1475	-1810		-1475	mV
V_{PP}	Differential Input Voltage ^b	0.12		1.3	0.12		1.3	V
V_{CMR}	Differential Cross Point Voltage ^c	$V_{EE}+0.5$		-0.3	$V_{EE}+0.5$		-0.3	V
I_{IH}	Input HIGH Current			150			150	μA
I_{IL}	Input LOW Current	$\begin{matrix} D \\ \bar{D} \end{matrix}$ 0.5 -150			$\begin{matrix} D \\ \bar{D} \end{matrix}$ 0.5 -150			μA

NOTE: ES6011 circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lpm is maintained.

a All loading with 50 ohms to $V_{CC}-2.0$ volts.

b V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.

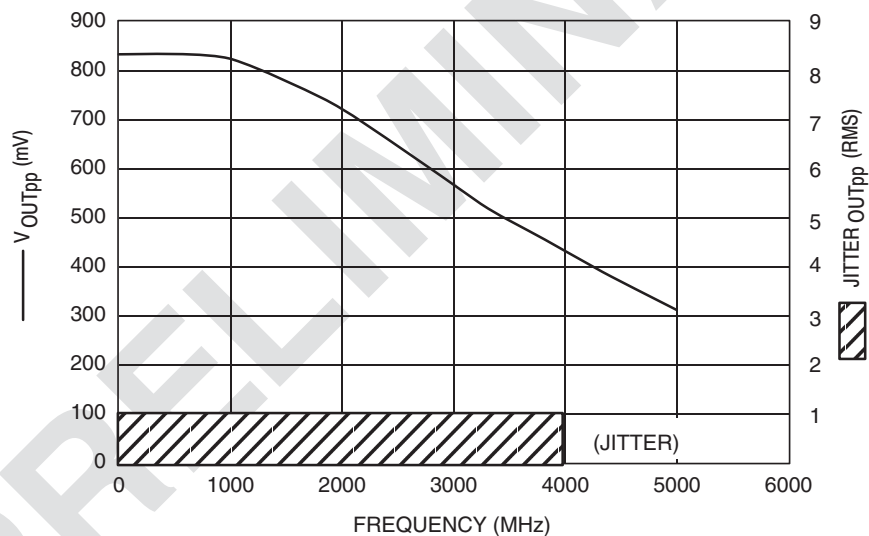
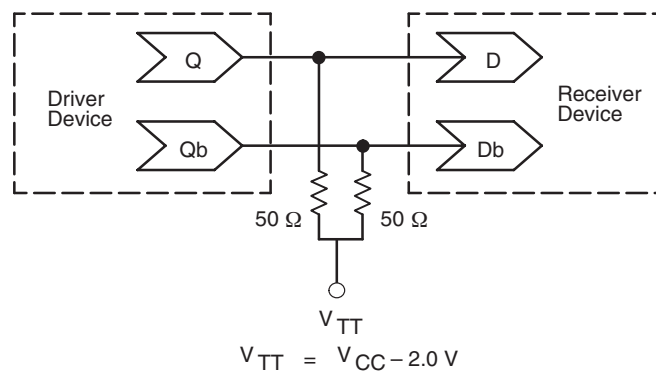
c V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 6. AC CHARACTERISTICS ($V_{CC} = 0\text{ V}$; $V_{EE} = -3.8\text{ V}$ to -2.375 V or $V_{CC} = 2.375\text{ V}$ to 3.8 V ; $V_{EE} = 0\text{ V}$)^a

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\max}$	Maximum Frequency (See Figure 2 $F_{\max}/\text{JITTER}$)		> 3			> 3			> 3		GHz
t_{PLH} , t_{PHL}	Propagation Delay (Differential) CLK to Q, $\bar{Q}$	170	230	300	180	240	310	210	270	360	ps
t_{SKEW}	Within Device Skew Q, $\bar{Q}$ Device to Device Skew ^b		5.0	20 130		5.0	20 130		5.0	20 150	ps
t_{JITTER}	Cycle-to-Cycle Jitter (See Figure 2 $F_{\max}/\text{JITTER}$)		< 2			< 2			< 2		ps
V_{PP}	Input Voltage Swing (Differential)	150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Differential Cross Point Voltage PECL ECL	0.2 $V_{EE}+0.2$		$V_{CC}-1.1$ -1.1	0.2 $V_{EE}+0.2$		$V_{CC}-1.1$ -1.1	0.2 $V_{EE}+0.2$		$V_{CC}-1.1$ -1.1	V
t_r , t_f	Output Rise/Fall Times Q, $\bar{Q}$ (20% – 80%)	70	110	170	80	120	180	100	140	200	ps

a Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to $V_{CC}-2.0\text{ V}$.

b Skew is measured between outputs under identical transitions.

**Figure 2. $F_{\max}/\text{Jitter}$** **Figure 3. Typical Termination for Output Driver and Device Evaluation**

Marking Notes:

Device Nomenclature	8-Lead SOIC Marking	8-Lead TSSOP Marking
MC100ES6011D	M6011	
MC100ES6011DT		6011

Trace Code Identification:

“A” – The First character indicates the Assembly location.

“L” – The Second character indicates the Source Wafer Lot Tracking Code.

“Y” – The Third character indicates the “ALPHA CODE” of the year device was assembled.

“W” – The Fourth character indicates the “ALPHA CODE” of the Work Week device was assembled.

The “Y” Year ALPHA CODES**The “W” Work Week ALPHA CODES**

Year	Month	Work Week Code	1st 6 Months (WW01 – WW26)	2nd 6 Months (WW27 – WW52)
A = 2003	FIRST 6 MONTHS	WW01 – WW26	A = WW01	A = WW27
B = 2003	SECOND 6 MONTHS	WW27 – WW52	B = WW02	B = WW28
C = 2004	FIRST 6 MONTHS	WW01 – WW26	C = WW03	C = WW29
D = 2004	SECOND 6 MONTHS	WW27 – WW52	D = WW04	D = WW30
E = 2005	FIRST 6 MONTHS	WW01 – WW26	E = WW05	E = WW31
F = 2005	SECOND 6 MONTHS	WW27 – WW52	F = WW06	F = WW32
G = 2006	FIRST 6 MONTHS	WW01 – WW26	G = WW07	G = WW33
H = 2006	SECOND 6 MONTHS	WW27 – WW52	H = WW08	H = WW34
I = 2007	FIRST 6 MONTHS	WW01 – WW26	I = WW09	I = WW35
J = 2007	SECOND 6 MONTHS	WW27 – WW52	J = WW10	J = WW36
K = 2008	FIRST 6 MONTHS	WW01 – WW26	K = WW11	K = WW37
L = 2008	SECOND 6 MONTHS	WW27 – WW52	L = WW12	L = WW38
M = 2009	FIRST 6 MONTHS	WW01 – WW26	M = WW13	M = WW39
N = 2009	SECOND 6 MONTHS	WW27 – WW52	N = WW14	N = WW40
O = 2010	FIRST 6 MONTHS	WW01 – WW26	O = WW15	O = WW41
P = 2010	SECOND 6 MONTHS	WW27 – WW52	P = WW16	P = WW42
Q = 2011	FIRST 6 MONTHS	WW01 – WW26	Q = WW17	Q = WW43
R = 2011	SECOND 6 MONTHS	WW27 – WW52	R = WW18	R = WW44
S = 2012	FIRST 6 MONTHS	WW01 – WW26	S = WW19	S = WW45
T = 2012	SECOND 6 MONTHS	WW27 – WW52	T = WW20	T = WW46
U = 2013	FIRST 6 MONTHS	WW01 – WW26	U = WW21	U = WW47
V = 2013	SECOND 6 MONTHS	WW27 – WW52	V = WW22	V = WW48
W = 2014	FIRST 6 MONTHS	WW01 – WW26	W = WW23	W = WW49
X = 2014	SECOND 6 MONTHS	WW27 – WW52	X = WW24	X = WW50
Y = 2015	FIRST 6 MONTHS	WW01 – WW26	Y = WW25	Y = WW51
Z = 2015	SECOND 6 MONTHS	WW27 – WW52	Z = WW26	Z = WW52

Marking Example:**XABR**

| | | |

X | | | = Assembly Location

| | |

A | | | = First Lot Assembled of this device in the designated Work Week

| | |

B | | | = 2003 Second 6 Months, WW27 – WW52

| | |

R = WW44 of 2003

Preliminary Information

2.5V / 3.3V 1:5 Differential ECL/PECL/HSTL/LVDS Clock Driver

The MC100ES6014 is a low skew 1-to-5 differential driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The ECL/PECL input signals can be either differential or single-ended (if the V_{BB} output is used). HSTL and LVDS inputs can be used when the ES6014 is operating under PECL conditions.

The ES6014 specifically guarantees low output-to-output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

To ensure that the tight skew specification is realized, both sides of any differential output need to be terminated identically into $50\ \Omega$ even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

The common enable ($\overline{EN}$) is synchronous, outputs are enabled/ disabled in the LOW state. This avoids a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock; therefore, all associated specification limits are referenced to the negative edge of the clock input.

The MC100ES6014, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the ES6014 to be used for high performance clock distribution in +3.3 V or +2.5 V systems. Single ended CLK input pin operation is limited to a $V_{CC} \geq 3.0\text{ V}$ in PECL mode, or $V_{EE} \leq -3.0\text{ V}$ in ECL mode. Designers can take advantage of the ES6014's performance to distribute low skew clocks across the backplane or the board.

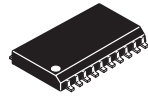
Features

- 100 ps Device-to-Device Skew
- 25 ps Within Device Skew
- 400 ps Typical Propagation Delay
- Maximum Frequency > 2 GHz Typical
- The 100 Series Contains Temperature Compensation
- PECL and HSTL Mode: $V_{CC} = 2.375\text{ V}$ to 3.8 V with $V_{EE} = 0\text{ V}$
- ECL Mode: $V_{CC} = 0\text{ V}$ with $V_{EE} = -2.375\text{ V}$ to -3.8 V
- LVDS and HSTL Input Compatible
- Open Input Default State

MC100ES6014



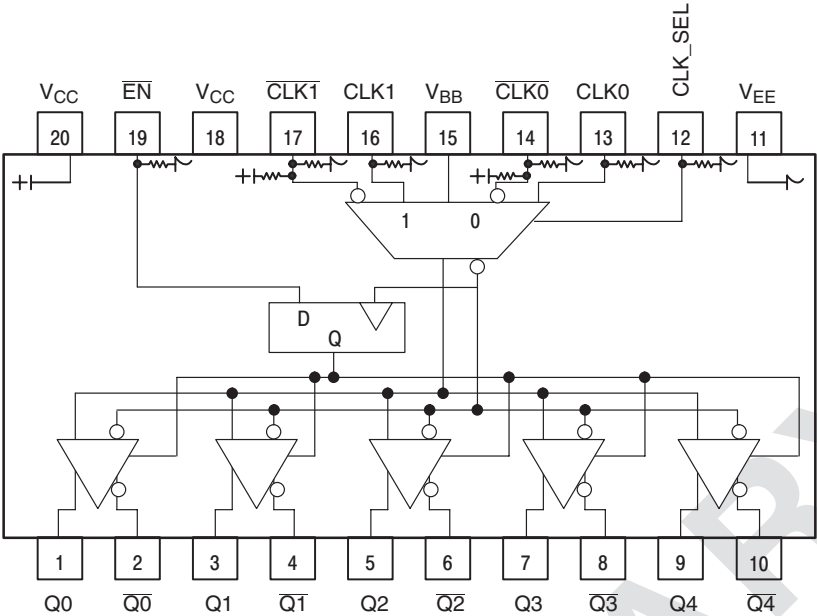
DT SUFFIX
20 LEAD TSSOP PACKAGE
CASE 948E



DW SUFFIX
20 LEAD SOIC PACKAGE
CASE 751D

ORDERING INFORMATION

Device	Package
MC100ES6014DT	TSSOP-20
MC100ES6014DTR2	TSSOP-20
MC100ES6014DW	SO-20
MC100ES6014DWR2	SO-20



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 20-Lead Pinout (Top View) and Logic Diagram

PIN DESCRIPTION

PINS	FUNCTION
CLK0*, $\overline{CLK0}$ **	ECL/PECL/HSTL CLK Input
CLK1*, $\overline{CLK1}$ **	ECL/PECL/HSTL CLK Input
Q0:4, $\overline{Q0}$:4	ECL/PECL Outputs
CLK_SEL*	ECL/PECL Active Clock Select Input
$\overline{EN}$ *	ECL Sync Enable
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

FUNCTION TABLE

CLK0	CLK1	CLK_SEL	$\overline{EN}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

* On next negative transition of CLK0 or CLK1

Table 1. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 k Ω
Internal Input Pullup Resistor		75 k Ω
ESD Protection	Human Body Model	> 2 kV
	Machine Model	> 100 V
	Charged Device Model	> 2 kV
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

Table 2. MAXIMUM RATINGS^a

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		4.6	V
V _{EE}	ECL Mode Power Supply	V _{CC} = 0 V		−4.6	V
V _I	PECL Mode Input Voltage ECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	4.6 −4.6	V V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
T _A	Operating Temperature Range			−40 to +85	°C
T _{stg}	Storage Temperature Range			−65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	20 TSSOP 20 TSSOP	TBD TBD	°C/W °C/W
		0 LFPM 500 LFPM	20 SOIC 20 SOIC	TBD TBD	°C/W °C/W

a Maximum Ratings are those values beyond which device damage may occur.

Table 3. DC CHARACTERISTICS, PECL (V_{CC} = 2.5 V ± 5%, V_{EE} = 0 V)

Symbol	Characteristic	−40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current		35			35		mA
V _{OH}	Output HIGH Voltage ^a	1415	1495	1620	1475	1545	1620	mV
V _{OL}	Output LOW Voltage ^a	670	805	945	690	795	880	mV
V _{IH}	Input HIGH Voltage (Single-Ended)	1335		1620	1335		1620	mV
V _{IL}	Input LOW Voltage (Single-Ended)	690		1025	690		1025	mV
V _{BB}	Output Reference Voltage	1120		1240	1120		1240	mV
V _{PP}	Differential Input Voltage ^b	0.12		1.3	0.12		1.3	V
V _{CMR}	Differential Cross Point Voltage ^c	1.0		V _{CC} −0.8	1.0		V _{CC} −0.8	V
I _{IH}	Input HIGH Current			150			150	μA
I _{IL}	Input LOW Current CLK CLK	0.5 −150			0.5 −150			μA

NOTE: ES6014 circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

a Output termination voltage V_{TT} = 0V for V_{CC} = 2.5V operation is supported but the power consumption of the device will increase.

b V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.

c V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 4. DC CHARACTERISTICS, PECL ($V_{CC} = 3.3 \text{ V} \pm 5\%$, $V_{EE} = 0 \text{ V}$)

Symbol	Characteristic	-40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		35			35		mA
V_{OH}	Output HIGH Voltage ^a	2215	2295	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage ^a	1470	1605	1745	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	mV
V_{BB}	Output Reference Voltage	1920		2040	1920		2040	mV
V_{PP}	Differential Input Voltage ^b	0.12		1.3	0.12		1.3	V
V_{CMR}	Differential Cross Point Voltage ^c	1.0		$V_{CC}-0.8$	1.0		$V_{CC}-0.8$	V
I_{IH}	Input HIGH Current			150			150	μA
I_{IL}	Input LOW Current	CLK -150			0.5 -150			μA

NOTE: ES6014 circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

a All loading with 50 ohms to $V_{CC}-2.0$ volts.

b V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.

c V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 5. DC CHARACTERISTICS, ECL ($V_{CC} = 0 \text{ V}$, $V_{EE} = -3.8 \text{ V}$ to -2.375 V)

Symbol	Characteristic	-40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		35			35		mA
V_{OH}	Output HIGH Voltage ^a	-1085	-100 5	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage ^a	-1830	-169 5	-155 5	-1810	-170 5	-162 0	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1810		-147 5	-1810		-147 5	mV
V_{BB}	Output Reference Voltage	-1380		-126 0	-1380		-126 0	mV
V_{PP}	Differential Input Voltage ^b	0.12		1.3	0.12		1.3	V
V_{CMR}	Differential Cross Point Voltage ^c	$V_{EE}+0.5$		-0.3	$V_{EE}+0.5$		-0.3	V
I_{IH}	Input HIGH Current			150			150	μA
I_{IL}	Input LOW Current	CLK -150			0.5 -150			μA

NOTE: ES6014 circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

a All loading with 50 ohms to $V_{CC}-2.0$ volts.

b V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.

c V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 6. DC CHARACTERISTICS, HSTL ($V_{CC} = 2.375\text{ V to }3.8\text{ V}$, $V_{EE} = 0\text{ V}$)

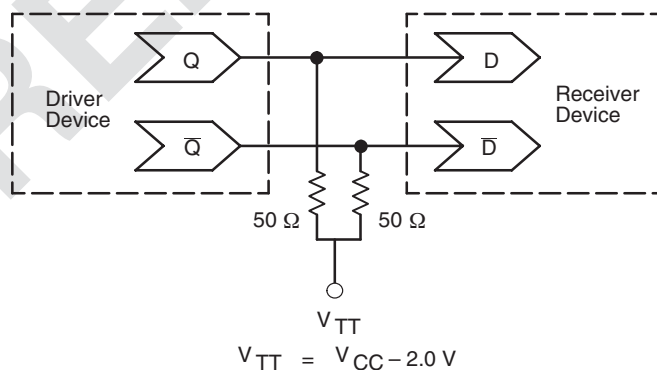
Symbol	Characteristic	-40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage	1200			1200			mV
V_{IL}	Input LOW Voltage			400			400	mV

Table 7. AC CHARACTERISTICS ($V_{CC} = 0\text{ V}$, $V_{EE} = -2.375\text{ V to }-3.8\text{ V}$ or $V_{CC} = 2.375\text{ V to }3.8\text{ V}$; $V_{EE} = 0\text{ V}$)^a

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\max}^{LV}$ PECL/ HSTL	Maximum Frequency		> 2			> 2			> 2		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output Differential	300	375	425	300	400	475	300	430	525	ps
t_{skew}	Within-Device Skew Device-to-Device Skew ^b		10 100	25 125		15 150	25 175		15 200	25 225	ps
t_s t_h	Setup Time Hold Time	100 200	50 140		100 200	50 140		100 200	50 140		ps
t_{JITTER}	Cycle-to-Cycle Jitter		< 2			< 2			< 2		ps
V_{PP}	Minimum Input Swing	150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Differential Cross Point Voltage PECL ECL	0.2 $V_{EE}+0.2$		$V_{CC}-1.1$ -1.1	0.2 $V_{EE}+0.2$		$V_{CC}-1.1$ -1.1	0.2 $V_{EE}+0.2$		$V_{CC}-1.1$ -1.1	V
t_r/t_f	Output Rise/Fall Time (20%–80%)	125	165	225	125	180	250	125	200	275	ps

a Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to $V_{CC}-2.0\text{ V}$.

b Skew is measured between outputs under identical transitions.

**Figure 2. Typical Termination for Output Driver and Device Evaluation**

Marking Notes:

Device Nomenclature	20-Lead TSSOP Marking	20-Lead SOIC W/B Marking
MC100ES6014DT	6014	
MC100ES6014DW		MC100ES6014

Trace Code Identification for 20 SOIC: AWLYYWW

“A” – The First character indicates the Assembly location.

“WL” – The Second & Third characters indicate the Source Wafer Lot Tracking Code.

“YY” – The Fourth & Fifth characters indicate the Year device was assembled.

“WW” – The Sixth & Seventh characters indicate the Work Week device was assembled.

Trace Code Identification for 20 TSSOP: ALYW

“A” – The First character indicates the Assembly location.

“L” – The Second character indicates the Source Wafer Lot Tracking Code.

“Y” – The Third character indicates the “ALPHA CODE” of the year device was assembled.

“W” – The Fourth character indicates the “ALPHA CODE” of the Work Week device was assembled.

The “Y” Year ALPHA CODES**The “W” Work Week ALPHA CODES**

Year	Month	Work Week Code	1st 6 Months (WW01 – WW26)	2nd 6 Months (WW27 – WW52)
A = 2003	FIRST 6 MONTHS	WW01 – WW26	A = WW01	A = WW27
B = 2003	SECOND 6 MONTHS	WW27 – WW52	B = WW02	B = WW28
C = 2004	FIRST 6 MONTHS	WW01 – WW26	C = WW03	C = WW29
D = 2004	SECOND 6 MONTHS	WW27 – WW52	D = WW04	D = WW30
E = 2005	FIRST 6 MONTHS	WW01 – WW26	E = WW05	E = WW31
F = 2005	SECOND 6 MONTHS	WW27 – WW52	F = WW06	F = WW32
G = 2006	FIRST 6 MONTHS	WW01 – WW26	G = WW07	G = WW33
H = 2006	SECOND 6 MONTHS	WW27 – WW52	H = WW08	H = WW34
I = 2007	FIRST 6 MONTHS	WW01 – WW26	I = WW09	I = WW35
J = 2007	SECOND 6 MONTHS	WW27 – WW52	J = WW10	J = WW36
K = 2008	FIRST 6 MONTHS	WW01 – WW26	K = WW11	K = WW37
L = 2008	SECOND 6 MONTHS	WW27 – WW52	L = WW12	L = WW38
M = 2009	FIRST 6 MONTHS	WW01 – WW26	M = WW13	M = WW39
N = 2009	SECOND 6 MONTHS	WW27 – WW52	N = WW14	N = WW40
O = 2010	FIRST 6 MONTHS	WW01 – WW26	O = WW15	O = WW41
P = 2010	SECOND 6 MONTHS	WW27 – WW52	P = WW16	P = WW42
Q = 2011	FIRST 6 MONTHS	WW01 – WW26	Q = WW17	Q = WW43
R = 2011	SECOND 6 MONTHS	WW27 – WW52	R = WW18	R = WW44
S = 2012	FIRST 6 MONTHS	WW01 – WW26	S = WW19	S = WW45
T = 2012	SECOND 6 MONTHS	WW27 – WW52	T = WW20	T = WW46
U = 2013	FIRST 6 MONTHS	WW01 – WW26	U = WW21	U = WW47
V = 2013	SECOND 6 MONTHS	WW27 – WW52	V = WW22	V = WW48
W = 2014	FIRST 6 MONTHS	WW01 – WW26	W = WW23	W = WW49
X = 2014	SECOND 6 MONTHS	WW27 – WW52	X = WW24	X = WW50
Y = 2015	FIRST 6 MONTHS	WW01 – WW26	Y = WW25	Y = WW51
Z = 2015	SECOND 6 MONTHS	WW27 – WW52	Z = WW26	Z = WW52

20 TSSOP Tracecode Marking Example:

5ABR

| | | |

5 | | | = Assembly Location

| | |

A | | = First Lot Assembled of this device in the designated Work Week

| |

B | = 2003 Second 6 Months, WW27 – WW52

|

R = WW44 of 2003

Preliminary Information

2.5V / 3.3V ECL/PECL/HSTL/ LVDS Dual Differential 2:1 Multiplexer

The MC100ES6056 is a dual, fully differential 2:1 multiplexer. The differential data path makes the device ideal for multiplexing low skew clock or other skew sensitive signals. Multiple V_{BB} pins are provided.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The device features both individual and common select inputs to address both data path and random logic applications.

The 100ES Series contains temperature compensation.

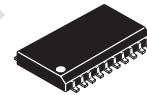
Features

- 360 ps Typical Propagation Delays
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range: $V_{CC} = 2.375$ V to 3.8 V with $V_{EE} = 0$ V
- ECL Mode Operating Range: $V_{CC} = 0$ V with $V_{EE} = -2.375$ V to -3.8 V
- Open Input Default State
- Separate and Common Select
- Q Output Will Default LOW with Inputs Open or at V_{EE}
- V_{BB} Outputs
- LVDS and HSTL Input cCompatible

MC100ES6056



DT SUFFIX
20 LEAD TSSOP PACKAGE
CASE 948E



DW SUFFIX
20 LEAD SOIC PACKAGE
CASE 751D

ORDERING INFORMATION

Device	Package
MC100ES6056DT	TSSOP-20
MC100ES6056DTR2	TSSOP-20
MC100ES6056DW	SO-20
MC100ES6056DWR2	SO-20

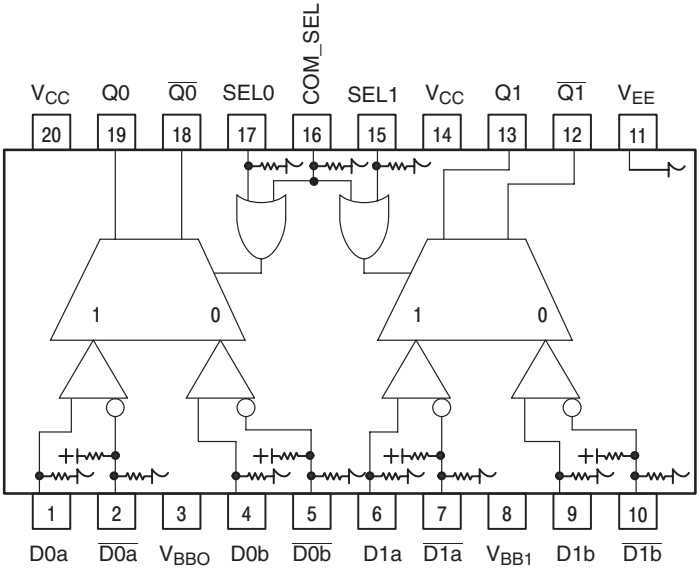


Figure 1. 20-Lead Package (Top View) and Logic Diagram

PIN DESCRIPTION

PIN	FUNCTION
D0a* – D1a*	ECL Input Data a
$\overline{D0a^*}$ – $\overline{D1a^*}$	ECL Input Data a Invert
D0b* – D1b*	ECL Input Data b
$\overline{D0b^*}$ – $\overline{D1b^*}$	ECL Input Data b Invert
SEL0* – SEL1*	ECL Indiv. Select Input
COM_SEL*	ECL Common Select Input
V_{BB0} , V_{BB1}	Output Reference Voltage
Q0 – Q1	ECL True Outputs
$\overline{Q0}$ – $\overline{Q1}$	ECL Inverted Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

* Pins will default LOW when left open.

TRUTH TABLE

SEL0	SEL1	COM_SEL	Q0, Q0	Q1, Q1
X	X	H	a	a
L	L	L	b	b
L	H	L	b	a
H	H	L	a	a
H	L	L	a	b

Table 1. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 k Ω
Internal Input Pullup Resistor		75 k Ω
ESD Protection	Human Body Model	> 2 kV
	Machine Model	> 200 V
	Charged Device Model	> 2 kV
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

Table 2. MAXIMUM RATINGS^a

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		4.6	V
V_{EE}	ECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-4.6	V
V_I	PECL Mode Input Voltage ECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	4.6 -4.6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	20 TSSOP 20 TSSOP	TBD TBD	°C/W °C/W
		0 LFPM 500 LFPM	20 SOIC 20 SOIC	TBD TBD	°C/W °C/W

a Maximum Ratings are those values beyond which device damage may occur.

Table 3. DC CHARACTERISTICS, PECL ($V_{CC} = 2.5\text{ V} \pm 5\%$, $V_{EE} = 0\text{ V}$)

Symbol	Characteristic	-40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		35			35		mA
V_{OH}	Output HIGH Voltage ^a	1415	1495	1620	1475	1545	1620	mV
V_{OL}	Output LOW Voltage ^a	670	805	945	690	795	880	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	1335		1620	1335		1620	mV
V_{IL}	Input LOW Voltage (Single-Ended)	690		1025	690		1025	mV
V_{BB}	Output Reference Voltage	1120		1240	1120		1240	mV
V_{PP}	Differential Input Voltage ^b	0.12		1.3	0.12		1.3	V
V_{CMR}	Differential Cross Point Voltage ^c	1.0		$V_{CC}-0.8$	1.0		$V_{CC}-0.8$	V
I_{IH}	Input HIGH Current			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			μA

NOTE: ES6014 circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lpm is maintained.

a Output termination voltage $V_{TT} = 0\text{ V}$ for $V_{CC} = 2.5\text{ V}$ operation is supported but the power consumption of the device will increase.

b V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.

c V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 4. DC CHARACTERISTICS, PECL ($V_{CC} = 3.3 \text{ V} \pm 5\%$, $V_{EE} = 0 \text{ V}$)

Symbol	Characteristic	-40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		17			17		mA
V_{OH}	Output HIGH Voltage ^a	2215	2295	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage ^a	1470	1605	1745	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	mV
V_{BB}	Output Reference Voltage	1920		2040	1920		2040	mV
V_{PP}	Differential Input Voltage ^b	0.12		1.3	0.12		1.3	V
V_{CMR}	Differential Cross Point Voltage ^c	1.0		$V_{CC}-0.8$	1.0		$V_{CC}-0.8$	V
I_{IH}	Input HIGH Current			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			μA

NOTE: MC100ES6056 circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lpm is maintained.

a All loading with 50Ω to $V_{CC}-2.0$ volts.

b V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.

c V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 5. DC CHARACTERISTICS, ECL ($V_{CC} = 0 \text{ V}$, $V_{EE} = -3.0 \text{ V} \pm 5\%$)

Symbol	Characteristic	-40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		17			17		mA
V_{OH}	Output HIGH Voltage ^a	-1085	-1005	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage ^a	-1830	-1695	-1555	-1810	-1705	-1620	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1810		-1475	-1810		-1475	mV
V_{BB}	Output Reference Voltage	-1380		-1260	-1380		-1260	mV
V_{PP}	Differential Input Voltage ^b	0.12		1.3	0.12		1.3	V
V_{CMR}	Differential Cross Point Voltage ^c	$V_{EE}+0.5$		-0.3	$V_{EE}+0.5$		-0.3	V
I_{IH}	Input HIGH Current			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			μA

NOTE: MC100ES6056 circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lpm is maintained.

a All loading with 50Ω to $V_{CC}-2.0$ volts.

b V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.

c V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 6. DC CHARACTERISTICS, HSTL ($V_{CC} = 2.375\text{ V to }3.8\text{ V}$, $V_{EE} = 0\text{ V}$)

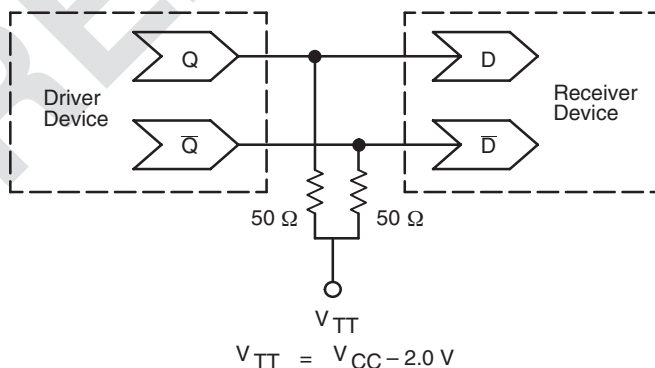
Symbol	Characteristic	-40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage (Single Ended)	1200			1200			mV
V_{IL}	Input LOW Voltage (Single Ended)			400			400	mV

Table 7. AC CHARACTERISTICS ($V_{CC} = 0\text{ V}$; $V_{EE} = -3.0\text{ V}$ or $V_{CC} = 3.0\text{ V}$; $V_{EE} = 0\text{ V}$)^a

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency		> 3			> 3			> 3		GHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential D to Q, $\bar{Q}$ SEL to Q, $\bar{Q}$ COM_SEL to Q, $\bar{Q}$	250 250 250	340 340 350	450 450 450	270 270 270	360 340 360	470 470 470	300 300 300	400 400 400	500 500 500	ps
t_{SKEW}	Within-Device Skew ^b Device to Device Skew		50	100 200		50	100 200		50	100 200	ps
t_{JITTER}	Cycle-to-Cycle Jitter		< 2			< 2			< 2		ps
V_{PP}	Input Voltage Swing (Differential)	150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Differential Cross Point Voltage PECL ECL	0.2 $V_{EE}+0.2$		$V_{CC}-1.1$ -1.1	0.2 $V_{EE}+0.2$		$V_{CC}-1.1$ -1.1	0.2 $V_{EE}+0.2$		$V_{CC}-1.1$ -1.1	V
t_r t_f	Output Rise/Fall Times Q, $\bar{Q}$ (20% – 80%)	70	120	170	80	130	180	100	150	230	ps

a Measured using a 750 mV source, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC}-2.0\text{ V}$.

b Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

**Figure 2. Typical Termination for Output Driver and Device Evaluation**

Marking Notes:

Device Nomenclature	20-Lead TSSOP Marking	20-Lead SOIC W/B Marking
MC100ES6056DT	6056	
MC100ES6056DW		MC100ES6056

Trace Code Identification for 20 SOIC: AWLYYWW

“A” – The First character indicates the Assembly location.

“WL” – The Second & Third characters indicate the Source Wafer Lot Tracking Code.

“YY” – The Fourth & Fifth characters indicate the Year device was assembled.

“WW” – The Sixth & Seventh characters indicate the Work Week device was assembled.

Trace Code Identification for 20 TSSOP: ALYW

“A” – The First character indicates the Assembly location.

“L” – The Second character indicates the Source Wafer Lot Tracking Code.

“Y” – The Third character indicates the “ALPHA CODE” of the year device was assembled.

“W” – The Fourth character indicates the “ALPHA CODE” of the Work Week device was assembled.

The “Y” Year ALPHA CODES**The “W” Work Week ALPHA CODES**

Year	Month	Work Week Code	1st 6 Months (WW01 – WW26)	2nd 6 Months (WW27 – WW52)
A = 2003	FIRST 6 MONTHS	WW01 – WW26	A = WW01	A = WW27
B = 2003	SECOND 6 MONTHS	WW27 – WW52	B = WW02	B = WW28
C = 2004	FIRST 6 MONTHS	WW01 – WW26	C = WW03	C = WW29
D = 2004	SECOND 6 MONTHS	WW27 – WW52	D = WW04	D = WW30
E = 2005	FIRST 6 MONTHS	WW01 – WW26	E = WW05	E = WW31
F = 2005	SECOND 6 MONTHS	WW27 – WW52	F = WW06	F = WW32
G = 2006	FIRST 6 MONTHS	WW01 – WW26	G = WW07	G = WW33
H = 2006	SECOND 6 MONTHS	WW27 – WW52	H = WW08	H = WW34
I = 2007	FIRST 6 MONTHS	WW01 – WW26	I = WW09	I = WW35
J = 2007	SECOND 6 MONTHS	WW27 – WW52	J = WW10	J = WW36
K = 2008	FIRST 6 MONTHS	WW01 – WW26	K = WW11	K = WW37
L = 2008	SECOND 6 MONTHS	WW27 – WW52	L = WW12	L = WW38
M = 2009	FIRST 6 MONTHS	WW01 – WW26	M = WW13	M = WW39
N = 2009	SECOND 6 MONTHS	WW27 – WW52	N = WW14	N = WW40
O = 2010	FIRST 6 MONTHS	WW01 – WW26	O = WW15	O = WW41
P = 2010	SECOND 6 MONTHS	WW27 – WW52	P = WW16	P = WW42
Q = 2011	FIRST 6 MONTHS	WW01 – WW26	Q = WW17	Q = WW43
R = 2011	SECOND 6 MONTHS	WW27 – WW52	R = WW18	R = WW44
S = 2012	FIRST 6 MONTHS	WW01 – WW26	S = WW19	S = WW45
T = 2012	SECOND 6 MONTHS	WW27 – WW52	T = WW20	T = WW46
U = 2013	FIRST 6 MONTHS	WW01 – WW26	U = WW21	U = WW47
V = 2013	SECOND 6 MONTHS	WW27 – WW52	V = WW22	V = WW48
W = 2014	FIRST 6 MONTHS	WW01 – WW26	W = WW23	W = WW49
X = 2014	SECOND 6 MONTHS	WW27 – WW52	X = WW24	X = WW50
Y = 2015	FIRST 6 MONTHS	WW01 – WW26	Y = WW25	Y = WW51
Z = 2015	SECOND 6 MONTHS	WW27 – WW52	Z = WW26	Z = WW52

20 TSSOP Tracecode Marking Example:

5ABR

| | |

5 | | | = Assembly Location

| | |

A | | = First Lot Assembled of this device in the designated Work Week

| |

B | = 2003 Second 6 Months, WW27 – WW52

|

R = WW44 of 2003

Low Voltage 2.5/3.3V Differential ECL/PECL/HSTL Fanout Buffer

The Motorola MC100ES6111 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6111 supports various applications that require distribution of precisely aligned differential clock signals. Using SiGe:C technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver is high performance clock distribution in computing, networking and telecommunication systems.

- 1:10 differential clock distribution
- 35 ps maximum device skew
- Fully differential architecture from input to all outputs
- SiGe:C technology supports near-zero output skew
- Supports DC to 2.7 GHz operation of clock or data signals
- ECL/PECL compatible differential clock outputs
- ECL/PECL/HSTL compatible differential clock inputs
- Single 3.3V, -3.3V, 2.5V or -2.5V supply
- Standard 32 lead LQFP package
- Industrial temperature range
- Pin and function compatible to the MC100EP111

Functional Description

The MC100ES6111 is designed for low skew clock distribution systems and supports clock frequencies up to 2.7 GHz. The device accepts two clock sources. The CLKA input can be driven by ECL or PECL compatible signals, the CLKB input accepts HSTL compatible signals. The selected input signal is distributed to 10 identical, differential ECL/PECL outputs. If VBB is connected to the CLKA input and bypassed to GND by a 10 nF capacitor, the MC100ES6111 can be driven by single-ended ECL/PECL signals utilizing the VBB bias voltage output.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The MC100ES6111 can be operated from a single 3.3V or 2.5V supply. As most other ECL compatible devices, the MC100ES6111 supports positive (PECL) and negative (ECL) supplies. The MC100ES6111 is pin and function compatible to the MC100EP111.

MC100ES6111

**LOW-VOLTAGE
1:10 DIFFERENTIAL
ECL/PECL/HSTL
CLOCK FANOUT DRIVER**



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A

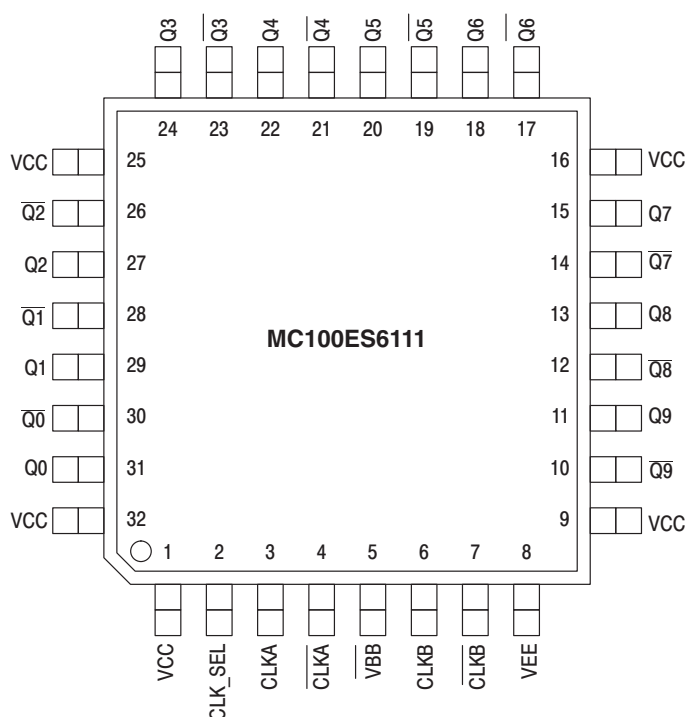


Figure 2. 32—Lead Package Pinout (Top View)

Pin	I/O	Type	Function
CLKA, $\overline{\text{CLKA}}$	Input	ECL/PECL	Differential reference clock signal input
CLKB, $\overline{\text{CLKB}}$	Input	HSTL	Alternative differential reference clock signal input
CLK_SEL	Input	ECL/PECL	Active clock input select
Q[0–9], $\overline{\text{Q}}$ [0–9]	Output	ECL/PECL	Differential clock outputs
V _{EE} ^a	Supply		Negative power supply
V _{CC}	Supply		Positive power supply. All V _{CC} pins must be connected to the positive power supply for correct DC and AC operation.
V _{BB}	Output	DC	Reference voltage output for single ended ECL or PECL operation

Table 2. FUNCTION TABLE

Control	Default	0	1
CLK_SEL	0	CLKA, $\overline{\text{CLKA}}$ input pair is active. CLKA can be driven by ECL or PECL compatible signals.	CLKB, $\overline{\text{CLKB}}$ input pair is active. CLKB can be driven by HSTL compatible signals.

Table 3. Absolute Maximum Ratings^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	3.6	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} + 0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} + 0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage temperature	-65	125	°C	
T _{Func}	Functional temperature range	T _A = -40	T _J = +110	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output termination voltage		V _{CC} - 2 ^a		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	4000			V	
CDM	ESD Protection (Charged device model)	2000			V	
LU	Latch-up immunity	200			mA	
C _{IN}			4.0		pF	Inputs
θ _{JA}	Thermal resistance junction to ambient JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ _{JC}	Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
T _J	Operating junction temperature ^b (continuous operation) MTBF = 9.1 years			110	°C	

- a. Output termination voltage V_{TT} = 0V for V_{CC} = 2.5V operation is supported but the power consumption of the device will increase
- b. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 and the application section in this datasheet for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6111 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6111 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 5. PECL/HSTL DC Characteristics ($V_{CC} = 2.5V \pm 5\%$ or $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = GND$, $T_J = 0^\circ C$ to $+110^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Control input CLK_SEL						
V_{IL}	Input voltage low	$V_{CC} - 1.810$		$V_{CC} - 1.475$	V	
V_{IH}	Input voltage high	$V_{CC} - 1.165$		$V_{CC} - 0.880$	V	
I_{IN}	Input Current ^a			100	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock input pair CLKA, $\overline{CLKA}$ (PECL differential signals)						
V_{PP}	Differential input voltage ^b	0.1		1.3	V	Differential operation
V_{CMR}	Differential cross point voltage ^c	1.0		$V_{CC} - 0.3$	V	Differential operation
I_{IN}	Input Current ^a			100	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock input pair CLKB, $\overline{CLKB}$ (HSTL differential signals)						
V_{DIF}	Differential input voltage ^d $V_{CC} = 3.3V$ $V_{CC} = 2.5V$	0.4 0.4			V V	
V_X	Differential cross point voltage ^e	0.68		0.9	V	
I_{IN}	Input Current			200	μA	$V_{IN} = V_X \pm 0.2V$
PECL clock outputs (Q0-9, $\overline{Q0-9}$)						
V_{OH}	Output High Voltage	$V_{CC} - 1.2$	$V_{CC} - 1.005$	$V_{CC} - 0.7$	V	$I_{OH} = -30 \text{ mA}^f$
V_{OL}	Output Low Voltage $V_{CC} = 3.3V \pm 5\%$ $V_{CC} = 2.5V \pm 5\%$	$V_{CC} - 1.9$ $V_{CC} - 1.9$	$V_{CC} - 1.705$ $V_{CC} - 1.705$	$V_{CC} - 1.5$ $V_{CC} - 1.3$	V	$I_{OL} = -5 \text{ mA}^f$
Supply current and V_{BB}						
I_{EE}	Maximum Quiescent Supply Current without output termination current ^g			100	mA	V_{EE} pin
V_{BB}	Output reference voltage	$V_{CC} - 1.4$		$V_{CC} - 1.2$	V	$I_{BB} = 200 \mu A$

a. Input have internal pullup/pulldown resistors which affect the input current

b. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality

c. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

d. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality.

e. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.

f. Equivalent to a termination of 50Ω to V_{TT} .

g. I_{CC} calculation: $I_{CC} = (\text{number of differential output pairs used}) \times (I_{OH} + I_{OL}) + I_{EE}$

$I_{CC} = (\text{number of differential output pairs used}) \times (V_{OH} - V_{TT})/R_{load} + (V_{OL} - V_{TT})/R_{load} + I_{EE}$.

Table 6. ECL DC Characteristics ($V_{EE} = -2.5V \pm 5\%$ or $V_{EE} = -3.3V \pm 5\%$, $V_{CC} = GND$, $T_J = 0^\circ C$ to $+110^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Control input CLK_SEL						
V _{IL}	Input voltage low	-1.810		-1.475	V	
V _{IH}	Input voltage high	-1.165		-0.880	V	
I _{IN}	Input Current ^a			100	μA	V _{IN} = V _{IL} or V _{IN} = V _{IH}
Clock input pair CLKA, $\overline{\text{CLKA}}$, CLKB, $\overline{\text{CLKB}}$ (ECL differential signals)						
V _{PP}	Differential input voltage ^b	0.1		1.3	V	Differential operation
V _{CMR}	Differential cross point voltage ^c	V _{EE} + 1.0		-0.3	V	Differential operation
I _{IN}	Input Current ^a			100	μA	V _{IN} = V _{IL} or V _{IN} = V _{IH}
ECL clock outputs (Q0-9, $\overline{\text{Q0-9}}$)						
V _{OH}	Output High Voltage	-1.2	-1.005	-0.7	V	I _{OH} = −30 mA ^d
V _{OL}	Output Low Voltage	V _{EE} = −3.3V±5% V _{EE} = −2.5V±5%	-1.9 -1.9	-1.705 -1.705	V	I _{OL} = −5 mA ^d
Supply current and V _{BB}						
I _{EE}	Maximum Quiescent Supply Current without output termination current ^e			100	mA	V _{EE} pin
V _{BB}	Output reference voltage	V _{CC} -1.4		V _{CC} -1.2	V	I _{BB} = 200 μA

a. Input have internal pullup/pulldown resistors which affect the input current

b. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality

c. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

d. Equivalent to a termination of 50Ω to V_{TT} .

e. I_{CC} calculation: $I_{CC} = (\text{number of differential output pairs used}) \times (I_{OH} + I_{OL}) + I_{EE}$

$I_{CC} = (\text{number of differential output pairs used}) \times (V_{OH} - V_{TT})/R_{load} + (V_{OL} - V_{TT})/R_{load} + I_{EE}$.

Table 7. AC Characteristics (ECL: $V_{EE} = -3.3V \pm 5\%$ or $V_{EE} = -2.5V \pm 5\%$, $V_{CC} = GND$) or
(HSTL/PECL: $V_{CC} = 3.3V \pm 5\%$ or $V_{CC} = 2.5V \pm 5\%$, $V_{EE} = GND$, $T_J = 0^\circ C$ to $+110^\circ C$) ^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLKA, $\overline{CLKA}$ (PECL or ECL differential signals)						
V_{PP}	Differential input voltage ^b (peak-to-peak)	0.15		1.3	V	
V_{CMR}	Differential input crosspoint voltage ^c PECL	$V_{EE} + 1.0$		$V_{CC} - 0.3$	V	
f_{CLK}	Input Frequency ^d			2.7	GHz	Differential
t_{PD}	Propagation Delay CLKA or CLKB to Q0-9	280	400	530	ps	Differential
Clock input pair CLKB, $\overline{CLKB}$ (HSTL differential signals)						
V_{DIF}	Differential input voltage ^e (peak-to-peak) ^e	0.4		1.0	V	
V_X	Differential input crosspoint voltage ^f	$V_{EE} + 0.68$		$V_{EE} + 0.9$	V	
f_{CLK}	Input Frequency			2.7	GHz	Differential
t_{PD}	Propagation Delay CLKB to Q0-9	280	400	530	ps	Differential
ECL clock outputs (Q0-9, $\overline{Q0-9}$)						
$V_{O(P-P)}$	Differential output voltage (peak-to-peak) $f_O < 300$ MHz $f_O < 1.5$ GHz $f_O < 2.7$ GHz	0.45 0.3 TBD	0.72 0.55 0.37	0.95 0.95 0.95	V V V	
$t_{sk(O)}$	Output-to-output skew			35	ps	Differential
$t_{sk(PP)}$	Output-to-output skew (part-to-part)			250	ps	Differential
$t_{JIT(CC)}$	Output cycle-to-cycle jitter		TBD			
$t_{sk(P)}$	Output Pulse skew ^g			75	ps	
t_r, t_f	Output Rise/Fall Time	0.05		0.3	ns	20% to 80%

- a. AC characteristics apply for parallel output termination of $50\ \Omega$ to V_{TT}
- b. V_{PP} (AC) is the minimum differential ECL/PECL input voltage swing required to maintain AC characteristics including t_{pd} and device-to-device skew
- c. V_{CMR} (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew
- d. The MC100ES6111 is fully operational up to 3.0 GHz and is characterized up to 2.7 GHz.
- e. V_{DIF} (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics including t_{pd} and device-to-device skew.
- f. V_X (AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the V_X (AC) range and the input swing lies within the V_{DIF} (AC) specification. Violation of V_X (AC) or V_{DIF} (AC) impacts the device propagation delay, device and part-to-part skew
- g. Output pulse skew is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.

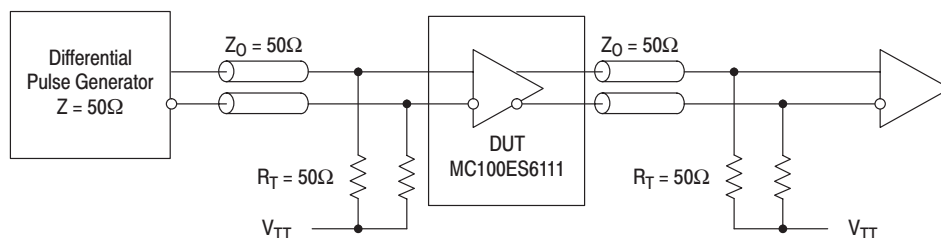


Figure 1. MC100ES6111 AC test reference

APPLICATIONS INFORMATION

Understanding the junction temperature range of the MC100ES6111

To make the optimum use of high clock frequency and low skew capabilities of the MC100ES6111, the MC100ES6111 is specified, characterized and tested for the junction temperature range of $T_J=0^{\circ}\text{C}$ to $+110^{\circ}\text{C}$. Because the exact thermal performance depends on the PCB type, design, thermal management and natural or forced air convection, the junction temperature provides an exact way to correlate the application specific conditions to the published performance data of this datasheet. The correlation of the junction temperature range to the application ambient temperature range and vice versa can be done by calculation:

$$T_J = T_A + R_{thja} \cdot P_{tot}$$

Assuming a thermal resistance (junction to ambient) of 54.4°C/W (2s2p board, 200 ft/min airflow, see table 4) and a typical power consumption of 610 mW (all outputs terminated 50 ohms to V_{TT} , $V_{CC}=3.3\text{V}$, frequency independent), the junction temperature of the MC100ES6111 is approximately $T_A + 33^{\circ}\text{C}$, and the minimum ambient temperature in this example case calculates to -33°C (the maximum ambient temperature is 77°C . See Table 8). Exceeding the minimum junction temperature specification of the MC100ES6111 does not have a significant impact on the device functionality. However, the continuous use the MC100ES6111 at high ambient temperatures requires thermal management to not exceed the specified maximum junction temperature. Please see the application note AN1545 for a power consumption calculation guideline.

Table 8: Ambient temperature ranges ($P_{tot} = 610\text{ mW}$)

R_{thja} (2s2p board)		$T_{A, \text{min}}$	$T_{A, \text{max}}$
Natural convection	59.0°C/W	-36°C	74°C
100 ft/min	54.4°C/W	-33°C	77°C
200 ft/min	52.5°C/W	-32°C	78°C
400 ft/min	50.4°C/W	-30°C	79°C
800 ft/min	47.8°C/W	-29°C	81°C

a. The MC100ES6111 device function is guaranteed from $T_A=-40^{\circ}\text{C}$ to $T_J=110^{\circ}\text{C}$

Maintaining Lowest Device Skew

The MC100ES6111 guarantees low output-to-output bank skew of 35 ps and a part-to-part skew of max. 250 ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. If an entire output bank is not used, it is recommended to leave all of these outputs open and unterminated. This will reduce the device power consumption while maintaining minimum output skew.

Power Supply Bypassing

The MC100ES6111 is a mixed analog/digital product. The differential architecture of the MC100ES6111 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

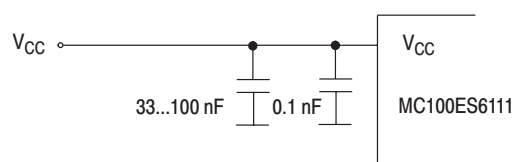


Figure 2. V_{CC} Power Supply Bypass

Preliminary Information

2.5V/3.3V

ECL/PECL/HSTL/LVDS $\div 2/4$, $\div 4/5/6$ Clock Generation Chip

The MC100ES6139 is a low skew $\div 2/4$, $\div 4/5/6$ clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, LVPECL input signals. In addition, by using the V_{BB} output, a sinusoidal source can be AC coupled into the device. If a single-ended input is to be used, the V_{BB} output should be connected to the CLK input and bypassed to ground via a 0.01 μ F capacitor.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple ES6139s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one ES6139, the MR pin need not be exercised as the internal divider design ensures synchronization between the $\div 2/4$ and the $\div 4/5/6$ outputs of a single device. All V_{CC} and V_{EE} pins must be externally connected to power supply to guarantee proper operation.

The 100ES Series contains temperature compensation.

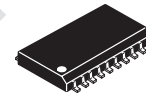
Features

- Maximum Frequency >1.0 GHz Typical
- 50 ps Output-to-Output Skew
- PECL Mode Operating Range: $V_{CC} = 2.375$ V to 3.8 V with $V_{EE} = 0$ V
- ECL Mode Operating Range: $V_{CC} = 0$ V with $V_{EE} = -2.375$ V to -3.8 V
- Open Input Default State
- Synchronous Enable/Disable
- Master Reset for Synchronization of Multiple Chips
- V_{BB} Output
- LVDS and HSTL Input Compatible

MC100ES6139



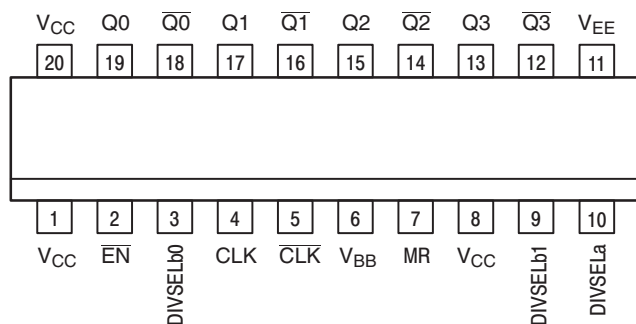
DT SUFFIX
20 LEAD TSSOP PACKAGE
CASE 948E



DW SUFFIX
20 LEAD SOIC PACKAGE
CASE 751D

ORDERING INFORMATION

Device	Package
MC100ES6139DT	TSSOP-20
MC100ES6139DTR2	TSSOP-20
MC100ES6139DW	SO-20
MC100ES6139DWR2	SO-20



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 20-Lead Pinout (Top View)

PIN DESCRIPTION

PIN	FUNCTION
CLK*, $\overline{\text{CLK}}^*$	ECL Diff Clock Inputs
$\overline{\text{EN}}^*$	ECL Sync Enable
$\overline{\text{MR}}^*$	ECL Master Reset
V_{BB}	ECL Reference Output
Q0, Q1, $\overline{\text{Q0}}$, $\overline{\text{Q1}}$	ECL Diff $\div 2/4$ Outputs
Q2, Q3, $\overline{\text{Q2}}$, $\overline{\text{Q3}}$	ECL Diff $\div 4/5/6$ Outputs
DIVSELa*	ECL Freq. Select Input $\div 2/4$
DIVSELb0*	ECL Freq. Select Input $\div 4/5/6$
DIVSELb1*	ECL Freq. Select Input $\div 4/5/6$
V_{CC}	ECL Positive Supply
V_{EE}	ECL Negative Supply

* Pins will default low when left open.

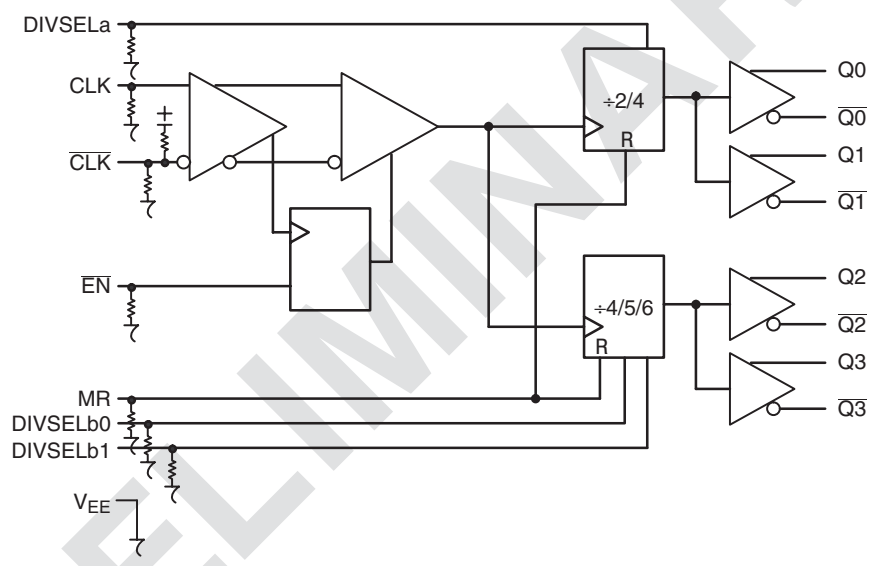


Figure 2. Logic Diagram

FUNCTION TABLES

CLK	$\overline{\text{EN}}$	$\overline{\text{MR}}$	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold Q0:3
X	X	H	Reset Q0:3

Z = Low-to-High Transition
ZZ = High-to-Low Transition

DIVSELa	Q0:1 OUTPUTS	
L	Divide by 2	
H	Divide by 4	
DIVSELb0	DIVSELb1	Q2:3 OUTPUTS
L	L	Divide by 4
H	L	Divide by 6
L	H	Divide by 5
H	H	Divide by 5

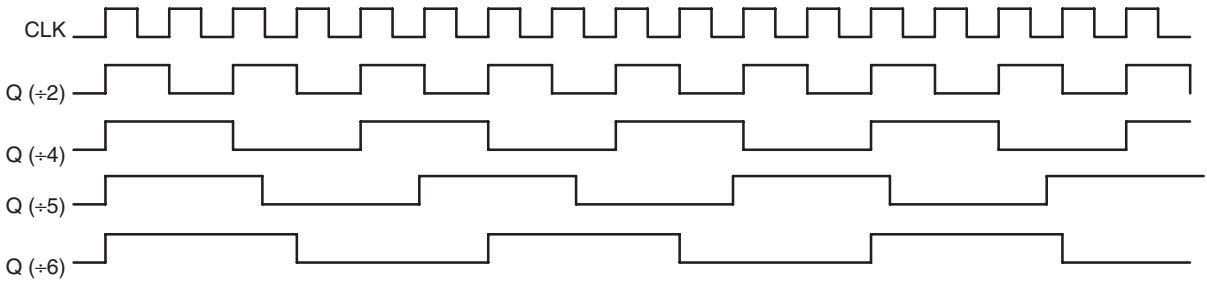


Figure 3. Timing Diagram

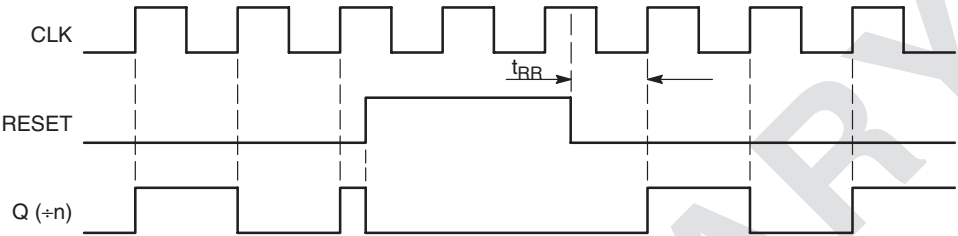


Figure 4. Timing Diagram

Table 1. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 k Ω
Internal Input Pullup Resistor		75 k Ω
ESD Protection	Human Body Model	> 2 kV
	Machine Model	> 100 V
	Charged Device Model	> 2 kV
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

Table 2. MAXIMUM RATINGS^a

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		4.6	V
V _{EE}	ECL Mode Power Supply	V _{CC} = 0 V		−4.6	V
V _I	PECL Mode Input Voltage ECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	4.6 −4.6	V V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
T _A	Operating Temperature Range			−40 to +85	°C
T _{stg}	Storage Temperature Range			−65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	20 TSSOP 20 TSSOP	TBD TBD	°C/W °C/W
		0 LFPM 500 LFPM	20 SOIC 20 SOIC	TBD TBD	°C/W °C/W

a Maximum Ratings are those values beyond which device damage may occur.

Table 3. DC CHARACTERISTICS, PECL (V_{CC} = 2.5 V±5%, V_{EE} = 0 V)

Symbol	Characteristic	−40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current		35			35		mA
V _{OH}	Output HIGH Voltage ^a	1415	1495	1620	1475	1545	1620	mV
V _{OL}	Output LOW Voltage ^a	670	805	945	690	795	880	mV
V _{IH}	Input HIGH Voltage (Single-Ended)	1335		1620	1335		1620	mV
V _{IL}	Input LOW Voltage (Single-Ended)	690		1025	690		1025	mV
V _{BB}	Output Reference Voltage	1120		1240	1120		1240	mV
V _{PP}	Differential Input Voltage ^b	0.12		1.3	0.12		1.3	V
V _{CMR}	Differential Cross Point Voltage ^c	1.0		V _{CC} −0.8	1.0		V _{CC} −0.8	V
I _{IH}	Input HIGH Current			150			150	μA
I _{IL}	Input LOW Current	0.5			0.5			μA

NOTE: ES6014 circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

a Output termination voltage V_{TT} = 0V for V_{CC} = 2.5V operation is supported but the power consumption of the device will increase.

b V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.

c V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 4. DC CHARACTERISTICS, PECL ($V_{CC} = 3.3 \text{ V} \pm 5\%$, $V_{EE} = 0 \text{ V}$)

Symbol	Characteristic	-40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		33			33		mA
V_{OH}	Output HIGH Voltage ^a	2215	2295	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage ^a	1470	1605	1745	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	mV
V_{BB}	Output Reference Voltage	1920		2040	1920		2040	mV
V_{PP}	Differential Input Voltage ^b	0.12		1.3	0.12		1.3	V
V_{CMR}	Differential Cross Point Voltage ^c	1.0		$V_{CC}-0.8$	1.0		$V_{CC}-0.8$	V
I_{IH}	Input HIGH Current			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			μA

NOTE: MC100ES6139 circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lpm is maintained.

a All loading with 50Ω to $V_{CC}-2.0$ volts.

b V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.

c V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 5. DC CHARACTERISTICS, ECL ($V_{CC} = 0 \text{ V}$, $V_{EE} = -3.0 \text{ V} \pm 5\%$)

Symbol	Characteristic	-40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		33			33		mA
V_{OH}	Output HIGH Voltage ^a	-1085	-100 5	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage ^a	-1830	-169 5	-155 5	-1810	-170 5	-162 0	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1810		-147 5	-1810		-147 5	mV
V_{BB}	Output Reference Voltage	-1380		-126 0	-1380		-126 0	mV
V_{PP}	Differential Input Voltage ^b	0.12		1.3	0.12		1.3	V
V_{CMR}	Differential Cross Point Voltage ^c	$V_{EE}+0.5$		-0.3	$V_{EE}+0.5$		-0.3	V
I_{IH}	Input HIGH Current			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			μA

NOTE: MC100ES6139 circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lpm is maintained.

a All loading with 50Ω to $V_{CC}-2.0$ volts.

b V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.

c V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 6. DC CHARACTERISTICS, HSTL ($V_{CC} = 2.375\text{ V to }3.8\text{ V}$, $V_{EE} = 0\text{ V}$)

Symbol	Characteristic	-40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage (Single Ended)	1200			1200			mV
V_{IL}	Input LOW Voltage (Single Ended)			400			400	mV

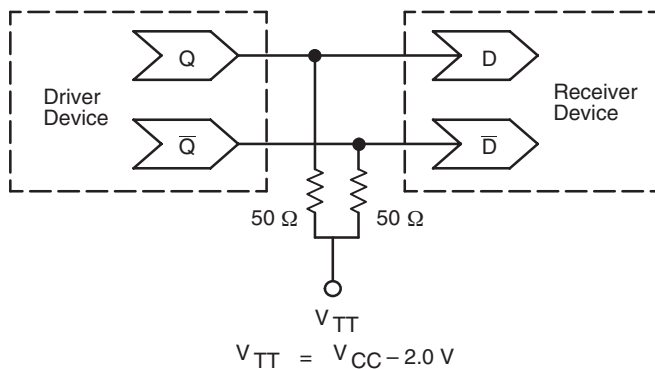
Table 7. AC CHARACTERISTICS ($V_{CC} = 0\text{ V}$; $V_{EE} = -3.0\text{ V}$ or $V_{CC} = 3.0\text{ V}$; $V_{EE} = 0\text{ V}$)^a

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency		> 1			> 1			> 1		GHz
t_{PLH} , t_{PHL}	Propagation Delay CLK, Q (Diff) MR, Q	550 700	700 800	800 900	600 700	750 850	900 1000	675 800	825 950	975 1100	ps
t_{RR}	Reset Recovery	200	100		200	100		200	100		ps
t_s	Setup Time EN, CLK DIVSEL, CLK	200 400	120 180		200 400	120 180		200 400	120 180		ps
t_h	Hold Time CLK, EN CLK, DIVSEL	100 200	50 140		100 200	50 140		100 200	50 140		ps
t_{PW}	Minimum Pulse Width MR	550	450		550	450		550	450		ps
t_{SKEW}	Within Device Skew Q, $\bar{Q}$ Device-to-Device Skew ^b		50 200	100 300		50 200	100 300		50 200	100 300	ps
t_{JITTER}	Cycle-to-Cycle Jitter		< 2			< 2			< 2		ps
V_{PP}	Input Voltage Swing (Differential)	150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Differential Cross Point Voltage PECL ECL	0.2 $V_{EE}+0.2$		$V_{CC}-1.1$ -1.1	0.2 $V_{EE}+0.2$		$V_{CC}-1.1$ -1.1	0.2 $V_{EE}+0.2$		$V_{CC}-1.1$ -1.1	V
t_r t_f	Output Rise/Fall Times (20% – 80%) Q, $\bar{Q}$	110	180	250	125	190	275	150	215	300	ps

a Measured using a 750 mV source, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC}-2.0\text{ V}$.

b Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

7

**Figure 5. Typical Termination for Output Driver and Device Evaluation**

Marking Notes:

Device Nomenclature	20-Lead TSSOP Marking	20-Lead SOIC W/B Marking
MC100ES6139DT	6139	
MC100ES6139DW		MC100ES6139

Trace Code Identification for 20 SOIC: AWLYYWW

“A” – The First character indicates the Assembly location.

“WL” – The Second & Third characters indicate the Source Wafer Lot Tracking Code.

“YY” – The Fourth & Fifth characters indicate the Year device was assembled.

“WW” – The Sixth & Seventh characters indicate the Work Week device was assembled.

Trace Code Identification for 20 TSSOP: ALYW

“A” – The First character indicates the Assembly location.

“L” – The Second character indicates the Source Wafer Lot Tracking Code.

“Y” – The Third character indicates the “ALPHA CODE” of the year device was assembled.

“W” – The Fourth character indicates the “ALPHA CODE” of the Work Week device was assembled.

The “Y” Year ALPHA CODES**The “W” Work Week ALPHA CODES**

Year	Month	Work Week Code	1st 6 Months (WW01 – WW26)	2nd 6 Months (WW27 – WW52)
A = 2003	FIRST 6 MONTHS	WW01 – WW26	A = WW01	A = WW27
B = 2003	SECOND 6 MONTHS	WW27 – WW52	B = WW02	B = WW28
C = 2004	FIRST 6 MONTHS	WW01 – WW26	C = WW03	C = WW29
D = 2004	SECOND 6 MONTHS	WW27 – WW52	D = WW04	D = WW30
E = 2005	FIRST 6 MONTHS	WW01 – WW26	E = WW05	E = WW31
F = 2005	SECOND 6 MONTHS	WW27 – WW52	F = WW06	F = WW32
G = 2006	FIRST 6 MONTHS	WW01 – WW26	G = WW07	G = WW33
H = 2006	SECOND 6 MONTHS	WW27 – WW52	H = WW08	H = WW34
I = 2007	FIRST 6 MONTHS	WW01 – WW26	I = WW09	I = WW35
J = 2007	SECOND 6 MONTHS	WW27 – WW52	J = WW10	J = WW36
K = 2008	FIRST 6 MONTHS	WW01 – WW26	K = WW11	K = WW37
L = 2008	SECOND 6 MONTHS	WW27 – WW52	L = WW12	L = WW38
M = 2009	FIRST 6 MONTHS	WW01 – WW26	M = WW13	M = WW39
N = 2009	SECOND 6 MONTHS	WW27 – WW52	N = WW14	N = WW40
O = 2010	FIRST 6 MONTHS	WW01 – WW26	O = WW15	O = WW41
P = 2010	SECOND 6 MONTHS	WW27 – WW52	P = WW16	P = WW42
Q = 2011	FIRST 6 MONTHS	WW01 – WW26	Q = WW17	Q = WW43
R = 2011	SECOND 6 MONTHS	WW27 – WW52	R = WW18	R = WW44
S = 2012	FIRST 6 MONTHS	WW01 – WW26	S = WW19	S = WW45
T = 2012	SECOND 6 MONTHS	WW27 – WW52	T = WW20	T = WW46
U = 2013	FIRST 6 MONTHS	WW01 – WW26	U = WW21	U = WW47
V = 2013	SECOND 6 MONTHS	WW27 – WW52	V = WW22	V = WW48
W = 2014	FIRST 6 MONTHS	WW01 – WW26	W = WW23	W = WW49
X = 2014	SECOND 6 MONTHS	WW27 – WW52	X = WW24	X = WW50
Y = 2015	FIRST 6 MONTHS	WW01 – WW26	Y = WW25	Y = WW51
Z = 2015	SECOND 6 MONTHS	WW27 – WW52	Z = WW26	Z = WW52

20 TSSOP Tracecode Marking Example:

5ABR

| | |

5 | | | = Assembly Location

| | |

A | | = First Lot Assembled of this device in the designated Work Week

| |

B | = 2003 Second 6 Months, WW27 – WW52

|

R = WW44 of 2003

Low Voltage 2.5/3.3V Differential ECL/PECL/HSTL Fanout Buffer

The Motorola MC100ES6210 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6210 supports various applications that require to distribute precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low clock skew outputs and superior digital signal characteristics. Target applications for this clock driver is high performance clock distribution in computing, networking and telecommunication systems.

Features:

- Dual 1:5 differential clock distribution
- 30 ps maximum device skew
- Fully differential architecture from input to all outputs
- SiGe technology supports near-zero output skew
- Supports DC to 3GHz operation of clock or data signals
- ECL/PECL compatible differential clock outputs
- ECL/PECL compatible differential clock inputs
- Single 3.3V, -3.3V, 2.5V or -2.5V supply
- Standard 32 lead LQFP package
- Industrial temperature range
- Pin and function compatible to the MC100EP210

Functional Description

The MC100ES6210 is designed for low skew clock distribution systems and supports clock frequencies up to 3 GHz. The device consists of two independent 1:5 clock fanout buffers. The input signal of each fanout buffer is distributed to five identical, differential ECL/PECL outputs. Both CLKA and CLKB inputs can be driven by ECL/PECL compatible signals.

If VBB is connected to the CLKA or CLKB input and bypassed to GND by a 10 nF capacitor, the MC100ES6210 can be driven by single-ended ECL/PECL signals utilizing the VBB bias voltage output.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The MC100ES6210 can be operated from a single 3.3V or 2.5V supply. As most other ECL compatible devices, the MC100ES6210 supports positive (PECL) and negative (ECL) supplies. The is function and pin compatible to the MC100EP210.

MC100ES6210

**LOW VOLTAGE DUAL
1:5 DIFFERENTIAL
PECL/ECL/HSTL
CLOCK FANOUT BUFFER**



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A

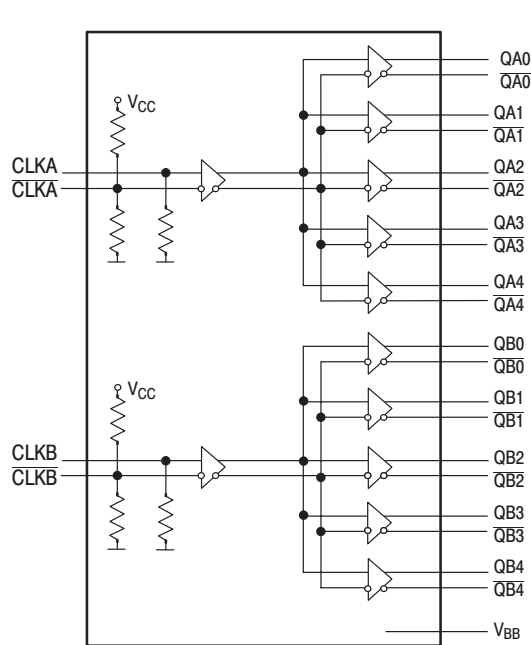


Figure 1. MC100ES6210 Logic Diagram

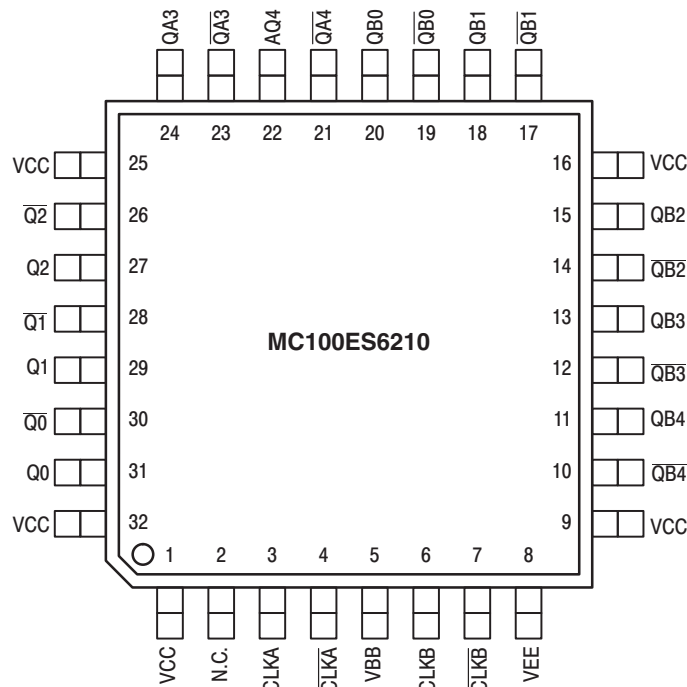


Figure 2. 32-Lead Package Pinout (Top View)

Table 1. Pin configuration

Pin	I/O	Type	Function
CLKA, $\overline{\text{CLKA}}$	Input	ECL/PECL	Differential reference clock signal input (fanout buffer A)
CLKB, $\overline{\text{CLKB}}$	Input	ECL/PECL	Differential reference clock signal input (fanout buffer B)
QA[0-4], $\overline{\text{QA}}$ [0-4]	Output	ECL/PECL	Differential clock outputs (fanout buffer A)
QB[0-4], $\overline{\text{QB}}$ [0-4]	Output	ECL/PECL	Differential clock outputs (fanout buffer B)
VEE ^a	Supply		Negative power supply
VCC	Supply		Positive power supply. All VCC pins must be connected to the positive power supply for correct DC and AC operation.
VBB	Output	DC	Reference voltage output for single ended ECL or PECL operation

a. In ECL mode (negative power supply mode), VEE is either -3.3V or -2.5V and VCC is connected to GND (0V).
In PECL mode (positive power supply mode), VEE is connected to GND (0V) and VCC is either +3.3V or +2.5V .
In both modes, the input and output levels are referenced to the most positive supply (VCC).

Table 2. ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	3.6	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} + 0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} + 0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output termination voltage		V _{CC} - 2 ^a		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model)				V	
LU	Latch-up immunity	200			mA	
C _{IN}			4.0		pF	Inputs
θ _{JA}	Thermal resistance junction to ambient JESD 51-3, single layer tes board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ _{JC}	Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
T _J	Operating junction temperature ^b (continuous operation) MTBF = 9.1 years			110	°C	

- a. Output termination voltage V_{TT} = 0V for V_{CC} = 2.5V operation is supported but the power consumption of the device will increase
- b. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6210 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6210 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 4. PECL DC Characteristics ($V_{CC} = 2.5V \pm 5\%$ or $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = \text{GND}$, $T_J = 0^\circ\text{C}$ to $+110^\circ\text{C}$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLKA , $\overline{\text{CLKA}}$, CLKB , $\overline{\text{CLKB}}$ (PECL differential signals)						
V_{PP}	Differential input voltage ^a	0.1		1.3	V	Differential operation
V_{CMR}	Differential cross point voltage ^b	1.0		$V_{CC} - 0.3$	V	Differential operation
I_{IN}	Input Current ^a			± 100	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
PECL clock outputs (QA0-4 , $\overline{\text{QA0-4}}$, QB0-4 , $\overline{\text{QB0-4}}$)						
V_{OH}	Output High Voltage	$V_{CC} - 1.2$	$V_{CC} - 1.005$	$V_{CC} - 0.7$	V	$I_{OH} = -30 \text{ mA}^c$
V_{OL}	Output Low Voltage $V_{CC} = 3.3V \pm 5\%$ $V_{CC} = 2.5V \pm 5\%$	$V_{CC} - 1.9$ $V_{CC} - 1.9$	$V_{CC} - 1.705$ $V_{CC} - 1.705$	$V_{CC} - 1.5$ $V_{CC} - 1.3$	V	$I_{OL} = -5 \text{ mA}^c$
Supply current and V_{BB}						
I_{EE}	Maximum Quiescent Supply Current without output termination current		60	100	mA	V_{EE} pin
V_{BB}	Output reference voltage	$V_{CC} - 1.38$	$V_{CC} - 1.26$	$V_{CC} - 1.14$	V	$I_{BB} = 0.2 \text{ mA}$

a. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality

b. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

c. Equivalent to a termination of 50Ω to V_{TT} .

Table 5. ECL DC Characteristics ($V_{EE} = -2.5V \pm 5\%$ or $V_{EE} = -3.3V \pm 5\%$, $V_{CC} = \text{GND}$, $T_J = 0^\circ\text{C}$ to $+110^\circ\text{C}$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLKA , $\overline{\text{CLKA}}$, CLKB , $\overline{\text{CLKB}}$ (ECL differential signals)						
V_{PP}	Differential input voltage ^a	0.1		1.3	V	Differential operation
V_{CMR}	Differential cross point voltage ^b	$V_{EE} + 1.0$		-0.3	V	Differential operation
I_{IN}	Input Current ^a			± 100	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
ECL clock outputs (QA0-4 , $\overline{\text{QA0-4}}$, QB0-4 , $\overline{\text{QB0-4}}$)						
V_{OH}	Output High Voltage	-1.2	-1.005	-0.7	V	$I_{OH} = -30 \text{ mA}^c$
V_{OL}	Output Low Voltage $V_{CC} = 3.3V \pm 5\%$ $V_{CC} = 2.5V \pm 5\%$	-1.9 -1.9	-1.705 -1.705	-1.5 -1.3	V	$I_{OL} = -5 \text{ mA}^c$
Supply current and V_{BB}						
I_{EE}	Maximum Quiescent Supply Current without output termination current		60	100	mA	V_{EE} pin
V_{BB}	Output reference voltage	-1.38	-1.26	-1.14	V	$I_{BB} = 0.2 \text{ mA}$

a. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality

b. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

c. Equivalent to a termination of 50Ω to V_{TT} .

Table 6. AC Characteristics (ECL: $V_{EE} = -3.3V \pm 5\%$ or $V_{EE} = -2.5V \pm 5\%$, $V_{CC} = GND$) or
(PECL: $V_{CC} = 3.3V \pm 5\%$ or $V_{CC} = 2.5V \pm 5\%$, $V_{EE} = GND$, $T_J = 0^\circ C$ to $+110^\circ C$)^{a b}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLKA, $\overline{CLKA}$, CLKB, $\overline{CLKB}$ (PECL or ECL differential signals)						
V _{PP}	Differential input voltage ^c (peak-to-peak)	0.3	0.3	1.3	V	
V _{CMR}	Differential input crosspoint voltage ^d PECL ECL	1.2 V _{EE} +1.2		V _{CC} - 0.3 -0.3V	V V	
ECL clock outputs (Q0-9, $\overline{Q0-9}$)						
f _{CLK}	Input Frequency	0		3000	MHz	Differential
t _{PD}	Propagation Delay CLKA to QAx or CLKB to QBx	175	260	350	ps	Differential
V _{O(P-P)}	Differential output voltage (peak-to-peak) f _O < 1.1 GHz f _O < 2.5 GHz f _O < 3.0 GHz	0.45 0.35 0.20	0.70 0.55 0.35		V V V	
t _{sk(O)}	Output-to-output skew (per bank)		13	30	ps	Differential
t _{sk(PP)}	Output-to-output skew (part-to-part)			175	ps	Differential
t _{JIT(CC)}	Output cycle-to-cycle jitter			TBD		
t _{SK(P)}	Output pulse skew ^e			50	ps	
DC _Q	Output Duty Cycle f _{REF} < 0.1 GHz f _{REF} < 1.0 GHz	49.5 45.0	50 50	50.5 55.0	% %	DC _{REF} = 50% DC _{REF} = 50%
t _r , t _f	Output Rise/Fall Time	30		250	ps	20% to 80%

- a. AC characteristics are design targets and pending characterization.
b. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
c. V_{PP} (AC) is the minimum differential ECL/PECL input voltage swing required to maintain AC characteristics including t_{pd} and device-to-device skew.
d. V_{CMR} (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.
e. Output pulse skew is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.

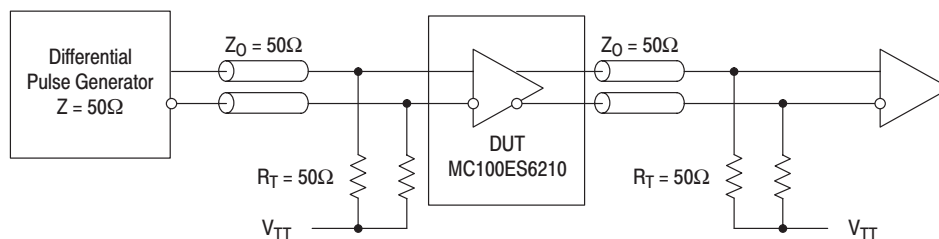


Figure 3. MC100ES6210 AC test reference

Low Voltage Dual 1:10 Differential ECL/PECL Clock Fanout Buffer

The Motorola MC100ES6220 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6220 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are high performance clock distribution in computing, networking and telecommunication systems.

Features

- Two independent 1:10 differential clock fanout buffers
- 130 ps maximum device skew
- SiGe technology
- Supports DC to 1GHz operation of clock or data signals
- ECL/PECL compatible differential clock outputs
- ECL/PECL compatible differential clock inputs
- Single 3.3V, -3.3V, 2.5V or -2.5V supply
- Standard 52 lead LQFP package with exposed pad for enhanced thermal characteristics
- Supports industrial temperature range
- Pin and function compatible to the MC100EP220

Functional Description

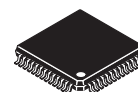
The MC100ES6220 is designed for low skew clock distribution systems and supports clock frequencies up to 1 GHz. The device consists of two independent clock fanout buffers. The CLKA and CLKB inputs can be driven by ECL or PECL compatible signals. The input signal of each clock buffer is distributed to 10 identical, differential ECL/PECL outputs. If VBB is connected to the $\overline{\text{CLKA}}$ or $\overline{\text{CLKB}}$ input and bypassed to GND by a 10 nF capacitor, the MC100ES6220 can be driven by single-ended ECL/PECL signals utilizing the VBB bias voltage output.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The MC100ES6220 can be operated from a single 3.3V or 2.5V supply. As most other ECL compatible devices, the MC100ES6220 supports positive (PECL) and negative (ECL) supplies. The MC100ES6220 is pin and function compatible to the MC100EP220.

MC100ES6220

**LOW VOLTAGE DUAL 1:10
DIFFERENTIAL ECL/PECL
CLOCK FANOUT BUFFER**



TB SUFFIX
52-LEAD LQFP PACKAGE
EXPOSED PAD
CASE 1336A

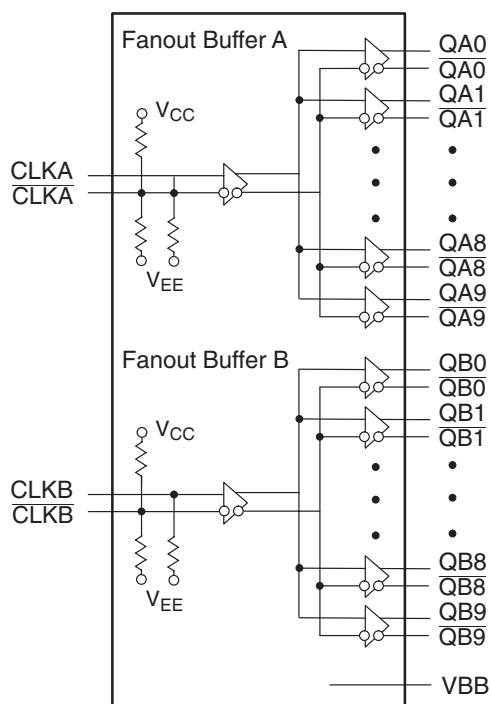


Figure 1. MC100ES6220 Logic Diagram

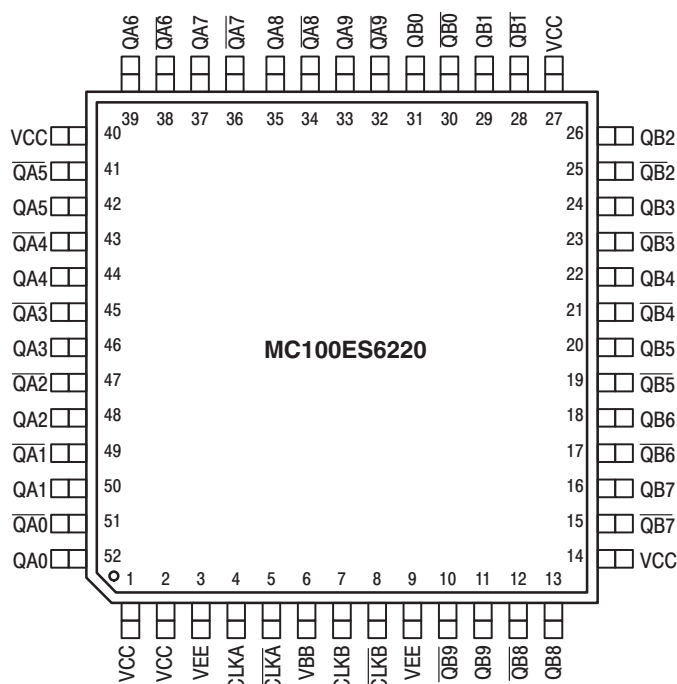


Figure 2. 52-Lead Package Pinout (Top View)

Table 1. Pin configuration

Pin	I/O	Type	Function
CLKA, $\overline{\text{CLKA}}$	Input	ECL/PECL	Differential reference clock signal input for fanout buffer A
CLKB, $\overline{\text{CLKB}}$	Input	ECL/PECL	Differential reference clock signal input for fanout buffer B
QA[0-9], $\overline{\text{QA}}[0-9]$	Output	ECL/PECL	Differential clock outputs of fanout buffer A
QB[0-9], $\overline{\text{QB}}[0-9]$	Output	ECL/PECL	Differential clock outputs of fanout buffer B
VEE ^a	Supply		Negative power supply
VCC	Supply		Positive power supply. All VCC pins must be connected to the positive power supply for correct DC and AC operation.
VBB	Output	DC	Reference voltage output for single ended ECL or PECL operation

a. In ECL mode (negative power supply mode), VEE is either -3.3V or -2.5V and VCC is connected to GND (0V). In PECL mode (positive power supply mode), VEE is connected to GND (0V) and VCC is either +3.3V or +2.5V. In both modes, the input and output levels are referenced to the most positive supply (VCC).

Table 2. Absolute Maximum Ratings^a

Symbol	Characteristics	Min	Max	Unit	Condition
VCC	Supply Voltage	-0.3	3.6	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} + 0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} + 0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage temperature	-65	125	°C	
T _{FUNC}	Functional temperature range	T _A = -40	T _J = +110	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		$V_{CC} - 2^a$		V	
MM	ESD Protection (Machine model)	175			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model)	TBD			V	
LU	Latch-up immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}, θ_{JC} θ_{JB}	Thermal resistance (junction-to-ambient, junction-to-board, junction-to-case)	See Table 8, Thermal Resistance, on page 702			°C/W	
T_J	Operating junction temperature ^b (continuous operation) MTBF = 9.1 years	0		110	°C	

- a. Output termination voltage $V_{TT} = 0V$ for $V_{CC} = 2.5V$ operation is supported but the power consumption of the device will increase.
- b. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6220 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6220 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 4. PECL DC Characteristics ($V_{CC} = 2.5V \pm 5\%$ or $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = GND$, $T_J = 0^\circ C$ to $+110^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair $CLKA, \overline{CLKA}, CLKB, \overline{CLKB}$ (PECL differential signals)						
V_{PP}	Differential input voltage ^a	0.1		1.3	V	Differential operation
V_{CMR}	Differential cross point voltage ^b	1.0		$V_{CC} - 0.3$	V	Differential operation
I_{IN}	Input Current ^a			± 150	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock inputs (PECL single ended signals)						
V_{IH}	Input Voltage High	$V_{CC} - 1.165$		$V_{CC} - 0.880$	V	
V_{IL}	Input Voltage Low	$V_{CC} - 1.810$		$V_{CC} - 1.475$	V	
I_{IN}	Input Current ^c			± 150	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
PECL clock outputs (QA0-A9, QA0-A9, QB0-B9, QB0-B9)						
V_{OH}	Output High Voltage	$V_{CC} - 1.1$	$V_{CC} - 1.005$	$V_{CC} - 0.7$	V	$I_{OH} = -30 \text{ mA}^d$
V_{OL}	Output Low Voltage	$V_{CC} - 1.9$	$V_{CC} - 1.705$	$V_{CC} - 1.4$	V	$I_{OL} = -5 \text{ mA}^d$
Supply current and V_{BB}						
I_{EE}^e	Maximum Quiescent Supply Current without output termination current		80	130	mA	V_{EE} pins
V_{BB}	Output reference voltage	$V_{CC} - 1.42$		$V_{CC} - 1.20$	V	$I_{BB} = 0.3 \text{ mA}$

- a. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
- b. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
- c. Input have internal pullup/pulldown resistors which affect the input current.
- d. Termination 50Ω to V_{TT} .
- e. I_{CC} calculation: $I_{CC} = (\text{number of differential output used}) \times (I_{OH} + I_{OL}) + I_{EE}$
 $I_{CC} = (\text{number of differential output used}) \times (V_{OH} - V_{TT}) / R_{load} + (V_{OL} - V_{TT}) / R_{load} + I_{EE}$.

Table 5. ECL DC Characteristics ($V_{EE} = -2.5V \pm 5\%$ or $V_{EE} = -3.3V \pm 5\%$, $V_{CC} = GND$, $T_J = 0^\circ C$ to $+110^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLKA, $\overline{CLKA}$, CLKB, $\overline{CLKB}$ (ECL differential signals)						
V_{PP}	Differential input voltage ^a	0.1		1.3	V	Differential operation
V_{CMR}	Differential cross point voltage ^b	$V_{EE} + 1.0$		-0.3	V	Differential operation
I_{IN}	Input Current ^a			± 150	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock inputs (ECL single ended signals)						
V_{IH}	Input Voltage High	-1.165		-0.880	V	
V_{IL}	Input Voltage Low	-1.810		-1.475	V	
I_{IN}	Input Current ^c			± 150	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
ECL clock outputs (QA0-A9, $\overline{QA0-A9}$, QB0-B9, $\overline{QB0-B9}$)						
V_{OH}	Output High Voltage	-1.1	-1.005	-0.7	V	$I_{OH} = -30 \text{ mA}^d$
V_{OL}	Output Low Voltage	-1.9	-1.705	-1.4	V	$I_{OL} = -5 \text{ mA}^d$
Supply current and V_{BB}						
I_{EE}^e	Maximum Quiescent Supply Current without output termination current		80	130	mA	V_{EE} pins
V_{BB}	Output reference voltage	-1.42		-1.20	V	$I_{BB} = 0.3 \text{ mA}$

a. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.

b. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

c. Input have internal pullup/pulldown resistors which affect the input current.

d. Termination 50Ω to V_{TT} .

e. I_{CC} calculation: $I_{CC} = (\text{number of differential output used}) \times (I_{OH} + I_{OL}) + I_{EE}$

$I_{CC} = (\text{number of differential output used}) \times (V_{OH} - V_{TT}) \div R_{load} + (V_{OL} - V_{TT}) \div R_{load} + I_{EE}$.

Table 6. AC Characteristics (ECL: $V_{EE} = -3.3V \pm 5\%$ or $V_{EE} = -2.5V \pm 5\%$, $V_{CC} = GND$) or (PECL: $V_{CC} = 3.3V \pm 5\%$ or $V_{CC} = 2.5V \pm 5\%$, $V_{EE} = GND$, $T_J = 0^\circ C$ to $+110^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair $\overline{CLKA}$, $\overline{CLKA}$, $\overline{CLKB}$, $\overline{CLKB}$ (PECL or ECL differential signals)						
V_{PP}	Differential input voltage ^b (peak-to-peak)	0.3		1.3	V	
V_{CMR}	Differential input crosspoint voltage ^c	PECL ECL 1.1 $V_{EE}+1.1$		$V_{CC}-0.3$ -0.3V	V V	
f_{CLK}	Input Frequency	0		1000	MHz	Differential
PECL/ECL clock outputs ($\overline{QA0-A9}$, $\overline{QA0-A9}$, $\overline{QB0-B9}$, $\overline{QB0-B9}$)						
t_{PD}	Propagation Delay $CLKx$ to $Qx0-9$	285		550	ps	Differential
$V_{O(P-P)}$	Differential output voltage (peak-to-peak)	400	600		mV	
$t_{sk(O)}$	Output-to-output skew		60	130	ps	Differential
$t_{sk(PP)}$	Output-to-output skew (part-to-part)			200	ps	Differential
$t_{JIT(CC)}$	Output cycle-to-cycle jitter			TBD	ps	
$t_{SK(P)}$	Output pulse skew ^d			35	ps	
DC_O	Output Duty Cycle	$f_{REF} < 0.1$ GHz	49.65	50	50.35	$DC_{REF} = 50\%$
		$f_{REF} < 1.0$ GHz	46.5	50	53.5	$DC_{REF} = 50\%$
t_r, t_f	Output Rise/Fall Time	50		350	ps	20% to 80%

- a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
- b. V_{PP} (AC) is the minimum differential ECL/PECL input voltage swing required to maintain AC characteristics including t_{pd} and device-to-device skew.
- c. V_{CMR} (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.
- d. Output pulse skew is the absolute difference of the propagation delay times: $|t_{pLH} - t_{pHL}|$.

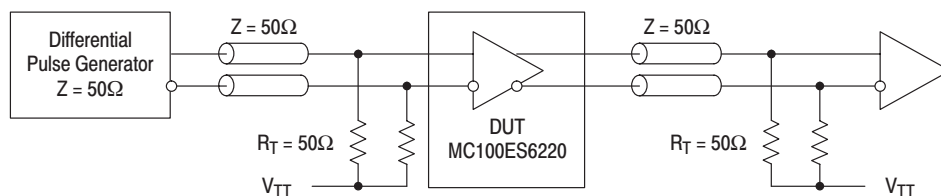


Figure 3. MC100ES6220 AC test reference

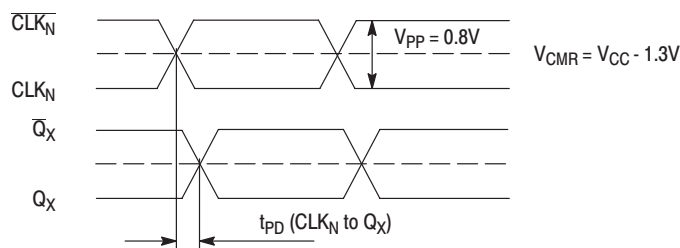


Figure 4. MC100ES6220 AC reference measurement waveform

APPLICATIONS INFORMATION

Understanding the junction temperature range of the MC100ES6220

To make the optimum use of high clock frequency and low skew capabilities of the MC100ES6220, the MC100ES6220 is specified, characterized and tested for the junction temperature range of $T_J=0^{\circ}\text{C}$ to $+110^{\circ}\text{C}$. Because the exact thermal performance depends on the PCB type, design, thermal management and natural or forced air convection, the junction temperature provides an exact way to correlate the application specific conditions to the published performance data of this datasheet. The correlation of the junction temperature range to the application ambient temperature range and vice versa can be done by calculation:

$$T_J = T_A + R_{thja} \cdot P_{tot}$$

Assuming a thermal resistance (junction to ambient) of 17°C/W (2s2p board, 200 ft/min airflow, see Table 8 on page 702) and a typical power consumption of 1049 mW (all outputs terminated 50 ohms to V_{TT} , $V_{CC}=3.3\text{V}$, frequency independent), the junction temperature of the MC100ES6220 is approximately $T_A + 18^{\circ}\text{C}$, and the minimum ambient temperature in this example case calculates to -18°C (the maximum ambient temperature is 92°C . See Table 7). Exceeding the minimum junction temperature specification of the MC100ES6220 does not have a significant impact on the device functionality. However, the continuous use the MC100ES6220 at high ambient temperatures requires thermal management to not exceed the specified maximum junction temperature. Please see the application note AN1545 for a power consumption calculation guideline.

Table 7. Ambient temperature ranges ($P_{tot} = 1049\text{mW}$)

R_{thja} (2s2p board)		T_A, min^a	T_A, max
Natural convection	20°C/W	-21°C	89°C
100 ft/min	18°C/W	-19°C	91°C
200 ft/min	17°C/W	-18°C	92°C
400 ft/min	16°C/W	-17°C	93°C
800 ft/min	15°C/W	-16°C	94°C

a. The MC100ES6220 device function is guaranteed from $T_A=-40^{\circ}\text{C}$ to $T_J=110^{\circ}\text{C}$

Maintaining Lowest Device Skew

The MC100ES6220 guarantees low output-to-output bank skew of 100 ps and a part-to-part skew of max. 200 ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. This will reduce the device power consumption while maintaining minimum output skew.

Power Supply Bypassing

The MC100ES6220 is a mixed analog/digital product. The differential architecture of the MC100ES6220 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

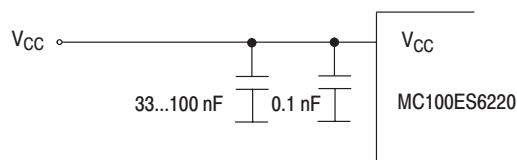


Figure 5. V_{CC} Power Supply Bypass

APPLICATIONS INFORMATION

Using the thermally enhanced package of the MC100ES6220

The MC100ES6220 uses a thermally enhanced exposed pad (EP) 100 lead LQFP package. The package is molded so that the leadframe is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance that supports the power consumption of the MC100ES6220 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100ES6220. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is a requirement for MC100ES6220 applications on multi-layer boards. The recommended thermal land design comprises a 3 x 3 thermal via array as shown in Figure 6 “Recommended thermal land pattern”, providing an efficient heat removal path.

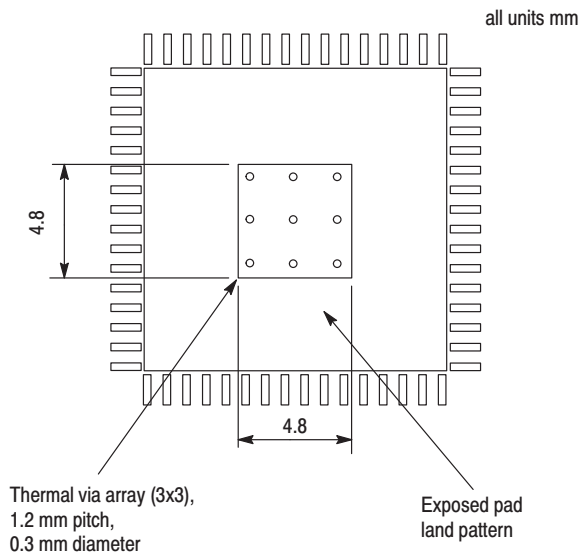


Figure 6. Recommended thermal land pattern

The via diameter should be approx. 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. Figure 7 “Recommended solder mask openings” shows a recommended solder mask

opening with respect to the recommended 3 x 3 thermal via array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as shown in Figure 7 For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

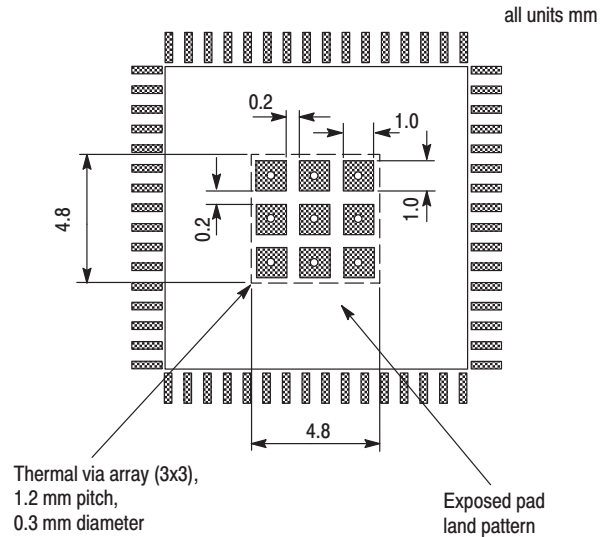


Figure 7. Recommended solder mask openings

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

Table 8. Thermal Resistance^a

Convection-LFPM	R_{THJA}^b °C/W	R_{THJA}^c °C/W	R_{THJC} °C/W	R_{THJB}^d °C/W
Natural	20	48	4 ^e 29 ^f	16
100	18	47		
200	17	46		
400	16	43		
800	15	41		

- a. Applicable for a 3 x 3 thermal via array
- b. Junction to ambient, four conductor layer test board (2S2P), per JES51-7 and JESD 51-5
- c. Junction to ambient, single layer test board, per JESD51-3
- d. Junction to board, four conductor layer test board (2S2P) per JESD 51-8
- e. Junction to exposed pad
- f. Junction to top of package

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100ES6220 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.

Low Voltage 1:20 Differential ECL/PECL/HSTL Clock Fanout Buffer

The Motorola MC100ES6221 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6221 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver is high performance clock distribution in computing, networking and telecommunication systems.

Features

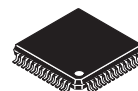
- 1:20 differential clock fanout buffer
- 100 ps maximum device skew
- SiGe technology
- Supports DC to 2 GHz operation of clock or data signals
- ECL/PECL compatible differential clock outputs
- ECL/PECL/HSTL compatible differential clock inputs
- Single 3.3V, -3.3V, 2.5V or -2.5V supply
- Standard 52 lead LQFP package with exposed pad for enhanced thermal characteristics
- Supports industrial temperature range
- Pin and function compatible to the MC100EP221

Functional Description

The MC100ES6221 is designed for low skew clock distribution systems and supports clock frequencies up to 2 GHz. The device accepts two clock sources. The CLK0 input can be driven by ECL or PECL compatible signals, the CLK1 input accepts HSTL compatible signals. The selected input signal is distributed to 20 identical, differential ECL/PECL outputs. If VBB is connected to the $\overline{\text{CLK0}}$ or $\overline{\text{CLK1}}$ input and bypassed to GND by a 10 nF capacitor, the MC100ES6221 can be driven by single-ended ECL/PECL signals utilizing the VBB bias voltage output.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The MC100ES6221 can be operated from a single 3.3V or 2.5V supply. As most other ECL compatible devices, the MC100ES6221 supports positive (PECL) and negative (ECL) supplies. The MC100ES6221 is pin and function compatible to the MC100EP221.

MC100ES6221**LOW-VOLTAGE
1:20 DIFFERENTIAL
ECL/PECL/HSTL
CLOCK FANOUT DRIVER****TB SUFFIX**
52-LEAD LQFP PACKAGE
EXPOSED PAD
CASE 1336A

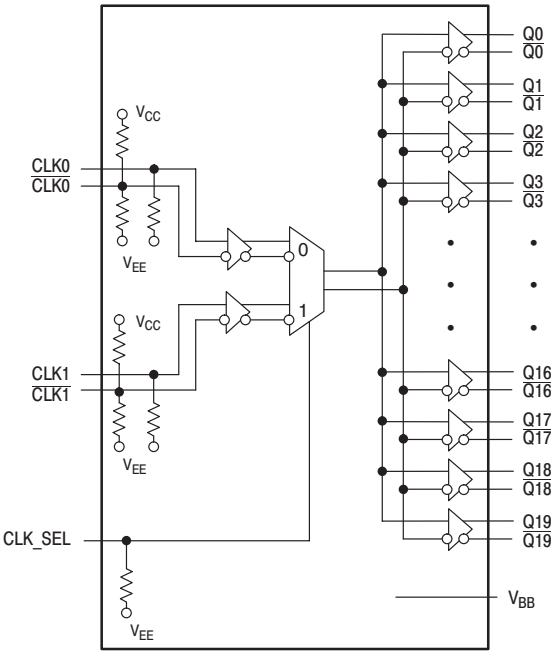


Figure 1. MC100ES6221 Logic Diagram

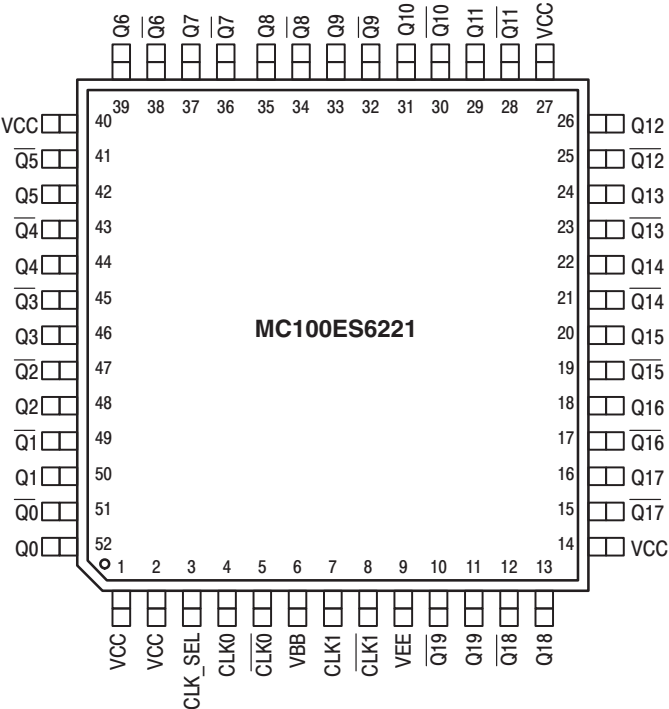


Figure 2. 52-Lead Package Pinout (Top View)

Table 1. PIN CONFIGURATION

Pin	I/O	Type	Function
CLK0, $\overline{\text{CLK0}}$	Input	ECL/PECL	Differential reference clock signal input
CLK1, $\overline{\text{CLK1}}$	Input	HSTL	Alternative differential reference clock signal input
CLK_SEL	Input	ECL/PECL	Reference clock input select
Q[0–19], $\overline{\text{Q}}[0–19]$	Output	ECL/PECL	Differential clock outputs
V_{EE}^a	Supply		Negative power supply
V_{CC}	Supply		Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
V_{BB}	Output	DC	Reference voltage output for single ended ECL or PECL operation

a. In ECL mode (negative power supply mode), V_{EE} is either -3.3V or -2.5V and V_{CC} is connected to GND (0V). In PECL mode (positive power supply mode), V_{EE} is connected to GND (0V) and V_{CC} is either $+3.3\text{V}$ or $+2.5\text{V}$. In both modes, the input and output levels are referenced to the most positive supply (V_{CC}).

Table 2. FUNCTION TABLE

Pin	0	1
CLK_SEL	CLK0, $\overline{\text{CLK0}}$ input pair is the reference clock. CLK0 can be driven by ECL or PECL compatible signals.	CLK1, $\overline{\text{CLK1}}$ input pair is the reference clock. CLK1 can be driven by HSTL compatible signals.

Table 3. Absolute Maximum Ratings^a

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.6	V	
V_{IN}	DC Input Voltage	-0.3	$V_{CC} + 0.3$	V	
V_{OUT}	DC Output Voltage	-0.3	$V_{CC} + 0.3$	V	
I_{IN}	DC Input Current		± 20	mA	
I_{OUT}	DC Output Current		± 50	mA	
T_S	Storage temperature	-65	125	°C	
T_{FUNC}	Functional temperature range	$T_A = -40$	$T_J = +110$	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		$V_{CC} - 2^a$		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model)	TBD			V	
LU	Latch-up immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
$\theta_{JA}, \theta_{JB}, \theta_{JC}$	Thermal resistance (junction-to-ambient, junction-to-board, junction-to-case)	See Table 9 "Thermal Resistance" on page 711			°C/W	
T_J	Operating junction temperature ^b (continuous operation) MTBF = 9.1 years	0		110	°C	

- a. Output termination voltage $V_{TT} = 0V$ for $V_{CC} = 2.5V$ operation is supported but the power consumption of the device will increase.
- b. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6221 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6221 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 5. PECL DC Characteristics ($V_{CC} = 2.5V \pm 5\%$ or $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = GND$, $T_J = 0^\circ C$ to $+110^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLK0, $\overline{CLK0}^a$ (PECL differential signals)						
V_{PP}	Differential input voltage ^b	0.1		1.3	V	Differential operation
V_{CMR}	Differential cross point voltage ^c	1.0		$V_{CC}-0.3$	V	Differential operation
I_{IN}	Input Current ^a			± 100	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock input pair CLK1, $\overline{CLK1}^d$ (HSTL differential signals)						
V_{DIF}	Differential input voltage ^e	0.2		1.4	V	
V_X	Differential cross point voltage ^f	0	0.68 – 0.9	$V_{CC}-0.7$	V	
V_{IH}	Input high voltage	$V_X+0.1$		$V_X+0.7$	V	
V_{IL}	Input low voltage	$V_X-0.7$		$V_X-0.1$	V	
I_{IN}	Input Current			± 100	μA	$V_{IN} = V_X \pm 0.2V$
Clock inputs (PECL single ended signals)						
V_{IH}	Input voltage high	$V_{CC}-1.165$		$V_{CC}-0.880$	V	
V_{IL}	Input voltage low	$V_{CC}-1.810$		$V_{CC}-1.475$	V	
I_{IN}	Input Current ^g			± 100	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
PECL clock outputs (Q0-19, $\overline{Q0-19}$)						
V_{OH}	Output High Voltage	$V_{CC}-1.1$	$V_{CC}-1.005$	$V_{CC}-0.7$	V	$I_{OH} = -30 \text{ mA}^h$
V_{OL}	Output Low Voltage	$V_{CC}-1.9$	$V_{CC}-1.705$	$V_{CC}-1.4$	V	$I_{OL} = -5 \text{ mA}^h$
Supply current and V_{BB}						
I_{EEI}	Maximum Quiescent Supply Current without output termination current		84	160	mA	V_{EE} pins
V_{BB}	Output reference voltage ($f_{ref} < 1.0 \text{ GHz}$) ^j	$V_{CC}-1.42$		$V_{CC}-1.20$	V	$I_{BB} = 0.4 \text{ mA}$

- a. The input pairs CLK0, CLK1 are compatible to differential signaling standards. CLK0 is compatible to LVPECL signals and CLK1 meets both HSTL differential signal specifications. The difference between CLK0 and CLK1 is the differential input threshold voltage (V_{CMR}).
- b. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
- c. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
- d. Clock inputs driven by differential HSTL compatible signals. Only applicable to CLK1, $\overline{CLK1}$.
- e. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality.
- f. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.
- g. Inputs have internal pullup/pulldown resistors which affect the input current.
- h. Equivalent to a termination of 50Ω to V_{TT} .
- i. I_{CC} calculation: $I_{CC} = (\text{number of differential output used}) \times (I_{OH} + I_{OL}) + I_{EE}$
 $I_{CC} = (\text{number of differential output used}) \times (V_{OH} - V_{TT}) \div R_{load} + (V_{OL} - V_{TT}) \div R_{load} + I_{EE}$.
- j. Using V_{BB} to bias unused single-ended inputs is recommended only up to a clock reference frequency of 1 GHz. Above 1 GHz, only differential input signals should be used with the MC100ES6221.

Table 6. ECL DC Characteristics ($V_{EE} = -2.5V \pm 5\%$ or $V_{EE} = -3.3V \pm 5\%$, $V_{CC} = GND$, $T_J = 0^\circ C$ to $+110^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLK0, $\overline{CLK0}$ (ECL differential signals)						
V_{PP}	Differential input voltage ^a	0.1		1.3	V	Differential operation
V_{CMR}	Differential cross point voltage ^b	$V_{EE}+1.0$		-0.3	V	Differential operation
I_{IN}	Input Current ^a			± 100	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock inputs (ECL single ended signals)						
V_{IH}	Input voltage high	-1.165		-0.880	V	
V_{IL}	Input voltage low	-1.810		-1.475	V	
I_{IN}	Input Current ^c			± 100	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
ECL clock outputs (Q0-A19, $\overline{Q0-A19}$)						
V_{OH}	Output High Voltage	-1.1	-1.005	-0.7	V	$I_{OH} = -30 \text{ mA}^d$
V_{OL}	Output Low Voltage	-1.9	-1.705	-1.4	V	$I_{OL} = -5 \text{ mA}^d$
Supply current and V_{BB}						
I_{EE}^e	Maximum Quiescent Supply Current without output termination current		84	160	mA	V_{EE} pins
V_{BB}	Output reference voltage ($f_{ref} < 1.0 \text{ GHz}$) ^f	-1.42		-1.20	V	$I_{BB} = 0.4 \text{ mA}$

a. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.

b. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

c. Inputs have internal pullup/pulldown resistors which affect the input current.

d. Equivalent to a termination of 50Ω to V_{TT} .

e. I_{CC} calculation: $I_{CC} = (\text{number of differential output used}) \times (I_{OH} + I_{OL}) + I_{EE}$

$I_{CC} = (\text{number of differential output used}) \times (V_{OH} - V_{TT}) \div R_{load} + (V_{OL} - V_{TT}) \div R_{load} + I_{EE}$.

f. V_{BB} can be used to bias unused single-ended inputs up to a clock reference frequency of 1 GHz. Above 1 GHz, only differential signals should be used with the MC100ES6221.

Table 7. AC Characteristics (ECL: $V_{EE} = -3.3V \pm 5\%$ or $V_{EE} = -2.5V \pm 5\%$, $V_{CC} = GND$) or (PECL: $V_{CC} = 3.3V \pm 5\%$ or $V_{CC} = 2.5V \pm 5\%$, $V_{EE} = GND$, $T_J = 0^\circ C$ to $+110^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLK0, $\overline{CLK0}$ (PECL or ECL differential signals)						
V_{PP}	Differential input voltage ^b (peak-to-peak)	0.2		1.3	V	
V_{CMR}	Differential input crosspoint voltage ^c	1.0 PECL ECL $V_{EE}+1.0$		$V_{CC}-0.3$ -0.3V	V V	
f_{CLK}	Input Frequency	0		2000	MHz	Differential
t_{PD}	Propagation Delay CLK0 to Q0-19	400	540	670	ps	Differential
Clock input pair CLK1, $\overline{CLK1}$ (HSTL differential signals)						
V_{DIF}	Differential input voltage ^d (peak-to-peak)	0.2		1.3	V	
V_X	Differential input crosspoint voltage ^e	0.1	0.68-0.9	$V_{CC}-1.0$	V	
f_{CLK}	Input Frequency	0		1000	MHz	Differential
t_{PD}	Propagation Delay CLK1 to Q0-19	650	780	950	ps	Differential
PECL/ECL clock outputs (Q0-19, $\overline{Q0-19}$)						
$V_{O(P-P)}$	Differential output voltage (peak-to-peak) $f_O < 1.0$ GHz $f_O < 2.0$ GHz	375 TDB	630 250		V V	
$t_{sk(O)}$	Output-to-output skew		50	100	ps	Differential
$t_{sk(PP)}$	Output-to-output skew (part-to-part) using CLK0 using CLK1 parts at one given T_J , V_{CC} , f_{ref}			270 300 250	ps ps ps	Differential
$t_{JIT(CC)}$	Output cycle-to-cycle jitter			TBD	ps	
$t_{SK(P)}$	Output pulse skew ^f		30	50	ps	
DC_Q	Output Duty Cycle $f_{REF} < 0.1$ GHz $f_{REF} < 1.0$ GHz	49.5 45.0	50 50	50.5 55.0	% %	$DC_{REF} = 50\%$ $DC_{REF} = 50\%$
t_r, t_f	Output Rise/Fall Time	50		350	ps	20% to 80%

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b. V_{PP} (AC) is the minimum differential ECL/PECL input voltage swing required to maintain AC characteristics including t_{pd} and device-to-device skew.

c. V_{CMR} (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.

d. V_{DIF} (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics including t_{pd} and device-to-device skew. Only applicable to CLKB.

e. V_X (AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the V_X (AC) range and the input swing lies within the V_{DIF} (AC) specification. Violation of V_X (AC) or V_{DIF} (AC) impacts the device propagation delay, device and part-to-part skew.

f. Output pulse skew is the absolute difference of the propagation delay times: $|t_{pLH} - t_{pHL}|$.

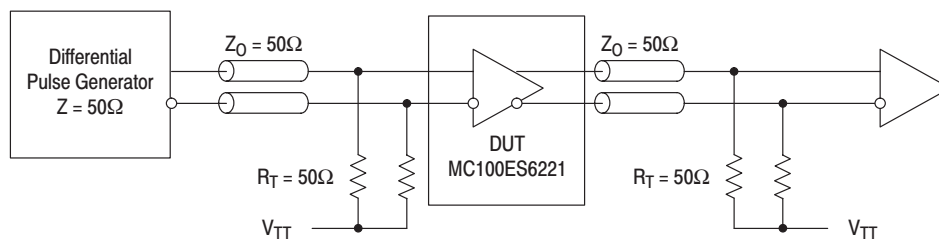


Figure 3. MC100ES6221 AC test reference

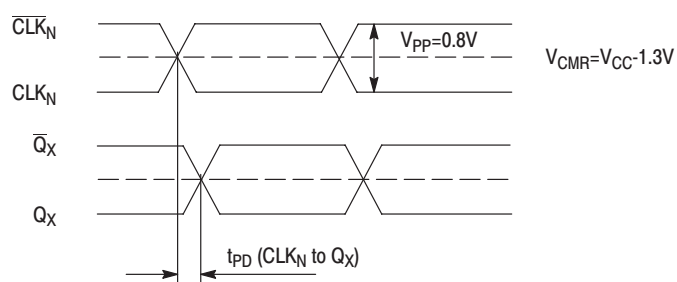


Figure 4. MC100ES6221 AC reference measurement waveform

APPLICATIONS INFORMATION

Understanding the junction temperature range of the MC100ES6221

To make the optimum use of high clock frequency and low skew capabilities of the MC100ES6221, the MC100ES6221 is specified, characterized and tested for the junction temperature range of $T_J=0^{\circ}\text{C}$ to $+110^{\circ}\text{C}$. Because the exact thermal performance depends on the PCB type, design, thermal management and natural or forced air convection, the junction temperature provides an exact way to correlate the application specific conditions to the published performance data of this datasheet. The correlation of the junction temperature range to the application ambient temperature range and vice versa can be done by calculation:

$$T_J = T_A + R_{thja} \cdot P_{tot}$$

Assuming a thermal resistance (junction to ambient) of 17°C/W (2s2p board, 200 ft/min airflow, see Table 9 on page 711) and a typical power consumption of 1148 mW (all outputs terminated 50 ohms to V_{TT} , $V_{CC}=3.3\text{V}$, frequency independent), the junction temperature of the MC100ES6221 is approximately $T_A + 21^{\circ}\text{C}$, and the minimum ambient temperature in this example case calculates to -21°C (the maximum ambient temperature is 89°C . See Table 8). Exceeding the minimum junction temperature specification of the MC100ES6221 does not have a significant impact on the device functionality. However, the continuous use the MC100ES6221 at high ambient temperatures requires thermal management to not exceed the specified maximum junction temperature. Please see the application note AN1545 for a power consumption calculation guideline.

Table 8. Ambient temperature ranges ($P_{tot} = 1148\text{mW}$)

R_{thja} (2s2p board)		$T_{A, \text{min}}^a$	$T_{A, \text{max}}$
Natural convection	20°C/W	-23°C	87°C
100 ft/min	18°C/W	-21°C	89°C
200 ft/min	17°C/W	-20°C	90°C
400 ft/min	16°C/W	-18°C	92°C
800 ft/min	15°C/W	-17°C	93°C

a. The MC100ES6221 device function is guaranteed from $T_A=-40^{\circ}\text{C}$ to $T_J=110^{\circ}\text{C}$

Maintaining Lowest Device Skew

The MC100ES6221 guarantees low output-to-output bank skew of 50 ps and a part-to-part skew of max. 270 ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. This will reduce the device power consumption while maintaining minimum output skew.

Power Supply Bypassing

The MC100ES6221 is a mixed analog/digital product. The differential architecture of the MC100ES6221 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

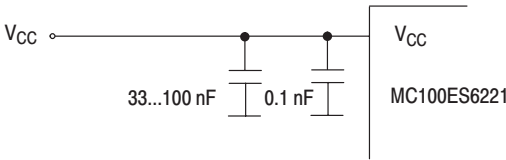


Figure 5. V_{CC} Power Supply Bypass

APPLICATIONS INFORMATION

Using the thermally enhanced package of the MC100ES6221

The MC100ES6221 uses a thermally enhanced exposed pad (EP) 52 lead LQFP package. The package is molded so that the leadframe is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance that supports the power consumption of the MC100ES6221 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100ES6221. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is a requirement for MC100ES6221 applications on multi-layer boards. The recommended thermal land design comprises a 3 x 3 thermal via array as shown in Figure 6 "Recommended thermal land pattern", providing an efficient heat removal path.

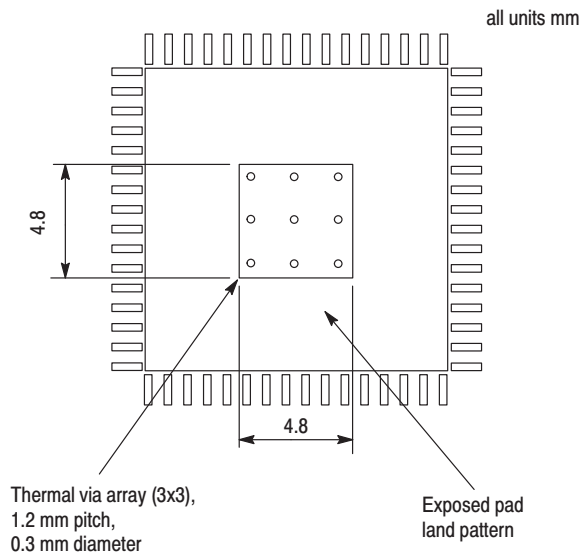


Figure 6. Recommended thermal land pattern

The via diameter is should be approx. 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. Figure 7 "Recommended solder mask openings" shows a recommend solder mask

opening with respect to the recommended 3 x 3 thermal via array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as shown in Figure 7. For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

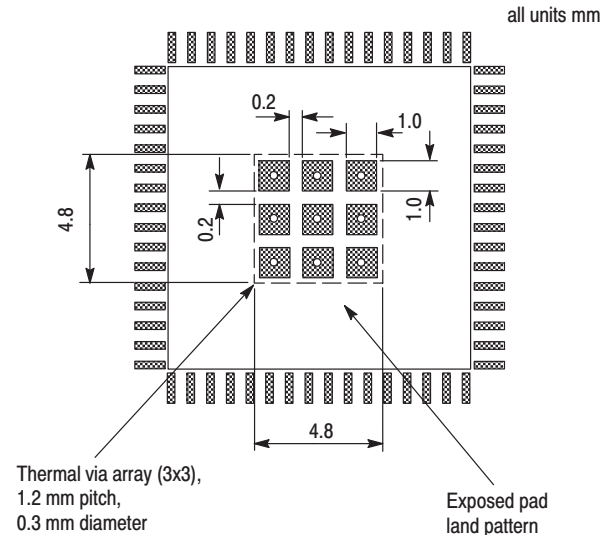


Figure 7. Recommended solder mask openings

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

Table 9. Thermal Resistance^a

Convection-LFPM	R_{THJA}^b °C/W	R_{THJA}^c °C/W	R_{THJC} °C/W	R_{THJB}^d °C/W
Natural	20	48	4 ^e 29 ^f	16
100	18	47		
200	17	46		
400	16	43		
800	15	41		

- Applicable for a 3 x 3 thermal via array
- Junction to ambient, four conductor layer test board (2S2P), per JES51-7 and JESD 51-5
- Junction to ambient, single layer test board, per JESD51-3
- Junction to board, four conductor layer test board (2S2P) per JESD 51-8
- Junction to exposed pad
- Junction to top of package

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100ES6221 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.

Low Voltage 1:15 Differential ECL/PECL Clock Divider and Fanout Buffer

The Motorola MC100ES6222 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6222 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver is high performance clock distribution in computing, networking and telecommunication systems.

Features

- 15 differential ECL/PECL outputs (4 output banks)
- 2 selectable differential ECL/PECL inputs
- Selectable $\div 1$ or $\div 2$ frequency divider
- 130 ps maximum device skew
- Supports DC to 3 GHz input frequency
- Single 3.3V, -3.3V, 2.5V or -2.5V supply
- Standard 52 lead LQFP package with exposed pad for enhanced thermal characteristics
- Supports industrial temperature range
- Pin and function compatible to the MC100EP222

Functional Description

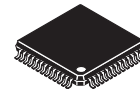
The MC100ES6222 is designed for low skew clock distribution systems and supports clock frequencies up to 3 GHz. The CLK0 and CLK1 inputs can be driven by ECL or PECL compatible signals. Each of the four output banks of two, three, four and six differential clock output pairs can be independently configured to distribute the input frequency or $\div 2$ of the input frequency. The FSELA, FSELB, FSELC, FSELD and CLK_SEL are asynchronous control inputs. Any changes of the control inputs require a MR pulse for resynchronization of the $\div 2$ outputs. For the functionality of the MR control input, see Figure 5, "Functional Diagram," on page 718.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The MC100ES6222 can be operated from a single 3.3V or 2.5V supply. As most other ECL compatible devices, the MC100ES6222 supports positive (PECL) and negative (ECL) supplies. The MC100ES6222 is pin and function compatible to the MC100EP222.

MC100ES6222

**LOW-VOLTAGE
1:15 DIFFERENTIAL
ECL/PECL CLOCK DIVIDER
AND FANOUT DRIVER**



TB SUFFIX
52-LEAD LQFP PACKAGE
EXPOSED PAD
CASE 1336A

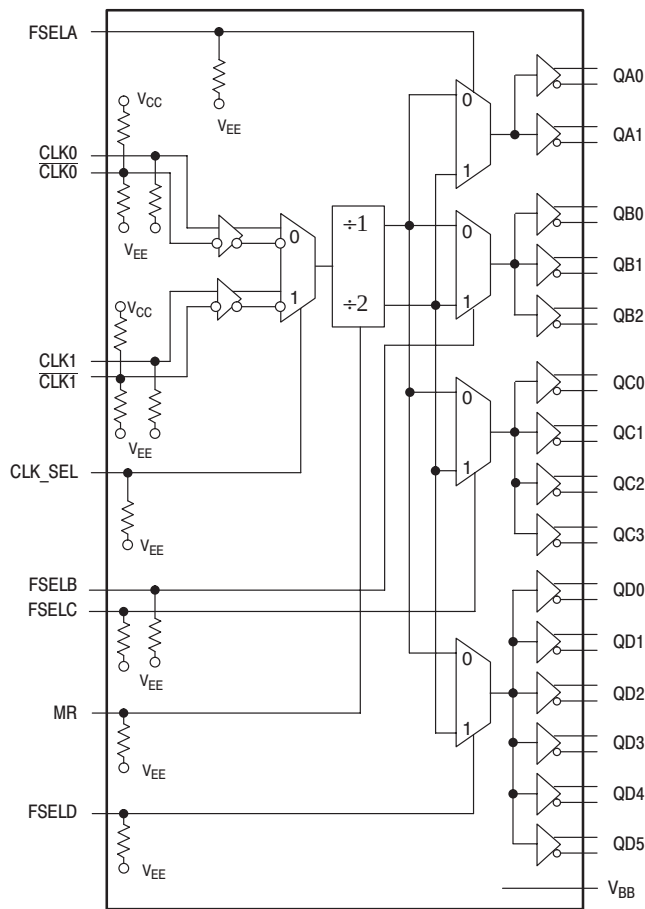


Figure 1. MC100ES6222 Logic Diagram

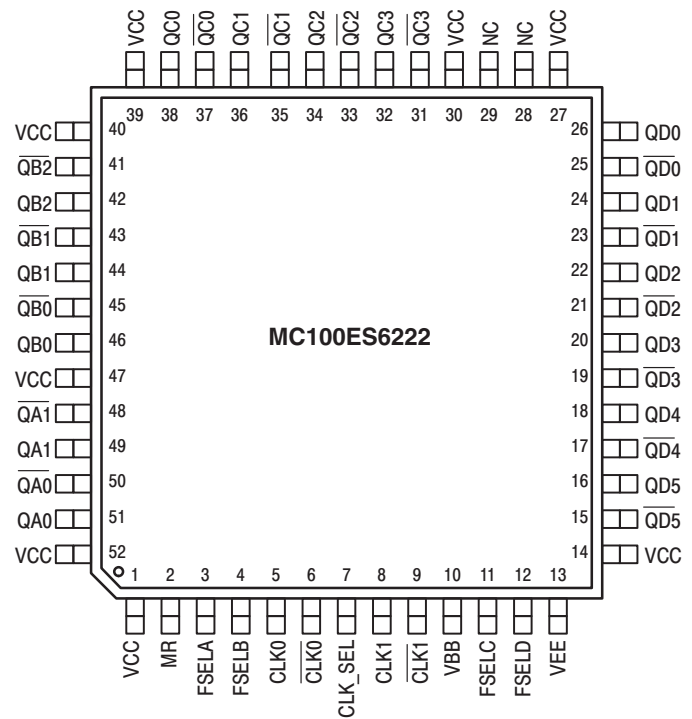


Figure 2. 52-Lead Package Pinout (Top View)

Table 1. Function Table

Control Pin	0	1
FSELA (asynchronous)	÷1	÷2
FSELB (asynchronous)	÷1	÷2
FSELC (asynchronous)	÷1	÷2
FSELD (asynchronous)	÷1	÷2
CLK_SEL (asynchronous)	CLK0	CLK1
MR (asynchronous)	Active	Reset. $Q_X = L$ and $\overline{Q}_X = H$.

Table 2. Pin Configuration

Pin	I/O	Type	Description
CLK0, $\overline{\text{CLK0}}$	Input	ECL/PECL	Differential reference clock signal input
CLK1, $\overline{\text{CLK1}}$	Input	ECL/PECL	Alternative differential reference clock signal input
FSELA, FSELB, FSELC, FSELD	Input	ECL/PECL	Selection output frequency divider for bank A, B, C and D
MR	Input	ECL/PECL	Reset
CLK_SEL	Input	ECL/PECL	Clock reference select input
QA[0:1], $\overline{\text{QA}}[0:1]$	Output	ECL/PECL	Bank A differential outputs
QB[0:2], $\overline{\text{QB}}[0:2]$	Output	ECL/PECL	Bank B differential outputs
QC[0:3], $\overline{\text{QC}}[0:3]$	Output	ECL/PECL	Bank C differential outputs
QD[0:5], $\overline{\text{QD}}[0:5]$	Output	ECL/PECL	Bank D differential outputs
VBB	Output	DC	Reference voltage output for single ended ECL or PECL operation
VEE ^a		Power supply	Negative power supply
VCC		Power supply	Positive power supply. All V _{CC} pins must be connected to the positive power supply for correct DC and AC operation.

a. In ECL mode (negative power supply mode), V_{EE} is either -3.3V or -2.5V and V_{CC} is connected to GND (0V). In PECL mode (positive power supply mode), V_{EE} is connected to GND (0V) and V_{CC} is either +3.3V or +2.5V. In both modes, the input and output levels are referenced to the most positive supply (V_{CC}).

Table 3. Absolute Maximum Ratings^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	3.6	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} + 0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} + 0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage temperature	-65	125	°C	
T _{FUNC}	Functional temperature range	T _A = -40	T _J = +110	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output termination voltage		V _{CC} - 2 ^a		V	
MM	ESD Protection (Machine model)	175			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model)	TBD			V	
LU	Latch-up immunity	200			mA	
C _{IN}	Input Capacitance		4.0		pF	Inputs
θ _{JA} , θ _{JC} θ _{JB}	Thermal resistance (junction-to-ambient, junction-to-board, junction-to-case)	See Table 9, "Thermal Resistance" on page 720			°C/W	
T _J	Operating junction temperature ^b (continuous operation) MTBF = 9.1 years	0		110	°C	

a. Output termination voltage V_{TT} = 0V for V_{CC} = 2.5V operation is supported but the power consumption of the device will increase.

b. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6222 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6222 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 5. PECL DC Characteristics ($V_{CC} = 2.5V \pm 5\%$ or $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = GND$, $T_J = 0^\circ C$ to $+110^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$ (PECL differential signals)						
V_{PP}	Differential Input Voltage ^a	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage ^b	1.0		$V_{CC} - 0.3$	V	Differential operation
I_{IN}	Input Current ^a			± 150	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock inputs MR, CLK_SEL, FSEL A, FSEL B, FSEL C, FSEL D (PECL single ended signals)						
V_{IH}	Input Voltage High	$V_{CC} - 1.165$		$V_{CC} - 0.880$	V	
V_{IL}	Input Voltage Low	$V_{CC} - 1.810$		$V_{CC} - 1.475$	V	
I_{IN}	Input Current ^c			± 150	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
PECL clock outputs (QA[0:1], $\overline{QA}$ [0:1], QB[0:2], $\overline{QB}$ [0:2], QC[0:3], $\overline{QC}$ [0:3], QD[0:5], $\overline{QD}$ [0:5])						
V_{OH}	Output High Voltage	$V_{CC} - 1.1$	$V_{CC} - 1.005$	$V_{CC} - 0.7$	V	$I_{OH} = -30 \text{ mA}^d$
V_{OL}	Output Low Voltage	$V_{CC} - 1.9$	$V_{CC} - 1.705$	$V_{CC} - 1.4$	V	$I_{OL} = -5 \text{ mA}^d$
Supply current and V_{BB}						
I_{EE}^e	Maximum Quiescent Supply Current without output termination current		96	170	mA	V_{EE} pins
V_{BB}	Output reference voltage	$V_{CC} - 1.38$		$V_{CC} - 1.22$	V	$I_{BB} = 0.4 \text{ mA}$

a. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.

b. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

c. Input have internal pullup/pulldown resistors which affect the input current.

d. Equivalent to a termination of 50Ω to V_{TT} .

e. I_{CC} calculation: $I_{CC} = (\text{number of differential output used}) \times (I_{OH} + I_{OL}) + I_{EE}$

$$I_{CC} = (\text{number of differential output used}) \times (V_{OH} - V_{TT}) \div R_{load} + (V_{OL} - V_{TT}) \div R_{load} + I_{EE}.$$

Table 6. ECL DC Characteristics ($V_{EE} = -2.5V \pm 5\%$ or $V_{EE} = -3.3V \pm 5\%$, $V_{CC} = GND$, $T_J = T_J = 0^\circ C$ to $+110^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$ (ECL differential signals)						
V_{PP}	Differential Input Voltage ^a	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage ^b	$V_{EE} + 1.0$		-0.3	V	Differential operation
I_{IN}	Input Current ^a			± 150	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock inputs MR, CLK_SEL, FSELA, FSELB, FSELC, FSELD (PECL single ended signals)						
V_{IH}	Input Voltage High	-1.165		-0.880	V	
V_{IL}	Input Voltage Low	-1.810		-1.475	V	
I_{IN}	Input Current ^c			± 150	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
ECL clock outputs (QA[0:1], $\overline{QA}$ [0:1], QB[0:2], $\overline{QB}$ [0:2], QC[0:3], $\overline{QC}$ [0:3], QD[0:5], $\overline{QD}$ [0:5])						
V_{OH}	Output High Voltage	-1.1	-1.005	-0.7	V	$I_{OH} = -30 \text{ mA}^d$
V_{OL}	Output Low Voltage	-1.9	-1.705	1.4	V	$I_{OL} = -5 \text{ mA}^d$
Supply current and V_{BB}						
I_{EE}^e	Maximum Quiescent Supply Current without output termination current		96	170	mA	V_{EE} pins
V_{BB}	Output reference voltage	-1.38		-1.22	V	$I_{BB} = 0.4 \text{ mA}$

a. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.

b. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

c. Input have internal pullup/pulldown resistors which affect the input current.

d. Equivalent to a termination of 50Ω to V_{TT} .

e. I_{CC} calculation: $I_{CC} = (\text{number of differential output used}) \times (I_{OH} + I_{OL}) + I_{EE}$

$I_{CC} = (\text{number of differential output used}) \times (V_{OH} - V_{TT}) \div R_{load} + (V_{OL} - V_{TT}) \div R_{load} + I_{EE}$.

Table 7. AC Characteristics (ECL: $V_{EE} = -3.3V \pm 5\%$ or $V_{EE} = -2.5V \pm 5\%$, $V_{CC} = GND$) or
(PECL: $V_{CC} = 3.3V \pm 5\%$ or $V_{CC} = 2.5V \pm 5\%$, $V_{EE} = GND$, $T_J = 0^\circ C$ to $+110^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$ (PECL or ECL differential signals)						
V_{PP}	Differential input voltage ^b (peak-to-peak)	0.2		1.3	V	
V_{CMR}	Differential input crosspoint voltage ^c	PECL ECL 1.0 $V_{EE}+1.0$		$V_{CC} - 0.3$ -0.3V	V V	
f_{CLK}	Input Frequency	0		2000	MHz	Differential
ECL/PECL clock outputs (QA[0:1], $\overline{QA}$ [0:1], QB[0:2], $\overline{QB}$ [0:2], QC[0:3], $\overline{QC}$ [0:3], QD[0:5], $\overline{QD}$ [0:5])						
t_{PD}	Propagation Delay CLK0 or CLK1 to Qx MR to Qx	670	820	970	ps ps	Differential
$V_{O(P-P)}$	Differential output voltage (peak-to-peak) $f_O < 1.0$ GHz $f_O < 2.0$ GHz	TBD TBD			mV mV	
$t_{sk(O)}$	Output-to-output skew within QA[0:1] within QB[0:2] within QC[0:3] within QD[0:5] any output			35 35 50 60 130	ps ps ps ps ps	Differential
$t_{sk(PP)}$	Output-to-output skew (part-to-part)			300	ps	Differential
$t_{JIT(CC)}$	Output cycle-to-cycle jitter			TBD	ps	
$t_{SK(P)}$	Output pulse skew ^d		5	15	ps	
DC_O	Output Duty Cycle $f_{REF} < 0.1$ GHz $f_{REF} < 1.0$ GHz $f_{REF} < 2.0$ GHz	49.85 48.50 47.00	50 50 50	50.15 51.50 53.00	% % %	$DC_{REF} = 50\%$ $DC_{REF} = 50\%$ $DC_{REF} = 50\%$
t_r, t_f	Output Rise/Fall Time	50		300	ps	20% to 80%

- a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
b. V_{PP} (AC) is the minimum differential ECL/PECL input voltage swing required to maintain AC characteristics including t_{pd} and device-to-device skew.
c. V_{CMR} (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.
d. Output pulse skew is the absolute difference of the propagation delay times: $|t_{pLH} - t_{pHL}|$.

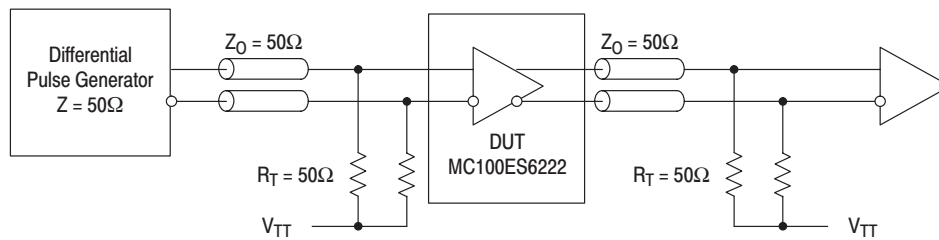
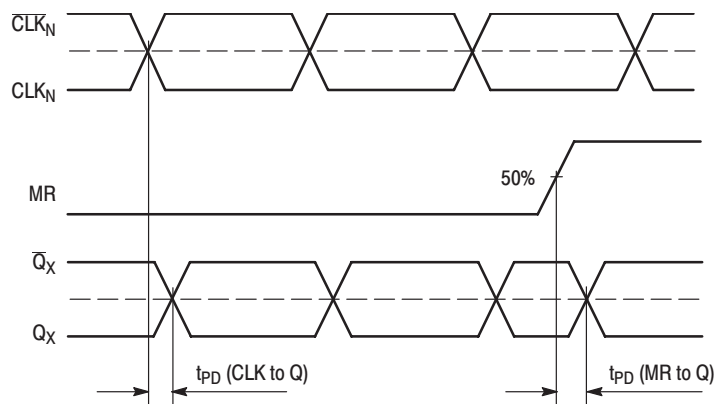


Figure 3. MC100ES6222 AC test reference

Figure 4. MC100ES6222 t_{PD} measurement waveform

APPLICATIONS INFORMATION

Asynchronous Reset Functional Diagram

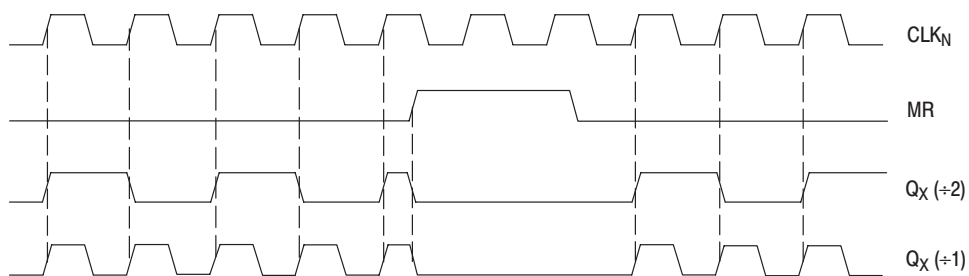


Figure 5. Functional diagram

APPLICATIONS INFORMATION

Understanding the junction temperature range of the MC100ES6222

To make the optimum use of high clock frequency and low skew capabilities of the MC100ES6222, the MC100ES6222 is specified, characterized and tested for the junction temperature range of $T_J=0^{\circ}\text{C}$ to $+110^{\circ}\text{C}$. Because the exact thermal performance depends on the PCB type, design, thermal management and natural or forced air convection, the junction temperature provides an exact way to correlate the application specific conditions to the published performance data of this datasheet. The correlation of the junction temperature range to the application ambient temperature range and vice versa can be done by calculation:

$$T_J = T_A + R_{thja} \cdot P_{tot}$$

Assuming a thermal resistance (junction to ambient) of 17°C/W (2s2p board, 200 ft/min airflow, see Table 9 on page 720) and a typical power consumption of 1026 mW (all outputs terminated 50 ohms to V_{TT} , $V_{CC}=3.3\text{V}$, frequency independent), the junction temperature of the MC100ES6222 is approximately $T_A + 17^{\circ}\text{C}$, and the minimum ambient temperature in this example case calculates to -17°C (the maximum ambient temperature is 93°C . See Table 8). Exceeding the minimum junction temperature specification of the MC100ES6222 does not have a significant impact on the device functionality. However, the continuous use the MC100ES6222 at high ambient temperatures requires thermal management to not exceed the specified maximum junction temperature. Please see the application note AN1545 for a power consumption calculation guideline.

Table 8. Ambient temperature ranges ($P_{tot} = 1026\text{mW}$)

R_{thja} (2s2p board)		T_A , min ^a	T_A , max
Natural convection	20°C/W	-21°C	89°C
100 ft/min	18°C/W	-18°C	92°C
200 ft/min	17°C/W	-17°C	93°C
400 ft/min	16°C/W	-16°C	94°C
800 ft/min	15°C/W	-15°C	95°C

a. The MC100ES6222 device function is guaranteed from $T_A=-40^{\circ}\text{C}$ to $T_J=110^{\circ}\text{C}$

Maintaining Lowest Device Skew

The MC100ES6222 guarantees low output-to-output bank skew of 130 ps and a part-to-part skew of max. 300 ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. This will reduce the device power consumption while maintaining minimum output skew.

Power Supply Bypassing

The MC100ES6222 is a mixed analog/digital product. The differential architecture of the MC100ES6222 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

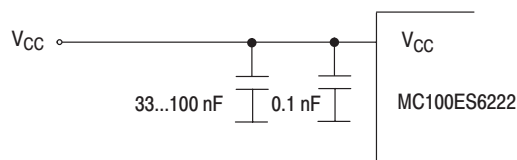


Figure 6. V_{CC} Power Supply Bypass

APPLICATIONS INFORMATION

Using the thermally enhanced package of the MC100ES6222

The MC100ES6222 uses a thermally enhanced exposed pad (EP) 52 lead LQFP package. The package is molded so that the leadframe is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance that supports the power consumption of the MC100ES6222 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100ES6222. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is a requirement for MC100ES6222 applications on multi-layer boards. The recommended thermal land design comprises a 3 x 3 thermal via array as shown in Figure 7 "Recommended thermal land pattern", providing an efficient heat removal path.

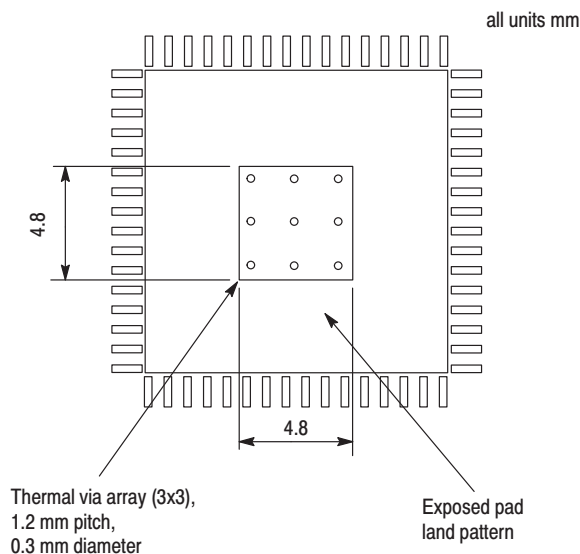


Figure 7. Recommended thermal land pattern

The via diameter is should be approx. 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. Figure 8 "Recommended solder mask openings" shows a recommend solder mask

opening with respect to the recommended 3 x 3 thermal via array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as shown in Figure 8 For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

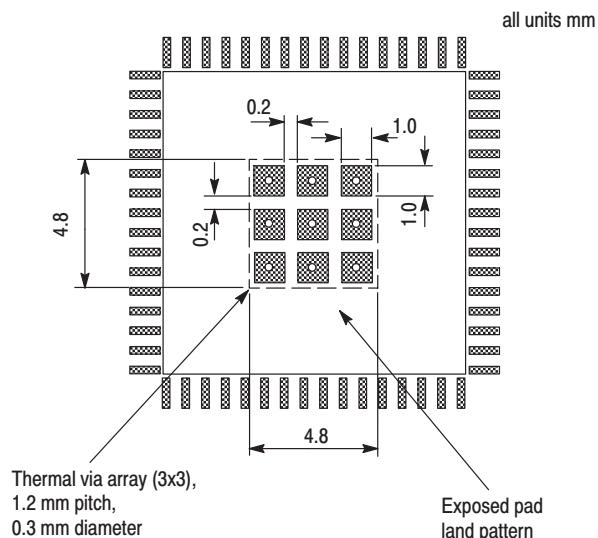


Figure 8. Recommended solder mask openings

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

Table 9. Thermal Resistance^a

Convection-LFPM	R_{THJA}^b °C/W	R_{THJA}^c °C/W	R_{THJC} °C/W	R_{THJB}^d °C/W
Natural	20	48	4 ^e 29 ^f	16
100	18	47		
200	17	46		
400	16	43		
800	15	41		

- Applicable for a 3 x 3 thermal via array
- Junction to ambient, four conductor layer test board (2S2P), per JES51-7 and JESD 51-5
- Junction to ambient, single layer test board, per JESD51-3
- Junction to board, four conductor layer test board (2S2P) per JESD 51-8
- Junction to exposed pad
- Junction to top of package

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100ES6222 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.

2.5/3.3V Differential LVPECL 1:9 Clock Distribution Buffer and Clock Divider

The Motorola MC100ES6226 is a bipolar monolithic differential clock distribution buffer and clock divider. Designed for most demanding clock distribution systems, the MC100ES6226 supports various applications that require a large number of outputs to drive precisely aligned clock signals. Using SiGe technology and a fully differential architecture, the device offers superior digital signal characteristics and very low clock skew error. Target applications for this clock driver are high performance clock distribution systems for computing, networking and telecommunication systems.

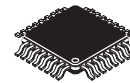
Features:

- Fully differential architecture from input to all outputs
- SiGe technology supports near-zero output skew
- Selectable 1:1 or 1:2 frequency outputs
- LVPECL compatible differential clock inputs and outputs
- LVCMOS compatible control inputs
- Single 3.3V or 2.5V supply
- Max. 35 ps maximum output skew (within output bank)
- Max. 50 ps maximum device skew
- Supports DC operation and up to 3 GHz (typ.) clock signals
- Synchronous output enable eliminating output runt pulse generation and metastability
- Standard 32 lead LQFP package
- Industrial temperature range

Functional Description

MC100ES6226 is designed for very skew critical differential clock distribution systems and supports clock frequencies from DC up to 3.0 GHz. Typical applications for the MC100ES6226 are primary clock distribution systems on backplanes of high-performance computer, networking and telecommunication systems, as well as on-board clocking of OC-3, OC-12 and OC-48 speed communication systems.

The MC100ES6226 can be operated from a 3.3V or 2.5V positive supply without the requirement of a negative supply line. Each of the output banks of three differential clock output pairs may be independently configured to distribute the input frequency or half of the input frequency. The FSEL0 and FSEL1 clock frequency selects are asynchronous control inputs. Any changes of the control inputs require a MR pulse for resynchronization of the ± 2 outputs.

MC100ES6226**2.5V/3.3V DIFFERENTIAL
LVPECL 1:9 CLOCK
DISTRIBUTION BUFFER AND
CLOCK DIVIDER****FA SUFFIX**
32-LEAD LQFP PACKAGE
CASE 873A

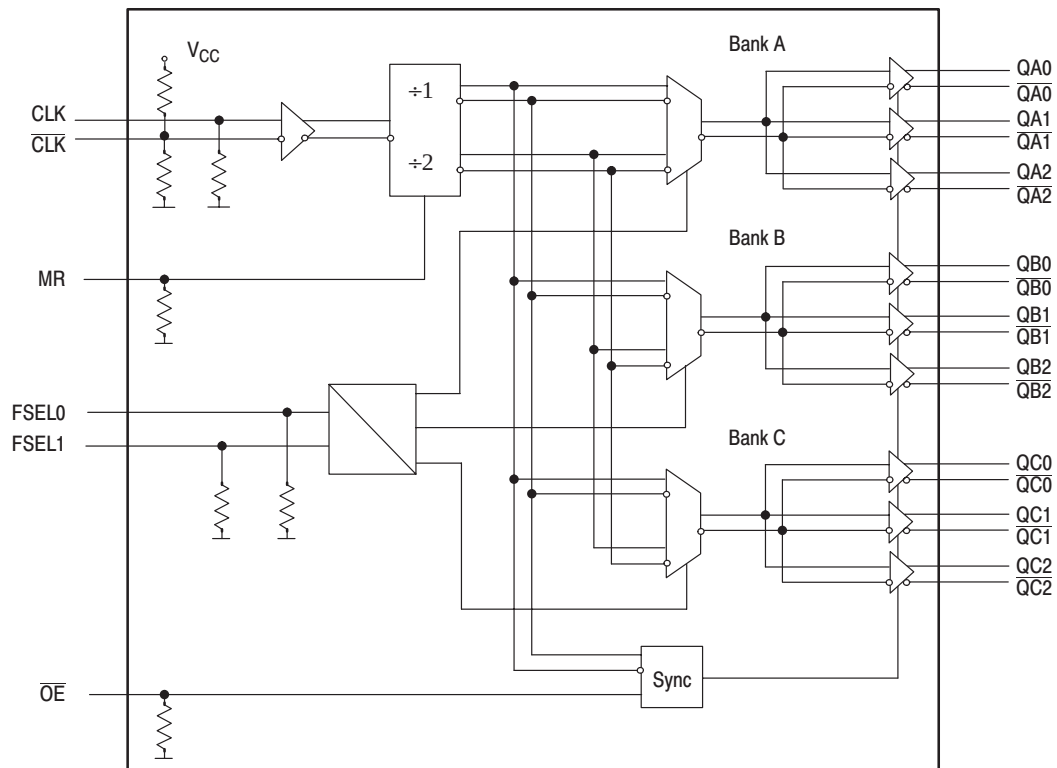


Figure 1. MC100ES6226 Logic Diagram

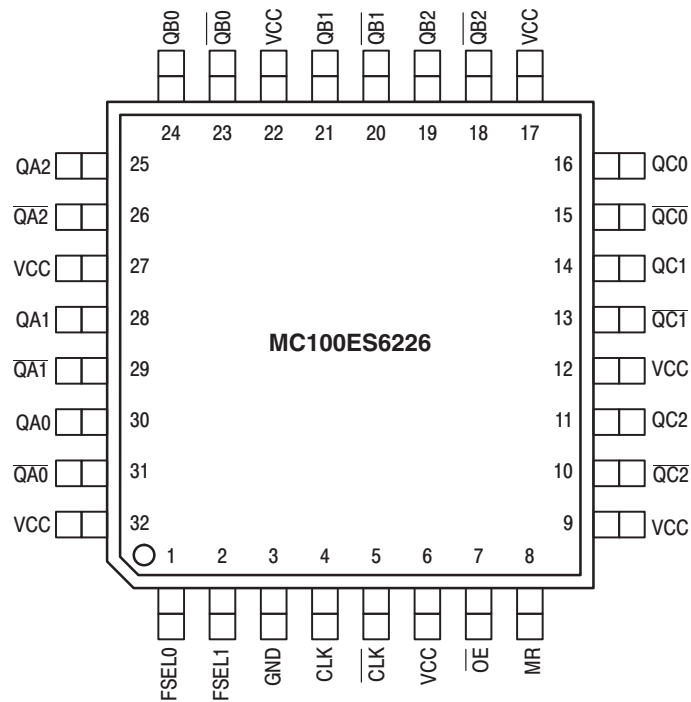


Figure 2. 32-Lead Package Pinout (Top View)

TABLE 1: PIN CONFIGURATION

Pin	I/O	Type	Function
CLK, $\overline{\text{CLK}}$	Input	LVPECL	Differential reference clock signal input
$\overline{\text{OE}}$	Input	LVC MOS	Output enable
MR	Input	LVC MOS	Device reset
FSEL0, FSEL1	Input	LVC MOS	Output frequency divider select
QA[0-2], $\overline{\text{QA}}$ [0-2] QB[0-2], $\overline{\text{QB}}$ [0-2] QC[0-2], $\overline{\text{QC}}$ [0-2]	Output	LVPECL	Differential clock outputs (banks A, B and C)
GND	Supply	GND	Negative power supply
V _{CC}	Supply	VCC	Positive power supply. All V _{CC} pins must be connected to the positive power supply for correct DC and AC operation

TABLE 2: FUNCTION TABLE

Control	Default	0	1
$\overline{\text{OE}}$	0	Qx[0-2], $\overline{\text{Qx}}$ [0-2] are active. Deassertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses	Qx[0-2] = L, $\overline{\text{Qx}}$ [0-2] = H (outputs disabled). Assertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses
MR	0	Normal operation	Device reset (asynchronous)
FSEL0, FSEL1	00	See Following Table	

TABLE 3: Output Frequency Select Control

FSEL0	FSEL1	QA0 to QA2	QB0 to QB2	QC0 to QC2
0	0	$f_{\text{QA0:2}} = f_{\text{CLK}}$	$f_{\text{QB0:2}} = f_{\text{CLK}}$	$f_{\text{QC0:2}} = f_{\text{CLK}}$
0	1	$f_{\text{QA0:2}} = f_{\text{CLK}}$	$f_{\text{QB0:2}} = f_{\text{CLK}}$	$f_{\text{QC0:2}} = f_{\text{CLK}} \div 2$
1	0	$f_{\text{QA0:2}} = f_{\text{CLK}}$	$f_{\text{QB0:2}} = f_{\text{CLK}} \div 2$	$f_{\text{QC0:2}} = f_{\text{CLK}} \div 2$
1	1	$f_{\text{QA0:2}} = f_{\text{CLK}} \div 2$	$f_{\text{QB0:2}} = f_{\text{CLK}} \div 2$	$f_{\text{QC0:2}} = f_{\text{CLK}} \div 2$

TABLE 4: ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	3.6	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} +0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} +0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

TABLE 5: GENERAL SPECIFICATIONS

Sym- bol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		$V_{CC} - 2^a$		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model)	1000			V	
LU	Latch-up immunity	200			mA	
C_{IN}			4.0		pF	Inputs
θ_{JA}	Thermal resistance junction to ambient JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
	Operating junction temperature ^b (continuous operation) MTBF = 9.1 years	0		110	°C	

a. Output termination voltage $V_{TT} = 0V$ for $V_{CC} = 2.5V$ operation is supported but the power consumption of the device will increase.

b. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6226 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6226 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

TABLE 6: DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$ and $2.5V \pm 5\%$, $T_J = 0^{\circ}C$ to $+110^{\circ}C$)^a

Sym- bol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS control inputs ($\overline{OE}$, FSEL0, FSEL1, MR)						
V_{IL}	Input voltage low $V_{CC} = 3.3V$ $V_{CC} = 2.5V$			0.8 0.7	V	
V_{IH}	Input voltage high $V_{CC} = 3.3V$ $V_{CC} = 2.5V$	2.2 1.7			V	
I_{IN}	Input Current ^b			± 150	μA	$V_{IN} = V_{CC}$ or $V_{IN} = GND$
LVPECL clock inputs (CLK, $\overline{CLK}$) ^c						
V_{PP}	DC differential input voltage ^d	0.1		1.3	V	Differential operation
V_{CMR}	Differential cross point voltage ^e	1.0		$V_{CC}-0.3$	V	Differential operation
V_{IH}	Input high voltage	TBD		TBD		
V_{IL}	Input low voltage	TBD		TBD		
I_{IN}	Input Current			± 150	μA	$V_{IN} = TBD$ or $V_{IN} = TBD$
LVPECL clock outputs (QA[2:0], QB[2:0], QC[2:0])						
V_{OH}	Output High Voltage	$V_{CC}-1.1$		$V_{CC}-0.8$	V	Termination 50Ω to V_{TT}
V_{OL}	Output Low Voltage	$V_{CC}-1.8$		$V_{CC}-1.4$	V	Termination 50Ω to V_{TT}
Supply current						
I_{GND}	Maximum Quiescent Supply Current without output termination current		65	110	mA	GND pin
I_{CC}	Maximum Quiescent Supply Current with output termination current		325	400	mA	All V_{CC} Pins

a. AC characteristics are design targets and pending characterization.

b. Input have internal pullup/pulldown resistors which affect the input current.

c. Clock inputs driven by LVPECL compatible signals.

d. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristic.

e. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

TABLE 7: AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$ and $2.5V \pm 5\%$, $T_J = 0^{\circ}C$ to $+110^{\circ}C$)^{a b}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{PP}	Differential input voltage ^c (peak-to-peak)	0.2	0.3	1.3	V	
V_{CMR}	Differential input crosspoint voltage ^d	1.0		$V_{CC}-0.3$	V	
$V_{X,OUT}$	Differential output crosspoint voltage	$V_{CC}-1.45$		$V_{CC}-1.1$	V	
$V_{O(P-P)}$	Differential output voltage (peak-to-peak) $f_O < 300$ MHz $f_O < 1.5$ GHz $f_O < 2.7$ GHz	0.45	0.72	0.95	V	
		0.3	0.55	0.95	V	
		TBD	0.37	0.95	V	
f_{CLK}	Input Frequency	0		3000 ^e	MHz	
t_{PD}	Propagation Delay CLK to Qx[]	475	500	800	ps	Differential
$t_{sk(O)}$	Output-to-output skew (within QA[2:0]) (within QB[2:0]) (within QC[2:0]) (within device)		11	25	ps	Differential
			12	25	ps	
			4	20	ps	
				60	ps	
$t_{sk(PP)}$	Output-to-output skew (part-to-part)			325	ps	Differential
$t_{JIT(CC)}$	Output cycle-to-cycle jitter single frequency configuration $\pm 1/\pm 2$ frequency configuration			TBD		FSEL0 = FSEL1 FSEL0 $\neq$ FSEL1
				TBD		
DC_O	Output duty cycle $Qx = +1$, $f_O < 300$ MHz $Qx = +1$, $f_O > 300$ MHz	48	50	52	%	$DC_{fref} = 50\%$
		45	50	55	%	
	$Qx = +2$, $f_O < 300$ MHz $Qx = +2$, $f_O > 300$ MHz	49	50	51	%	
		47.5	50	52.5	%	
t_r, t_f	Output Rise/Fall Time	0.05		200	ns	20% to 80%
t_{PDL}^f	Output disable time	$2.5 \cdot T + t_{PD}$		$4.5 \cdot T + t_{PD}$	ns	$T = CLK$ period
t_{PLD}^g	Output enable time	$3 \cdot T + t_{PD}$		$5 \cdot T + t_{PD}$	ns	$T = CLK$ period

a. AC characteristics are design targets and pending characterization.

b. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

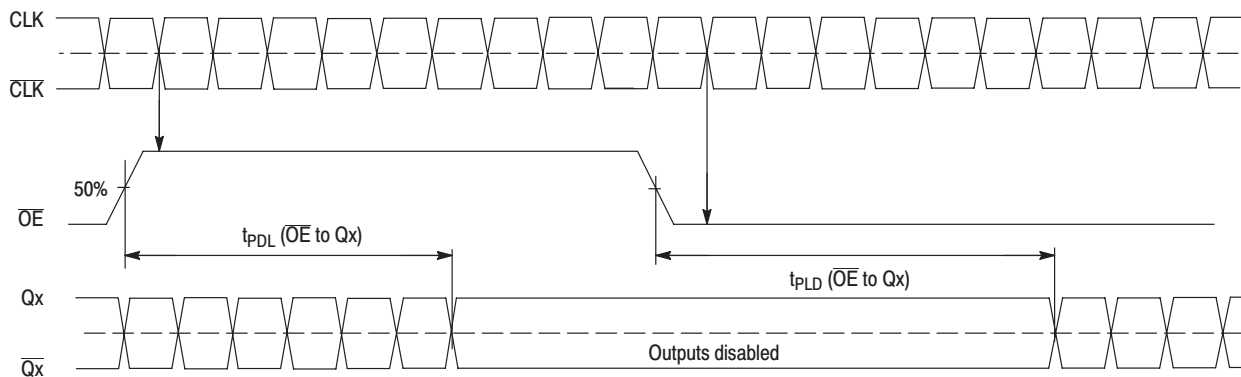
c. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including t_{pd} and device-to-device skew.

d. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.

e. The MC100ES6226 is fully operational up to 3.0 GHz and is characterized up to 2.7 GHz.

f. Propagation delay $\overline{OE}$ deassertion to differential output disabled (differential low: true output low, complementary output high).

g. Propagation delay $\overline{OE}$ assertion to output enabled (active).

**Figure 3. MC100ES6226 output disable/enable timing**

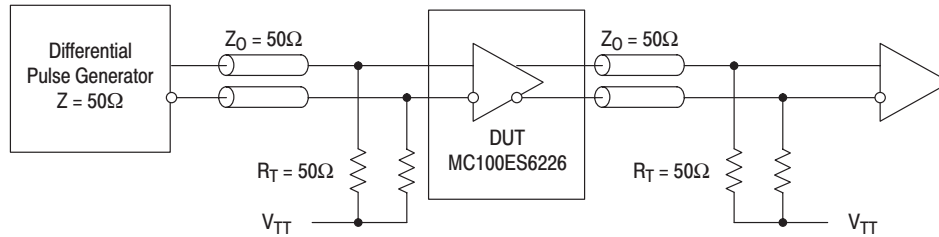


Figure 4. MC100ES6226 AC test reference

APPLICATIONS INFORMATION

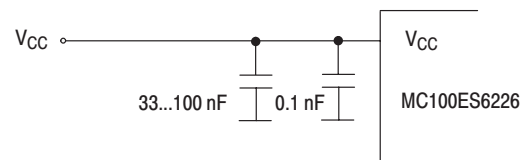
Maintaining Lowest Device Skew

The MC100ES6226 guarantees low output-to-output bank skew of 35 ps and a part-to-part skew of max. TBD ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. If an entire output bank is not used, it is recommended to leave all of these outputs open and unterminated. This will reduce the device power consumption while maintaining minimum output skew.

Power Supply Bypassing

The MC100ES6226 is a mixed analog/digital product. The differential architecture of the MC100ES6226 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the

spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

Figure 5. V_{CC} Power Supply Bypass

2.5/3.3V Differential LVPECL 2x2 Clock Switch and Fanout Buffer

The Motorola MC100ES6254 is a bipolar monolithic differential 2x2 clock switch and fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6254 supports various applications that require to drive precisely aligned clock signals. The device is capable of driving and switching differential LVPECL signals. Using SiGe technology and a fully differential architecture, the device offers superior digital signal characteristics and very low clock skew error. Target applications for this clock driver are high performance clock/data switching, clock distribution or data loopback in computing, networking and telecommunication systems.

Features:

- Fully differential architecture from input to all outputs
- SiGe technology supports near-zero output skew
- Supports DC to 3GHz operation¹ of clock or data signals
- LVPECL compatible differential clock inputs and outputs
- LVCMOS compatible control inputs
- Single 3.3V or 2.5V supply
- 50 ps maximum device skew¹
- Synchronous output enable eliminating output runt pulse generation and metastability
- Standard 32 lead LQFP package
- Industrial temperature range

Functional Description

MC100ES6254 is designed for very skew critical differential clock distribution systems and supports clock frequencies from DC up to 3.0 GHz. Typical applications for the MC100ES6254 are primary clock distribution, switching and loopback systems of high-performance computer, networking and telecommunication systems, as well as on-board clocking of OC-3, OC-12 and OC-48 speed communication systems. Primary purpose of the MC100ES6254 is high-speed clock switching applications. In addition, the MC100ES6254 can be configured as single 1:6 or dual 1:3 LVPECL fanout buffer for clock signals, or as loopback device in high-speed data applications.

The MC100ES6254 can be operated from a 3.3V or 2.5V positive supply without the requirement of a negative supply line.

MC100ES6254

**2.5V/3.3V DIFFERENTIAL
LVPECL 2x2
CLOCK SWITCH
AND FANOUT BUFFER**



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A

1. The device is functional up to 3 GHz and characterized up to 2.7 GHz.

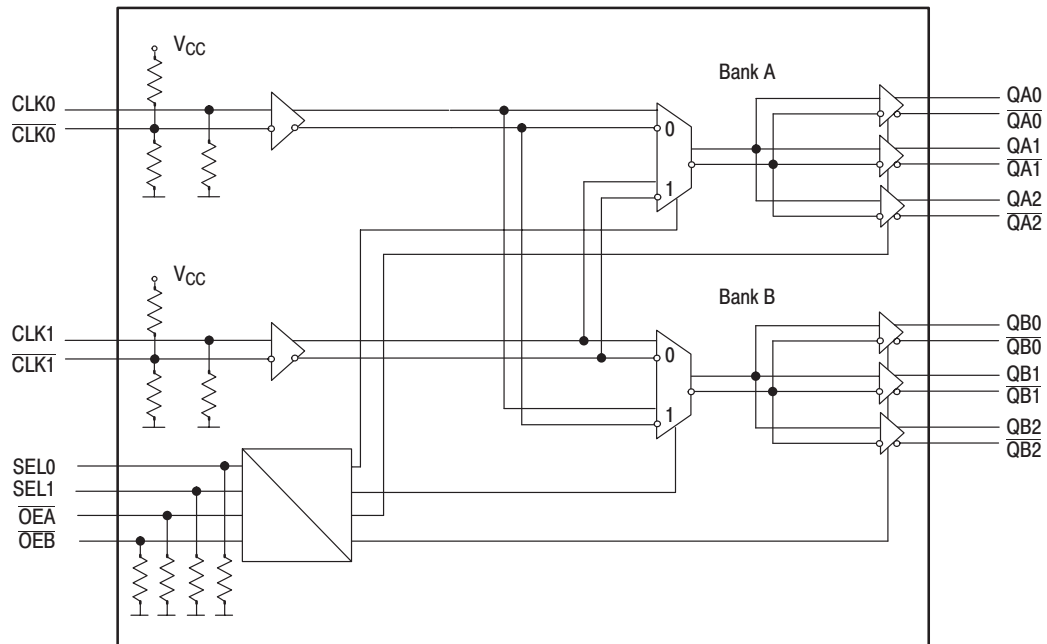


Figure 1. MC100ES6254 Logic Diagram

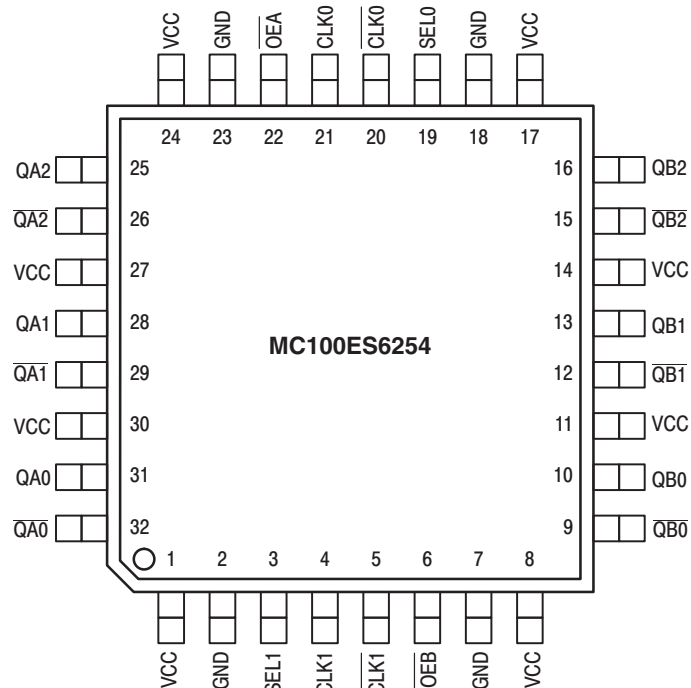


Figure 2. 32-Lead Package Pinout (Top View)

TABLE 1: PIN CONFIGURATION

Pin	I/O	Type	Function
CLK0, $\overline{\text{CLK0}}$	Input	LVPECL	Differential reference clock signal input 0
CLK1, $\overline{\text{CLK1}}$	Input	LVPECL	Differential reference clock signal input 1
$\overline{\text{OEA}}$, $\overline{\text{OEB}}$	Input	LVC MOS	Output enable
SEL0, SEL1	Input	LVC MOS	Clock switch select
QA[0:2], $\overline{\text{QA}}[0:2]$ QB[0:2], $\overline{\text{QB}}[0:2]$	Output	LVPECL	Differential clock outputs (banks A and B)
GND	Supply	GND	Negative power supply
V _{CC}	Supply	VCC	Positive power supply. All V _{CC} pins must be connected to the positive power supply for correct DC and AC operation

TABLE 2: FUNCTION TABLE

Control	Default	0	1
$\overline{\text{OEA}}$, $\overline{\text{OEB}}$ (see Table 3)	0	Q _X , $\overline{\text{Q}}_X$ are active. Deassertion of $\overline{\text{OE}}_X$ can be asynchronous to the reference clock without generation of output runt pulses	Q _X = L, $\overline{\text{Q}}_X$ = H (outputs disabled). Assertion of $\overline{\text{OE}}_X$ can be asynchronous to the reference clock without generation of output runt pulses
SEL0, SEL1	00	See Table 3	

TABLE 3: CLOCK SELECT CONTROL

SEL 0	SEL 1	CLK0 routed to	CLK1 routed to	OEA enables/disables	OEB enables/disables	Application Mode
0	0	QA[0:2] and QB[0:2]	---	QA[0:2] and QB[0:2]	---	1:6 fanout of CLK0
0	1	---	QA[0:2] and QB[0:2]	---	QA[0:2] and QB[0:2]	1:6 fanout of CLK1
1	0	QA[0:2]	QB[0:2]	QA[0:2]	QB[0:2]	Dual 1:3 buffer
1	1	QB[0:2]	QA[0:2]	QB[0:2]	QA[0:2]	Dual 1:3 buffer (crossed)

TABLE 4: ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	3.6	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} +0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} +0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

TABLE 5: GENERAL SPECIFICATIONS

Sym- bol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		$V_{CC} - 2^a$		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model)	1500			V	
LU	Latch-up immunity	200			mA	
C_{IN}			4.0		pF	Inputs
θ_{JA}	Thermal resistance junction to ambient JESD 51-3, single layer test board		83.1 73.3 68.9 63.8 57.4	86.0 75.4 70.9 65.3 59.6	°C/W °C/W °C/W °C/W °C/W	Natural convection 100 ft/min 200 ft/min 400 ft/min 800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0 54.4 52.5 50.4 47.8	60.6 55.7 53.8 51.5 48.8	°C/W °C/W °C/W °C/W °C/W	Natural convection 100 ft/min 200 ft/min 400 ft/min 800 ft/min
θ_{JC}	Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
	Operating junction temperature ^b (continuous operation) MTBF = 9.1 years			110	°C	
T_{Func}	Functional temperature range	$T_A = -40$		$T_J = +110$	°C	

a. Output termination voltage $V_{TT} = 0V$ for $V_{CC} = 2.5V$ operation is supported but the power consumption of the device will increase.

b. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 and the application section in this datasheet for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6254 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6254 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

TABLE 6: DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_J = 0^\circ$ to $+110^\circ C$)

Sym- bol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS control inputs ($\overline{OE}A$, $\overline{OE}B$, $SEL0$, $SEL1$)						
V_{IL}	Input voltage low			0.8	V	
V_{IH}	Input voltage high	2.0			V	
I_{IN}	Input Current ^a			± 100	μA	$V_{IN} = V_{CC}$ or $V_{IN} = GND$
LVPECL clock inputs ($CLK0$, $\overline{CLK0}$, $CLK1$, $\overline{CLK1}$)						
V_{PP}	AC differential input voltage ^b	0.1		1.3	V	Differential operation
V_{CMR}	Differential cross point voltage ^c	1.0		$V_{CC} - 0.3$	V	Differential operation
LVPECL clock outputs ($QA0-2$, $\overline{QA0-2}$, $QB0-2$, $\overline{QB0-2}$)						
V_{OH}	Output High Voltage	$V_{CC} - 1.2$	$V_{CC} - 1.005$	$V_{CC} - 0.7$	V	$I_{OH} = -30 \text{ mA}^d$
V_{OL}	Output Low Voltage $V_{CC} = 3.3V \pm 5\%$ $V_{CC} = 2.5V \pm 5\%$	$V_{CC} - 1.9$ $V_{CC} - 1.9$	$V_{CC} - 1.705$ $V_{CC} - 1.705$	$V_{CC} - 1.5$ $V_{CC} - 1.3$	V	$I_{OL} = -5 \text{ mA}^e$
I_{GND}	Maximum Quiescent Supply Current without output termination current		52	85	mA	GND pin

a. Input have internal pullup/pulldown resistors which affect the input current.

b. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristic.

c. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

d. Equivalent to a termination 50Ω to V_{TT} .

e. I_{CC} calculation: $I_{CC} = (\text{number of differential output pairs used}) * (I_{OH} + I_{OL}) + I_{GND}$

$I_{CC} = (\text{number of differential output pairs used}) * (V_{OH} - V_{TT}) \div R_{load} + (V_{OL} - V_{TT}) \div R_{load} + I_{GND}$

TABLE 7: AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_J = 0^\circ$ to $+110^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{PP}	Differential input voltage ^b (peak-to-peak)	0.3		1.3	V	
V_{CMR}	Differential input crosspoint voltage ^c	1.2		$V_{CC}-0.3$	V	
$V_{O(P-P)}$	Differential output voltage (peak-to-peak)					
		$f_O < 1.1$ GHz	0.45	0.7	V	
		$f_O < 2.5$ GHz	0.35	0.55	V	
		$f_O < 3.0$ GHz	0.20	0.35	V	
f_{CLK}	Input Frequency	0		3000 ^d	MHz	
t_{PD}	Propagation delay CLK, 1 to QA[] or QB[]	485	360	610	ps	Differential
$t_{sk(O)}$	Output-to-output skew			50	ps	Differential
$t_{sk(PP)}$	Output-to-output skew (part-to-part)			250	ps	Differential
$t_{SK(P)}$	Output pulse skew ^e			60	ps	
DC_O	Output duty cycle	$t_{REF} < 100$ MHz	49.4	50.6	%	$DC_{fref} = 50\%$
		$t_{REF} < 800$ MHz	45.2	54.8	%	$DC_{fref} = 50\%$
$t_{JIT(CC)}$	Output cycle-to-cycle jitter (SEL0 $\neq$ SEL1)			TBD		
t_r, t_f	Output Rise/Fall Time	0.05		300	ps	20% to 80%
t_{PDLf}	Output disable time	$2.5 \cdot T + t_{PD}$		$3.5 \cdot T + t_{PD}$	ns	$T = CLK$ period
t_{PLDg}	Output enable time	$3 \cdot T + t_{PD}$		$4 \cdot T + t_{PD}$	ns	$T = CLK$ period

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

b. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.

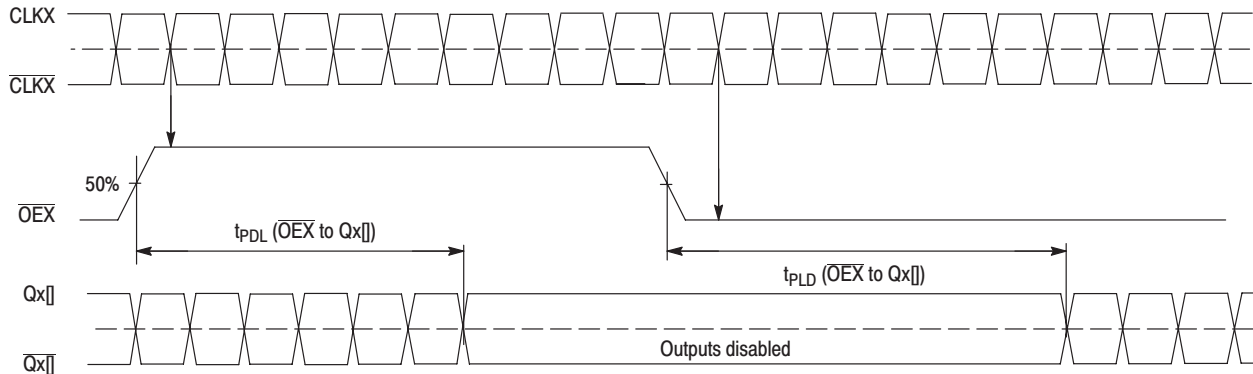
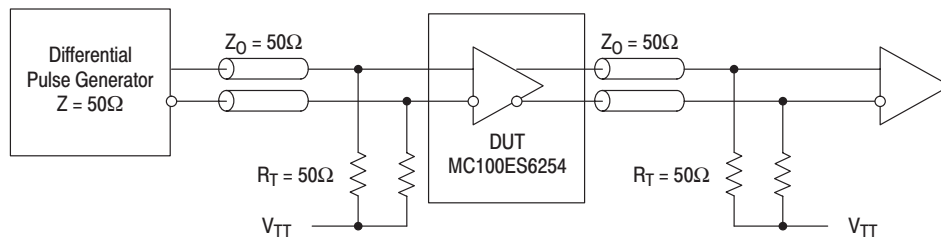
c. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.

d. The MC100ES6254 is fully operational up to 3.0 GHz and is characterized up to 2.7 GHz.

e. Output pulse skew is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PLL}|$.

f. Propagation delay $\overline{OE}$ deassertion to differential output disabled (differential low: true output low, complementary output high).

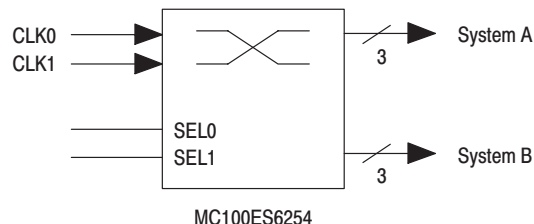
g. Propagation delay $\overline{OE}$ assertion to output enabled (active).

**Figure 3. MC100ES6254 output disable/enable timing****Figure 4. MC100ES6254 AC test reference**

APPLICATIONS INFORMATION

Example Configurations

2x2 clock switch

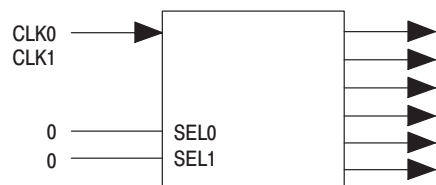


MC100ES6254

SEL0	SEL1	Switch configuration
0	0	CLK0 clocks system A and system B
0	1	CLK1 clocks system A and system B
1	0	CLK0 clocks system A and CLK1 clocks system
1	1	CLK1 clocks system B and CLK1 clocks system

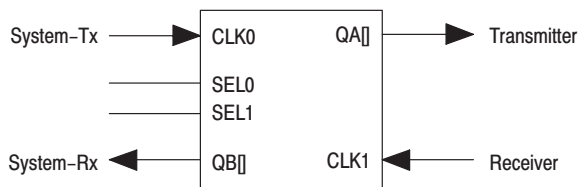
A

1:6 Clock Fanout Buffer



MC100ES6254

Loopback device



MC100ES6254

SEL0	SEL1	Switch configuration
0	0	System loopback
0	1	Line loopback
1	0	Transmit / Receive operation
1	1	System and line loopback

Understanding the junction temperature range of the MC100ES6254

To make the optimum use of high clock frequency and low skew capabilities of the MC100ES6254, the MC100ES6254 is specified, characterized and tested for the junction temperature range of $T_J = 0^\circ\text{C}$ to $+110^\circ\text{C}$. Because the exact thermal performance depends on the PCB type, design, thermal management and natural or forced air convection, the junction temperature provides an exact way to correlate the application specific conditions to the published performance data of this datasheet. The correlation of the junction temperature range to the application ambient temperature range and vice versa can be done by calculation:

$$T_J = T_A + R_{thja} \cdot P_{tot}$$

Assuming a thermal resistance (junction to ambient) of 54.4°C/W (2s2p board, 200 ft/min airflow, see table 4) and a typical power consumption of 467 mW (all outputs terminated 50 ohms to V_{TT} , $V_{CC} = 3.3\text{V}$, frequency independent), the junction temperature of the MC100ES6254 is approximately $T_A + 24.5^\circ\text{C}$, and the minimum ambient temperature in this example case calculates to -24.5°C (the maximum ambient temperature is 85.5°C . See Table 8). Exceeding the minimum junction temperature specification of the MC100ES6254 does not have a significant impact on the device functionality. However, the continuous use the MC100ES6254 at high ambient temperatures requires thermal management to not exceed the specified maximum junction temperature. Please see the application note AN1545 for a power consumption calculation guideline.

Table 8: Ambient temperature ranges ($P_{tot} = 467\text{ mW}$)

R _{thja} (2s2p board)		T _{A, min} ^a	T _{A, max}
Natural convection	59.0 °C/W	-28 °C	82 °C
100 ft/min	54.4 °C/W	-25 °C	85 °C
200 ft/min	52.5 °C/W	-24.5 °C	85.5 °C
400 ft/min	50.4 °C/W	-23.5 °C	86.5 °C
800 ft/min	47.8 °C/W	-22 °C	88 °C

a. The MC100ES6254 device function is guaranteed from $T_A = -40^\circ\text{C}$ to $T_J = 110^\circ\text{C}$

Maintaining Lowest Device Skew

The MC100ES6254 guarantees low output-to-output bank skew of 50 ps and a part-to-part skew of max. 250 ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. If an entire output bank is not used, it is recommended to leave all of these outputs open and unterminated. This will reduce the device power consumption while maintaining minimum output skew.

Power Supply Bypassing

The MC100ES6254 is a mixed analog/digital product. The differential architecture of the MC100ES6254 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above

the noise bandwidth.

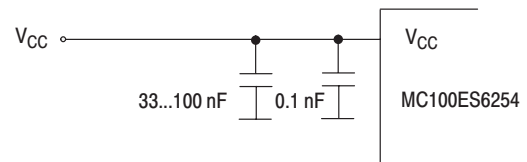


Figure 5. V_{CC} Power Supply Bypass

Preliminary Information

Low Voltage 1:10 Differential LVDS Clock Fanout Buffer

The Motorola MC100ES7111 is a LVDS differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES7111 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are high performance clock distribution in computing, networking and telecommunication systems.

Features:

- 1:10 differential clock fanout buffer
- 50 ps maximum device skew¹
- SiGe technology
- Supports DC to 1000 MHz operation³ of clock or data signals
- LVDS compatible differential clock outputs
- PECL and HSTL/LVDS compatible differential clock inputs
- 3.3V power supply
- Supports industrial temperature range
- Standard 32 lead LQFP package

Functional Description

The MC100ES7111 is designed for low skew clock distribution systems and supports clock frequencies up to 1000 MHz¹. The device accepts two clock sources. The CLK0 input accepts LVDS or HSTL compatible signals and CLK1 accepts PECL compatible signals. The selected input signal is distributed to 10 identical, differential LVDS compatible outputs.

The output enable control is synchronized internally preventing output runt pulse generation. Outputs are only disabled or enabled when the outputs are already in logic low state (true outputs logic low, inverted outputs logic high). The internal synchronizer eliminates the setup and hold time requirements for the external clock enable signal. The device is packaged in a 7x7 mm² 32-lead LQFP package.

MC100ES7111**LOW-VOLTAGE
1:10 DIFFERENTIAL
LVDS CLOCK
FANOUT DRIVER****FA SUFFIX**
32-LEAD LQFP PACKAGE
CASE 873A

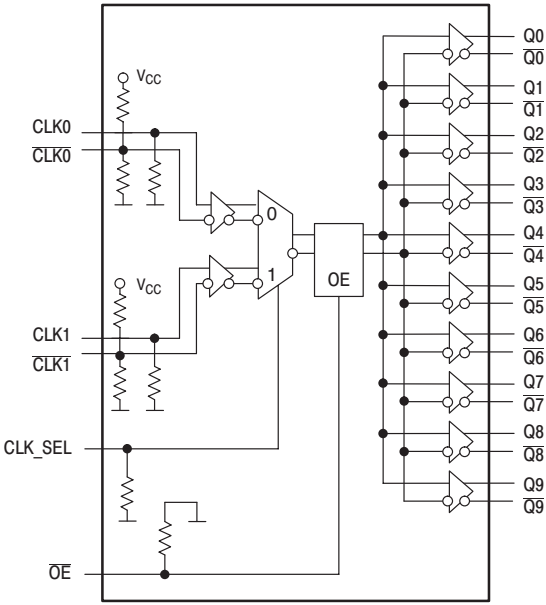


Figure 1. MC100ES7111 Logic Diagram

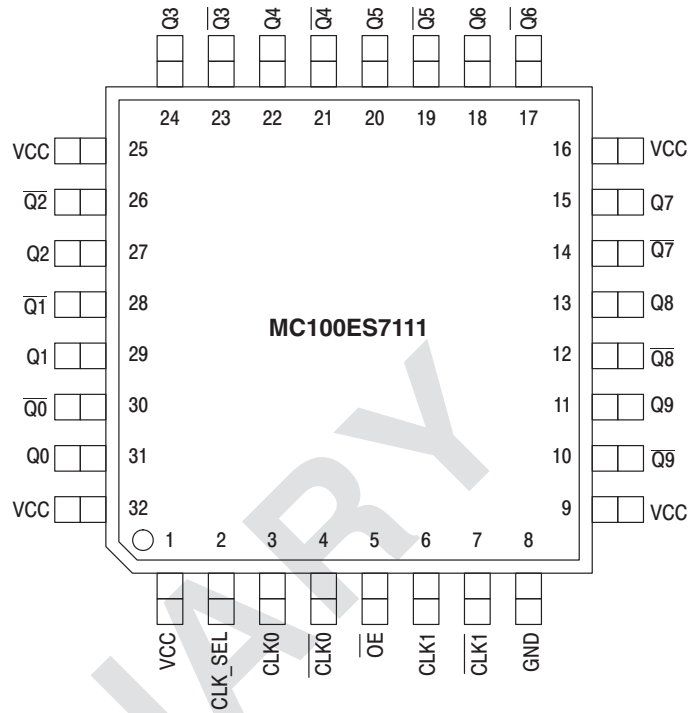


Figure 2. 32-Lead Package Pinout (Top View)

Table 1. PIN CONFIGURATION

Pin	I/O	Type	Function
CLK0, CLK0	Input	HSTL/LVDS	Differential HSTL or LVDS reference clock signal input
CLK1, CLK1	Input	PECL	Differential PECL reference clock signal input
CLK_SEL	Input	LVC MOS	Reference clock input select
OE	Input	LVC MOS	Output enable/disable. OE is synchronous to the input reference clock which eliminates possible output runt pulses when the OE state is changed.
Q[0-9], Q[0-9]	Output	LVDS	Differential clock outputs
GND	Supply		Negative power supply
VCC	Supply		Positive power supply of the device (3.3V)

Table 2. FUNCTION TABLE

Control	Default	0	1
CLK_SEL	0	CLK0, CLK0 (HSTL/LVDS) is the active differential clock input	CLK1, CLK1 (PECL) is the active differential clock input
OE	0	Q[0-9], Q[0-9] are active. Deassertion of OE can be asynchronous to the reference clock without generation of output runt pulses.	Q[0-9] = L, Q[0-9] =H (outputs disabled). Assertion of OE can be asynchronous to the reference clock without generation of output runt pulses.

Table 3. Absolute Maximum Ratings^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	3.9	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} + 0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} + 0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage temperature	-65	125	°C	
T _{Func}	Functional temperature range	T _A = -40	T _J = +110	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model)	TBD			V	
LU	Latch-up immunity	200			mA	
C _{IN}	Input Capacitance		4.0		pF	Inputs
θ _{JA}	Thermal resistance junction to ambient JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ _{JC}	Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
T _J	Operating junction temperature ^a (continuous operation) MTBF = 9.1 years			110	°C	

a. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 and the application section in this datasheet for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES7111 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES7111 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 5. DC Characteristics ($V_{CC} = 3.3V \pm 5\%$, $T_J = 0^\circ\text{C}$ to $+110^\circ\text{C}$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLK0, $\overline{\text{CLK0}}$ (HSTL/LVDS differential signals)						
V_{DIF}	Differential input voltage ^b	0.2			V	
$V_{X, IN}$	Differential cross point voltage ^c	0.25	0.68 - 0.9	$V_{CC} - 1.3$	V	
V_{IH}	Input high voltage	$V_X + 0.1$			V	
V_{IL}	Input low voltage			$V_X - 0.1$	V	
I_{IN}	Input Current			± 150	mA	$V_{IN} = V_X \pm 0.1V$
Clock input pair CLK1, $\overline{\text{CLK1}}$ (PECL differential signals)						
V_{PP}	Differential input voltage ^d	0.15		1.0	V	Differential operation
V_{CMR}	Differential cross point voltage ^e	1.0		$V_{CC} - 0.6$	V	Differential operation
V_{IH}	Input voltage high	$V_{CC} - 1.165$		$V_{CC} - 0.880$	V	
V_{IL}	Input voltage low	$V_{CC} - 1.810$		$V_{CC} - 1.475$	V	
I_{IN}	Input Current ^a			± 150	mA	$V_{IN} = V_{IH}$ or V_{IL}
LVCMOS control inputs $\overline{\text{OE}}$, CLK_SEL						
V_{IL}	Input voltage low			0.8	V	
V_{IH}	Input voltage high	2.0			V	
I_{IN}	Input Current			± 150	mA	$V_{IN} = V_{IH}$ or V_{IL}
LVDS clock outputs (Q[0-9], $\overline{\text{Q}}[0-9]$)						
V_{PP}	Output Differential Voltage (peak-to-peak)	250			mV	LVDS
V_{OS}	Output Offset Voltage	1125		1275	mV	LVDS
Supply current						
I_{CC}	Maximum Quiescent Supply Current without output termination current		TBD	TBD	mA	V_{CC} pin (core)

a. DC characteristics are design targets and pending characterization.

b. V_{DIF} (DC) is the minimum differential HSTL/LVDS input voltage swing required for device functionality.

c. V_X (DC) is the crosspoint of the differential HSTL/LVDS input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.

d. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.

e. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 6. AC Characteristics ($V_{CC} = 3.3V \pm 5\%$, $T_J = 0^\circ\text{C}$ to $+110^\circ\text{C}$) ^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLK0, $\overline{\text{CLK0}}$ (HSTL/LVDS differential signals)						
V_{DIF}	Differential input voltage ^c (peak-to-peak)	0.4			V	
$V_{X, \text{IN}}$	Differential cross point voltage ^d	0.68		1.275	V	
f_{CLK}	Input Frequency		1000	TBD	MHz	
t_{PD}	Propagation Delay CLK0 to Q[0-9]			TBD	ps	
Clock input pair CLK1, $\overline{\text{CLK1}}$ (PECL differential signals)						
V_{PP}	Differential input voltage ^e (peak-to-peak)	0.2		1.0	V	
V_{CMR}	Differential input crosspoint voltage ^f	1		$V_{\text{CC}} - 0.6$	V	
f_{CLK}	Input Frequency		1000		MHz	Differential
t_{PD}	Propagation Delay CLK1 to Q[0-9]			TBD	ps	Differential
LVDS clock outputs (Q[0-9], $\overline{\text{Q}}[0-9]$)						
$t_{\text{sk(O)}}$	Output-to-output skew			50	ps	Differential
$t_{\text{sk(PP)}}$	Output-to-output skew (part-to-part)			TBD	ps	Differential
$t_{\text{JIT(CC)}}$	Output cycle-to-cycle jitter			TBD		
DC_O	Output duty cycle	TBD	50	TBD	%	$\text{DC}_{\text{fref}} = 50\%$
t_r, t_f	Output Rise/Fall Time	0.05		TBD	ns	20% to 80%
t_{PDL}^g	Output disable time	$2.5 \cdot T + t_{\text{PD}}$		$3.5 \cdot T + t_{\text{PD}}$	ns	$T = \text{CLK period}$
t_{PLD}^h	Output enable time	$3 \cdot T + t_{\text{PD}}$		$4 \cdot T + t_{\text{PD}}$	ns	$T = \text{CLK period}$

a. AC characteristics are design targets and pending characterization.

b. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

c. V_{DIF} (DC) is the minimum differential HSTL/LVDS input voltage swing required for device functionality.

d. V_X (DC) is the crosspoint of the differential HSTL/LVDS input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{DIF} (DC) specification.

e. V_{PP} (AC) is the minimum differential PECL input voltage swing required to maintain AC characteristics including t_{pd} and device-to-device skew.

f. V_{CMR} (AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.

g. Propagation delay $\overline{\text{OE}}$ deassertion to differential output disabled (differential low: true output low, complementary output high).

h. Propagation delay $\overline{\text{OE}}$ assertion to output enabled (active).

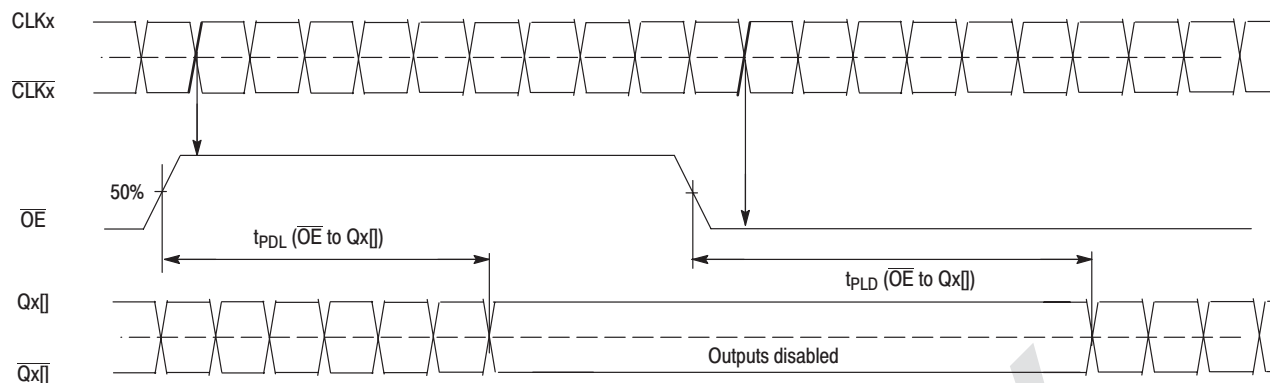


Figure 3. MC100ES7111 AC test reference

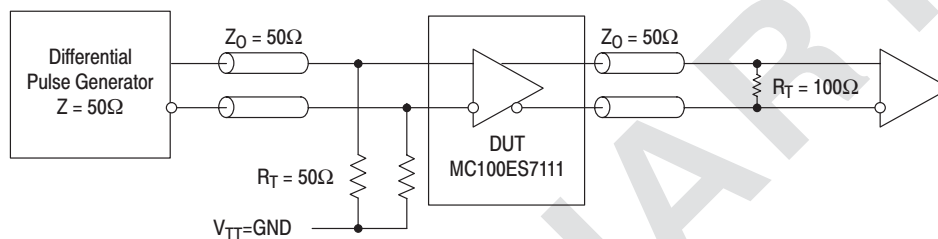


Figure 4. MC100ES7111 AC test reference

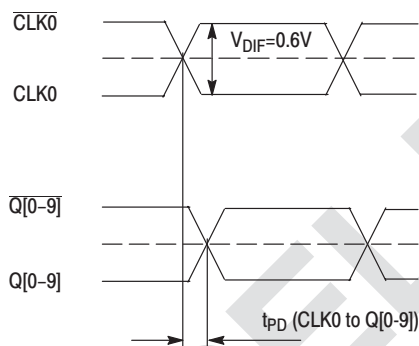


Figure 5. MC100ES7111 AC reference measurement waveform (HSTL input)

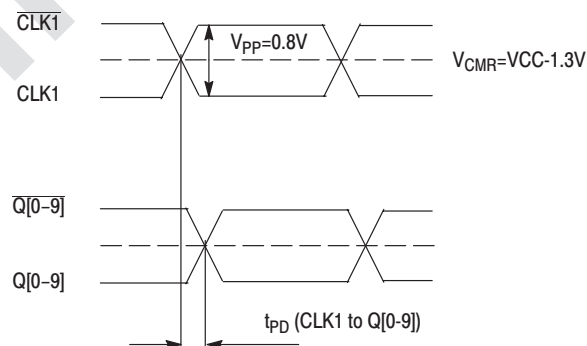


Figure 6. MC100ES7111 AC reference measurement waveform (PECL input)

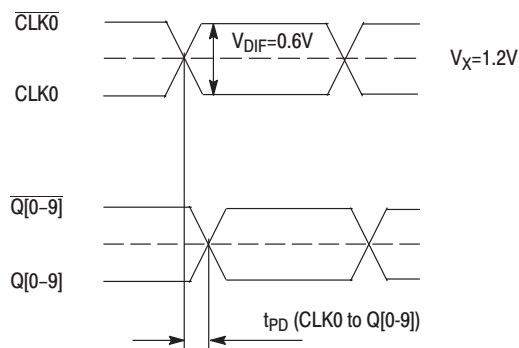


Figure 7. MC100ES7111 AC reference measurement waveform (LVDS input)

Preliminary Information

Low Voltage 1:10 Differential HSTL Clock Fanout Buffer

The Motorola MC100ES8111 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES8111 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are high performance clock distribution in computing, networking and telecommunication systems.

Features:

- 1:10 differential clock fanout buffer
- 50 ps maximum device skew¹
- SiGe technology
- Supports DC to 400 MHz operation⁴ of clock or data signals
- 1.5V HSTL compatible differential clock outputs
- PECL and HSTL compatible differential clock inputs
- 3.3V power supply for device core, 1.5V or 1.8V HSTL output supply
- Supports industrial temperature range
- Standard 32 lead LQFP package

Functional Description

The MC100ES8111 is designed for low skew clock distribution systems and supports clock frequencies up to 400 MHz¹. The device accepts two clock sources. The CLK0 input accepts HSTL compatible signals and CLK1 accepts PECL compatible signals. The selected input signal is distributed to 10 identical, differential HSTL compatible outputs.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all 10 outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The HSTL compatible output levels are generated with an open emitter architecture. This minimizes part-to-part and output-to-output skew. The open-emitter outputs require a 50Ω DC termination to GND (0V). The output supply voltage can be either 1.5V or 1.8V, the core voltage supply is 3.3V. The output enable control is synchronized internally preventing output runt pulse generation. Outputs are only disabled or enabled when the outputs are already in logic low state (true outputs logic low, inverted outputs logic high). The internal synchronizer eliminates the setup and hold time requirements for the external clock enable signal. The device is packaged in a 7x7 mm² 32-lead LQFP package.

MC100ES8111**LOW-VOLTAGE
1:10 DIFFERENTIAL
HSTL CLOCK
FANOUT DRIVER****FA SUFFIX**
32-LEAD LQFP PACKAGE
CASE 873A

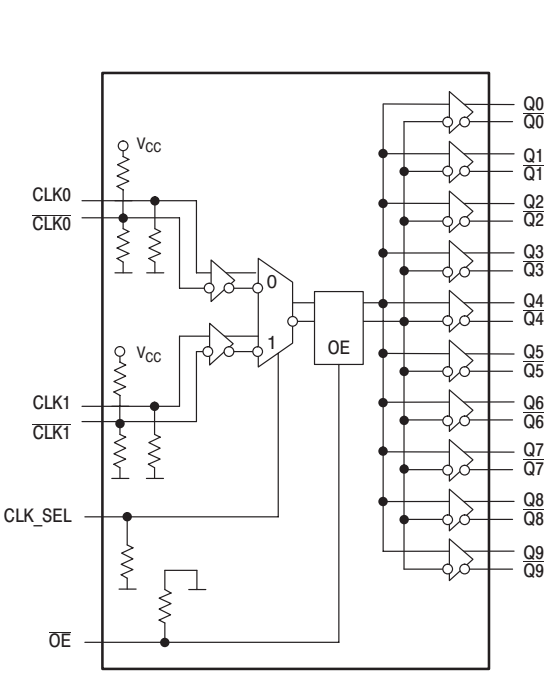


Figure 1. MC100ES8111 Logic Diagram

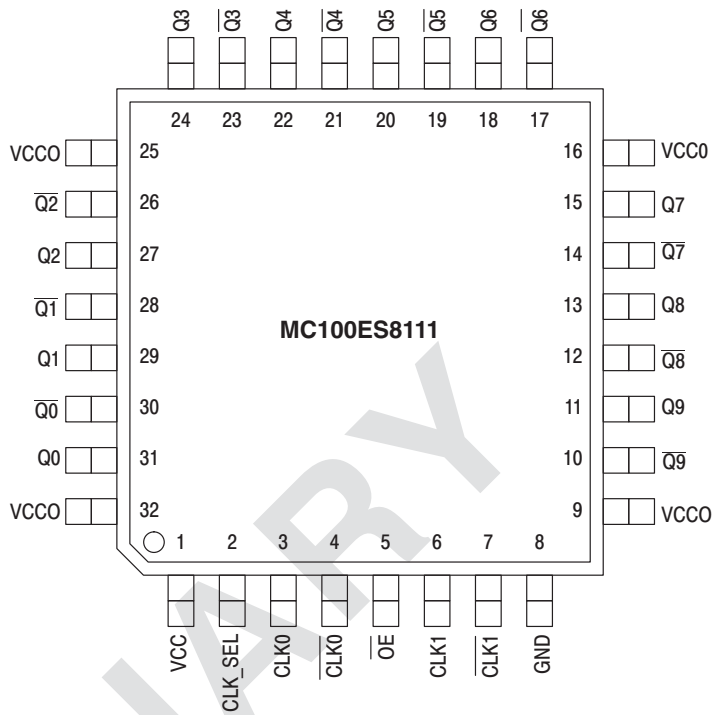


Figure 2. 32-Lead Package Pinout (Top View)

Table 1. PIN CONFIGURATION

Pin	I/O	Type	Function
CLK0, $\overline{\text{CLK0}}$	Input	HSTL	Differential HSTL reference clock signal input
CLK1, $\overline{\text{CLK1}}$	Input	PECL	Differential PECL reference clock signal input
CLK_SEL	Input	LVC MOS	Reference clock input select
$\overline{\text{OE}}$	Input	LVC MOS	Output enable/disable. OE is synchronous to the input reference clock which eliminates possible output runt pulses when the OE state is changed.
Q[0-9], $\overline{\text{Q[0-9]}}$	Output	ECL/PECL	Differential clock outputs
GND	Supply		Negative power supply
V _{CC}	Supply		Positive power supply of the device core (3.3V)
V _{CC0}	Supply		Positive power supply of the HSTL outputs. All V _{CC0} pins must be connected to the positive power supply (1.5V or 1.8V) for correct DC and AC operation.

Table 2. FUNCTION TABLE

Control	Default	0	1
CLK_SEL	0	CLK0, $\overline{\text{CLK0}}$ (HSTL) is the active differential clock input	CLK1, $\overline{\text{CLK1}}$ (PECL) is the active differential clock input
$\overline{\text{OE}}$	0	Q[0-9], $\overline{\text{Q[0-9]}}$ are active. Deassertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses.	Q[0-9] = L, $\overline{\text{Q[0-9]}}$ = H (outputs disabled). Assertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses.

Table 3. Absolute Maximum Ratings^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	3.6	V	
V _{CCO}	Supply Voltage	-0.3	3.1	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} + 0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} + 0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage temperature	-65	125	°C	
T _{Func}	Functional temperature range	T _A = -40	T _J = +110	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output termination voltage		0		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model)	TBD			V	
LU	Latch-up immunity	200			mA	
C _{IN}	Input Capacitance		4.0		pF	Inputs
θ _{JA}	Thermal resistance junction to ambient JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ _{JC}	Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
T _J	Operating junction temperature ^a (continuous operation) MTBF = 9.1 years			110	°C	

a. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 and the application section in this datasheet for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES8111 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES8111 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 5. DC Characteristics ($V_{CC} = 3.3V \pm 5\%$, $V_{CCO} = 1.5V \pm 0.1V$ or $V_{CCO} = 1.8V \pm 0.1V$, $T_J = 0^\circ C$ to $+110^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLK0, $\overline{CLK0}$ (HSTL differential signals)						
V_{DIF}	Differential input voltage ^b	0.2			V	
$V_{X, IN}$	Differential cross point voltage ^c	0.25	0.68 - 0.9	$V_{CC} - 1.3$	V	
V_{IH}	Input high voltage	$V_{X} + 0.1$			V	
V_{IL}	Input low voltage			$V_{X} - 0.1$	V	
I_{IN}	Input Current			± 150	mA	$V_{IN} = V_X \pm 0.1V$
Clock input pair CLK1, $\overline{CLK1}$ (PECL differential signals)						
V_{PP}	Differential input voltage ^d	0.15		1.0	V	Differential operation
V_{CMR}	Differential cross point voltage ^e	1.0		$V_{CC} - 0.6$	V	Differential operation
V_{IH}	Input voltage high	$V_{CC} - 1.165$		$V_{CC} - 0.880$	V	
V_{IL}	Input voltage low	$V_{CC} - 1.810$		$V_{CC} - 1.475$	V	
I_{IN}	Input Current ^a			± 150	mA	$V_{IN} = V_{IH}$ or V_{IL}
LVCMOS control inputs $\overline{OE}$, CLK_SEL						
V_{IL}	Input voltage low			0.8	V	
V_{IH}	Input voltage high	2.0			V	
I_{IN}	Input Current			± 150	mA	$V_{IN} = V_{IH}$ or V_{IL}
HSTL clock outputs (Q[0-9], $\overline{Q}$ [0-9])						
$V_{X, OUT}$	Output differential crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output High Voltage	1			V	
V_{OL}	Output Low Voltage			0.4	V	
Supply current						
I_{CC}	Maximum Quiescent Supply Current without output termination current		100	TBD	mA	V_{CC} pin (core)
I_{CCO}^f	Maximum Quiescent Supply Current, outputs terminated 50Ω to V_{TT}		TBD	TBD	mA	V_{CCO} pins (outputs)

a. DC characteristics are design targets and pending characterization.

b. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality.

c. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.

d. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.

e. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

f. I_{CC} includes current through the output resistors (all outputs terminated to V_{TT}).

Table 6. AC Characteristics ($V_{CC} = 3.3V \pm 5\%$, $V_{CCO} = 1.5V \pm 0.1V$ or $V_{CCO} = 1.8V \pm 0.1V$, $T_J = 0^\circ C$ to $+110^\circ C$) ^{a b}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLK0, $\overline{CLK0}$ (HSTL differential signals)						
V_{DIF}	Differential input voltage ^c (peak-to-peak)	0.4			V	
$V_{X, IN}$	Differential cross point voltage ^d	0.68		0.9	V	
f_{CLK}	Input Frequency		0-400	TBD	MHz	
t_{PD}	Propagation Delay CLK0 to Q[0-9]			TBD	ps	
Clock input pair CLK1, $\overline{CLK1}$ (PECL differential signals)						
V_{PP}	Differential input voltage ^e (peak-to-peak)	0.2		1.0	V	
V_{CMR}	Differential input crosspoint voltage ^f	1		$V_{CC}-0.6$	V	
f_{CLK}	Input Frequency		0-400		MHz	Differential
t_{PD}	Propagation Delay CLK1 to Q[0-9]			TBD	ps	Differential
HSTL clock outputs (Q[0-9], $\overline{Q}$ [0-9])						
$V_{X, OUT}$	Output differential crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output High Voltage	1			V	
V_{OL}	Output Low Voltage			0.5	V	
$V_{O(P-P)}$	Differential output voltage (peak-to-peak)	0.5			V	
$t_{sk(O)}$	Output-to-output skew			50	ps	Differential
$t_{sk(PP)}$	Output-to-output skew (part-to-part)			TBD	ps	Differential
$t_{JIT(CC)}$	Output cycle-to-cycle jitter			TBD		
DC_O	Output duty cycle	TBD	50	TBD	%	$DC_{fref} = 50\%$
t_r, t_f	Output Rise/Fall Time	0.05		TBD	ns	20% to 80%
t_{PDL}^g	Output disable time	$2.5 \cdot T + t_{PD}$		$3.5 \cdot T + t_{PD}$	ns	$T = CLK$ period
t_{PLD}^h	Output enable time	$3 \cdot T + t_{PD}$		$4 \cdot T + t_{PD}$	ns	$T = CLK$ period

a. AC characteristics are design targets and pending characterization.

b. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

c. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality.

d. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{DIF} (DC) specification.

e. V_{PP} (AC) is the minimum differential PECL input voltage swing required to maintain AC characteristics including t_{pd} and device-to-device skew.

f. V_{CMR} (AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.

g. Propagation delay $\overline{OE}$ deassertion to differential output disabled (differential low: true output low, complementary output high).

h. Propagation delay $\overline{OE}$ assertion to output enabled (active).

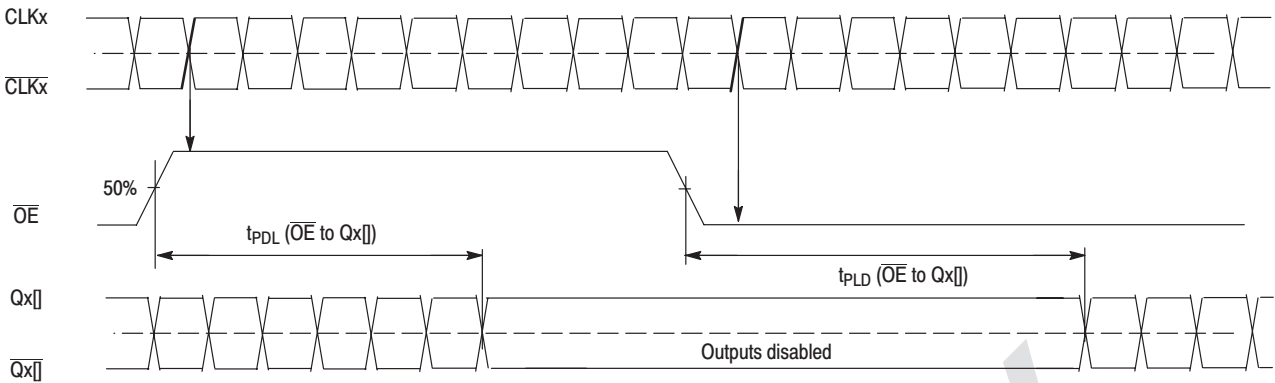


Figure 3. MC100ES8111 AC test reference

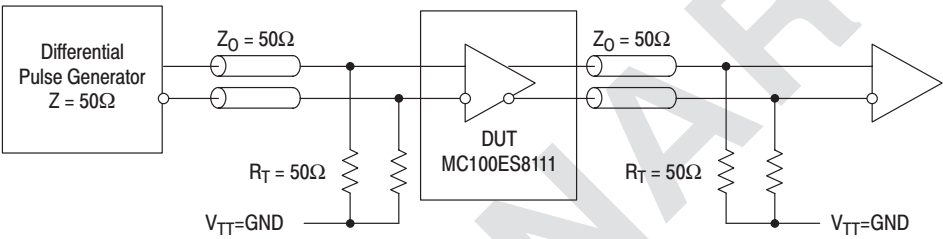


Figure 4. MC100ES8111 AC test reference

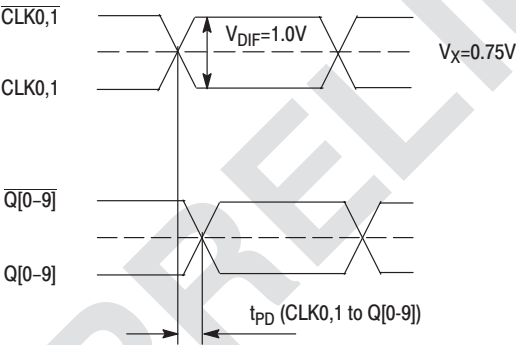


Figure 5. MC100ES8111 AC reference measurement waveform (HSTL input)

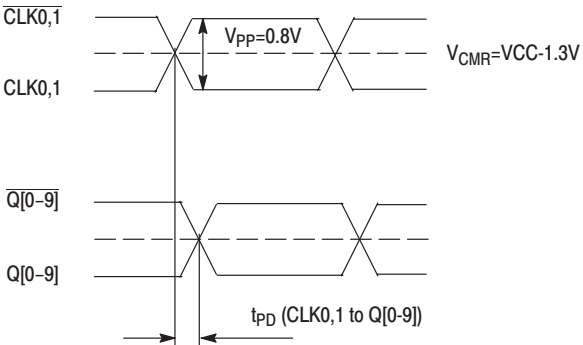


Figure 6. MC100ES8111 AC reference measurement waveform (PECL input)

Preliminary Information

Low Voltage 1:22 Differential HSTL Clock Fanout Buffer

The Motorola MC100ES8223 is a bipolar monolithic differential clock fanout buffer. Designed for the most demanding clock distribution systems, the MC100ES8223 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are high performance clock distribution in computing, networking and telecommunication systems.

Features

- 1:22 differential clock fanout buffer
- 50 ps maximum device skew¹
- SiGe technology
- Supports DC to 800 MHz operation¹ of clock or data signals
- 1.5V HSTL compatible differential clock outputs
- PECL and HSTL compatible differential clock inputs
- 3.3V power supply for device core, 1.5V or 1.8V HSTL output supply
- Standard 64 lead LQFP package with exposed pad for enhanced thermal characteristics
- Supports industrial temperature range
- Pin and function compatible to the MC100EP223

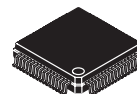
Functional Description

The MC100ES8223 is designed for low skew clock distribution systems and supports clock frequencies up to 800 MHz¹. The device accepts two clock sources. The HCLK input can be driven by HSTL compatible signals, the PCLK input accepts PECL compatible signals. The selected input signal is distributed to 22 identical, differential HSTL outputs.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all 22 outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The HSTL compatible output levels are generated with an open emitter architecture. This minimizes part-to-part and output-to-output skew. The open-emitter outputs require a 50Ω DC termination to GND (0V). The output supply voltage can be either 1.5V or 1.8V, the core voltage supply is 3.3V. The output enable (OE) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. In the case of an asynchronous control, there is a chance of generating a 'runt' clock pulse when the device is enabled/disabled.

The MC100ES8223 is pin and function compatible to the MC100EP223.

MC100ES8223**LOW-VOLTAGE
1:22 DIFFERENTIAL HSTL
CLOCK FANOUT DRIVER****TC SUFFIX**
64-LEAD LQFP PACKAGE
EXPOSED PAD
CASE 840K**7**

2. AC specifications are design targets and subject to change

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

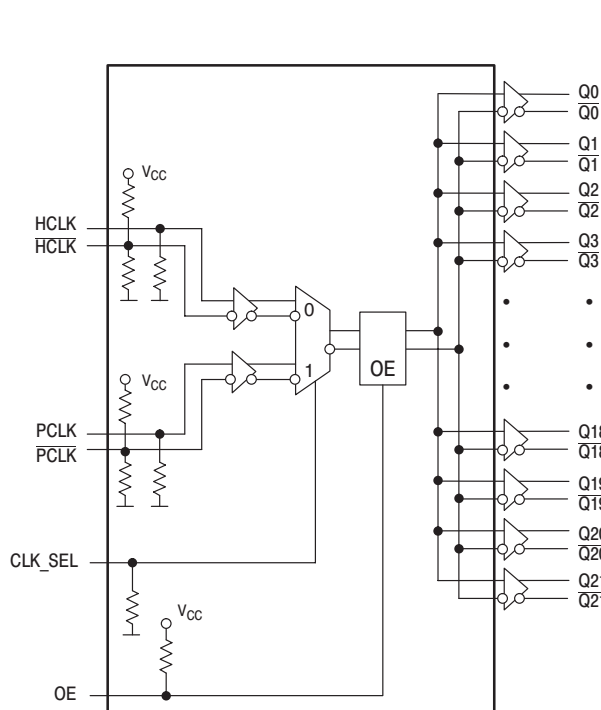


Figure 1. MC100ES8223 Logic Diagram

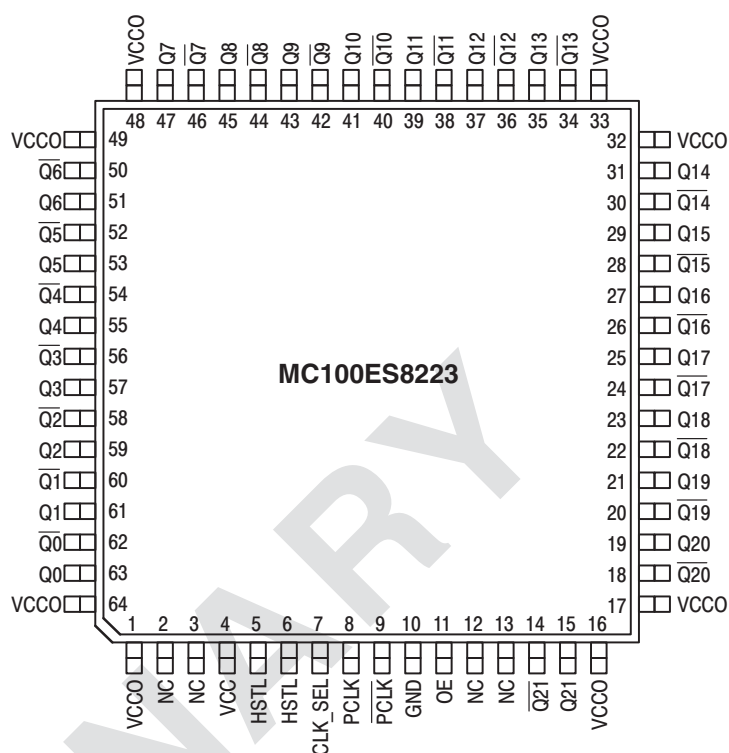


Figure 2. 64-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
HCLK1, $\overline{\text{HCLK}}$	Input	HSTL	Differential HSTL reference clock signal input
PCLK, $\overline{\text{PCLK0}}$	Input	PECL	Differential PECL reference clock signal input
CLK_SEL	Input	LVCMOS	Reference clock input select
OE	Input	LVCMOS	Output enable/disable. OE is synchronous to the input reference clock which eliminates possible output runt pulses when the OE state is changed.
Q[0-21], $\overline{\text{Q}}[0-21]$	Output	HSTL	Differential clock outputs
GND	Supply		Negative power supply
V _{CC}	Supply		Positive power supply of the device core (3.3V)
V _{CC0}	Supply		Positive power supply of the HSTL outputs. All V _{CC0} pins must be connected to the positive power supply (1.5V or 1.8V) for correct DC and AC operation.

Table 2. Function Table

Pin	0	1
CLK_SEL	HCLK, HCLK input pair is the reference clock. HCLK is HSTL compatible.	PCLK, PCLK input pair is the reference clock. PCLK is PECL compatible.
OE	Outputs disabled, Q[0:21]=L, $\overline{Q[0:21]}$ =H	Outputs enabled

Table 3. Absolute Maximum Ratings^a

Symbol	Characteristics	Min	Max	Unit	Condition
V _{CC}	Supply Voltage	-0.3	3.6	V	
V _{CCO}	Supply Voltage	-0.3	3.6	V	
V _{IN}	DC Input Voltage	-0.3	V _{CC} + 0.3	V	
V _{OUT}	DC Output Voltage	-0.3	V _{CC} + 0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output termination voltage		0		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model)	TBD			V	
LU	Latch-up immunity	200			mA	
C _{IN}	Input Capacitance		4.0		pF	Inputs
θ _{JA} , θ _{JB} , θ _{JC}	Thermal resistance (junction-to-ambient, junction-to-board, junction-to-case)	See Table 7 "Thermal Resistance" on page 752			°C/W	
T _J	Operating junction temperature ^a (continuous operation) MTBF = 9.1 years	0		110	°C	

a. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES8223 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES8223 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 5. DC Characteristics ($V_{CC} = 3.3V \pm 5\%$, $V_{CCO} = 1.5V \pm 0.1V$ or $V_{CCO} = 1.8V \pm 0.1V$, $T_J = 0^\circ C$ to $+110^\circ C$)^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair HCLK, HCLK (HSTL differential signals)						
V_{DIF}	Differential input voltage ^b	0.2			V	
$V_{X, IN}$	Differential cross point voltage ^c	0.68		0.9	V	
V_{IH}	Input high voltage	$V_X + 0.1$			V	
V_{IL}	Input low voltage			$V_X - 0.1$	V	
I_{IN}	Input Current			± 150	μA	$V_{IN} = V_X \pm 0.1V$
Clock input pair PCLK, PCLK (PECL differential signals)						
V_{PP}	Differential input voltage ^d	0.15		1.0	V	Differential operation
V_{CMR}	Differential cross point voltage ^e	1.0		$V_{CC} - 0.6$	V	Differential operation
V_{IH}	Input voltage high	$V_{CC} - 1.165$		$V_{CC} - 0.880$	V	
V_{IL}	Input voltage low	$V_{CC} - 1.810$		$V_{CC} - 1.475$	V	
I_{IN}	Input Current ^a			± 150	μA	$V_{IN} = V_{IH}$ or V_{IL}
LVCMOS control inputs OE, CLK_SEL						
V_{IL}	Input voltage low			0.8	V	
V_{IH}	Input voltage high	2.0			V	
I_{IN}	Input Current			± 150	μA	$V_{IN} = V_{IH}$ or V_{IL}
HSTL clock outputs (Q[0-21], Q[0-21])						
$V_{X, OUT}$	Output differential crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output High Voltage	1.1			V	
V_{OL}	Output Low Voltage			0.4	V	
Supply current						
I_{CC}	Maximum Quiescent Supply Current without output termination current		TBD	TBD	mA	V_{CC} pin (core)
I_{CCO}^f	Maximum Quiescent Supply Current, outputs terminated 50 Ω to V_{TT}		TBD	TBD	mA	V_{CCO} pins (outputs)

a. DC characteristics are design targets and pending characterization.

b. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality.

c. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.

d. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.

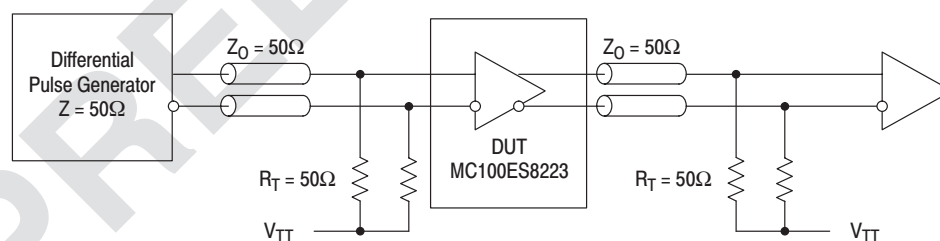
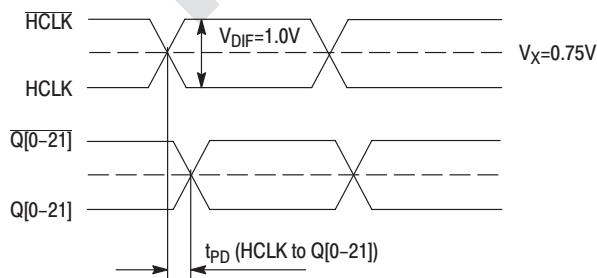
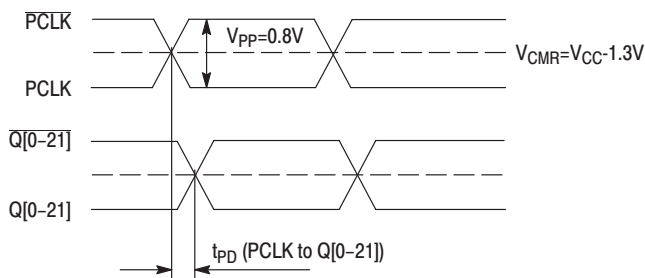
e. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

f. I_{CC} includes current through the output resistors (all outputs terminated to V_{TT}).

Table 6. AC Characteristics ($V_{CC} = 3.3V \pm 5\%$, $V_{CCO} = 1.5V \pm 0.1V$ or $V_{CCO} = 1.8V \pm 0.1V$, $T_J = 0^\circ C$ to $+110^\circ C$)^{a b}

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair HCLK, HCLK (HSTL differential signals)						
V_{DIF}	Differential input voltage ^c (peak-to-peak)	0.4			V	
$V_{X, IN}$	Differential cross point voltage ^d	0.68		0.9	V	
f_{CLK}	Input Frequency		0-800	TBD	MHz	
t_{PD}	Propagation Delay HCLK0 to Q[0-21]			TBD	ps	
Clock input pair PCLK, PCLK (PECL differential signals)						
V_{PP}	Differential input voltage ^e (peak-to-peak)	0.2		1.0	V	
V_{CMR}	Differential input crosspoint voltage ^f	1		$V_{CC}-0.6$	V	
f_{CLK}	Input Frequency		0-800		MHz	Differential
t_{PD}	Propagation Delay PCLK0 to Q[0-21]			TBD	ps	Differential
HSTL clock outputs (Q[0-21], $\overline{Q}$ [0-21])						
$V_{X, OUT}$	Output differential crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output High Voltage	1			V	
V_{OL}	Output Low Voltage			0.5	V	
$V_{O(P-P)}$	Differential output voltage (peak-to-peak)	0.5			V	
$t_{sk(O)}$	Output-to-output skew			50	ps	Differential
$t_{sk(PP)}$	Output-to-output skew (part-to-part)			TBD	ps	Differential
$t_{JIT(CC)}$	Output cycle-to-cycle jitter			TBD		
DC_O	Output duty cycle	TBD	50	TBD	%	$DC_{fref} = 50\%$
t_r, t_f	Output Rise/Fall Time	0.05		TBD	ns	20% to 80%

- a. DC characteristics are design targets and pending characterization.
b. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
c. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality.
d. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{DIF} (DC) specification.
e. V_{PP} (AC) is the minimum differential PECL input voltage swing required to maintain AC characteristics including t_{pd} and device-to-device skew.
f. V_{CMR} (AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.

**Figure 3. MC100ES8223 AC test reference****Figure 4. MC100ES8223 AC reference measurement waveform****Figure 5. MC100ES8223 AC reference measurement waveform**

APPLICATIONS INFORMATION

Using the thermally enhanced package of the MC100ES8223

The MC100ES8223 uses a thermally enhanced exposed pad (EP) 64 lead LQFP package. The package is molded so that the leadframe is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance that supports the power consumption of the MC100ES8223 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100ES8223. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is the absolute minimum requirement for MC100ES8223 applications on multi-layer boards. The recommended thermal land design comprises a 5 x 5 thermal via array as shown in Figure 6 "Recommended thermal land pattern", providing an efficient heat removal path.

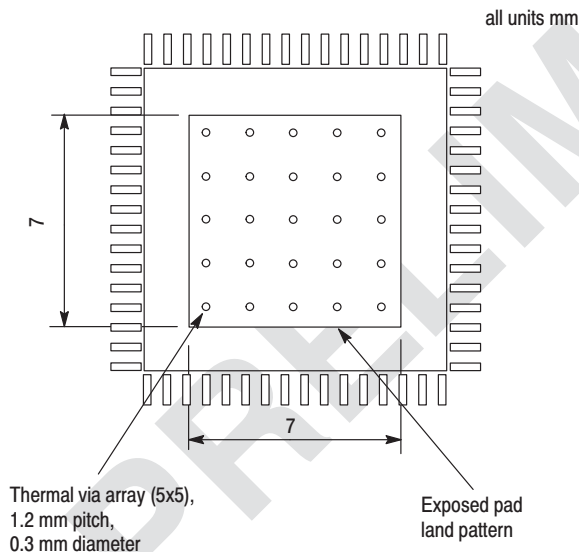


Figure 6. Recommended thermal land pattern

The via diameter is should be approx. 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. Figure 7 "Recommended solder mask openings" shows a recommend solder mask opening with respect to the recommended 5 x 5 thermal via

array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as shown in Figure 7. For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

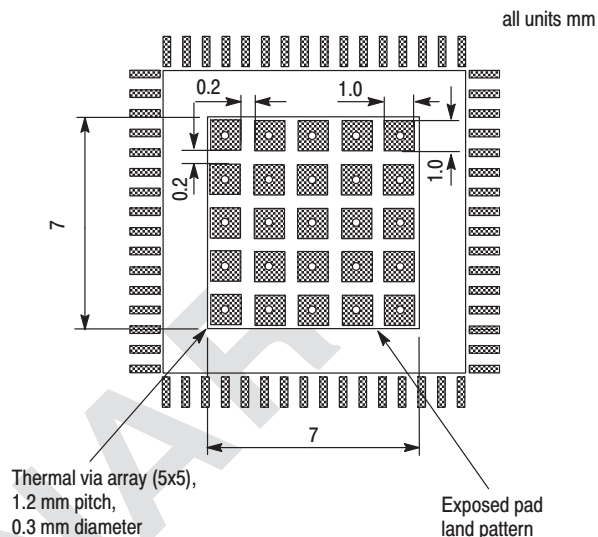


Figure 7. Recommended solder mask openings

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided. For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

Table 7. Thermal Resistance^a

Convection-LFPM	R_{THJA}^b °C/W	R_{THJA}^c °C/W	R_{THJC}^d °C/W	R_{THJB}^e °C/W
Natural	57.1	24.9	15.8	9.7
100	50.0	21.3		
200	46.9	20.0		
400	43.4	18.7		
800	38.6	16.9		

- Thermal data pattern with a 3 x 3 thermal via array on 2S2P boards (based on empirical results)
- Junction to ambient, single layer test board, per JESD51-6
- Junction to ambient, four conductor layer test board (2S2P), per JES51-6
- Junction to case, per MIL-SPEC 883E, method 1012.1
- Junction to board, four conductor layer test board (2S2P) per JESD 51-8

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100ES8223 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.

Chapter Eight

Packaging Information

The packaging information for each device type can be determined in one of two ways: by the specific case number indicated on the individual data sheet (for example, the case number for MPC9600/D is 932), or by using the *Case Dimension Cross-Reference Tables* provided at the beginning of this chapter. Case dimension information is presented in numerical order; by case number.

Case Dimension Cross-Reference Tables

Table 1. Clock Generators

Device	Package	Case Number	Page
MPC9315	32 LQFP	873A	761
MPC9330	32 LQFP	873A	761
MPC9331	32 LQFP	873A	761
MPC9350	32 LQFP	873A	761
MPC9351	32 LQFP	873A	761
MPC9352	32 LQFP	873A	761
MPC93R51	32 LQFP	873A	761
MPC93R52	32 LQFP	873A	761
MPC9600	48 LQFP	932	762
MPC9772	52 LQFP	848D	760
MPC9773	52 LQFP	848D	760
MPC9774	52 LQFP	848D	760
MPC9850	100 PBGA	1462	768
MPC9893	48 LQFP	932	762
MPC9992	32 LQFP	873A	761
MPC9993	32 LQFP	873A	761
MC88915	28 LQFP	776	758
MC88915T	28 LQFP	776	758
MC88LV915T	28 LQFP	776	758
MC88916	20 SOIC	751D	757
MC88920	20 SOIC	751D	757
MC88LV926	20 SOIC	751D	757

Table 2. Failover or Redundant Clock

Device	Package	Case Number	Page
MPC9892	32 LQFP	873A	761
MPC9893	48 LQFP	932	762
MPC9894	100 PBGA	1462	768
MPC9895	100 PBGA	1462	768
MPC993	32 LQFP	873A	761
MPC9993	32 LQFP	873A	761

Table 3. Clock Synthesizers

Device	Package	Case Number	Page
MPC926508	20 SSOP	1461	767
MPC9229	28 PLCC	776	758
	32 LQFP	873A	761
MPC9230	28 PLCC	776	758
	32 LQFP	873A	761
MPC9239	28 PLCC	776	758
MPC9259	32 LQFP	873A	761

Table 4. Zero-Delay Buffers

Device	Package	Case Number	Page
MPC962305	8 SOIC	751	756
	8 TSSOP	948J	765
MPC962308	16 SOIC	751B	756
	16 TSSOP	948F	764
MPC962309	16 SOIC	751B	756
	16 TSSOP	948F	764
MPC9608	32 LQFP	873A	761
MPC9653	32 LQFP	873A	761
MPC9658	32 LQFP	873A	761
MPC961C	32 LQFP	873A	761
MPC961P	32 LQFP	873A	761

Table 5. LVCMOS Fanout Buffers

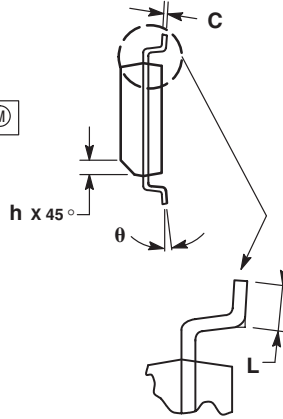
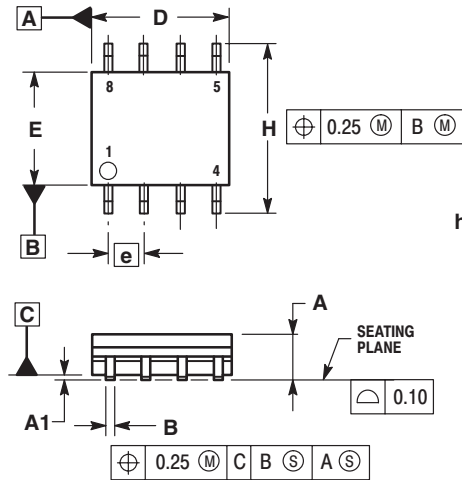
Device	Package	Case Number	Page
MPC905	16 SOIC	751B	756
MPC940L	32 LQFP	873A	761
MPC941	48 LQFP	932	762
MPC942C	32 LQFP	873A	761
MPC942P	32 LQFP	873A	761
MPC9443	48 LQFP	932	762
MPC9446	32 LQFP	873A	761
MPC9447	32 LQFP	873A	761
MPC9448	32 LQFP	873A	761
MPC9449	52 LQFP	848D	760
MPC9456	32 LQFP	873A	761

Table 6. Differential Fanout Buffers

Device	Package	Case Number	Page
MC100ES6011	8 SOIC	751	756
	8 TSSOP	TBD	TBD
MC100ES6014	20 SOIC	751D	757
	20 TSSOP	948E	763
MC100ES6056	20 SOIC	751D	757
	20 TSSOP	948E	763
MC100ES6111	32 LQFP	873A	761
MC100ES6139	20 SOIC	751D	757
	20 TSSOP	948E	763
MC100ES6210	32 LQFP	873A	761
MC100ES6220	52 LQFP-EP	1336A	766
MC100ES6221	52 LQFP-EP	1336A	766
MC100ES6222	52 LQFP-EP	1336A	766
MC100ES6226	32 LQFP	873A	761
MC100ES6254	32 LQFP	873A	761
MC100ES7111	32 LQFP	873A	761
MC100ES8111	32 LQFP	873A	761
MC100ES8223	64 LQFP-EP	840K	759

Case Dimensions

D SUFFIX PLASTIC 8 SOIC PACKAGE CASE 751-06 ISSUE T

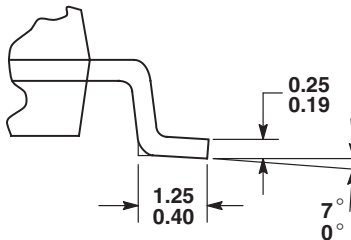
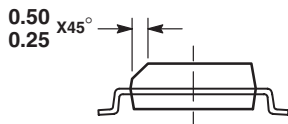
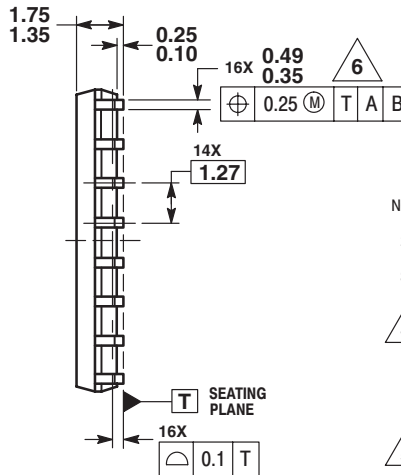
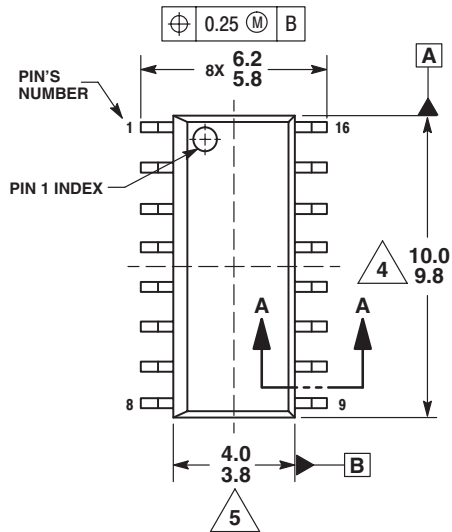


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27	BSC
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

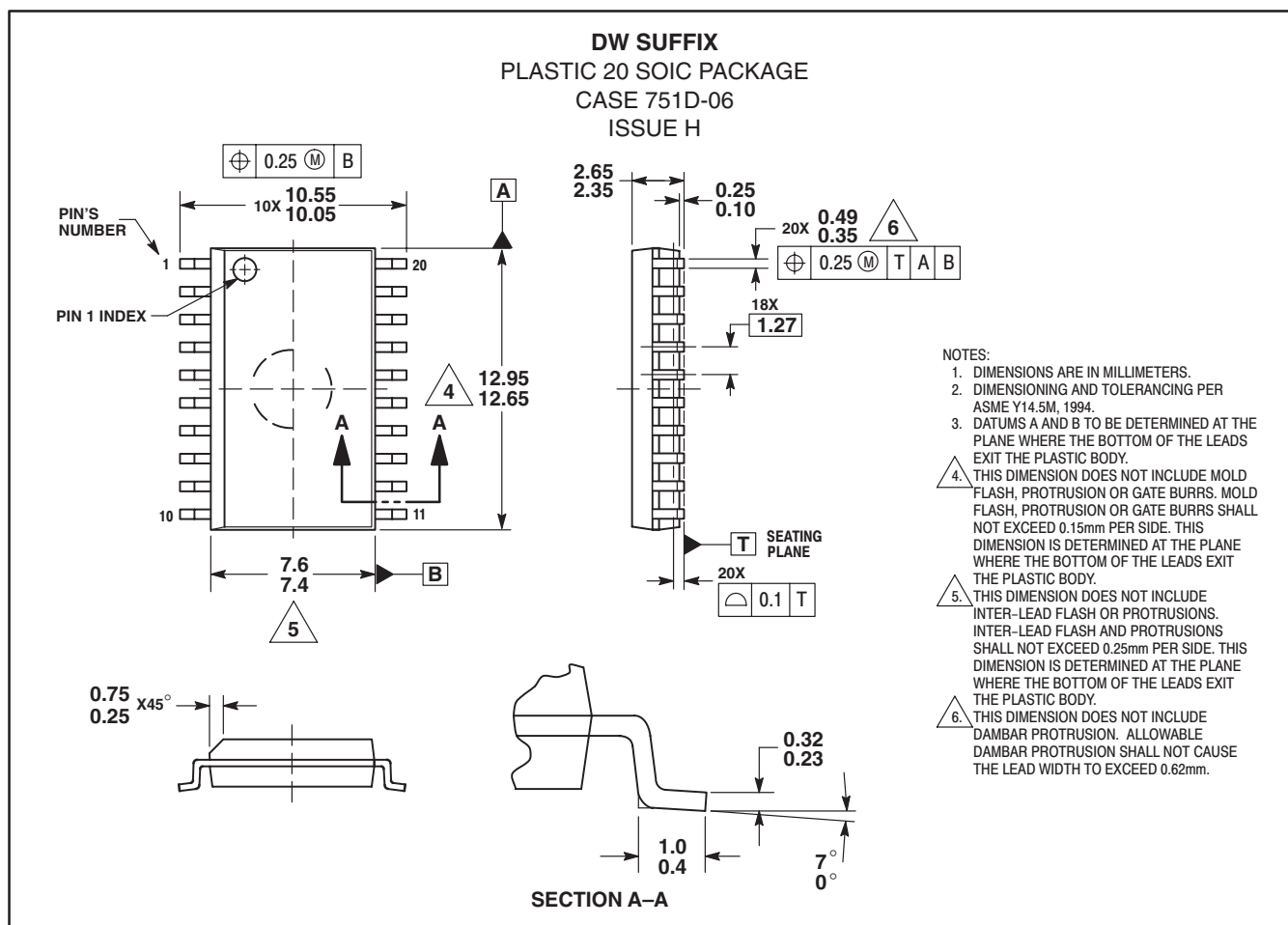
D SUFFIX PLASTIC 16 SOIC PACKAGE CASE 751B-05 ISSUE K



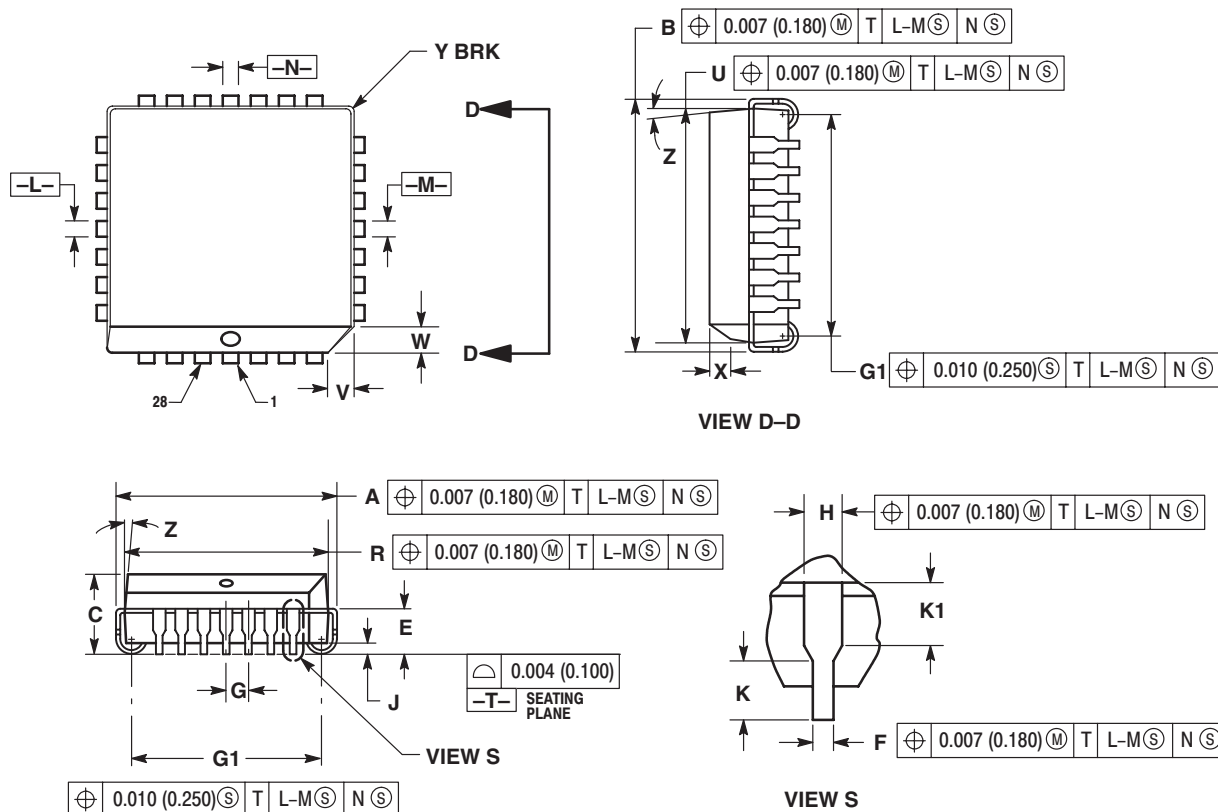
SECTION A-A

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62mm.



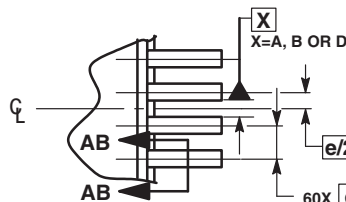
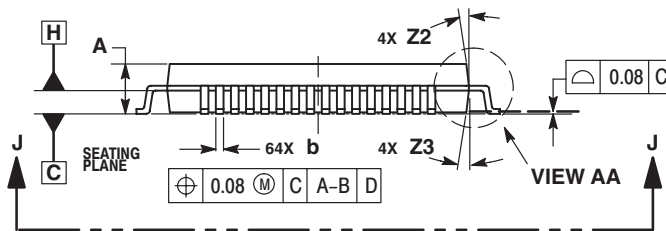
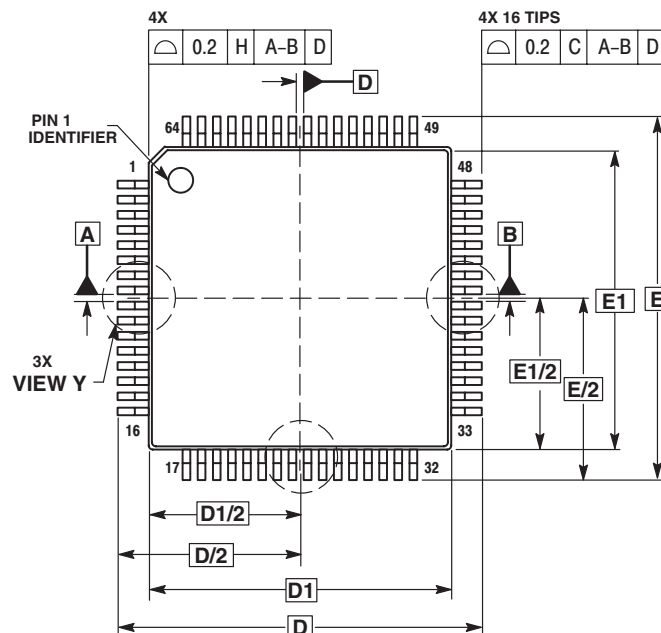
FN SUFFIX
PLASTIC 28 PLCC PACKAGE
CASE 776-02
ISSUE D

**NOTES:**

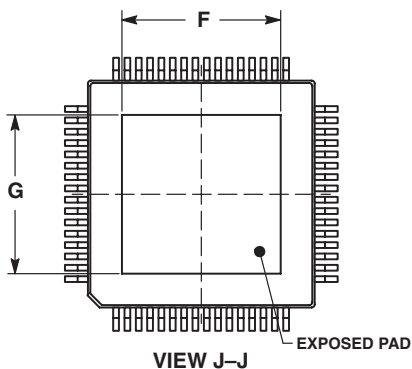
- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

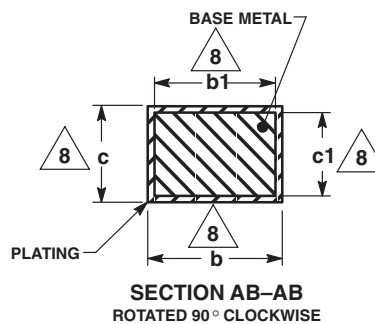
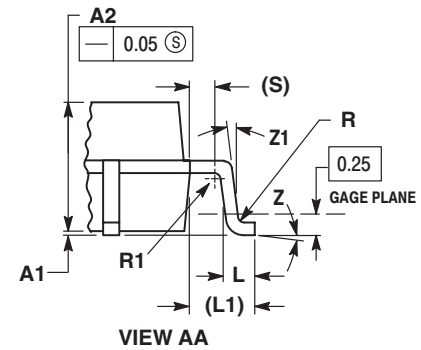
FA SUFFIX
PLASTIC 64 LQFP EXPOSED PAD PACKAGE
CASE 840K-01
ISSUE O



VIEW Y



VIEW J-J

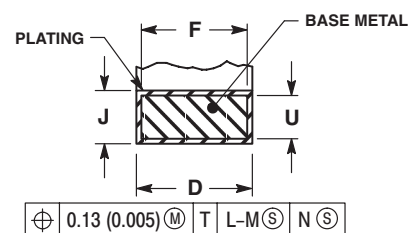
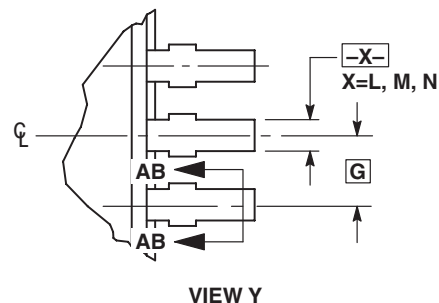
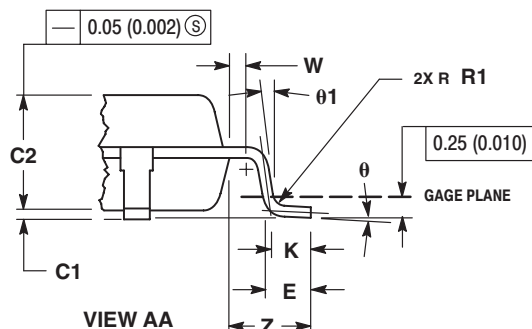
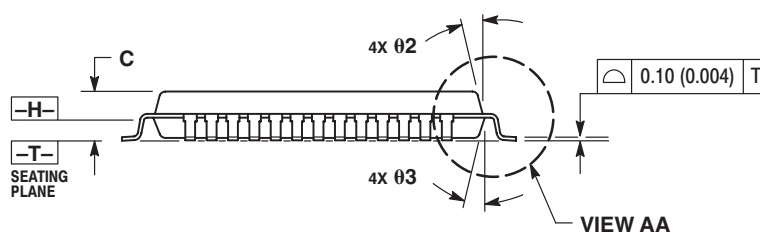
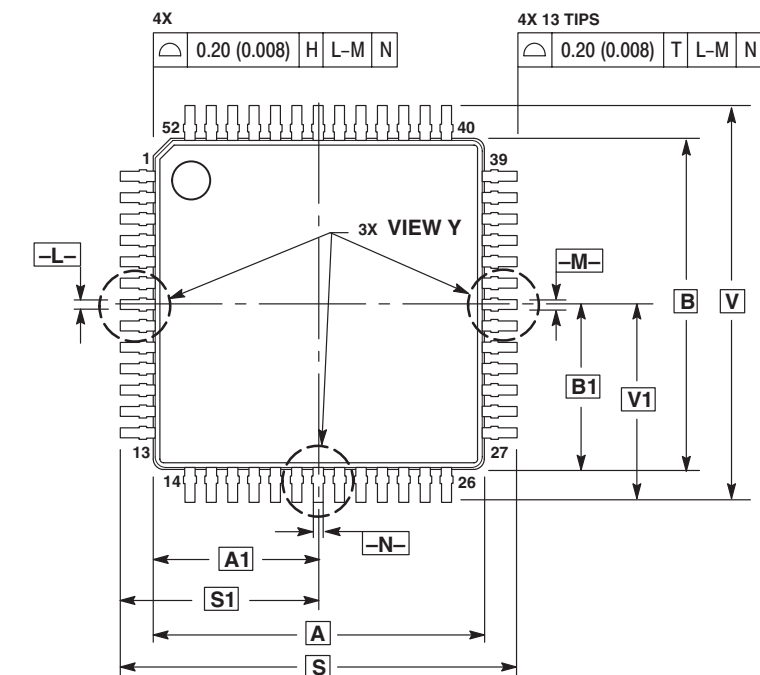
SECTION AB-AB
ROTATED 90° CLOCKWISE

NOTES:

- DIMENSIONS ARE IN MILLIMETERS.
- INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
- DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 mm.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
- EXACT SHAPE OF EACH CORNER IS OPTIONAL.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.

DIM	MILLIMETERS	
	MIN	MAX
A	---	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
D	12.00 BSC	
D1	10.00 BSC	
e	0.50 BSC	
E	12.00 BSC	
E1	10.00 BSC	
L	0.45	0.75
L1	1.00 REF	
R1	0.08	---
R2	0.08	---
S	0.20	---
F	6.00	7.00
G	6.00	7.00
Z	0°	7°
Z1	0°	---
Z2	11°	13°
Z3	11°	13°

FA SUFFIX
PLASTIC 52 LQFP PACKAGE
CASE 848D-03
ISSUE D

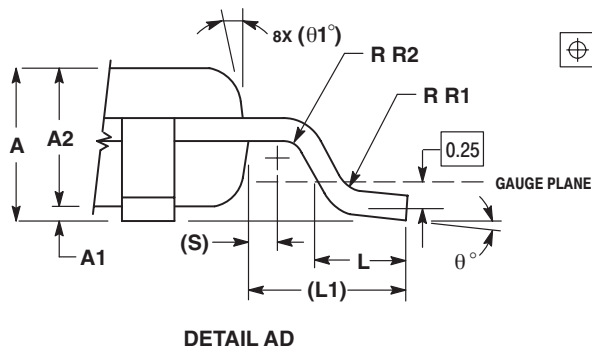
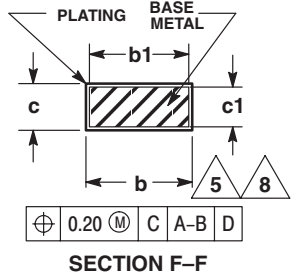
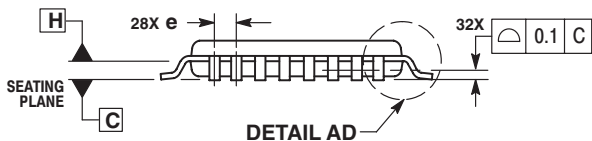
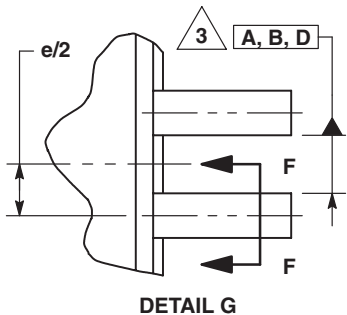
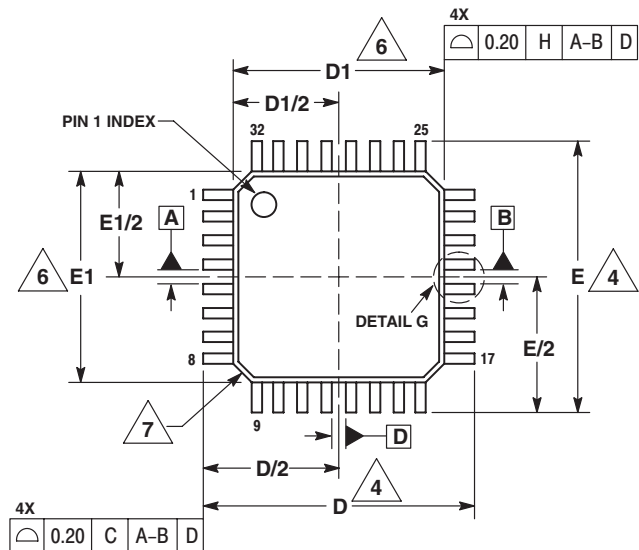


NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION: MILLIMETER.
- 3 DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
- 4 DATUMS -L-, -M- AND -N- TO BE DETERMINED AT DATUM PLANE -H-.
- 5 DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-.
- 6 DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
- 7 DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	---	1.70	---	0.067
C1	0.05	0.20	0.002	0.008
C2	1.30	1.50	0.051	0.059
D	0.20	0.40	0.008	0.016
E	0.45	0.75	0.018	0.030
F	0.22	0.35	0.009	0.014
G	0.65 BSC		0.026 BSC	
J	0.07	0.20	0.003	0.008
K	0.50 REF		0.020 REF	
R1	0.08	0.20	0.003	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
Ø	0°	7°	0°	7°
Ø1	0°	---	0°	---
Ø2	12° REF		12° REF	
Ø3	12° REF		12° REF	

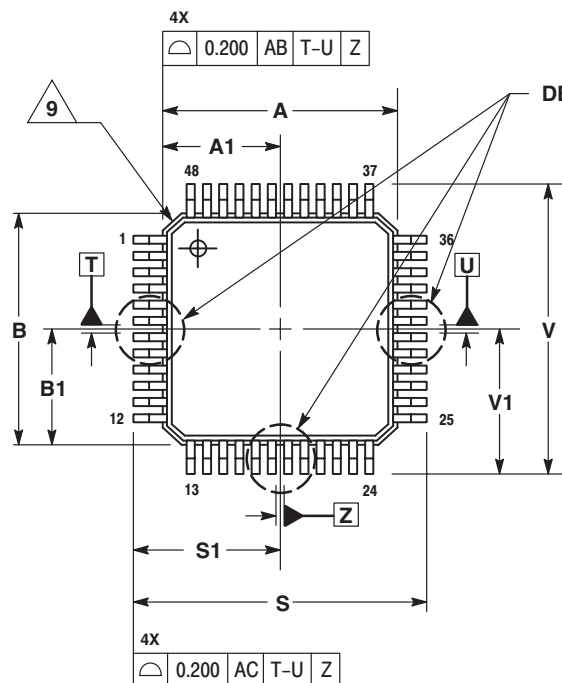
FA SUFFIX
PLASTIC 32 LQFP PACKAGE
CASE 873A-03
ISSUE B



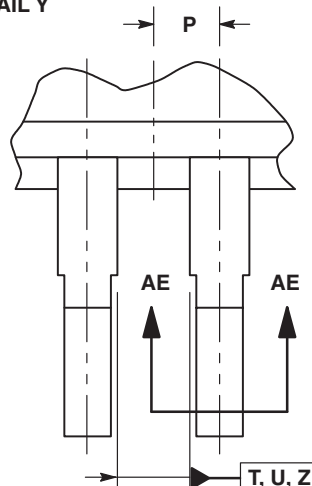
- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
 4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
 5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08-mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07-mm.
 6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25-mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
 7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
 8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1-mm AND 0.25-mm FROM THE LEAD TIP.

DIM	MILLIMETERS	
	MIN	MAX
A	1.40	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.30	0.45
b1	0.30	0.40
c	0.09	0.20
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
e	0.80 BSC	
E	9.00 BSC	
E1	7.00 BSC	
L	0.50	0.70
L1	1.00 REF	
θ	0°	7°
θ1	12° REF	
R1	0.08	0.20
R2	0.08	---
S	0.20 REF	

FA SUFFIX
PLASTIC 48 LQFP PACKAGE
CASE 932-03
ISSUE F



DETAIL Y

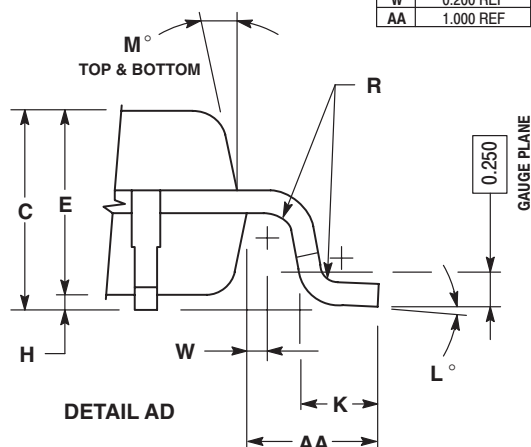
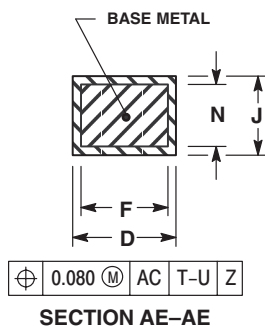
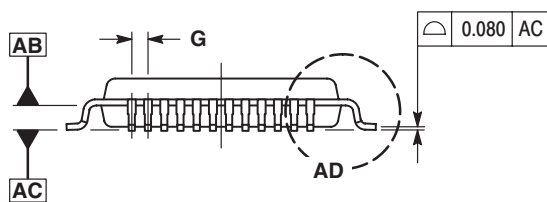


DETAIL Y

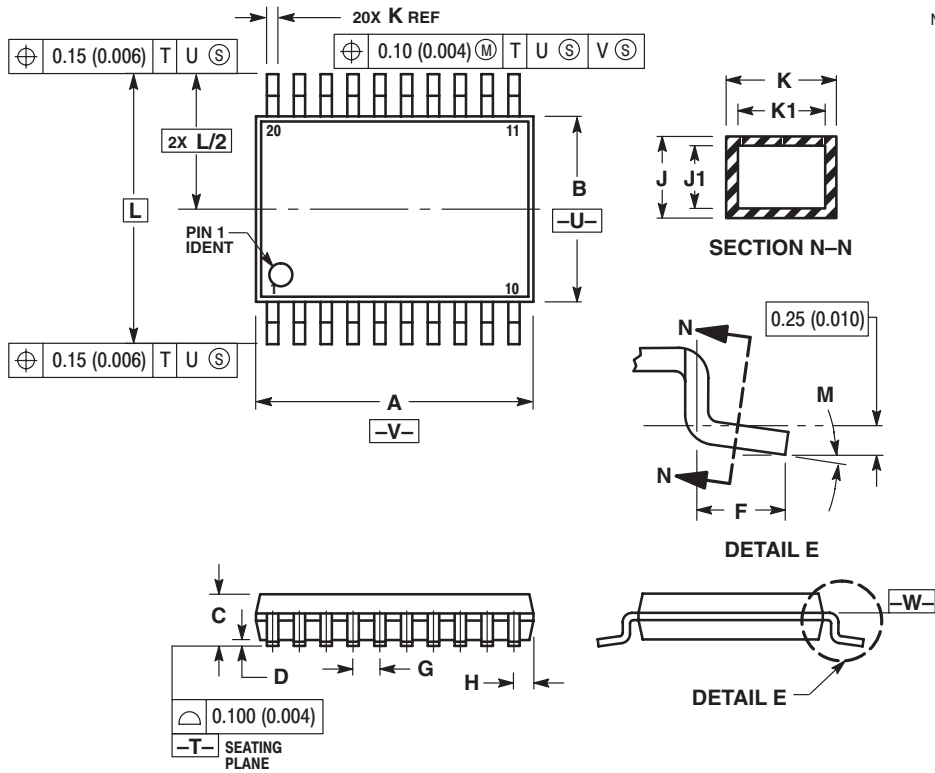
NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2 CONTROLLING DIMENSION: MILLIMETER.
- 3 DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
- 4 DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
- 5 DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
- 6 DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
- 7 DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
- 8 MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
- 9 EXACT SHAPE OF EACH CORNER IS OPTIONAL.

MILLIMETERS		
DIM	MIN	MAX
A	7.000 BSC	
A1	3.500 BSC	
B	7.000 BSC	
B1	3.500 BSC	
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	0°	7°
M	12° REF	
N	0.090	0.160
P	0.250 BSC	
R	0.150	0.250
S	9.000 BSC	
S1	4.500 BSC	
V	9.000 BSC	
V1	4.500 BSC	
W	0.200 REF	
AA	1.000 REF	



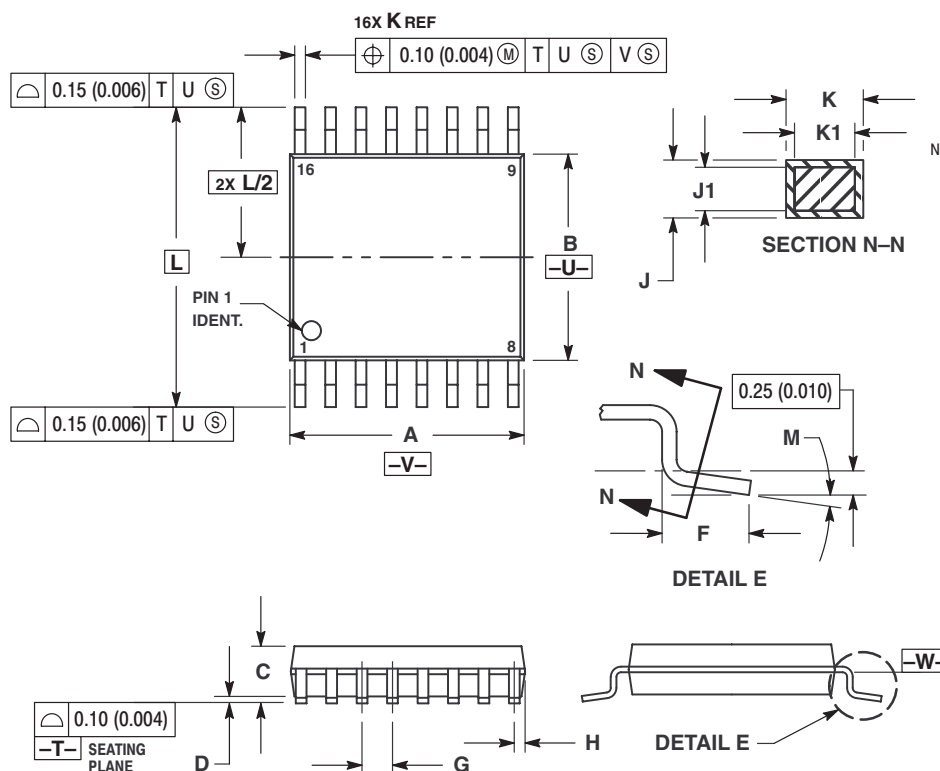
DT SUFFIX
PLASTIC 20 TSSOP PACKAGE
CASE 948E-02
ISSUE A



- NOTES:
- 1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - 2 CONTROLLING DIMENSION: MILLIMETER.
 - 3 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 - 4 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 - 5 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 - 6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 - 7 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC	0.026 BSC		
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC	0.252 BSC		
M	0°	8°	0°	8°

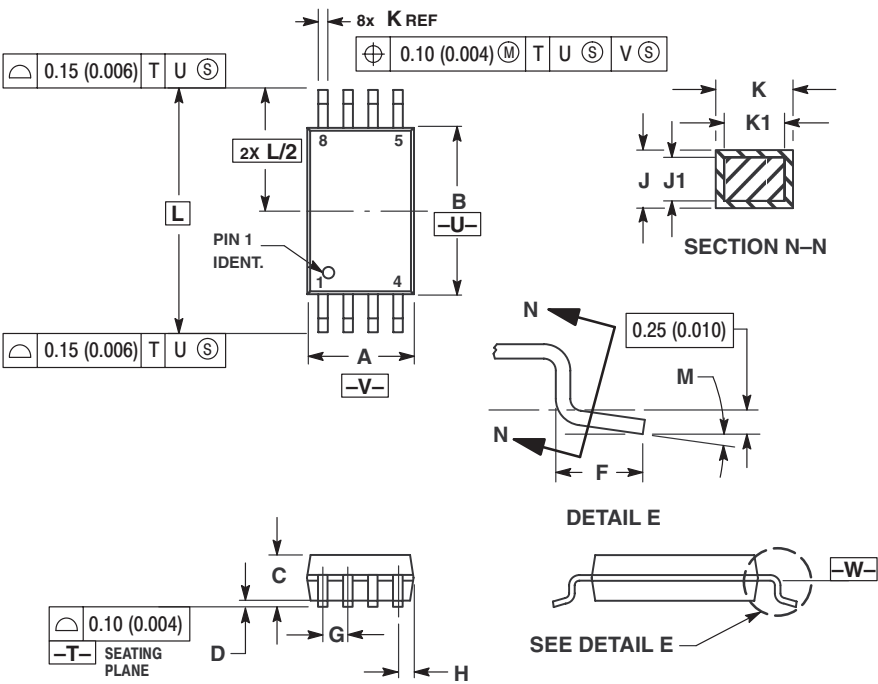
DT SUFFIX
PLASTIC 16 TSSOP PACKAGE
CASE 948F-01
ISSUE O



- NOTES:
- 1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - 2 CONTROLLING DIMENSION: MILLIMETER.
 - 3 DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 - 4 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 - 5 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 - 6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 - 7 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

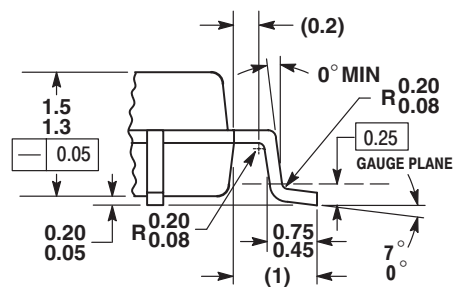
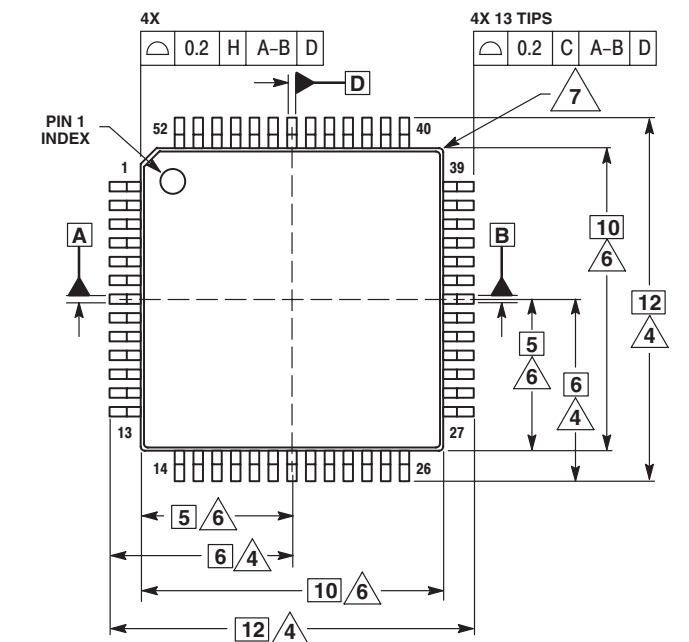
DT SUFFIX
PLASTIC 8 TSSOP PACKAGE
CASE 948J-01
ISSUE O



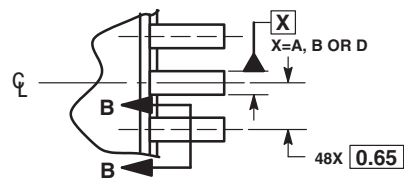
- NOTES:
- 1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - 2 CONTROLLING DIMENSION: MILLIMETER.
 - 3 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 - 4 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 - 5 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 - 6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 - 7 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

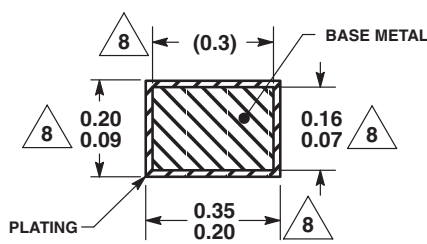
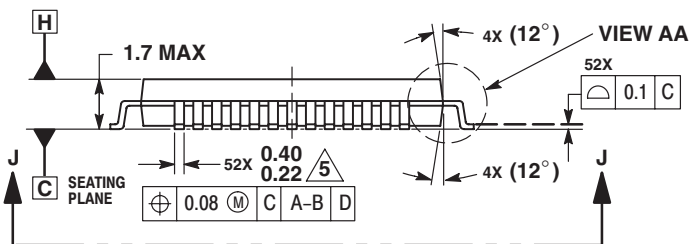
FA SUFFIX
PLASTIC 52 LQFP EXPOSED PAD PACKAGE
CASE 1336A-01
ISSUE O



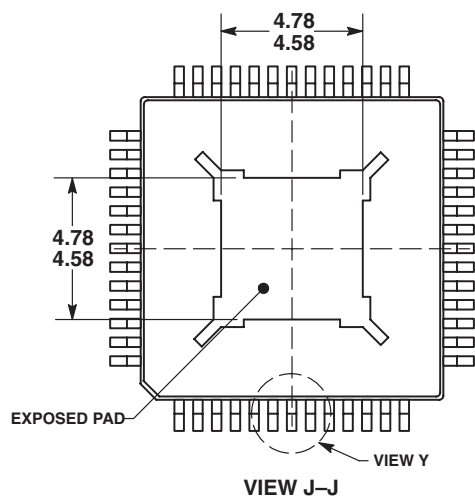
VIEW AA



VIEW Y



SECTION B-B

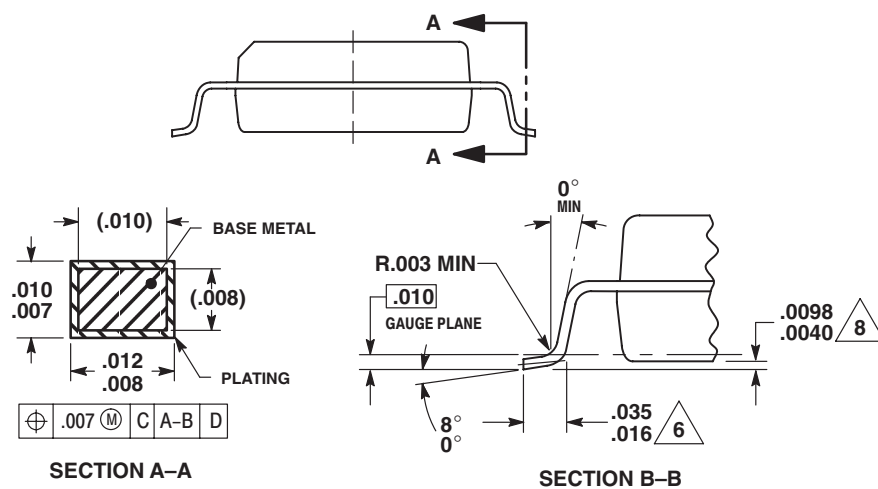
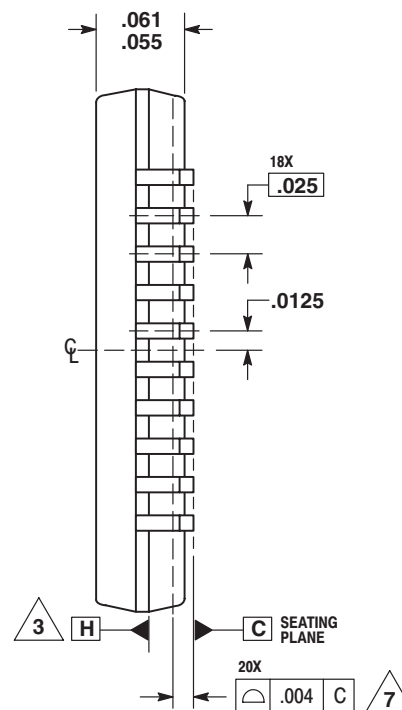


- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
 3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
 4. DIMENSION TO BE DETERMINED AT SEATING PLANE C.
 5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
 6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
 7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
 8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.

Technical drawing of a 2X 10 TIPS part. The drawing shows a rectangular component with two rows of ten tips each. Key features and dimensions include:

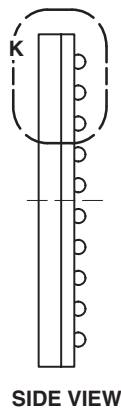
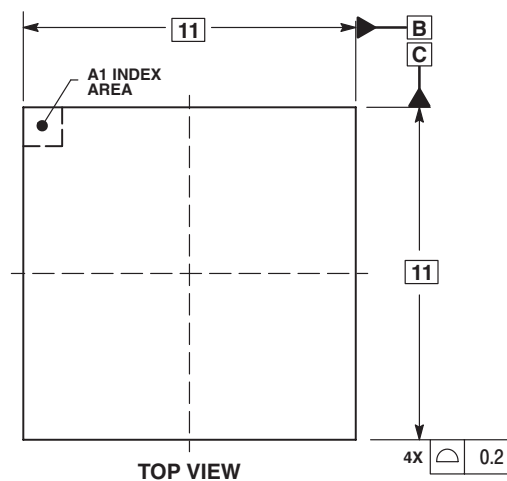
- Dimensions:**
 - Overall width: .236
 - Distance from left edge to centerline: .157
 - Distance from centerline to right edge: .150
 - Overall height: .344
 - Distance from bottom edge to centerline: .337
 - Tip width: .118
- Feature Callouts:**
 - PIN 1 ID:** Indicated by an arrow pointing to the top-left corner.
 - Feature 4:** Four triangular features are shown, labeled with a triangle containing '4'. Two are on the left side (near pins 1 and 10) and two are on the right side (near pins 20 and 11).
 - Feature B:** Two rectangular features are shown on the left side, labeled with a rectangle containing 'B'.
 - Feature A:** One rectangular feature is shown on the right side, labeled with a rectangle containing 'A'.
- Part Identification:**
 - 2X 10 TIPS:** Located at the bottom left.
 - Table:**

△	.003	H	A-B	D



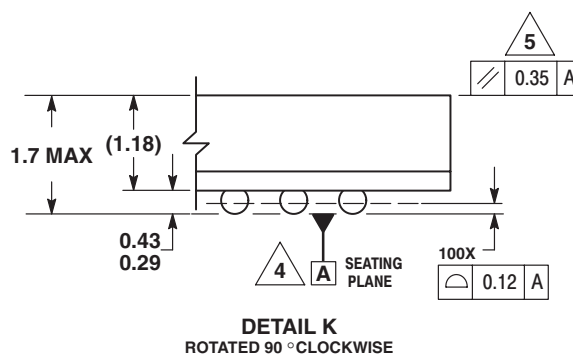
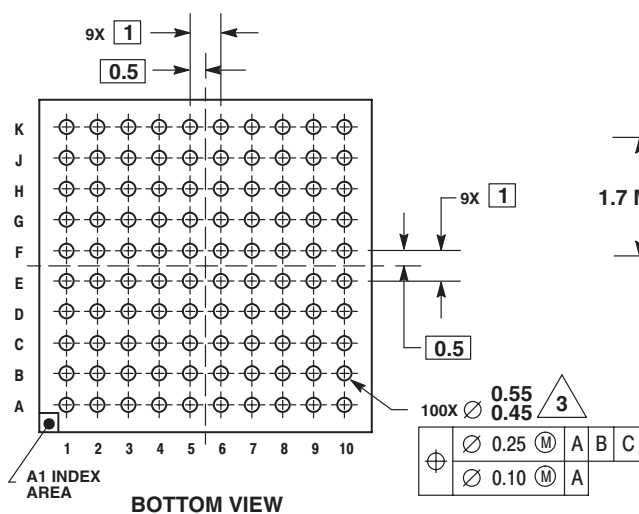
- NOTES:
1. DIMENSIONS ARE IN INCHES.
 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 3. DATUM PLANE H LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
 4. DATUM A, B AND D TO BE DETERMINED WHERE CENTERLINE BETWEEN LEADS EXITS PLASTIC BODY AT DATUM PLANE H.
 5. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES FOR ENDS AND .008 INCHES FOR SIDES.
 6. THIS DIMENSION IS LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
 7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004 INCHES AT SEATING PLANE.
 8. THIS DIMENSION IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

VF SUFFIX
100 MAP PBGA PACKAGE
CASE 1462-01
ISSUE O



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGING



Chapter Nine

Application Notes

Application Notes	
Document Number	Page
AN1091/D	770
AN1405/D	777
AN1406/D	783
AN1545/D	790
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AN1091

Low Skew Clock Drivers and Their System Design Considerations

ABSTRACT

This application note addresses various system design issues to help ensure that Motorola's low skew clock drivers are used effectively in a system environment.

Several varieties of clock drivers with 1 ns or less skew from output-to-output are available from Motorola. Microprocessor-based systems are now running at 33 MHz and beyond, and system clock distribution at these frequencies mandate the use of low skew clock drivers. Unfortunately, just plugging a high performance clock driver into a system does not guarantee trouble free operation. Only careful board layout and consideration of system noise issues can guarantee reliable clock distribution. This application note addresses these system design issues to help ensure that Motorola's low skew clock drivers are used effectively in a system environment.

INTRODUCTION

With frequencies regularly reaching 33 MHz and approaching 40-50 MHz in today's CISC and RISC microprocessor systems, well controlled and precise clock signals are required to maintain a synchronous system. Many microprocessors also require input clock duty cycles very close to 50%. These stringent timing requirements mandate the use of specially designed, low skew clock distribution circuits or 'clock drivers.' However, just plugging one of these parts into your board does not ensure a trouble free system. Careful system and board design techniques must be used in conjunction with a low skew clock driver to meet system timing requirements and provide clean clock signals.

Why are Low Skew Clock Drivers Necessary

An MPU system designer wants to utilize as much of a clock cycle as possible without adding unnecessary timing guard-bands. Propagation delays of peripheral logic do not scale with frequency. Therefore, as the clock period decreases, the system designer has less time but the same logic delays to accomplish the function. How can he get more time? A viable option is to use a special clock source that minimizes clock 'uncertainty.'

A simple example illustrates this concept. At 33 MHz, $T_{\text{cycle}} = 30$ ns. An FCT240A, for example, has a High-Low uncertainty of the min/max spread of t_{PLH} to t_{PHL} of approximately 3.3 ns. If 1.7 ns of pin-to-pin skew due to the actual part and PCB trace delays is also considered, then only 25 ns of the clock period is still available. The worst case t_p of clock-to-data valid on the 88200 M-Bus is 12 ns, which leaves only 13 ns to accomplish additional functions. In this case 17% of a cycle is required for clock distribution or clock 'uncertainty,' which is an unacceptable penalty from a system designer's point of view. At 50 MHz this penalty becomes 25%. A maximum of 10% of the period allotted for clock distribution is an acceptable standard.

If multiple levels of clock distribution (one clock driver's output feeding the inputs of several other clock drivers) are necessary due to large clock fan-outs, the additional part-to-part skew variations add even more to the clock uncertainty. Standard logic has always been specified with a large (and conservative) delta between the minimum and maximum propagation delays. This delta creates the excessive amount of clock 'uncertainty' which the system designer has been forced to design into his system, even though it is not realistic. When system frequencies were below 16 MHz this large clock penalty could be tolerated, but as the above example points out, not anymore. A clock driver's specs guarantee this min/max delta to be a specific, small value. To reduce the clock overhead to manageable levels, a clock driver with minimal variation (<5%) from a 50% duty cycle and guaranteed low output-to-output and part-to-part skew must be used.

DEFINITIONS

A typical clock driver has a single input which is usually driven by a crystal oscillator. The clock driver can have any number of outputs which have a certain frequency relationship to the clock input. Clock driver skew is typically defined by three different specs. These specs are graphically illustrated in Figure 1.

The first spec, t_{OS} , measures the difference between the fastest and slowest propagation delays (any transition) between the outputs of a single part. This number must be 1 ns or less for high-end systems.

The second, t_{PS} , measures the difference between the high-to-low and low-to-high transition for a single output (pin). This spec defines how close to a 50% duty cycle the outputs of the clock driver will be. For example, if this spec is 1 ns (± 0.5 ns), at 33 MHz the output duty cycle is 50% $\pm 3.5\%$. A clock driver which only buffers the crystal input, creating a 1:1 input to output frequency relationship, can be a problem if a very tight tolerance to a 50% duty cycle is required. In this situation the output duty cycle is directly dependent on the input duty cycle, which is not well controlled in most crystal oscillators. The clock driver's outputs switching at half the input frequency ($\div 2$) is a common relationship, which means that the outputs switch on only one edge of the oscillator, eliminating the output's dependence on the duty cycle of the input (crystal oscillator frequency is very stable).

The third spec, t_{PV} , measures the maximum propagation delay delta between any given pin on any part. This spec defines the part to part variation between any clock driver (of the same device type) which is ever shipped. This number reflects the process variation inherent in any technology. For CMOS, this spec is usually 3 ns or less. High performance ECL technologies can bring this number down into the 1-2 ns range. Another way to minimize the part-to-part variation is to use a phase-locked loop clock driver, which are just now becoming available.

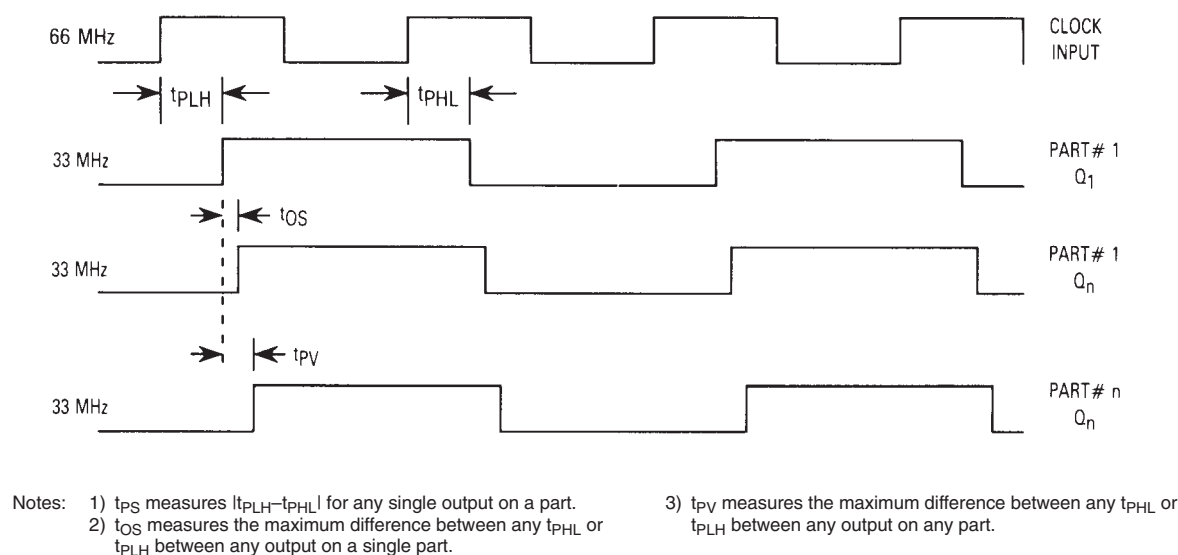


Figure 1. Timing Diagram Depicting Clock Skew Specs Within One Part and Between Any Two Parts

An important consideration when designing a clock driver into a system is that the skew specs described above are usually specified at a fixed, lumped capacitive load. In a real system environment the clock lines usually have various loads distributed over several inches of PCB trace which can contribute additional delay and sometimes act like transmission lines, so the system designer must use careful board layout techniques to minimize the total system skew. In other words, just plugging a low skew clock driver into a board will not solve all your timing problems.

DESIGN CONSIDERATIONS

Figure 2 is a scale replication of a section of an actual 88000 RISC system board layout. The section shown in Figure 2 includes the MC88100 MPU and the MC88200 CMMU devices and the MC88914 CMOS clock driver. The only PCB traces shown are the clock output traces from the MC88914 to the various loads. For this clock driver the output-to-output skew (t_{OS}) is guaranteed to be less than 1 ns at any given temperature, supply voltage, and fixed load up to 50 pF.

In calculating the total system skew, the difference in clock PCB trace length and loading must be taken into account. For an unloaded PCB trace, the signal delay per unit length, t_{PD} , is dependent only on the dielectric constant, ϵ_r , of the board material. The characteristic impedance, Z_O , of the line is dependent upon ϵ_r and the geometry of the trace. These relationships are depicted in Figure 3 for a microstrip line.¹ The formulas for t_{PD} and Z_O are slightly different for other types of strip lines, but for simplicity's sake all calculations in this article will assume a microstrip line.

The equations in Figure 3 are valid only for an unloaded trace; loading down a line will increase its delay and lower its impedance. The signal propagation delay (t_{PD}') and characteristic impedance (Z_O') due to a loaded trace are calculated by the following formulas:

$$t_{PD}' = t_{PD} \sqrt{1 + \frac{C_d}{C_O}}$$

$$Z_O' = \frac{Z_O}{\sqrt{1 + \frac{C_d}{C_O}}}$$

C_d is the distributed load capacitance per unit length, which is the total input capacitance of the receiving devices divided by the length of the trace. C_O is the intrinsic capacitance of the trace, which is defined as:

$$C_O = \frac{t_{PD}}{Z_O}$$

Assuming typical microstrip dimensions and characteristics as $w = 0.01$ in, $t = 0.002$ in, $h = 0.012$ in, and $\epsilon_r = 4.7$, the equations of Figure 3 yield $Z_O = 69.4 \Omega$ and $t_{PD} = 0.144$ ns/in. C_O is then calculated as 2.075 pF/in. If it is assumed that an MC88100 or 88200 clock input load is 15 pF, and that two of these loads, in addition to a 7 pF FAST TTL load, are distributed along a 9.6 in clock trace,

$$C_d = (2 \times 15 + 7) \text{ pF} / 9.6 \text{ in} = \text{pF/in.}$$

The loaded trace propagation delay and characteristic impedance are then calculated as

$$t_{PD}' = 0.243 \text{ ns/in and } Z_O' = 41 \Omega.$$

Looking at trace C in Figure 2, the two MC88200's are approximately 3 inches apart. Using the calculated value of t_{PD}' , the clock signal skew due to the trace is about 0.7 ns. Since these two devices are on the same trace, this is the total clock skew between these devices. Upon careful inspection of all the clock traces, it can be seen that clock signal skew was

accounted for and minimized on this board layout. The longest distance between any 88 K devices on a single clock trace is about 4.5 inches, which translates to approximately 1.1 ns of skew. The two 88 K devices farthest away from the clock driver (traces a and c), are located at almost exactly the same distance along their respective traces, making the clock skew between them the 1ns guaranteed from output to output of the clock

driver. This means that the worst case clock skew between any two devices on this board is approximately 2.1 ns, which at 33 MHz is 7% of the period. Without careful attention to matching the clock traces on the board, this number could easily exceed 3 ns and the 10% cut-off point, even if a low skew clock driver is used.

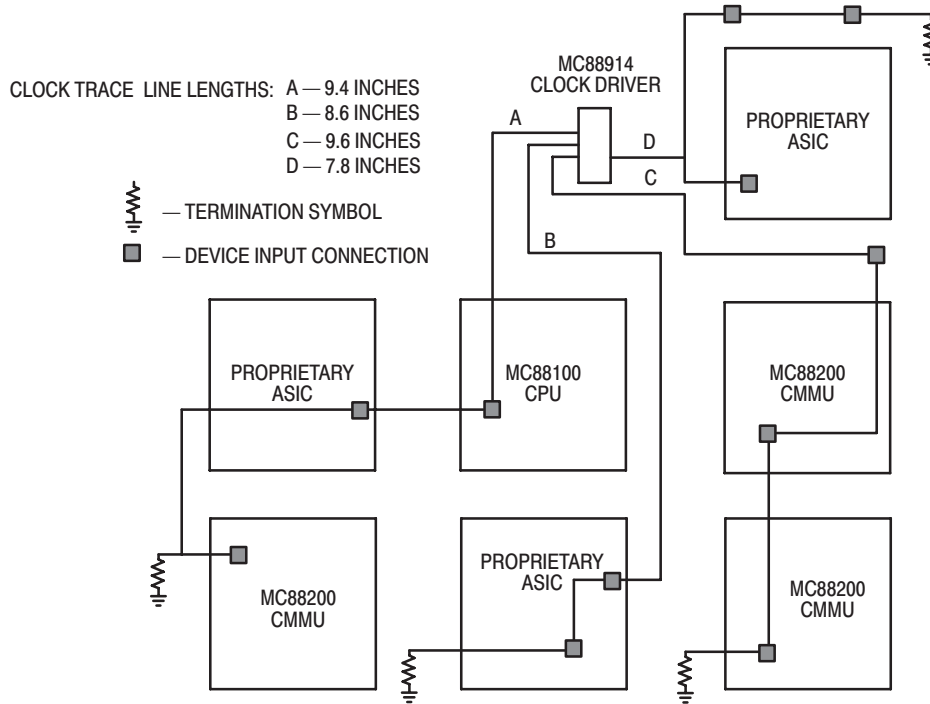
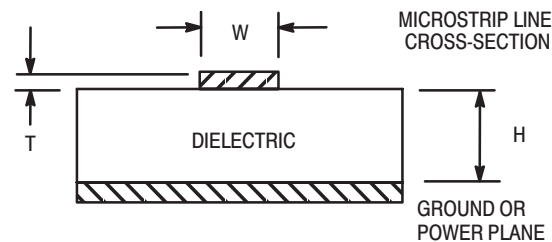


Figure 2. Scale Representation of an Actual 88000 System PCB Layout
(Only sections of the board related to the clock driver outputs are shown.)



WHERE:

e_r = Relative Dielectric Constant of the Board Material
w, h, t = Dimensions Indicated in a Microstrip Diagram

Figure 3. Formulas for the Characteristic Impedance and Propagation Delay of a Microstrip Line (Ref 1)

CLOCK SIGNAL TERMINATIONS

Transmission line effects occur when a large mismatch is present between the characteristic impedance of the line and the input or output impedances of the receiving or driving device. The basic guidelines used to determine if a PCB trace needs to be examined for transmission line effects is that if the smaller of the driving device's rise or fall time is less than three times the propagation delay of a switching wave through a trace, the transmission line effects will be present.² This relationship can be stated in equation form as:³

$$3 \times t_{PD} \times \text{trace length} \leq t_{RISE} \text{ or } t_{FALL}$$

For the MC88914 CMOS clock driver described in this article, rise and fall times are typically 1.5 ns or less (from 20% to 80% of V_{CC}). Analyzing the clock trace characteristics presented earlier for transmission line effects, $3 \times 0.243 \text{ ns/in} \times \text{trace length} \leq 1 \text{ ns}$ (1 ns is used as 'fastest' rise or fall time). Therefore the trace length must be less than 1.5 inches for the transmission line effects to be masked by the rise and fall times.

Figure 4 shows the clock signal waveform seen at the receiver end of an unterminated 0.5 inch trace and an unterminated 9 inch trace. These results were obtained using SPICE simulations, which may not be exact, but are adequate to predict trends and for comparison purposes. The 9 inch trace, which is well beyond the 1.5 inch limit where transmission line effects come into play, exhibits unacceptable switching characteristics caused by reflections going back and forth on the trace. Even the 0.5 inch line exhibits substantial overshoot and undershoot. Any unterminated line will exhibit some overshoot and undershoot at these edge rates.

Clock lines shorter than 1-1.5 inches are unrealistic on a practical board layout, therefore it is recommended that CMOS clock lines be terminated if the driver has 1-2 ns edge rates. Termination, which is used to more closely match the line to the load or source impedances, has been a fact of life in the ECL world for many years (reference 1 is an excellent source for transmission line theory and practice in ECL systems), but CMOS and TTL devices have only recently reached the speeds and edge rates which require termination. CMOS outputs further complicate the issue by driving from rail to rail (5 V), with slew rates exceeding those of high performance ECL devices.

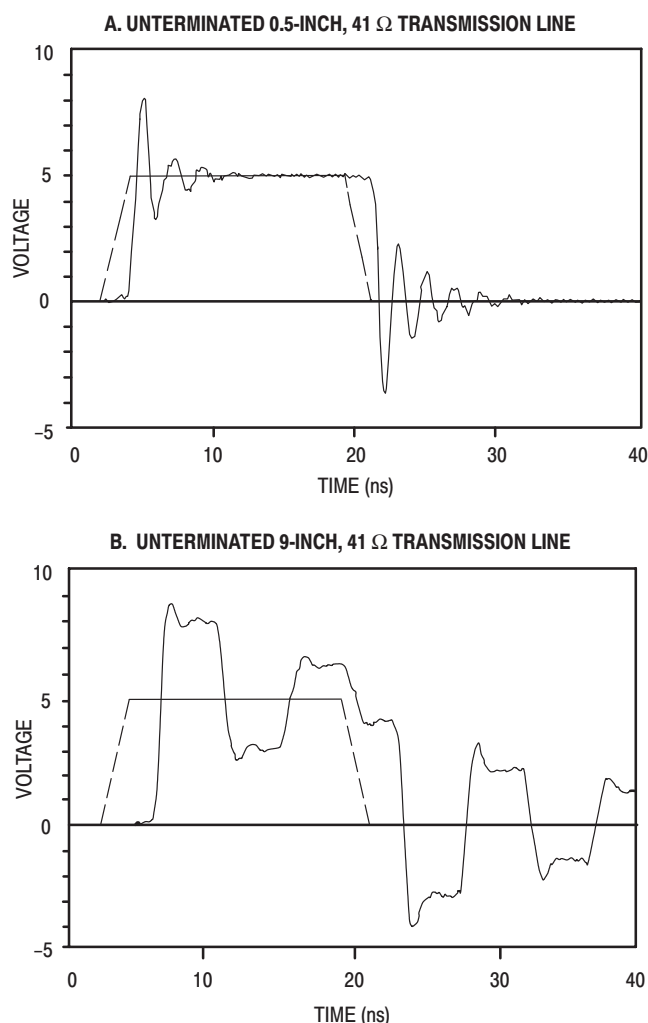


Figure 4. SPICE Simulation Results of 'Short' and 'Long' Transmission Lines. Simulations Were Run with Typical Parameters @ 25°C and $V_{CC} = 5.0 \text{ V}$

Since clock lines are only driven from a single location, they lend themselves to termination more easily than bus lines which are commonly driven from multiple locations. Termination of bus lines with multiple drivers is a complicated manner which will not be addressed in this article. The most common types of termination in digital systems are shown in Figure 5. Since no single termination scheme is optimal in all cases, the tradeoffs involving the use of each will be discussed, and recommendations specific to clock drivers will be made. Reference 2 is a comprehensive and practical treatment of transmission line theory and analysis of CMOS signals, and is recommended reading for those who want to gain a better understanding of transmission lines. Figure 6 shows SPICE simulated waveforms of the different termination schemes to be discussed. The driving device in the simulations was the MC88914 output buffer; in all simulations it drove a 9 inch 41 Ω transmission line. The simulations were run using typical model parameters at 25°C and $V_{CC} = 5 \text{ V}$.

Series termination, depicted in Figure 5b, is recommended if the load is lumped at the end of the trace and the output impedance of the driving device is less than the loaded characteristic impedance of the trace, or when a minimum number of components is required. The main problem with

series termination occurs when the driving device has different output impedance values in the low and high states, which is a problem in TTL and some CMOS devices. A well designed CMOS clock driver should have nearly equal output impedances in the high and low states, avoiding this problem. An additional advantage is that series termination does not create a DC current path, thus the V_{OL} and V_{OH} levels are not degraded. The SPICE generated waveforms of series termination in Figure 6a show that series termination effectively masks the transmission line effects exhibited in Figure 4. If each clock output is driving only one device, series termination would be recommended, but this is not a realistic case in most systems, so series termination is not generally recommended for termination of clock lines.

Parallel termination utilizes a single resistor tied to ground or V_{CC} whose value is equal to the characteristic impedance of the line. Its major disadvantage is the DC current path it creates when the driver is in the high state (if the resistor is tied to ground). This causes excessive power dissipation and V_{OH} level degradation. Since a clock driver output is always switching, the DC current draw argument loses some credibility at higher frequencies because the AC switching current becomes a major component of the overall current. Therefore the main consideration in parallel termination is how much V_{OH} degradation can be tolerated by the receiving devices. Figure 6b demonstrates that this termination technique is effective in minimizing the switching noise, but Thevenin termination has some advantages over parallel termination.

Thevenin termination utilizes one resistor tied to ground and a second tied to V_{CC} . An important consideration when using this type of termination is choosing the resistor values to avoid settling of the voltage between the high and low logic levels of the receiving device.² TTL designers commonly use a 220/330 resistor value ratio, but CMOS is a little tricky because the switch point is at $V_{CC}/2$. With a 1:1 resistor ratio a failure at the driver output would cause the line to settle at 2.5 V, causing system debug problems and also potential damage to the receiving devices.

In Thevenin termination, the parallel equivalent value of the two resistors should be equal to the characteristic impedance of the line. A DC path does exist in both the high and low states, but it is not as bad as parallel termination because the resistance in the Thevenin DC path is at least 2 times greater.

Figure 6c shows the termination waveforms, which exhibit characteristics similar to parallel termination, but with less V_{OH} degradation. The only real advantage of parallel over Thevenin is less resistors (1/2 as many) and less space taken up on the board by the resistors. If this is not a factor, Thevenin termination is recommended over parallel.

AC termination, shown in Figure 5e, normally utilizes a resistor and capacitor in series to ground. The capacitor blocks DC current flow, but allows the AC signal to flow to ground

during switching. The RC time constant of the resistor and capacitor must be greater than twice the loaded line delay. AC termination is recommended because of its low power dissipation and also because of the availability of the resistor and capacitor in single-in-line packages (SIP). A pullup resistor to V_{CC} is sometimes added to set the DC level at a certain point because of the failure condition described in regards to Thevenin termination. As discussed earlier, the argument of lower DC current is less convincing at high frequencies. The AC terminated waveform walks out slightly toward the end of a high-to-low or low-to-high transition as seen in Figure 6d, making it slightly less desirable than Thevenin termination.

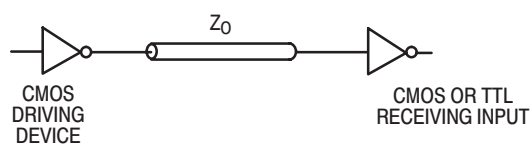
Thevenin and AC termination are the two recommended termination schemes for clock lines, but it depends on what frequency the clock is running at when making a decision between these types of termination. Although hard data is not provided to back this statement up, it is a safe assumption that at frequencies of 25 MHz and below AC is the best choice. If the system frequency could reach 40 MHz and beyond, Thevenin becomes the better choice.

ADDITIONAL CONSIDERATIONS WHEN TERMINATING CLOCK LINES

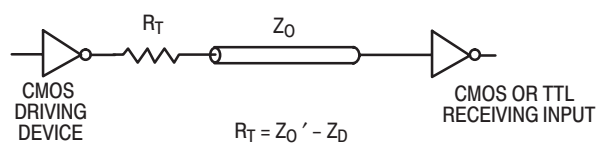
The results presented might imply that terminating the clock lines will completely solve noise problems, but termination can cause secondary problems with some logic devices. Termination acts to reduce the noise seen at the receiver, but that noise actually is seen as additional current and noise at the output of the driving device. If the internal and input logic on the source device is not sufficiently decoupled on chip from the high current outputs, internal threshold problems can occur. This phenomenon is commonly known as 'dynamic threshold.' It is usually evidenced by glitches appearing on the outputs of a fast, high current drive logic device as it switches high or low. This is most severe on 'ACT' devices which have high current and high slew rate CMOS outputs along with TTL inputs which have low noise immunity. This problem can be minimized by decoupling the internal ground and V_{CC} supplies on-chip and in the package. This decoupling is accomplished by having separate 'quiet' ground and V_{CC} pads on chip which supply the input circuitry's ground and V_{CC} references. These pads are then tied to extra 'quiet' ground and 'quiet' V_{CC} pins on the package, or to special 'split leads' which resemble a tuning fork and utilize the leadframe inductance to accomplish the decoupling. When choosing a clock source, make sure that the part has one of these decoupling schemes.

References

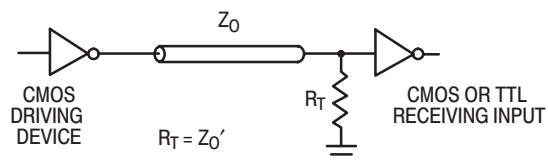
1. Blood, William R., *MECL System Design Handbook*, Motorola Inc., 1983.
2. Application Note AN1051, *Transmission Line Effects in PCB Applications*, Motorola Inc., 1990.
3. *Motorola FACT Data Book* DL138, Motorola Inc., 1990.



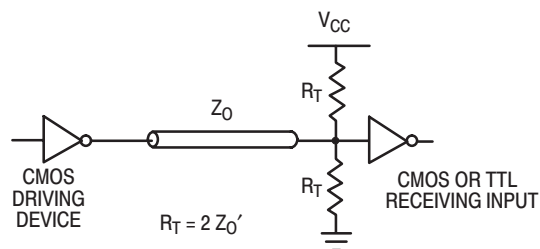
A. TRANSMISSION LINE WITH NO TERMINATION

WHERE, Z_D = DRIVING DEVICE OUTPUT IMPEDANCE

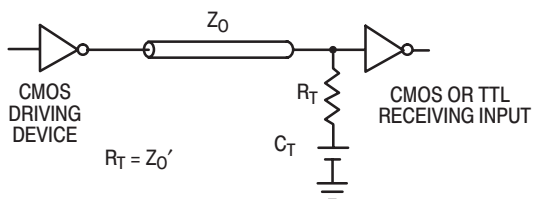
B. TRANSMISSION LINE WITH SERIES TERMINATION



C. TRANSMISSION LINE WITH PARALLEL TERMINATION



D. TRANSMISSION LINE WITH THEVENIN TERMINATION



E. TRANSMISSION LINE WITH AC TERMINATION

Figure 5. Schematic Representation of Common Termination Techniques

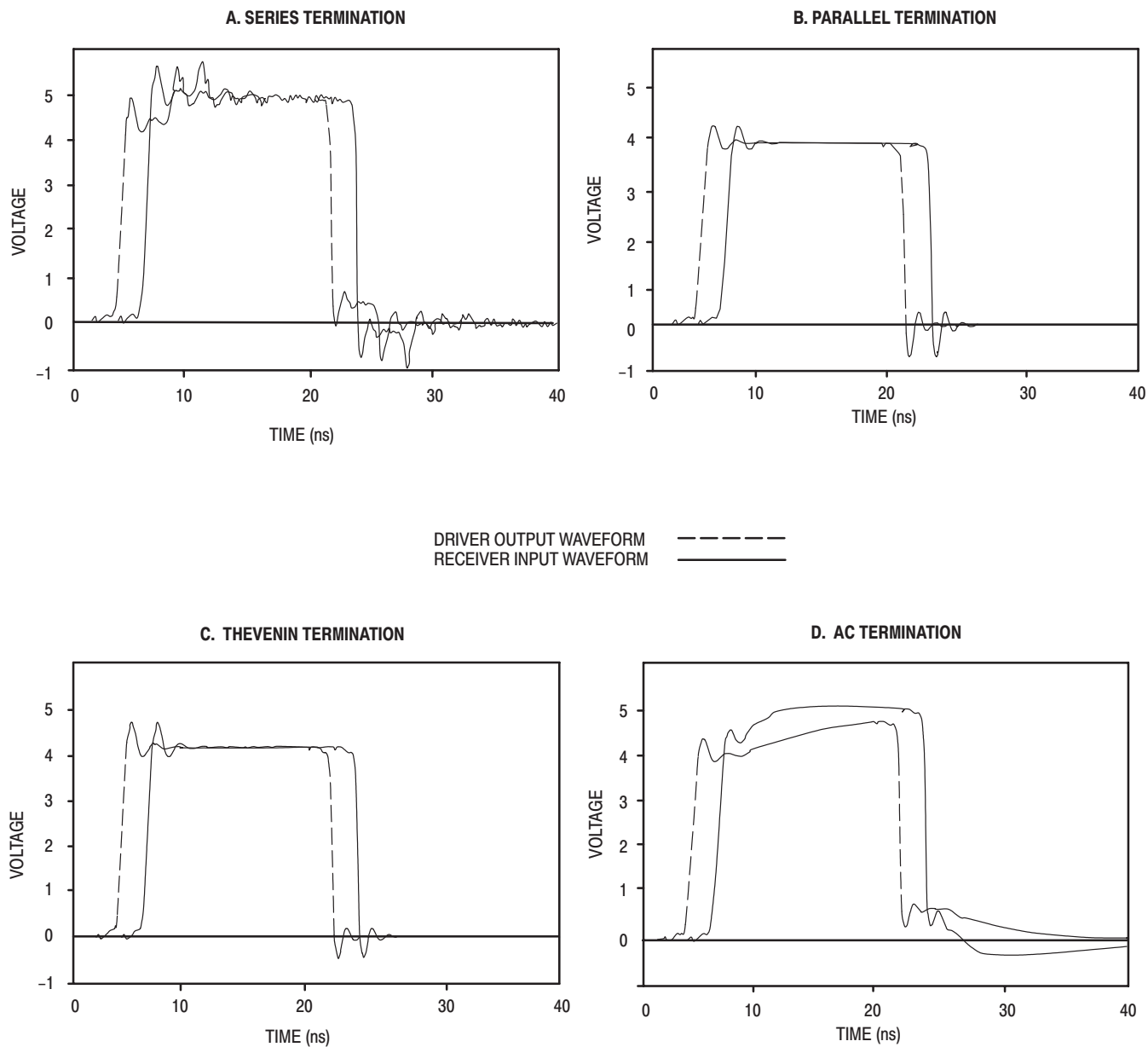


Figure 6. SPICE Simulation Results for Various Terminations of a 9-Inch 41 Ω Transmission Line. Simulations Were Run with Typical Model Parameters @ 25°C and $V_{CC} = 5.0$ V

AN1405

ECL Clock Distribution Techniques

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Abstract

This application note provides information on system design using ECL logic technologies for reducing system clock skew over the alternative CMOS and TTL technologies.

INTRODUCTION

The ever increasing performance requirements of today's systems has placed an even greater emphasis on the design of low skew clock generation and distribution networks. Clock skew, the difference in time between "simultaneous" clock transitions within a system, is a major component of the constraints which form the upper bound for the system clock frequency. Reductions in system clock skew allow designers to increase the performance of their designs without having to resort to more complicated architectures or more costly, faster logic. ECL logic technologies offer a number of advantages for reducing system clock skew over the alternative CMOS and TTL technologies.

SKEW DEFINITIONS

The skew introduced by logic devices can be divided into three parts: duty cycle skew, output-to-output skew and part-to-part skew. Depending on the specific application, each of the three components can be of equal or overriding importance.

Duty Cycle Skew

The duty cycle skew is a measure of the difference between the T_{PLH} and T_{PHL} propagation delays (Figure 1). Because differences in T_{PLH} and T_{PHL} will result in pulse width distortion the duty cycle skew is sometimes referred to as pulse skew. Duty cycle skew is important in applications where timing operations occur on both edges or when the duty cycle of the clock signal is critical. The latter is a common requirement when driving the clock inputs of advanced microprocessors.

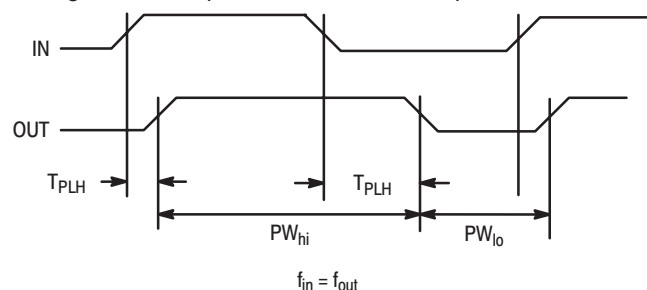


Figure 1. Duty Cycle Skew

Output-to-Output Skew

Output-to-output skew is defined as the difference between the propagation delays of all the outputs of a device. A key constraint on this measurement is the requirement that the

output transitions are identical, therefore if the skew between all edges produced by a device is important the output-to-output skew would need to be added to the duty cycle skew to get the total system skew. Typically the output-to-output skew will be smaller than the duty cycle skew for TTL and CMOS devices. Because of the near zero duty cycle skew of a differential ECL device the output-to-output skew will generally be larger. The output-to-output skew is important in systems where either a single device can provide all of the necessary clocks or for the first level device of a nested clock distribution tree. In these two situations the only parameter of importance will be the relative position of each output with respect to the other outputs on that die. Since these outputs will all see the same environmental and process conditions the skew will be significantly less than the propagation delay windows specified in the standard device data sheet.

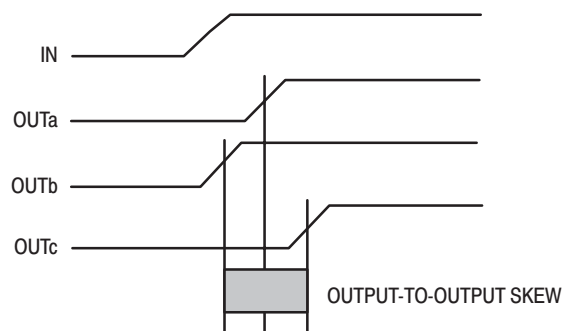


Figure 2. Output-to-Output Skew

Part-to-Part Skew

The part-to-part skew specification is by far the most difficult performance aspect of a device to minimize. Because the part-to-part skew is dependent on both process variations and variations in the environment the resultant specification is significantly larger than for the other two components of skew. Many times a vendor will provide subsets of part-to-part skew specifications based on non-varying environmental conditions. Care should be taken in reading data sheets to fully understand the conditions under which the specified limits are guaranteed. If the part-to-part skew is specified and is different than the specified propagation delay window for the device one can be assured there are constraints on the part-to-part skew specification.

Power supply and temperature variations are major contributors to variations in propagation delays of silicon devices. Constraints on these two parameters are commonly seen in part-to-part skew specifications. Although there are situations where the power supply variations could be ignored, it is difficult for this author to perceive of a realistic system whose devices are all under identical thermal conditions. Hot spots on boards

or cabinets, interruption in air flow and variations in IC density of a board all lead to thermal gradients within a system. These thermal gradients will guarantee that devices in various parts of the system are under different junction temperature conditions. Although it is unlikely that a designer will need the entire commercial temperature range, a portion of this range will need to be considered. Therefore, a part-to-part skew specified for a single temperature is of little use, especially if the temperature coefficient of the propagation delay is relatively large.

For designs whose clock distribution networks lie on a single board which utilizes power and ground planes an assumption of non-varying power supplies would be a valid assumption and a specification limit for a single power supply would be valuable. If, however, various pieces of the total distribution tree will be on different boards within a system there is a very real possibility that each device will see different power supply levels. In this case a specification limit for a fixed V_{CC} will be inadequate for the design of the system. Ideally the data sheets for clock distribution devices should include information which will allow designers to tailor the skew specifications of the device to their application environment.

SYSTEM ADVANTAGES OF ECL

Skew Reductions

ECL devices provide superior performance in all three areas of skew over their TTL or CMOS competitors. A skew reducing mechanism common to all skew parameters is the faster propagation delays of ECL devices. Since, to some extent, all skew represent a percentage of the typical delays faster delays will usually mean smaller skews. ECL devices, especially clock distribution devices, can be operated in either single-ended or differential modes. To minimize the skew of these devices the differential mode of operation should be used, however even in the single-ended mode the skew performance will be significantly better than for CMOS or TTL drivers.

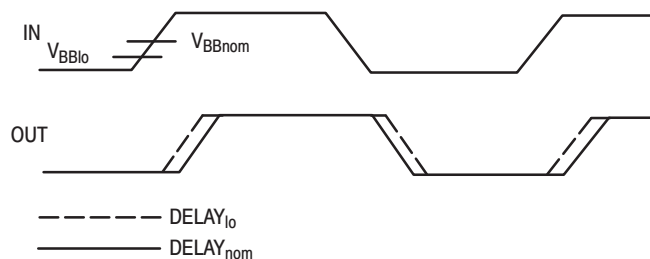


Figure 3. V_{BB} Induced Duty Cycle Skew

ECL output buffers inherently show very little difference between T_{PLH} and T_{PHL} delays. What differences one does see are due mainly to switching reference levels which are not ideally centered in the input swing (see Figure 3). For worst case switching reference levels the pulse skew of an ECL device will still be less than 300 ps. If the ECL device is used differentially the variation in the switching reference will not impact the duty cycle skew as it is not used. In this case the pulse skew will be less than 50 ps and can generally be ignored in all but the highest performance designs. The problem of generating clocks which are capable of meeting the duty cycle requirements of the most advanced microprocessors, would be a trivial task if differential ECL compatible clock inputs were

used. TTL and CMOS clock drivers on the other hand have inherent differences between the T_{PLH} and T_{PHL} delays in addition to the problems with non-centered switching thresholds. In devices specifically designed to minimize this parameter it generally cannot be guaranteed to anything less than 1ns.

The major contributors to output-to-output skew is IC layout and package choice. Differences in internal paths and paths through the package generally can be minimized regardless of the silicon technology utilized at the die level, therefore ECL devices offer less of an advantage in this area than for other skew parameters. CMOS and TTL output performance is tied closely to the power supply levels and the stability of the power busses within the chip. Clock distribution trees by definition always switch simultaneously, thus creating significant disturbances on the internal power busses. To alleviate this problem multiple power and ground pins are utilized on TTL and CMOS clock distribution devices. However even with this strategy TTL and CMOS clock distribution devices are limited to 500 ps – 700 ps output-to-output skew guarantees. With differential ECL outputs very little if any noise is generated and coupled onto the internal power supplies. This coupled with the faster propagation delays of the output buffers produces output-to-output skews on ECL clock chips as low as 50 ps.

Two aspects of ECL clock devices will lead to significantly smaller part-to-part skews than their CMOS and TTL competitors: faster propagation delays and delay insensitivity to environmental variations. Variations in propagation delays with process are typically going to be based on a percentage of the typical delay of the device. Assuming this percentage is going to be approximately equivalent between ECL, TTL and CMOS processes, the faster the device the smaller the delay variations. Because state-of-the-art ECL devices are at least 5 times faster than TTL and CMOS devices, the expected delay variation would be one fifth those of CMOS and TTL devices without even considering environmental dependencies.

The propagation delays of an ECL device are insensitive to variations in power supply while CMOS and TTL device propagation delays vary significantly with changes in this parameter. Across temperature the percentage variation for all technologies is comparable, however, again the faster propagation delays of ECL will reduce the magnitude of the variation. Figure 4 on the following page represents normalized propagation delay versus temperature and power supply for the three technologies.

Low Impedance Line Driving

The clock requirements of today's systems necessitate an almost exclusive use of controlled impedance interconnect. In the past this requirement was unique to the performance levels associated with ECL technologies, and in fact precluded its use in all but the highest performance systems. However the high performance CMOS and TTL clock distribution chips now require care in the design and layout of PC boards to optimize their performance, with this criteria established the migration from these technologies to ECL is simplified. In fact, the difficulties involved in designing with these "slower" technologies in a controlled impedance environment may even enhance the potential of using ECL devices as they are ideally suited to the task.

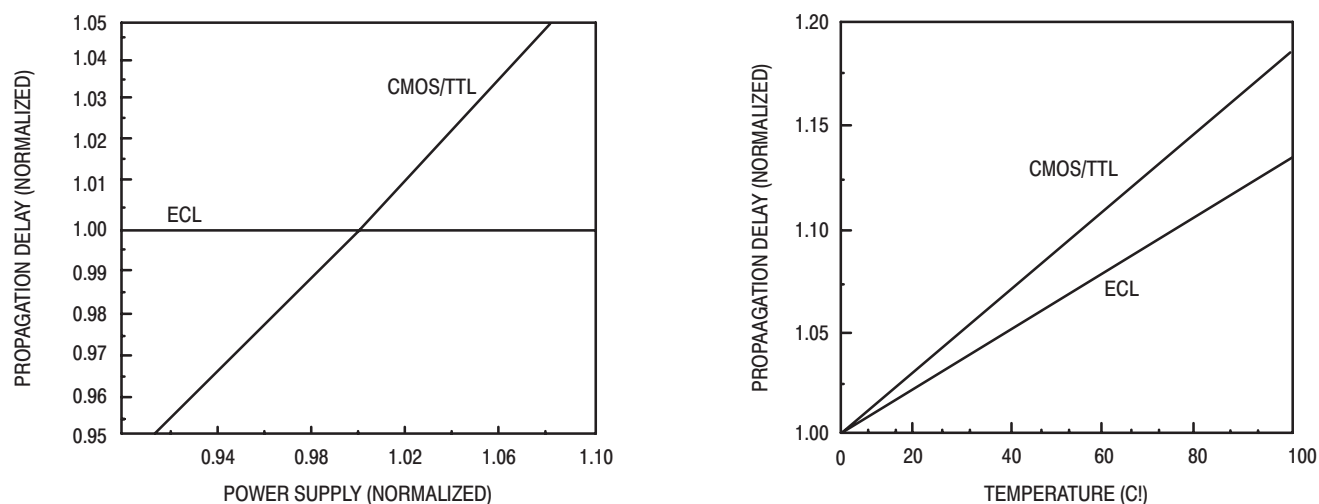


Figure 4. T_{PD} vs Environmental Condition Comparison

The low impedance outputs and high impedance inputs of an ECL device are ideal for driving 50 Ω to 130 Ω controlled impedance transmission lines. The specified driving impedance of ECL is 50 Ω , however this value is used only for convenience sake due to the 50 Ω impedance of most commonly used measurement equipment. Utilizing higher impedance lines will reduce the power dissipated by the termination resistors and thus should be considered in power sensitive designs. The major drawback of higher impedance lines (delays more dependent on capacitive loading) may not be an issue in the point to point interconnect scheme generally used in low skew clock distribution designs.

Differential Interconnect

The device skew minimization aspects of differential ECL have already been discussed however there are other system level advantages that should be mentioned. Whenever clock lines are distributed over long distances the losses in the line and the variations in power supply upset the ideal relationship between input voltages and switching thresholds. Because differential interconnect "carries" the switching threshold information from the source to the load the relationship between the two is less likely to be changed. In addition for long lines the smaller swings of an ECL device produce much lower levels of cross-talk between adjacent lines and minimizes EMI radiation from the PC board.

There is a cost associated with fully differential ECL, more pins for equivalent functions and more interconnect to be laid on a typically already crowded PC board. The first issue is really a non-issue for clock distribution devices. The output-to-output and duty cycle skew are very much dependent on quiet internal power supplies. Therefore the pins sacrificed for the complimentary outputs would otherwise have to be used as power supply pins, thus functionality is actually gained for an equivalent pin count as the inversion function is also available on a differential device. The presence of the inverted signal could be invaluable for a design which clocks both off the positive and negative edges. Figure 5 shows a method of obtaining very low skew (<50 ps) 180° shifted two phase clocks.

It is true that differential interconnect requires more signals to be routed on the PC board. Fortunately with the wide data and address buses of today's designs the clock lines represent a

small fraction of the total interconnect. The final choice as to whether or not to use differential interconnect lies in the level of skew performance necessary for the design. It should be noted that although single-ended ECL provides less attractive skew performance than differential ECL, it does provide significantly better performance than equivalent CMOS and TTL functions.

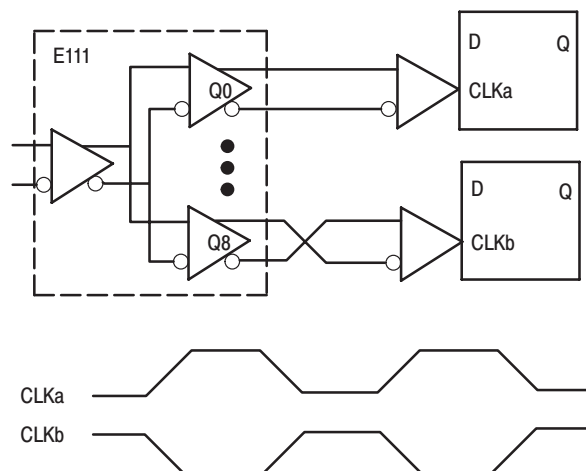


Figure 5. 180° Shifted Two Phase Clocks

USING ECL WITH POSITIVE SUPPLIES

It is hard to argue with the clock distribution advantages of ECL presented thus far, but it may be argued that except for all ECL designs it is too costly to include ECL devices in the distribution tree. This claim is based on the assumption that at least two extra power supplies are required; the negative V_{EE} supply and the negative V_{TT} termination voltage. Fortunately both these assumptions are false. PECL (Positive ECL) is an acronym which describes using ECL devices with a positive rather than negative power supply. It is important to understand that all ECL devices are also PECL devices. By using ECL devices as PECL devices on a +5 volt supply and incorporating termination techniques which do not require a separate termination voltage (series termination, thevenin equivalent) ECL can be incorporated in a CMOS or TTL design with no added cost.

The reason for the choice of negative power supplies as standard for ECL is due to the fact that all of the output levels and internal switching bias levels are referenced to the V_{CC} rail. It is generally easier to keep the grounds quieter and equal potential throughout a system than it is with a power supply. Because the DC parameters are referenced to the V_{CC} rail any disturbances or voltage drops seen on V_{CC} will translate 1:1 to the output and internal reference levels. For this reason when communicating with PECL between two boards it is recommended that only differential interconnect be used. By using differential interconnect V_{CC} variations within the specified range will not in any way affect the performance of the device.

Finally mentioning ECL to a CMOS designer invariably conjures up visions of space heaters as their perception of ECL is high power. Although it is true that the static power of ECL is higher than for CMOS the dynamic power differences between the technologies narrows as the frequency increases. As can be seen in Figure 6 at frequencies as low as 20 MHz the per gate power of ECL is actually less than for CMOS. Since clock distribution devices are never static it does not make sense to compare the power dissipation of the two technologies in a static environment.

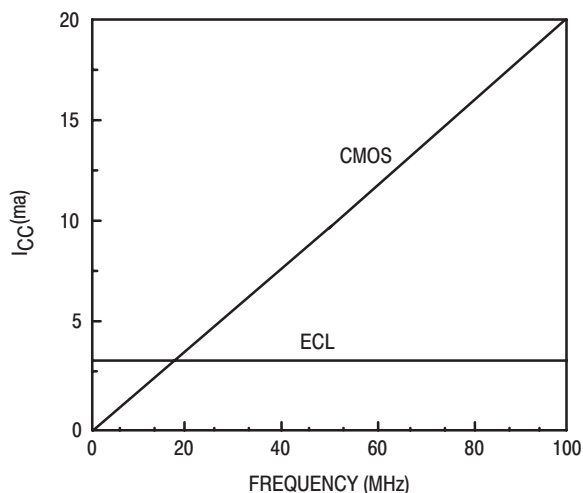


Figure 6. ICC/Gate vs Frequency Comparison

MIXED SIGNAL CLOCK DISTRIBUTION

ECL Clock Distribution Networks

Clock distribution in a ECL system is a relatively trivial matter. Figure 7 illustrates a two level clock distribution tree which produces nine differential ECL clocks on six different cards. The ECLinPS E211 device gives the flexibility of disabling each of the cards individually. In addition the synchronous registered enables will disable the device only when the clock is already in the LOW state, thus avoiding the problem of generating runt pulses when an asynchronous disable is used. The device also provides a muxed clock input for incorporating a high speed system clock and a lower speed test or scan clock within the same distribution tree. The ECLinPS E111 device is used to

receive the signals from the backplane and distribute it on the card. The worst case skew between all 54 clocks in this situation would be 275 ps assuming that all the loads and signal traces are equalized.

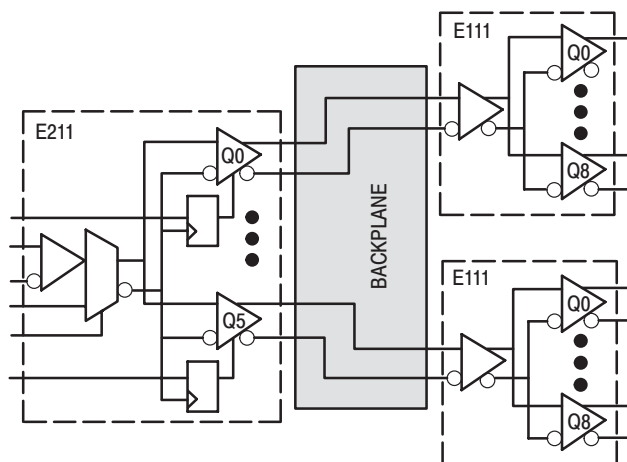


Figure 7. ECL Clock Distribution Tree

Mixed Technology Distribution Networks

Building clock networks in TTL and CMOS systems can be a little more complicated as there are more alternatives available. For simple one level distribution trees fanout devices like the MECL 10H645 1:9 TTL to TTL fanout tree can be used. However as the number of levels of fanout increases the addition of ECL devices in an other wise TTL or CMOS system becomes attractive. In Figure 8 on the next page an E111 device is combined with a MECL H641 device to produce 81 TTL level clocks. Analyzing the skew between the 81 clocks yields a worst case skew, allowing for the full temperature and V_{CC} range variation, of 1.25 ns. Under ideal situations, no variation in temperature or V_{CC} supply, the skew would be only 750 ps. When compared with distribution trees utilizing only TTL or CMOS technologies these numbers represent $\approx 50\%$ improvement, more if the environmental conditions vary to any degree. For a 50 MHz clock the total skew between the 81 TTL clocks is less than 6.5% of the clock period, thus providing the designer extra margin for layout induced skew to meet the overall skew budget of the design.

Many designers have already realized the benefits of ECL clock distribution trees and thus are implementing them in their designs. Furthermore where they have the capability, i.e. ASICs, they are building their VLSI circuits with ECL compatible clock inputs. Unfortunately other standard VLSI circuits such as microprocessors, microprocessor support chips and memory still cling to TTL or CMOS clock inputs. As a result many systems need both ECL and TTL clocks within the same system. Unlike the situation outlined in Figure 8 the ECL levels are not merely intermediate signals but rather are driving the clock inputs of the logic. As a result the ECL edges need to be matched with the TTL edges as pictured in Figure 9.

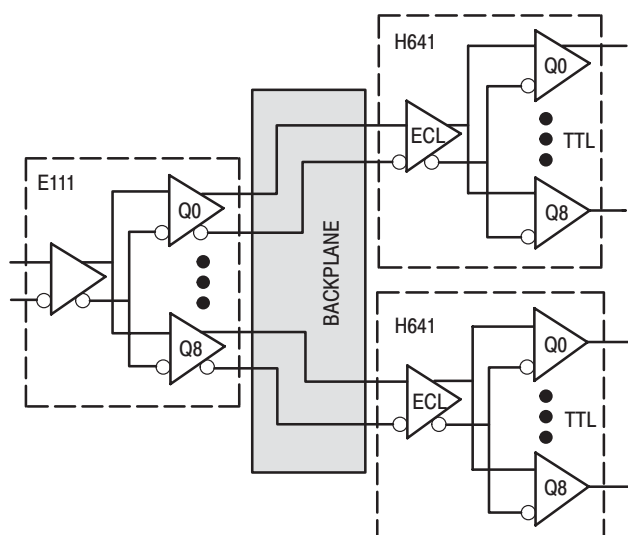


Figure 8. ECL to TTL Clock Distribution

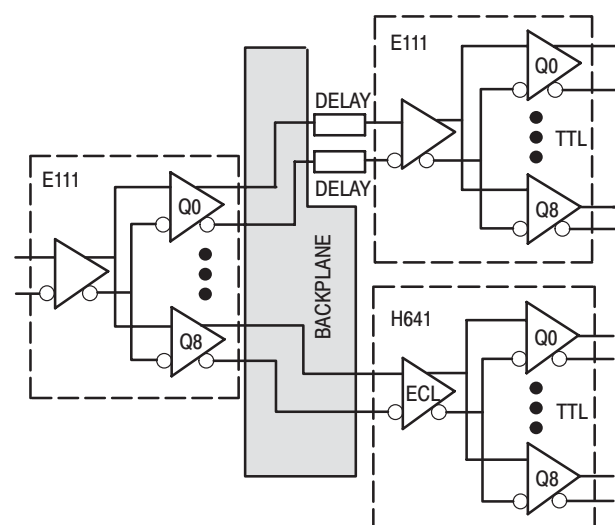


Figure 9. Mixed ECL and TTL Distribution

An ECL clock driver will be significantly faster than a TTL or CMOS equivalent function. Therefore to de-skew the ECL and TTL signals of Figure 9 a delay needs to be added to the input of the ECL device. Because a dynamic delay adjust would not lend itself to most production machines a static delay would be used. The value of the delay element would be a best guess estimate of the differences in the two propagation delays. It is highly unlikely that the temperature coefficients of the propagation delays of the ECL devices, TTL devices and delay devices would be equal. Although these problems will add skew to the system, the resultant total skew of the distribution network will be less than if no ECL chips were used.

PLL Based Clock Drivers

A potential solution for the problem outlined in Figure 9 is in the use of phase locked loop based clock distribution chips. Because these devices feedback an output and lock it to a reference clock input the delay differences between the various technology output buffers will be eliminated. One might believe that with all of the euphoria surrounding the performance of PLL based clock distribution devices that the need for any ECL in the distribution tree will be eliminated. However when analyzed further the opposite appears to be the case.

For a single board design with a one level distribution system there obviously is no need for ECL. When, however, a multiple board system is required where nested levels of devices are needed ECL once again becomes useful. One major aspect of part-to-part skew for PLL based clock chips often overlooked is the dependence on the skew of the various reference clocks being locked to. As can be seen in Figure 10 the specified part-to-part skew of the device would necessarily need to be added to the reference clock skew to get the overall skew of the clock tree. From the arguments presented earlier this skew will be minimized if the reference clock is distributed in ECL. It has not been shown as of yet where a PLL based ECL clock distribution chip can provide the skew performance of the simple fanout buffer. From a system standpoint the buffer type circuits are much easier to design with and thus given equivalent performance would represent the best alternative. The extra features provided by PLL based chips could all be realized if they were used in only the final stage of the distribution tree.

The MPC973 is a PLL based clock driver which features differential PECL reference clock inputs. When combined with the very low skew MC10E111 fanout buffer, very low skew clock trees can be realized for multiprocessor MPP designs. There will be a family of devices featuring various technology compatible inputs and outputs to allow for the building of precisely aligned clock trees based on either ECL, TTL, CMOS or differential GTL (or a mixture of all four) compatible levels.

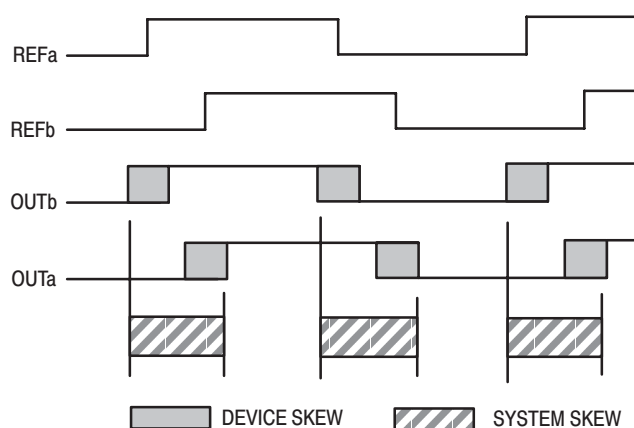


Figure 10. System Skew For PLL Clock Distribution

Conclusion

The best way to maximize the performance of any synchronous system is to spend the entire clock period performing value added operations. Obviously any portion of the clock period spent idle due to clock skew limits the potential performance of the system. Using ECL technology devices in clock distribution networks will minimize all aspects of skew and thus maximize the performance of a system. Unfortunately the VLSI world is not yet ECL clock based so that the benefits of a

totally ECL based distribution tree cannot be realized for many systems. However there are methods of incorporating ECL into the intermediate levels of the tree to significantly reduce the overall skew. In addition the system designers can utilize their new found knowledge to incorporate ECL compatible clocks on those VLSI chips of which they have control while at the same time pressuring other VLSI vendors in doing the same so that future designs can enjoy fully the advantages of distributing clocks with ECL.

AN1406

Designing With PECL (ECL at +5.0 V) The High Speed Solution for the CMOS/TTL Designer

Prepared by: Cleon Petty, Todd Pearson
ECL Applications Engineering

ABSTRACT

This application note provides detailed information on designing with Positive Emitter Coupled Logic (PECL) devices.

INTRODUCTION

PECL, or Positive Emitter Coupled Logic, is nothing more than standard ECL devices run off of a positive power supply. Because ECL, and therefore PECL, has long been the "black magic" of the logic world many misconceptions and falsehoods have arisen concerning its use. However, many system problems which are difficult to address with TTL or CMOS technologies are ideally suited to the strengths of ECL. By breaking through the wall of misinformation concerning the use of ECL, the TTL and CMOS designers can arm themselves with a powerful weapon to attack the most difficult of high speed problems.

It has long been accepted that ECL devices provide the ultimate in logic speed; it is equally well known that the price for this speed is a greater need for attention to detail in the design and layout of the system PC boards. Because this requirement stems only from the speed performance aspect of ECL devices, as the speed performance of any logic technology increases these same requirements will hold. As can be seen in Table 1 the current state-of-the-art TTL and CMOS logic families have attained performance levels which require controlled impedance interconnect for even relatively short distances between source and load. As a result system designers who are using state-of-the-art TTL or CMOS logic are already forced to deal with the special requirements of high speed logic; thus it is a relatively small step to extend their thinking from a TTL and CMOS bias to include ECL devices where their special characteristics will simplify the design task.

Table 1. Relative Logic Speeds

Logic Family	Typical Output Rise/Fall	Maximum Open Line Length (L_{max})*
10KH	1.0 ns	3"
ECLinPS	400 ps	1"
FAST	2.0 ns	6"
FACT	1.5 ns	4"

* Approximate for stripline interconnect ($L_{max} = T_r/2T_{pd}$)

SYSTEM ADVANTAGES OF ECL

The most obvious area to incorporate ECL into an otherwise CMOS/TTL design would be for a subsystem which requires very fast data or signal processing. Although this is the most obvious it may also be the least common. Because of the need

for translation between ECL and CMOS/TTL technologies the performance gain must be greater than the overhead required to translate back and forth between technologies. With typical delays of six to seven nanoseconds for translating between technologies, a significant portion of the logic would need to be realized using ECL for the overall system performance to improve. However, for very high speed subsystem requirements ECL may very well provide the best system solution.

Transmission Line Driving

Many of the inherent features of an ECL device make it ideal for driving long, controlled impedance lines. The low impedance of the open emitter outputs and high input impedance of any standard ECL device make it ideally suited for driving controlled impedance lines. Although designed to drive 50 Ω lines an ECL device is equally adept at driving lines of impedances of up to 130 Ω without significant changes in the AC characteristics of the device. Although some of the newer CMOS/TTL families have the ability to drive 50 Ω lines many require special driver circuits to supply the necessary currents to drive low impedance transmission interconnect. In addition the large output swings and relatively fast output slew rates of today's high performance CMOS/TTL devices exacerbate the problems of crosstalk and EMI radiation. The problems of crosstalk and EMI radiation, along with common mode noise and signal amplitude losses, can be alleviated to a great degree with the use of differential interconnect. Because of their architectures, neither CMOS nor TTL devices are capable of differential communication. The differential amplifier input structure and complimentary outputs of ECL devices make them perfectly suited for differential applications. As a result, for systems requiring signal transmission between several boards, across relatively large distances, ECL devices provide the CMOS/TTL designer a means of ensuring reliable transmission while minimizing EMI radiation and crosstalk.

Figure 1 shows a typical application in which the long line driving, high bandwidth capabilities of ECL can be utilized. The majority of the data processing is done on wide bit width words with a clock cycle commensurate with the bandwidth capabilities of CMOS and TTL logic. The parallel data is then serialized into a high bandwidth data stream, a bandwidth which requires ECL technologies, for transmission across a long line to another box or machine. The signal is received differentially and converted back to relatively low speed parallel data where it can be processed further in CMOS/TTL logic. By taking advantage of the bandwidth and line driving capabilities of ECL the system minimizes the number of lines required for interconnecting the subsystems without sacrificing the overall performance. Furthermore by taking advantage of PECL this application can be realized with a single five volt power supply. The configuration of Figure 1 illustrates a situation where the mixing of logic

technologies can produce a design which maximizes the overall performance while managing power dissipation and minimizing cost.

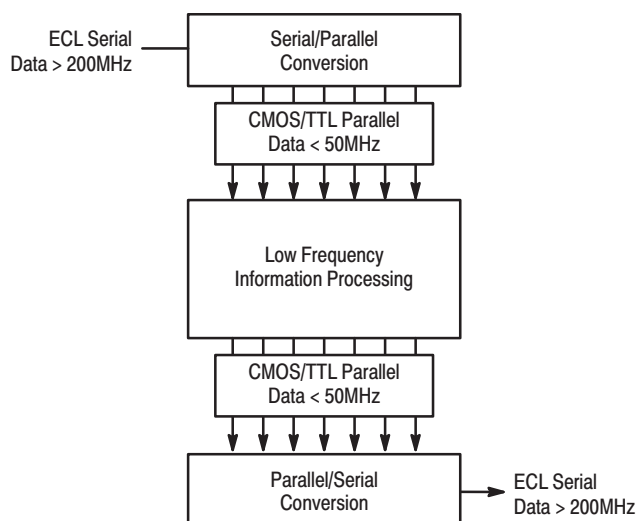


Figure 1. Typical Use of ECL's High Bandwidth, Line Driving Capabilities

Clock Distribution

Perhaps the most attractive area for ECL in CMOS/ TTL designs is in clock distribution. The ever increasing performance capabilities of today's designs has placed an even greater emphasis on the design of low skew clock generation and distribution networks. Clock skew, the difference in time between "simultaneous" clock transitions throughout an entire system, is a major component of the constraints which form the upper bound for the system clock frequency. Reductions in system clock skew allow designers to increase the performance of their designs without having to resort to more complicated architectures or costly, faster logic. ECL logic has the capability of significantly reducing the clock skew of a system over an equivalent design utilizing CMOS or TTL technologies.

The skew introduced by a logic device can be broken up into three areas; the part-to-part skew, the within-part skew and the rise-to-fall skew. The part-to-part skew is defined as the differences in propagation delays between any two devices while the within-device skew is the difference between the propagation delays of similar paths for a single device. The final portion of the device skew is the rise-to-fall skew or simply the differences in propagation delay between a rising input and a falling input on the same gate. The within-device skew and the rise-to-fall skew combine with delay variations due to environmental conditions and processing to comprise the part-to-part skew. The part-to-part skew is defined by the propagation delay window described in the device data sheets.

Careful attention to die layout and package choice will minimize within-device skew. Although this minimization is independent of technology, there are other characteristics of ECL which will further reduce the skew of a device. Unlike their CMOS/TTL counterparts, ECL devices are relatively insensitive to variations in supply voltage and temperature. Propagation

delay variations with environmental conditions must be accounted for in the specification windows of a device. As a result because of ECLs AC stability the delay windows for a device will inherently be smaller than similar CMOS or TTL functions.

The virtues of differential interconnect in line driving have already been addressed, however the benefits of differential interconnect are even more pronounced in clock distribution. The propagation delay of a signal through a device is intimately tied to the switching threshold of that device. Any deviations of the threshold from the center of the input voltage swing will increase or decrease the delay of the signal through the device. This difference will manifest itself as rise-to-fall skew in the device. The threshold levels for both CMOS and TTL devices are a function of processing, layout, temperature and other factors which are beyond the control of the system level designer. Because of the variability of these switching references, specification limits must be relaxed to guarantee acceptable manufacturing yields. The level of relaxation of these specifications increases with increasing logic depth. As the depth of the logic within a device increases the input signal will switch against an increasing number of reference levels; each encounter will add skew when the reference level is not perfectly centered. These relaxed timing windows add directly to the overall system skew. Differential ECL, both internal and external to the die, alleviates this threshold sensitivity as a DC switching reference is no longer required. Without the need for a switching reference the delay windows, and thus system skew, can be significantly reduced while maintaining acceptable manufacturing yields.

What does this mean to the CMOS/TTL designer? It means that CMOS/TTL designers can build their clock generation card and backplane clock distribution using ECL. Designers will not only realize the benefits of driving long lines with ECL but will also be able to realize clock distribution networks with skew specs unheard of in the CMOS/TTL world. Many specialized functions for clock distribution are available from Motorola (MC10/100E111, MC10/100E211, MC10/100EL11). Care must be taken that all of the skew gained using ECL for clock distribution is not lost in the process of translating into CMOS/ TTL levels. To alleviate this problem the MC10/100H646 can be used to translate and fanout a differential ECL input signal into TTL levels. In this way all of the fanout on the backplane can be done in ECL while the fanout on each card can be done in the CMOS/TTL levels necessary to drive the logic.

Figure 2 illustrates the use of specialized fanout buffers to design a CMOS/TTL clock distribution network with minimal skew. With 50ps output-to-output skew of the MC10/100E111 and 1ns part-to-part skew available on the MC10/100H646 or MC10/100H641, a total of 72 or 81 TTL clocks, respectively, can be generated with a worst case skew between all outputs of only 1.05 ns. A similar distribution tree using octal CMOS or TTL buffers would result in worst case skews of more than 6ns. This 5 ns improvement in skew equates to about 50% of the up/down time of a 50MHz clock cycle. It is not difficult to imagine situations where an extra 50% of time to perform necessary operations would be either beneficial or even a life saver. For more information about using ECL for clock distribution, refer to application note AN1405/D – ECL Clock Distribution Techniques.

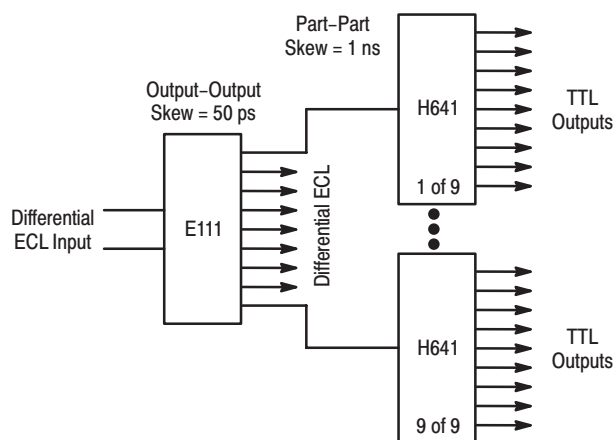


Figure 2. Low Skew Clock Fanout Tree

PECL VERSUS ECL

Nobody will argue that the benefits presented thus far are not attractive, however the argument will be made that the benefits are not enough to justify the requirements of including ECL devices in a predominantly CMOS/TTL design. After all the inclusion of ECL requires two additional negative voltage supplies; V_{EE} and the terminating voltage V_{TT} . Fortunately this is where the advantages of PECL come into play. By using ECL devices on a positive five volt CMOS/TTL power supply and using specialized termination techniques ECL logic can be incorporated into CMOS/TTL designs without the need for additional power supplies. What about power dissipation you ask, although it is true that in a DC state ECL will typically dissipate more power than a CMOS/TTL counterpart, in applications which operate continually at frequency, i.e., clock distribution, the disparity between ECL and CMOS/TTL power dissipation is reduced. The power dissipation of an ECL device remains constant with frequency while the power of a CMOS/TTL device will increase with frequency. As frequencies approach 50MHz the difference between the power dissipation of a CMOS or TTL gate and an ECL gate will be minimal. 50MHz clock speeds are becoming fairly common in CMOS/TTL based designs as today's high performance MPUs are fast approaching these speeds. In addition, because ECL output swings are significantly less than those of CMOS and TTL the power dissipated in the load will be significantly less under continuous AC conditions.

It is clear that PECL can be a powerful design tool for CMOS/TTL designers, but where can one get these PECL devices. Perhaps the most confusing aspect of PECL is the misconception that a PECL device is a special adaptation of an ECL device. In reality every ECL device is also a PECL device; there is nothing magical about the negative voltage supply used for ECL devices. The only real requirement of the power supplies is that the potential difference described in the device data sheets appears across the upper and lower power supply rails (V_{CC} and V_{EE} respectively). A potential stumbling block arises in the specified V_{EE} levels for the various ECL families. The 10 H and 100 K families specify parametric values for potential differences between V_{CC} and V_{EE} of 4.94 V to 5.46 V and 4.2 V to 4.8 V respectively; this poses a problem for the CMOS/TTL designer who works with a typical V_{CC} of $5.0V \pm 5\%$. However, because both of these ECL standards are voltage

compensated both families will operate perfectly fine and meet all of the performance specifications when operated on standard CMOS/TTL power supplies. In fact, Motorola is extending the V_{EE} specification ranges of many of their ECL families to be compatible with standard CMOS/TTL power supplies. Unfortunately earlier ECL families such as MECL 10 K™ are not voltage compensated and therefore any reduction in the potential difference between the two supplies will result in an increase in the V_{OL} level, and thus a decreased noise margin. For the typical CMOS/TTL power supplies a 10 K device will experience an ≈ 50 mV increase in the V_{OL} level. Designers should analyze whether this loss of noise margin could jeopardize their designs before implementing PECL formatted 10 K using $5.0V \pm 5\%$ power supplies.

The traditional choice of a negative power supply for ECL is the result of the upper supply rail being used as the reference for the I/O and internal switching bias levels of the technology. Since these critical parameters are referenced to the upper rail any noise on this rail will couple 1:1 onto them; the result will be reduced noise margins in the design. Because, in general, it is a simpler task to keep a ground rail relatively noise free, it is beneficial to use the ground rail as this reference. However when careful attention is paid to the power supply design, PECL can be used to optimize system performance. Once again the use of differential PECL will simplify the designer's task as the noise margins of the system will be doubled and any noise riding on the upper V_{CC} rail will appear as common mode noise; common mode noise will be rejected by the differential receiver.

MECL TO PECL DC LEVEL CONVERSION

Although using ECL on positive power supplies is feasible, as with any high speed design there are areas in which special attention should be placed. When using ECL devices with positive supplies the input output voltage levels need to be translated. This translation is a relatively simple task. Since these levels are referenced off of the most positive rail, V_{CC} , the following equation can be used to calculate the various specified DC levels for a PECL device:

$$\text{PECL Level} = V_{CC\text{NEW}} - \text{ISpecification Level}$$

As an example, the $V_{OH\text{MAX}}$ level for a 10H device operating with a V_{CC} of 5.0 V at 25°C would be as follows:

$$\text{PECL Level} = 5.0V - 1 - 0.81V$$

$$\text{PECL Level} = (5.0 - 0.81)V = 4.19V$$

The same procedure can be followed to calculate all of the DC levels, including V_{BB} for any ECL device. Table 2, on page 786, outlines the various PECL levels for a V_{CC} of 5.0V for both the 10H and 100K ECL standards. As mentioned earlier any changes in V_{CC} will show up 1:1 on the output DC levels. Therefore any tolerance values for V_{CC} can be transferred to the device I/O levels by simply adding or subtracting the V_{CC} tolerance values from those values provided in Table 2.

PECL TERMINATION SCHEMES

PECL outputs can be terminated in all of the same ways standard ECL, this would be expected since an ECL and a PECL device are one in the same. Figure 3 illustrates the various output termination schemes utilized in typical ECL systems. For best performance the open line technique in Figure 3 would not be used except for very short interconnect between devices; the definition of short can be found in the various design guides for the different ECL families. In general

for the fastest performance and the ability to drive distributive loads the parallel termination techniques are the best choice. However occasions may arise where a long uncontrolled or variable impedance line may need to be driven; in this case the series termination technique would be appropriate. For a more thorough discourse on when and where to use the various termination techniques the reader is referred to the MECL System Design Handbook (HB205/D) and the design guide in

the ECLinPS Databook (DL140/D). The parallel termination scheme of Figure 3 requires an extra V_{TT} power supply for the impedance matching load resistor. In a system which is built mainly in CMOS/TTL this extra power supply requirement may prohibit the use of this technique. The other schemes of Figure 3 use only the existing positive supply and ground and thus may be more attractive for the CMOS/ TTL based machine.

Table 2. ECL/PECL DC Level Conversion for $V_{CC} = 5.0V$

Symbol	10E Characteristics						100E Characteristics		Unit
	0°C		25°C		85°C		0 to 85°C		
	Min	Max	Min	Max	Min	Max	Min	Max	
V _{OH}	−1.02/3.98	−0.84/4.16	−0.98/4.02	−0.81/4.19	−0.92/4.08	−0.735/4.265	−1.025/3.975	−0.880/4.120	V
V _{OL}	−1.95/3.05	−1.63/3.37	−1.95/3.05	−1.63/3.37	−1.95/3.05	−1.600/3.400	−1.810/3.190	−1.620/3.380	V
V _{OHA}	—	—	—	—	—	—	—	−1.610/3.390	V
V _{OLA}	—	—	—	—	—	—	−1.035/3.965	—	V
V _{IH}	−1.17/3.83	−0.84/4.16	−1.13/3.87	−0.81/4.19	−1.07/3.93	−0.735/4.265	−1.165/3.835	−0.880/4.120	V
V _{IL}	−1.95/3.05	−1.48/3.52	−1.95/3.05	−1.48/3.52	−1.95/3.05	−1.450/3.550	−1.810/3.190	−1.475/3.525	V
V _{BB}	−1.38/3.62	−1.27/3.73	−1.35/3.65	−1.25/3.75	−1.31/3.69	−1.190/3.810	−1.380/3.620	−1.260/3.740	V

Parallel Termination Schemes

Because the techniques using an extra V_{TT} power supply consume significantly less power, as the number of PECL devices incorporated in the design increases the more attractive the V_{TT} supply termination scheme becomes. Typically ECL is specified driving $50\ \Omega$ into a $-2.0\ V$, therefore for PECL with a V_{CC} supply different than ground the V_{TT} terminating voltage will be $V_{CC} - 2.0\ V$. Ideally the V_{TT} supply would track 1:1 with V_{CC} , however in theory this scenario is highly unlikely. To ensure proper operation of a PECL device within the system the tolerances of the V_{TT} and the V_{CC} supplies should be considered. Assume for instance that the nominal case is for a $50\ \Omega$ load (R_t) into a $+3.0\ V$ supply; for a 10H compatible device with a V_{OHmax} of $-0.81\ V$ and a realistic V_{OLmin} of $-1.85\ V$ the following can be derived:

$$I_{OHmax} = (V_{OHmax} - V_{TT})/R_t$$

$$I_{OHmax} = ((5.0 - 0.81) - 3.0)/50 = 23.8\ \text{mA}$$

$$I_{OLmin} = (V_{OLmin} - V_{TT})/R_t$$

$$I_{OLmin} = ((5.0 - 1.85) - 3.0)/50 = 3.0\ \text{mA}$$

If $\pm 5\%$ supplies are assumed a V_{CC} of $V_{CCnom} - 5\%$ and a V_{TT} of $V_{TTnom} + 5\%$ will represent the worst case. Under these conditions, the following output currents will result:

$$I_{OHmax} = ((4.75 - 0.81) - 3.15)/50 = 15.8\ \text{mA}$$

$$I_{OLmin} = ((4.75 - 1.85) - 3.15)/50 = 0\ \text{mA}$$

Using the other extremes for the supply voltages yields:

$$I_{OHmax} = 31.8\ \text{mA}$$

$$I_{OLmin} = 11\ \text{mA}$$

The changes in the I_{OH} currents will affect the DC V_{OH} levels by $\pm 40\text{mV}$ at the two extremes. However in the vast majority of cases the DC levels for ECL devices are well centered in their specification windows, thus this variation will simply move the level within the valid specification window and no loss of worst case noise margin will be seen. The I_{OL} situation on the other

hand does pose a potential AC problem. In the worst case situation the output emitter follower could move into the cutoff state. The output emitter followers of ECL devices are designed to be in the conducting "on" state at all times. If cutoff, the delay of the device will be increased due to the extra time required to pull the output emitter follower out of the cutoff state. Again this situation will arise only under a number of simultaneous worst case situations and therefore is highly unlikely to occur, but because of the potential it should not be overlooked.

Thevenin Equivalent Termination Schemes

The Thevenin equivalent parallel termination technique of Figure 3 is likely the most attractive scheme for the CMOS/TTL designer who is using a small amount of ECL. As mentioned earlier this technique will consume more power, however the absence of an additional power supply will more than compensate for the extra power consumption. In addition, this extra power is consumed entirely in the external resistors and thus will not affect the reliability of the IC. As is the case with standard parallel termination, the tolerances of the V_{TT} and V_{CC} supplies should be addressed in the design phase. The following equations provide a means of determining the two resistor values and the resulting equivalent V_{TT} terminating voltage.

$$R1 = R2 \{ (V_{CC} - V_{TT}) / (V_{TT} - V_{EE}) \}$$

$$R2 = Z_0 \{ (V_{CC} - V_{EE}) / (V_{CC} - V_{TT}) \}$$

$$V_{TT} = V_{CC} (R2 / (R1 + R2))$$

For the typical setup:

$$V_{CC} = 5.0\ V; V_{EE} = \text{GND}; V_{TT} = 3.0\ V; \text{ and } Z_0 = 50\ \Omega$$

$$R2 = 50 \{ (5 - 0) / (5 - 3) \} = 125\ \Omega$$

$$R1 = 125 \{ (5 - 3) / (3 - 0) \} = 83.3\ \Omega$$

checking for V_{TT}

$$V_{TT} = 5 \{ (125 / (125 + 83.3)) \} = 3.0\ V$$

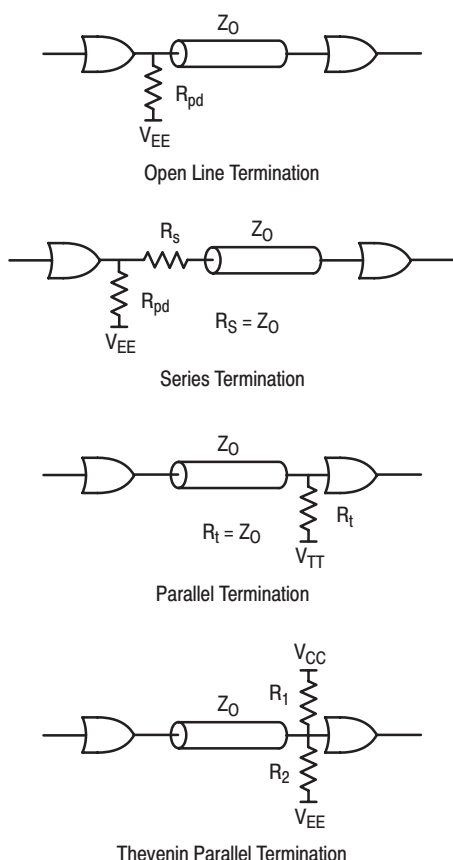


Figure 3. Termination Techniques for ECL/PECL Devices

Because of the resistor divider network used to generate V_{TT} the variation in V will be intimately tied to the variation in V_{CC} . Differentiating the equation for V_{TT} with respect to V_{CC} yields:

$$dV_{TT}/dV_{CC} = R2/(R1 + R2) dV_{CC}$$

Again for the nominal case this equation reduces to:

$$\Delta V_{TT} = 0.6 \Delta V_{CC}$$

So that for $\Delta V_{CC} = \pm 5\% = \pm 0.25$ V, $\Delta V_{TT} = \pm 0.15$ V.

As mentioned previously the real potential for problems will be if the V_{OL} level can potentially put the output emitter follower into cutoff. Because of the relationship between the V_{CC} and V_{TT} levels the only situation which could present a problem will be for the lowest value of V_{CC} . Applying the equation for I_{OLmin} under this condition yields:

$$I_{OLmin} = (V_{OLmin} - V_{TT})/R_t$$

$$I_{OLmin} = (4.75 - 1.85) / 2.85 = 1.0 \text{ mA}$$

From this analysis it appears that there is no potential for the output emitter follower to be cutoff. This would suggest that the Thevenin equivalent termination scheme is actually a better design to compensate for changes in V_{CC} due to the fact that these changes will affect V_{TT} , although not 1:1 as would be ideal, in the same way. To make the design even more immune to potential output emitter follower cutoff the designer can

design for nominal operation for the worst case situation. Since the designer has the flexibility of choosing the V_{TT} level via the selection of the $R1$ and $R2$ resistors the following procedure can be followed.

Let $V_{CC} = 4.75$ V and $V_{TT} = V_{CC} - 2.0$ V = 2.75 V

Therefore:

$R2 = 119 \Omega$ and $R1 = 86 \Omega$ thus:

$I_{OHmax} = 23$ mA and $I_{OLmin} = 3.0$ mA

Plugging in these values for the equations at the other extreme for $V_{CC} = 5.25$ V yields:

$V_{TT} = 3.05$ V, $I_{OHmax} = 28$ mA and $I_{OLmin} = 5.2$ mA

Although the output currents are slightly higher than nominal, the potential for performance degradation is much less and the results of any degradation present will be significantly less dramatic than would be the case when the output emitter follower is cutoff. Again in most cases the component manufacturers will provide devices with typical output levels; typical levels significantly reduces any chance of problems. However it is important that the system designer is aware of where any potential problems may come from so they can be dealt with during the initial design.

Differential ECL Termination

Differential ECL outputs can be terminated using two different strategies. The first strategy is to simply treat the complimentary outputs as independent lines and terminate them as previously discussed. For simple interconnect between devices on a single board or short distances across the backplane this is the most common method used. For interconnect across larger distances or where a controlled impedance backplane is not available the differential outputs can be distributed via twisted pair of ribbon cable (use of ribbon cable assumes every other wire is a ground so that a characteristics impedance will arise). Figure 4 illustrates common termination techniques for twisted pair/ribbon cable applications. Notice that Thevenin equivalent termination techniques can be extended to twisted pair and ribbon cable applications as pictured in Figure 4. However for twisted pair/ribbon cable applications the standard termination technique picture in Figure 4 is somewhat simpler and also does not require a separate termination voltage supply. If however the Thevenin techniques are necessary for a particular application the following equations can be used:

$$R1 = R2 = Z_0/2$$

$$R3 = R1 (V_{TT} - V_{EE}) / (V_{OH} + V_{OL} - 2V_{TT})$$

$$V_{TT} = (R3\{V_{OH} + V_{OL}\} + R1\{V_{EE}\}) / (R1 + 2R3)$$

where V_{OH} , V_{OL} , V_{EE} and V_{TT} are PECL voltage levels.

Plugging in the various values for V_{CC} will show that the V_{TT} tracks with V_{CC} at a rate of approximately 0.7:1. Although this rate is approaching ideal it would still behoove the system designer to ensure there are no potential situations where the output emitter follower could become cutoff. The calculations are similar to those performed previously and will not be repeated. The same equations with the change $R1 = R2 = Z_0$ can be used to calculate a "Y" termination for differential outputs into separate microstrip, strip or coaxial cables.

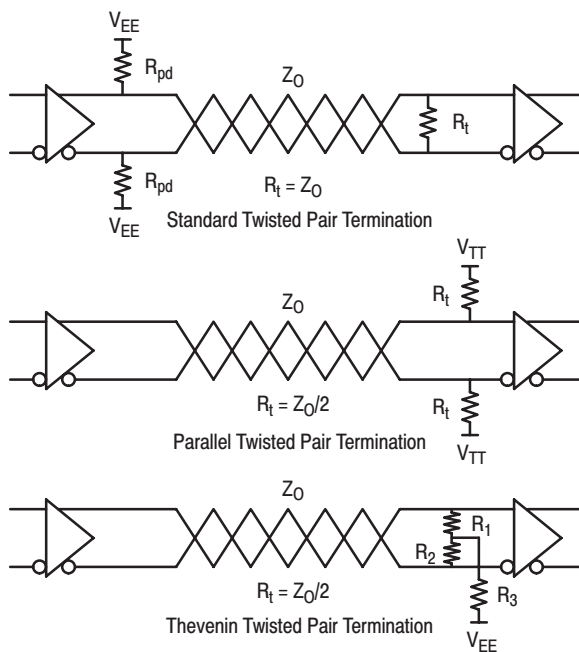


Figure 4. Twisted Pair Termination Techniques

NOISE AND POWER SUPPLY DISTRIBUTION

Since ECL devices are top rail referenced it is imperative that the V_{CC} rail be kept as noise free and variation free as possible. To minimize the V_{CC} noise of a system liberal bypassing techniques should be employed. Placing a bypass capacitor of $0.01\mu\text{F}$ to $0.1\mu\text{F}$ on the V_{CC} pin of every device will help to ensure a noise free V_{CC} supply. In addition when using PECL in a system populated heavily with CMOS and TTL logic the two power supply planes should be isolated as much as possible. This technique will help to keep the large current spike noise typically seen in CMOS and TTL drivers from coupling into the ECL devices. The ideal situation would be multiple power planes; two dedicated to the PECL V_{CC} and ground and the other two to the CMOS/TTL V_{CC} and ground. However if these extra planes are not feasible due to board cost or board thickness constraints common planes with divided subplanes can be used (Figure 5 on page 789). In either case the planes or sub planes should be connected to the system power via separate paths. Use of separate pins of the board connectors is one example of connecting to the system supplies.

For single supply translators or dual supply translators which share common power pins the package pins should be

connected to the ECL V_{CC} and ground planes to ensure the noise introduced to the part through the power plane is minimal. For translating devices with separate TTL and ECL power supply pins, the pins should be tied to the appropriate power planes.

Another concern is the interconnect between two cards with separate connections to the V_{CC} supply. If the two boards are at the opposite extremes of the V_{CC} tolerance, with the driver being at the higher limit and the receiver at the lower limit, there is potential for soft saturation of the receiver input. Soft saturation will manifest itself as degradation in AC performance. Although this scenario is unlikely, again the potential should be examined. For situations where this potential exists there are devices available which are less susceptible to the saturation problem. This variation in V_{CC} between boards will also lead to variations in the input switching references. This variation will lead to switching references which are not ideally centered in the input swing and cause rise/fall skew within the receiving device. Obviously the later skew problem can be eliminated by employing differential interconnect between boards.

When using PECL to drive signals across a backplane, situations may arise where the driver and the receiver are on different power supplies. A potential problem exists if the receiver is powered down independent of the driver. Figure 6, on page 789, represents a generic driver/receiver pair. A current path exists through the receiver's V_{CC} plane when the receiver is powered-down and the driver is powered-on, as shown in Figure 6. If the receiver has ESD protection, the current will flow through the ESD diode to V_{CC} . If the receiver has NO ESD protection, the current will flow through the input transistor and emitter-follower base-collector junctions to V_{CC} . The amount of current flow, in either case, will be enough to damage both the driver and receiver devices. Either of these situations could lead to degradation of the reliability of the devices. Because different devices have different ESD protection schemes, and input architectures, the extent of the potential problem will vary from device to device.

Another issue that arises in driving backplanes is situations where the input signals to the receiver are lost and present an open input condition. Many differential input devices will become unstable in this situation, however, most of the newer designs, and some of the older designs, incorporate internal clamp circuitry to guarantee stable outputs under open input conditions. All of the ECLinPS (except for the E111), ECLinPS Lite, and H600 devices, along with the MC10125, 10H125 and 10114 will maintain stable outputs under open input conditions.

CONCLUSION

The use of ECL logic has always been surrounded by clouds of misinformation; none of those clouds have been thicker than the one concerning PECL. By breaking through this cloud of misinformation the traditional CMOS/TTL designers can approach system problems armed with a complete set of tools. For areas within their designs which require very high speed, the driving of long, low impedance lines or the distribution of very low skew clocks, designers can take advantage of the built in

features of ECL. By incorporating this ECL logic using PECL methodologies this inclusion need not require the addition of more power supplies to unnecessarily drive up the cost of their systems. By following the simple guidelines presented here CMOS/TTL designers can truly optimize their designs by utilizing ECL logic in areas in which they are ideally suited. Thus bringing to market products which offer the ultimate in performance at the lowest possible cost.

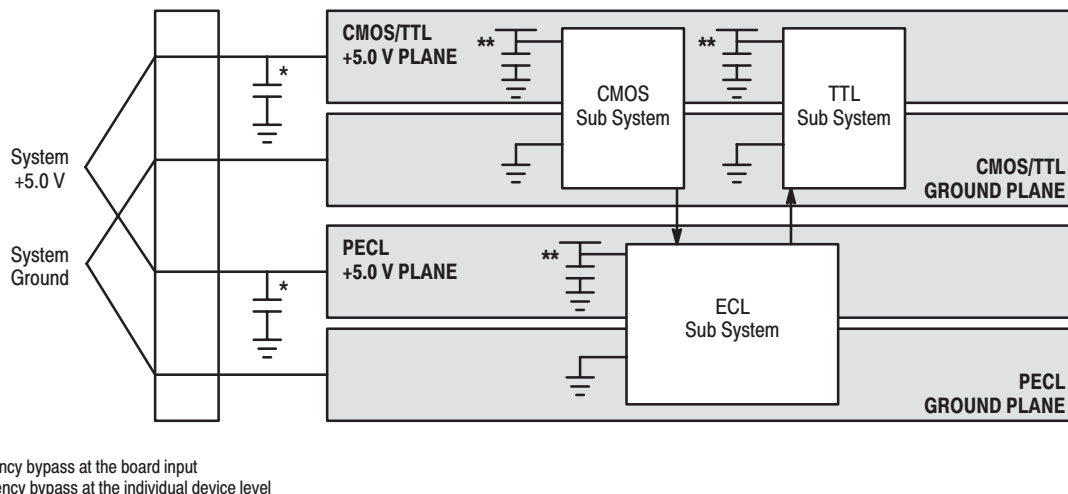


Figure 5. Power Plane Isolation in Mixed Logic Systems

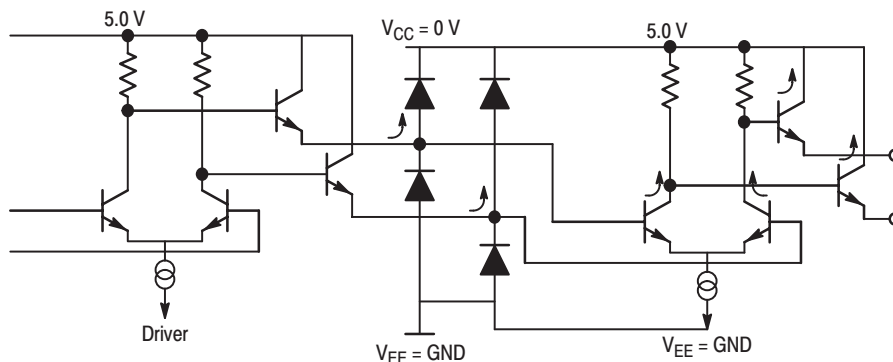


Figure 6. Generic Driver/Receiver Pair

AN1545

Thermal Data for MPC Clock Drivers

Prepared by: Todd Pearson
Applications Engineering

INTRODUCTION

This application note provides general information on thermal and related reliability issues with respect to the MPC family of clock driver products. In addition, methods are presented to estimate power dissipation and junction temperatures for the MPC product family.

Package Choice

The Motorola Timing Solutions products are offered in a variety of surface mount plastic packages. These packages include the 16 and 20 lead SOIC, 20 and 28 lead PLCC and the 32 and 52 lead TQFP packages. The bulk of the newer products are being introduced in the SOIC and TQFP packages with the PLCC being used for the older mature products.

The surface mount plastic packages were selected as the optimum combination of performance, physical size and thermal handling in a low cost standard package. While more exotic packages exist to improve the thermal and electrical performance the cost of these are prohibitive for many applications.

Long Term Failure Mechanisms in Plastic Packages

When analyzing a design for its long term reliability it is important that the dominant failure mechanisms are well understood. Although today's plastic packages are as reliable as ceramic packages under most environmental conditions, as the junction temperature increases a failure mode unique to plastic packages becomes a significant factor in the long term reliability of the device.

Modern plastic package assembly utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. Because plastic packages use injection molding the bond wires used must be extremely ductile to keep from breaking or being pulled from the bond pad during the injection process. Gold wire has far better ductility than aluminum wire and therefore is used in the process of plastic packaging. Aluminum is the metal used in the majority of low cost digital IC processes for transistor and bond wire interconnect. As the temperature of the silicon (junction temperature) increases an intermetallic forms between the gold and aluminum interface. This intermetallic formation results in a significant increase in the impedance of the wire bond and can lead to performance failure of the affected pin. With this relationship between intermetallic formation and junction temperature established, it is incumbent on the designer to ensure that the junction temperature for which a device will operate is consistent with the long term reliability goals of the system.

Reliability studies were performed at elevated ambient temperatures (125°C) from which an arrhenius equation relating junction temperature to bond failure was established. The application of the equation yields Table 1. This table relates the junction temperature of a device in a plastic package to the continuous operating time before 0.1% bond failure (1 failure

per 1000 bonds). Note that this equation only holds for continuous elevated junction temperature levels, as the curve is quite steep if a system cycles through a temperature range but spends a relatively short amount of time at the extreme the numbers provided in this table will grossly underestimate the lifetime of the device based solely on the worst case junction temperature seen.

Table 1. Package Junction Temperatures

Junction Temperature (°C)	Time (Hours)	Time (Years)
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.1
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

The Motorola Timing solutions products are designed with chip power levels that permit acceptable reliability levels, in most systems, under conventional 500lfpm (2.5m/s) airflow. However because of their flexibility and programmability there may be some situations where special thermal considerations may be required.

Thermal Management

In any system design proper thermal management is essential to establish the appropriate trade-off between performance, density, reliability and cost. In particular the designer should be aware of the reliability implication of continuously operating semiconductor devices at high junction temperatures.

The increasing popularity of plastic, small outline surface mount packages is putting a greater emphasis on the need for better thermal management of a system. This is due to the fact that the newer SMD packages generally require less board space than their first generation brethren. Thus designs incorporating the latest generation SMD packaging technologies have a higher thermal density. To optimize the thermal management of a system it is imperative that the user understand all of the variables which contribute to the junction temperature of the device.

The variables involved in determining the junction temperature of a device are both supplier and user defined. The supplier, through lead frame design, mold compounds, die size and die attach can positively impact the thermal resistance and thus, the junction temperature of a device. Motorola continually experiments with new package designs and assembly techniques in an attempt to further enhance the thermal performance of its products.

It can be argued that the user has the greatest control of the variables which commonly impact the thermal performance of a device. Ambient temperature, air flow and related cooling techniques are the obvious user controlled variables, however

PCB substrate material, layout density, amount of exposed copper and weight of copper used in the power planes can all have significant impacts on the thermal performance of a system.

PCB substrates all have different thermal characteristics, these characteristics should be considered when exploring the PCB alternatives. Users should also account for the different power dissipation of the different devices in their systems and space them accordingly. In this way the heat load is spread across a larger area and “hot spots” do not appear in the layout. Copper interconnect and power planes act as heat radiators, therefore significant thermal dissipation can be achieved by paying special attention to the copper elements of a PCB. The thermal resistance of copper (package leadframes are made from copper) is significantly lower than that of the epoxy used for the body of plastic packages. As a result the dominant mode of heat flow out of a package is through the leads. By employing techniques at the board level to enhance the transfer of this heat from the package leads to the PCB one can reduce the effective thermal resistance of the plastic package. Copper interconnect traces on the top layer of the PCB are excellent radiators for transferring heat to the ambient air, especially if these traces are exposed to even moderate air flow. In addition using thick copper power planes not only reduces the electrical resistance but also enhances their thermal carrying capabilities. The power planes can be thermally enhanced further by employing special edge connectors which draw the heat from the planes and again dissipate it into the ambient. Finally, the use of thermal conductive epoxies between the underneath of a device and thermal vias to a power plane can accelerate the transfer of heat from the device to the PCB where once again it can more easily be passed to the ambient.

The advent of small outline SMD packaging and the industry push towards smaller, denser designs makes it incumbent on the designer to provide for the removal of thermal energy from the system. Users should be aware that they control many of the variables which impact the junction temperatures and, thus, to some extent, the long term reliability of their designs.

Calculating Junction Temperature

Since the reliability of a device is directly related to junction temperature and that temperature cannot be measured directly there needs to be a means of calculating the approximate junction temperature from measurable parameters. There are two equations which can be used:

$$T_J = T_A + PD\theta_{JA} \text{ or } T_J = T_C + PD\theta_{JC}$$

where:

T_J = Junction Temperature

T_A = Ambient Temperature (°C)

T_C = Case Temperature (°C)

PD = Internal Power Dissipation of the Device (W)

θ_{JA} = Avg Pkg Thermal Resistance (Junction – Ambient)

θ_{JC} = Avg Pkg Thermal Resistance (Junction – Case)

The θ_{JC} numbers are determined by submerging a device in a liquid bath and measuring the temperature rise of the bath, it therefore represents an average case temperature. The difficulty in using this method arises in the determination of the case temperature in an actual system. The case temperature is a function of the location on the package at which the temperature is measured. Therefore, to use the θ_{JC} method the case temperature would have to be measured at several

different points and averaged to represent the T_C of the device. This in practice could prove difficult and relatively inaccurate. To alleviate this problem manufacturers will sometimes provide a θ_{Jref} value for a package. This number represents the thermal resistance between the die and a specific spot on the package (usually the top dead center). This measure of thermal resistance typically has a much wider standard deviation than the standard resistance parameters and therefore is sometimes avoided, however it is the most easily measured parameter from which junction temperatures can be calculated.

The θ_{JA} method of estimating junction temperature is the most widely used. To use this method one need only measure the ambient air temperature in the vicinity of the device in question and calculate the internal power dissipation of that device. The total power dissipation in a device is made up of two parts; the static power and the dynamic power. The two components can be calculated separately and then added together. Another source of power is the termination power as clock drivers are generally used to drive terminated transmission lines. For an ECL output this can be significant however for CMOS outputs the termination load current is pulled through very little voltage (the output HIGH and LOW voltages are very near the rail) so that most of the power is dissipated in the actual load. With this in mind we will address calculating power for ECL and CMOS/BiCMOS separately.

Because clock drivers generally drive transmission lines we will not assume any lumped capacitive load at the outputs. Lumped capacitive loads on outputs add significantly to the power dissipated on chip, when however the capacitive loads are at the end of transmission lines they are buffered from the driving device and thus do not add to the power dissipation above that attributed to driving the transmission line. Note that for the purpose of power dissipation calculations it is not equivalent to calculate the distributed capacitance of a transmission line and treat it as a lumped load at the output of the device. This technique will significantly overestimate the calculated power of a device.

Calculating Power Dissipation in CMOS/BiCMOS Devices

The total power dissipated in a device can be represented as follows:

$$P_D = I_{CC}(\text{static}) \cdot V_{CC} + I_{CC}(\text{dynamic}) \cdot V_{CC} + n(I_{OH} \cdot (V_{CC} - V_{OH}) + I_{OL} \cdot (V_{OL})) / 2$$

In general rather than using dynamic I_{CC} numbers the dynamic power is calculated using power dissipation capacitance numbers (C_{PD}). Using C_{PD} numbers the above equation becomes:

$$P_D = I_{CC}(\text{static}) \cdot V_{CC} + C_{PD} \cdot V_{CC}^2 \cdot f + n(I_{OH} \cdot (V_{CC} - V_{OH}) + I_{OL} \cdot (V_{OL})) / 2$$

As mentioned previously since the output logic levels are very nearly rail to rail, the third part of the above equation can be ignored. Note that although this assumption may be true for series terminated lines it may not be true for parallel termination where the relatively large DC currents will drive the output voltage levels away from the rails. If we assume series termination then the equation reduces to the following:

$$P_D = I_{CC}(\text{static}) \cdot V_{CC} + C_{PD} \cdot V_{CC}^2 \cdot f$$

The dynamic dissipation may be a function of the number of outputs switching, if this is the case a CPD number may be provided for each output buffer. In this case the equation would expand to:

$$P_D = I_{CC}(\text{static}) \cdot V_{CC} + C_{PD}(\text{internal}) \cdot V_{CC}^2 \cdot f + C_{PD}(\text{output}) \cdot V_{CC}^2 \cdot f \cdot n$$

where n = number of outputs at the given frequency f .

Finally for a CMOS device the $I_{CC}(\text{static}) = 0$ and for a BiCMOS device which utilizes ECL gates internal the $C_{PD}(\text{internal}) = 0$ so that the equations reduce to:

$$\text{CMOS } P_D = C_{PD}(\text{internal}) \cdot V_{CC}^2 \cdot f + C_{PD}(\text{output}) \cdot V_{CC}^2 \cdot f \cdot n$$

$$\text{BiCMOS } P_D = I_{CC}(\text{static}) \cdot V_{CC} + C_{PD}(\text{output}) \cdot V_{CC}^2 \cdot f \cdot n$$

Calculating Power Dissipation in ECL Devices

Starting from the same basic equation:

$$P_D = I_{CC}(\text{static}) \cdot V_{CC} + I_{CC}(\text{dynamic}) \cdot V_{CC} + n(I_{OH} \cdot (V_{CC} - V_{OH}) + I_{OL} \cdot (V_{CC} - V_{OL})) / 2$$

For ECL devices the static current is equal to the dynamic current (I_{CC} is independent of frequency) therefore the equation reduces to:

$$P_D = I_{CC} \cdot V_{CC} + n(I_{OH} \cdot (V_{CC} - V_{OH}) + I_{OL} \cdot (V_{CC} - V_{OL})) / 2$$

The above equation assumes a 50% duty cycle on a single ended output and thus takes the average of the high state and low state power dissipation. For differential outputs it is simpler to calculate the power per output pairs. Since the pairs are always in complementary states the output power for the pair is simply the addition of the low state and high state power consumption. The only time one will see a difference between a single ended and differential output calculation is under worst case conditions. For say an 18 single ended output device the worst case condition would be for all 18 to be in the worst case logic state for power dissipation purposes. For a device on the other hand with 9 pairs of complimentary outputs (18 total) only 9 of the outputs can be in the worst case condition at a time so that the worst case power dissipation of a complimentary output device will be less than a device with an equivalent number of single ended outputs.

The only issue left is determining I_{OL} and I_{OH} . These values are a function of the termination technique and the pull down voltage used. The currents are easily calculated based on the V_{OH}/V_{OL} levels the pull down resistance and the pull down voltage used. For a standard termination of 50Ω to a voltage of 2.0V below V_{CC} :

$$I_{OH} = (V_{CC} - 0.98) - (V_{CC} - 2.0) / 50 = 20.4 \text{ mA}$$

$$I_{OL} = (V_{CC} - 1.7) - (V_{CC} - 2.0) / 50 = 6.0 \text{ mA}$$

9

Thermal Resistance of Plastic Packages

With the power estimates calculated the θ_{JA} of the appropriate package is the only required parameter left to estimate the junction temperature of a device. The θ_{JA} number for a package is expressed in °C per Watt (°C/W) and is used to determine the temperature elevation of the die (junction) over the external ambient temperature. Standard lab measurements of this parameter for the various timing solution packages are provided in the graphs of figure 1 through figure 3.

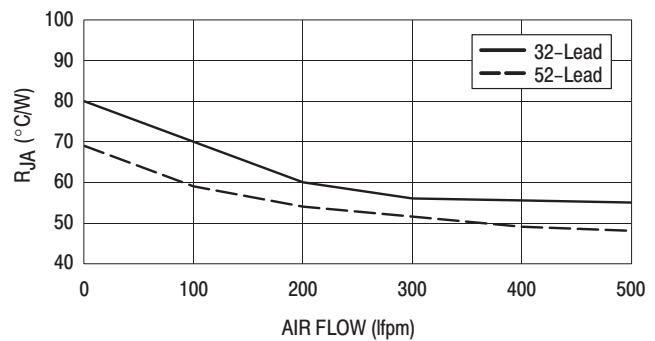


Figure 1. Thermal Resistance of the TQFP Packages

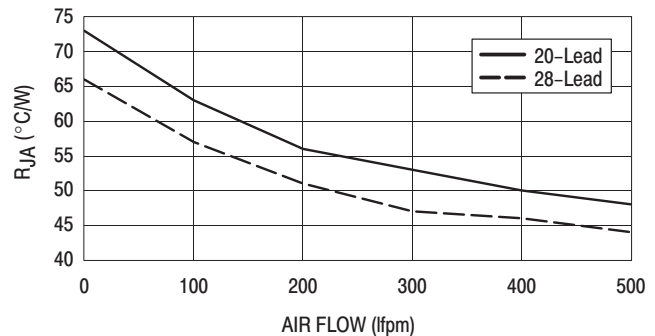


Figure 2. Thermal Resistance of the PLCC Packages

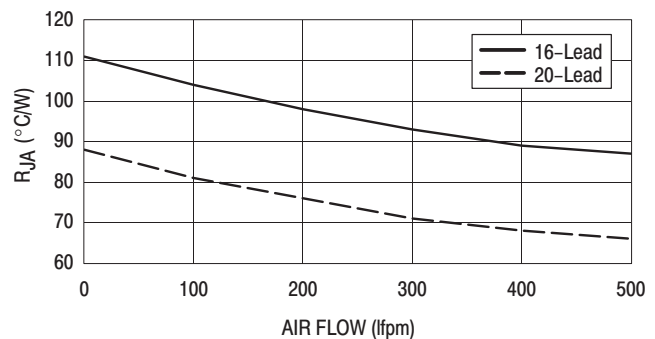


Figure 3. Thermal Resistance of the SOIC Packages

Junction Temperature Calculation Example

As an example the junction temperature of the MPC951 will be calculated. The static I_{CC} of the MPC951 is 95mA and the C_{PD} per output is 25pf. From these numbers the following results:

$$P_D = 95 \text{ mA} \cdot 3.3 \text{ V} + 3.3 \text{ V} \cdot 3.3 \text{ V} \cdot 25 \text{ pf} \cdot f \cdot n = 315 \text{ mW} + 2.72 \text{ e-10} \cdot f \cdot n$$

Assume we will configure all 9 outputs to the same frequency, the curve in figure 4 shows the power dissipation vs frequency for the MPC951.

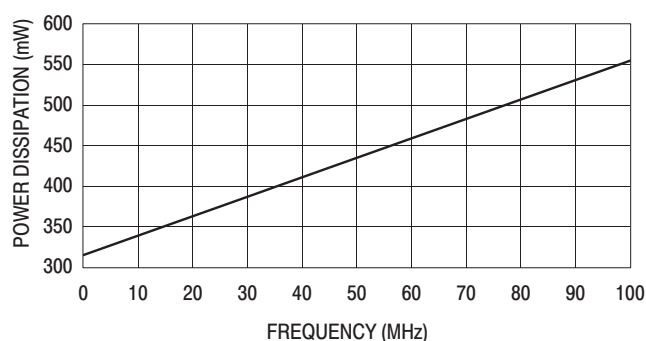


Figure 4. MPC951 Junction Temperature Calculation

Assume that one is building a design with all nine outputs operating at 66MHz. From the graph this corresponds to a power dissipation of 470 mW. The MPC951 is packaged in the 32lead TQFP; from the θ_{JA} chart (assume zero air flow) the thermal resistance of the package is 97°C/W. Plugging these into the T_J equation yields the following:

$$T_J = T_A + 80^\circ\text{C/W} \cdot 0.470 \text{ W} = T_A + 38^\circ\text{C}.$$

For a worst case ambient temperature of 70°C the resulting junction temperature would be 108°C. From the MTBF table this would correspond to a lifetime of greater than nine years, a lifetime which is well within the requirements of most systems. If however the user needed a little higher performance of 100MHz on the outputs the T_J would be:

$$T_J = T_A + 80^\circ\text{C/W} \cdot 0.555 \text{ W} = T_A + 44^\circ\text{C}$$

Under these conditions the worst case junction temperature would be 114°C and the worst case lifetime would be approaching 4 years. This may not be a satisfactory lifetime and the user would have to do some thermal management to reduce the junction temperature. Obvious enhancements would be providing airflow or perhaps reducing the maximum ambient specifications. If airflow was added (200lfpm) the junction temperature would reduce to:

$$T_J = T_A + 60^\circ\text{C/W} \cdot 0.555 \text{ W} = T_A + 33^\circ\text{C}$$

This drops the junction temperature down into the same range as the 66 MHz output case.

The second example will use an ECL output device; the MC100LVE111. The device has 9 differential output pairs and an I_{CC} of 65mA. Assume that the outputs are terminated 50Ω to 2.0V below V_{CC} .

$$P_D = 65 \text{ mA} \cdot 3.3 \text{ V} + 9((0.98 \cdot 1.02/50) + (1.7 \cdot 0.3/50)) = 215 \text{ mW} + 270 \text{ mW} = 485 \text{ mW}$$

The MC100LVE111 is packaged in the 28lead PLCC; from the θ_{JA} tables the θ_{JA} at 500lfpm is 45°C/W. This yield the following approximate junction temperature:

$$T_J = T_A + 45^\circ\text{C/W} \cdot 0.485 \text{ W} = T_A + 22^\circ\text{C}$$

For a maximum ambient of 70°C the LVE111 exhibits more than satisfactory long term reliability for most systems under standard operating conditions.

Note in both cases the most efficient way to lower the junction temperature is to reduce the ambient temperature of the system. Unit changes in ambient temperature result in unit changes in junction temperature no other parameter is this tightly coupled to junction temperature.

Limitations to Junction Temperature Calculations

The use of the previously described technique for estimating junction temperatures is intimately tied to the measured values of the θ_{JA} of the package. Since this parameter is a function of not only the package, but also the test fixture the results may not be applicable for every environmental condition. As mentioned previously the θ_{JA} of a package in a system could be somewhat higher or lower depending on the thermal design of the board.

In addition the reliability numbers derived for the intermetallic formation assumes constant usage at the specific conditions. In the real world devices will not be exposed to worst case conditions continuously but rather will cycle between the worst case and a lower junction temperature. The MTBF table does not take into account this cycling so that simply calculating the worst case junction temperature and applying it to the table directly will significantly underestimate the long term reliability of the device. Because reliability and environmental conditions are statistical in nature it is important that statistical analysis be applied to any long term reliability studies done on the clock driver products.

AN1934

Effects of Skew and Jitter on Clock Tree Design

Prepared by: Don Aldridge and Tom Borr
September, 2001

ABSTRACT

This application note discusses the parametrics of skew and jitter as these terms apply to PLL clock drivers and clock buffers. The application note covers the definition of the various types of skew and jitter, the measurement techniques and values associated with these parameters, and concludes with an example clock tree design and analysis of the skew and jitter.

INTRODUCTION

At first glance, clock distribution trees are relatively simple. As shown in Figure 1, a typical clock distribution tree consists of a clock source and a series of clock distribution buffers that deliver multiple copies of the clock source to many locations in an electronic system. The clock source may be a crystal oscillator (Figure 1) or an external clock source. This clock source may be at the desired frequency or may need to be translated to the desired frequency or frequencies as part of the clock tree circuitry. The clock tree will consist of some combination of PLL clock drivers and/or fanout buffers providing multiple outputs. The clock tree may consist of several devices or be composed of a single integrated circuit. Individual clock outputs deliver the clock signal to various locations on a PC board.

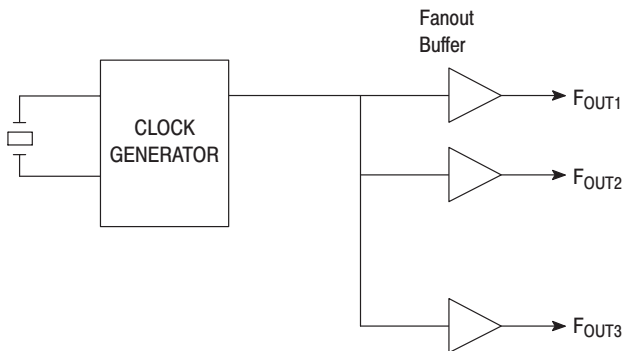


Figure 1. Typical Clock Distribution Tree

After a more detailed look at the requirements of the clock system and the data sheet specifications of the devices used to implement the clock tree, the design appears a bit more complicated and requires a more detailed analysis. The specifications that are most important for this type of analysis are usually found in the AC parameter portion of the clock driver data sheet and consist of parameters such as propagation delay, skew, and jitter.

This application note discusses these parameters by reviewing the definition, the measurement techniques, and their effects on system performance. The application note concludes with the analysis of a typical clock distribution tree based upon these parameters.

Standards for Skew, Jitter Definitions, and Notations

The reference used to determine the standards for skew, jitter definitions, and notations for this application note are the EIA specification EIA/JESD65. This EIA specification documents the current industry standard for these parameters. This document is available in a downloadable PDF format at the web site of <http://www.jedec.org/>.

Clock Driver Devices

Clock driver devices consist of both clock fanout buffers and PLL based clock generators. Typical fanout buffers are shown in Figure 2 and consist of an input buffer driving many outputs through individual output buffers. The specific devices shown are the MPC942C and MPC942P which offer 18 LVCMOS outputs and have either a LVCMOS input or a LVPECL input. Some fanout buffers have an optional internal divider network to produce an input clock divided by two. A Phase Lock Loop device is shown in Figure 4 and may or may not have built-in fanout buffers. It is not the intention of this application note to explain all of the fundamentals of a PLL; however, a quick review of the components is covered.

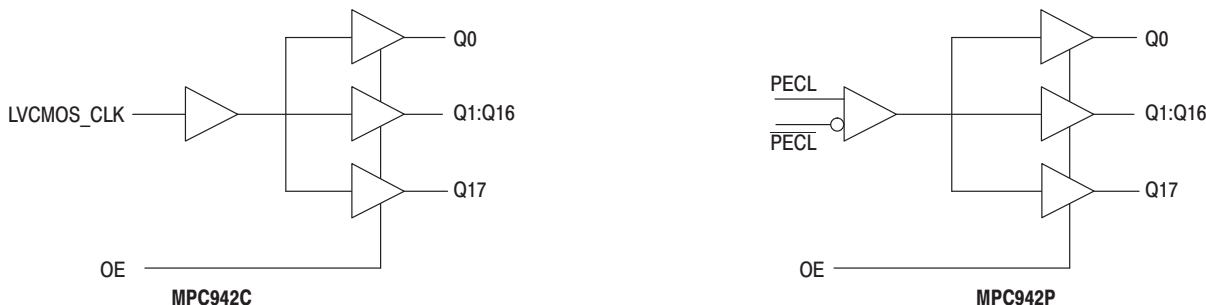


Figure 2. Fanout Buffer

A basic PLL clock architecture (Figure 3) consists of a phase detector, a low pass filter, a V_{CO} , and (in this diagram) two divider networks. Both dividers are at the inputs of the phase detector. The input to the clock driver, or the reference frequency, may be external or sourced from a crystal oscillator that is included as part of the clock driver architecture. This input frequency may be divided by an optional P divider block and then applied to the input of the phase detector. The phase detector produces a correction signal based upon the difference in phase in its two inputs. The correction signal or the output of the voltage controlled oscillator; V_{CO} . The output of the V_{CO} is applied to the M divider and becomes feedback and the second of the two inputs to the phase detector. When the loop is in "lock," the two inputs to the phase detector are the same frequency and the same phase. The output frequency, or F_{OUT} , is the reference frequency divided by P and then multiplied by M and will continually track the reference frequency.

With a few additions to the basic PLL clock architecture, we can create a multi-frequency and multi-clock distribution device as shown in Figure 4. The more complex divider network shown provides the M divide value for the feedback path to the input of the phase detector and, also, the N divider divides down the V_{CO} frequency to the desired system frequency or frequencies. Multiple outputs from the clock divider may provide for the generation of multiple frequencies. Note that fanout buffers are included for each output to provide the required system clock drive. Also note that an equivalent fanout buffer is included for the feedback path. The feedback connection for the PLL is external to the device and thus equalizes the delay through the main clock outputs. As is discussed later, the external feedback path may also include compensating trace delay which allows the phase of F_{OUT} clock to be advanced forward or backward with respect to the input clock.

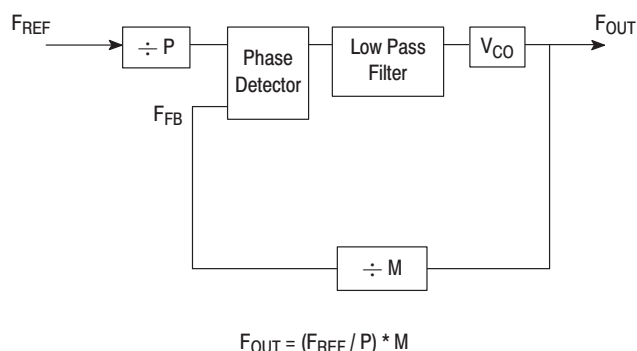


Figure 3. Basic PLL

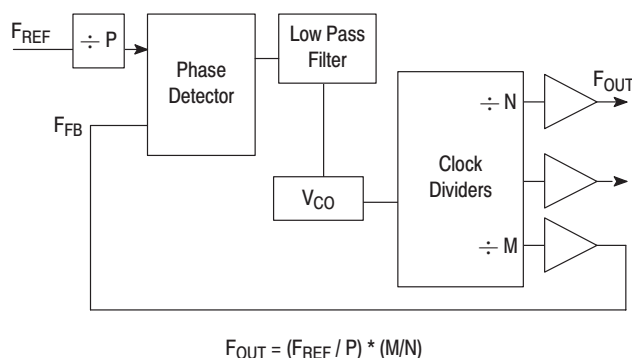


Figure 4. PLL Based Clock Driver

Clock Driver Parametrics

The clock driver parameters that are of interest in this application note are Buffer Propagation Delay, Zero Reference Delay, Skew, Jitter, and PLL Bandwidth and Jitter. These parameters are typically found in the AC parameter portion of a clock driver data sheet.

Fanout buffers have output skew, jitter, and propagation delay. PLL clock driver devices are characterized with jitter, output skew, and an effective input to output propagation delay called Zero Reference Phase Delay. In a clock tree design, the parameters that complicate the analysis is skew between the outputs of a clock fanout buffer and edge or frequency jitter. Jitter commonly is generated in the very early stages of a clock tree and potentially at each stage of the clock tree. These jitter sources may or may not be cumulative and be passed to the outputs.

Buffer Propagation Delay

Clock distribution buffers have a propagation delay from input to output. Typical values for this delay are in the order of a few nanoseconds. Data sheet specifications may be given for a single propagation delay or as separate values given for a low to high edge; versus a high to low edge. The low to high edge value and the high to low edge value should be very similar but not necessarily the same. The notation for propagation delay is t_{pd} . Also the notations of t_{plh} and t_{phl} are used to indicate the propagation delay for a low to high transition and a high to low transition of a waveform, respectively.

Reference Zero Delay

Reference Zero Delay is the JEDEC term for the effective PLL buffer delay. This parameter is also referred to as Static Phase Offset (or SPO). The JEDEC notation is t_{ϕ} . The value of SPO is defined as the average difference in phase between the input reference clock and the feedback input signal, when the PLL is locked. The value of the Reference Zero Delay can be compensated for by including PC board trace delay in the feedback path of the PLL. Specially constructed PLL clock drivers called Zero-delay Buffers make use of this occurrence and can produce a clock edge at the output that is exactly in phase with the input.

Skew

Clock fanout buffers and PLL clock drivers with built-in fanout buffers offer multiple outputs. These clock outputs are routed across a PC board to various devices. A typical fanout buffer may have as many as 18 to 20 clock outputs. Typically, these

outputs are designed to drive a 50 ohm cable or a 50 ohm PC board trace. Ideally, all of the outputs are timed such that clock edges on each output switch at exactly the same time. However, real life devices do not. Small amounts of skew exist between the high to low or low to high transition on one output as compared to another output. For systems that require synchronization between data and clocks or multiple clocks on the PC board, this skew is a bad thing. Clock integrated circuit designers try to minimize the amount of skew in a device. However, skew does exist and the device data sheet usually specifies the amount of skew.

This output skew is typically defined in three ways: output-to-output, process, or part-to-part skew.

Output-to-output skew is defined as the skew between the various output edges on a single device. Process skew is defined as the skew between the same output pin on two different devices. Finally, the part-to-part skew is defined as the skew between any output on two different devices. Figure 5 illustrates output skew types for both single-ended and differential output waveforms. Typically, both output-to-output and part-to-part skew are specified on a data sheet. The JEDEC specification states that the skew values are to be determined with the outputs driving identical specified loads.

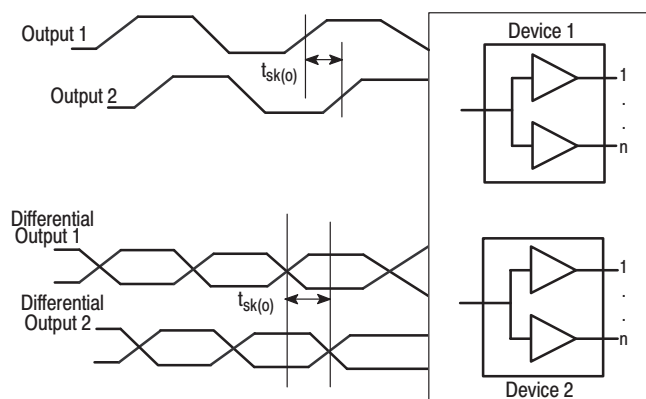


Figure 5. Output-to-Output Skew

Jitter

Jitter is a deviation of the edge location on the output of the clock buffer. As with skew, jitter is a bad thing and is usually measured in picoseconds. There are three categories of jitter that are of interest: cycle-to-cycle, period, and phase jitter.

Cycle-to-cycle jitter is the difference in the period of any two adjacent clock cycles. The difference is reported as an absolute value according to the JEDEC specification. However, quite often a $\pm$ value is used. The JEDEC symbol for cycle-to-cycle jitter is $t_{jit(cc)}$. Cycle-to-cycle is usually measured over some large sampling of cycles and specified as the maximum difference. Figure 6 shows the measurement and calculation of cycle-to-cycle jitter.

In PLL based systems, the value of the cycle-to-cycle jitter is usually small since the PLL does not quickly respond to changes on its input. Since cycle-to-cycle jitter is the difference in the period from one cycle to the next, this jitter is at the clock frequency. This jitter is also referred to as short term jitter.

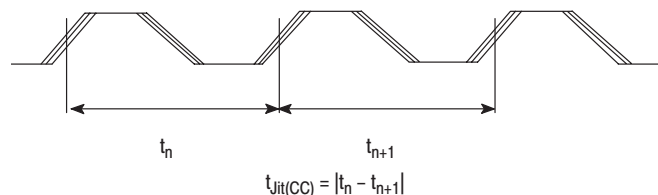


Figure 6. Cycle-to-Cycle Jitter

Clock integrated circuits have an inherent jitter generated within the device. In addition, external sources contribute to this jitter. Specifically, power supply noise may be a source of jitter in both PLL based and non-PLL based clock driver devices. Power supply design, power supply filtering, and board layout contributes to the overall jitter values measured on the output of the clock device.

The second type of jitter is period jitter, which is defined in the JEDEC specification as the deviation in cycle time of a signal with respect to an ideal period. Figure 7 shows the definition and calculation of period jitter. This jitter type is reported as an absolute maximum value as measured over a long time period. The JEDEC symbol for period jitter is $t_{jit(per)}$. The long time period varies from measurement system to measurement system. Typical time periods are 64 microseconds which, at a frequency of 100 MHz or so, yields many (6400) clock cycle period values. This type of jitter represents the random movement in the instantaneous output frequency or output period of the clock source.

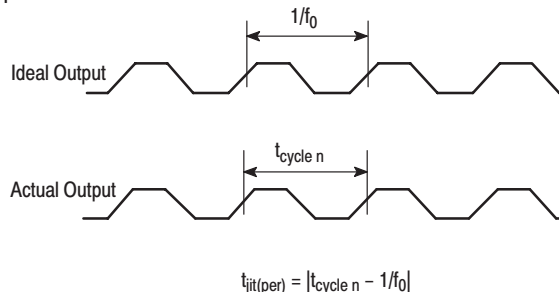


Figure 7. Period Jitter

The last jitter type covered is that of phase jitter. Phase jitter is associated with PLL based clock drivers. The JEDEC specification notation is $t_{jit(\phi)}$. This value represents the input to output jitter associated with a PLL clock driver. The value is given as an absolute value of the range or variation in the difference between the phase of the reference input and the phase of the feedback input to the integrated circuit. (See Figure 8)

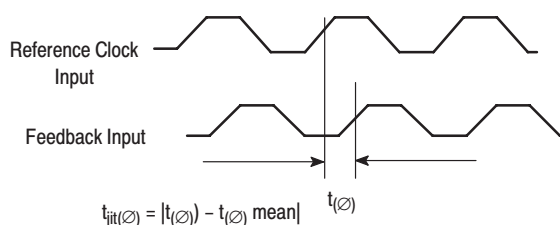


Figure 8. Phase Jitter

Jitter Values and Data Sheets

Definitions of the various types of jitter and the equations for calculating the values are necessary for an understanding of

jitter and how it relates to a clock design. However, another important factor in understanding clock drivers is the metrics and methods used of the published specifications. These metrics may vary from manufacturer to manufacturer and also within a manufacturer's clock driver offering. The values may be given as RMS values or as a peak-to-peak value. They may be listed as typical or as actual maximum values. Understanding of the background of the jitter values on a data sheet are necessary for circuit design as well as comparing clock driver devices.

Jitter measurements, whether cycle-to-cycle period or phase, are measured over some large number of samples. The data for a typical device, when plotted, represents a classic distribution Gaussian or bell shaped curve where most of the clock cycles are close to the ideal frequency (in the case of period jitter) with fewer and fewer devices having increasing deviation from the ideal period.

In classical statistics, the distance from the center of the Gaussian curve is defined in values of standard deviation or sigma; and the higher the sigma multiplier, the higher the confidence level is that a device will not exhibit a jitter value greater than a predefined amount.

Data sheet specifications that list RMS values imply a 1 sigma deviation above the mean and 1 sigma deviation below the mean or a total of 2 sigma confidence level. Table 1 lists these confidence factors for ± 1 sigma through ± 6 sigma. If data sheet values are specified as RMS values and higher levels of confidence are desired, then the data sheet values for jitter must be multiplied by the desired confidence factor.

Figure 9 shows the Gaussian distribution curve and sigma points for a device with an output frequency of 400 MHz (period of 2.5 ns). A value of ± 3 sigma or 6 sigma gives a confidence level or a probability that the clock edge is within the distribution of 0.9970007%. The ± 3 sigma limits define the upper period limit of approximately 2.52 ns and the lower period limit of approximately 2.48 ns.

Figure 10 shows actual measurements made for the period jitter of a 400 MHz clock device.

In this example, the mean period is 2.49921 ns (approximately 2.5 ns) with the standard deviation being 6.48 ps and the peak-to-peak jitter being 57 ps. This data was captured with a sample size of 13100 samples.

Table 1. Confidence Factor

Sigma	Value	Confidence Factor
± 1	(2 sigma)	0.68268948
± 2	(3 sigma)	0.95449988
± 3	(6 sigma)	0.99730007
± 4	(8 sigma)	0.99993663
± 5	(10 sigma)	0.99999943
± 6	(12 sigma)	0.99999999

RMS values for jitter look better on the data sheet than peak-to-peak. However, peak-to-peak values may be needed for clock jitter analysis. If RMS values are specified, peak-to-peak values may be derived based upon the required system reliability for the specific applications. If the other cases where peak values are specified, these values may be used directly. However, the question that must be asked in order to use the manufacturer's peak-to-peak values is what level of uncertainty is being specified. These parameters may be specified differently on each manufacturer data sheet. Therefore, care must be taken to insure that when one is comparing values, the values are specified and measured in a similar fashion.

The above discussion assumes the jitter measurements have the classic Gaussian curve or statistical distribution. This would be the case if the jitter is completely random. However, clock driver devices may have internal mechanisms that produce jitter that deviates from the classic bell curve. In this case, the total jitter is composed of the addition of a series of bell curves providing a more complex distribution. With care, the terms of RMS and the various sigma levels may still apply.

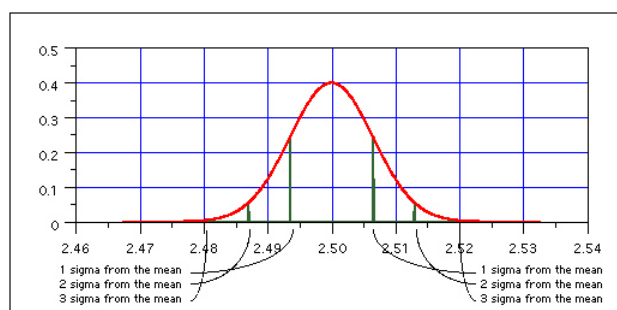


Figure 9. Classic Gaussian Distribution Curve

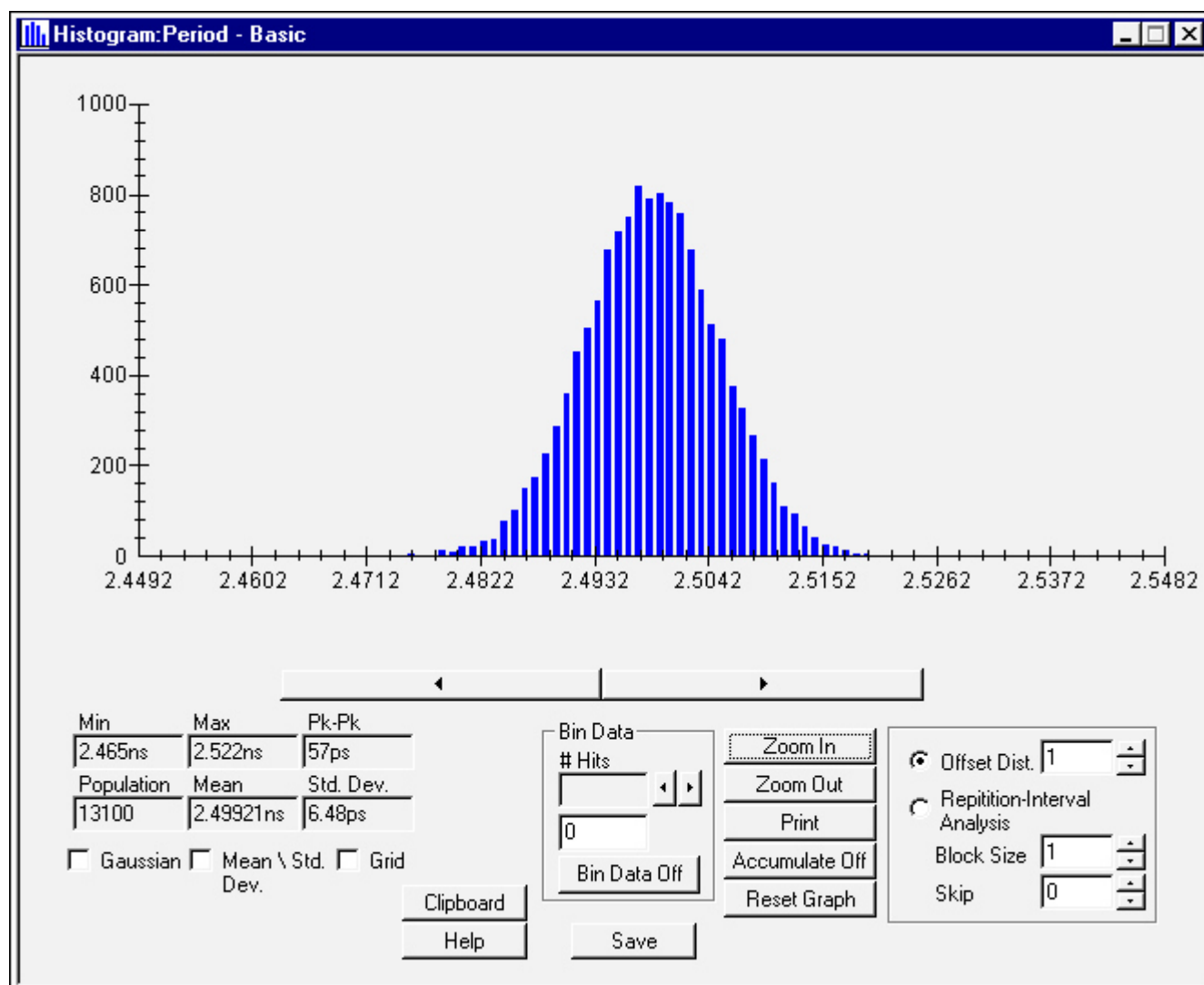


Figure 10. Period Jitter for Typical PLL Clock Device with $F_{OUT} = 400$ MHz

PLL Bandwidth and Jitter

The PLL based clock driver locks on to a reference frequency and maintains an output frequency based upon that reference frequency. If the reference frequency changes, the PLL attempts to follow the change in the reference frequency. However, if the change is faster than the PLL can follow, the PLL based clock driver acts as a low pass filter and ignores or effectively filters out the higher frequency changes on its input. As with any low pass filters, the PLL has a cutoff frequency, or bandwidth, associated with it. This bandwidth becomes important to our clock tree design. High frequency noise and jitter will not pass through the PLL.

The actual bandwidth of the locked PLL is dependent on many factors, including the feedback divider ratio. The higher the divide ratio, the lower the bandwidth. Thus, those PLL clock

driver devices that have selectable feedback divide ratios will have varying bandwidth values. Bandwidth may or may not be specified by the PLL clock driver manufacturer. If not specified, the information is usually available on request.

Figure 11 is a typical PLL frequency modulation bandwidth waveform. Note the cutoff frequency is about 300 kHz. As mentioned before, the cutoff frequency will vary with a change in the divide ratio in the feedback loop. Bandwidths of PLL-based clock drivers vary from low values of a few kHz to higher values of a MHz or more depending upon the intended application of the device. Clock synthesizers typically have the lowest bandwidth. Bandwidths of these devices are in the order of 30 to 50 kHz. Clock generators are next with bandwidths of a few hundred kHz. The devices with the highest bandwidth are the Zero-Delay-Buffers. The bandwidths of these devices are typically a MHz and above.

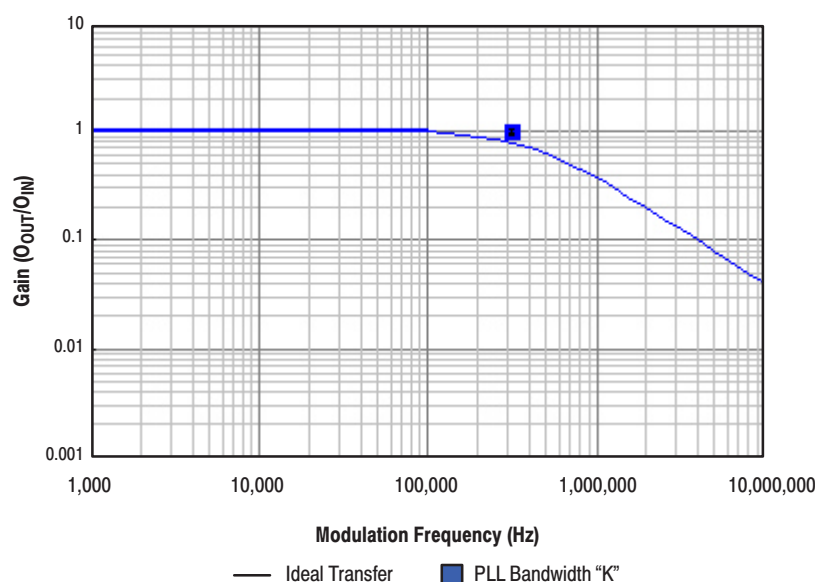


Figure 11. PLL Bandwidth

Clock Tree Application Example Analysis

Figure 12 shows an example clock tree application which is used to show the effects of skew and jitter in a system. The goal of this design is to provide multiple phase aligned HSTL and LVCMOS outputs. The reference for this clock tree is a crystal oscillator while the outputs of the tree provide both HSTL and LVCMOS to various system locations. The tree starts with a crystal oscillator in the MC12430 integrated circuit. The MC12430 is a PLL based clock synthesizer that allows very fine control of the output frequency in 1 MHz steps.

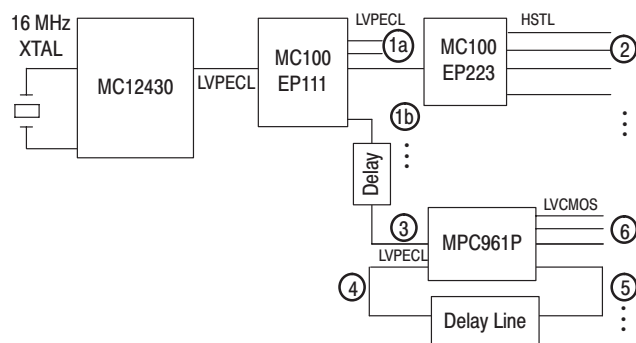


Figure 12. Example Clock Tree

The LVPECL output of the MC12430 drives the LVPECL input to the MC100EP111 fanout buffer.

The MC100EP111 consists of 10 LVPECL differential pairs of which one pair is connected to a MC100EP223 input and another pair connected to the MPC961P input. The MC100EP223 fanout buffer provides HSTL outputs while the MPC961P is a PLL-based clock generator that provides several LVCMOS outputs. Notice there is an introduced delay from the LVPECL output of the EP111 to the LVPECL input of the MPC961P zero-delay buffer. This introduced delay is due to backplane or cable distance which will skew the LVCMOS outputs to later than the HSTL outputs. To compensate for this delay, the MPC961P zero-delay buffer is used in conjunction with a PC board delay line in the feedback path.

Figure 13 provides an analysis of the example clock tree for the situation where we have no (or choose to ignore both) jitter and skew in the devices. Later, in Figure 14, an analysis with both jitter and skew is shown. The circled numbers in Figure 12 are used as reference points on the clock analysis waveforms.

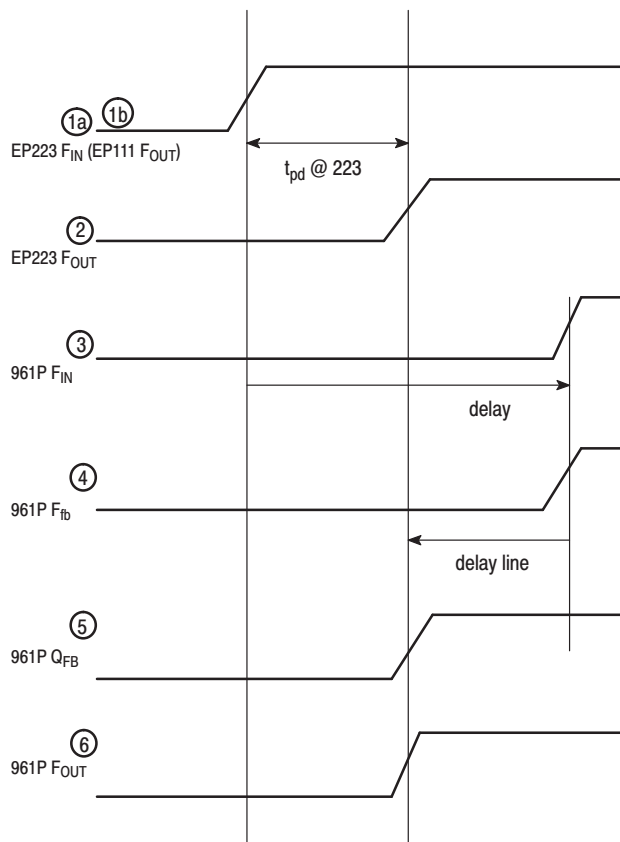


Figure 13. Example Clock Tree Analysis without Jitter and Skew

The first analysis of the clock tree is with the assumption that there is zero output-to-output skew and zero jitter. With zero skew between the outputs of the MC100EP111, the signals 1a and 1b are identical. The waveform at point 2 is delayed due to propagation delay, t_{pd} , of the MC100EP223.

The waveform at point 3 is delayed due to the delay associated with the backplane or cable distribution. By using the MPC961P zero-delay buffer and placing the appropriate trace delay in the feedback path of the PLL, we can compensate for the backplane trace and bring the waveform for points 5 and 6 back in line with the output of the MC100EP223.

Next, we will do the same analysis but we will include the output skew on the MC100EP111, the MC100EP223, and the phase jitter for the MPC961. (See Figure 14.)

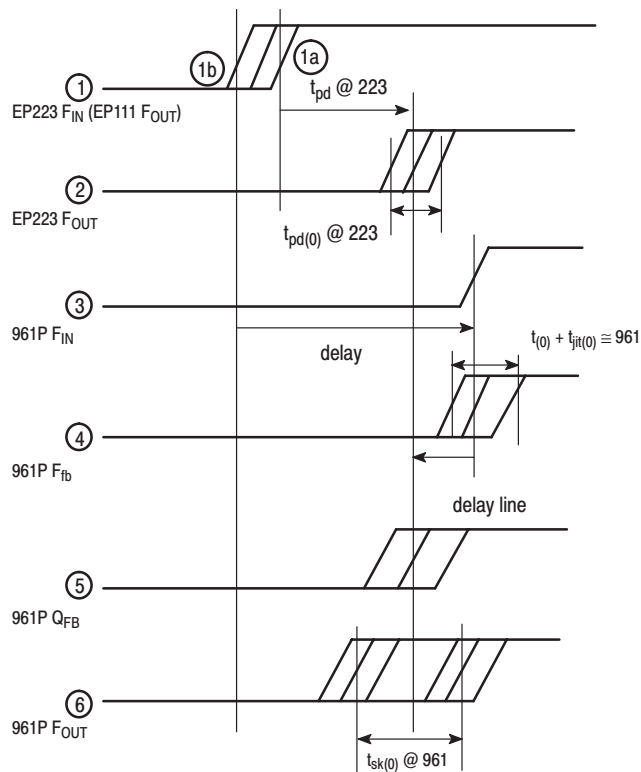


Figure 14. Example Clock Tree Analysis with Jitter and Skew

Initially, we have the output-to-output skew for the EP111. We will assume that the output connected to the MC100EP223 is the slowest and thus the longest delay output and that the output connected through the delay line to the input of the MPC961C is the fastest or shortest delay output. This analysis must also be done for the opposite situation; where the MPC961P is connected to the slowest output and the MC100EP223 is connected to the fastest output.

The waveform at point 2 is delayed from point 1a by the propagation delay, t_{pd} , of the MC100EP223 as we had in Figure 13. However, by including the output-to-output skew for the MC100EP223, we find uncertainty in the location of point 2 as shown in the waveform of point 2 of Figure 14.

Point 3 shows the waveform arriving at the input to the MPC961P. Point 4 is the feedback input to the MPC961P and, in the ideal case, is exactly the same as point 3. However, in this situation, we have the uncertainty caused by the combination of the static phase offset, t_{ϕ} , and the phase jitter for the MPC961P. Figure 14 depicts these two values added together. The waveform of point 5 now moves back in time due to the delay line in the feedback path of the PLL such that the nominal output now coincides with the HSTL outputs of point 2. Point 6 shows the added uncertainty of the outputs due to the output-to-output skew from the MPC961P. Note that Figure 14 is not to scale and the magnitudes of the skew and jitter are actually much smaller than indicated.

Table 2 lists the skew and jitter values for the 3 devices used in the example. The MC100EP111 has a specification for output-to-output skew. The MPC961P has parametric values for Static Phase Offset, phase jitter and output-to-output skew. The MC100EP223 has values for propagation delay and output-to-output skew.

Table 2. Confidence Factor

Device	Parameter
MC100EP111	tsk(o): 70 ps
MPC961P	t _(o) : -50 to 225 ps t _{jtt(o)} ΔF ~ 100 ps t _{sk(o)} ΔF @ 150 ps
MC100EP223	t _{pd} : estimated 700 ps t _{sk(o)} : estimated 50 ps

A similar analysis can be done for the case where the MC100EP111 outputs connected to the MC100EP223 and MPC961P are reversed in time. Thus, the MC100EP111 output connected to the MC100EP223 is the fastest and the output connected to the MPC961P is the slowest.

One last comment on the example is that the jitter associated with the clock source, MC12429, was not mentioned in the

analysis. This value was ignored for this example due to the fact that all of the clock outputs are derived from the same source, and jitter that occurs on one output would show up on all outputs. Applications that have clock outputs derived from different sources, or have the clock source compared to a frequency standard, would mandate the need to include the source jitter in the analysis.

SUMMARY

Skew and jitter are real characteristics of clock driver devices and may or may not be of importance to a clock tree design. Understanding data sheet values and applying this knowledge to clock tree design can sometimes be a real challenge. With a bit of analysis, one can determine which parameters are critical to a specific clock tree design and be able to compare the values of these parameters from one device/vendor to another. Lastly, data sheet values of jitter are often measured in a lab environment under the best of conditions. Real designs with clock drivers on PC boards with other digital circuitry, noisy power supplies, long traces, and other clock sources can make the overall jitter worse. Careful design practices are a must for the best clock driver design.

AN1939

Clock Driver Primer — Functionality and Usage

Prepared by: Don Aldridge and Tom Borr
November, 2001

ABSTRACT

This application note focuses on the fundamentals of clock drivers, including definitions, applications, and characteristics of integrated devices. This application note is intended for the system designer that is tasked with creating a clock source for a microprocessor-based system. Although the clock may be a small portion of the system schematic, its design becomes a fundamental contributor to the overall system performance.

INTRODUCTION

Tucked away in the corner of a complex microprocessor PC board is the clock source that provides the timing for the entire PC board. This clock source may be simple or it may be complex. It may only consist of a crystal, a couple of integrated circuits, and some traces on the PC board. It may also be very complex with many clock outputs, zero-delay buffers and precise timing delays that are built into the PC board. This application note covers the basics of a clock tree design for

microprocessor applications. These basics include the definitions of terms used in clock driver applications, how Phase Locked Loops (PLL) work, what makes the basic PLL into a clock driver, what distinguishes one clock driver from another, and how to select the appropriate devices for a specific application. Also, this application note covers a few of the clock tree design “gotchas.”

Applications for clock trees abound in the electronics for telecommunications and computer systems. The system requirements are for clocks of several megahertz to hundreds of megahertz. There are many common frequencies that need to be generated based upon the application for the clock. Frequencies of 33 MHz, 66 MHz, 100 MHz, and others are common in most applications. Figure 1 shows two clock trees. A simple clock tree on the left that has a crystal input of 16.66 MHz and a 200 MHz output, but is selectable from 25 MHz to 400 MHz. The clock on the right is more complex, with 16 MHz as its input, and provides as its output several clock outputs of varying drive levels. To compensate for the delay in routing the clock across a backplane or PC board, a zero-delay buffer is used to provide a clock with aligned edges.

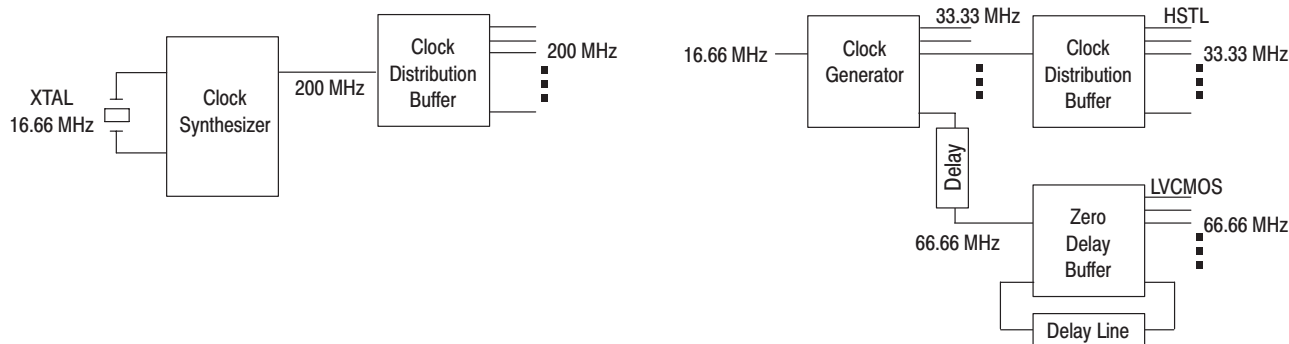


Figure 1. Typical Clock Trees

PLL CLOCK DEVICES

9

The Basic Phase Locked Loop

A phase locked loop or PLL is one of the fundamental elements of clock drivers. Although PLLs get used in many different electronic circuit applications, their usage in clock driver circuits dictate certain unique characteristics. It is not the intention of this application note to have complete coverage of phase lock loops. However, the fundamental operation of the PLL circuitry for clock driver applications is covered.

A phase locked loop has, as its input, a clock frequency source of which the PLL locks on to and produces, as its output, another clock signal. The output clock may be at the same

frequency as the input or at some multiple of the input frequency. If the input clock should change in frequency or phase, the output clock follows this change.

A basic PLL clock architecture consists of a phase detector, a low pass filter, and a voltage-controlled oscillator or VCO, which are connected as shown in Figure 2. In addition to these blocks, the PLL has a frequency divider network which, in Figure 2, is called the M divider. This divider network is connected between the output of the VCO and one of the inputs of the phase detector. The other input to the phase detector is the reference frequency to which the PLL is to lock. The output of the PLL is F_{OUT} , which is the clock that is distributed throughout the clock tree system.

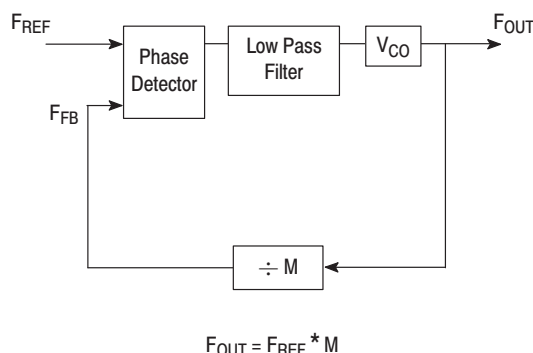


Figure 2. Basic Phase Locked Loop (PLL)

The phase detector has two inputs which are compared and used to produce a correction or error signal based upon the difference in the phase of those two inputs. One of these inputs is the previously mentioned reference frequency. The other input is the feedback signal from the VCO/divider network.

The PLL correction signal, which is the output of the phase detector, is filtered and applied to the input of a voltage-controlled oscillator or VCO. This filtered correction signal sets the VCO frequency. The output of the VCO is applied to the M (or feedback) divider and becomes the second of the two inputs to the phase detector. When the loop is in “lock,” the two inputs to the phase detector are the same frequency and the same phase. This is due to the phase detector correction signal approaching zero and thus stabilizing the input control voltage to the VCO. The VCO output frequency, or F_{OUT} , becomes the reference frequency multiplied by M and continually tracks the reference frequency. The equation for F_{OUT} is the reference frequency multiplied by M. If M is 1, then the output frequency is the same as the input reference frequency.

By changing the value of M, the VCO frequency changes in increments of the reference frequency. Thus a lower reference frequency input can be multiplied up to the desired output frequency.

The VCO has a limited frequency range over which it can operate. The input frequency multiplied by the feedback divide value must produce a frequency that is within the allowable range of the VCO. If this condition is not met, the VCO is considered to be “railed” high or “railed” low and the PLL is no longer in lock.

Basic PLL Clock Driver

Figure 3 depicts additions to the previous basic PLL Clock Architecture circuitry, which creates a multi-frequency and multi-clock distribution source. The more complex divider

network on the output of the VCO provides the M divide value for the feedback path to the input of the phase detector and also divides down the VCO frequency to the desired system frequency or frequencies.

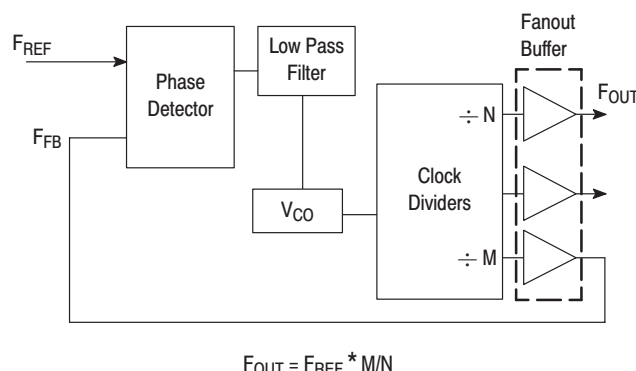


Figure 3. PLL Based Clock Generator

The outputs from this example clock generator provide multiple outputs and multiple frequencies for distribution in the application. Fanout buffers are included for each output to provide the required system drive. Also, if the device has a special feedback output, then an equivalent fanout buffer is included for the feedback path. The feedback connection may be external to the device, and this buffer equalizes the delay through the main clock outputs. By incorporating the M divider with the output dividers, the phase relationship is known between the input reference clock and the output clock(s). Also, both the feedback divider and the output divider(s) may be selectable; this allows the user to adjust the output frequency or frequencies.

Later in this application note, we will discuss how the external feedback path may also include some PC board trace delay. Design of this external trace delay allows the phase of the output clock to be aligned forward or backward (relative to the input clock phase).

A Look at an Actual Clock Driver – MPC9351

Next, let's look at an actual clock driver. Figure 4 is the block diagram of a typical clock driver, the MPC9351. This device has a PLL block which contains the phase detector and VCO. The input to the MPC9351 can be either a differential clock on the PCLK and ~PCLK inputs or on the single ended input TCLK. The MPC9351 has a total of nine LVCMOS level outputs for system clock usage.

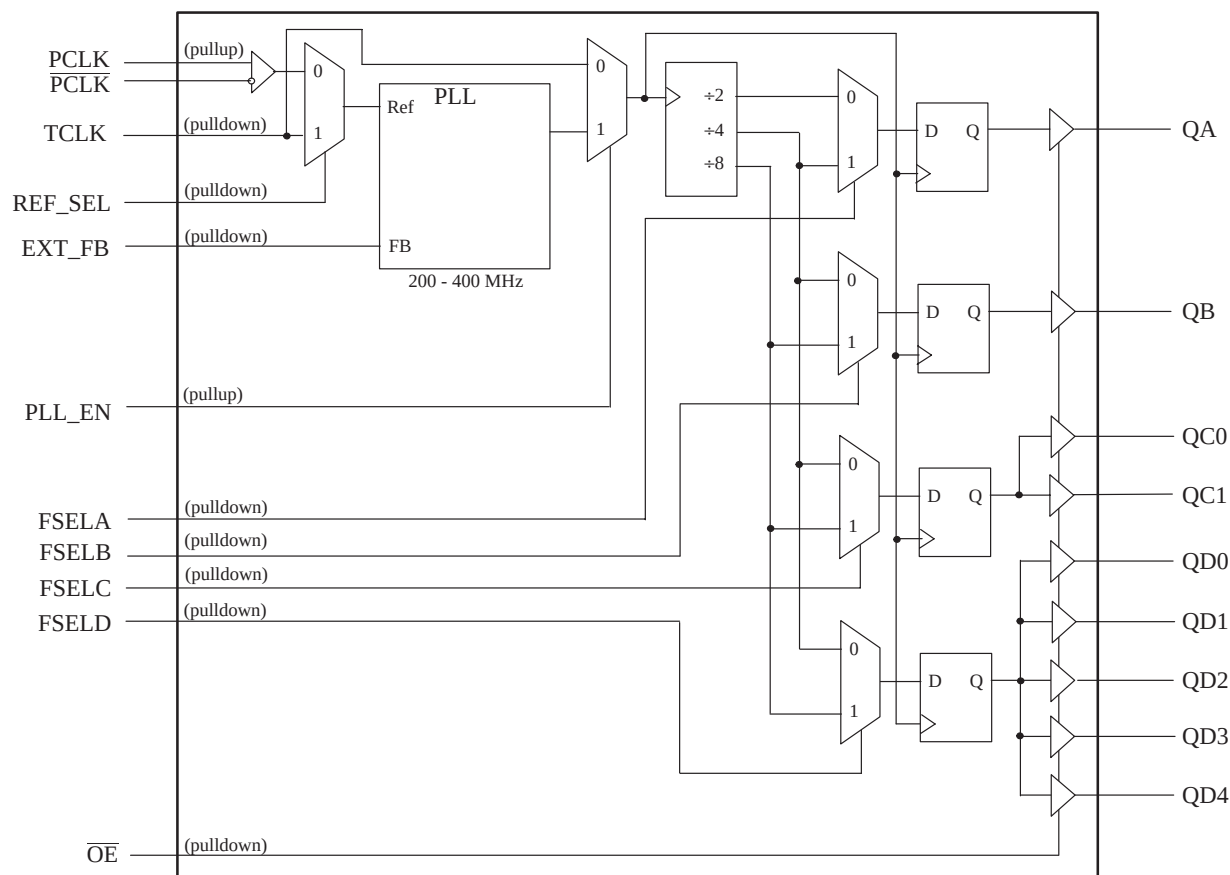


Figure 4. MPC9351 Clock Generator Block Diagram

Of special interest is the divider network and output circuitry. The VCO output of the MPC9351 is available through four banks of outputs where each bank of outputs has a selectable divide value. The first bank of outputs (labeled QA) consists of a single output. This output may provide a clock output frequency of the VCO frequency divided by either 2 or 4. The second bank of outputs (labeled QB) also consists of a single output which can be at the VCO frequency divided by 4 or 8. The third bank of 2 outputs (labeled QC0 and QC1) has the same selectable divide values of 4 or 8. Lastly, the fourth bank has four outputs (labeled QD0 – QD4) with the same divide by either 4 or 8. Although this clock driver does not have specific outputs for the feedback, typically one of the QD outputs would be used for the feedback input to the PLL. The FSELA through FSELD inputs are used to select the output divide ratios for each of the four banks.

A typical connection of the MPC9351 is shown in Figure 5. Here, a 33.33 MHz input frequency is multiplied by the feedback divide value of 8 which produces a VCO frequency of 266 MHz. This is in the allowable range of the MPC9351 VCO. The 266 MHz VCO frequency is then divided by 2 for the QA output to produce 133 MHz. Separately, the 266 MHz VCO frequency is divided by 4 for the QB output. Likewise, the 266 MHz VCO is divided by 4 for the QC outputs. This provides one clock output at 133 MHz, four clock outputs at 66.66 MHz, and four clock outputs at 33.33 MHz.

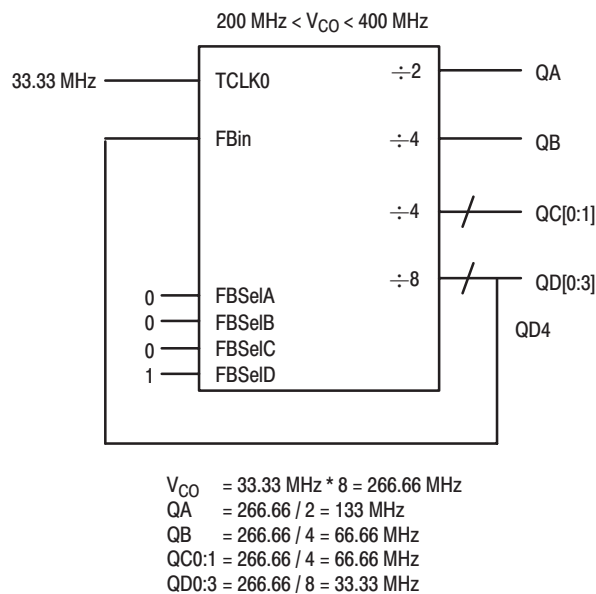


Figure 5. MPC9351 Clock Generator Application

Clock Drivers—The Differences

The Motorola Advanced Clock Driver Selector Guide (SG392) has over 30 PLL clock driver devices. Each of these devices is similar in functionality but each is unique in features and the specifics of their functionality. These devices differ in the number of outputs, how the outputs are divided into banks, what feedback divider ratios are offered, and whether the device has crystal oscillator circuitry or uses an external reference input. The devices differ on whether they have differential or single-ended outputs, the frequency range of the VCO, the output duty cycle, and whether the device has an input divider for the reference. Also, the AC electrical specifications of jitter, skew, and bandwidth vary from one device to the next. The next few sections discuss some of these characteristics.

Outputs

Typically, a clock driver output is used to deliver a timing signal source to a single location in a design. If multiple locations require clock signals then multiple outputs are used. This simplifies the electrical design and the PC board design. For example, the usage of individual clock outputs eliminates the requirement of matching PC board trace lengths and worrying about trace stubs that one would have to consider when routing a single clock output to many different locations of a PC board.

Application requirements of multiple outputs result in clock drivers with different numbers of outputs. Some devices have a few outputs while others have as many as 21 individual outputs. In addition to the number of outputs, the grouping of these outputs into banks differ from one device to the next. Grouping the outputs into banks, with taps to the output divider at different values in the divider chain, allows the device to produce different output frequencies. Therefore, a device may be configured with one bank of outputs to provide a high frequency processor clock, a second bank to provide PCI clock outputs, and a third to provide specific frequencies associated with various I/O peripherals.

Input/Output Voltage Levels

The voltage threshold levels on the input and output of the clock driver differ from one clock driver to the next. Popular logic voltage levels are LVCMOS, LVPECL and HSTL. Also, the clock drivers may have one level for the input clock and a different level for the output clock. Some clocks offer a selection of input levels. For instance, a clock input selection pin would allow the user to select between a differential pair of LVPECL inputs or a single-ended LVCMOS input.

LVCMOS is usually used as a single ended input or output. It is specified at 3.3, 2.5, and 1.8 Volts. The voltage levels are compatible to many of the inputs to microprocessors, FPGA or ASIC devices, and peripheral devices. LVCMOS is specified in JEDEC specifications EIA/JESD36 and 80.

LVPECL is typically used in differential input and output signaling. It is the low voltage, 3.3 V, version of the 5 V PECL logic specification. (PECL is the positive level specification for ECL logic.) The signal swing is approximately 600 mv and is centered at 1 volt below the supply voltage. The differential nature of LVPECL offers advantages over single ended levels. These advantages are discussed later in this application note.

The logic level specification of HSTL stands for High Speed Transceiver Logic. It is specified in EIA/JESD8–6 and is titled “A 1.5 V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits.” It may be used as a single-ended logic interface but is more commonly used as a differential signal. HSTL has a differential voltage value V_x and common mode voltage V_{cmr} .

Figure 6 shows the output levels for LVCMOS, LVPECL, and HSTL. For the LVCMOS clocks, the voltage levels of 3.3, 2.5, and 1.8 are shown with the output drive levels as taken from the JEDEC specifications. Other JEDEC specifications also specify LVCMOS drive levels; however, the specifications shown here have the capability of driving 50 ohm transmission lines as would be used in clock distribution.

VDDQ	_____	_____	_____
VOH	-----	-----	-----
VOL	-----	-----	-----
GND	_____	_____	_____
LVCMOS		LVPECL	HSTL
VDDQ = 3.3	2.5	1.8	VDDQ = 1.5
VOH = 2.0	1.8	1.6	VOH = VDDQ - 0.5
VOL = 0.55	0.6	0.2	VOL = 0.5
VTT = VDDQ/2	VDDQ/2	VDDQ/2	VTT = VDDQ/2
I = 24 ma	8 ma	100 μ a	I = ma

Figure 6. Logic Levels

AC Characteristics – Skew and Jitter

Two important, but often misunderstood, characteristics of clock drivers are output skew and jitter. Output skew is the difference in the timing of coincident edges between outputs for multiple outputs of a clock driver. Jitter is a deviation in the frequency or period of the output clock from the specified frequency or period.

There are three different types of skew defined per the JEDEC specifications. Output-to-output skew is defined as the skew between the various output edges on a single device. Process skew is defined as the skew between the same output pin on different devices due to process variation. Finally, part-to-part skew is defined as the skew between any output on two different devices. Figure 7 illustrates output skew types for both single-ended and differential output waveforms. Typically, both output-to-output and part-to-part skew is specified on a data sheet.

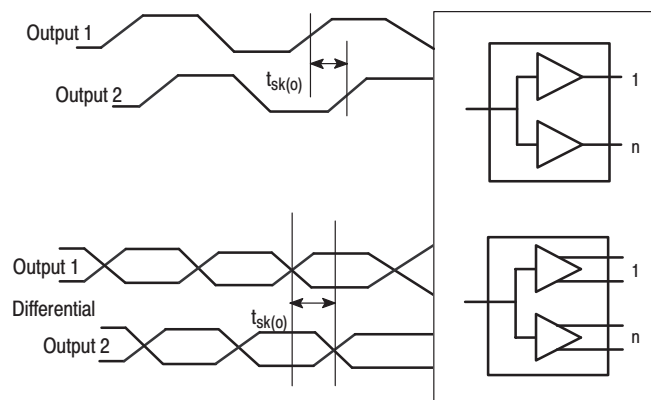


Figure 7. Output Skew

Jitter is a deviation of the edge location on the output of the clock buffer. There are three categories of jitter that are of interest: cycle-to-cycle, period, and phase jitter. One, two or all three may be specified on a clock driver data sheet. The first two are associated with both PLL and non-PLL clock drivers. The third, phase jitter, is only associated with PLL based clock drivers.

Cycle-to-cycle jitter is the difference in time between the periods of any two adjacent clock cycles. Period jitter is the deviation of time of individual periods of a signal with respect to an ideal period. Phase jitter represents the timing variation of the output with respect to the input associated with a PLL clock driver. Figure 8 shows the three types of jitter along with the associated mathematical definitions.

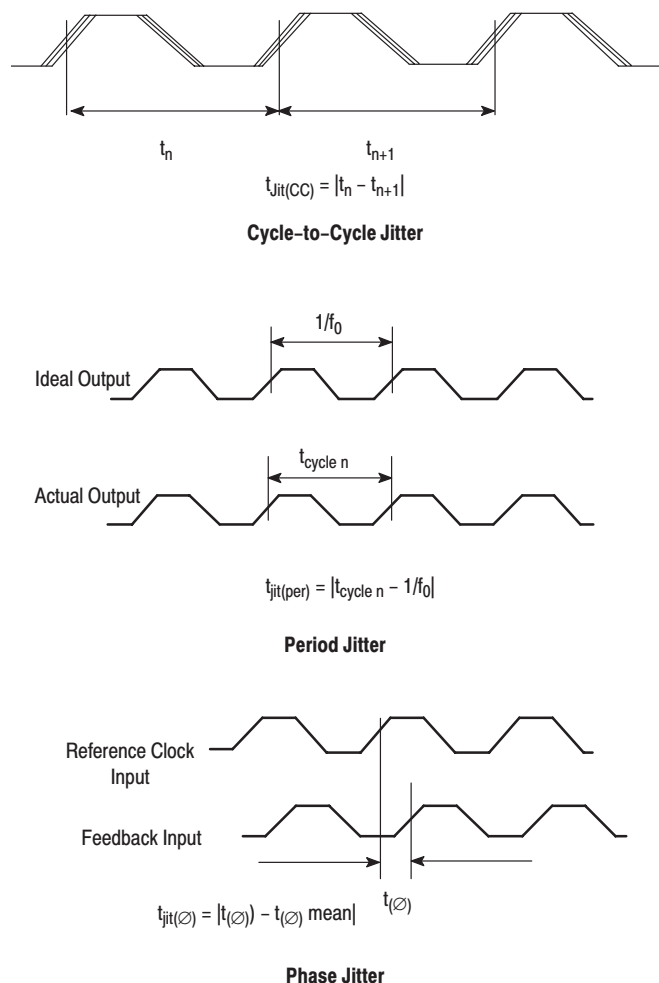


Figure 8. Clock Jitter

Additional details of skew and jitter may be found in the Motorola Application Note, AN1934.

AC Characteristics – Tracking Bandwidth

PLL clock drivers lock on to an input reference frequency and remain locked to that frequency. If that reference frequency varies, the PLL will follow that frequency and remain locked to the new input frequency. However, if the input frequency varies at a rate faster than the PLL can keep up with, then the output frequency will not track the input reference change and the PLL will appear to ignore the variation in the input frequency. The point that the PLL does not follow input frequency changes defines the upper bound of the PLL bandwidth.

The bandwidth of a PLL has a transfer characteristic much like a transfer characteristic of a lowpass filter. The bandwidth characteristic can be used to an advantage in certain clock applications. Higher frequency noise or jitter on the reference clock input can be filtered by this characteristic. Input jitter above the bandwidth will not pass to the output of the VCO while input jitter below the bandwidth will pass through to the output.

Bandwidth of the PLL clock driver varies based upon the actual design of the PLL. One of the components that affect the bandwidth is the feedback divide ratio. Figure 9 shows a typical PLL clock generator and its bandwidth curves. PLL clock

drivers that have selectable feedback divide ratios also have variable bandwidths. Higher divide ratios lower the bandwidth of the PLL clock driver.

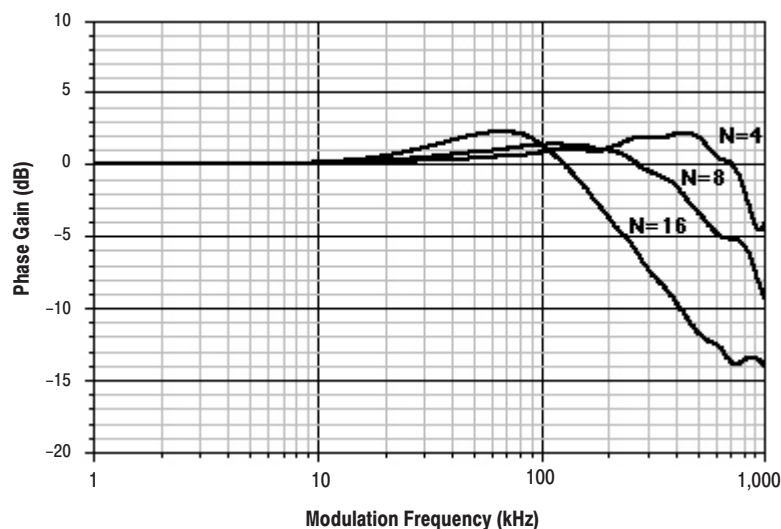


Figure 9. PLL Clock Generator Bandwidth

PLL Clock Driver Categories

Motorola PLL clock drivers are sorted into three different categories. The three categories are frequency synthesizers, clock generators, and zero-delay buffers. Although the categories are based upon the intended application, each category also reflects some uniqueness of the AC characteristics of the PLL.

Frequency Synthesizers

The first category of PLL based clock drivers is clock synthesizers. Clock synthesizers usually start with a low frequency clock source, which may come from an external source or from a crystal oscillator. This low frequency source may be further divided to produce an even lower PLL input reference frequency. With the use of the PLL, the low frequency

reference frequency is multiplied up to the desired output frequency. If the device has a crystal oscillator as a reference, the oscillator circuitry would typically be part of the IC circuitry with the only required external component that of a crystal.

The clock synthesizer usually has output frequency steps with fine granularity or resolution such as 1 MHz. The overall output frequency of the clock synthesizer may be as high as 850 MHz. Examples of Motorola clock synthesizers are MPC9229, MPC9230, and MPC9239. The MPC9229 and MPC9230 each start with a midrange clock source, typically 16 MHz. This input frequency is divided by 16, which then becomes a 1 MHz input reference to the PLL. A programmable feedback divider then effectively multiplies this reference to the VCO frequency. The VCO frequency is then divided to produce the desired output frequency, as shown in Figure 10.

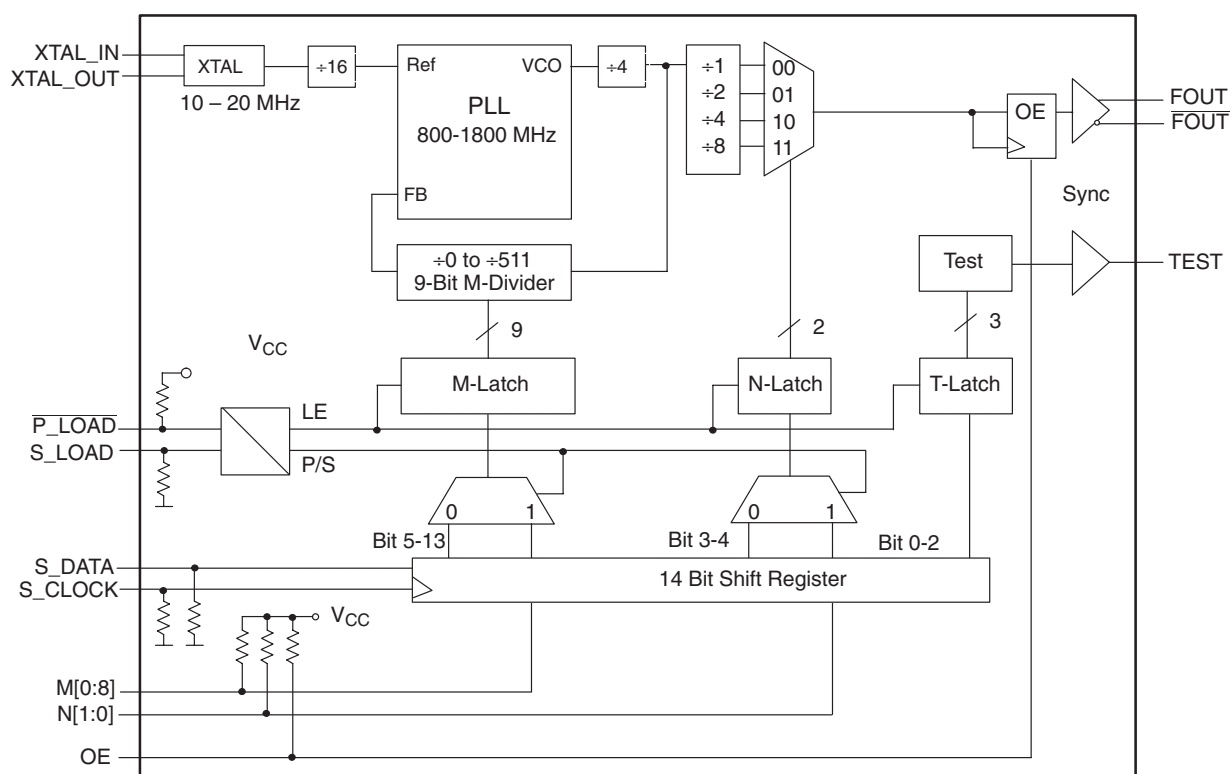


Figure 10. MPC9229 Frequency Synthesizer

A frequency synthesizer usually has a limited number of outputs; either one or two. The output frequency may be configurable in the user application. The ability to change the output frequency in small steps allows the circuit designer to do frequency margining. This is a technique where the system frequency is gradually increased/decreased while analyzing system performance.

The bandwidth of frequency synthesizers is usually the lowest of the three clock driver categories. Typical bandwidths for clock synthesizers are usually 30 to 50 kHz.

The clock synthesizer allows the system design to use a low frequency and low cost crystal oscillator and multiply the frequency up to the actual desired frequency, thus reducing the cost of the high frequency clock generation.

Clock Generators

Clock generators are used to generate clocks that are synchronous and phase aligned to an input reference clock. The category of clock generators make up the largest portion of Motorola's portfolio of the three categories of PLL based devices.

These devices typically have multiple outputs which are often grouped into multiple banks of outputs. Each bank can be set up for a different frequency. The previously discussed MPC9351 device is in the category of clock generators and, as we saw from the block diagram, it had nine outputs which were spread across four banks of outputs.

The output frequency adjustment step is usually more coarse than with the clock synthesizer. The reference frequency for a clock generator might be 15, 20, or 25 MHz, which would set the frequency step to a minimum of 15, 20, or 25 MHz. In some applications the previously discussed clock synthesizer might be used to generate the input clock for clock generators. Some clock generators have a crystal oscillator circuitry built-in.

The bandwidth of a clock generator is higher than that of a clock synthesizer and may be in the range of 300 to 500 kHz. This is considered to be a midrange bandwidth device. Clock generators maintain a phase relationship between the input clock and the output clock.

Zero-Delay Buffers

The third category of PLL clock drivers is zero-delay buffers. The concept of a zero-delay clock buffer for clock distribution may be a bit foreign, but with the use of a PLL, the concept is quite possible. The category of zero-delay buffers offers a higher bandwidth PLL than the clock generator category. Typical bandwidths are 1 to 2 MHz.

The zero-delay buffer maintains a known and precise phase relationship between the input and output clock waveforms. By adjustment of the feedback path delay, the output clock waveform may be aligned exactly to the input clock. This feedback path delay would typically be produced by the length of the PC board trace. Knowing the characteristics of the PC board material and the construction of the trace on the board can produce precise delays. Typical trace delays might be 1 to 2 ns per foot. Thus, a few inches of PC board trace can shift a clock output relative to the clock input by a significant amount. Figure 11 shows a zero-delay buffer and the equations that define the effective delay of the clock through the device. The parameter of $t(\phi)$ is the effective delay of the zero-delay buffer. The Load Trace Delay shown on one of the clock outputs is the normal trace delay that is produced by routing the clock across the PC board. The effect of this delay can be effectively eliminated with the use of a zero-delay buffer.

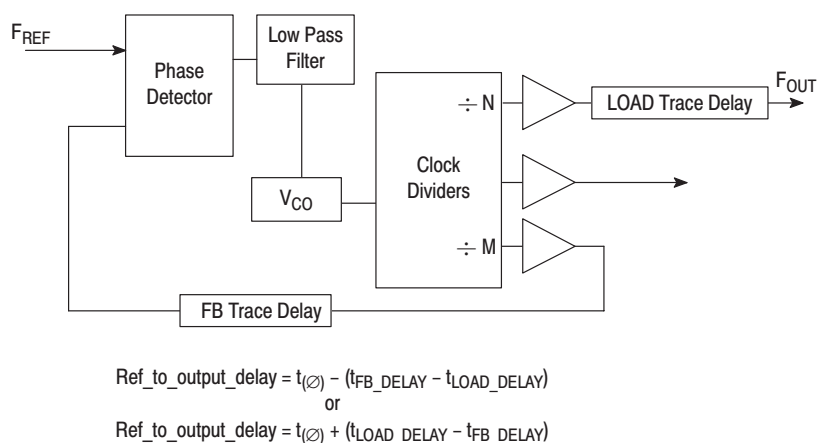


Figure 11. Zero-Delay Buffer

Although the zero-delay clock buffer is PLL based and shares many of the same characteristics with the clock generator, it typically has better jitter and skew performance.

Clock Distribution Buffers

In addition to the PLL based clock drivers, Motorola offers a number of devices classified as distribution buffers. There are two categories: LVCMOS single-ended output and differential clock output buffers.

Figure 12 shows two of the LVCMOS output devices. The MPC961C and the MPC961P have the same number of outputs

with the same output AC characteristics; however, they differ on the type of inputs. The MPC961C has LVCMOS inputs while the MPC961P has LVPECL compatible inputs. The devices can distribute an "at frequency" clock to many locations on a PC board. Some of these clock buffers offer a built-in divider block to be able to optionally divide the input clock by two. Care should be used when using this optional divider as a half frequency output can induce additional noise and thus cause jitter to the full frequency clock.

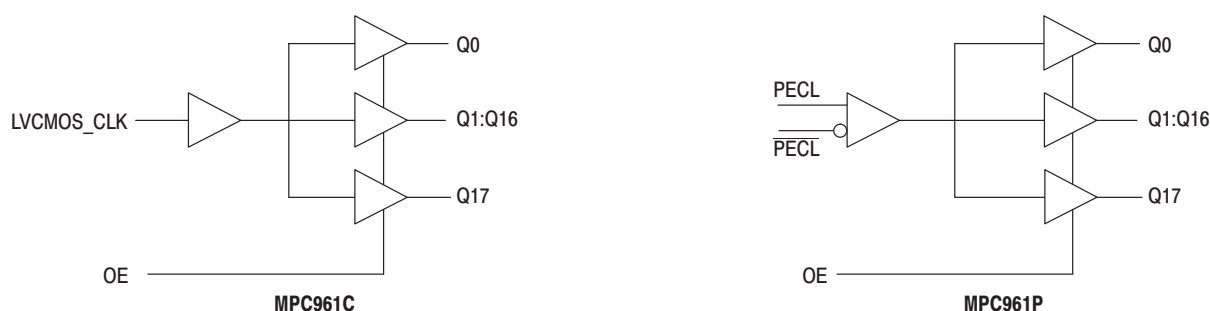


Figure 12. LVCMOS Clock Buffers, MPC942C and MPC942P

As previously mentioned, one of these categories of clock buffers have differential outputs. These outputs, and typically the input, are LVPECL or HSTL levels. Differential input and output signals offer many advantages as are discussed in the following section. An example of a differential output buffer is the MC100ES6111 differential clock driver shown in Figure 13. It has LVPECL inputs and 10 pairs of LVPECL outputs.

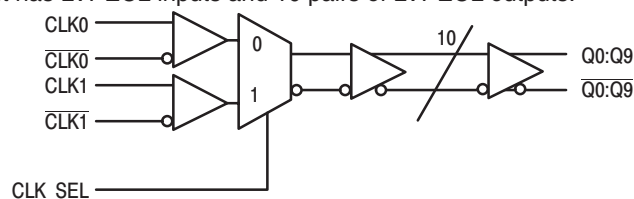


Figure 13. Differential Output Buffer MC100ES6111

Clock Redundancy

Some systems require a backup or redundant clock to be generated. Figure 14 shows two applications of a redundant clock system.

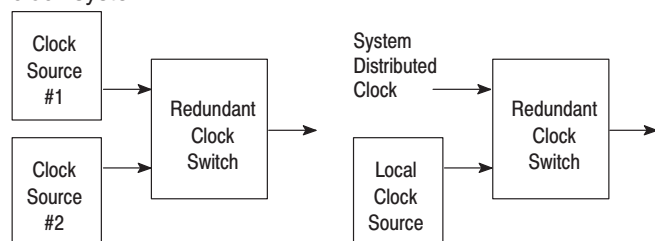


Figure 14. Redundant Clock Applications

The diagram on the left of Figure 14 shows a redundant main clock being sourced from two different central clock generation points and distributed over a cable or backplane. In this application, the redundant clock switch assures that a clock is available in the event of a removed clock board or a dead clock source.

The diagram on the right of Figure 14 shows a locally generated clock is available as a backup clock and must be switched in when the main clock fails. The redundant clock switch must make the transition from the current clock source to the backup clock in a smooth manner. While the transition takes place, the output of the clock generator must be stable with no disruption in the clock signal. The generation of runt pulses or short cycle clock periods must be avoided.

Motorola offers the MPC9993 Intelligent Dynamic Clock Switch as shown in Figure 15. The input clock sources come through the differential pair inputs of CLK0 and CLK1. The device automatically selects the good input and supplies this to the PLL. On detection of a clock failure, the device smoothly switches to the second input and continues to supply a clock to the PLL. A clock failure is defined as the input clock pins stuck high or low for at least one clock period. Status outputs from the Dynamic Switch Logic provide an indication of the current clock source.

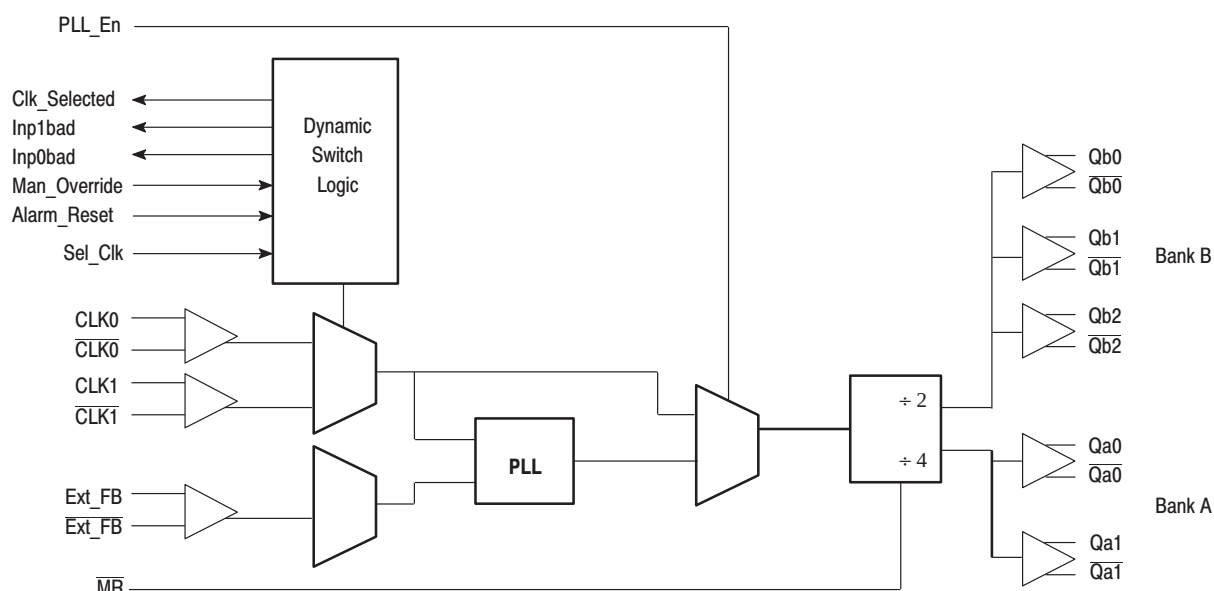


Figure 15. MPC9993 Redundant Clock Generator

The specification for the MPC9993 lists the maximum rate of period change as this clock switch is made. The data sheet also lists the typical delta period/cycle of 200ps/cycle. An actual clock switch may take as many as 100 to 200 clock cycles to complete. And as a result, the output will appear to be a “graceful” change from one clock source to the next. The automatic valid clock reference detection function may optionally be disabled and the clocks may be selected/switched manually.

The multiple outputs of the MPC9993 provide drive capability for several application system interfaces for the output clock as well as providing the feedback input to the PLL. The VCO for this device runs at 4X the input clock frequency. The outputs of

the MPC9993 are grouped into two banks. Bank A is the input clock divided by 4 and has two outputs. The output of this bank is typically used for the feedback to the phase detector. Bank B consists of 3 separate outputs and is the input reference divided by 2.

Figure 16 shows a possible connection for a redundant clock system using the MPC9993. The main clock reference comes externally from the system while the backup clock comes from a MPC9229 crystal oscillator based source. One pair of the differential Bank A outputs are routed back to the EXT_FB inputs. The remaining Bank A pair of outputs and Bank B outputs are available for system usage.

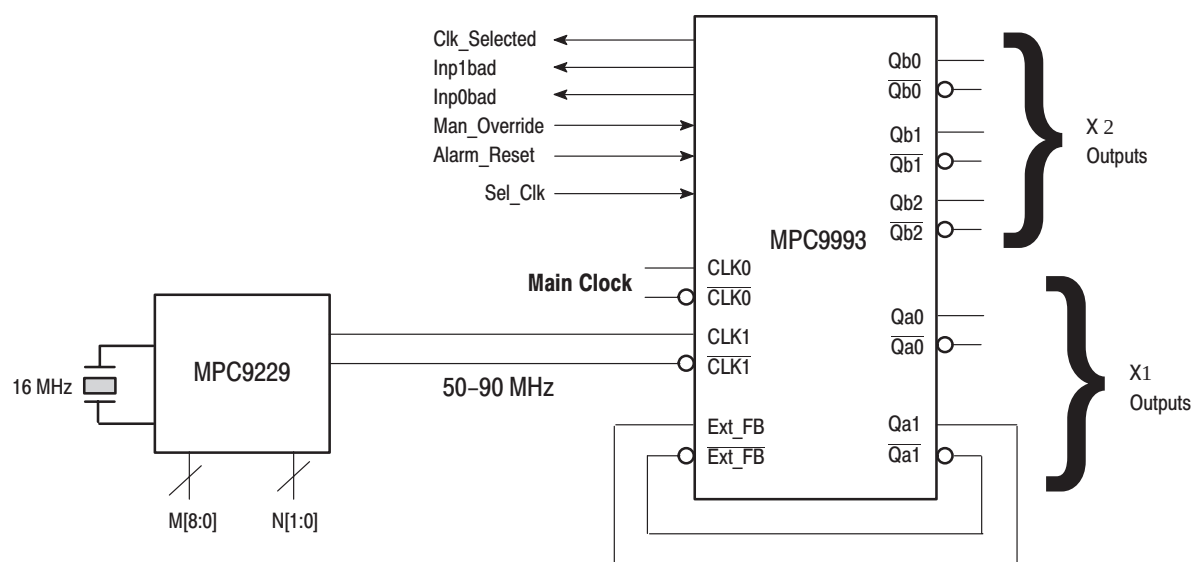


Figure 16. MPC9993 Redundant Clock Application

Figure 17 shows the “switchover” from the current clock to the backup clock. Clock A and Clock B represent the two available

clock sources. When Clock A fails, this triggers the switch to Clock B. The MPC9993 slowly slews to the phase of Clock B

and, after many input clock cycles, the output clock is in phase with Clock B.

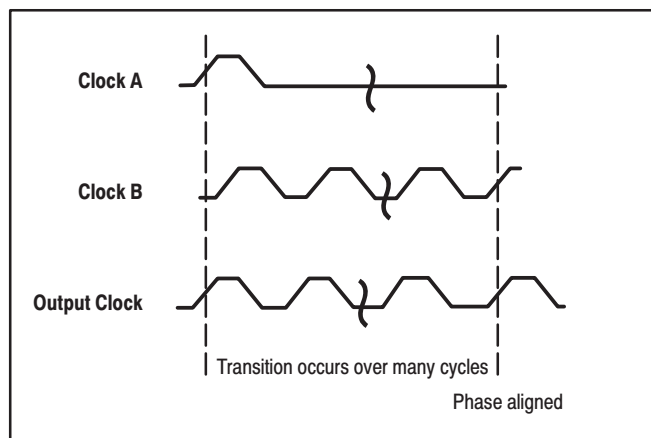


Figure 17. MPC9993 Clock Switch

Clock Tree Design and Layout

Clock performance can be predicted by understanding the clock functionality and data sheet parameters for jitter and skew, but the overall clock performance is highly dependent on design of the clock circuitry and its environment on the PC board. The following sections point out areas of clock design that need special attention to ensure the best clock performance obtainable from the design. The first of these topics is that of power supplies.

Power Supplies

Noisy power supplies have an affect on clock trees by generating jitter on the clock outputs. This is due to the noise on the power supply affecting the input-switching threshold and/or modulating the input control voltage to the VCO. Many of the Motorola clock generators offer separate PLL power pins, allowing for the isolation of the PLL power from the output driver supply. Use lots of high quality filter caps and (physically) place them as close to the clock driver package as possible.

Most of the PLL clock driver devices are analog devices. These drivers are designed with separate power supply connections for the outputs and the PLL analog circuitry. The example shown in Figure 18 separates out the analog supply, V_{CCA} , from the supply driving the rest of the chip. A simple RC filter decreases the noise injected into the analog supply pin, minimizing the jitter due to power supply noise. The value of R_S must be calculated based up the maximum I_{CCA} current. Filter caps should be of high quality for best overall frequency characteristics. Noisy power supplies may significantly compromise good clock tree designs on paper.

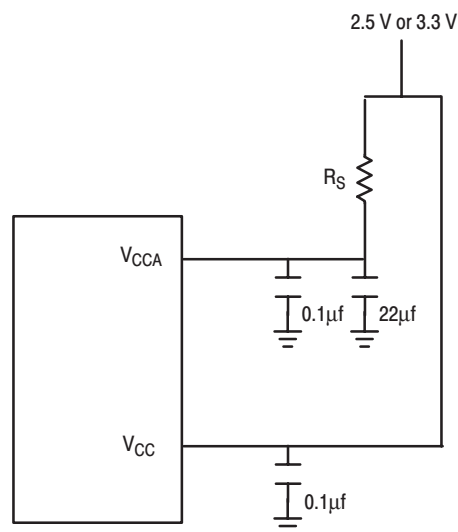


Figure 18. Power Supply Filtering

PC Board Trace Impedance Matching

In system applications utilizing high frequency clocks and/or microprocessor bus speeds, the PC board traces are characteristic transmission lines and must be treated appropriately. Termination of the transmission line must be done in order to minimize reflections and maintain proper signals in the system. Either parallel termination or series termination may terminate clock-signaling lines. Each method has advantages.

Parallel termination places a resistor on the load end of the transmission line. The value of the termination resistor is equal to the impedance of the transmission line. Figure 19 depicts the parallel termination on a clock line with the associated waveform of a clock edge propagating down the line. Since the parallel termination is equal to the characteristic impedance of the line, there is no reflection when the clock edge reaches the load.

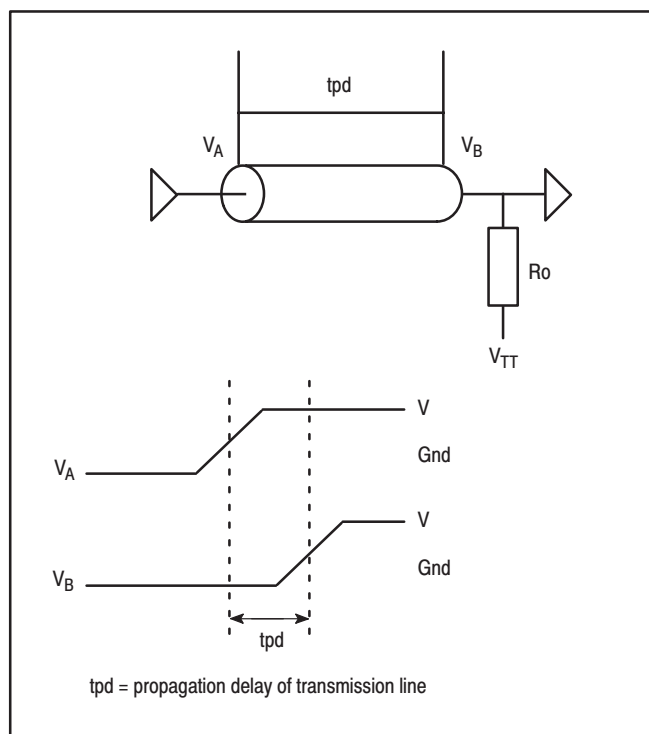


Figure 19. Parallel Termination with Waveform

Series termination places a resistor on the source end of the transmission line and in series with the transmission line. The resistor value is chosen such that the output impedance of the clock driver output buffer, plus this resistor, equals the characteristic impedance of the transmission line. No termination impedance is placed at the load end of the transmission line.

Figure 20 shows the waveform of a clock edge as it appears on the output of the clock driver and as it propagates down the transmission line. As the clock edge starts down the transmission line, the series resistor and the impedance of the transmission line act as a voltage divider causing an edge of amplitude $V/2$ to be propagated. After tpd time period, the edge arrives at the load end of the transmission line. This point appears to be an open line to the propagated edge causing a reflection of the edge of amplitude $V/2$ to be sent back to the source. On arrival at the source, the reflected waveform encounters the series termination which damps the reflected voltage and the waveform establishes a steady state. Since the voltage at the source is V and the voltage at the load is also V , there is no current flow down the transmission line other than the initial charging of the line.

The advantage of series termination is that there is no steady state loading on the line and thus the steady state drive requirements of the clock driver is low.

Single-Ended Verses Differential Clock Lines

Distribution of clock signals via differential paths has several advantages over single-ended clocks. Most of these advantages relate to noise immunity.

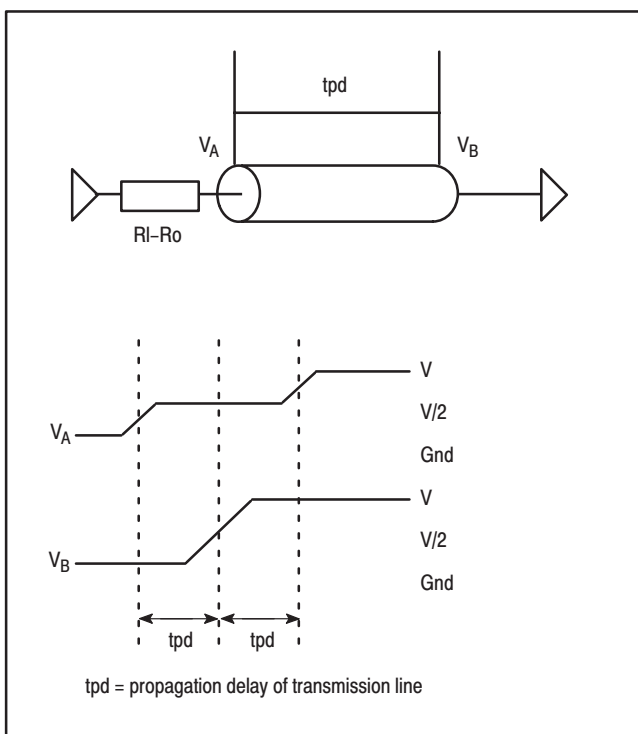


Figure 20. Series Termination with Waveform

Even though the differential clock complicates the routing of the PC board by doubling the number of traces, differential clocks may ease the PC board layout due to ground plane issues.

All currents are in the signal traces for the differential pair and not in the underlying ground plane. Thus, the effects of breaks or discontinuities in the PC board ground plane within the vicinity of the clock drive circuitry are minimized. In addition, since one output or the other is always driving a signal, the constant supply current leads to V_{cc}/Ground Bounce reduction.

There are many detailed references dealing with the subject of PC board layout and transmission line characteristics, which should be consulted for additional information.

Steps in Selecting a Clock Driver

Now that we have looked at the definitions, characteristics, and categories of clock driver devices, the question is, "How do I choose the devices or devices that fit into my application?" The following list of questions should be answered in order to understand what type of clock drivers are required.

1. What are the input and output requirements for logic levels in the application?
2. Does the application have or require differential input or output?
3. What is the clock source? Is it externally provided? What is the frequency?
4. Is a PLL based clock driver required?
5. What are the output frequency requirement(s)?
6. What number of outputs at each frequency is required?

Once these user application questions are answered, the next step in the clock design is to consult the Advanced Clock Driver Selector Guide for devices that match these requirements. If a PLL clock driver is needed, determine the feedback divide ratio and determine if the allowable VCO range is met. Once the VCO frequency is determined, next determine the output divide ratios required meeting output frequency requirement(s). Once a potential device has been selected, evaluate the jitter and skew specifications of that device based upon the system parametrics.

SUMMARY

Whether the clock design is simple or complex, the performance of the clock circuitry can best be optimized by an understanding of the parameters of the clock devices involved in the design. Many parameters may be of little or no importance to the design; however, the designer should understand these parameters and make that determination. Finally, clock tree design should be given proper attention to ensure the reliability of the system design.

CLOCK DRIVER RESOURCES

AN1934/D – Effects of Skew and Jitter on Clock Tree Design

DL207/D – Advanced Clock Drivers Device Data Book

SG392/D – Advanced Clock Drivers Selector Guide

1 **Selector Guide**

2 **Failover / Redundant Clocks**

3 **Clock Generator Data Sheets**

4 **Clock Synthesizer Data Sheets**

5 **Zero-Delay Buffer Data Sheets**

6 **LVC MOS Fanout Buffer Data Sheets**

7 **Differential Fanout Buffer Data Sheets**

8 **Packaging Information**

9 **Application Notes**

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