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18Mb High Speed Synchronous Pipeline SRAMs

Features

- **High performance pipeline operation**
- **Cycle times up to 250MHz**
  Access times as fast as 2.6nS
- **Fully synchronous operation**
- **Options for power supply**
  3.3V +10% and -5% or
  2.5V +/- 5%
- **Separate I/O power supply of 3.3V or 2.5V**
- **Individual byte write operation**
- **Three chip enable signals**
  Simple depth expansion
- **ZZ mode for low power sleep mode**
- **Mode pin for setting interleave or linear burst mode of operation**
- **Single cycle and dual cycle deselect options**
- **JTAG Boundary Scan (BGA only)**
- **JEDEC standard 100-pin TQFP, 165-ball FPBGA and 119-ball PBGA packages**

Functional Description

The N18S3625P1(2)B, N18S3633P1(2)B, N18S1825P1(2)B and N18S1833P1(2)B are 18Mb high performance synchronous SRAMs that are part of a family of options for those demanding high performance.
The memory devices contain 18Mb of memory cells organized as 524,288 x 36 (N18S3625P1(2)B, N18S3633P1(2)B) and 1,048,576 x 18 (N18S1825P1(2)B, N18S1833P1(2)B). The devices operate in a synchronous manner with control signals, addresses and data inputs synchronized and captured at the rising edge of clock for ease of use. An asynchronous $\overline{OE}$ is available for disabling the outputs at any time. An asynchronous ZZ signal can be used to put the device into sleep mode with all data retained. The devices are fabricated using NanoAmp's advanced CMOS process and high-speed/ ultra low-power circuit technology.

These 18Mb devices are the type of SRAMs originally developed as L2 cache memories for high performance CPUs. They now can be used in applications ranging from processor caches, DSP storage and networking memory.

Pipeline Performance and Power

	Sort				Unit
	167	200	225	250	
t_{CYCLE}	6.0	5.0	4.4	4.0	nS
t_{ACCESS}	3.4	3.0	2.8	2.6	nS
Icc	275	300	325	350	mA
Isb	70	70	70	70	mA

Options

- **Organization**

512Kb x 36	N18S36
1Mb x 18	N18S18

- **Power supply**

3.3V w/ Vddq = 3.3/2.5V	33
2.5V w/ Vddq = 2.5V	25

- **Operating Mode**

Single Cycle Deselect (SCD)	P1
Dual Cycle Deselect (DCD)	P2

- **Package**

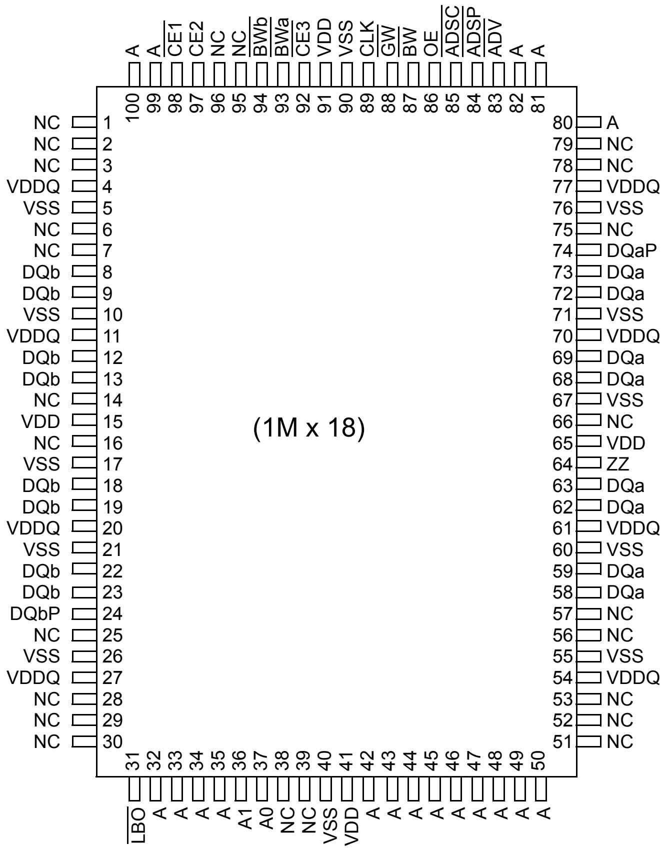
100-pin TQFP	Q
119-ball PBGA	G
165-ball FPBGA	F

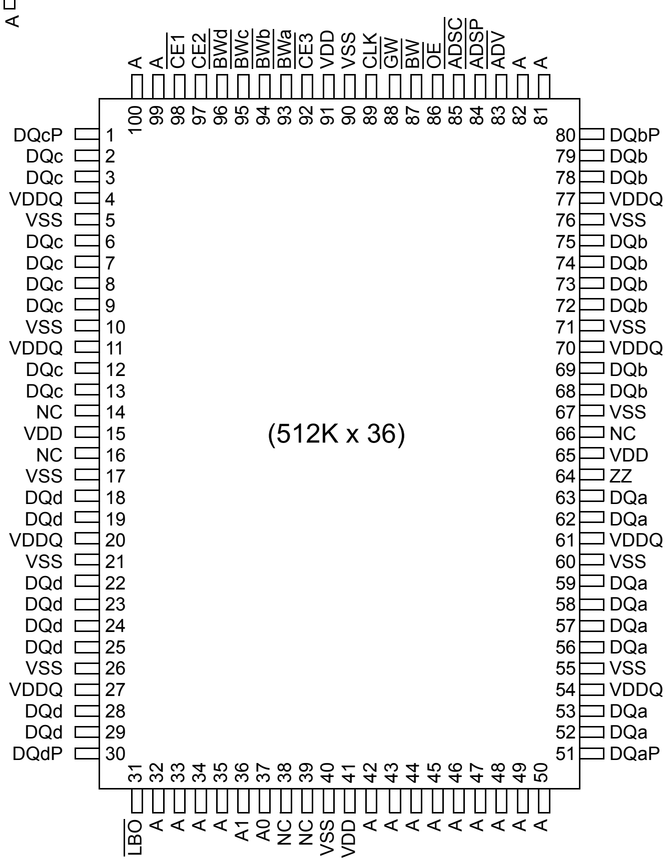
- **Speed**

167MHz	16
200MHz	20
225MHz	22
250MHz	25

Part number example:
N18S3625P1BQ-25C

100-Pin TQFP Packages





119-Ball PBGA Packages

1Mb x 18

	1	2	3	4	5	6	7
A	VDDQ	A	A	$\overline{\text{ADSP}}$	A	A	VDDQ
B	NC	A	A	$\overline{\text{ADSC}}$	A	A	NC
C	NC	A	A	VDD	A	A	NC
D	DQb	NC	VSS	NC	VSS	DQaP	NC
E	NC	DQb	VSS	$\overline{\text{CE1}}$	VSS	NC	DQa
F	VDDQ	NC	VSS	$\overline{\text{OE}}$	VSS	DQa	VDDQ
G	NC	DQb	$\overline{\text{BWb}}$	$\overline{\text{ADV}}$	VSS	NC	DQa
H	DQb	NC	VSS	$\overline{\text{GW}}$	VSS	DQa	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	DQb	VSS	CLK	VSS	NC	DQa
L	DQb	NC	VSS	NC	$\overline{\text{BWa}}$	DQa	NC
M	VDDQ	DQb	VSS	$\overline{\text{BW}}$	VSS	NC	VDDQ
N	DQb	NC	VSS	A1	VSS	DQa	NC
P	NC	DQbP	VSS	A0	VSS	NC	DQa
R	NC	A	$\overline{\text{LBO}}$	VDD	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

512Kb x 36

	1	2	3	4	5	6	7
A	VDDQ	A	A	$\overline{\text{ADSP}}$	A	A	VDDQ
B	NC	A	A	$\overline{\text{ADSC}}$	A	A	NC
C	NC	A	A	VDD	A	A	NC
D	DQc	DQcP	VSS	NC	VSS	DQbP	DQb
E	DQc	DQc	VSS	$\overline{\text{CE1}}$	VSS	DQb	DQb
F	VDDQ	DQc	VSS	$\overline{\text{OE}}$	VSS	DQb	VDDQ
G	DQc	DQc	$\overline{\text{BWc}}$	$\overline{\text{ADV}}$	$\overline{\text{BWb}}$	DQb	DQb
H	DQc	DQc	VSS	$\overline{\text{GW}}$	VSS	DQb	DQb
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	DQd	DQd	VSS	CLK	VSS	DQa	DQa
L	DQd	DQd	$\overline{\text{BWd}}$	NC	$\overline{\text{BWa}}$	DQa	DQa
M	VDDQ	DQd	VSS	$\overline{\text{BW}}$	VSS	DQa	VDDQ
N	DQd	DQd	VSS	A1	VSS	DQa	DQa
P	DQd	DQdP	VSS	A0	VSS	DQaP	DQa
R	NC	A	$\overline{\text{LBO}}$	VDD	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

7 x 17 Ball BGA with 1.27 mm Ball Pitch

165-Ball FPBGA Packages

1M x 18

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE1}$	$\overline{BWb}$	NC	$\overline{CE3}$	$\overline{BW}$	$\overline{ADSC}$	$\overline{ADV}$	A	A
B	NC	A	CE2	NC	$\overline{BWa}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQaP
D	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
E	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
F	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
G	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
H	NC	VSS	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
K	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
L	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
M	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
N	DQbP	NC	VDDQ	VSS	NC	A	NC	VSS	VDDQ	NC	NC
P	NC	NC	A	A	TDI	A1	TDO	A	A	A	A
R	$\overline{LBO}$	NC	A	A	TMS	A0	TCK	A	A	A	A

512K x 36

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE1}$	$\overline{BWc}$	$\overline{BWb}$	$\overline{CE3}$	$\overline{BW}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC	A	CE2	$\overline{BWd}$	$\overline{BWa}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC
C	DQcP	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQbP
D	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
E	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
H	NC	VSS	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
M	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
N	DQdP	NC	VDDQ	VSS	NC	A	NC	VSS	VDDQ	NC	DQaP
P	NC	NC	A	A	TDI	A1	TDO	A	A	A	A
R	$\overline{LBO}$	NC	A	A	TMS	A0	TCK	A	A	A	A

11 x 15 Ball BGA with 1.0 mm Ball Pitch

Pin Descriptions

Signal	Type	POWER
A0, A1	Synch Input	Address inputs sampled at the rising edge of CLK. Least significant address bits are used to set the internal burst counter (if used).
Ax	Synch Input	Address inputs 2 through 18/19, sampled at the rising edge of CLK.
LBO	Synch Input	Linear burst order, active low, used for setting the address order of the burst counter. A low selects linear burst order while a high selects interleave burst order and if floating, this input will default to a high (interleave order) This should not be changed while operating the SRAM.
ADV	Synch Input	Advance, sampled at the rising edge of clock. When asserted low, automatically increments the internal burst counter.
ADSP	Synch Input	Address strobe from processor, sampled at the rising edge of clock. When asserted low, all addresses are captured. ADSP is ignored if CE1 is high.
ADSC	Synch Input	Address strobe from controller, sampled at the rising edge of clock. When asserted low, all addresses are captured.
BWa BWb BWc BWd	Synch Input	Byte writes, active low, sampled at the rising edge of CLK if WE is low for a write cycle. BWa controls byte a (DQa) inputs, BWb controls byte b (DQb) inputs, BWc controls byte c (DQc) inputs and BWd controls byte d (DQd) inputs. For x18 devices, only BWa and BWb apply.
BW	Synch Input	Byte write enable, active low, sampled at the rising edge of CLK. A low state initiates a byte write.
GW	Synch Input	Global write enable, active low, sampled at the rising edge of CLK. A low state writes to all bytes regardless of BWx and BW.
CLK	Clock Input	Clock
CE1	Synch Input	Chip enable 1, active low, sampled on the rising edge of CLK. Used with CE2 and CE3 and to select the device. If inactive, ADSP is ignored.
CE2	Synch Input NA on 119-BGA	Chip enable 2, active high, sampled on the rising edge of CLK. Used with CE1 and CE3 and to select the device.
CE3	Synch Input NA on 119-BGA	Chip enable 3, active low, sampled on the rising edge of CLK. Used with CE2 and CE1 and to select the device.
OE	Asynch Input	Output enable, asynchronous active low, tri-states the output buffers when high and enables the output buffers when low.
ZZ	Asynch Input	Sleep mode, asynchronous active high, puts the device in a low power sleep mode that retains all data while high.
DQa DQb DQc DQd	Synch Input/ Output	During a write cycle, the data lines are synchronous inputs that are sampled at the rising edge of CLK to specify data to be written to the memory array. During a read cycle, the data lines are driven out with data from the SRAM array. DQ(a, b, c, d) refer to the bytes a, b, c, d. For x18 devices, only DQa and DQb apply.
VDD	Power Supply	Supplies power to the device core.
VDDQ	I/O Power Supply	Supplies power to the I/O section of the device.
VSS	Ground supply	Ground
TMS	Input (BGA)	Test Mode Select supplies input command to the TAP controller with TCK.
TDI	Input (BGA)	Test Data Input supplies serial input to test registers.
TDO	Output (BGA)	Test Data Output supplies serial data out from test registers.
TCK	Input (BGA)	Test Clock controls TAP controller and serial data in and data out.
NC	-	No connect

Functional Truth Table [1, 5, 7]

Operation	Address	$\overline{CE1}$	CE2	$\overline{CE3}$	$\overline{ADV}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{W}^2$	$\overline{OE}$	ZZ	CLK^3	DQ^6	Notes
DESELECT	NA	H	X	X	X	X	L	X	X	L	L-H	High-Z	
DESELECT	NA	L	L	X	X	L	X	X	X	L	L-H	High-Z	
DESELECT	NA	L	X	H	X	L	X	X	X	L	L-H	High-Z	
DESELECT	NA	L	L	X	X	X	L	X	X	L	L-H	High-Z	
DESELECT	NA	L	X	H	X	X	L	X	X	L	L-H	High-Z	
READ, begin burst	Ext	L	H	L	X	L	X	X	L	L	L-H	Data-out	
READ, begin burst	Ext	L	H	L	X	H	L	H	L	L	L-H	Data-out	
READ, continue burst	Int	X	X	X	L	H	H	H	L	L	L-H	Data-out	4, 7
READ, continue burst	Int	H	X	X	L	X	H	H	L	L	L-H	Data-out	4, 7
READ, suspend burst	Current	X	X	X	H	H	H	H	L	L	L-H	Data-out	
READ, suspend burst	Current	H	X	X	H	X	H	H	L	L	L-H	Data-out	
WRITE, begin burst	Ext	L	H	L	X	H	L	L	X	L	L-H	Data-in	
WRITE, continue burst	Int	X	X	X	L	H	H	L	X	L	L-H	Data-in	4, 7
WRITE, continue burst	Int	H	X	X	L	X	H	L	X	L	L-H	Data-in	4, 7
WRITE, suspend burst	Current	X	X	X	H	H	H	L	X	L	L-H	Data-in	
WRITE suspend burst	Current	H	X	X	H	X	H	L	X	L	L-H	Data-in	
Deep Sleep	NA	X	X	X	X	X	X	X	X	H	X	High-Z	

Notes:
1. X = don't care; H = logic HIGH; L = logic LOW.
2. W = L means write cycle per Write Truth Table below. W = H means read cycle.
3. L-H refers to the CLK edge transitioning from a low to a high state.
4. All continue burst cycles use the same control inputs. The type of cycle is chosen in the first cycle prior to the continue cycle.
5. All inputs except $\overline{OE}$ and ZZ must meet set-up and hold times.
6. All outputs will remain in high-Z during power-up.
7. A 2-bit burst counter is included which is incremented for all continue burst cycles. The address wraps around every fourth burst cycle.

Write Truth Table [1, 2]

Function	$\overline{GW}$	$\overline{BW}$	$\overline{Ba}$	$\overline{Bb}$	$\overline{Bc}$	$\overline{Bd}$
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE byte a [3]	H	L	L	H	H	H
WRITE byte b [3]	H	L	H	L	H	H
WRITE byte c [3]	H	L	H	H	L	H
WRITE byte d [3]	H	L	H	H	H	L
WRITE all bytes	H	L	L	L	L	L
WRITE all bytes	L	X	X	X	X	X

Notes:
1. This represents the x36 device. For the x18 device, only $\overline{BWa}$ and $\overline{BWb}$ are used.
2. X = don't care; H = logic HIGH; L = logic LOW.
3. Multiple bytes may be exercised during a cycle.

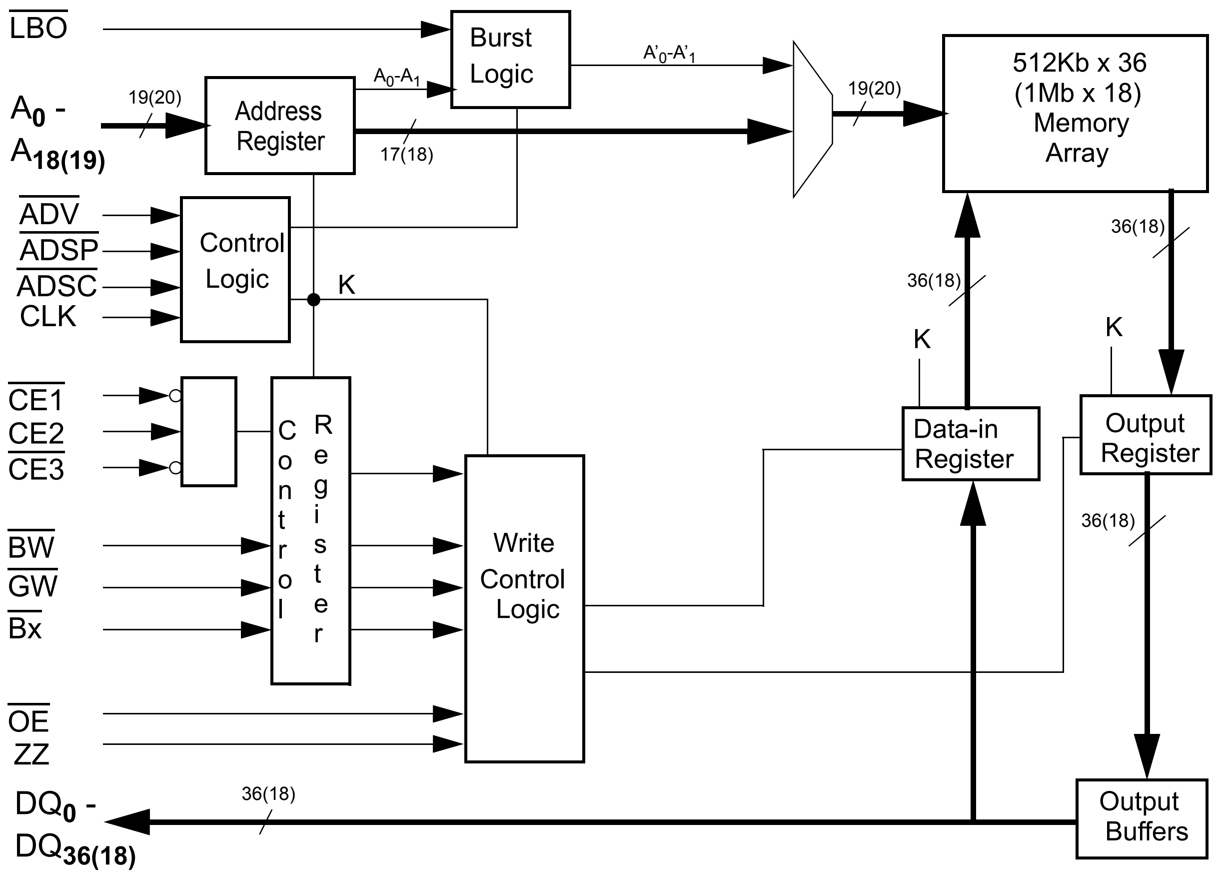
Burst Order Tables

Interleave	Starting digits		Starting digits		Starting digits		Starting digits	
$\overline{LBO}$ = High	A1	A0	A1	A0	A1	A0	A1	A0
First address	0	0	0	1	1	0	1	1
Second address	0	1	0	0	1	1	1	0
Third address	1	0	1	1	0	0	0	1
Fourth address	1	1	1	0	0	1	0	0

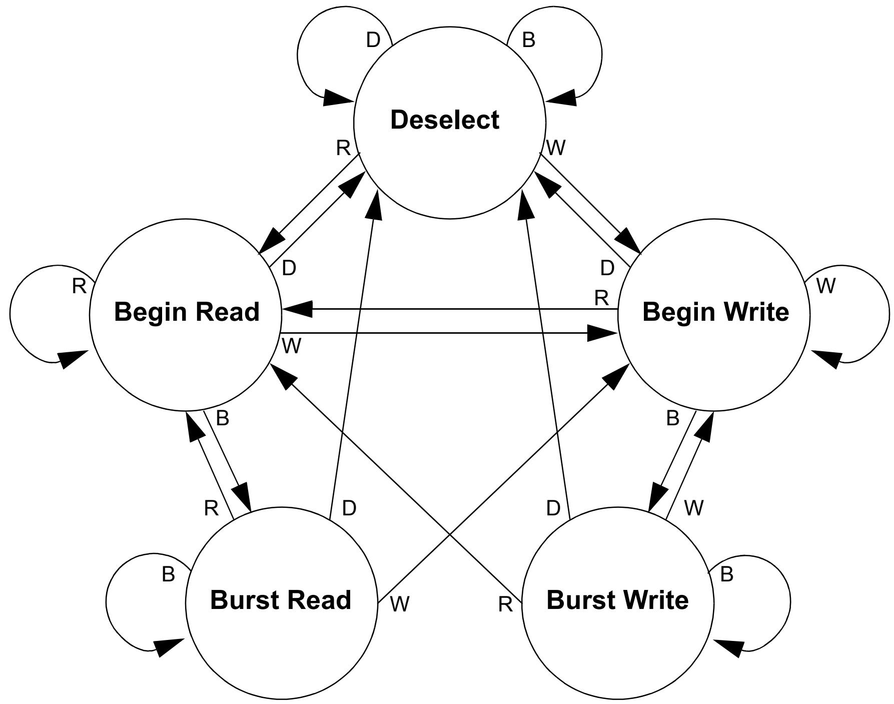
Linear	Starting digits		Starting digits		Starting digits		Starting digits	
$\overline{LBO}$ = Low	A1	A0	A1	A0	A1	A0	A1	A0
First address	0	0	0	1	1	0	1	1
Second address	0	1	1	0	1	1	0	0
Third address	1	0	1	1	0	0	0	1
Fourth address	1	1	0	0	0	1	1	0

Note:
At the end of a burst of four, the burst counter wraps to the starting address and continues.

Functional Block Diagram



Read and Write State Diagram



Key:
State diagram shows current state and transitions to possible next states.
D = Deselect
R = Read
W = Write
B = Burst (read, write or deselect)

Functional Operation

The N18S1825P1(2)B, N18S1833P1(2)B, N18S3625P1(2)B and N18S3633P1(2)B are developed for high performance applications such as level 2 caches, DSP main storage and networking memory. Devices are available for both pipeline and flow-through modes of operation depending on the particular system needs. All inputs except OE, LBO and ZZ are synchronized and registered by the rising edges of the clock (CLK). Three chip enables are available in the TQFP package for depth expansion with CE1 and CE3 being active low and CE2 active high. The address inputs are latched and used as the location in memory to start a memory cycle . Output enable (OE), linear burst mode (LBO) and sleep mode (ZZ) are asynchronous signals that control other aspects of the device. OE is used to disable the output buffers at any time. LBO is either tied high for interleave burst order or low for linear burst order. ZZ is used to put the device in a low power sleep mode, while all data is retained in the SRAM memory array. For a burst cycle to start, all three chip enables must be active. Read operations are started with CE1, CE3 and ADSP being asserted low at the rising edge of CLK along with CE2 being asserted high. ADSC can also be used to initiate the read cycle. In this case, CE1, CE3 and ADSC are asserted low at the rising edge of CLK along with CE2 and ADSP being asserted high and the write controls (GW, BW, Bx) in a read operation configuration.

In a single cycle deselect device, when the device is deselected at the rising edge of clock, the outputs will go to a high-Z state immediately.

In a dual cycle deselect device, when the device is deselected at the rising edge of clock, the outputs will go to a high-Z state after the following rising clock edge.

Write Operation

Write operations are started with CE1, CE3 and ADSC being asserted low at the rising edge of CLK along with CE2 and ADSP being asserted high and the write controls (GW, BW, Bx) in a write operation configuration. Address and data-in must be setup at this first clock edge. Another way to start a write operation is with ADSP. In this case, CE1, CE3 and ADSP must be asserted low at the rising edge of CLK along with CE2 and ADSC being asserted high. Here, the write controls do not matter until the next clock edge. At the following rising edge of CLK, write controls must be active, ADV must be asserted high and the data-in must be setup. For write controls, GW asserted low will write to all bytes regardless of the byte write control inputs. If GW is high, then BW and Bx will control which bytes of data get written to the SRAM. For a write cycle, all the necessary control signals must be setup at the rising edge of CLK as stated above. The BW and Bx must be setup active low for whichever bytes will be written too.

Burst Operation

Burst cycles are continued with ADV being asserted low at the rising edge of CLK while ADSP and ADSC are high. In this operation, the internal burst counter is incremented and an internal address is used to access the SRAM array. The burst counter is a four bit counter and can be incremented in two orders, interleave and linear. The burst counter wraps around after four addresses and continues to operate as long as burst commands are valid and valid CLK cycles are performed.

Pipeline Operation

For a read cycle, all the necessary control signals must be setup at the rising edge of CLK as stated above. The memory array is then accessed. During this first cycle, data proprogates through to the output registers. At the next rising edge of CLK, data moves through the output registers and out of the SRAM on the DQ pins. This pipeline operation reads data out on the clock edge following the initial rising edge.

.Sleep Mode

Sleep mode is a low power mode that allows the device to continue to retain data in a power down mode. ZZ is asserted high to enter sleep mode and after two clock cycles, the operating current will be reduced to $I_{SL.}$ Since ZZ is an asynchronous operation, sleep mode should not be started until all operations are completed. ZZ should be asserted low for normal operation.

Absolute Maximum Ratings

Symbol	Description		Value	Unit
V_{DD}	Voltage on any V_{DD} pin wrt Ground	3.3V Device	-0.5 to 4.6	V
		2.5V Device	-0.5 to 3.6	
V_{IN}[1]	Voltage on any input pin		-0.5 to V_{DDQ} +0.5V	V
$V_{I/O}$[1]	Voltage on any DQ pin		-0.5 to V_{DDQ} +0.5V	V
T_{BIAS}	Temperature under bias		-55 to 125	^oC
T_{STOR}	Storage temperature		-65 to150	^oC
I_{OUT}	Current into output circuit		20	mA
ESD	Static Discharge Voltage		> 2100	V
I_{Latch}	Latch-Up Current		> 200	mA

.1) Minimum voltage must not exceed -2V for pulse widths of < 20% t_{CYC}.

Pin Capacitance[1]

Item	Symbol	Conditions	Max	Unit	
Input Capacitance	C_{in}	$T_a = 25^oC$, VDD = Typ, f = 1MHz	tbd	pF	
Clock Capacitance	C_{clk}		tbd	pF	
Input/Output Cpacitance	$C_{i/o}$		tbd	pF	

1) Not 100% tested.

Thermal Resistance[1]

Item	Conditions	Theta JA Junction to Ambient	Theta JC Junction to Case	Unit
100-pin TQFP	Still air, soldered on a 2 layer board	31	6	$^oC/W$
119-ball PBGA	Still air, soldered on a 4 layer board	45	7	$^oC/W$
165-ball FPBGA		46	3	

1) Not 100% tested.

Operating Conditions and DC Characteristics

Over the operating range. All voltages referenced to ground (V_{ss}).

3.3V Device[1]

Iteml		Conditions		Min	Typ[4]	Max	Unit
Supply Voltage	V_{DD}			3.135	3.3	3.63	V
I/O Supply Voltage	V_{DDQ}			2.375	2.5	V_{DD}	V
Input High Voltage	V_{IH}	w/ 3.3V V_{DDQ}		2.0		V_{DD} + 0.3	V
		w/ 2.5V V_{DDQ}		1.7		V_{DD} + 0.3	
Input Low Voltage	V_{IL}	w/ 3.3V V_{DDQ}		–0.3		0.8	V
		w/ 2.5V V_{DDQ}		–0.3		0.7	
Output High Voltage[5]	V_{OH}	w/ 3.3V V_{DDQ}, I_{OH} = -4.0mA		2.4			V
		w/ 2.5V V_{DDQ}, I_{OH} = -1.0mA		2.0			
Output Low Voltage[5]	V_{OL}	w/ 3.3V V_{DDQ}, I_{OL} = 8.0mA				0.4	V
		w/ 2.5V V_{DDQ}, I_{OL} = 1.0mA				0.4	
Operating Current[2, 3]	I_{DD}	Device selected; All inputs < V_{IL} or > V_{IH}; Frequency = $1/T_{cyc}$ (MIN); Outputs open	- 16			275	mA
			- 20			300	
			- 22			325	
			- 25			350	
Deselect Current - Standby (CMOS)[3]	I_{SB1}	Device deselected; All inputs static and < 0.3V or > V_{DDQ}-0.3, Frequency = 0	All			70	mA
Device Current - Standby (TTL)[3]	I_{SB2}	Device deselected; All inputs static and < V_{IL} or > V_{IH}, Frequency = 0	All			80	mA
Deselect Current - Clock running (CMOS)[3]	I_{SB3}	Device deselected; All inputs < 0.3V or > V_{DDQ}-0.3;Frequency = $1/T_{cyc}$	- 16			85	mA
			- 20			95	
			- 22			100	
			- 25			105	
Deselect Current - Clock running (TTL)[3]	I_{SB4}	Device deselected; All inputs static and < V_{IL} or > V_{IH}, Frequency = $1/T_{cyc}$	- 16			90	mA
			- 20			100	
			- 22			110	
			- 25			120	

2.5V Device[1]

Iteml		Conditions		Min	Typ[4]	Max	Unit
Supply Voltage	V_{DD}			2.375	2.5	2.625	V
I/O Supply Voltage	V_{DDQ}			2.375	2.5	2.625	V
Input High Voltage	V_{IH}			1.7		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}			–0.3		0.7	V
Output High Voltage[5]	V_{OH}	I_{OH} = -1.0mA		2.0			V
Output Low Voltage[5]	V_{OL}	I_{OL} = 1.0mA				0.4	V
Operating Current[2,3]	I_{DD}	Device selected; All inputs < V_{IL} or > V_{IH}; Frequency = 1/T_{cyc} (MIN); Outputs open	- 16			275	mA
			- 20			300	
			- 22			325	
			- 25			350	
Deselect Current - Standby (CMOS)[3]	I_{SB1}	Device deselected; All inputs static and < 0.3V or > V_{DDQ}-0.3, Frequency = 0	All			70	mA
Device Current - Standby (TTL)[3]	I_{SB2}	Device deselected; All inputs static and < V_{IL} or > V_{IH}, Frequency = 0	All			80	mA
Deselect Current - Clock running (CMOS)[3]	I_{SB3}	Device deselected; All inputs < 0.3V or > V_{DD}-0.3;Frequency = 1/T_{cyc}	- 16			85	mA
			- 20			95	
			- 22			100	
			- 25			105	
Deselect Current - Clock running (TTL)[3]	I_{SB4}	Device deselected; All inputs static and < V_{IL} or > V_{IH}, Frequency = 1/T_{cyc}	- 16			90	mA
			- 20			100	
			- 22			110	
			- 25			120	

1) Currents are specified for V_{DD} = V_{DD} max.
2) Does not include output currents.
3) Device selected refers to a device in the active mode. Device deselected refers to a device as defined in the truth table.
4) Typical values measured at V_{DD} TYP and 25^{o}C.
5) Ouput load B used.

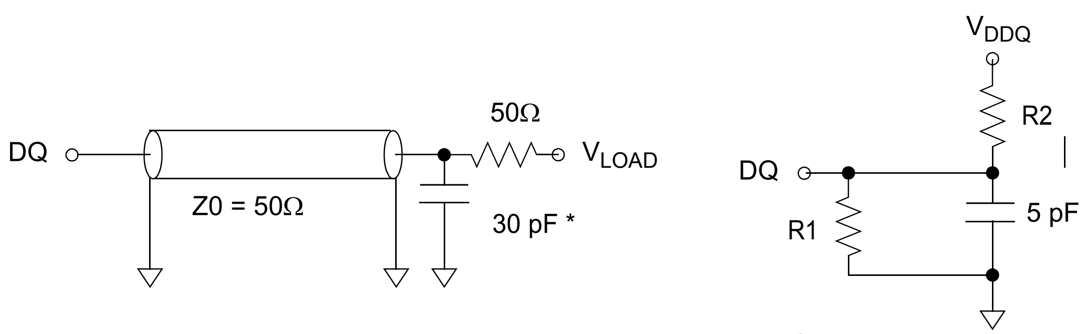
Leakage Currents

Item	Symbol	Conditions	Min	Max	Units	Notes
Input Leakage Current	I_{LI}[1]	0V < V_{IN} < V_{DD}	-5.0	5.0	µA	1
Input Leakage Current of LBO and ZZ pins			-30.0	30.0		
Output Leakage Current	I_{LO}	Outputs disabled 0V < V_{IN} < V_{DDQ}	-5.0	5.0	µA	

1. LBO and ZZ inputs: I_{LI} = +/- 30µA due to internal resistors for floating conditions.

AC Test Conditions

Item	Value
Input Pulse Level	0V to Vcc
Input Rise and Fall Time	1.0V/nS (10% to 90%)
Input Timing Reference Level	$V_{DD}/2$
Output Timing Reference Level	$V_{DDQ}/2$
Output Load	See diagram below



Output Load A

* Includes Jig Capacitance

Output Load B

AC Output Load

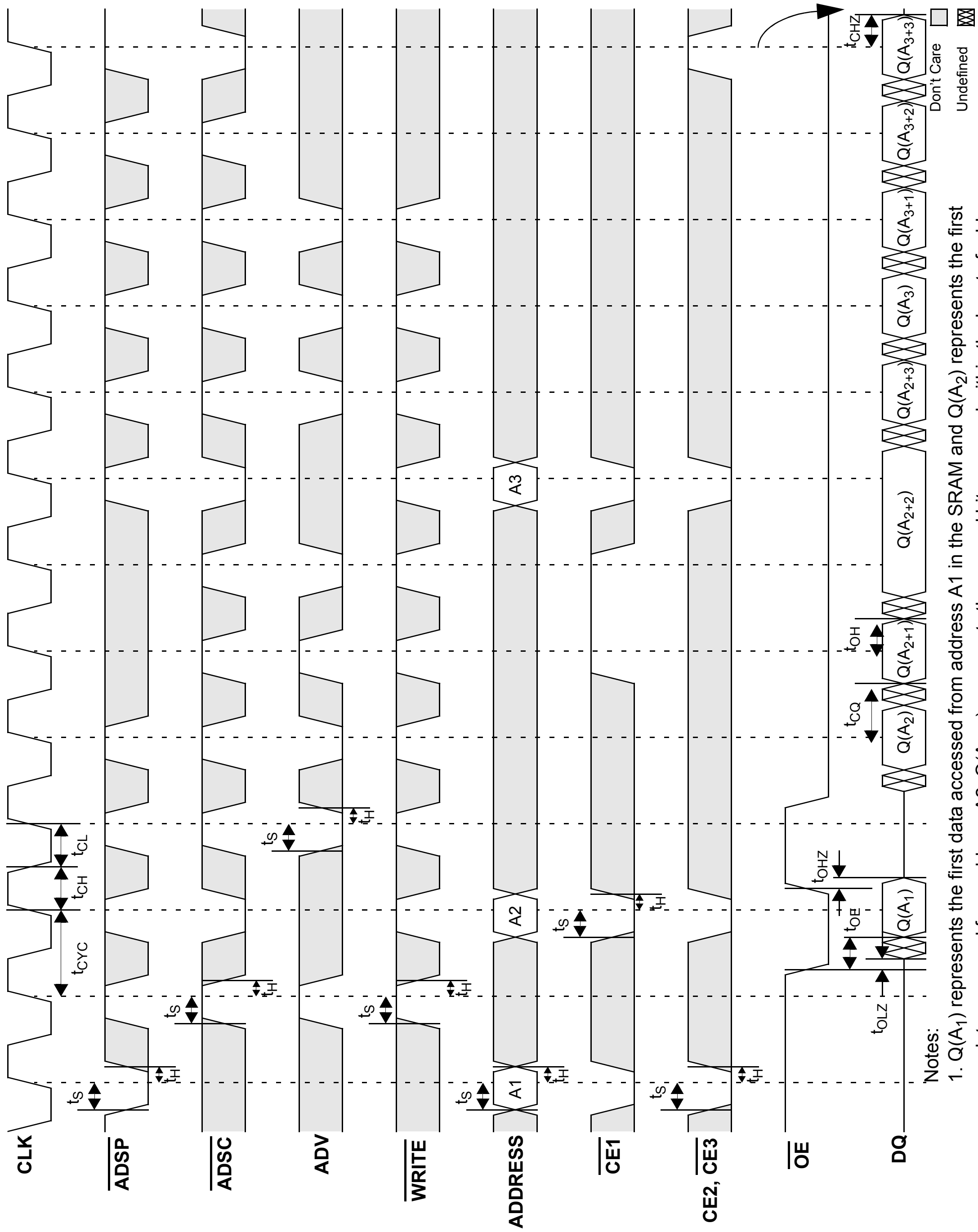
Component	Value		Unit
	3.3V VDDQ	2.5V VDDQ	
VLOAD	1.5	1.25	V
R1	351	1538	Ω
R2	317	1667	Ω

AC Timing Characteristics

Parameter	Symbol	-25		-22		-20		-16		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
CLOCK TIMINGS										
Clock Cycle Time	t_{CYC}	4.0		4.4		5.0		6.0		nS
Clock High Pulse Width	t_{CH}	1.7		2.0		2.0		2.2		nS
Clock Low Pulse Width	t_{CL}	1.7		2.0		2.0		2.2		nS
Clock Frequency	F_{MAX}		250		225		200		167	MHz
OUTPUT TIMINGS										
Clock high to output valid	t_{CQ}		2.6		2.8		3.0		3.4	nS
Output hold from clock high	t_{OH}	1.0		1.0		1.3		1.3		nS
Clock to output in low-Z[1]	t_{CLZ}	1.0		1.0		1.3		1.3		nS
Clock to output in high-Z[1]	t_{CHZ}		2.6		2.8		3.0		3.4	nS
OE low to output valid	t_{tOE}		2.6		2.8		3.0		3.4	nS
OE low to output in low-Z[1]	t_{OLZ}	0		0		0		0		nS
OE high to output in high-Z[1]	t_{OHZ}		2.6		2.8		3.0		3.4	nS
SETUP AND HOLD TIMES										
Setup Time	t_S	1.2		1.4		1.4		1.5		nS
Hold Time	t_H	0.3		0.4		0.4		0.5		nS

1) t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ} are specified with output load B.

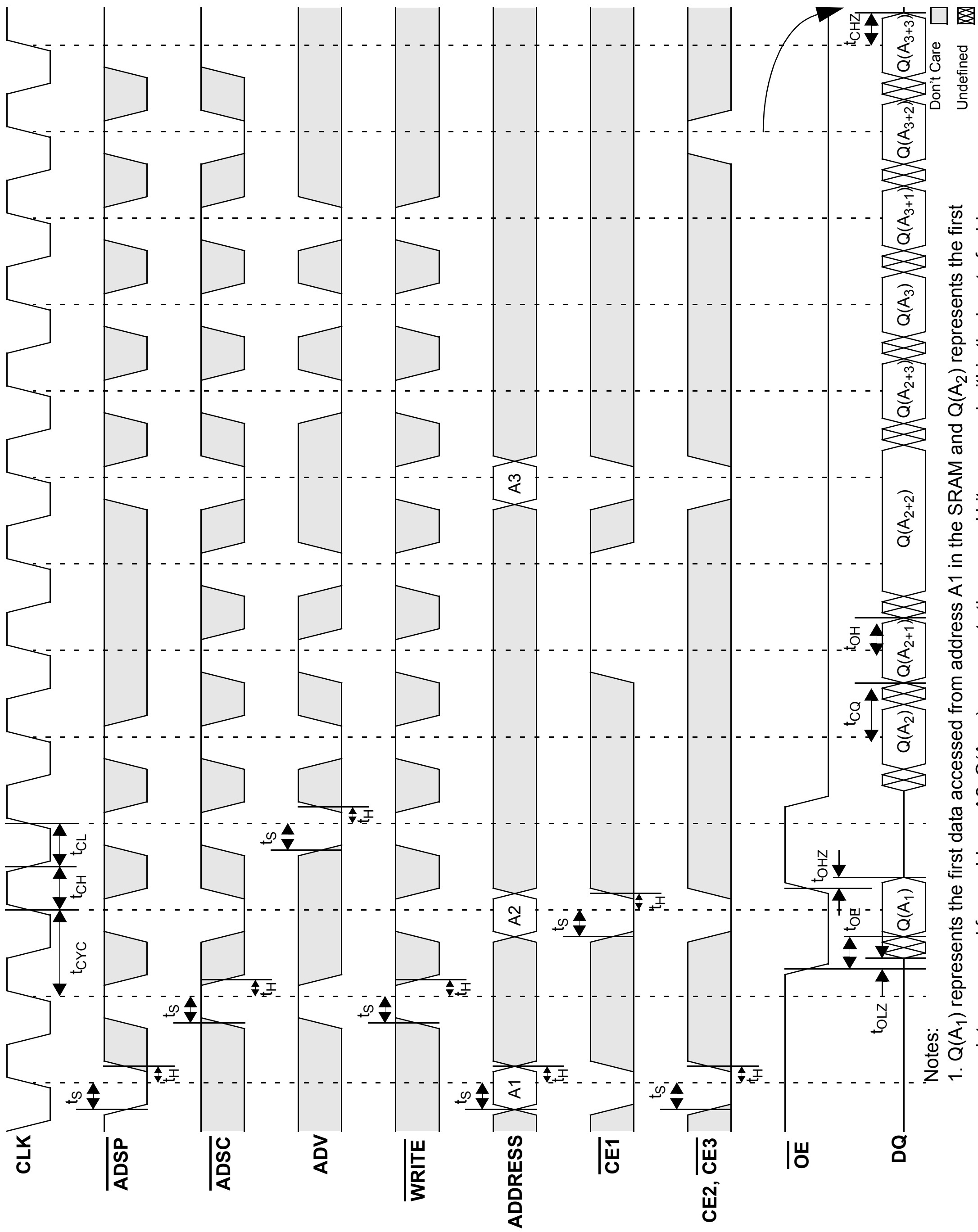
Timing Waveforms for READ Cycles - (Single Cycle Deselect)



Notes:

1. $Q(A_1)$ represents the first data accessed from address A1 in the SRAM and $Q(A_2)$ represents the first data accessed from address A2. $Q(A_{2+1})$ represents the second bit accessed within the burst of address A2.
2. CE2, $\overline{CE3}$ = L means active, $\overline{CE3}$ = L and CE2 = H. CE2, $\overline{CE3}$ = H means inactive, $\overline{CE3}$ = H or CE2 = L.
3. $\overline{WRITE}$ = L means write cycle defined by Writh Truth Table. $\overline{WRITE}$ = H means read cycle.

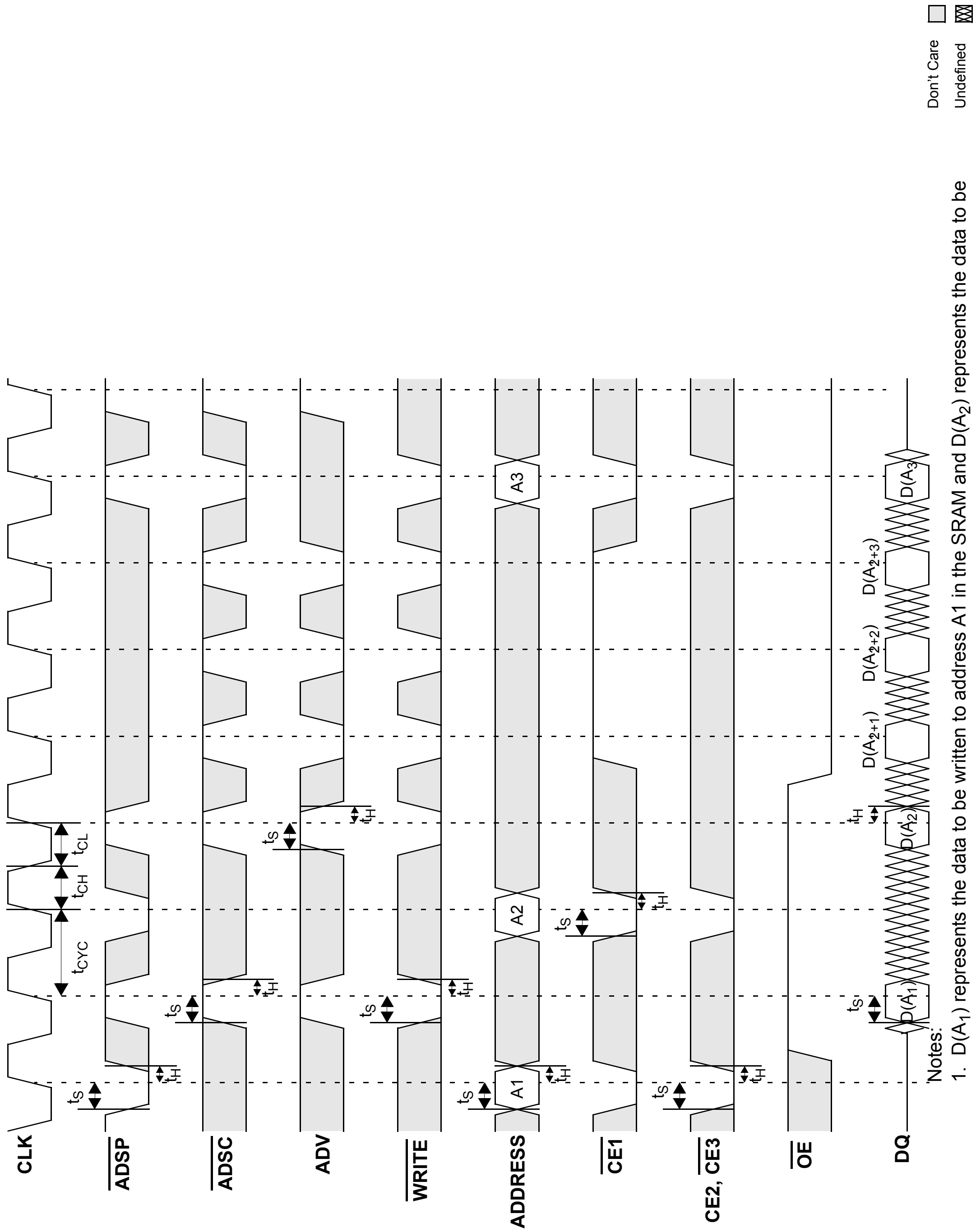
Timing Waveforms for READ Cycles - Pipeline Device (Dual Cycle Deselect)



Notes:

1. $Q(A_1)$ represents the first data accessed from address A1 in the SRAM and $Q(A_2)$ represents the first data accessed from address A2. $Q(A_{2+1})$ represents the second bit accessed within the burst of address A2.
2. CE2, $\overline{CE3}$ = L means active, $\overline{CE3}$ = L and CE2 = H. CE2, $\overline{CE3}$ = H means inactive, $\overline{CE3}$ = H or CE2 = L.
3. $\overline{WRITE}$ = L means write cycle defined by Writh Truth Table. $\overline{WRITE}$ = H means read cycle.

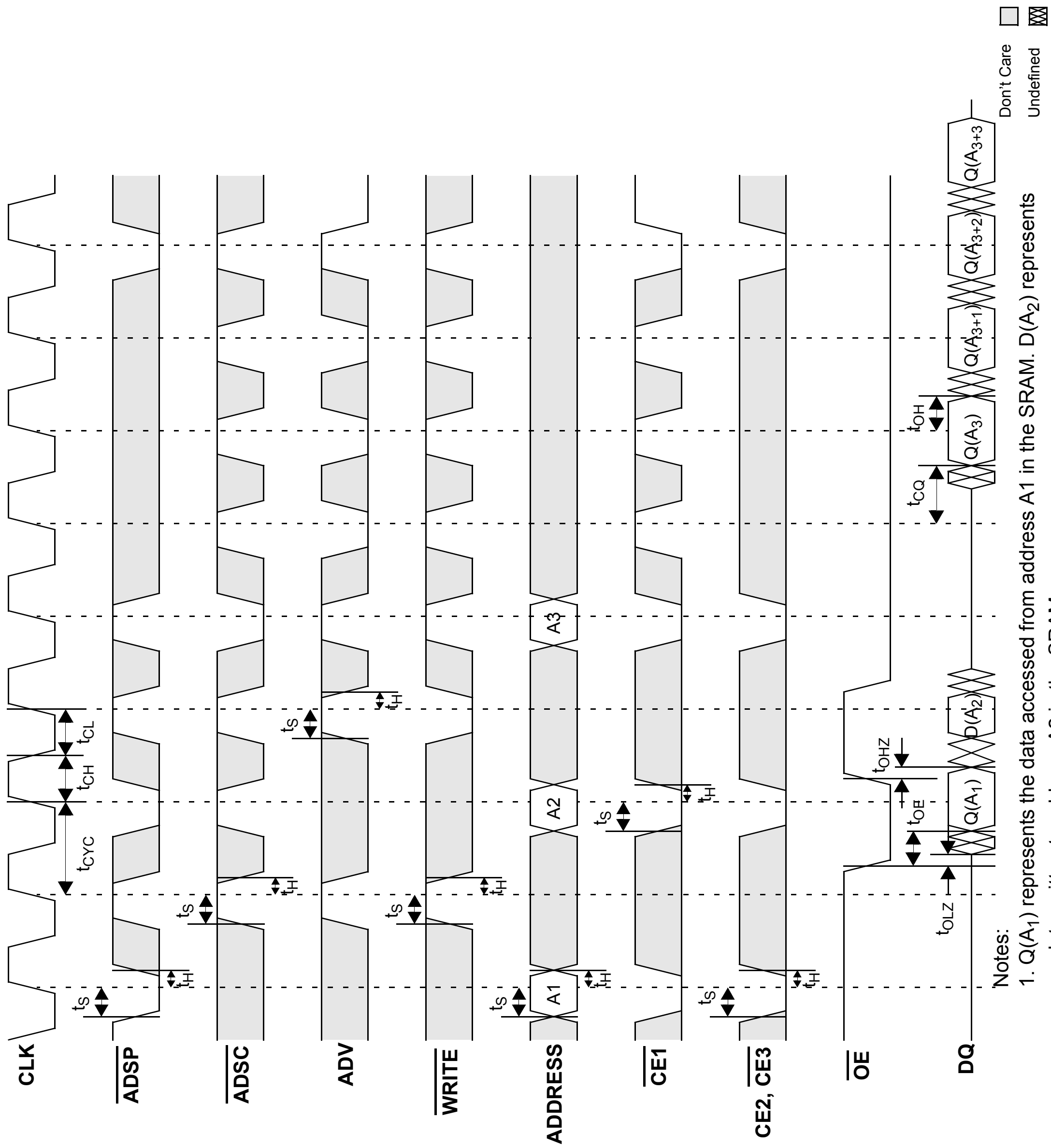
Timing Waveforms for WRITE Cycles



Notes:

1. D(A_1) represents the data to be written to address A1 in the SRAM and D(A_2) represents the data to be written to address A2. D(A_{2+1}) represents the second bit to be written to address A2+1 during the burst.
2. CE2, $\overline{CE3}$ = L means active, $\overline{CE3}$ = L and CE2 = H. CE2, $\overline{CE3}$ = H means inactive, $\overline{CE3}$ = H or CE2 = L.

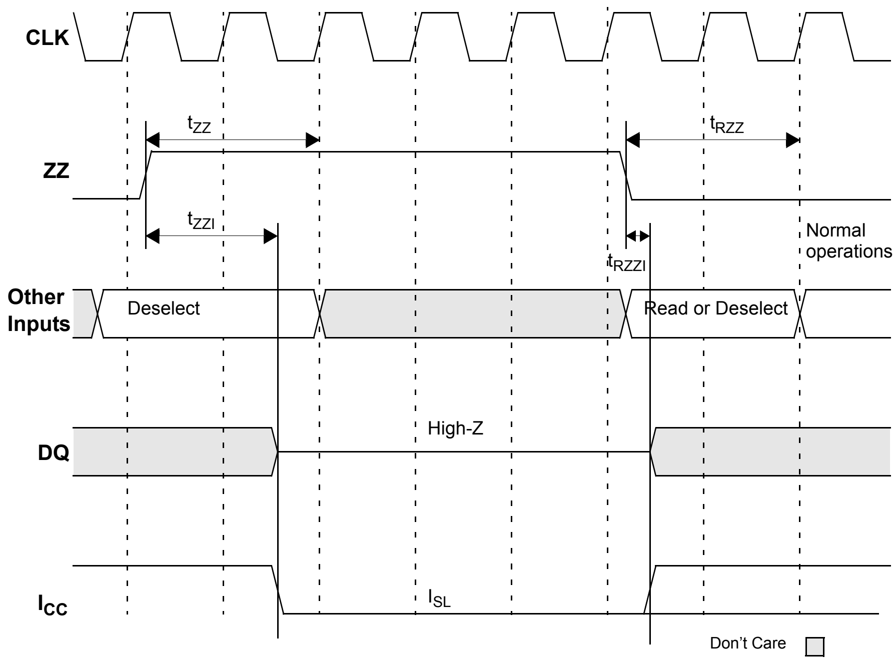
Timing Waveforms for Combined READ/WRITE Cycles



Notes:

1. $Q(A_1)$ represents the data accessed from address A1 in the SRAM. $D(A_2)$ represents data written to address A2 in the SRAM.
2. CE2, $\overline{CE3}$ = L means active, $\overline{CE3}$ = L and CE2 = H. CE2, $\overline{CE3}$ = H means inactive, $\overline{CE3}$ = H or CE2 = L.
3. $\overline{WRITE}$ = L means write cycle from Write Truth Table.

Timing Waveforms Sleep Mode



Sleep Mode Characteristics

Item	Symbol	Conditions	Min	Max	Units	Notes
ZZ active to input ignored	t_{ZZ}	ZZ > V_{IH}		2	cycles	
ZZ inactive to input sampled	t_{RZZ}		2		cycles	
ZZ active to sleep current	t_{ZZI}			2	cycles	
ZZ inactive to exit sleep current	t_{RZZI}		2		cycles	
Sleep mode power supply current	I_{SL}			60	mA	

JTAG Serial Boundary Scan

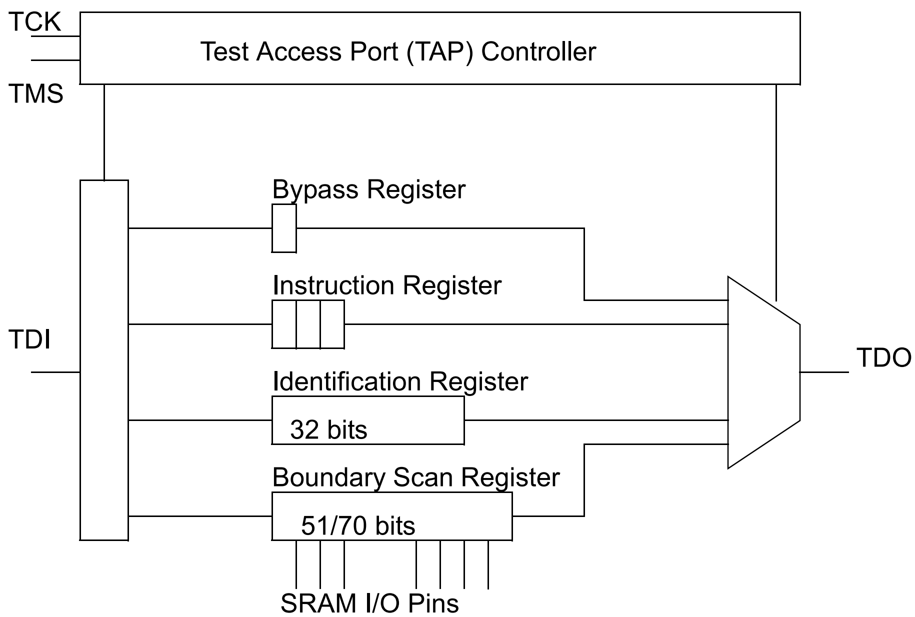
The N18S1825P1(2)B, N18S1833P1(2)B, N18S3625P1(2)B and N18S3633P1(2)B all incorporate JTAG serial boundary scan capability in the BGA packages only. This test function utilizes the test Access Port (TAP) to and operates consistent with IEEE Standard 1149.1-1900, but is not fully compliant since a subset of functions are omitted. The exclusion of these TAP controller functions does not conflict with other 1149.1 compliant devices. This test function allows connectivity scan testing during board level debug. This JTAG port operates using standard 2.5V I/O levels.

Disabling the JTAG Feature

There are no issues with using this SRAM and not using the JTAG feature. For normal operation with the TAP controller disabled, TCK must be tied low and TDI and TMS should be left floating or tied to Vdd. TDO should be left unconnected.

Performing a TAP Reset

Upon power-up, the TAP controller will be in a reset state and it will not interfere with the operation of the SRAM. A reset can be entered by holding TMS at a high level for five consecutive rising edges of TCK.



JTAG Block Diagram

TAP Pin Description

Signal	Name	Type	Description
TCK	Test Clock	Input clock	Clock for all TAP events. All inputs are captured on the rising edge of TCK. All outputs are driven with the falling edge of TCK.
TMS	Test Mode Select	Input	Input for commands to theTAP controller. Sampled on the rising edge of TCK
TDI	Test Data-In	Input	Input for serial registers sampled on rising edge of TCK.
TDO	Test Data-Out	Output	Output of serial registers that changes on the falling edge of TCK.

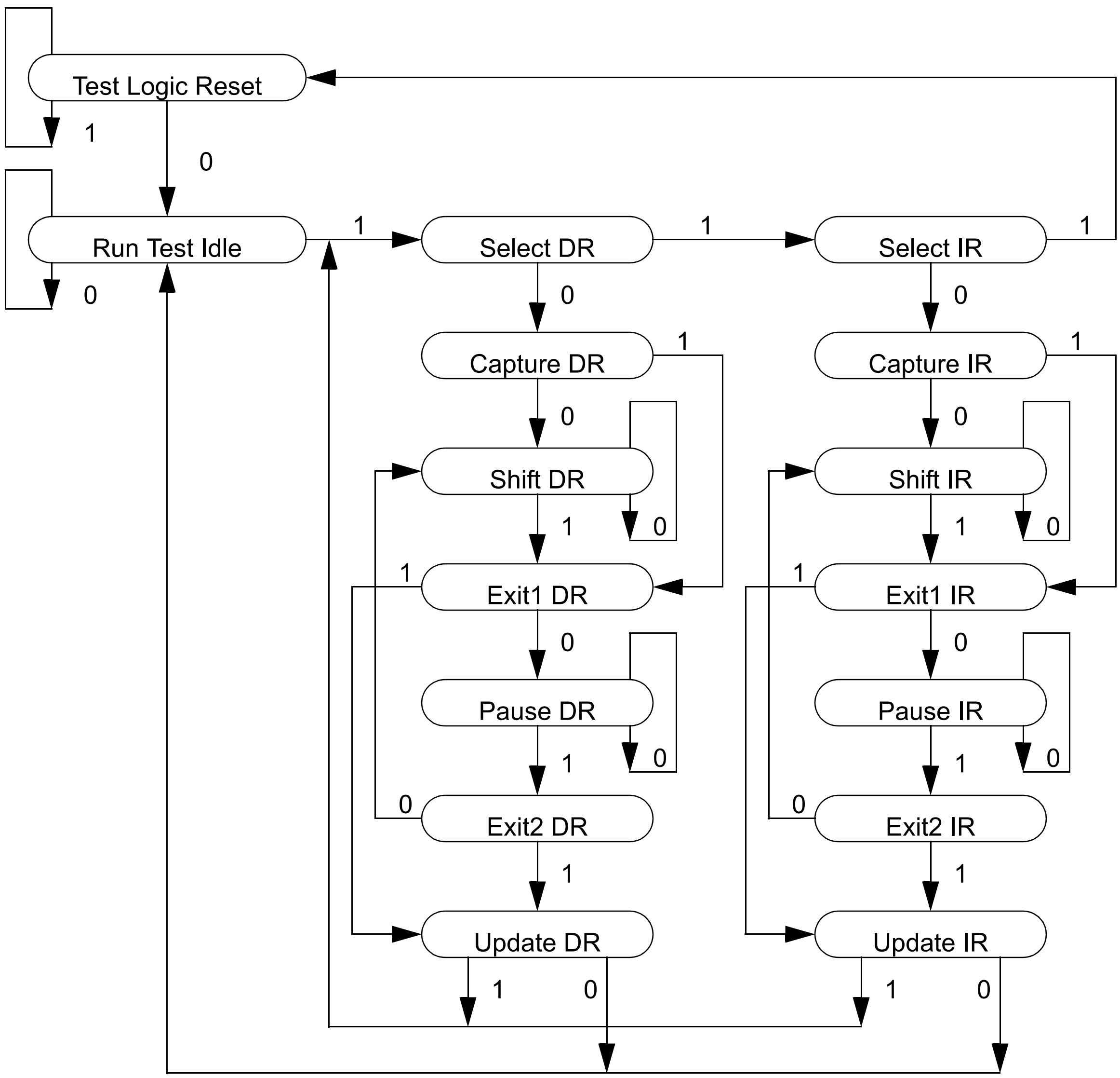
TAP Registers

Name	Length	Description
Instruction	3	Holds instruction for the TAP controller. Loaded when placed between TDI and TDO and automatically loaded with IDCODE at power-up and after a reset.
Boundary Scan	51 for x18 70 for x36	Loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state.
Identification Code	32	The ID register is loaded with a vendor-specific code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. Defined in the ID Register Definition table.
Bypass	1	Register allows serial test data to be shifted through the SRAM with minimal delay.

TAP Controller Instructions

Code	Instruction	Description	Notes
000	EXTEST	Captures I/O ring contents and places boundary scan register between TDI and TDO. Places SRAM outputs in High-Z.	
001	IDCODE	Loads ID register and places it between TDI and TDO.	
010	SAMPLE-Z	Captures I/O ring contents and places boundary scan register between TDI and TDO. Places SRAM outputs in High-Z.	
011	Reserved	Reserved for future, do not use.	
100	SAMPLE/ PRELOAD	Captures I/O ring contents and places boundary scan register between TDI and TDO. Does not implement the preload function.	
101	Reserved	Reserved for future, do not use.	
110	Reserved	Reserved for future, do not use.	
111	BYPASS	Places the bypass register between TDI and TDO.	

TAP Controller State Diagram



Identification Register Description

	Die Revision	Device ID	Device Type	Width & Density	JEDEC ID Code
Bit #s	**31... 28**	**27... 24**	**23... 18**	**17... 12**	**11... 1**
512K x 36	0100	1010	000000	100101	000001101001
1M x 18	0100	1010	000000	010101	000001101001

TAP DC Operating Conditions
3.3V VDDQ

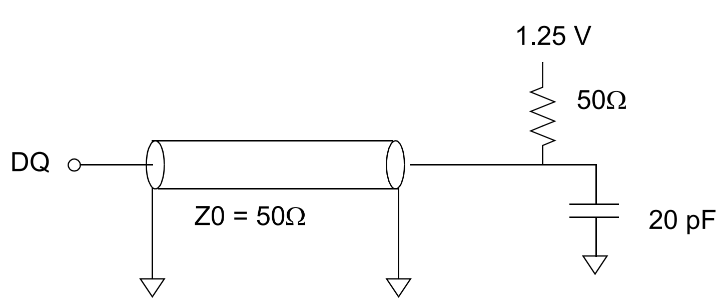
Parameter	Symbol	Min	Max	Unit	Notes
Input High Level	V_{IHT}	2.0	V_{DD} + 0.3	V	
Input Low Level	V_{ILT}	-0.5	0.7	V	
Output High Level	V_{OHT1}	2.4		V	I_{OHT1} = -4.0mA
	V_{OHT2}	2.9		V	I_{OHT2} = -100uA
Output Low Level	O_{ILT1}		0.4	V	I_{OLT1} = 8.0mA
	O_{ILT2}		0.2	V	I_{OLT2} = 100uA
Input Leakage Current	I_{LIT}	-5	5	uA	

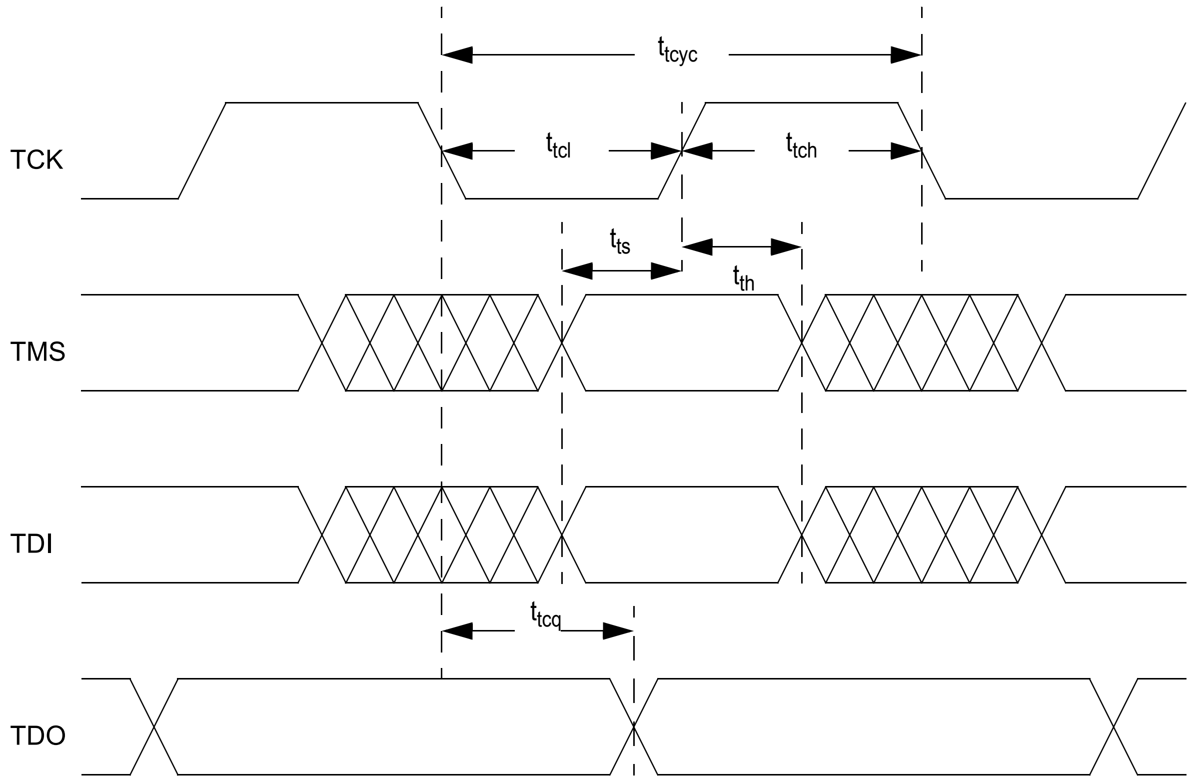
2.5V VDDQ

Parameter	Symbol	Min	Max	Unit	Notes
Input High Level	V_{IHT}	1.7	V_{DD} + 0.3	V	
Input Low Level	V_{ILT}	-0.3	0.7	V	
Output High Level	V_{OHT1}	1.7	-	V	I_{OHT1} = -1.0mA
	V_{OHT2}	2.1	-	V	I_{OHT2} = -100uA
Output Low Level	O_{ILT1}	-	0.7	V	I_{OLT1} = 1.0mA
	O_{ILT2}	-	0.2	V	I_{OLT2} = 100uA
Input Leakage Current	I_{LIT}	-5	5	uA	

TAP AC Test Conditions

Parameter	Conditions
Input High Level	2.5 V
Input Low Level	0.0 V
Input Slew Rate	1 nS
Input and Output Reference Level	1.25 V





TAP AC Timing Characteristics

Parameter	Symbol	Min	Max	Units
TCK Cycle Time	t_{tcyc}	100	-	nS
TCK High Pulse Width	t_{tch}	40	-	nS
TCK Low Pulse Width	t_{tcl}	40	-	nS
TMS / TDI Setup Time	t_{ts}	10	-	nS
TMS / TDI Hold Time	t_{th}	10	-	nS
TCK Low to Output Valid	t_{tcq}	-	20	nS

Boundary Scan Order (119 PBGA)

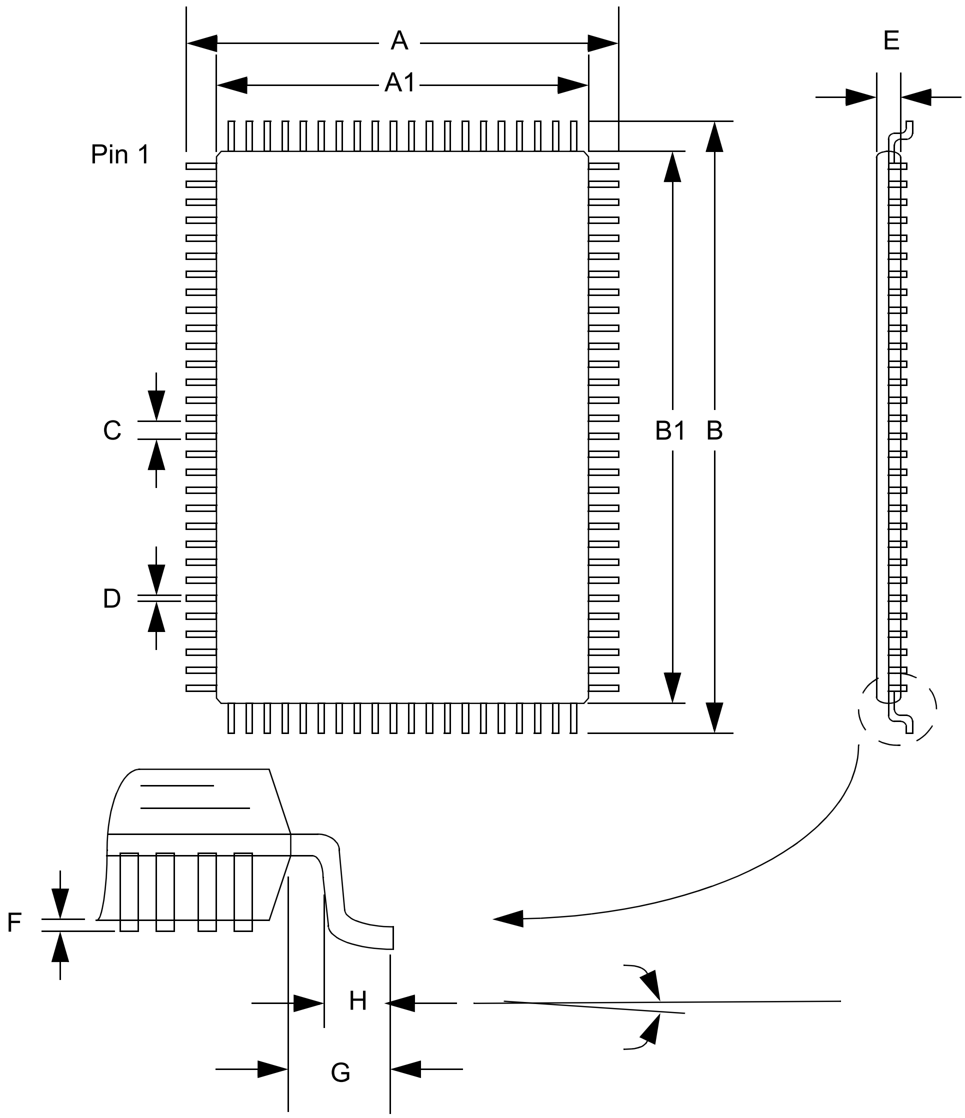
512Kx36

Bit #	Ball	Bump ID	Bit #	Ball	Bump ID
1	tbd	tbd	36	tbd	tbd
2	tbd	tbd	37	tbd	tbd
3	tbd	tbd	38	tbd	tbd
4	tbd	tbd	39	tbd	tbd
5	tbd	tbd	40	tbd	tbd
6	tbd	tbd	41	tbd	tbd
7	tbd	tbd	42	tbd	tbd
8	tbd	tbd	43	tbd	tbd
9	tbd	tbd	44	tbd	tbd
10	tbd	tbd	45	tbd	tbd
11	tbd	tbd	46	tbd	tbd
12	tbd	tbd	47	tbd	tbd
13	tbd	tbd	48	tbd	tbd
14	tbd	tbd	49	tbd	tbd
15	tbd	tbd	50	tbd	tbd
16	tbd	tbd	51	tbd	tbd
17	tbd	tbd	52	tbd	tbd
18	tbd	tbd	53	tbd	tbd
19	tbd	tbd	54	tbd	tbd
20	tbd	tbd	55	tbd	tbd
21	tbd	tbd	56	tbd	tbd
22	tbd	tbd	57	tbd	tbd
23	tbd	tbd	58	tbd	tbd
24	tbd	tbd	59	tbd	tbd
25	tbd	tbd	60	tbd	tbd
26	tbd	tbd	61	tbd	tbd
27	tbd	tbd	62	tbd	tbd
28	tbd	tbd	63	tbd	tbd
29	tbd	tbd	64	tbd	tbd
30	tbd	tbd	65	tbd	tbd
31	tbd	tbd	66	tbd	tbd
32	tbd	tbd	67	tbd	tbd
33	tbd	tbd	68	tbd	tbd
34	tbd	tbd	69	tbd	tbd
35	tbd	tbd	70	tbd	tbd

1M x18

Bit #	Ball	Bump ID	Bit #	Ball	Bump ID
1	tbd	tbd	27	tbd	tbd
2	tbd	tbd	28	tbd	tbd
3	tbd	tbd	29	tbd	tbd
4	tbd	tbd	30	tbd	tbd
5	tbd	tbd	31	tbd	tbd
6	tbd	tbd	32	tbd	tbd
7	tbd	tbd	33	tbd	tbd
8	tbd	tbd	34	tbd	tbd
9	tbd	tbd	35	tbd	tbd
10	tbd	tbd	36	tbd	tbd
11	tbd	tbd	37	tbd	tbd
12	tbd	tbd	38	tbd	tbd
13	tbd	tbd	39	tbd	tbd
14	tbd	tbd	40	tbd	tbd
15	tbd	tbd	41	tbd	tbd
16	tbd	tbd	42	tbd	tbd
17	tbd	tbd	43	tbd	tbd
18	tbd	tbd	44	tbd	tbd
19	tbd	tbd	45	tbd	tbd
20	tbd	tbd	46	tbd	tbd
21	tbd	tbd	47	tbd	tbd
22	tbd	tbd	48	tbd	tbd
23	tbd	tbd	49	tbd	tbd
24	tbd	tbd	50	tbd	tbd
25	tbd	tbd	51	tbd	tbd
26	tbd	tbd			

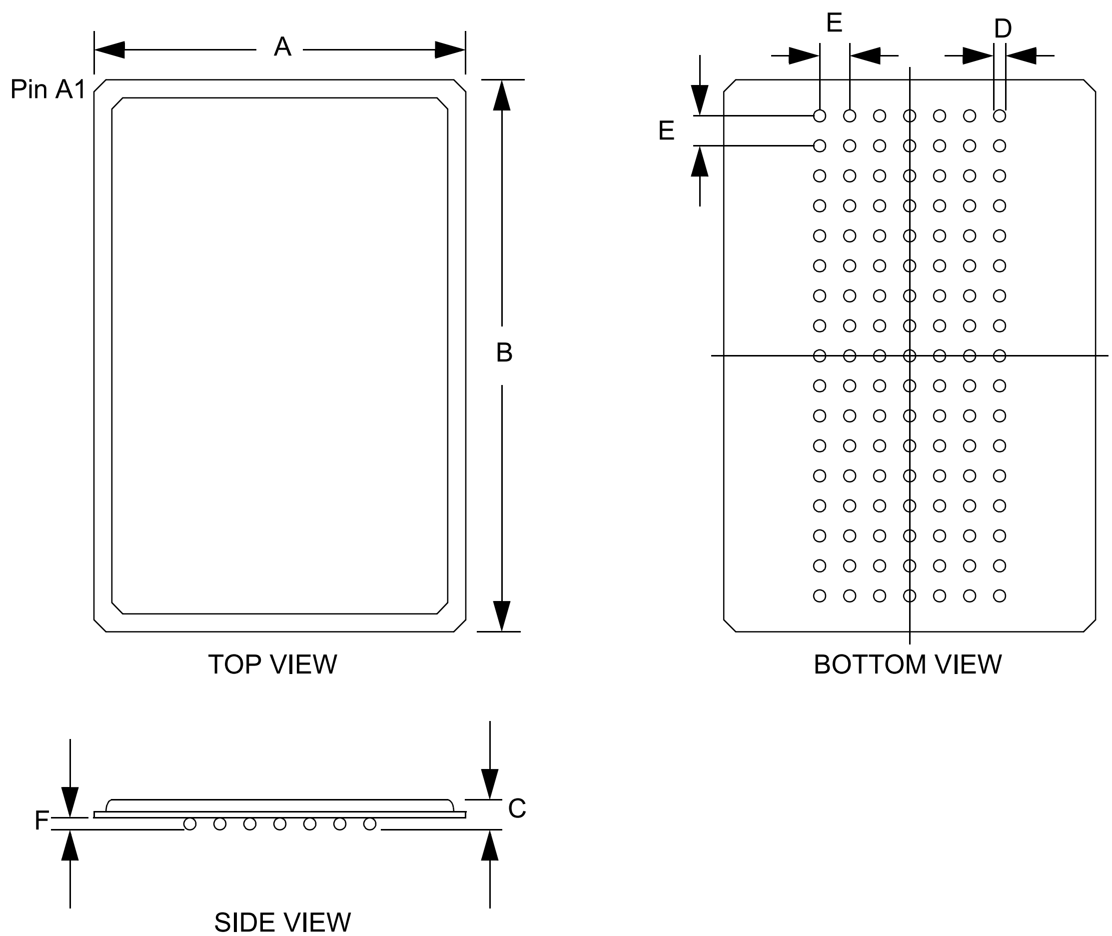
100-Pin TQFP Package Dimensions



All dimensions in mm

Symbol	Description	Min	Nom	Max	Notes
A	Overall Width	15.80	16.00	16.20	
A1	Width	13.90	14.00	14.10	
B	Overall Length	21.80	22.00	22.20	
B1	Length	19.90	20.00	20.10	
C	Pin Pitch		0.65		
D	Lead Width	0.22	0.30	0.38	
E	Package Height	1.35	1.40	1.45	
F	Standoff	0.05		0.15	
G	Lead Extension		1.00		
H	Lead Bend Length	0.45	0.60	0.75	

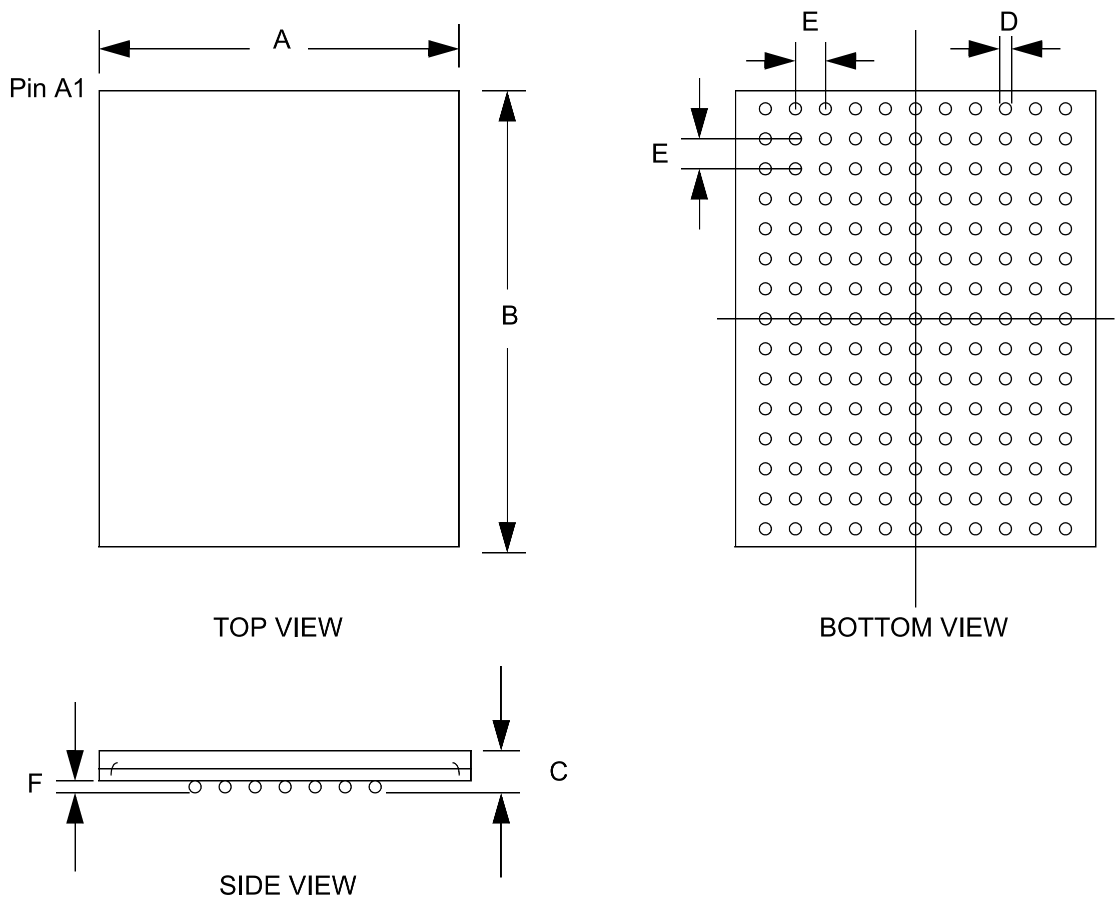
119-Ball BGA Package Dimensions



All Dimensions in mm

Symbol	Description	Min	Nom	Max
A	Package Width	13.80	14.00	14.20
B	Package Length	21.80	22.00	22.20
C	Package Height			2.40
D	Ball Width	0.70	0.75	0.80
E	Ball Pitch		1.27	
F	Ball Height	0.60	0.65	0.70

165-Ball BGA Package Dimen-



All Dimensions in mm

Symbol	Description	Min	Nom	Max
A	Package Width	12.90	13.00	13.10
B	Package Length	14.90	15.00	15.10
C	Package Height			1.20
D	Ball Width	0.40	0.45	0.50
E	Ball Pitch		1.00	
F	Ball Height	0.25		0.40

Ordering Information

N18SxxyyP$Bz- ##C

Valid Part Number	I/O		Vcc		Deselect Cycles		Package		Performance Options
	xx	I/O	yy	Vcc	$	Cycles	z	Package	##
N18S1833P1BQ-	18	x18	33	3.3V	1	1	Q	100-TQFP	16, 20, 22, 25
N18S3633P1BQ-	36	x36	33	3.3V	1	1			
N18S1825P1BQ-	18	x18	25	2.5V	1	1			
N18S3625P1BQ-	36	x36	25	2.5V	1	1			
N18S1833P1BF-	18	x18	33	3.3V	1	1	F	165-FPBGA	
N18S3633P1BF-	36	x36	33	3.3V	1	1			
N18S1825P1BF-	18	x18	25	2.5V	1	1			
N18S3625P1BF-	36	x36	25	2.5V	1	1			
N18S1833P1BG-	18	x18	33	3.3V	1	1	G	119-BGA	
N18S3633P1BG-	36	x36	33	3.3V	1	1			
N18S1825P1BG-	18	x18	25	2.5V	1	1			
N18S3625P1BG-	36	x36	25	2.5V	1	1			
N18S1833P2BQ-	18	x18	33	3.3V	2	2	Q	100-TQFP	
N18S3633P2BQ-	36	x36	33	3.3V	2	2			
N18S1833P2BF-	18	x18	33	3.3V	2	2	F	165-FPBGA	
N18S3633P2BF-	36	x36	33	3.3V	2	2			
N18S1833P2BG-	18	x18	33	3.3V	2	2	G	119-BGA	
N18S3633P2BG-	36	x36	33	3.3V	2	2			

Revision History

Revision #	Date	Change Description
A	June 2003	Initial Release