184-pin Unbuffered DDR DIMM Based on DDR400 32Mx8 SDRAM

Features

- 64Mx64 Unbuffered DDR DIMM based on 32Mx8 DDR SDRAM
- JEDEC Standard 184-pin Dual In-Line Memory Module
- Performance:

		PC3200A	PC3200B	Unit
Speed Sort		-5	-5T	
DIMM $\overline{CAS}$ Latency		2.5	3	
f_{CK}	Clock Frequency	200	200	MHz
t_{CK}	Clock Cycle	5	5	ns
f_{DQ}	DQ Burst Frequency	400	400	MHz

- Intended for 200 MHz applications
- Inputs and outputs are SSTL-2 compatible
- V_{DD} = 2.6Volt ± 0.1, V_{DDQ} = 2.6Volt ± 0.1
- SDRAMs have 4 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- DRAM DLL aligns DQ and DQS transitions with clock transitions
- Address and control signals are fully synchronous to positive clock edge
- Programmable Operation:
  - DIMM $\overline{CAS}$ Latency: 2.5, 3
  - Burst Type: Sequential or Interleave
  - Burst Length: 2, 4, 8
  - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 13/10/2 Addressing (row/column/bank)
- 7.8 μs Max. Average Periodic Refresh Interval
- Serial Presence Detect
- Gold contacts
- SDRAMs in 66-pin TSOP Type II Package
- Lead-free and Halogen-free product available

Description

NT512D64S8HB1G and NT512D64S8HB1GY are unbuffered 184-Pin Double Data Rate (DDR) Synchronous DRAM Dual In-Line Memory Modules (DIMM), organized as a two-bank 64Mx64 high-speed memory array. The module uses sixteen 32Mx8 DDR SDRAMs in 400 mil TSOP II packages. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All NANYA DDR SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint.

The DIMM is intended for use in applications operating up to 200 MHz clock speeds and achieves high-speed data transfer rates of up to 400 MHz. Prior to any access operation, the device $\overline{CAS}$ latency and burst type/ length/operation type must be programmed into the DIMM by address inputs A0-A12 and I/O inputs BA0 and BA1 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial 2,048-bit EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

Ordering Information

Part Number	Speed			Organization	Leads	Power
NT512D64S8HB1G-5	200MHz (5ns @ CL = 2.5)	DDR400A	PC3200A	64Mx64	Gold	2.6V
	166MHz (6ns @ CL = 2.5)					
NT512D64S8HB1G-5T	200MHz (5ns @ CL = 3)	DDR400B	PC3200B	64Mx64	Gold	2.6V
	166MHz (6ns @ CL = 2.5)					
NT512D64S8HB1GY-5*	200MHz (5ns @ CL = 2.5)	DDR400A	PC3200A	64Mx64	Gold	2.6V
	166MHz (6ns @ CL = 2.5)					
NT512D64S8HB1GY-5T*	200MHz (5ns @ CL = 3)	DDR400B	PC3200B	64Mx64	Gold	2.6V
	166MHz (6ns @ CL = 2.5)					

* Lead-free and Halogen-free product

Pin Description

CK0, CK1, CK2, $\overline{\text{CK0}}$, $\overline{\text{CK1}}$, $\overline{\text{CK2}}$	Differential Clock Inputs	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	DQS0-DQS7	Bi-directional data strobes
$\overline{\text{RAS}}$	Row Address Strobe	DM0-DM7	Input Data Mask
$\overline{\text{CAS}}$	Column Address Strobe	VDD	Power (2.6V)
$\overline{\text{WE}}$	Write Enable	VDDQ	Supply voltage for DQs (2.6V)
$\overline{\text{S0}}$, $\overline{\text{S1}}$	Chip Selects	VSS	Ground
A0-A9, A11, A12	Address Inputs	NC	No Connect
A10/AP	Address Input/Autoprecharge	SCL	Serial Presence Detect Clock Input
BA0, BA1	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
VREF	Ref. Voltage for SSTL_2 inputs	SA0-2	Serial Presence Detect Address Inputs
VDDID	VDD Identification flag (Not used when VDD=VDDQ)	VDDSPD	Serial EEPROM positive power supply (2.6V)

Pinout

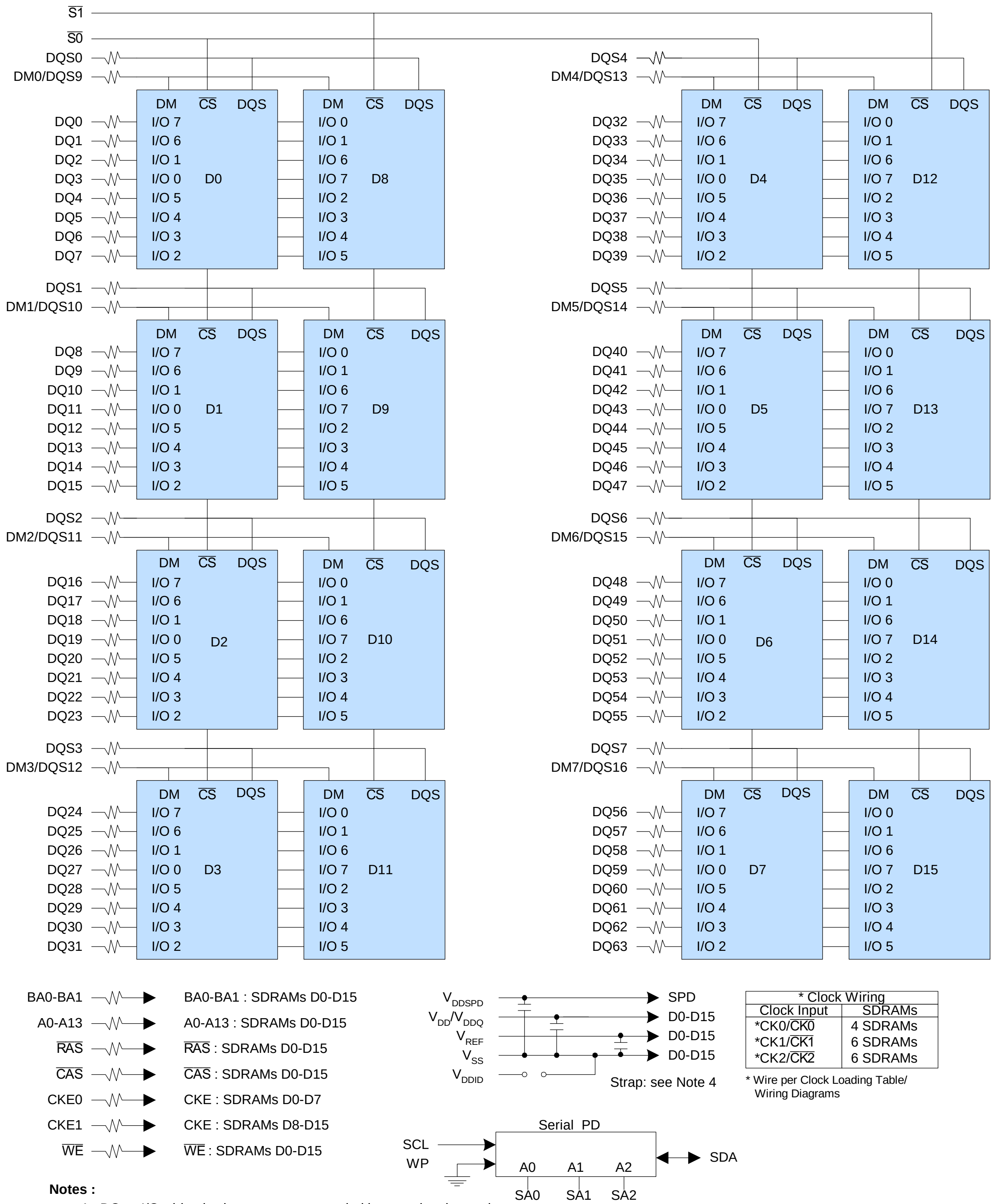
Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREF	93	VSS	32	A5	124	VSS	62	VDDQ	154	$\overline{\text{RAS}}$
2	DQ0	94	DQ4	33	DQ24	125	A6	63	$\overline{\text{WE}}$	155	DQ45
3	VSS	95	DQ5	34	VSS	126	DQ28	64	DQ41	156	VDDQ
4	DQ1	96	VDDQ	35	DQ25	127	DQ29	65	$\overline{\text{CAS}}$	157	$\overline{\text{S0}}$
5	DQS0	97	DM0	36	DQS3	128	VDDQ	66	VSS	158	$\overline{\text{S1}}$
6	DQ2	98	DQ6	37	A4	129	DM3	67	DQS5	159	DM5
7	VDD	99	DQ7	38	VDD	130	A3	68	DQ42	160	VSS
8	DQ3	100	VSS	39	DQ26	131	DQ30	69	DQ43	161	DQ46
9	NC	101	NC	40	DQ27	132	VSS	70	VDD	162	DQ47
10	NC	102	NC	41	A2	133	DQ31	71	NC	163	NC
11	VSS	103	NC	42	VSS	134	NC	72	DQ48	164	VDDQ
12	DQ8	104	VDDQ	43	A1	135	NC	73	DQ49	165	DQ52
13	DQ9	105	DQ12	44	NC	136	VDDQ	74	VSS	166	DQ53
14	DQS1	106	DQ13	45	NC	137	CK0	75	$\overline{\text{CK2}}$	167	NC
15	VDDQ	107	DM1	46	VDD	138	$\overline{\text{CK0}}$	76	CK2	168	VDD
16	CK1	108	VDD	47	NC	139	VSS	77	VDDQ	169	DM6
17	$\overline{\text{CK1}}$	109	DQ14	48	A0	140	NC	78	DQS6	170	DQ54
18	VSS	110	DQ15	49	NC	141	A10	79	DQ50	171	DQ55
19	DQ10	111	CKE1	50	VSS	142	NC	80	DQ51	172	VDDQ
20	DQ11	112	VDDQ	51	NC	143	VDDQ	81	VSS	173	NC
21	CKE0	113	NC	52	BA1	144	NC	82	VDDID	174	DQ60
22	VDDQ	114	DQ20	KEY		KEY		83	DQ56	175	DQ61
23	DQ16	115	A12	53	DQ32	145	VSS	84	DQ57	176	VSS
24	DQ17	116	VSS	54	VDDQ	146	DQ36	85	VDD	177	DM7
25	DQS2	117	DQ21	55	DQ33	147	DQ37	86	DQS7	178	DQ62
26	VSS	118	A11	56	DQS4	148	VDD	87	DQ58	179	DQ63
27	A9	119	DM2	57	DQ34	149	DM4	88	DQ59	180	VDDQ
28	DQ18	120	VDD	58	VSS	150	DQ38	89	VSS	181	SA0
29	A7	121	DQ22	59	BA0	151	DQ39	90	WP	182	SA1
30	VDDQ	122	A8	60	DQ35	152	VSS	91	SDA	183	SA2
31	DQ19	123	DQ23	61	DQ40	153	DQ44	92	SCL	184	VDDSPD

Note: All pin assignments are consistent for all 8-byte unbuffered versions.

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0, CK1, CK2	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs. All the DDR SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
$\overline{CK0}$, $\overline{CK1}$, $\overline{CK2}$	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self-Refresh mode.
$\overline{S0}$, $\overline{S1}$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL-2 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA0, BA1	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP A11, A12	(SSTL)	-	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A8 defines the column address (CA0-CA8) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Auto-precharge operation at the end of the Burst Read or Write cycle. If AP is high, auto-precharge is selected and BA0/BA1 define the bank to be precharged. If AP is low, auto-precharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 - DQ63	(SSTL)	-	Data and Check Bit input/output pins operate in the same manner as on conventional DRAMs.
DQS0 - DQS7	(SSTL)	Active High	Data strobes: Output with read data, input with write data. Edge aligned with read data, centered on write data. Used to capture write data.
DM0 - DM7	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic
SA0 - SA2		-	Address inputs. Connected to either V_{DD} or V_{SS} on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pullup.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pullup.
V_{DDSPD}	Supply		Serial EEPROM positive power supply.

Functional Block Diagram (2 Bank, 32Mx8 DDR SDRAMs)



Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): V_{DD} is not equal to V_{DDQ}.

Serial Presence Detect -- Part 1 of 2

64Mx64 SDRAM DIMM based on 32Mx8, 4Banks, 8K Refresh, 2.6V DDR SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		DDR400A -5	DDR400B -5T	DDR400A -5	DDR400B -5T	
0	Number of Serial PD Bytes Written during Production	128		80		
1	Total Number of Bytes in Serial PD device	256		08		
2	Fundamental Memory Type	SDRAM DDR		07		
3	Number of Row Addresses on Assembly	13		0D		
4	Number of Column Addresses on Assembly	10		0A		
5	Number of DIMM Bank	2		02		
6	Data Width of Assembly	X64		40		
7	Data Width of Assembly (cont')	X64		00		
8	Voltage Interface Level of this Assembly	SSTL 2.5V		04		
9	DDR SDRAM Device Cycle Time at CL=3	5ns	5ns	50	50	
10	DDR SDRAM Device Access Time from Clock at CL=3	0.60ns	0.60ns	60	60	
11	DIMM Configuration Type	Non-Parity		00		
12	Refresh Rate/Type	SR/1x(7.8us)		82		
13	Primary DDR SDRAM Width	X8		08		
14	Error Checking DDR SDRAM Device Width	N/A		00		
15	DDR SDRAM Device Attr: Min CLK Delay, Random Col Access	1 Clock		01		
16	DDR SDRAM Device Attributes: Burst Length Supported	2,4,8		0E		
17	DDR SDRAM Device Attributes: Number of Device Banks	4		04		
18	DDR SDRAM Device Attributes: CAS Latencies Supported	2.5/3	2/2.5/3	18	1C	
19	DDR SDRAM Device Attributes: CS Latency	0		01		
20	DDR SDRAM Device Attributes: WE Latency	1		02		
21	DDR SDRAM Device Attributes:	Differential Clock		20		
22	DDR SDRAM Device Attributes: General	+/-0.1V Voltage Tolerance		00		
23	Minimum Clock Cycle at CL=2.5	5ns	6ns	50	60	
24	Maximum Data Access Time from Clock at CL=2.5	0.6ns	0.7ns	60	70	
25	Minimum Clock Cycle Time at CL=2	N/A	7.5ns	00	75	
26	Maximum Data Access Time from Clock at CL=2	N/A	7.5ns	00	75	
27	Minimum Row Precharge Time (t_{RP})	15ns	15ns	3C	3C	
28	Minimum Row Active to Row Active delay (t_{RRD})	10ns	10ns	28	28	
29	Minimum RAS to CAS delay (t_{RCD})	15ns	15ns	3C	3C	
30	Minimum RAS Pulse Width (t_{RAS})	40ns	40ns	28	28	
31	Module Bank Density	256MB		40		
32	Address and Command Setup Time Before Clock	0.6ns	0.6ns	60	60	
33	Address and Command Hold Time After Clock	0.6ns	0.6ns	60	60	
34	Data Input Setup Time Before Clock	0.4ns	0.4ns	40	40	
35	Data Input Hold Time After Clock	0.4ns	0.4ns	40	40	
36-40	Reserved	Undefined		00		
41	Minimum Active/Auto-Refresh Time (t_{RC})	55ns	55ns	37	37	
42	SDRAM Device Minimum Auto-Refresh to Active/Auto-Refresh Command Period (t_{RFC})	70ns	70ns	46	46	
43	SDRAM Device Maximum Cycle Time (t_{CK} max)	8	8	20	20	
44	SDRAM Device DQS-DQ Skew Time (t_{DQSQ})	0.4	0.4	28	28	
45	SDRAM Device Maximum Read Data Hold Skew Factor (t_{QHS})	0.5	0.5	50	50	
46-61	Superset Information (Reserved)	Undefined		00		
62	SPD Revision	Initial	Initial	00	00	
63	Checksum Data			81	8F	

Serial Presence Detect -- Part 2 of 2

64Mx64 SDRAM DIMM based on 32Mx8, 4Banks, 8K Refresh, 2.6V DDR SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		DDR400A -5	DDR400B -5T	DDR400A -5	DDR400B -5T	
64-71	Manufacturer's JEDEC ID Code	NANYA		7F7F7F0B00000000		
72	Module Manufacturing Location	N/A		00		
73-90	Module Part number	N/A	N/A	00	00	
91-92	Module Revision Code	N/A		00		
93-94	Module Manufacturing Data	Year/Week Code		yy/ww		1, 2
95-98	Module Serial Number	Serial Number		00		
99-255	Reserved	Undefined		00		

1. yy= Binary coded decimal year code, 0-99(Decimal), 00-63(Hex)
2. ww= Binary coded decimal year code, 01-52(Decimal), 01-34(Hex)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.5 to VDDQ+0.5	V
V_{IN}	Voltage on Input relative to Vss	-0.5 to +3.6	V
V_{DD}	Voltage on VDD supply relative to Vss	-0.5 to +3.6	V
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-0.5 to +3.6	V
T_A	Operating Temperature (Ambient)	0 to +70	°C
T_{STG}	Storage Temperature (Plastic)	-55 to +150	°C
P_D	Power Dissipation	16	W
I_{OUT}	Short Circuit Output Current	50	mA

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance

Parameter	Symbol	Max.	Units	Notes
Input Capacitance: CK0, $\overline{CK0}$, CK1, $\overline{CK1}$, CK2, $\overline{CK2}$	C_{I1}	TBD	pF	1
Input Capacitance: A0-A12, BA0, BA1, $\overline{WE}$, $\overline{RAS}$, $\overline{CAS}$, CKE0, CKE1, $\overline{S0}$, $\overline{S1}$	C_{I2}	TBD	pF	1
Input Capacitance: SA0-SA2, SCL	C_{I4}	TBD	pF	1
Input/Output Capacitance: DQ0-63; DQS0-7	C_{IO1}	TBD	pF	1, 2
Input/Output Capacitance: SDA	C_{IO3}	TBD	pF	

1. $V_{DDQ} = V_{DD} = 2.6V \pm 0.1V$, f = 100 MHz, T_A = 25 °C, V_{OUT} (DC) = $V_{DDQ}/2$, V_{OUT} (Peak to Peak) = 0.2V.
2. DQS inputs are grouped with I/O pins reflecting the fact that they are matched in loading to DQ and DQS to facilitate trace matching at the board level.

DC Electrical Characteristics and Operating Conditions

(TA = 0 °C ~ 70 °C; V_{DDQ} = 2.6V ± 0.1V; V_{DD} = 2.6V ± 0.1V, See AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	2.5	2.7	V	1
V_{DDQ}	I/O Supply Voltage	2.5	2.7	V	1
V_{SS}, V_{SSQ}	Supply Voltage, I/O Supply Voltage	0	0	V	
V_{REF}	I/O Reference Voltage	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	1, 2
V_{TT}	I/O Termination Voltage (System)	V_{REF} – 0.04	V_{REF} + 0.04	V	1, 3
V_{IH} (DC)	Input High (Logic1) Voltage	V_{REF} + 0.15	V_{DDQ} + 0.3	V	1
V_{IL} (DC)	Input Low (Logic0) Voltage	-0.3	V_{REF}- 0.15	V	1
V_{IN} (DC)	Input Voltage Level, CK and $\overline{CK}$ Inputs	-0.3	V_{DDQ} + 0.3	V	1
V_{ID} (DC)	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.30	V_{DDQ} + 0.6	V	1, 4
I_I	Input Leakage Current Any input 0V ≤ V_{IN} ≤ V_{DD}; (All other pins not under test = 0V)	-5	5	uA	1
I_{OZ}	Output Leakage Current (DQs are disabled; 0V ≤ V_{out} ≤ V_{DDQ}	-5	5	uA	1
I_{OH}	Output High Current (V_{OUT} = V_{DDQ} -0.373V, min V_{REF}, min V_{TT})	-16.8	-	mA	1
I_{OL}	Output Low Current (V_{OUT} = 0.373, max V_{REF}, max V_{TT})	16.8	-	mA	1

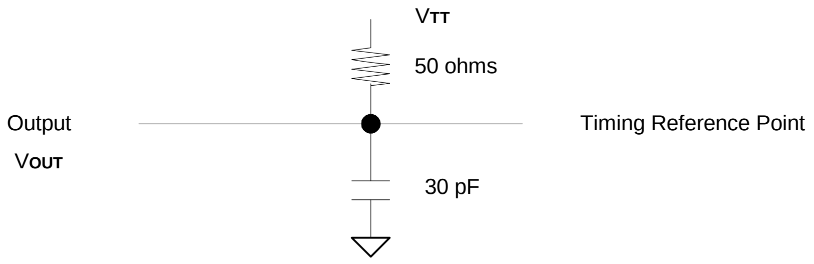
1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
3. V_{TT} is not applied directly to the DIMM. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF} .
4. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

AC Characteristics

(Notes 1-5 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, Operating, Standby, and Refresh Currents, and Electrical Characteristics and AC Timing.)

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load. Refer to the AC Output Load Circuit below.
4. AC timing and I_{DD} tests may use a V_{IL} to V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK, $\overline{CK}$), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between $V_{IL\ (AC)}$ and $V_{IH\ (AC)}$ unless otherwise specified.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.

AC Output Load Circuits



AC Operating Conditions

(TA = 0 °C ~ 70 °C; V_{DDQ} = 2.6V ± 0.1V; V_{DD} = 2.6V ± 0.1V, See AC Characteristics)

Symbol	Parameter/Condition	Min	Max	Unit	Notes
$V_{IH\ (AC)}$	Input High (Logic 1) Voltage	V_{REF} + 0.31	-	V	1, 2
$V_{IL\ (AC)}$	Input Low (Logic 0) Voltage	-	V_{REF} - 0.31	V	1, 2
$V_{ID\ (AC)}$	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.62	V_{DDQ} + 0.6	V	1, 2, 3
$V_{IX\ (AC)}$	Input Differential Pair Cross Point Voltage, CK and $\overline{CK}$ Inputs	0.5 x V_{DDQ} - 0.2	0.5 x V_{DDQ} + 0.2	V	1, 2, 4

1. Input slew rate = 1V/ ns.
2. Inputs are not recognized as valid until V_{REF} stabilizes.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
4. The value of V_{IX} is expected to equal 0.5 x V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

Operating, Standby, and Refresh Currents

(TA = 0 °C ~ 70 °C; V_{DDQ} = 2.6V ± 0.1V; V_{DD} = 2.6V ± 0.1V, See AC Characteristics)

Symbol	Parameter/Condition	PC3200A (-5)	PC3200B (-5T)	Unit	Notes
I DD0	Operating Current: one bank; active/precharge; tRC = tRC (MIN); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1320	1320	mA	1, 2
I DD1	Operating Current: one bank; active/read/precharge; Burst = 2; tRC = tRC (MIN); CL=2.5; tCK = tCK (MIN); IOUT = 0mA; address and control inputs changing once per clock cycle	1500	1500	mA	1, 2
I DD2P	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ VIL (MAX); tCK = tCK (MIN)	280	280	mA	1, 2
I DD2N	Idle Standby Current: CS ≥ VIH (MIN); all banks idle; CKE ≥ VIH (MIN); tCK = tCK (MIN); address and control inputs changing once per clock cycle	680	680	mA	1, 2
I DD3P	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ VIL (MAX); tCK = tCK (MIN)	280	280	mA	1, 2
I DD3N	Active Standby Current: one bank; active/precharge; CS ≥ VIH (MIN); CKE ≥ VIH (MIN); tRC = tRAS (MAX); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	940	940	mA	1, 2
I DD4R	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; tCK = tCK (MIN); IOUT = 0mA	2180	2180	mA	1, 2
I DD4W	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; tCK = tCK (MIN)	1700	1700	mA	1, 2
I DD5	Auto-Refresh Current: tRC = tRFC (MIN)	2100	2100	mA	1, 2, 4
I DD6	Self-Refresh Current: CKE ≤ 0.2V	48	48	mA	1, 2
I DD7	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; tRC = tRC (min); IOUT = 0mA.	3200	3200	mA	1, 2

1. I DD specifications are tested after the device is properly initialized.
2. Input slew rate = 1V/ ns.
3. Enables on-chip refresh and address counters.
4. Current at 7.8 µs is time-averaged value of IDD5 at tRFC (MIN) and IDD2P over 7.8 µs.

AC Timing Specifications for DDR SDRAM Devices Used on Module

(TA = 0 °C ~ 70 °C; V_{DDQ} = 2.6V ± 0.1V; V_{DD} = 2.6V ± 0.1V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter		-5		-5T		Unit	Notes
			Min.	Max.	Min.	Max.		
tAC	DQ output access time from CK/$\overline{CK}$		-0.6	+0.6	-0.6	+0.6	ns	1-4
tDQSCK	DQS output access time from CK/$\overline{CK}$		-0.5	+0.5	-0.5	+0.5	ns	1-4
tCH	CK high-level width		0.45	0.55	0.45	0.55	tCK	1-4
tCL	CK low-level width		0.45	0.55	0.45	0.55	tCK	1-4
tCK	Clock cycle time	CL=3	5	8	5	8	ns	1-4
tCK		CL=2.5	5	12	6	12	ns	1-4
tCK		CL=2	-	-	7.5	12	ns	1-4
tDH	DQ and DM input hold time		0.4		0.4		ns	1-4, 15, 16
tDS	DQ and DM input setup time		0.4		0.4		ns	1-4, 15, 16
tIPW	Input pulse width		2.2		2.2		ns	2-4, 12
tDIPW	DQ and DM input pulse width (each input)		1.75		1.75		ns	1-4
tHZ	Data-out high-impedance time from CK/$\overline{CK}$		-0.6	+0.6	-0.6	+0.6	ns	1-4, 5
tLZ	Data-out low-impedance time from CK/$\overline{CK}$		-0.6	+0.6	-0.6	+0.6	ns	1-4, 5
tDQSQ	DQS-DQ skew (DQS & associated DQ signals)			0.4		0.4	ns	1-4
tHP	Minimum half clk period for any given cycle; defined by clk high (tCH) or clk low (tCL) time		t_{CH} or t_{CL}		t_{CH} or t_{CL}		tCK	1-4
tQH	Data output hold time from DQS		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		tCK	1-4
tQHS	Data hold Skew Factor			0.5ns		0.5ns	tCK	1-4
tDQSS	Write command to 1st DQS latching transition		0.72	1.28	0.72	1.28	tCK	1-4
tDQSL,H	DQS input low (high) pulse width (write cycle)		0.35		0.35		tCK	1-4
tDSS	DQS falling edge to CK setup time (write cycle)		0.2		0.2		tCK	1-4
tDSH	DQS falling edge hold time from CK (write cycle)		0.2		0.2		tCK	1-4
tMRD	Mode register set command cycle time		2		2		tCK	1-4
tWPRES	Write preamble setup time		0		0		ns	1-4, 7
tWPST	Write postamble		0.40	0.60	0.40	0.60	tCK	1-4, 6
tWPRE	Write preamble		0.25		0.25		tCK	1-4
tIH	Address and control input hold time (fast slew rate)		0.6		0.6		ns	2-4, 9, 11, 12
tIS	Address and control input setup time (fast slew rate)		0.6		0.6		ns	2-4, 9, 11, 12
tIH	Address and control input hold time (slow slew rate)		0.7		0.7		ns	2-4, 10, 11, 12, 14
tIS	Address and control input setup time (slow slew rate)		0.7		0.7		ns	2-4, 10-12, 14

AC Timing Specifications for DDR SDRAM Devices Used on Module

(TA = 0 °C ~ 70 °C; V_{DDQ} = 2.6V ± 0.1V; V_{DD} = 2.6V ± 0.1V, See AC Characteristics) (Part 2 of 2)

Symbol	Parameter	-5		-5T		Unit	Notes
		Min.	Max.	Min.	Max.		
tRPRE	Read preamble	0.9	1.1	0.9	1.1	tCK	1-4
tRPST	Read postamble	0.40	0.60	0.40	0.60	tCK	1-4
tRAS	Active to Precharge command	40	120,000	40	120,000	ns	1-4
tRC	Active to Active/Auto-refresh command period	55		55		ns	1-4
tRFC	Auto-refresh to Active/Auto-refresh command period	70		70		ns	1-4
tRCD	Active to Read or Write delay	15		15		ns	1-4
tRAP	Active to Read Command with Autoprecharge	15		15		ns	1-4
tRP	Precharge command period	15		15		ns	1-4
tRRD	Active bank A to Active bank B command	10		10		ns	1-4
tWR	Write recovery time	15		15		ns	1-4
tDAL	Auto precharge write recovery + precharge time	(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		tCK	1-4, 13
tWTR	Internal write to read command delay	2		2		tCK	1-4
tPDEX	Power down exit time	5		5		ns	1-4
tXSNR	Exit self-refresh to non-read command	75		75		ns	1-4
tXSRD	Exit self-refresh to read command	200		200		tCK	1-4
tREFI	Average Periodic Refresh Interval		7.8		7.8	µs	1-4, 8

AC Timing Specification Notes

1. Input slew rate = 1V/ns.
2. The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$ is V_{REF}.
3. Inputs are not recognized as valid until V_{REF} stabilizes.
4. The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (Note 3) is V_{TT}.
5. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
6. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
7. The specific requirement is that DQS be valid (high, low, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from high to low at this time, depending on tDQSS.
8. A maximum of eight Auto refresh commands can be posted to any given DDR SDRAM device.
9. For command/address input slew rate >= 1.0 V/ns. Slew rate is measured between V_{OH} (AC) and V_{OL} (AC).
10. For command/address input slew rate >= 0.5 V/ns and < 1.0 V/ns. Slew rate is measured between V_{OH} (AC) and V_{OL} (AC).
11. CK/$\overline{CK}$ slew rates are >= 1.0 V/ns.
12. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester characterization.
13. For each of the terms in parentheses, if not already an integer, round to the next highest integer. t CK is equal to the actual system clock cycle time. For example, for PC2100 at CL= 2.5, t DAL = (15ns/7.5ns) +(20ns/7.0ns) = 2 + 3 = 5.
14. An input setup and hold time derating table is used to increase t IS and t IH in the case where the input slew rate is below 0.5 V/ns.

Input Slew Rate	Delta (tIS)	Delta (tIH)	Unit	Note
0.5 V/ns	0	0	ps	1, 2
0.4 V/ns	+50	0	ps	1, 2
0.3 V/ns	+100	0	ps	1, 2

1. Input slew rate is based on the lesser of the slew rates determined by either $V_{IH (AC)}$ to $V_{IL (AC)}$ or $V_{IH (DC)}$ to $V_{IL (DC)}$, similarly for rising transitions.
2. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

15. An input setup and hold time derating table is used to increase t DS and t DH in the case where the I/O slew rate is below 0.5 V/ns.

Input Slew Rate	Delta (tDS)	Delta (tDH)	Unit	Note
0.5 V/ns	0	0	ps	1, 2
0.4 V/ns	+75	+75	ps	1, 2
0.3 V/ns	+150	+150	ps	1, 2

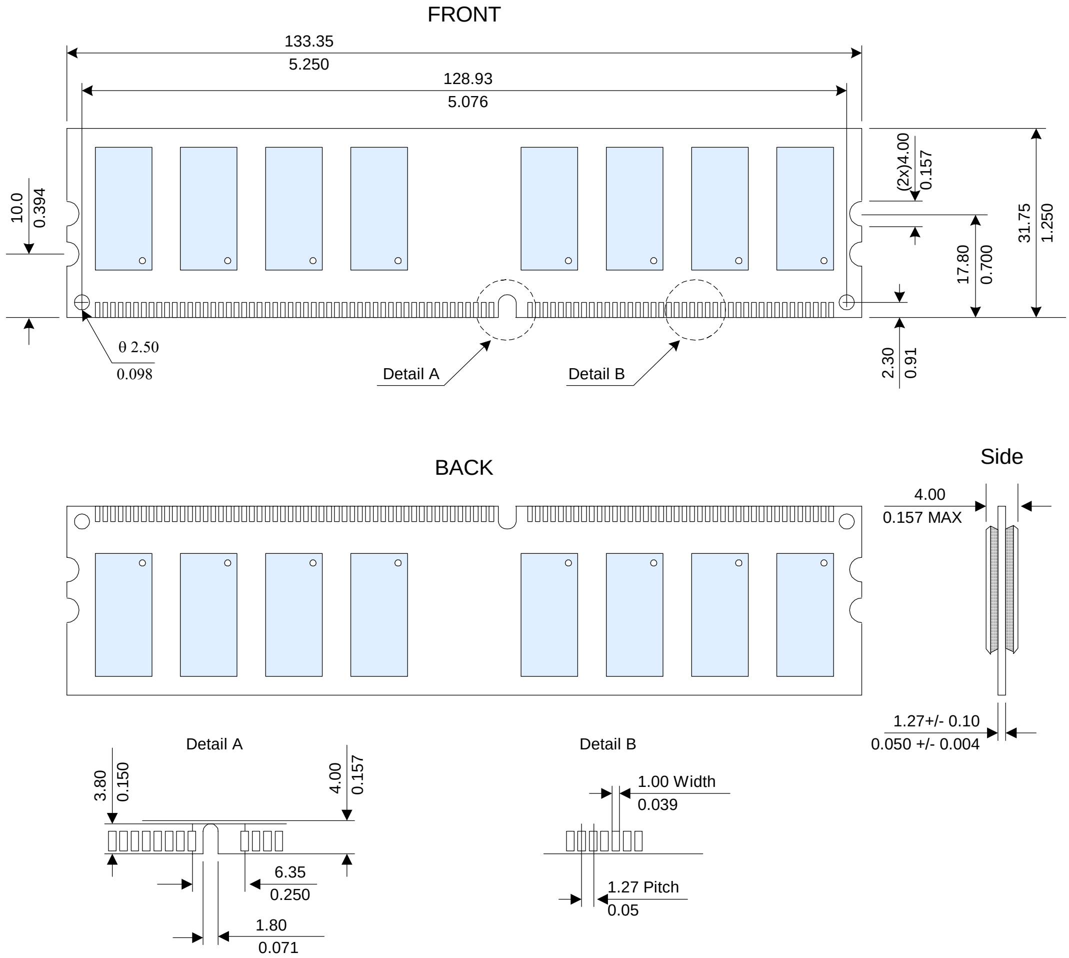
1. I/O slew rate is based on the lesser of the slew rates determined by either $V_{IH (AC)}$ to $V_{IL (AC)}$ or $V_{IH (DC)}$ to $V_{IL (DC)}$, similarly for rising transitions.
2. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

16. An I/O Delta Rise, Fall Derating table is used to increase t DS and t DH in the case where DQ, DM, and DQS slew rates differ.

Delta Rise and Fall Rate	Delta (tDS)	Delta (tDH)	Unit	Note
0.0 ns/V	0	0	ps	1-4
0.25 ns/V	+50	+50	ps	1-4
0.5 ns/V	+100	+100	ps	1-4

1. Input slew rate is based on the lesser of the slew rates determined by either $V_{IH (AC)}$ to $V_{IL (AC)}$ or $V_{IH (DC)}$ to $V_{IL (DC)}$, similarly for rising transitions.
2. Input slew rate is based on the larger of AC to AC delta rise, fall rate and DC to DC delta rise, fall rate.
3. The delta rise, fall rate is calculated as: [1/(slew rate 1)] - [1/(slew rate 2)]
   For example: slew rate 1 = 0.5 V/ns; slew rate 2 = 0.4 V/ns. Delta rise, fall = (1/0.5) - (1/0.4) [ns/V] = -0.5 ns/V
   Using the table above, this would result in an increase in t_{DS} and t_{DH} of 100 ps.
4. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

Package Dimensions



Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated.

Units: Millimeters (Inches)

Revision Log

Rev	Date	Modification
0.1	01/2003	Preliminary Release
0.2	02/2003	Updated SPD Table
0.3	02/2003	Updated t_{QHS} from 0.55ns to 0.5ns in AC Timing Specifications Table
0.4	03/2003	Added DDR400B (-5T) speed grade
1.0	04/2003	Updated I_{DD} values in Operating, Standby, and Refresh Currents Table
		Official Release
1.1	06/2003	Added Lead-free and Halogen-free product part numbers