NEC Electronics Inc.

EA-C9
3.3-Volt, 0.35-Micron (drawn) CMOS Embedded Array

Preliminary

March 1997

Description

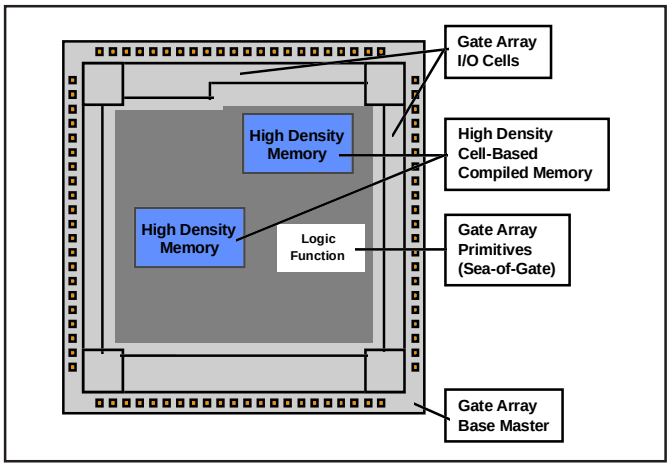
NEC's high-performance 0.35 µm drawn (0.27 µm L-effective) EA-C9 embedded array family offers both support for embedded high-density macros as well as the short turnaround time of a gate array resulting in a time-to-market advantage. In this product, NEC combines high-performance CMOS gate array primitives with diffused, embedded blocks such as RAM and ROM.

EA-C9 features 2- and 3- level metal CMOS technology with an extensive family of interface macros to support very high-speed system clocks such as GTL, GTL+, HSTL, and pECL. PCI signaling standards are also supported including 3.3V 66 MHz PCI. This technology is enhanced by a set of advanced features including phase-locked loops, clock tree synthesis, and high-speed memory.

The EA-C9 embedded array family of 3.3V devices consists of 18 masters, offered in densities of 190K raw gates to 1.5 million raw gates. Usable gates range from 76K to 927K used gates.

As the EA-C9 ASIC family follows basically a gate array approach, it offers short turnaround times for silicon processing and lower development costs compared to cell-based ASICs. The turnaround time is kept short by fixing the embedded core locations and beginning prototype fabrication in parallel with place and route design steps.

Figure 1. Embedded Array Core Integration



Applications

The EA-C9 family is ideal for applications where high density is mandatory and a short time-to-market path is required. For example, RAM-dominated designs can be realized with reduced die size and a reasonable turn-around time. EA-C9 is well-suited for designs that may require rework, because the logic function portion of the design uses gate array primitives created just by the final metal masks. Typical applications include engineering workstations, telecommunications systems, advanced graphics and low power applications where very high performance is required.

Table 1. EA-C9 Series Features and Benefits

EA-C9 Series Features	EA-C9 Series Benefits
• 0.35 µm (drawn) 2- and 3-level metal CMOS technology	⇒ Delivers dense cell structure and high speed
• Advanced embedded array architecture	⇒ Enables fast TAT and dense memories
• Eighteen base arrays with raw gates from 190K to 1.5M	⇒ Provides many base sizes to give best fit to design needs
• Narrow pad pitch for maximum gate to pad ratio	⇒ Minimizes device cost
• Pad counts from 300 to 1060M	⇒ Support high I/O integration and wide system bus widths
• GTL, GTL+, pECL, and all four classes of HSTL	⇒ Interfaces to high speed memory and processor buses
• Full range of 5V-protected I/O buffers	⇒ Allows interface with 5V logic while protecting 3.3V ASIC
• PCI buffers including 3.3V 66 MHz PCI buffer	⇒ Supports signaling methods defined in the PCI Specification
• Digital Phase-Locked Loop (DPLL) macros	⇒ Eliminates clock insertion delay, reduces total clock skew
• Low power dissipation: 0.9 µW/MHz/gate	⇒ Provides low power consumption at high system clock rates
• Extensive package offering: PQFP, TQFP, BGA, TAB	⇒ Delivers customer-specific package requirements
• Clock Tree Synthesis tool automates clock tree design	⇒ Minimizes on-chip clock skew for high performance
• Floorplanner supplies layout information for resynthesis	⇒ Reduces design time and improves device performance
• Popular, third-party CAE tools supported	⇒ Enables a smooth flow from customer design to silicon

Array Architecture

The EA-C9 gate array family is built with NEC's 0.35-micron (drawn) channelless array architecture. As shown in Figure 2, the array is divided into I/O and core regions. The I/O region contains input and output buffers. The core region contains the sea-of-gates array and embedded blocks.

The EA-C9 gate arrays architecture provides extra flexibility for high performance system designs. As shown in Figure 2, the arrays contain two power rails: a 3.3V rail, and a second power rail (V_{DD2}) for special I/O types.

The V_{DD2} rail is used for interfaces such as HSTL where a very low I/O power supply is required (1.4 to 1.6V). All four classes of HSTL buffer are supported.

The V_{DD2} rail may be separated into sections to allow one device to support two or more buses requiring special I/O voltages. Examples of spread I/O cells that may use this V_{DD} rail are HSTL and 5V PCI. Each section can operate as an independent voltage zone, and sections can be linked together to form common voltage zones.

Core Region

The core region consists of an array of gates. Each gate contains 2 n-channel and 2 p-channel MOS logic transistors. One core gate is equivalent to one 2-input NAND gate (L302). The logic transistors are sized to offer a superior ratio of speed to silicon area.

Table 2. EA-C9 Base Array Line-up

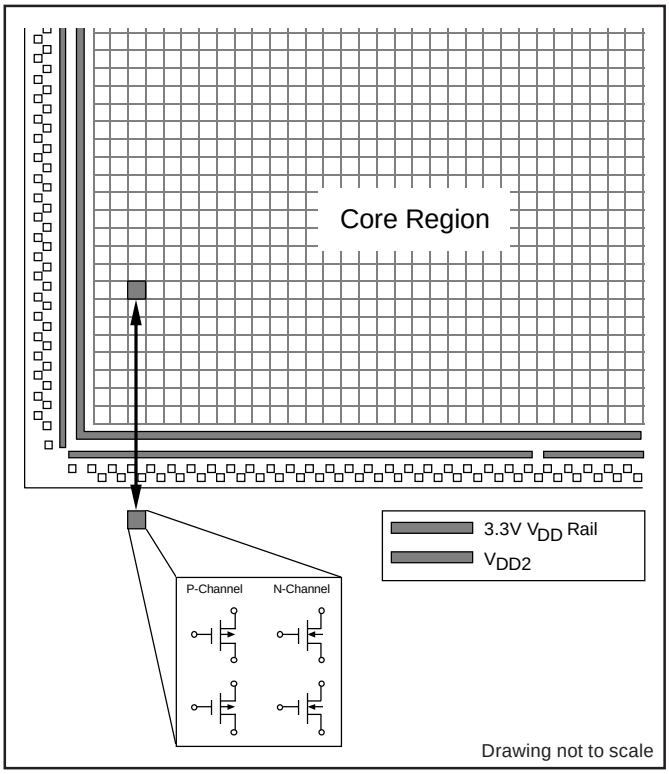
Device[1] (μPD654xx)		Available	Usable Gates[2]		Max Pads Reg.	Max Pads Tight
2LM	3LM	Gates	2LM	3LM	Pitch	Pitch
06	26	190152	76061	114091	300	388
07	27	249948	99979	149969	340	444
08	28	317904	127162	190742	380	500
09	29	376740	150696	226044	412	540
10	30	462088	184835	277253	452	596
11	31	629824	251930	377894	524	692
13	33	805580	322232	483348	588	772
15	35	1076032	430413	645619	676	892
17	37	1545240	618096	927144	804	1060

Notes:

(1) 2LM represents two-layer metal; "3LM" represents three-layer metal.

(2) Actual gate utilization varies depending on circuit implementation. Utilization is 40% for 2LM; 60% for 3LM.

Figure 2. Power Rail Structure



The embedded array approach allows the combination of high-density cores with a prototype turnaround time equal to gate arrays. Embedded blocks such as RAM and ROM can be placed into the sea-of-gates area within the EA-C9 base master. The area used for these blocks is defined by pre-diffusion. The logical function is created by the final metalization masks. This enables the usage of a gate array master and digital macros from the cell-based technology CB-C9. Cores from the BiCMOS QB-9 family may also be embedded.

Various kinds of memory macros are available for EA-C9. Designers can select either gate array memory compilers using gate array cells or cell-based compilers which offer higher density and faster access times. Cell-based type memory blocks are generated based on advanced memory compiler tools and thus ensure highest flexibility for design requirements. The available memory types are described in Table 3.

Table 3. EA-C9 Compiled Memory Types

Family	Type	Mode	Ports	Word Size	Max. Size
CB-IC	High-speed	Sync.	1	1-32 bits	32-2K words 8-word incr.
		Sync.	2	1-32 bits	32-2K words 8-word incr.
	High-density	Sync.	1	1-32 bits	32-2K words 1-word incr.
G/A		Async.	1	2-128 bits	2-1K words 2-word incr.
		Async.	2	2-128 bits	2-1K words 2-word incr.

Packaging and Test

EA-C9 gate arrays support automatic test generation through a scan-test methodology, which allows higher fault coverage, easier testing and quicker development time. NEC also offers optional BIST test structures for RAM testing.

NEC offers advanced packaging solutions including Tape Ball Grid Arrays (TBGA), Ball Grid Arrays (BGA), Plastic Ball Grid Arrays (PBGA), Plastic Quad Flat Packs (PQFP), Low Profile Plastic Quad Flat Packs (LQFP), Thin Plastic Quad Flat Packs (TQFP), and Pin Grid Arrays (PGA).

Please call your local NEC ASIC Design Center for a listing of available master/package combinations.

CAD Support

The EA-C9 family is fully supported by NEC's sophisticated OpenCAD® design framework, EA-C9 maximizes design quality and flexibility while minimizing ASIC design time.

NEC's OpenCAD system allows designers to combine the EDA industry's most popular third-party design tools with proprietary NEC tools, including those for advanced floorplanner, clock tree synthesis, automatic test pattern generation (ATPG), full-timing simulation, accelerated fault grading and advanced place and route algorithms. The latest OpenCAD system is open for sign-off using standard EDA tools. NEC offers RTL- and STA- (Static Timing Analysis) sign-off procedures to shorten the ASIC design cycle of high-complexity designs.

Support of High-Speed Systems. High-speed systems require tight control of clock skew on the chip and between devices on a printed circuit board. EA-C9 provides two features to control clock skew: the Digital PLL (DPLL) working at frequencies up to 100 MHz (with planned support for 160 MHz) for chip-to-chip skew minimization and Clock Tree Synthesis (CTS). CTS — supported by an NEC proprietary design tool — is used for clock skew management through the automatic insertion of a balanced buffer tree. The clock tree insertion method minimizes large-capacitive trunks and is especially useful with the hierarchical, synthesized design style being used for high-integration devices. RC values for actual net lengths of the clock tree are used for back annotation after place and route operations. A skew as low as ±100 ps can be achieved.

Accurate Design Verification. Nonlinear timing calculation is a very important requirement of the high-density, deep sub-micron ASIC designs. NEC makes use of the increased accuracy delivered by the nonlinear table look-up delay calculation methodology and offers consistent wire load models to ensure a high accuracy of the design verification.

Design Rule Check. A comprehensive design rule check (DRC) program reports design rule violations as well as chip utilization statistics for the design netlist. The generated report contains such information as net counts, total pin and gate counts, and utilization figures.

Layout. During design synthesis, wire load models are used to get delay estimations in a very early state of the design flow. In general, there's no need for customers to perform the floorplanning to meet the required timing. During layout, enhanced in-place optimization (IPO) features of the layout tools and engineering change order (ECO) capabilities of the synthesis tools are used to optimize critical timing paths defined by the given timing constraints. This feature can reduce the total design time.

Test Support

The EA-C9 family supports automatic test generation through a scan test methodology. It includes internal scan, boundary scan (JTAG) and built-in-self-test (BIST) architecture for easy and high-performance production RAM testing. This allows higher fault coverage, easier testing and faster development time.

Supplemental Publications

This data sheet contains preliminary specifications and operational data for the EA-C9 embedded array family. Additional information is available in NEC's EA-C9 Design Manual, Block Library, Memory Macro Design Manual and other related documents.

Please call your local NEC design center for additional information; see the back of this data sheet for locations and telephone numbers.

Absolute Maximum Ratings

Power supply voltage, V_{DD}	-0.5 to +4.6 V
Input Voltage, V_I	
3V Input buffer (at $V_I < V_{DD} + 0.5V$)	-0.5 to 4.6 V
3V Fail-safe input buffer (at $V_I < V_{DD} + 0.5V$)	-0.5 to 4.6 V
5V Input buffer (at $V_I < V_{DD} + 0.5V$)	-0.5 to 6.6 V
Output Voltage, V_O	
3V Output buffer (at $V_O < V_{DD} + 0.5V$)	-0.5 to 4.6 V
5V TTL Output buffer (at $V_O < V_{DD} + 3.0V$)	-0.5 to 6.6 V
5V CMOS Output buffer (at $V_O < V_{DD} + 3.0V$)	-0.5 to 6.6 V
Latch-up current, I_{LATCH}	>1 A (typ)
Operating temperature, T_{OPT}	-40 to +85°C
Storage temperature, T_{STG}	-65 to +150°C

Input/Output Capacitance

$V_{DD} = V_I = 0$ V; f = 1 MHz

Terminal		Symbol	Min	Typ	Max	Unit
Input	3V	C_{IN}	4.0		6.0	pF
	5V		8.0		10.0	
Output	3V	C_{OUT}	4.0		6.0	pF
	5V		8.0		10.0	
I/O	3V	$C_{I/O}$	4.0		6.0	pF
	5V		8.0		10.0	

(1) Values include package pin capacitance.

Power Consumption

Description	Limits	Unit
Internal gate	1.09	µW/MHz
Input buffer (FI01)	15.05	µW/MHz
Output buffer (FO01 @ 15 pF)	234	µW/MHz

Caution: Exposure to absolute maximum ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should not be operated outside the recommended operating conditions.

Recommended Operating Conditions

Parameter	Symbol	3.3V Interface Block		5V Interface Block		5V PCI Level		3.3V PCI Level		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
I/O Power supply voltage	V_{DD}	3.0	3.6	3.0	3.6	3.0	3.6	3.0	3.6	V
Junction temperature	T_J	-40	+125	-40	+125	-40	+125	-40	+125	°C
High-level input voltage	V_{IH}	2.0	V_{DD}	2.0	5.5	2.0	V_{CC}	$0.5V_{CC}$	V_{CC}	V
Low-level input voltage	V_{IL}	0	0.8	0	0.8	0	0.8	0	$0.3V_{CC}$	V
Positive trigger voltage	V_P	1.5	2.7	2.2	2.55	—	—	—	—	V
Negative trigger voltage	V_N	0.6	1.4	0.84	1.01	—	—	—	—	V
Hysteresis voltage	V_H	1.1	1.5	1.36	1.54	—	—	—	—	V
Input rise/fall time	t_R, t_F	0	200	0	200	0	200	0	200	ns
Input rise/fall time, Schmitt	t_R, t_F	0	10	0	10	—	—	—	—	ns

AC Characteristics

V_{DD} = 3.3V ± 0.3V; T_j = -40 to +125°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Toggle frequency (D-flip-flop)	f_{TOG}			670	MHz	F/O = 2, 5V
Delay time, 2-input NAND gate @ 5V						
Standard gate (F302)	t_{PD}		99		ps	F/O = 1; L = 0 mm
			150		ps	F/O = 2; L = 0.5 mm
Power gate (F322)	t_{PD}		84		ps	F/O = 1; L = 0 mm
			119		ps	F/O = 2; L = 0.5 mm
Delay time, buffer						
Input buffer (FI01)	t_{PD}		188		ps	F/O = 1; L = 0.5 mm
Input buffer (FI01)	t_{PD}		216		ps	F/O = 2; L = 0 mm
Output buffer (FO01)	t_{PD}		1.40		ns	C_L = 15 pF
Output rise time (FO01)	t_R		2.35		ns	C_L = 15 pF
Output fall time (FO01)	t_F		1.83		ns	C_L = 15 pF

DC Characteristics

V_{DD} = 3.3V ± 0.3V; T_j = -40 to +125°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Quiescent current (µPD654xx) (1)						
-19, -39	I_L		70	1400	µA	$V_I = V_{DD}$ or GND
-17, -37, -15, -35, -13, -33, -11, -31	I_L		40	800	µA	$V_I = V_{DD}$ or GND
-10, -30, -09, -29, -08, -28	I_L		20	400	µA	$V_I = V_{DD}$ or GND
-06, -26, -07, -27	I_L		10	200	µA	$V_I = V_{DD}$ or GND
Off-state output leakage current						
3V output buffer	I_{OZ}			±10	µA	$V_O = V_{DD}$ or GND
5V-protected TTL buffer	I_{OZ}			±10	µA	$V_O = V_{DD}$ or GND
Output short circuit current (3)	I_{OS}			-250	mA	V_O = GND
Input leakage current (2)						
Regular	I_I		$\pm 10^{-4}$	±10	µA	$V_I = V_{DD}$ or GND
50 kΩ pull-up	I_I	36	89	165	µA	V_I = GND
5 kΩ pull-up	I_I	284	654	1305	µA	V_I = GND
50 kΩ pull-down	I_I	28	79	141	µA	$V_I = V_{DD}$
Resistor values						
50 kΩ pull-up (4)	R_{pu}	21.8	37.1	83.1	kΩ	
5 kΩ pull-up	R_{pu}	2.8	5.0	10.6	kΩ	
50 kΩ pull-down	R_{pu}	25.6	41.9	105.8	kΩ	
Low-level output current (5V Interface Block)						
1 mA	I_{OL}	1		TBD	mA	V_{OL} = 0.4 V
2 mA	I_{OL}	2		TBD	mA	V_{OL} = 0.4 V
3 mA	I_{OL}	3		TBD	mA	V_{OL} = 0.4 V
6 mA	I_{OL}	6		TBD	mA	V_{OL} = 0.4 V
9 mA	I_{OL}	9		TBD	mA	V_{OL} = 0.4 V
12 mA	I_{OL}	12		TBD	mA	V_{OL} = 0.4 V
High-level output current (5V Interface Block)						
1 mA	I_{OH}	-1			mA	V_{OH} = 2.4 V
2 mA	I_{OH}	-1			mA	V_{OH} = 2.4 V
3 mA	I_{OH}	-3			mA	V_{OH} = 2.4 V
6 mA	I_{OH}	-3			mA	V_{OH} = 2.4 V
9 mA	I_{OH}	-3			mA	V_{OH} = 2.4 V
12 mA	I_{OH}	-3			mA	V_{OH} = 2.4 V
Low-level output current (3.3V Interface Block)						
3 mA (FO09)	I_{OL}	3		10	mA	V_{OL} = 0.4 V
6 mA (FO04)	I_{OL}	6		20	mA	V_{OL} = 0.4 V
9 mA (FO01)	I_{OL}	9		30	mA	V_{OL} = 0.4 V
12 mA (FO02)	I_{OL}	12		40	mA	V_{OL} = 0.4 V
18 mA (FO03)	I_{OL}	18		60	mA	V_{OL} = 0.4 V
24 mA (FO06)	I_{OL}	24		75	mA	V_{OL} = 0.4 V
High-level output current (3.3V Interface Block)						
3 mA (FO09)	I_{OH}	-3			mA	V_{OH} = 2.4 V
6 mA (FO04)	I_{OH}	-6			mA	V_{OH} = 2.4 V
9 mA (FO01)	I_{OH}	-9			mA	V_{OH} = 2.4 V
12 mA (FO02)	I_{OH}	-12			mA	V_{OH} = 2.4 V
18 mA (FO03)	I_{OH}	-18			mA	V_{OH} = 2.4 V
24 mA (FO06)	I_{OH}	-24			mA	V_{OH} = 2.4 V
Low-level output voltage	V_{OL}			0.1	V	I_{OL} = 0 mA
High-level output voltage	V_{OH}	V_{DD}-0.1			V	I_{OH} = 0 mA

Notes:

(1) Static current consumption increases if an I/O block with on-chip pull-up/pull-down resistor or an oscillator is used. Contact an NEC ASIC Design Center for assistance in calculation.

(2) Leakage current is limited by tester capabilities. Specification listed represents this measurement limitation. Actual values will be significantly lower.

(3) Rating is for only one output operating in this mode for less than 1 second.

(4) Resistor is called 50kΩ for backwards compatibility.

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