NEC

MOS INTEGRATED CIRCUIT
μPD442000A-X

2M-BIT CMOS STATIC RAM
256K-WORD BY 8-BIT
EXTENDED TEMPERATURE OPERATION

Description

The μPD442000A-X is a high speed, low power, 2,097,152 bits (262,144 words by 8 bits) CMOS static RAM.

The μPD442000A-X has two chip enable pins (/CE1, CE2) to extend the capacity. And battery backup is available.

★ The μPD442000A-X is packed in 32-pin PLASTIC TSOP (I) (Normal bent) and 32-pin PLASTIC TSOP (I) (Reverse bent).

Features

- 262,144 words by 8 bits organization
- Fast access time : 55, 70, 85, 100, 120 ns (MAX.)
- Low voltage operation : V_{CC} = 2.7 to 3.6 V (-BB55X, -BB70X, -BB85X)
  V_{CC} = 2.2 to 3.6 V (-BC70X, -BC85X, -BC10X)
  V_{CC} = 1.8 to 2.2 V (-DD85X, -DD10X, -DD12X)
- Low V_{CC} data retention : 1.0 V (MIN.)
- Operating ambient temperature : T_A = –25 to +85 °C
- Output Enable input for easy application
- Two Chip Enable inputs : /CE1, CE2

μPD442000A	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Supply current		
				At operating mA (MAX.)	At standby μA (MAX.)	At data retention μA (MAX.)
-BB55X, -BB70X, -BB85X	55, 70, 85	2.7 to 3.6	–25 to +85	30 Note	2	1
-BC70X, -BC85X, -BC10X	70, 85, 100	2.2 to 3.6		30		
-DD85X, -DD10X, -DD12X	85, 100, 120	1.8 to 2.2		15	1.5	

Note Cycle time ≥ 70 ns, -BB55X : 35 mA

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The mark ★ shows major revised points.

Ordering Information

	Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C
	μPD442000AGU-BB55X-9JH	32-pin PLASTIC TSOP (I) (8×13.4) (Normal bent)	55	2.7 to 3.6	−25 to +85
	μPD442000AGU-BB70X-9JH		70		
	μPD442000AGU-BB85X-9JH		85		
	μPD442000AGU-BC70X-9JH		70	2.2 to 3.6	
	μPD442000AGU-BC85X-9JH		85		
	μPD442000AGU-BC10X-9JH		100		
	μPD442000AGU-DD85X-9JH		85	1.8 to 2.2	
	μPD442000AGU-DD10X-9JH		100		
	μPD442000AGU-DD12X-9JH		120		
★	μPD442000AGU-BB55X-9KH	32-pin PLASTIC TSOP (I) (8×13.4) (Reverse bent)	55	2.7 to 3.6	
★	μPD442000AGU-BB70X-9KH		70		
★	μPD442000AGU-BB85X-9KH		85		
★	μPD442000AGU-BC70X-9KH		70	2.2 to 3.6	
★	μPD442000AGU-BC85X-9KH		85		
★	μPD442000AGU-BC10X-9KH		100		
★	μPD442000AGU-DD85X-9KH		85	1.8 to 2.2	
★	μPD442000AGU-DD10X-9KH		100		
★	μPD442000AGU-DD12X-9KH		120		

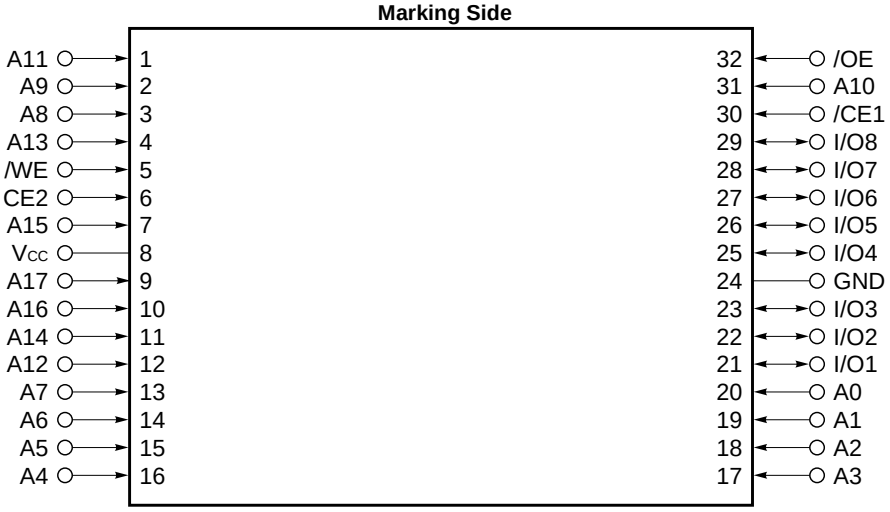
Pin Configurations

/xxx indicates active low signal.

32-pin PLASTIC TSOP (I) (8×13.4) (Normal bent)

[μPD442000AGU-9JH]

Marking Side



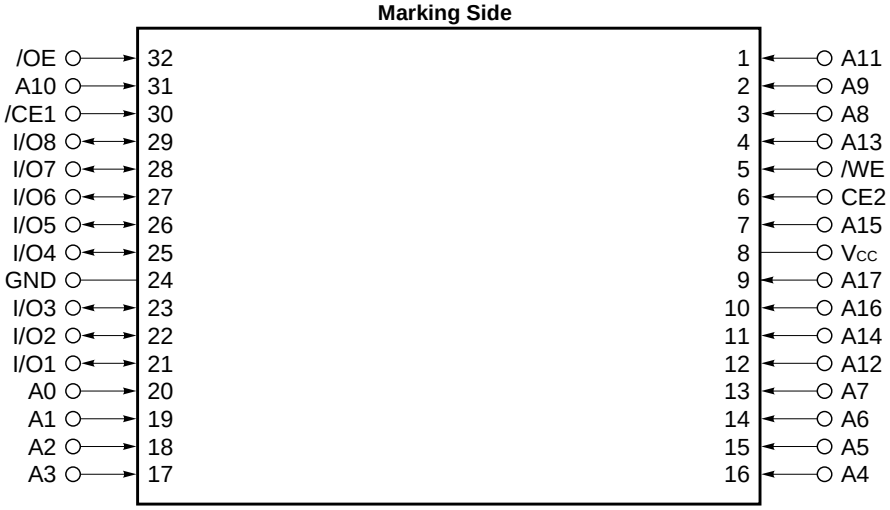
A0 to A17	:	Address inputs
I/O1 to I/O8	:	Data inputs / outputs
/CE1, CE2	:	Chip Enable 1, 2
/WE	:	Write Enable
/OE	:	Output Enable
VCC	:	Power supply
GND	:	Ground

Remark Refer to **Package Drawings** for the 1-pin index mark.

★ **32-pin PLASTIC TSOP (I) (8×13.4) (Reverse bent)**

[μPD442000AGU-9KH]

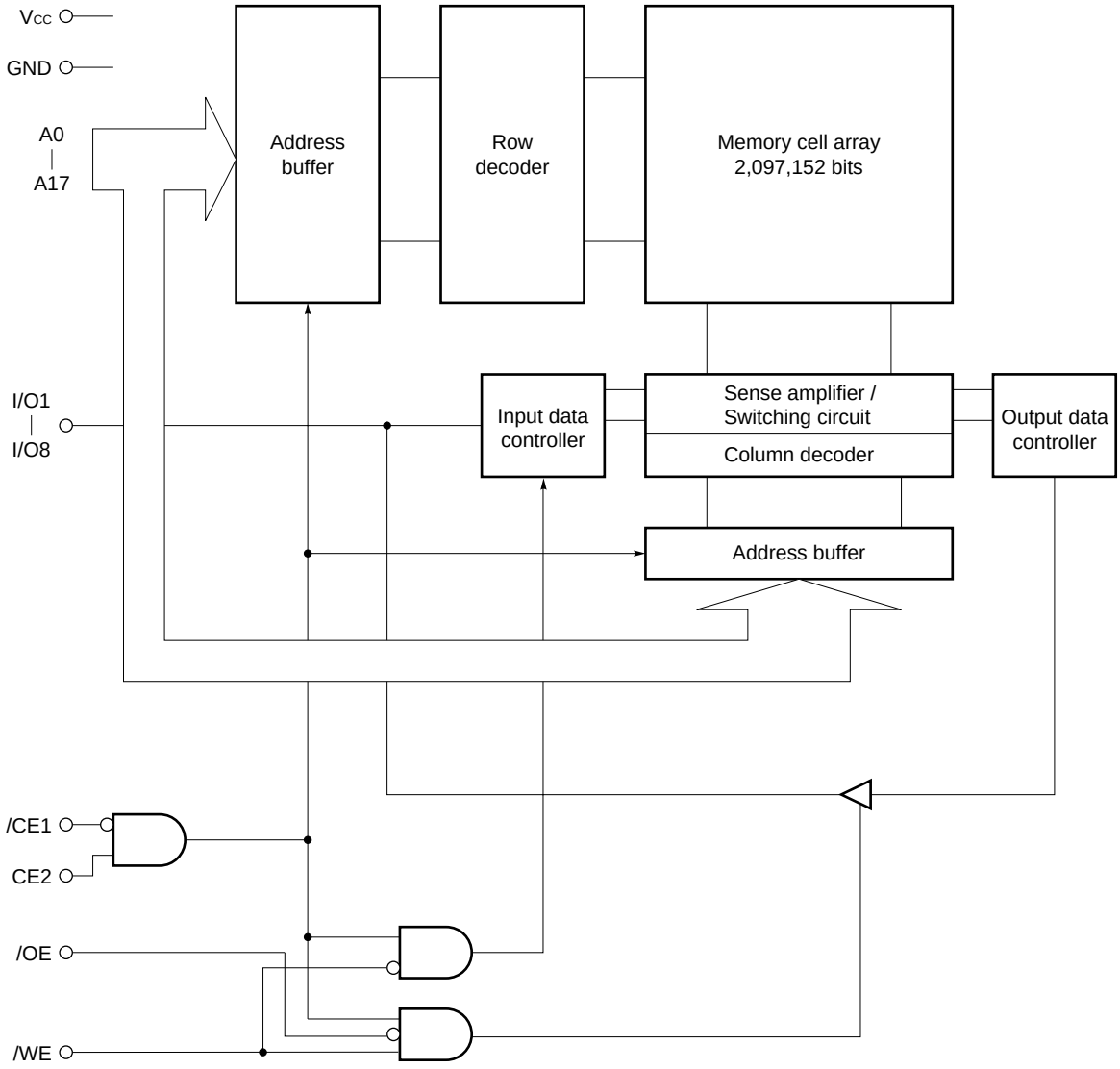
Marking Side



A0 to A17	:	Address inputs
I/O1 to I/O8	:	Data inputs / outputs
/CE1, CE2	:	Chip Enable 1, 2
/WE	:	Write Enable
/OE	:	Output Enable
V_{CC}	:	Power supply
GND	:	Ground

Remark Refer to **Package Drawings** for the 1-pin index mark.

Block Diagram



Truth Table

/CE1	CE2	/OE	/WE	Mode	I/O	Supply current
H	×	×	×	Not selected	High-Z	I_{SB}
×	L	×	×	Not selected	High-Z	
L	H	H	H	Output disable	High-Z	I_{CCA}
L	H	L	H	Read	D_{OUT}	
L	H	×	L	Write	D_{IN}	

Remark × : V_{IH} or V_{IL}

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			-BB55X, -BB70X, -BB85X -BC70X, -BC85X, -BC10X	-DD85X, -DD10X, -DD12X	
Supply voltage	V_{CC}		–0.5 Note to +4.0	–0.5 Note to +2.7	V
Input / Output voltage	V_T		–0.5 Note to V_{CC}+0.4 (4.0 V MAX.)	–0.5 Note to V_{CC}+0.4 (2.7 V MAX.)	V
Operating ambient temperature	T_A		–25 to +85	–25 to +85	°C
Storage temperature	T_{stg}		–55 to +125	–55 to +125	°C

Note –3.0 V (MIN.) (Pulse width : 30 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	-BB55X,-BB70X,-BB85X		-BC70X,-BC85X,-BC10X		-DD85X,-DD10X,-DD12X		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Supply voltage	V_{CC}		2.7	3.6	2.2	3.6	1.8	2.2	V
High level input voltage	V_{IH}	2.7 V ≤ V_{CC} ≤ 3.6 V	2.4	V_{CC}+0.4	2.4	V_{CC}+0.4	–	–	V
		2.2 V ≤ V_{CC} < 2.7 V	–	–	2.0	V_{CC}+0.3	–	–	
		1.8 V ≤ V_{CC} < 2.2 V	–	–	–	–	1.6	V_{CC}+0.2	
Low level input voltage	V_{IL}		–0.3 Note	+0.5	–0.3 Note	+0.4	–0.2 Note	+0.2	V
Operating ambient temperature	T_A		–25	+85	–25	+85	–25	+85	°C

Note –1.0 V (MIN.) (Pulse width : 20 ns)

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			8	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

2. These parameters are not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (1/2)

Parameter	Symbol	Test condition		-BB55X, -BB70X, -BB85X			Unit
				MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /CE1 = V_{IH} or CE2 = V_{IL} or /WE = V_{IL} or /OE = V_{IH}		–1.0		+1.0	μA
Operating supply current	I_{CCA1}	/CE1 = V_{IL}, CE2 = V_{IH}, Minimum cycle time, $I_{I/O}$ = 0 mA	Cycle time = 55 ns		–	35	mA
			Cycle time ≥ 70 ns		–	30	
	I_{CCA2}	/CE1 = V_{IL}, CE2 = V_{IH}, Cycle time = ∞, $I_{I/O}$ = 0 mA			–	4	
	I_{CCA3}	/CE1 ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V, Cycle time = 1 μs, $I_{I/O}$ = 0 mA, V_{IL} ≤ 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V			–	4	
Standby supply current	I_{SB}	/CE1 = V_{IH} or CE2 = V_{IL}			–	0.35	mA
	I_{SB1}	/CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V			0.1	2	μA
	I_{SB2}	CE2 ≤ 0.2 V			0.1	2	
High level output voltage	V_{OH}	I_{OH} = –0.5 mA		2.4			V
Low level output voltage	V_{OL}	I_{OL} = 1.0 mA				0.4	V

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

2. These DC characteristics are in common regardless of product classification.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (2/2)

Parameter	Symbol	Test condition		-BC70X, -BC85X, -BC10X			-DD85X, -DD10X, -DD12X			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		–1.0		+1.0	–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /CE1 = V_{IH} or		–1.0		+1.0	–1.0		+1.0	μA
		CE2 = V_{IL} or /WE = V_{IL} or /OE = V_{IH}								
Operating supply current	I_{CCA1}	/CE1 = V_{IL}, CE2 = V_{IH},			–	30		–	–	mA
		Minimum cycle time,	V_{CC} ≤ 2.7 V		–	25		–	–	
		$I_{I/O}$ = 0 mA	V_{CC} ≤ 2.2 V		–	–		–	15	
	I_{CCA2}	/CE1 = V_{IL}, CE2 = V_{IH},			–	4		–	–	
		Cycle time = ∞,	V_{CC} ≤ 2.7 V		–	2		–	–	
		$I_{I/O}$ = 0 mA	V_{CC} ≤ 2.2 V		–	–		–	1	
	I_{CCA3}	/CE1 ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V,			–	4		–	–	
		Cycle time = 1 μs, $I_{I/O}$ = 0 mA,								
		V_{IL} ≤ 0.2 V,	V_{CC} ≤ 2.7 V		–	3		–	–	
		V_{IH} ≥ V_{CC} – 0.2 V	V_{CC} ≤ 2.2 V		–	–		–	3	
Standby supply current	I_{SB}	/CE1 = V_{IH} or CE2 = V_{IL}			–	0.35		–	–	mA
			V_{CC} ≤ 2.7 V		–	0.35		–	–	
			V_{CC} ≤ 2.2 V		–	–		–	0.35	
	I_{SB1}	/CE1 ≥ V_{CC} – 0.2 V,			0.1	2		–	–	μA
		CE2 ≥ V_{CC} – 0.2 V	V_{CC} ≤ 2.7 V		0.08	2		–	–	
			V_{CC} ≤ 2.2 V		–	–		0.05	1.5	
	I_{SB2}	CE2 ≤ 0.2 V			0.1	2		–	–	
			V_{CC} ≤ 2.7 V		0.08	2		–	–	
			V_{CC} ≤ 2.2 V		–	–		0.05	1.5	
High level output voltage	V_{OH}	I_{OH} = –0.5 mA		2.4			–			V
			V_{CC} ≤ 2.7 V	1.8			–			
			V_{CC} ≤ 2.2 V	–			1.5			
Low level output voltage	V_{OL}	I_{OL} = 1.0 mA				0.4			–	V
			V_{CC} ≤ 2.7 V			0.4			–	
			V_{CC} ≤ 2.2 V			–			0.4	

Remarks 1. V_{IN} : Input voltage

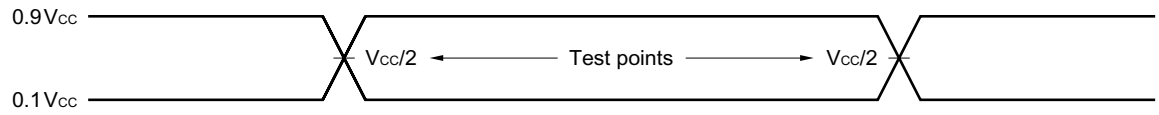
$V_{I/O}$: Input / Output voltage

2. These DC characteristics are in common regardless of product classification.

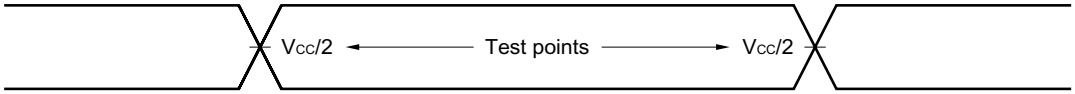
AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

AC Test Conditions

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

[-BB55X, -BB70X, -BB85X]

1TTL + 50 pF

[-BC70X, -BC85X, -BC10X, -DD85X, -DD10X, -DD12X]

1TTL + 30 pF

Read Cycle (1/3)

Parameter	Symbol	$V_{CC} \geq 2.7$ V						Unit	Condition
		-BB55X		-BB70X		-BB85X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	55		70		85		ns	
Address access time	t_{AA}		55		70		85	ns	**Note 1**
/CE1 access time	t_{CO1}		55		70		85	ns	
CE2 access time	t_{CO2}		55		70		85	ns	
/OE to output valid	t_{OE}		30		35		40	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
/CE1 to output in Low-Z	t_{LZ1}	10		10		10		ns	**Note 2**
CE2 to output in Low-Z	t_{LZ2}	10		10		10		ns	
/OE to output in Low-Z	t_{OLZ}	5		5		5		ns	
/CE1 to output in High-Z	t_{HZ1}		20		25		30	ns	
CE2 to output in High-Z	t_{HZ2}		20		25		30	ns	
/OE to output in High-Z	t_{OHZ}		20		25		30	ns	

Notes 1. The output load is 1TTL + 50 pF.

2. The output load is 1TTL + 5 pF.

Read Cycle (2/3)

Parameter	Symbol	$V_{CC} \geq 2.2$ V						Unit	Condition
		-BC70X		-BC85X		-BC10X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	70		85		100		ns	
Address access time	t_{AA}		70		85		100	ns	**Note 1**
/CE1 access time	t_{CO1}		70		85		100	ns	
CE2 access time	t_{CO2}		70		85		100	ns	
/OE to output valid	t_{OE}		35		40		50	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
/CE1 to output in Low-Z	t_{LZ1}	10		10		10		ns	**Note 2**
CE2 to output in Low-Z	t_{LZ2}	10		10		10		ns	
/OE to output in Low-Z	t_{OLZ}	5		5		5		ns	
/CE1 to output in High-Z	t_{HZ1}		25		30		35	ns	
CE2 to output in High-Z	t_{HZ2}		25		30		35	ns	
/OE to output in High-Z	t_{OHZ}		25		30		35	ns	

Notes 1. The output load is 1TTL + 30 pF.

2. The output load is 1TTL + 5 pF.

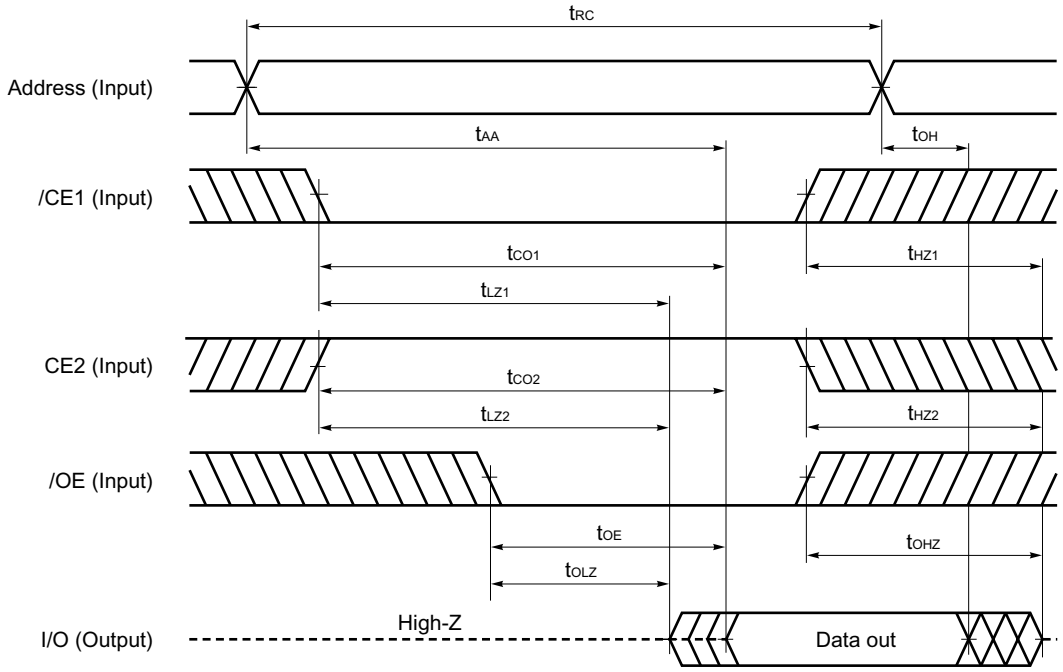
Read Cycle (3/3)

Parameter	Symbol	$V_{CC} \geq 1.8$ V						Unit	Condition
		-DD85X		-DD10X		-DD12X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	85		100		120		ns	
Address access time	t_{AA}		85		100		120	ns	**Note 1**
/CE1 access time	t_{CO1}		85		100		120	ns	
CE2 access time	t_{CO2}		85		100		120	ns	
/OE to output valid	t_{OE}		40		50		60	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
/CE1 to output in Low-Z	t_{LZ1}	10		10		10		ns	**Note 2**
CE2 to output in Low-Z	t_{LZ2}	10		10		10		ns	
/OE to output in Low-Z	t_{OLZ}	5		5		5		ns	
/CE1 to output in High-Z	t_{HZ1}		30		35		40	ns	
CE2 to output in High-Z	t_{HZ2}		30		35		40	ns	
/OE to output in High-Z	t_{OHZ}		30		35		40	ns	

Notes 1. The output load is 1TTL + 30 pF.

2. The output load is 1TTL + 5 pF.

Read Cycle Timing Chart



Remark In read cycle, /WE should be fixed to high level.

Write Cycle (1/3)

Parameter	Symbol	$V_{CC} \geq 2.7$ V						Unit	Condition
		-BB55X		-BB70X		-BB85X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	55		70		85		ns	
/CE1 to end of write	t_{CW1}	50		55		70		ns	
CE2 to end of write	t_{CW2}	50		55		70		ns	
Address valid to end of write	t_{AW}	50		55		70		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	45		50		55		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	25		30		35		ns	
Data hold time	t_{DH}	0		0		0		ns	
/WE to output in High-Z	t_{WHZ}		20		25		30	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		ns	

Note The output load is 1TTL + 5 pF.

Write Cycle (2/3)

Parameter	Symbol	$V_{CC} \geq 2.2$ V						Unit	Condition
		-BC70X		-BC85X		-BC10X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	70		85		100		ns	
/CE1 to end of write	t_{CW1}	55		70		80		ns	
CE2 to end of write	t_{CW2}	55		70		80		ns	
Address valid to end of write	t_{AW}	55		70		80		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	50		55		60		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	30		35		40		ns	
Data hold time	t_{DH}	0		0		0		ns	
/WE to output in High-Z	t_{WHZ}		25		30		35	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		ns	

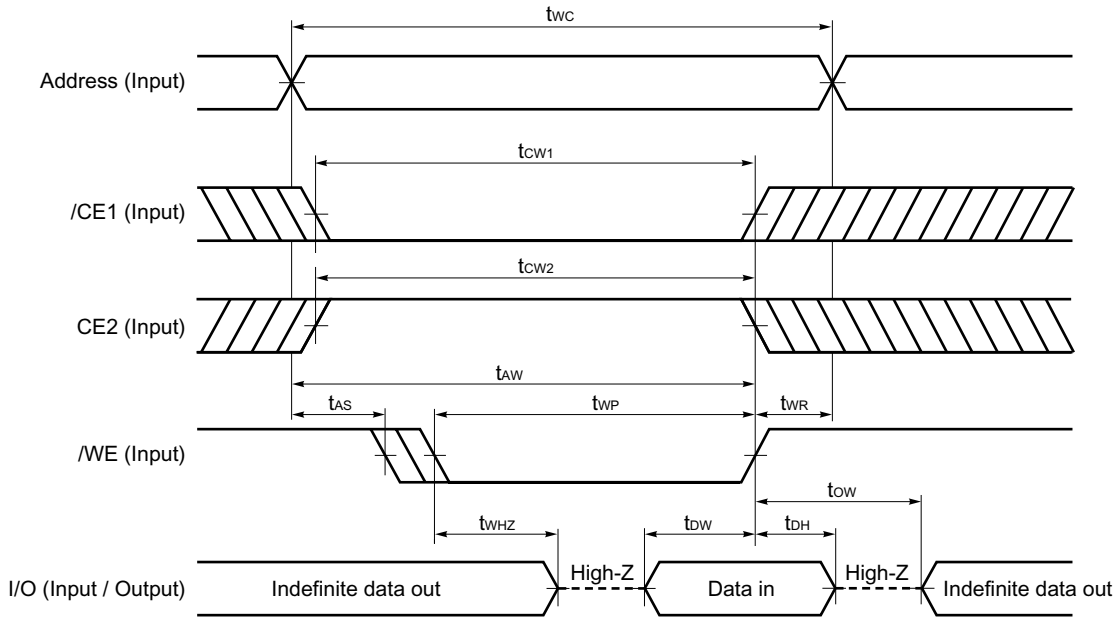
Note The output load is 1TTL + 5 pF.

Write Cycle (3/3)

Parameter	Symbol	$V_{CC} \geq 1.8$ V						Unit	Condition
		-DD85X		-DD10X		-DD12X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	85		100		120		ns	
/CE1 to end of write	t_{CW1}	70		80		100		ns	
CE2 to end of write	t_{CW2}	70		80		100		ns	
Address valid to end of write	t_{AW}	70		80		100		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	55		60		85		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	35		40		60		ns	
Data hold time	t_{DH}	0		0		0		ns	
/WE to output in High-Z	t_{WHZ}		30		35		40	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		ns	

Note The output load is 1TTL + 5 pF.

Write Cycle Timing Chart 1 (/WE Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

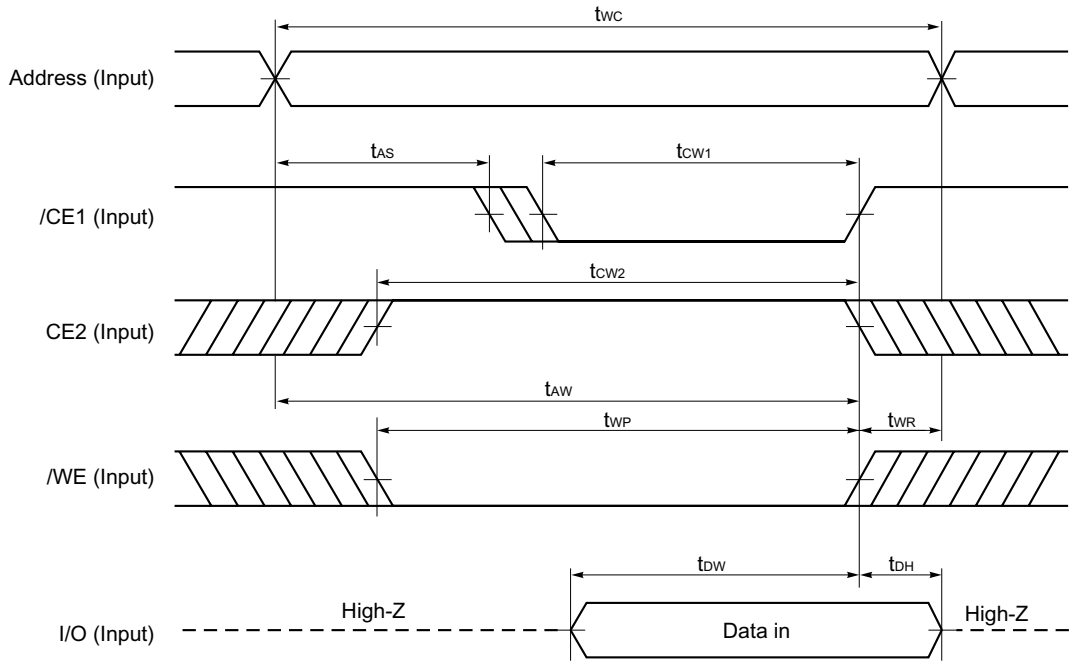
2. Do not input data to the I/O pins while they are in the output state.

Remarks 1. Write operation is done during the overlap time of a low level /CE1, /WE, and a high level CE2.

2. If /CE1 changes to low level at the same time or after the change of /WE to low level, or if CE2 changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.

3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

Write Cycle Timing Chart 2 (/CE1 Controlled)

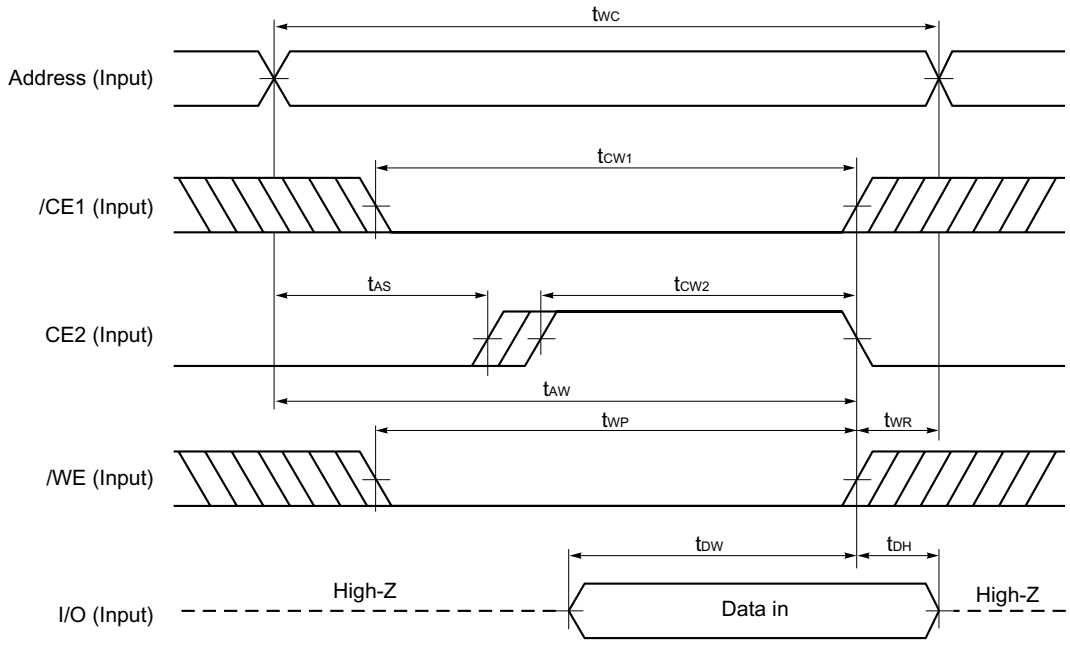


Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, and a high level CE2.

Write Cycle Timing Chart 3 (CE2 Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, and a high level CE2.

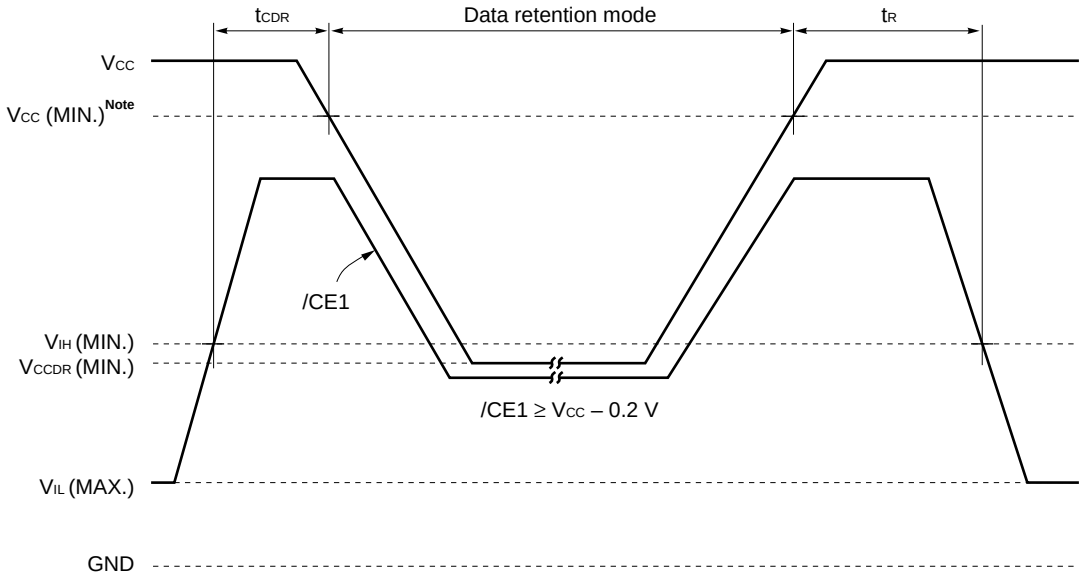
Low V_{CC} Data Retention Characteristics (T_A = –25 to +85 °C)

Parameter	Symbol	Test Condition	-BB55X, -BB70X, -BB85X			-BC70X, -BC85X, -BC10X			-DD85X, -DD10X, -DD12X			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Data retention supply voltage	V_{CCDR1}	/CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V	1.0		3.6	1.0		3.6	1.0		2.2	V
	V_{CCDR2}	CE2 ≤ 0.2 V	1.0		3.6	1.0		3.6	1.0		2.2	
Data retention supply current	I_{CCDR1}	V_{CC} = 1.2 V, /CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V		0.05	1		0.05	1		0.05	1	μA
	I_{CCDR2}	V_{CC} = 1.2 V, CE2 ≤ 0.2 V		0.05	1		0.05	1		0.05	1	
Chip deselection to data retention mode	t_{CDR}		0			0			0			ns
Operation recovery time	t_R		t_{RC} Note			t_{RC} Note			t_{RC} Note			ns

Note t_{RC} : Read cycle time

Data Retention Timing Chart

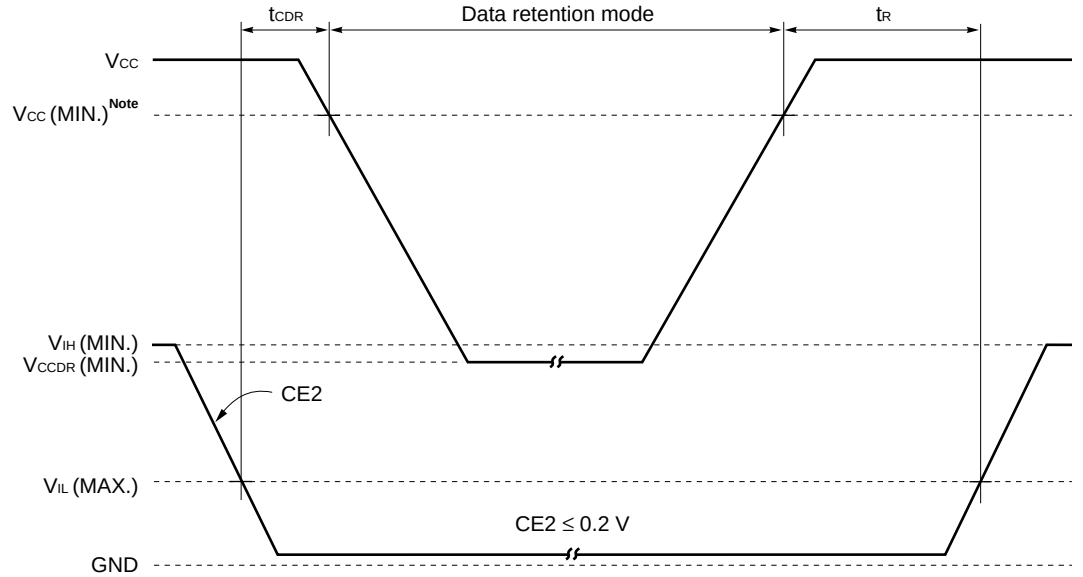
(1) /CE1 Controlled



Note 2.7 V (-BB55X, -BB70X, -BB85X), 2.2 V (-BC70X, -BC85X, -BC10X), 1.8 V (-DD85X, -DD10X, -DD12X)

Remark On the data retention mode by controlling /CE1, the input level of CE2 must be ≥ V_{CC} – 0.2 V or ≤ 0.2 V. The other pins (Address, I/O, /WE, /OE) can be in high impedance state.

(2) CE2 Controlled

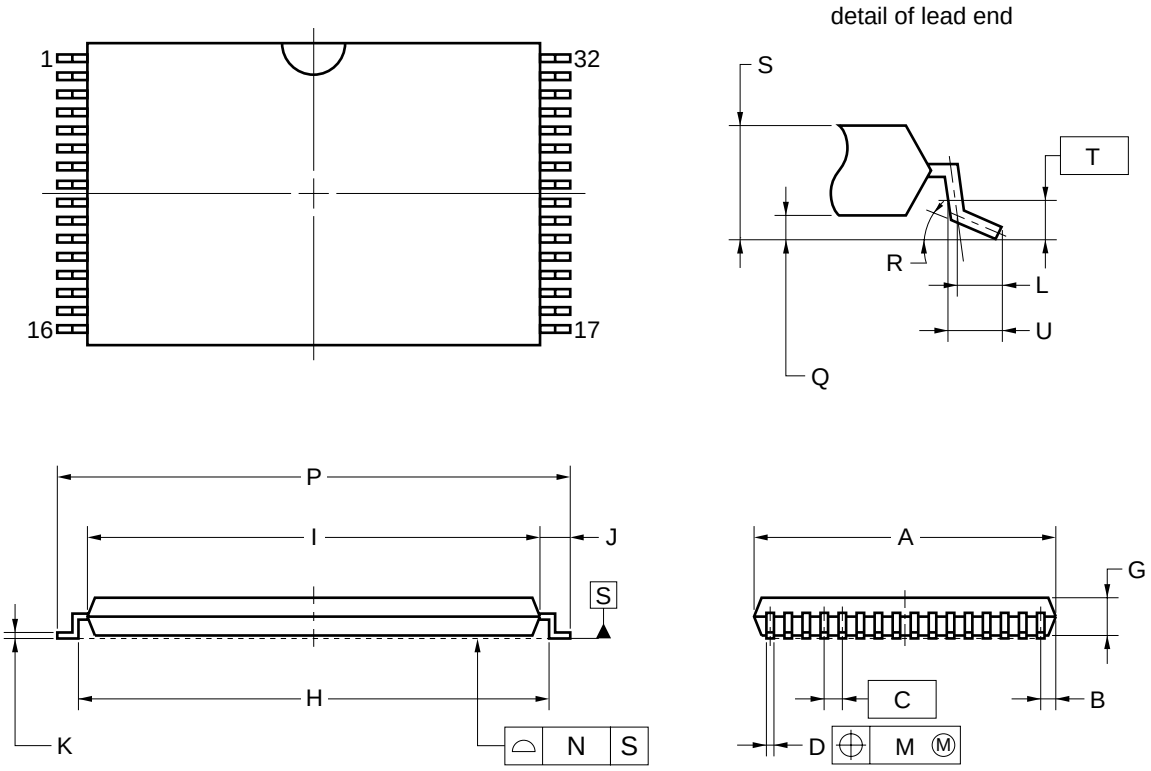


Note 2.7 V (-BB55X, -BB70X, -BB85X), 2.2 V (-BC70X, -BC85X, -BC10X), 1.8 V (-DD85X, -DD10X, -DD12X)

Remark On the data retention mode by controlling CE2, the other pins (/CE1, Address, I/O, /WE, /OE) can be in high impedance state.

Package Drawings

32-PIN PLASTIC TSOP(I) (8x13.4)



NOTES

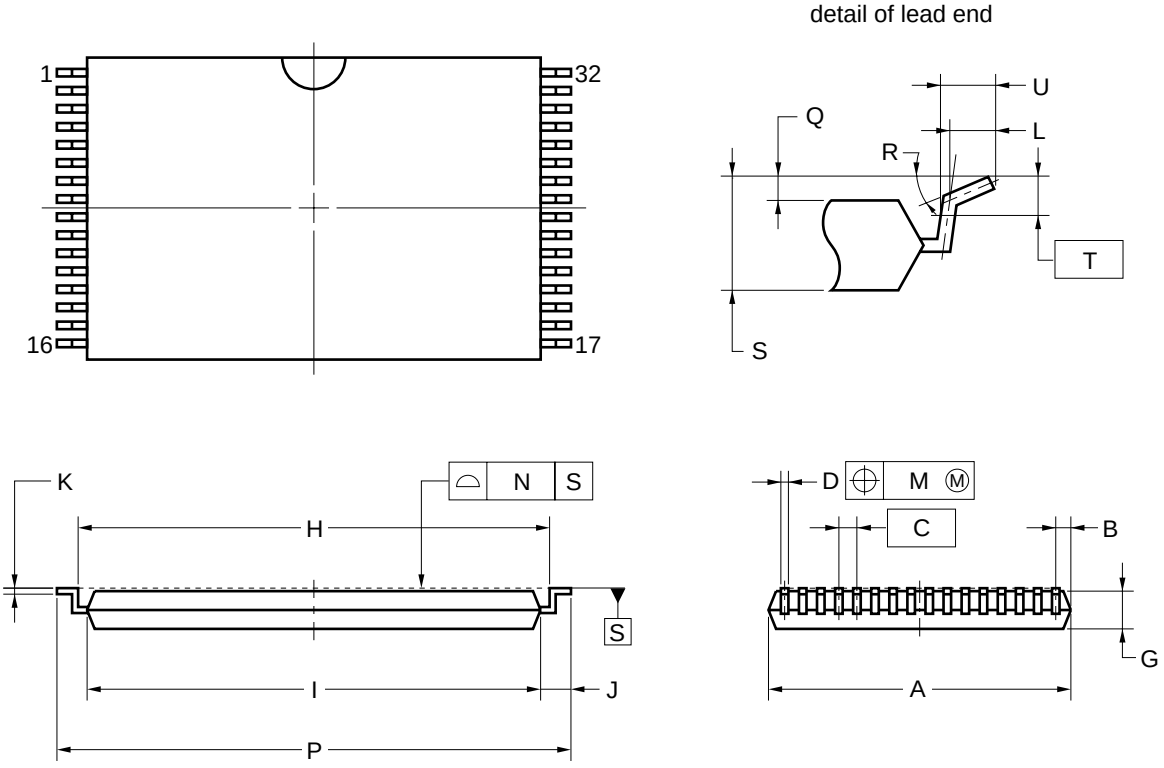
1. Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

ITEM	MILLIMETERS
A	8.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
G	1.0±0.05
H	12.4±0.2
I	11.8±0.1
J	0.8±0.2
K	$0.145^{+0.025}_{-0.015}$
L	0.5
M	0.08
N	0.08
P	13.4±0.2
Q	0.1±0.05
R	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
S	1.2 MAX.
T	0.25
U	0.6±0.15

P32GU-50-9JH-2

★ 32-PIN PLASTIC TSOP(I) (8x13.4)



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P32GU-50-9KH-2

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD442000A-X.

Types of Surface Mount Device

μPD442000AGU-9JH : 32-pin PLASTIC TSOP (I) (8×13.4) (Normal bent)

★ μPD442000AGU-9KH : 32-pin PLASTIC TSOP (I) (8×13.4) (Reverse bent)

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
6th edition/ Jul. 2002	pp.6, 7	pp.6, 7	Modification	DC Characteristics	-BB55X,-BB70X,-BB85X(MAX.) : I_{SB} = 0.6mA → 0.35mA
					-BC70X,-BC85X,-BC10X(MAX.) : I_{SB} = 0.6mA → 0.35mA
					-BC70X,-BC85X,-BC10X(MAX.) : I_{SB}(V_{CC} ≥ 2.7 V) = 0.6mA → 0.35mA
					-DD85X,-DD10X,-DD12X(MAX.) : I_{SB} = 0.6mA → 0.35mA
	p.8	p.8	Modification	AC Characteristics	Integration of Input Waveform and Output Waveform
7th edition/ Oct. 2002	pp.2, 4, 21-22	pp.2, 3, 19-20	Addition	Ordering Information, Pin Configurations, Package Drawings, Recommended Soldering Conditions	32-pin PLASTIC TSOP (I) (8×13.4) (Reverse bent) μPD442000AGU-***-9KH *** : Speed grades BB55X, BB70X, BB85X, BC70X, BC85X, BC10X, DD85X, DD10X, DD12X

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

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