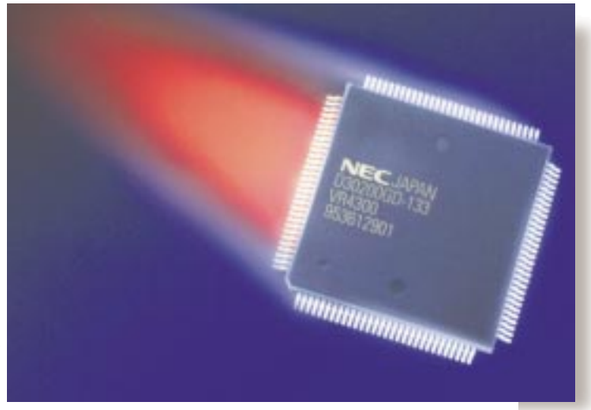
V_R4300™ 64-BIT MIPS® RISC MICROPROCESSOR

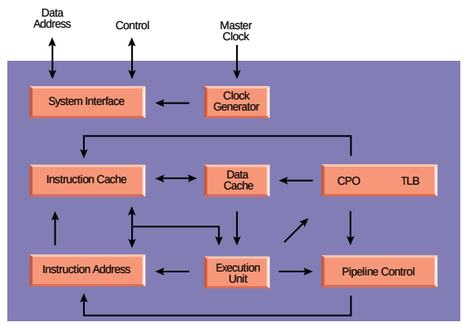
For Windows® CE Applications

Designed around the popular MIPS architecture, the V_R4300 offers one of the best MIPS performance/die size solutions on the market. Its internal operating frequency is either 100 MHz or 133 MHz at 3.3V. The V_R4300 CPU has an optimized five-stage pipeline, 16K instruction cache, 8K data cache, memory management unit, floating-point arithmetic unit (FPU) and clock generator. The V_R4300 is one of the most powerful processors available to support Windows CE, making it ideal for many performance-intensive tethered applications.



SALIENT FEATURES

- 64-bit MIPS RISC architecture
- 133 or 100 MHz operation
- Conformance to MIPS I/II/III instruction set architectures
- Five-stage pipeline processing
- High-speed execution of integer and floating-point operations
- Performance levels of 80/60 SPECint92 (133MHz) and 60/45 SPECfp92 (100MHz)
- Same input clock as system bus frequency
- 16K instruction cache and 8K data cache
- Multiplexed 32-bit address/data bus
- Low power dissipation: 1.8 W typical and 2.2 W maximum
- Supply voltage of 3.3 volts
- 120-pin plastic QFP packaging



FEATURE DESCRIPTION

Execution Unit
- 64-bit register file
- 64-bit integer/mantissa data bus
- 12-bit exponent data bus

Co-Processor
- Exception processing unit with system control co-processor registers
- Memory management unit that converts virtual addresses into physical addresses and verifies memory access of kernel, supervisor and user memory segments
- Seven page sizes: 4K, 16K, 64K, 256K, 1M, 4M and 16M (VSIZE=40 and PSIZE=32)
- Translation lookaside buffer with 32 entries, each mapped to an even or odd frame buffer page

Cache Memory Unit
- 16K direct-mapped instruction cache and 8K data cache
- Write-back cache for reducing store operations

Pipeline Control
- Occurrence of cache misses
- Flash buffer full
- Multicycle instructions
- Occurrence of system exceptions

Floating-Point Arithmetic Unit
- Integrated into CPU's integer arithmetic unit
- 32-bit (single-precision) and 64-bit (double-precision) IEEE 754 floating-point arithmetic support

Clock Generator
- Four clocks generated from MasterClock input
- Phase-locked loop (PLL) to suppress skew between the input clock and internal clock

High Performance
- 60 SPECint92, 45 SPECfp92, 131 MIPS (100MHz)
- 80 SPECint92, 60 SPECfp92, 173 MIPS (133MHz)

Low Power Consumption
- 1.8W typical @ 100MHz, 3.3V
- 2.4W typical @ 133MHz, 3.3V

ORDERING INFORMATION

PART NUMBER	PACKAGE
µPD30200GD-100-MBB	120-pin QFP (28mmx28mm) 100 MHz
µPD30200GD-133-MBB	120-pin QFP (28mmx28mm) 133 MHz