National Semiconductor

CLC005 ITU-T G.703 Cable Driver with Adjustable Outputs

General Description

National's Comlinear CLC005 is a monolithic, high-speed cable driver designed for the ITU-T G.703 serial digital data transmission standard. The CLC005 drives 75 Ω transmission lines (Belden 8281 or equivalent) at data rates from DC to over 622 Mbps. Output signal waveforms produced by the CLC005 comply with G.703 specifications. Controlled output rise and fall times (650 ps typical) minimize transition-induced jitter. The output voltage swing, typically 2.0V, set by an accurate, low-drift internal bandgap reference, delivers a 1.0V swing to back-matched and terminated 75 Ω cable. Output swing is adjustable from 0.7 V_{p-p} to 2.2 V_{p-p} using external resistors.

The CLC005's class AB output stage consumes less power than other designs, 185 mW with both outputs terminated, and requires no external bias resistors. The differential inputs accept a wide range of digital signals from 200 mV_{p-p} to G.703 levels within the specified common-mode limits. All this make the CLC005 an excellent general purpose high speed driver for digital applications.

The CLC005 is powered from a single +5V or -5.2V supply and comes in an 8-pin SOIC package.

Key Specifications

- 650 ps rise and fall times
- Data rates to 622 Mbps
- 200 mV differential input
- Low residual jitter (25 ps_{pp})

Features

- No external pull-down resistors
- Adjustable output amplitude
- Differential input and output
- Low power dissipation
- Single +5V or -5.2V supply

Applications

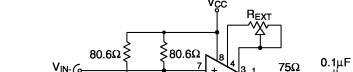
- ITU-T G.703, Sonet/SDH, and ATM compatible driver
- Digital routers and distribution amplifiers

75Ω Coax

75Ω Coax

- Coaxial cable driver for digital transmission line
- Twisted pair driver
- Buffer applications





133Ω

CLC005

75Ω

0.1μF



August 1998

133Ω≶

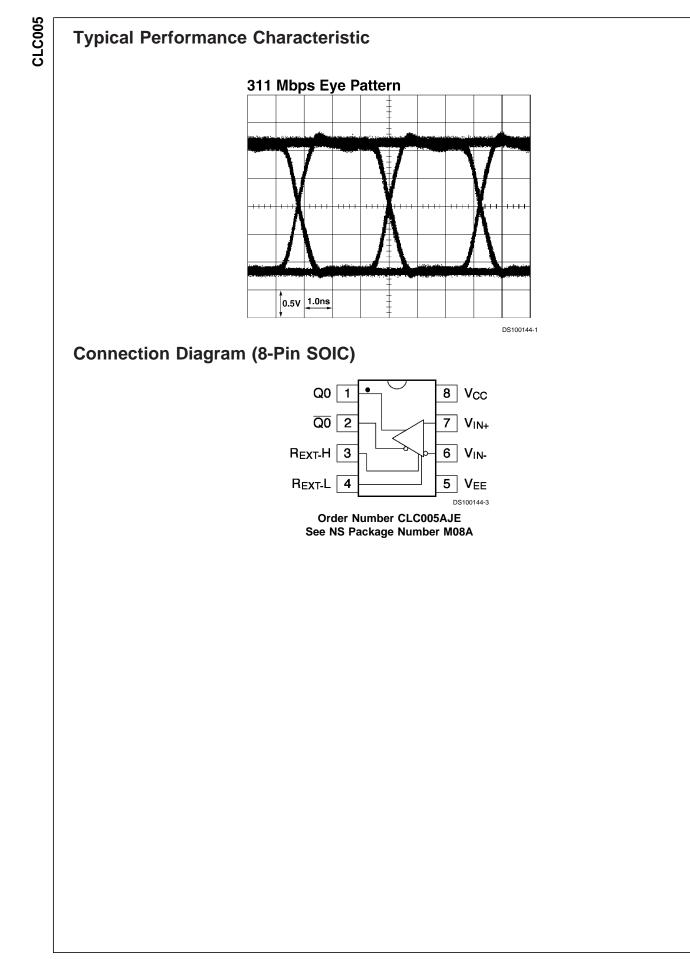
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75Ω

DS100144-2

Vo

≩75Ω ↓



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	6V
Output Current	30 mA
Maximum Junction Temperature	+125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature	
(Soldering 10 seconds)	+300°C
ESD Rating (Human Body Model)	1000V

Package Thermal Resistance
θ JA Surface Mount AJE125°C/WθJC Surface Mount AJE105°C/WReliability Information72Transistor count72MTTF254 Mhr

Recommended Operating Conditions

Supply Voltage Range (V $_{CC}$ -V $_{EE}$)

+4.5V to +5.5V

CLC005

Electrical Characteristics ($V_{CC} = 0V$, $V_{EE} = -5V$; unless otherwise specified).

Parameter	Condition	Тур +25°С	Min/Max +25°C	Min/Max 0°C to +70°C	Min/Max -40°C to +85°C	Units
STATIC DC PERFORMANCE	·		•			
	150Ω @ 270 Mbps (Notes 5, 7)	37	-	-	-	mA
Supply Current, Unloaded	(Note 3)	34	28/37	26/39	26/39	mA
Output HIGH Voltage (V _{OH})	(Note 3)	-1.7	-2.0/1.4	-2.0/1.4	-2.0/1.4	V
Output LOW Voltage (V _{OL})	(Note 3)	-3.7	-4.0/3.4	-4.0/3.4	-4.0/3.4	V
Input Bias Current	(Note 4)	10	30	50	50	μA
Output Swing	$R_{EXT} = \infty$ (Note 3)	2.0	1.86/2.14	1.86/2.14	1.86/2.14	V
Output Swing	$R_{EXT} = 10 \text{ k}\Omega \text{ (Note 5)}$	1.30	-	-	-	V
Common Mode Input Range Upper Limit		-0.7	-0.8	-0.8	-0.8	V
Common Mode Input Range Lower Limit		-2.6	-2.5	-2.5	-2.5	V
Minimum Differential Input Swing (Note 5)		200	200	200	200	mV
Power Supply Rejection Ratio (Note 3)		26	20	20	20	dB
AC PERFORMANCE						
Output Rise and Fall Time	(Notes 3, 6, 7)	650	425/825	400/850	400/850	ps
Overshoot	(Note 5)	5				%
Propagation Delay	(Note 5)	1.0				ns
Duty Cycle Distortion	(Note 5)	50				ps
Residual Jitter	(Note 5)	25	-	-	-	ps _{pp}
MISCELLANEOUS PERFORMANCE						•
Input Capacitance	(Note 5)	1.0				pF
Output Resistance	(Note 5)	10				Ω
Output Inductance	(Note 5)	6				nH

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Note 3: Spec is 100% tested at +25°C, sample tested at +85°C.

Note 4: Spec is 100% tested at +35 $^\circ\text{C}$ at wafer probe.

Note 5: Spec is guaranteed by design.

Note 6: Measured between the 20% and 80% levels of the waveform.

Note 7: Measured with both outputs driving 150 Ω , AC coupled at 270 Mbps.

Operation

INPUT INTERFACING

The CLC005 has high impedance, emitter-follower buffered, differential inputs. Single-ended signals may also be input. Transmission lines supplying input signals must be properly terminated close to the CLC005. Either A.C. or D.C. coupling as in *Figure 2* or *Figure 3* may be used. *Figures 2*, 4 and *Figure 5* show how Thevenin-equivalent resistor networks are

used to provide input termination and biasing. The input D.C. common-mode voltage range is 0.8V to 2.5V below the positive power supply (V_{CC}). Input signals plus bias should be kept within the specified common-mode range. For an 800 mV_{P-P} input signal, typical input bias levels range from 1.2V to 2.1V below the positive supply.

Load Type	Resistor to V _{cc} (R1)	Resistor to V _{EE} (R2)
ECL, 50Ω, 5V, V _T =2V	82.5Ω	124Ω
ECL, 50Ω, 5.2V, V _T =2V	80.6Ω	133Ω
ECL, 75Ω, 5V, V _T =2V	124Ω	187Ω
ECL, 75Ω, 5.2V, V _T =2V	121Ω	196Ω
$800mV_{P-P}$, 50Ω, 5V, V _T =1.6V	75.0Ω	154Ω
800mV _{P-P} , 75Ω, 5V, V _T =1.6V	110Ω	232Ω
800mV _{P-P} , 2.2K Ω , 5V, V _T =1.6V	3240Ω	6810Ω

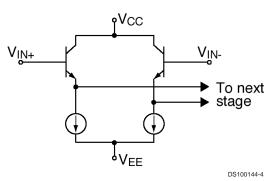


FIGURE 1. Input Stage

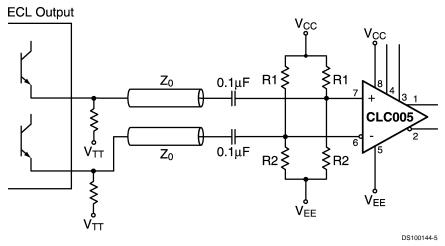


FIGURE 2. AC Coupled Input

Operation (Continued)

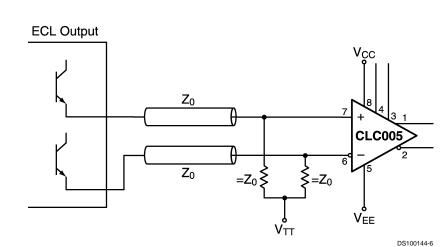


FIGURE 3. DC Coupled Input

OUTPUT INTERFACING

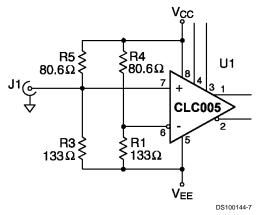


FIGURE 4. Single Ended 50 Ω ECL Input

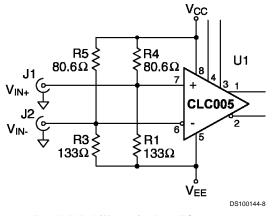
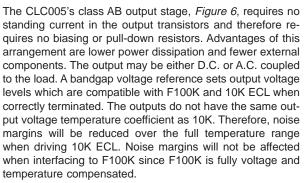


FIGURE 5. Differential 50 Ω ECL Input



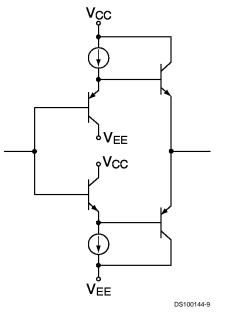


FIGURE 6. Output Stage

Operation (Continued)

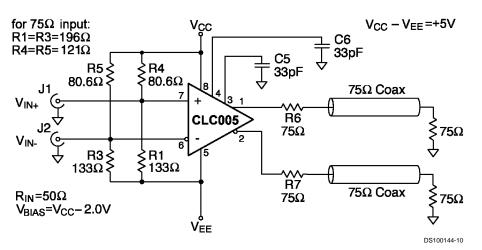


FIGURE 7. Differential Input DC Coupled Output

OUTPUT AMPLITUDE ADJUSTMENT

The high and low output levels of the CLC005 are set by a circuit shown simplified in Figure 8. Output high and low levels may be set independently with external resistor networks connected between $R_{\text{EXT-H}}$ (pin 3), $R_{\text{EXT-L}}$ (pin 4) and the power supplies. The resistor networks affect the high and low output levels by changing the internally generated bias voltages, $V_{\rm H}$ and V $_{\rm L}.$ The nominal high and low output levels are V_{CC} -1.7V and V_{CC} -3.7V, respectively, when the pins $R_{\text{EXT-H}}$ and $R_{\text{EXT-L}}$ are left unconnected. Though the internal components which determine output voltage levels have accurate ratios, their absolute values may be controlled only within about ±15% of nominal. Even so, without external adiustment, output voltages are well controlled. A final design should accommodate the variation in externally set output voltages due to the CLC005's part-to-part and external component tolerances.

Output voltage swing may be reduced with the circuit shown in *Figure 9*. A single resistance chosen with the aid of the graph, *Figure 10*, is connected between pins 3 and 4. Output voltage swing may be increased with the circuit of *Figure 11*. *Figure 12* is used to estimate a value for resistor R. Note that both of these circuits and the accompanying graphs assume that the CLC005 is loaded with the standard 150 Ω . Be aware that output loading will affect the output swing and the high

and low levels. It may be necessary to empirically select resistances used to set output levels when the D.C. loading on the CLC005 differs appreciably from 150Ω .

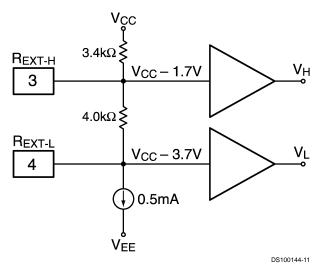
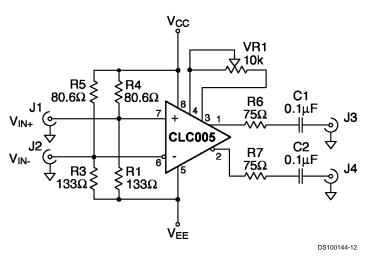
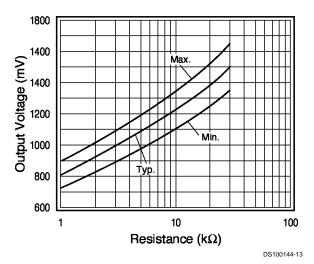


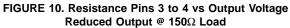
FIGURE 8. Equivalent Bias Generation Circuit











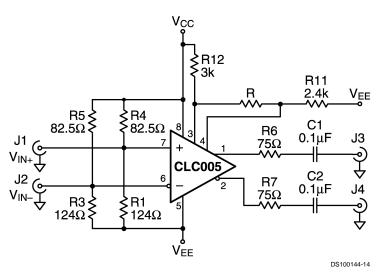


FIGURE 11. Differential Input Increased Output

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Operation (Continued)

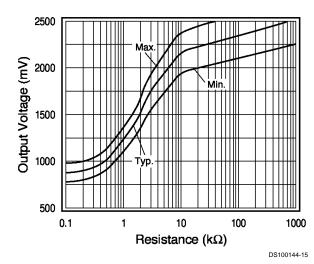


FIGURE 12. Resistance Pins 3 to 4 vs Output Voltage Increased Output @ 150Ω Load

OUTPUT RISE AND FALL TIMES

Output load capacitance can significantly affect output rise and fall times. The effect of load capacitance, stray or otherwise, may be reduced by placing the output back-match resistor close to the output pin and by minimizing all interconnecting trace lengths. *Figure 13* shows the effect on risetime of parallel load capacitance across a 150Ω load.

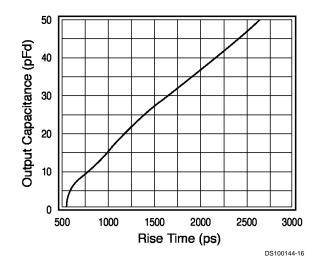


FIGURE 13. Rise Time vs CL

PCB Layout Recommendations

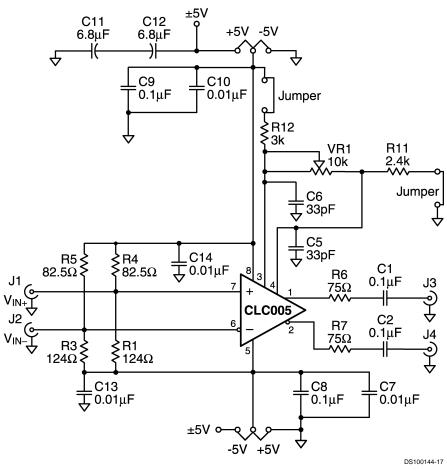
Printed circuit board layout affects the performance of the CLC005. The following guidelines will aid in achieving satisfactory device performance.

- Use a ground plane or power/ground plane sandwich design for optimum performance.
- Bypass device power with a 0.01 µF monolithic ceramic capacitor in parallel with a 6.8 µF tantalum electrolytic capacitor located no more than 0.1" (2.5 mm) from the device power pins.
- Provide short, symmetrical ground return paths for:
 - inputs,
 - supply bypass capacitors and
 - the output load.
- Provide short, grounded guard traces located
 - under the centerline of the package,
 - 0.1" (2.5 mm) from the package pins
 - on both top and bottom of the board with connecting vias.

EVALUATION BOARD

A schematic, parts list and layout for a suitable evaluation board are given on the following page. The artwork includes trace, silk screen and ground layers. The individual printed circuit board is available unassembled from National Semiconductor. To order this evaluation board, part number CLC730056, contact your local sales representative or the National Semiconductor Customer Response Center in your area. (This evaluation board is identical to that for the CLC007 for which some of the listed parts are not required.)

The evaluation board is a guide to proper circuit layout and makes prototyping and measurement-taking easy. Since the board is designed to accommodate many of the application circuits possible with the CLC005, your particular application may not require all of the listed parts or may require different values. The evaluation board may be powered from standard ECL supply voltages by installing the two jumpers in the locations labeled "–5". For PECL supply voltages, install the jumpers in the locations labeled "+5".

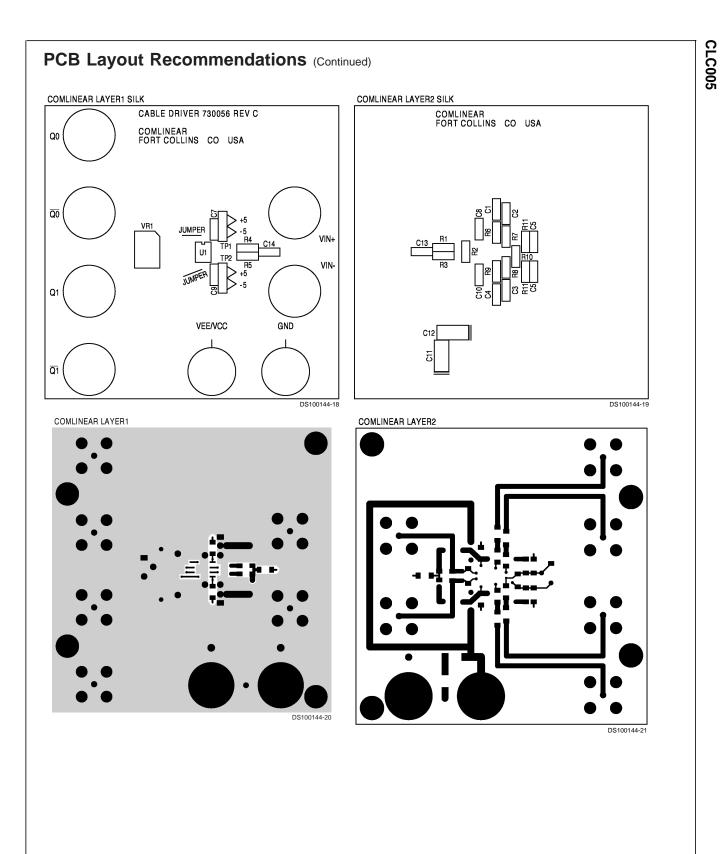


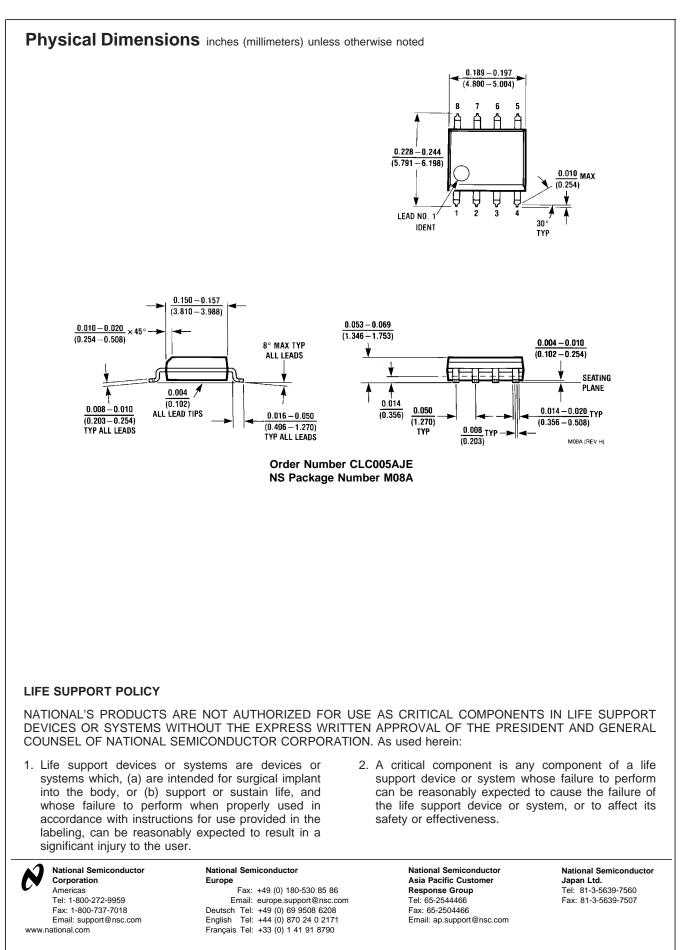
CLC005 Evaluation Board Schematic

CLC005

PCB Layout Recommendations (Continued)

ltem	Reference Designator	Part Description	Qty
1	C1, C2, C8, C9	0.1 µF SMD Capacitor, Size 1206	4
2	C5, C60	33 pF SMD Capacitor, Size 1206	2
3	C7, C10, C13, C14	0.01 µF SMD Tantalum Capacitor, Size 12062	4
4	C11, C12	6.8 µF SMD Tantalum Capacitor, Size 6032	2
5	J1, J2	BNC PC Amphenol #31-5329-52RFX	2
6	J3, J4	BNC PC Amphenol #31-5329-72RFX	2
7	R3, R1	124Ω SMD Resistor, Size 1206	2
8	R4, R5	82.5Ω SMD Resistor, Size 1206	2
9	R6,R7	75Ω SMD Resistor, Size 1206	2
10	R11	2.4 kΩ SMD Resistor, Size 1206	1
11	R12	3 kΩ SMD Resistor, Size 1206	1
12	U1	CLC005AJE Cable Driver	1
13	+5, -5	Jumper	4
14	VR1	10 kΩ Potentiometer, Bourns 3299	1





National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.