National Semiconductor

April 2001

DS90LV001
3.3V LVDS-LVDS Buffer

General Description

The DS90LV001 LVDS-LVDS Buffer takes an LVDS input signal and provides an LVDS output signal. In many large systems, signals are distributed across backplanes, and one of the limiting factors for system speed is the 'stub length' or the distance between the transmission line and the unterminated receivers on individual cards. Although it is generally recognized that this distance should be as short as possible to maximize system performance, real-world packaging concerns often make it difficult to make the stubs as short as the designer would like.

The DS90LV001, available in the LLP (Leadless Leadframe Package) package, will allow the receiver to be placed very close to the main transmission line, thus improving system performance.

A wide input dynamic range will allow the DS90LV001 to receive differential signals from LVPECL as well as LVDS sources. This will allow the device to also fill the role of an LVPECL-LVDS translator.

An output enable pin is provided, which allows the user to place the LVDS output in TRI-STATE.

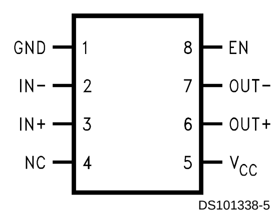
The DS90LV001 is offered in two package options, an 8 pin LLP and SOIC.

Features

- Single +3.3 V Supply
- LVDS receiver inputs accept LVPECL signals
- TRI-STATE outputs
- Receiver input threshold < ±100 mV
- Fast propagation delay of 1.4 ns (typ)
- Low jitter 800 Mbps fully differential data path
- 100 ps (typ) of pk-pk jitter with PRBS = $2^{23}-1$ data pattern at 800 Mbps
- Compatible with ANSI/TIA/EIA-644-A LVDS standard
- 8 pin SOIC and space saving (70%) LLP package
- Industrial Temperature Range

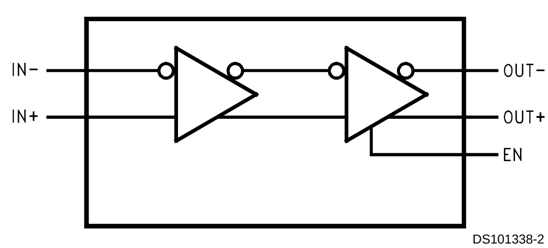
Connection Diagram

Top View



Order Number DS90LV001TM, DS90LV001TLD
See NS Package Number M08A, LDA08A

Block Diagram



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
LVCMOS/LVTTL Input Voltage (EN)	−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage (IN+, IN−)	−0.3V to +4V
LVDS Driver Output Voltage (OUT+, OUT−)	−0.3V to +4V
LVDS Output Short Circuit Current	Continuous
Junction Temperature	+150˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature Range	
Soldering (4 sec.)	+260˚C
Maximum Package Power Dissipation at 25˚C	
M Package	726 mW
Derate M Package	5.8 mW/˚C above +25˚C
LDA Package	2.44 W
Derate LDA Package	19.49 mW/˚C above +25˚C
ESD Ratings	
(HBM, 1.5kΩ, 100pF)	≥2.5kV
(EIAJ, 0Ω, 200pF)	≥250V

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Receiver Input Voltage	0		V_{CC}	V
Operating Free Air Temperature	−40	+25	+85	˚C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVCMOS/LVTTL DC SPECIFICATIONS (EN)							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IH}	High Level Input Current	V_{IN} = 3.6V or 2.0V, V_{CC} = 3.6V			+7	+20	μA
I_{IL}	Low Level Input Current	V_{IN} = GND or 0.8V, V_{CC} = 3.6V			±1	±10	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.6	−1.5	V
LVDS OUTPUT DC SPECIFICATIONS (OUT)							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	325	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States	*Figure 1* and *Figure 2*				20	mV
V_{OS}	Offset Voltage	R_L = 100Ω		1.080	1.19	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States	*Figure 1*				20	mV
I_{OZ}	Output TRI-STATE Current	EN = 0V, V_{OUT} = V_{CC} or GND			±1	±10	μA
I_{OFF}	Power-Off Leakage Current	V_{CC} = 0V, V_{OUT} = 3.6V or GND			±1	±10	μA
I_{OS}	Output Short Circuit Current (Note 4)	EN = V_{CC}, V_{OUT+} and V_{OUT-} = 0V			−16	−24	mA
I_{OSD}	Differential Output Short Circuit Current (Note 4)	EN = V_{CC}, V_{OD} = 0V			−7	−12	mA
LVDS RECEIVER DC SPECIFICATIONS (IN)							
V_{TH}	Differential Input High Threshold	V_{CM} = +0.05V, +1.2V or +3.25V			0	+100	mV
V_{TL}	Differential Input Low Threshold			−100	0		mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 100mV, V_{CC} = 3.3V		0.05		3.25	V
I_{IN}	Input Current	V_{IN} = +3.0V	V_{CC} = 3.6V or 0V		±1	±10	μA
		V_{IN} = 0V			±1	±10	μA
ΔI_{IN}	Change in Magnitude of I_{IN}	V_{IN} = +3.0V	V_{CC} = 3.6V or 0V		1	6	μA
		V_{IN} = 0V			1	6	μA
SUPPLY CURRENT							
I_{CCD}	Total Supply Current	EN = V_{CC}, R_L = 100Ω, C_L = 5 pF			47	70	mA
I_{CCZ}	TRI-STATE Supply Current	EN = 0V			22	35	mA

AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 5pF *Figure 3* and *Figure 4*	1.0	1.4	2.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.0	1.4	2.0	ns
t_{SKD1}	Pulse Skew $\|t_{PLHD} - t_{PHLD}\|$ (Note 5) (Note 6)			20	200	ps
t_{SKD3}	Part to Part Skew (Note 5) (Note 7)			0	60	ps
t_{SKD4}	Part to Part Skew (Note 5) (Note 8)				400	ps
t_{LHT}	Rise Time (Note 5)	R_L = 100Ω, C_L = 5pF *Figure 3* and *Figure 5*	200	320	450	ps
t_{HLT}	Fall Time (Note 5)		200	310	450	ps
t_{PHZ}	Disable Time (Active High to Z)	R_L = 100Ω, C_L = 5pF *Figure 6* and *Figure 7*		3	25	ns
t_{PLZ}	Disable Time (Active Low to Z)			3	25	ns
t_{PZH}	Enable Time (Z to Active High)			25	45	ns
t_{PZL}	Enable Time (Z to Active Low)			25	45	ns
t_{DJ}	LVDS Data Jitter, Deterministic (Peak-to-Peak) (Note 9)	V_{ID} = 300mV; PRBS = $2^{23} - 1$ data; V_{CM} = 1.2V at 800Mbps (NRZ)		100	135	ps
t_{RJ}	LVDS Clock Jitter, Random (Note 9)	V_{ID} = 300mV; V_{CM} = 1.2V at 400MHz clock		2.2	3.5	ps

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.

Note 3: All typical are given for V_{CC} = +3.3V and T_A = +25˚C, unless otherwise stated.

Note 4: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Note 5: The parameters are guaranteed by design. The limits are based on statistical analysis of the device performance over the PVT (process, voltage and temperature) range.

Note 6: t_{SKD1}, $|t_{PLHD} - t_{PHLD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

Note 7: t_{SKD3}, Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5˚C of each other within the operating temperature range.

Note 8: t_{SKD4}, Part to Part Skew, is the differential channel-to- channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.

Note 9: The parameters are guaranteed by design. The limits are based on statistical analysis of the device performance over the PVT range with the following test equipment setup: HP8133A (pattern pulse generator), 5 feet of RG142B cable with DUT test board and HP83480A (digital scope mainframe) with HP83484A (50GHz scope module). The HP8133A with RG142B cable exhibit a t_{DJ} = 21ps and t_{RJ} = 1.8ps.

DC Test Circuits

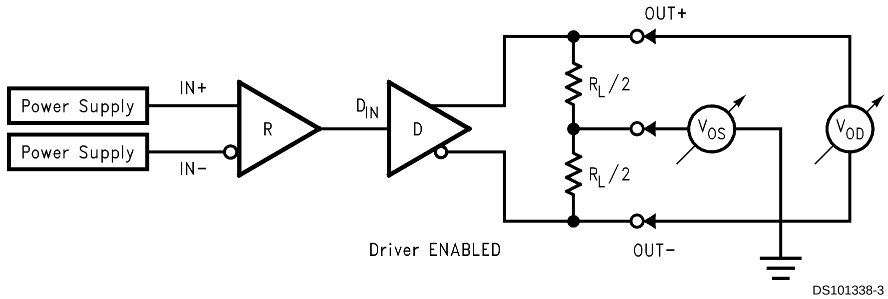


FIGURE 1. Differential Driver DC Test Circuit

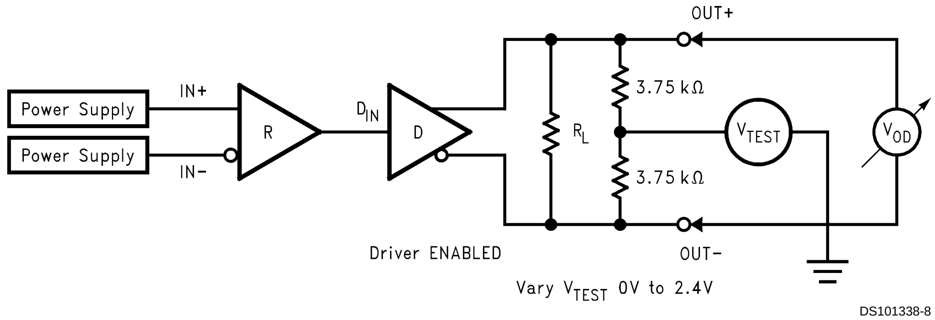


FIGURE 2. Differential Driver Full Load DC Test Circuit

AC Test Circuits and Timing Diagrams

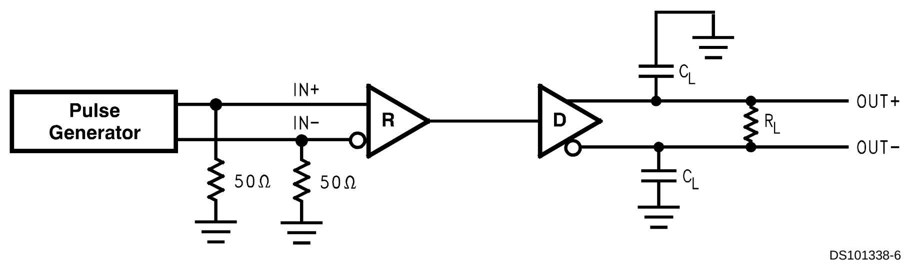


FIGURE 3. LVDS Output Load

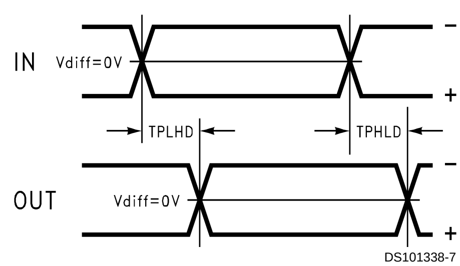


FIGURE 4. Propagation Delay Low-to-High and High-to-Low

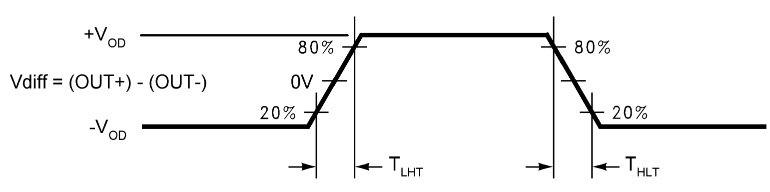
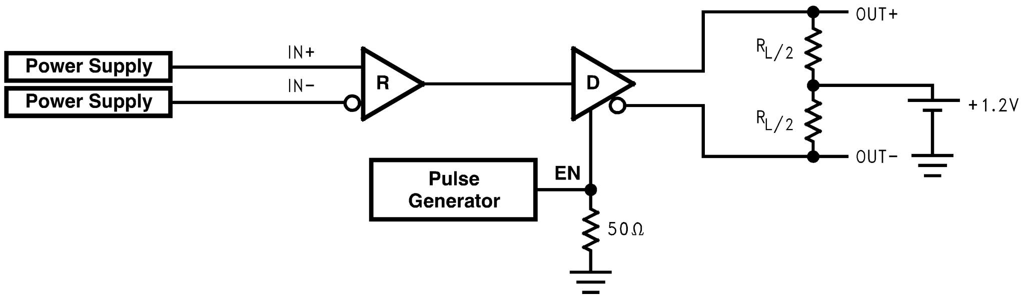


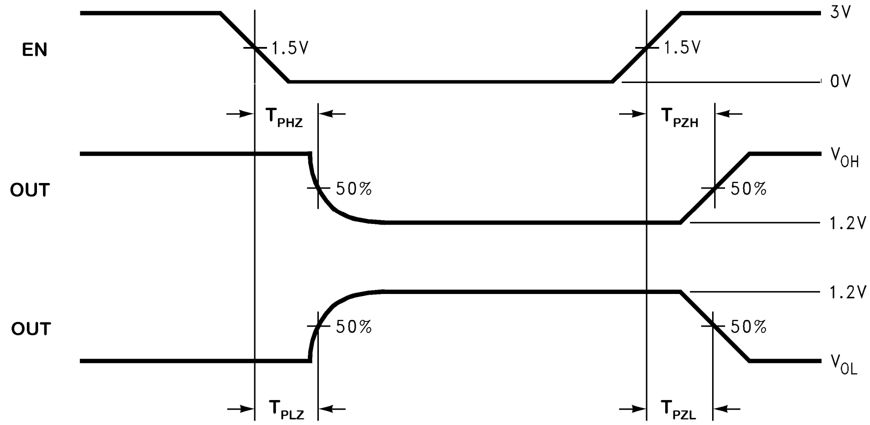
FIGURE 5. LVDS Output Transition Time

AC Test Circuits and Timing Diagrams (Continued)



DS101338-1

FIGURE 6. TRI-STATE Delay Test Circuit



DS101338-4

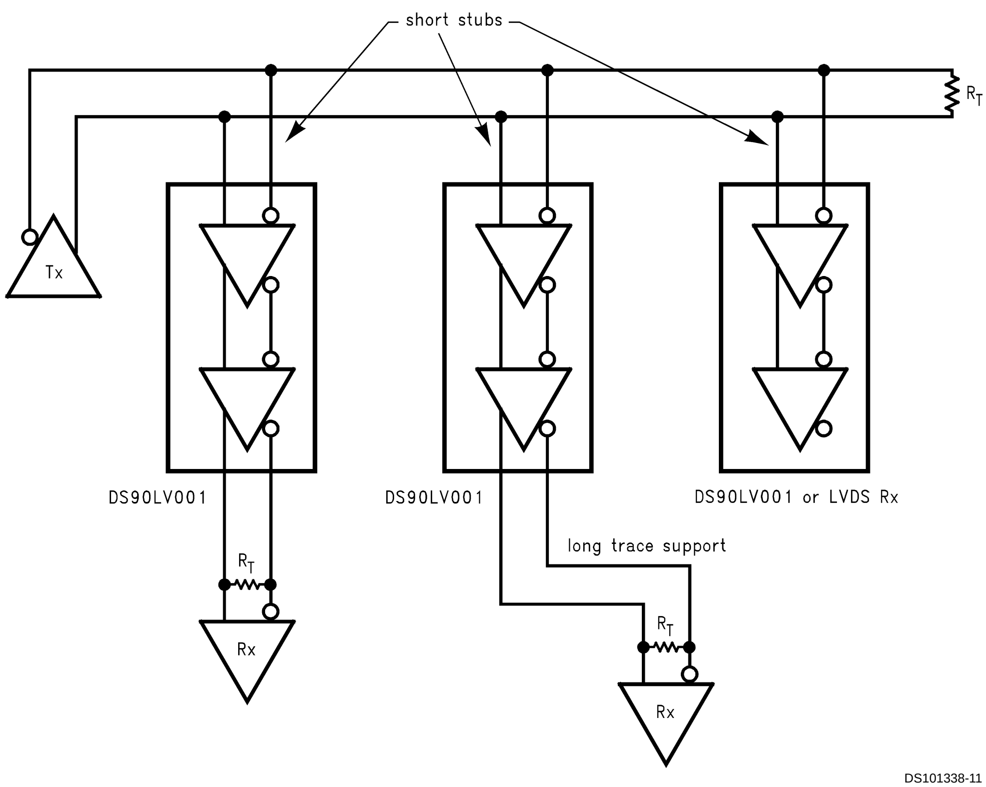
FIGURE 7. Output active to TRI-STATE and TRI-STATE to active output time

DS90LV001 Pin Description (SOIC and LLP)

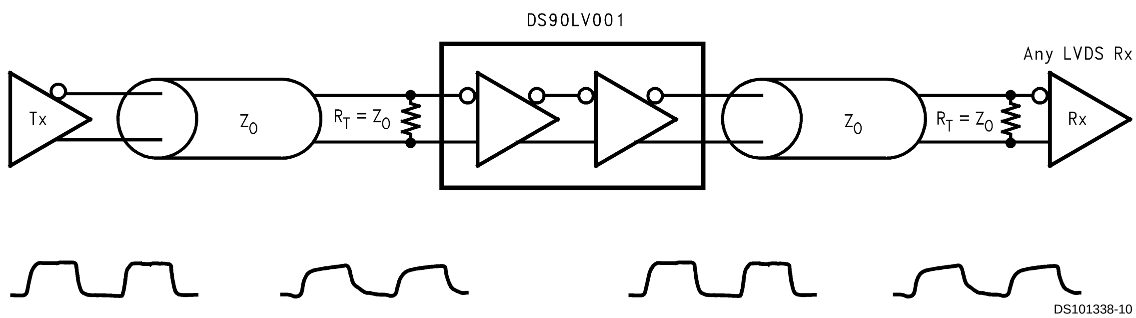
Pin Name	Pin #	Input/Output	Description
GND	1	P	Ground
IN −	2	I	Inverting receiver LVDS input pin
IN+	3	I	Non-inverting receiver LVDS input pin
NC	4		No Connect
V_{CC}	5	P	Power Supply, 3.3V ± 0.3V.
OUT+	6	O	Non-inverting driver LVDS output pin
OUT -	7	O	Inverting driver LVDS output pin
EN	8	I	Enable pin. When EN is LOW, the driver is disabled and the LVDS outputs are in TRI-STATE. When EN is HIGH, the driver is enabled. LVCMOS/LVTTL levels.

Typical Applications

Backplane Stub-Hider Application



Cable Repeater Application



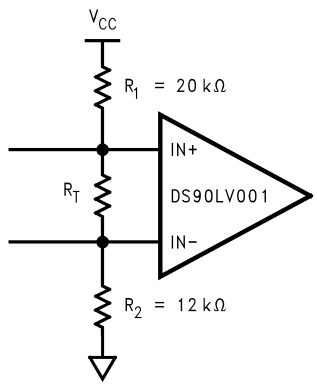
Application Information

Mode of Operation:

The DS90LV001 can be used as a 'stub-hider.' In many systems, signals are distributed across backplanes, and one of the limiting factors for system speed is the 'stub length' or the distance between the transmission line and the unterminated receivers on the individual cards. Although it is generally recognized that this distance should be as short as possible to maximize system performance, real-world packaging concerns and PCB designs often make it difficult to make the stubs as short as the designer would like. The DS90LV001, available in the LLP (Leadless Leadframe Package) package, can improve system performance by allowing the receiver to be placed very close to the main transmission line either on the backplane itself or very close to the connector on the card. Longer traces to the LVDS receiver may be placed after the DS90LV001. This very small LLP package is a 75% space savings over the SOIC package.

Input failsafe:

The receiver inputs of the DS90LV001 do not have internal failsafe biasing. For point-to-point and multidrop applications with a single source, failsafe biasing may not be required. When the driver is off, the link is in-active. If failsafe biasing is required, this can be accomplished with external high value resistors. Using the equations in the LVDS Owner's Manual Chapter 4, the IN+ should be pull to V_{CC} (3.3V) with 20kΩ and the IN− should be pull to GND with 12kΩ. This provides a slight positive differential bias, and sets a known HIGH state on the link with a minimum amount of distortion.



DS101338-15

PCB Layout and Power System Bypass:

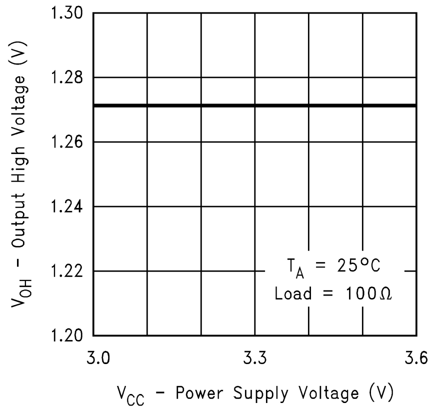
Circuit board layout and stack-up for the DS90LV001 should be designed to provide noise-free power to the device. Good layout practice also will separate high frequency or high level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range 0.01 µF to 0.1 µF. Tantalum capacitors may be in the range 2.2 µF to 10 µF. Voltage rating for tantalum capacitors should be at least 5X the power supply voltage being used. It is recommended practice to use two vias at each power pin of the DS90LV001 as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance by up to half, thereby reducing interconnect inductance and extending the effective frequency range of the bypass components.

The outer layers of the PCB may be flooded with additional ground plane. These planes will improve shielding and isolation as well as increase the intrinsic capacitance of the power supply plane system. Naturally, to be effective, these planes must be tied to the ground supply plane at frequent intervals with vias. Frequent via placement also improves signal integrity on signal transmission lines by providing short paths for image currents which reduces signal distortion. The planes should be pulled back from all transmission lines and component mounting pads a distance equal to the width of the widest transmission line or the thickness of the dielectric separating the transmission line from the internal power or ground plane(s) whichever is greater. Doing so minimizes effects on transmission line impedances and reduces unwanted parasitic capacitances at component mounting pads.

There are more common practices which should be followed when designing PCBs for LVDS signaling. Please see application note AN-1108 for guidelines. In addition, application note AN-1187 has additional information specifically related to LLP recommendations.

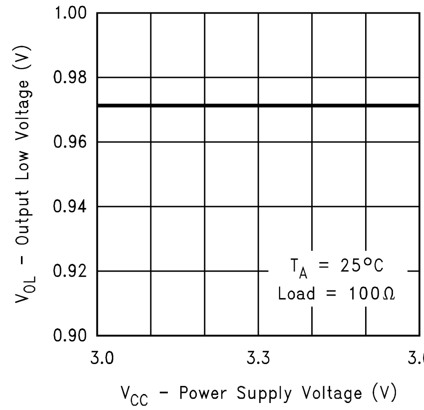
Typical Performance Curves

Output High Voltage vs Power Supply Voltage



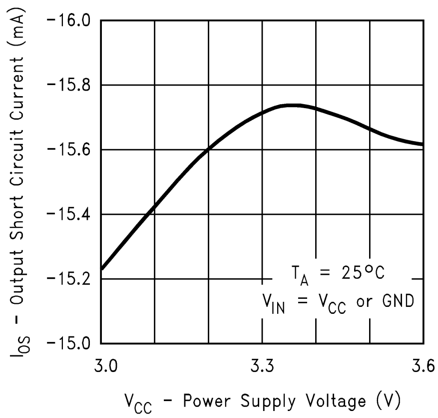
DS101338-16

Output Low Voltage vs Power Supply Voltage



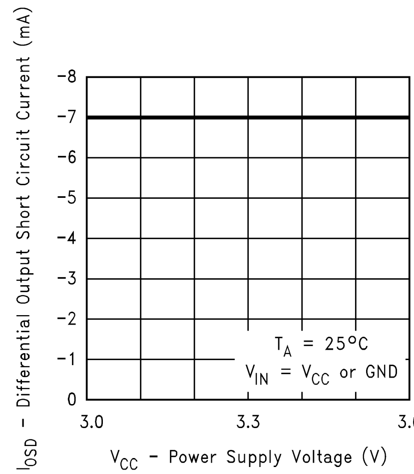
DS101338-17

Output Short Circuit Current vs Power Supply Voltage



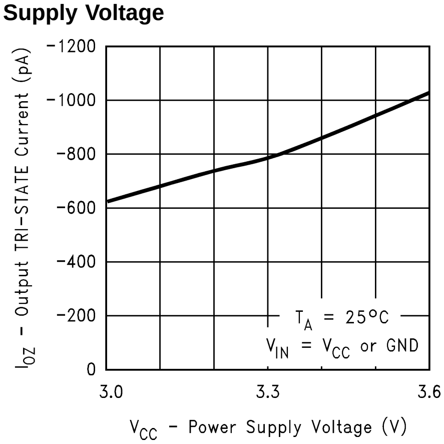
DS101338-18

Differential Output Short Circuit Current vs Power Supply Voltage



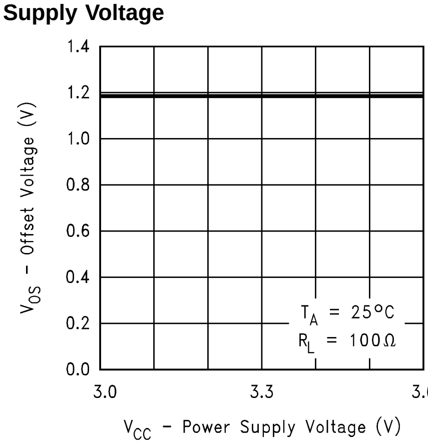
DS101338-19

Output TRI-STATE Current vs Power Supply Voltage



DS101338-20

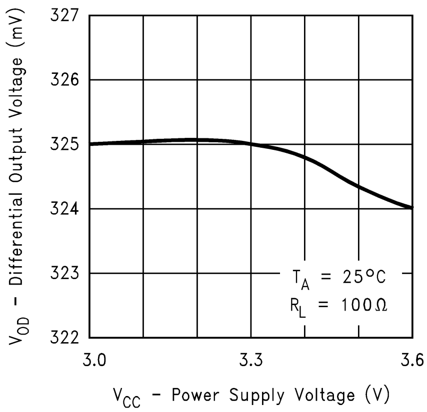
Offset Voltage vs Power Supply Voltage



DS101338-21

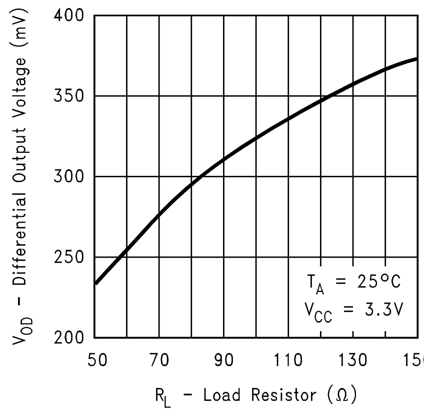
Typical Performance Curves (Continued)

Differential Output Voltage vs Power Supply Voltage



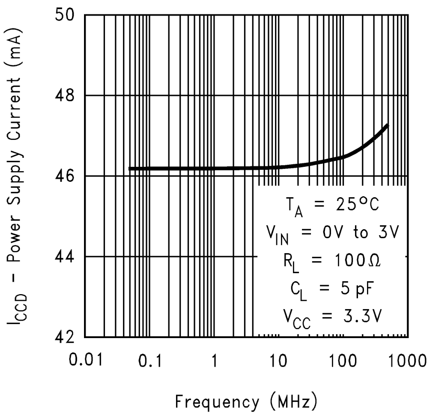
DS101338-22

Differential Output Voltage vs Load Resistor



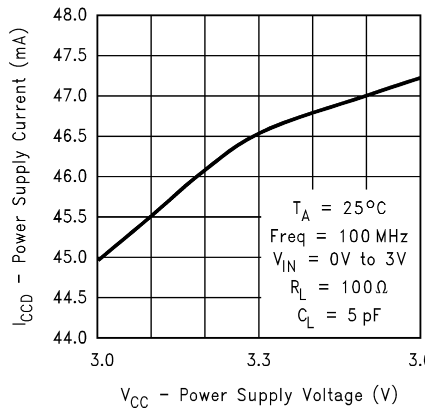
DS101338-23

Power Supply Current vs Frequency



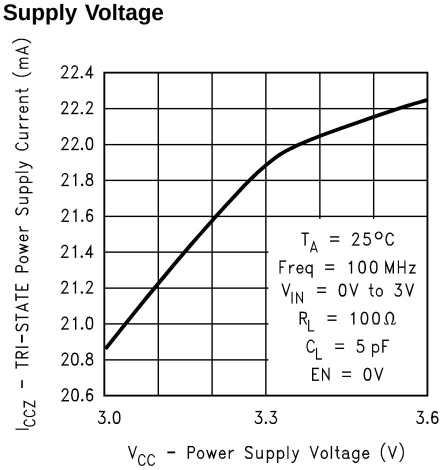
DS101338-24

Power Supply Current vs Power Supply Voltage



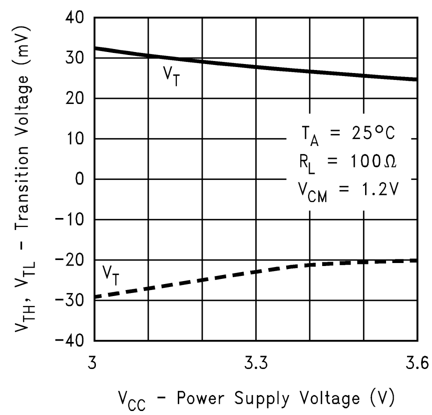
DS101338-25

TRI-STATE Power Supply Current vs Power Supply Voltage



DS101338-26

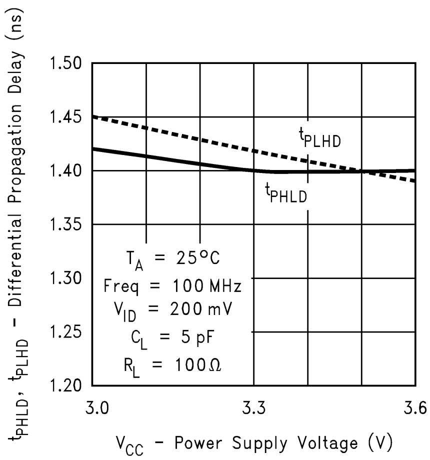
Differential Transition Voltage vs Power Supply Voltage



DS101338-27

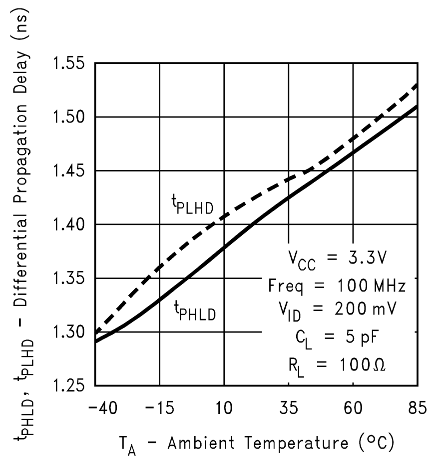
Typical Performance Curves (Continued)

Differential Propagation Delay vs Power Supply Voltage



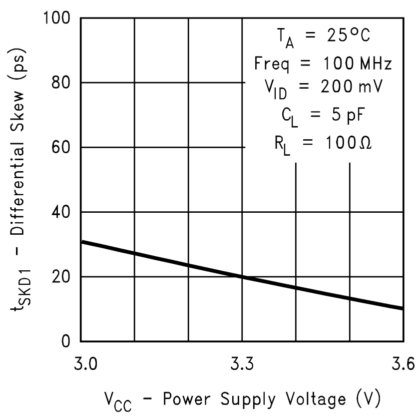
DS101338-28

Differential Propagation Delay vs Ambient Temperature



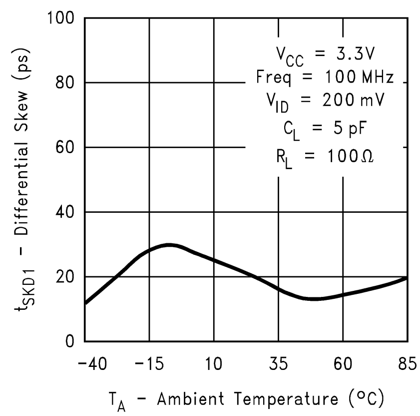
DS101338-36

Differential Skew vs Power Supply Voltage



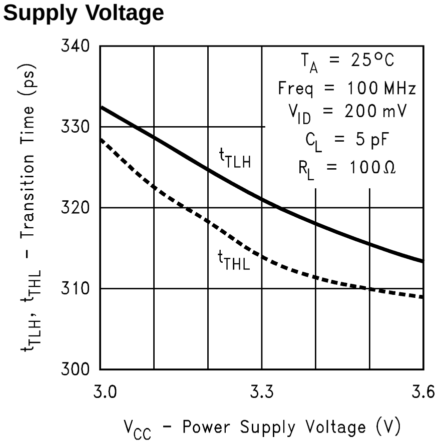
DS101338-29

Differential Skew vs Ambient Temperature



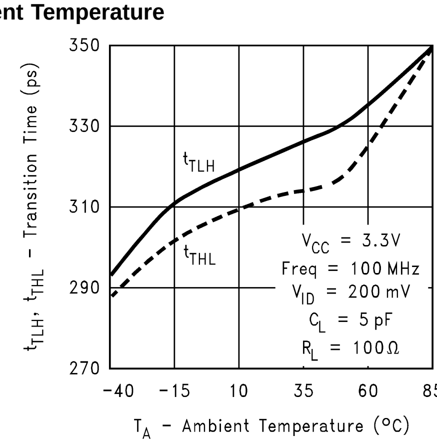
DS101338-37

Transition Time vs Power Supply Voltage



DS101338-30

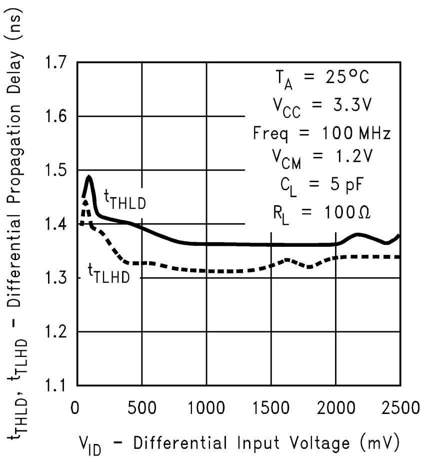
Transition Time vs Ambient Temperature



DS101338-38

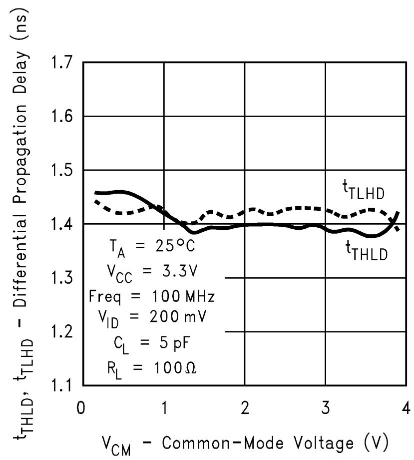
Typical Performance Curves (Continued)

Differential Propagation Delay vs Differential Input Voltage



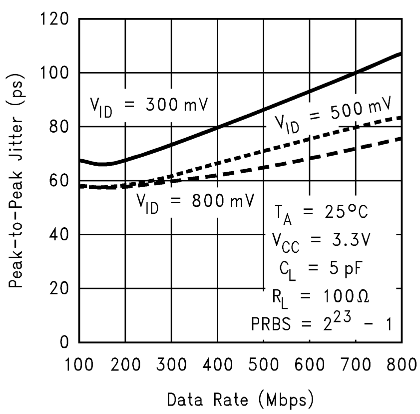
DS101338-31

Differential Propagation Delay vs Common-Mode Voltage



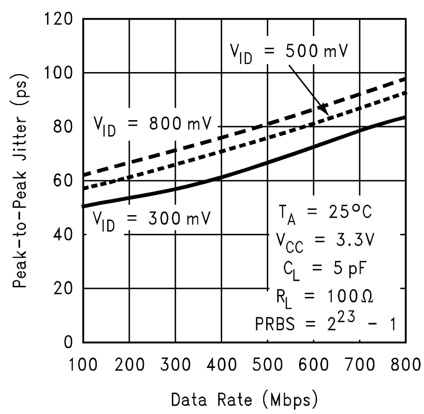
DS101338-32

Peak-to-Peak Output Jitter at V_{CM} = 0.4V vs Differential Input Voltage



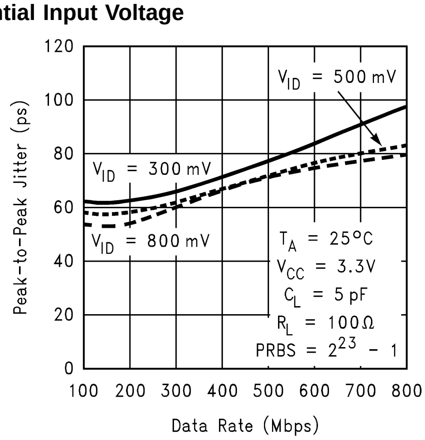
DS101338-33

Peak-to-Peak Output Jitter at V_{CM} = 2.9V vs Differential Input Voltage



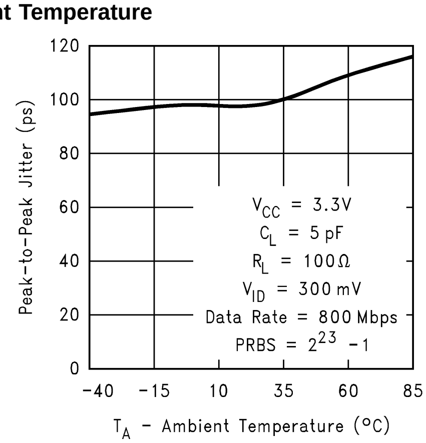
DS101338-35

Peak-to-Peak Output Jitter at V_{CM} = 1.2V vs Differential Input Voltage



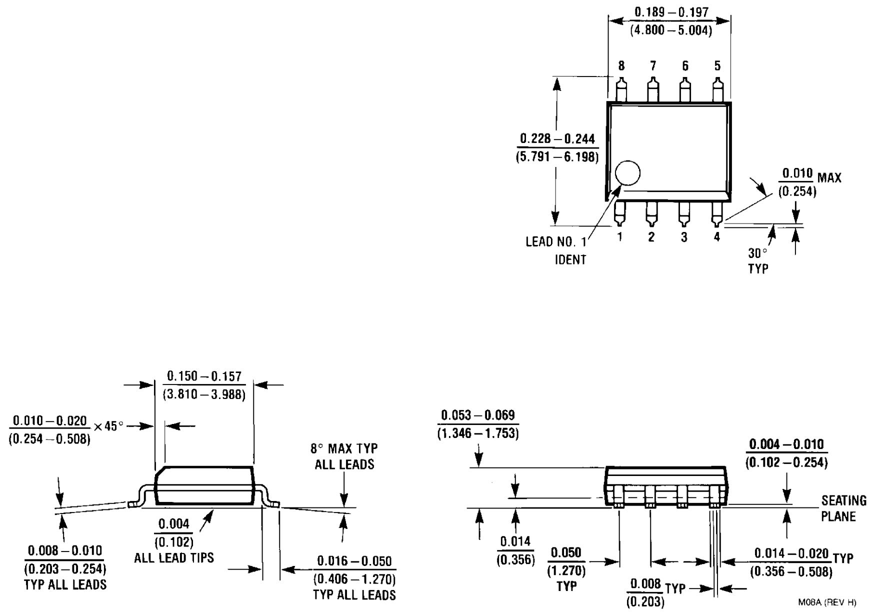
DS101338-34

Peak-to-Peak Output Jitter at V_{CM} = 1.2V vs Ambient Temperature

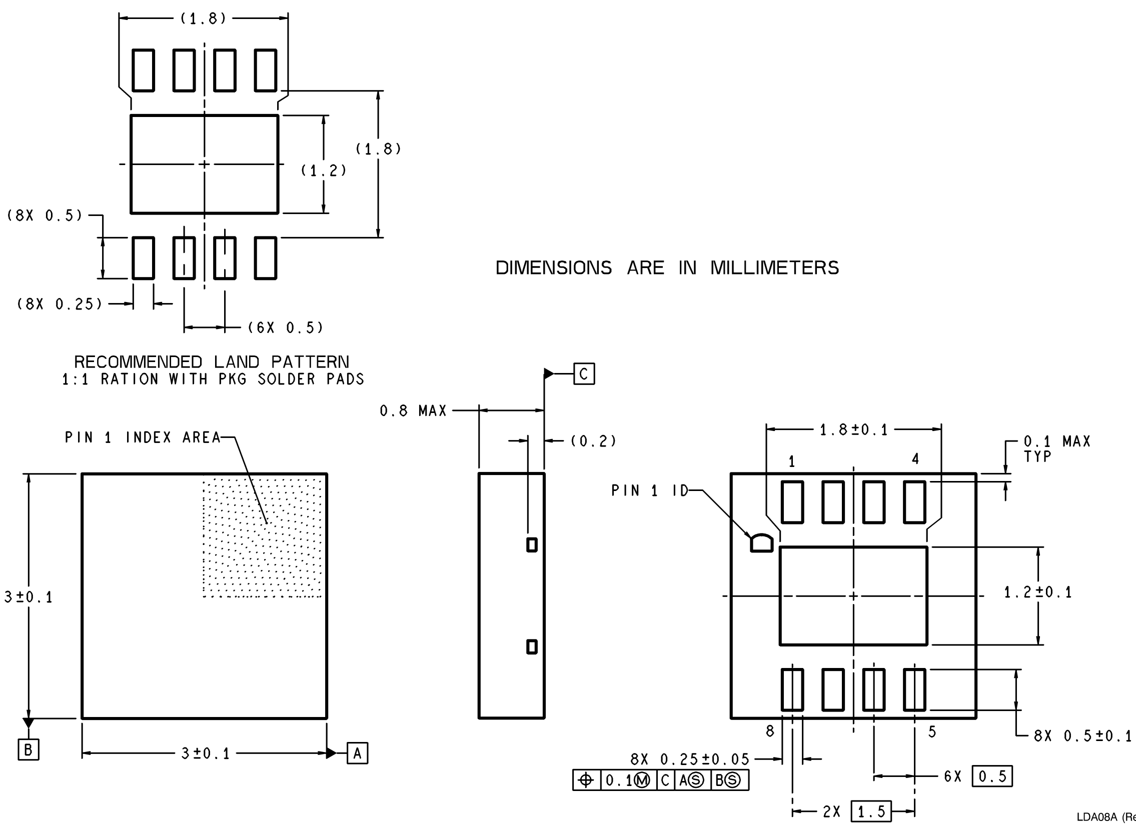


DS101338-39

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number DS90LV001TM
See NS Package Number M08A



Order Number DS90LV001TLD
See NS Package Number LDA08A

Notes

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com
www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507