August 2002

National Semiconductor

DS90LV012A/DS90LT012A
3V LVDS Single CMOS Differential Line Receiver

General Description

The DS90LV012A and DS90LT012A are single CMOS differential line receivers designed for applications requiring ultra low power dissipation, low noise, and high data rates. The devices are designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Swing (LVDS) technology

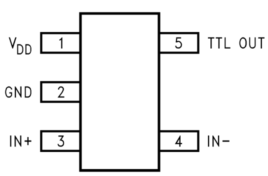
The DS90LV012A and DS90LT012A accept low voltage (350 mV typical) differential input signals and translates them to 3V CMOS output levels. The receivers also support open, shorted, and terminated (100Ω) input fail-safe. The receiver output will be HIGH for all fail-safe conditions. The DS90LV012A has a pinout designed for easy PCB layout. The DS90LT012A includes an input line termination resistor for point-to-point applications.

The DS90LV012A and DS90LT012A, and companion LVDS line driver provide a new alternative to high power PECL/ECL devices for high speed interface applications.

Features

- Compatible with ANSI TIA/EIA-644-A Standard
- >400 Mbps (200 MHz) switching rates
- 100 ps differential skew (typical)
- 3.5 ns maximum propagation delay
- Integrated line termination resistor (102Ω typical)
- Single 3.3V power supply design (2.7V to 3.6V range)
- Power down high impedance on LVDS inputs
- Accepts small swing (350 mV typical) differential signal levels
- LVDS receiver inputs accept LVDS/BLVDS/LVPECL inputs
- Supports open, short and terminated input fail-safe
- Pinout simplifies PCB layout
- Low Power Dissipation (10mW typical@ 3.3V static)
- SOT-23 5-lead package
- Leadless LLP-8 package (3x3 mm body size)
- SOT version pin compatible with SN65LVDS2, SN65LVDT2
- Electrically similar to the DS90LV018A
- Fabricated with advanced CMOS process technology
- Industrial temperature operating range (−40˚C to +85˚C)

Connection Diagrams



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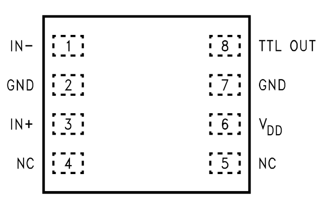
(Top View)
Order Number DS90LV012ATMF, DS90LT012ATMF
See NS Package Number MF05A



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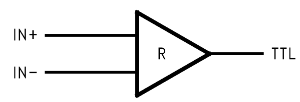
(Top View)
Order Number DS90LV012ATLD, DS90LT012ATLD
See NS Package Number LDA08A

Functional Diagram

DS90LV012A



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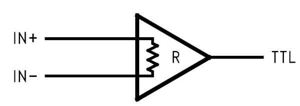
DS90LT012A



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Truth Table

INPUTS	OUTPUT
[IN+] – [IN–]	**TTL OUT**
$V_{ID} \geq 0V$	H
$V_{ID} \leq -0.1V$	L
Full Fail-safe OPEN/SHORT or Terminated	H

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.3V to +4V
Input Voltage (IN+, IN−)	−0.3V to +3.9V
Output Voltage (TTL OUT)	−0.3V to (V_{DD} + 0.3V)
Output Short Circuit Current	−100mA
Maximum Package Power Dissipation @ +25˚C	
LDA Package	2.26 W
Derate LDA Package	18.1 mW/˚C above +25˚C
Thermal resistance (θ_{JA})	55.3˚C/W
MF Package	902mW
Derate MF Package	7.22 mW/˚C above +25˚C
Thermal resistance (θ_{JA})	138.5˚C/W
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature Range Soldering (4 sec.)	+260˚C
Maximum Junction Temperature	+150˚C
ESD Ratings (Note 4)	

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{DD})	+2.7	+3.3	+3.6	V
Operating Free Air Temperature (T_A)	−40	25	+85	˚C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{CM} dependant on V_{DD} (Note 11)		IN+, IN−		−30	0	mV
V_{TL}	Differential Input Low Threshold				−100	−30		mV
V_{CM}	Common-Mode Voltage	V_{DD} = 2.7V, V_{ID} = 100mV			0.05		2.35	V
		V_{DD} = 3.0V to 3.6V, V_{ID} = 100mV			0.05		V_{DD} - 0.3V	V
I_{IN}	Input Current (DS90LV012A)	V_{IN} = +2.8V	V_{DD} = 3.6V or 0V		−10	±1	+10	μA
		V_{IN} = 0V			−10	±1	+10	μA
		V_{IN} = +3.6V	V_{DD} = 0V		−20		+20	μA
ΔI_{IN}	Change in Magnitude of I_{IN}	V_{IN} = +2.8V	V_{DD} = 3.6V or 0V			4		μA
		V_{IN} = 0V				4		μA
		V_{IN} = +3.6V	V_{DD} = 0V			4		μA
I_{IND}	Differential Input Current (DS90LT012A)	V_{IN+} = +0.4V, V_{IN-} = +0V			3	3.9	4.4	mA
		V_{IN+} = +2.4V, V_{IN-} = +2.0V						
R_T	Integrated Termination Resistor (DS90LT012A)					102		Ω
C_{IN}	Input Capacitance	IN+ = IN− = GND				3		pF
V_{OH}	Output High Voltage	I_{OH} = −0.4 mA, V_{ID} = +200 mV		TTL OUT	2.4	3.1		V
		I_{OH} = −0.4 mA, Inputs terminated			2.4	3.1		V
		I_{OH} = −0.4 mA, Inputs shorted			2.4	3.1		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{ID} = −200 mV				0.3	0.5	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 5)			−15	−50	−100	mA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−1.5	−0.7		V
I_{DD}	No Load Supply Current	Inputs Open		V_{DD}		5.4	9	mA

Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 6, 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 15 pF	1.0	1.8	3.5	ns
t_{PLHD}	Differential Propagation Delay Low to High	V_{ID} = 200 mV	1.0	1.7	3.5	ns
t_{SKD1}	Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$ (Note 8)	(*Figure 1* and *Figure 2*)	0	100	400	ps
t_{SKD3}	Differential Part to Part Skew (Note 9)		0	0.3	1.0	ns
t_{SKD4}	Differential Part to Part Skew (Note 10)		0	0.4	1.5	ns
t_{TLH}	Rise Time			350	800	ps
t_{THL}	Fall Time			175	800	ps
f_{MAX}	Maximum Operating Frequency (Note 12)		200	250		MHz

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified (such as V_{ID}).

Note 3: All typicals are given for: V_{DD} = +3.3V and T_A = +25˚C.

Note 4: ESD Ratings:

DS90LV012A:

- HBM (1.5 kΩ, 100 pF) ≥ 2kV
- EIAJ (0Ω, 200 pF) ≥ 900V
- CDM ≥ 2000V
- IEC direct (330Ω, 150 pF) ≥ 5kV

DS90LT012A:

- HBM (1.5 kΩ, 100 pF) ≥ 2kV
- EIAJ (0Ω, 200 pF) ≥ 700V
- CDM ≥ 2000V
- IEC direct (330Ω, 150 pF) ≥ 7kV

Note 5: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.

Note 6: C_L includes probe and jig capacitance.

Note 7: Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r and t_f (0% to 100%) ≤ 3 ns for IN±.

Note 8: t_{SKD1} is the magnitude difference in differential propagation delay time between the positive-going-edge and the negative-going-edge of the same channel.

Note 9: t_{SKD3}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{DD} and within 5˚C of each other within the operating temperature range.

Note 10: t_{SKD4}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over the recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.

Note 11: V_{DD} is always higher than IN+ and IN− voltage. IN+ and IN− are allowed to have voltage range −0.05V to +2.35V when V_{DD} = 2.7V and $|V_{ID}|$ / 2 to V_{DD} − 0.3V when V_{DD} = 3.0V to 3.6V. V_{ID} is not allowed to be greater than 100 mV when V_{CM} = 0.05V to 2.35V when V_{DD} = 2.7V or when V_{CM} = $|V_{ID}|$ / 2 to V_{DD} − 0.3V when V_{DD} = 3.0V to 3.6V.

Note 12: f_{MAX} generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, differential (1.05V to 1.35 peak to peak). Output criteria: 60%/40% duty cycle, V_{OL} (max 0.4V), V_{OH} (min 2.4V), load = 15 pF (stray plus probes). The parameter is guaranteed by design. The limit is based on the statistical analysis of the device over the PVT range by the transition times (t_{TLH} and t_{THL}).

Parameter Measurement Information

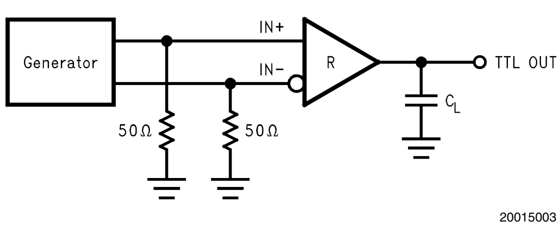


FIGURE 1. Receiver Propagation Delay and Transition Time Test Circuit

Parameter Measurement Information (Continued)

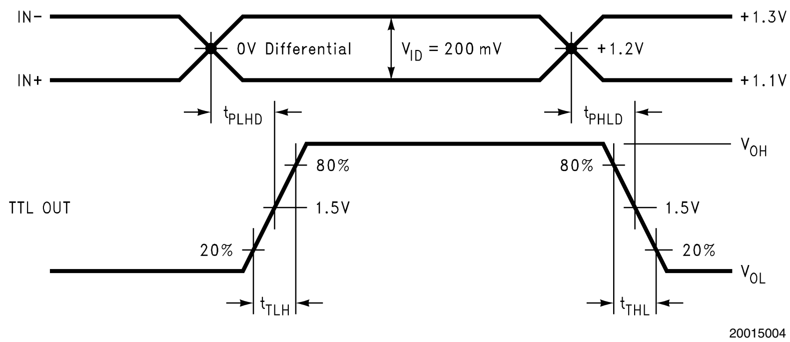


FIGURE 2. Receiver Propagation Delay and Transition Time Waveforms

Typical Application

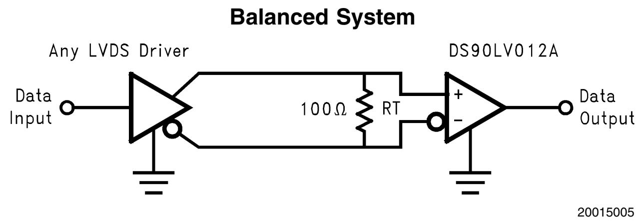


FIGURE 3. Point-to-Point Application (DS90LV012A)

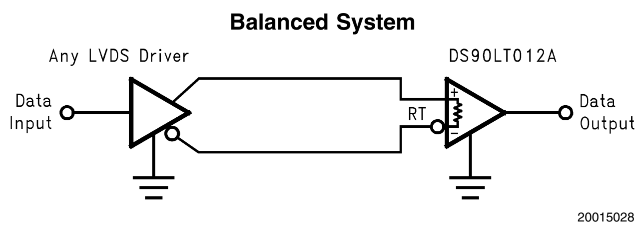


FIGURE 4. Point-to-Point Application (DS90LT012A)

Applications Information

General application guidelines and hints for LVDS drivers and receivers may be found in the following application notes: LVDS Owner's Manual (lit #550062-002), AN-808, AN-977, AN-971, AN-916, AN-805, AN-903.

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in *Figure 3*. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90LV012A and DS90LT012A differential line receivers are capable of detecting signals as low as 100 mV, over a ±1V common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift ±1V around this center point. The ±1V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. The AC parameters of both receiver input pins are optimized for a recommended operating input voltage range of 0V to +2.4V (measured from each pin to ground). The device will operate for receiver input voltages up to V_{DD}, but exceeding V_{DD} will turn on the ESD protection circuitry which will clamp the bus voltages.

Applications Information (Continued)

Power Decoupling Recommendations:

Bypass capacitors must be used on power pins. Use high frequency ceramic (surface mount is recommended) 0.1µF and 0.001µF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10µF (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board between the supply and ground.

PC Board considerations:

Use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL signals may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

For PC board considerations for the LLP package, please refer to application note AN-1187 “Leadless Leadframe Package.” It is important to note that to optimize signal integrity (minimize jitter and noise coupling), the LLP thermal land pad, which is a metal (normally copper) rectangular region located under the package, should be attached to ground and match the dimensions of the exposed pad on the PCB (1:1 ratio).

Differential Traces:

Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10mm long). This will help eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result! (Note that the velocity of propagation, $v = c/E_r$ where c (the speed of light) = 0.2997mm/ps or 0.0118 in/ps). Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90˚ turns (these cause impedance discontinuities). Use arcs or 45˚ bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

Termination:

DS90LV012A:

Use a termination resistor which best matches the differential impedance or your transmission line. The resistor should be between 90Ω and 130Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice.

Surface mount 1% - 2% resistors are the best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be < 10mm (12mm MAX).

DS90LT012A:

The DS90LT012A integrates the terminating resistor for point-to-point applications. The resistor value will be between 90Ω and 133Ω.

Threshold:

The LVDS Standard (ANSI/TIA/EIA-644-A) specifies a maximum threshold of ±100mV for the LVDS receiver. The DS90LV012A and DS90LT012A support an enhanced threshold region of −100mV to 0V. This is useful for fail-safe biasing. The threshold region is shown in the Voltage Transfer Curve (VTC) in *Figure 5*. The typical DS90LV012A or DS90LT012A LVDS receiver switches at about −30mV. Note that with V_{ID} = 0V, the output will be in a HIGH state. With an external fail-safe bias of +25mV applied, the typical differential noise margin is now the difference from the switch point to the bias point. In the example below, this would be 55mV of Differential Noise Margin (+25mV − (−30mV)). With the enhanced threshold region of −100mV to 0V, this small external fail-safe biasing of +25mV (with respect to 0V) gives a DNM of a comfortable 55mV. With the standard threshold region of ±100mV, the external fail-safe biasing would need to be +25mV with respect to +100mV or +125mV, giving a DNM of 155mV which is stronger fail-safe biasing than is necessary for the DS90LV012A or DS90LT012A. If more DNM is required, then a stronger fail-safe bias point can be set by changing resistor values.

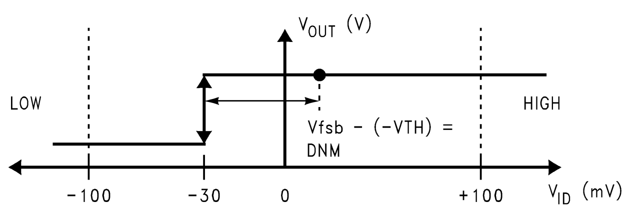


FIGURE 5. VTC of the DS90LV012A and DS90LT012A LVDS Receivers

Applications Information (Continued)

Fail-Safe Feature:

The LVDS receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

1. **Open Input Pins.** The DS90LV012A and DS90LT012A are single receiver devices. Do not tie the receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will guarantee a HIGH, stable output state for open inputs.
2. **Terminated Input.** If the driver is disconnected (cable unplugged), or if the driver is in a power-off condition, the receiver output will again be in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable will offer better balance than flat ribbon cable.
3. **Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output will remain in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

External lower value pull up and pull down resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry.

The DS90LV012A and DS90LT012A are compliant to the original ANSI EIA/TIA-644 specification and is also compliant to the new ANSI EIA/TIA-644-A specification with the exception the newly added ΔI_{IN} specification. Due to the internal fail-safe circuitry, ΔI_{IN} cannot meet the 6μA maximum specified. This exception will not be relevant unless more than 10 receivers are used.

Additional information on fail-safe biasing of LVDS devices may be found in AN-1194.

Probing LVDS Transmission Lines:

Always use high impedance (> 100kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will give deceiving results.

Cables and Connectors, General Comments:

When choosing cable and connectors for LVDS it is important to remember:

Use controlled impedance media. The cables and connectors you use should have a matched differential impedance of about 100Ω. They should not introduce major impedance discontinuities.

Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation a common-mode (not differential mode) noise which is rejected by the receiver.

For cable distances < 0.5M, most cables can be made to work effectively. For distances 0.5M ≤ d ≤ 10M, CAT 3 (category 3) twisted pair cable works well, is readily available and relatively inexpensive.

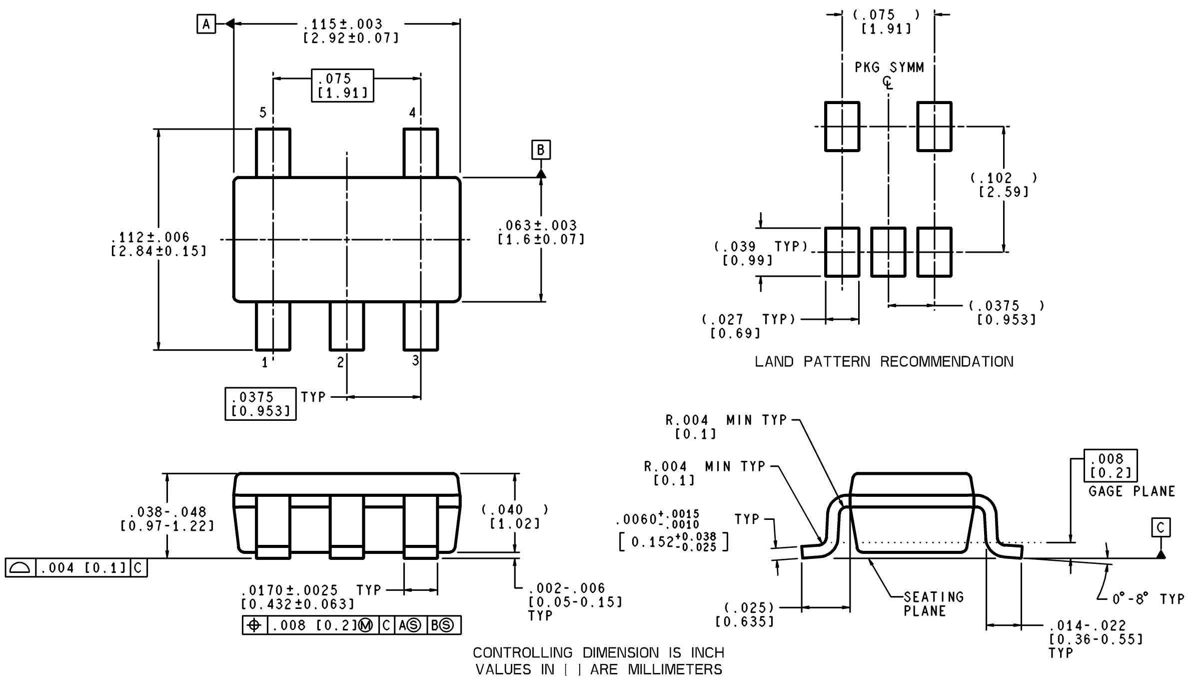
Pin Descriptions

Package Pin Number		Pin Name	Description
SOT23	LLP		
4	1	IN−	Inverting receiver input pin
3	3	IN+	Non-inverting receiver input pin
5	8	TTL OUT	Receiver output pin
1	6	V_{DD}	Power supply pin, +3.3V ± 0.3V
2	2, 7	GND	Ground pin
	4, 5	NC	No connect

Ordering Information

Operating Temperature	Package Type/ Number	Order Numbers
−40˚C to +85˚C	MF05A	DS90LV012ATMF, DS90LT012ATMF
	LDA08A	DS90LV012ATLD, DS90LT012ATLD

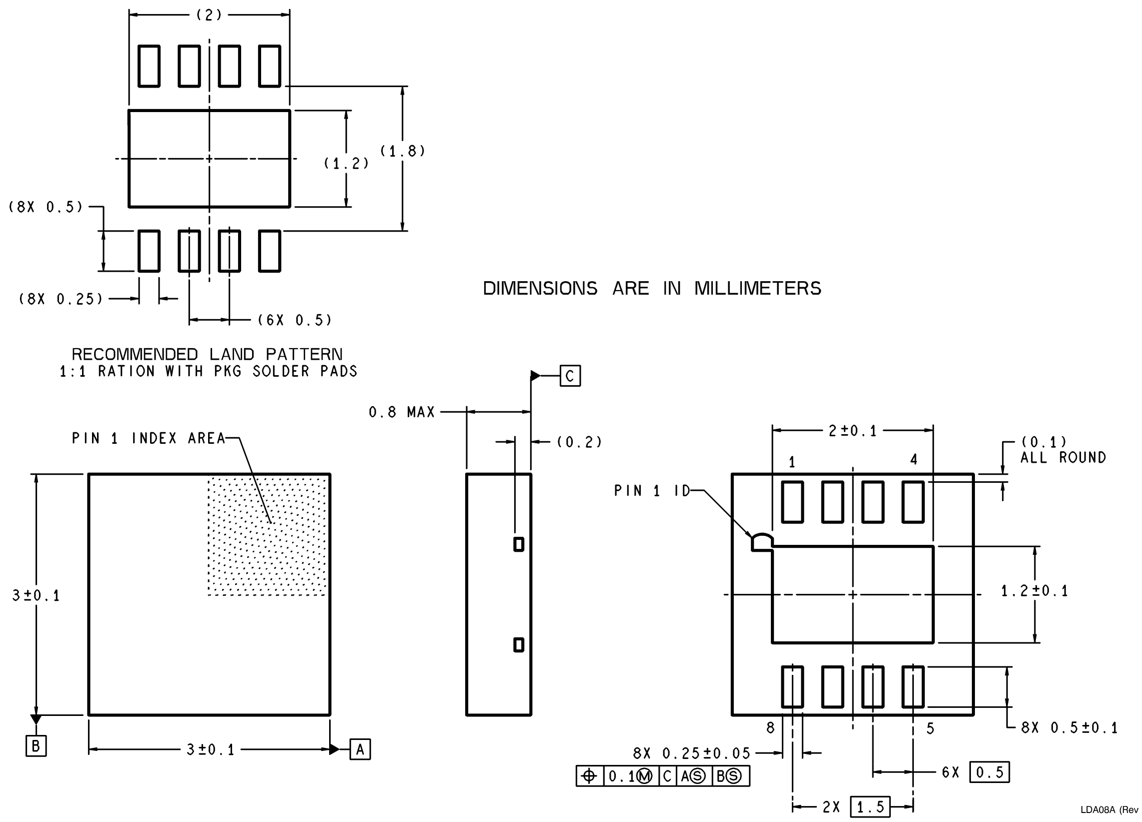
Physical Dimensions inches (millimeters) unless otherwise noted



MF05A (Rev A)

5-Lead SOT23, JEDEC MO-178, 1.6mm
Order Number DS90LV012ATMF, DS90LT012ATMF
NS Package Number MF05A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LLP-8, 3mm x 3mm Body
Order Number DS90LV012ATLD, DS90LT012ATLD
NS Package Number LDA08A

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