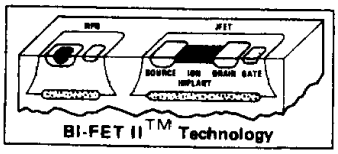
National Semiconductor



LF401/LF401A Precision Fast Settling JFET Input Operational Amplifier

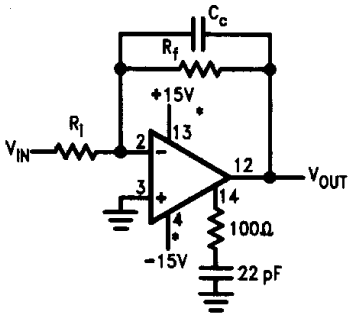
General Description

The LF401A is a fast settling (guaranteed under 400 ns to 0.01% for a 10V output step) BI-FET operational amplifier. The input offset voltage of the LF401A is guaranteed less than 200 μV maximum at 25°C. The LF401 also features 16 MHz bandwidth, 70 V/μs inverting slew rate and adjustable short circuit current limit, enabling it to drive 600Ω loads easily.

Applications

- DAC output amplifiers
- Fast buffers
- High speed ramp generators
- Sample-and-holds
- Fast integrators
- Piezoelectric transducer signal conditioners

Typical Connection

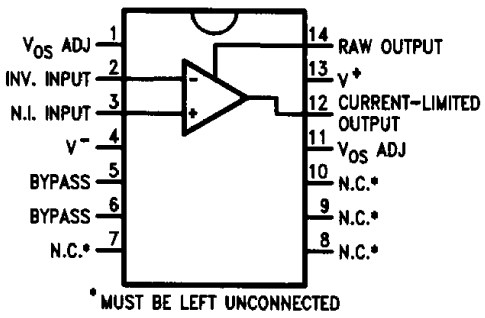


TL/H/8839-1

*See *Figure 2* for Power Supply Bypassing.

Connection Diagram

Dual-In-Line Package

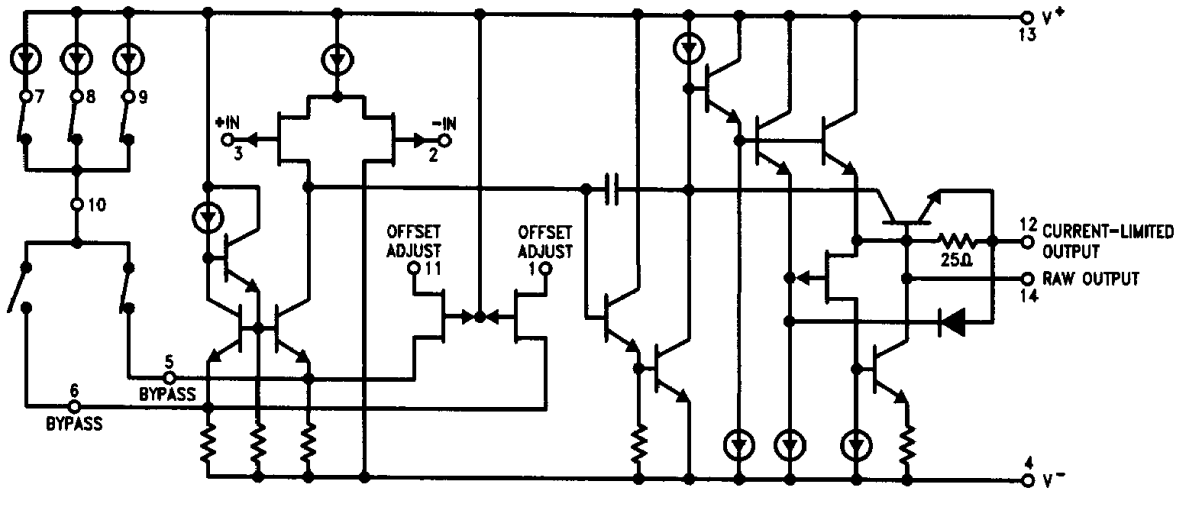


*MUST BE LEFT UNCONNECTED

TL/H/8839-2

Order Number LF401ACD or LF401CD
See NS Package Number D14E

Simplified Schematic



TL/H/8839-3

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	±18V
Differential Input Voltage	±32V
Input Voltage Range (Note 3)	±16V
Output Short Circuit Duration (Pin 12)	Continuous
Power Dissipation (Note 4) D package	500 mW
Junction Temperature (T_{JMAX})	115°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Susceptibility (Note 10)	500V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LF401ACD, LF401CD	$0°C \le T_A \le +70°C$
Positive Supply Voltage	+10V to +16V
Negative Supply Voltage	−10V to −16V
Total Supply Voltage ($V^+ - V^-$)	20V to 32V

AC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$ unless otherwise specified. **Tested Limits in Boldface apply for T_J = 25°C to 95°C. Design Limits in Boldface apply for $T_A = T_{MIN}$ to T_{MAX};** other Design Limits are for T_A = 25°C; all other limits for T_J = 25°C.

Symbol	Parameter	Conditions	LF401ACD			LF401CD			Unit
			Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
t_s	Maximum Settling Time to 0.01% to 0.10%	See *Figure 1*, $C_L \le 50$ pF See *Figure 1*, $C_L \le 50$ pF	335 200	400		335 200	500		ns ns
GBW	Minimum Gain Bandwidth Product	$A_V = +1$, $C_L = 10$ pF, f = 100 kHz	16	14		16	14		MHz
SR	Minimum Slew Rate	$A_V = +1$, $C_L = 10$ pF		27			27		V/μs
		$A_V = -1$, $C_L = 10$ pF	70			70			V/μs
ϕ	Minimum Phase Margin	$A_{VOL} = +1$, $C_L = 10$ pF	60			60			°
e_n	Input Noise Voltage	f = 1 KHz, Rs = 100Ω Broadband, Rs = 100Ω, 10 Hz to 10 kHz	23 2.3			23 2.3			nV/√Hz μV rms
i_n	Input Noise Current	f = 1 kHz Broadband 10 Hz to 10 kHz	0.01 2.0			0.01 2.0			pA/√Hz pA rms
THD	Total Harmonic Distortion (Max)	f = 1 kHz, Av = −1, R_L = 10k	0.002			0.002			%
CIN	Input Capacitance	Differential	7			7			pF

DC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$ unless otherwise specified. **Tested Limits in Boldface apply for T_J = 25°C to 95°C. Design Limits in Boldface apply for $T_A = T_{MIN}$ to T_{MAX};** other Design Limits are for T_A = 25°C; all other limits for T_J = 25°C.

Symbol	Parameter		Conditions	LF401ACD			LF401CD			Unit
				Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
V_{OS}	Maximum Input Offset Voltage (Note 9)		V_{CM} = 0V, R_S = 0, R_L = ∞ T_A = 25°C T_A = 70°C		±200 ±600			±500 ±1500		μV μV
I_{OS}	Maximum Input Offset Current		V_{CM} = 0V, (Note 5)		±100	±400 **±2.5**		±100	±400 **±2.5**	pA nA
I_B	Maximum Input Bias Current		V_{CM} = 0V, (Note 5)		200	**26**		200	**26**	pA nA
R_{IN}	Input Resistance		T_J = 25°C	10^{11}			10^{11}			Ω
V_{CM}	Input Common-Mode Voltage Range			+14/−12	±11		+14/−12	±11		V
A_{VOL}	Minimum Large Signal Voltage Gain	Using Pin 12 Using Pin 14	V_O = ±10V, R_L = 2 kΩ V_O = ±10V, R_L = 600Ω	300 300	100 100		300 300	100 100		V/mV V/mV
V_O	Minimum Output Voltage Swing	Using Pin 12 Using Pin 14	R_L = 2 kΩ R_L = 600Ω	±12.5 ±12	±12 ±11		±12.5 ±12	±12 ±11		V V
I_{SC}	Output Short Circuit Current	MIN Using Pin 12 MAX Using Pin 12 MIN Using Pin 14	Pulse Test		15 45 100			15 45 100		mA mA mA
R_O	Output Resistance	Using Pin 12 Using Pin 14	Open Loop, DC Open Loop, DC	75 50			75 50			Ω Ω
CMRR	Minimum DC Common Mode Rejection Ratio		−11V ≤ V_{IN} ≤ +11V	100	90		100	80		dB
PSRR	Minimum DC Power Supply Rejection Ratio		+10V ≤ V^+ < +15V, −15V ≤ V^- < −10V, V_{CM} = 0V	100	90		100	80		dB
I_S	Maximum Supply Current		V_O = 0V, R_L = ∞	9	12		9	12		mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are with respect to ground.

Note 3: Unless otherwise specified, the Absolute Maximum Negative Input Voltage is equal to the negative power supply voltage.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or 500 mW, whichever is less. θ_{JA} for the LF401D is typically 87°C/W.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature T_J. Due to limited production test time, input bias currents are measured at T_J = 25°C. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation P_D. Use of a heat sink is recommended when input bias current must be minimized.

Note 6: Typicals represent the most likely parametric norm.

Note 7: Guaranteed to National's AOQL (Average Outgoing Quality Level).

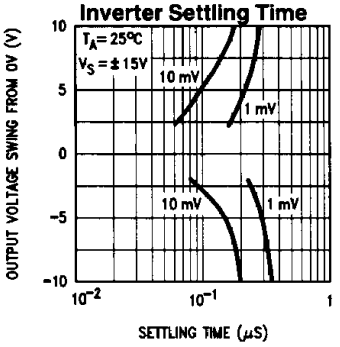
Note 8: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 9: Tested and correlated to a 10 minute warm up period.

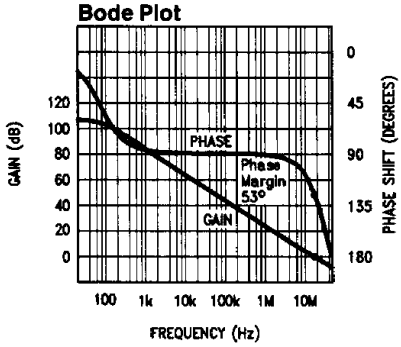
Note 10: Human body model, 100 pF discharged through a 1500Ω resistor.

Typical Performance Characteristics

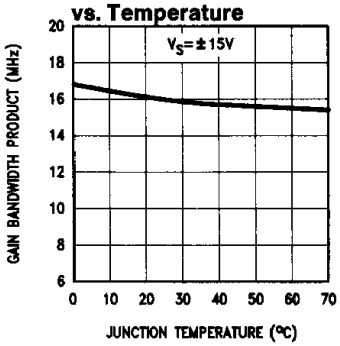
Inverter Settling Time



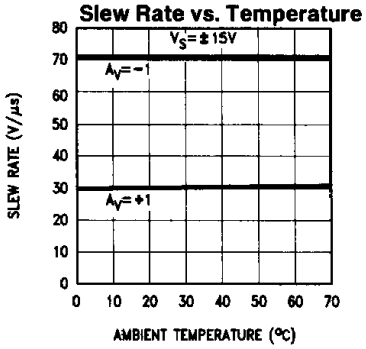
Bode Plot



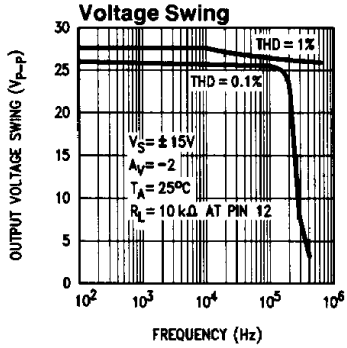
Gain Bandwidth vs. Temperature



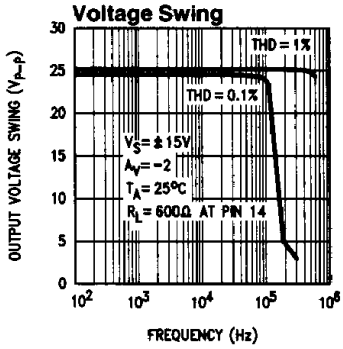
Slew Rate vs. Temperature



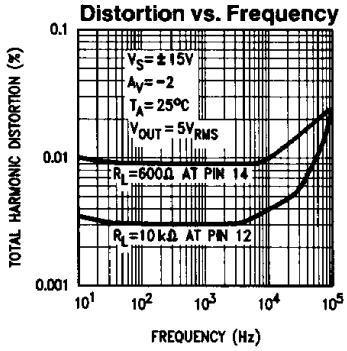
Undistorted Output Voltage Swing



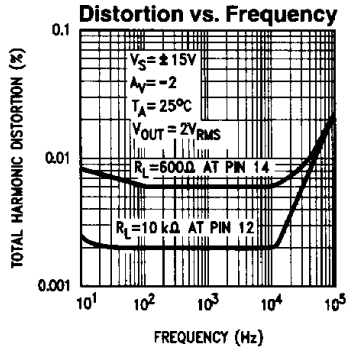
Undistorted Output Voltage Swing



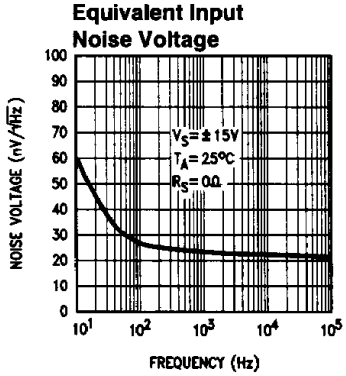
Distortion vs. Frequency



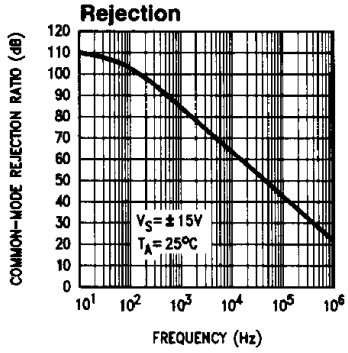
Distortion vs. Frequency



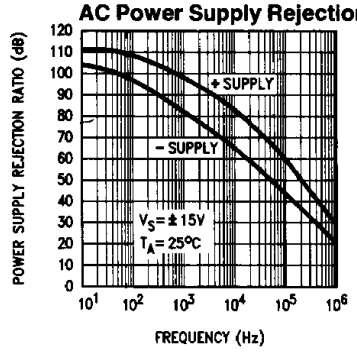
Equivalent Input Noise Voltage



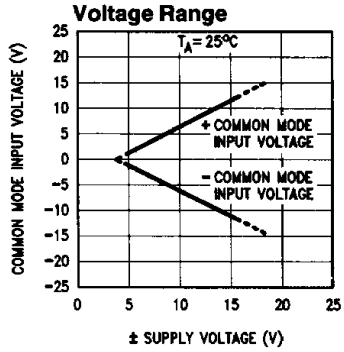
AC Common-Mode Rejection



AC Power Supply Rejection



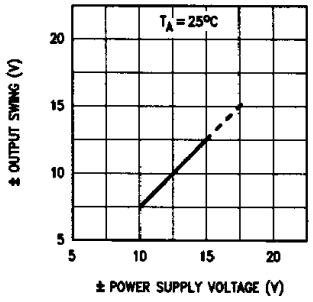
Common-Mode Input Voltage Range



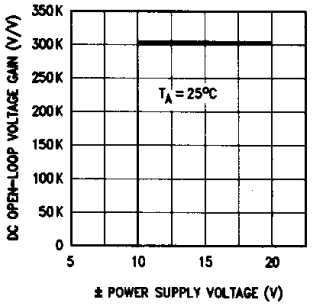
TL/H/8839–4

Typical Performance Characteristics (Continued)

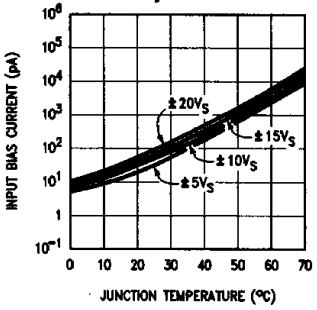
Output Voltage Swing vs. Supply Voltage



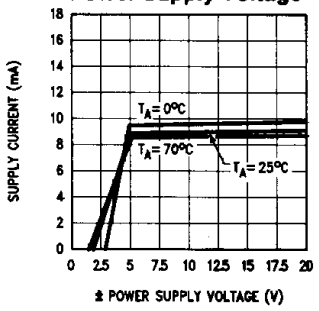
DC Gain vs. Supply Voltage



Input Bias Current vs. Temperature

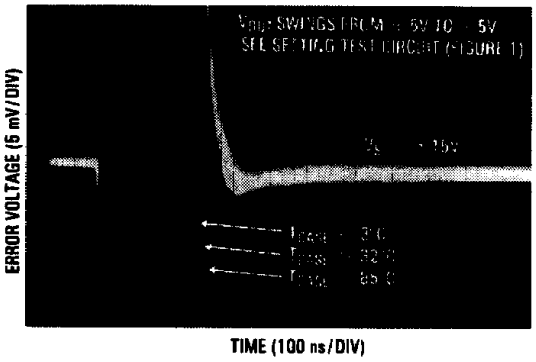


Power Supply Current vs. Power Supply Voltage



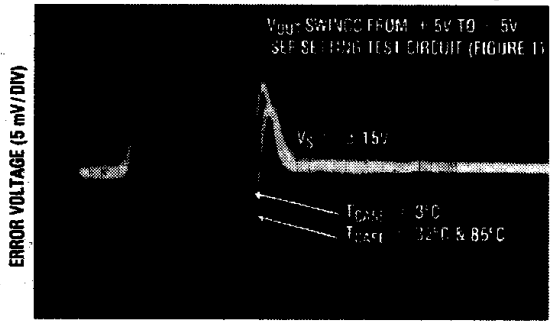
TL/H/8839-5

Settling Time—Positive Output Swing



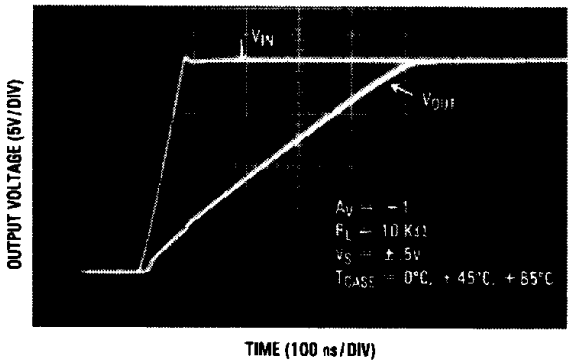
TL/H/8839-6

Settling Time—Negative Output Swing



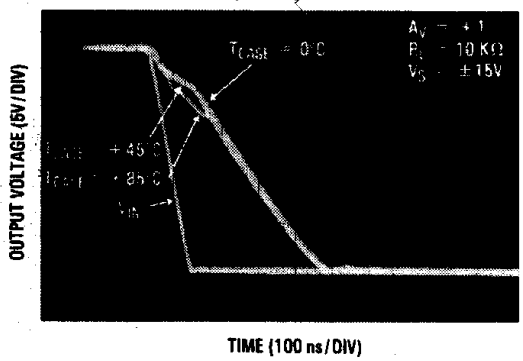
TL/H/8839-7

Step Response



TL/H/8839-22

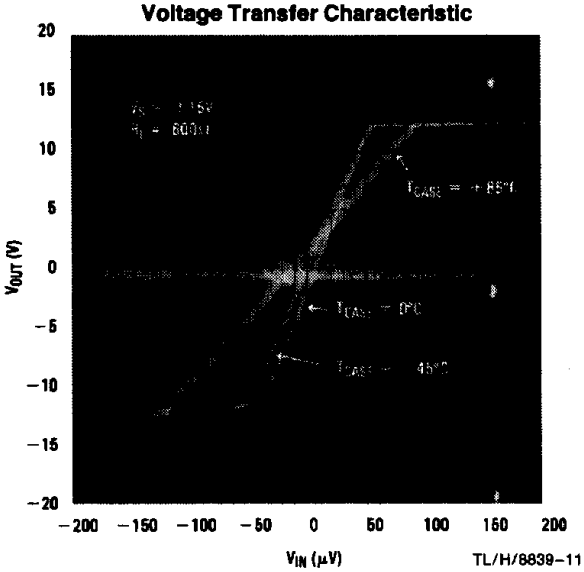
Step Response



TL/H/8839-9

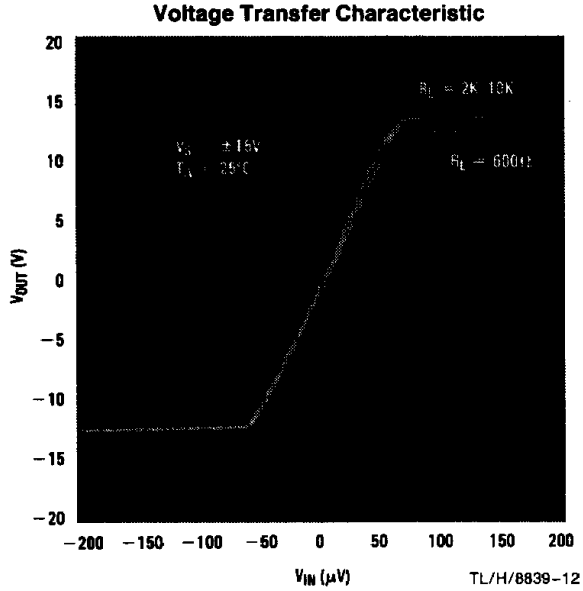
Typical Performance Characteristics (Continued)

Voltage Transfer Characteristic



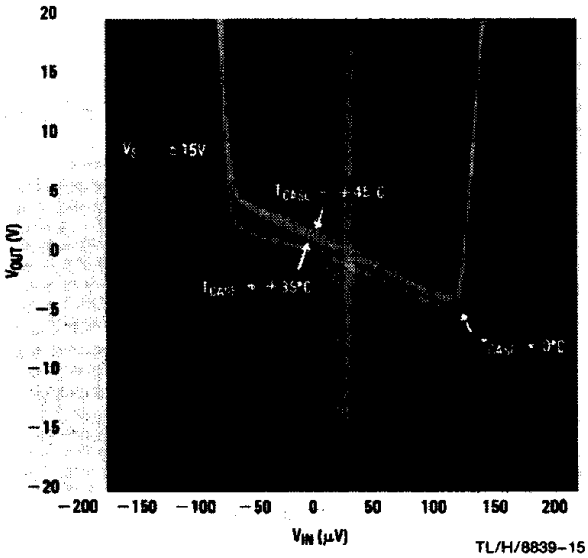
TL/H/8839–11

Voltage Transfer Characteristic



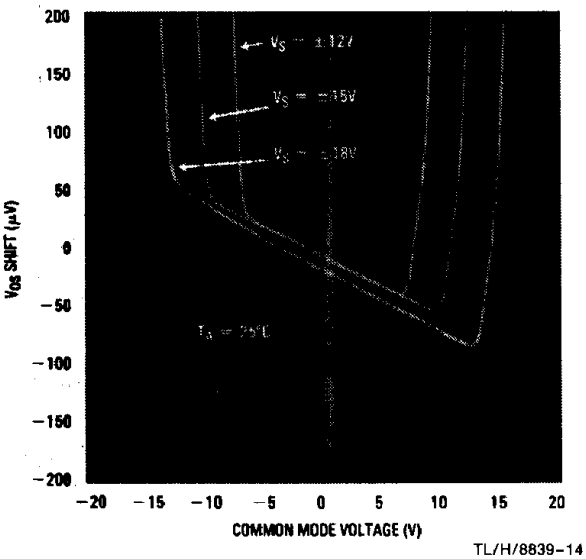
TL/H/8839–12

Common Mode Voltage Transfer Characteristic



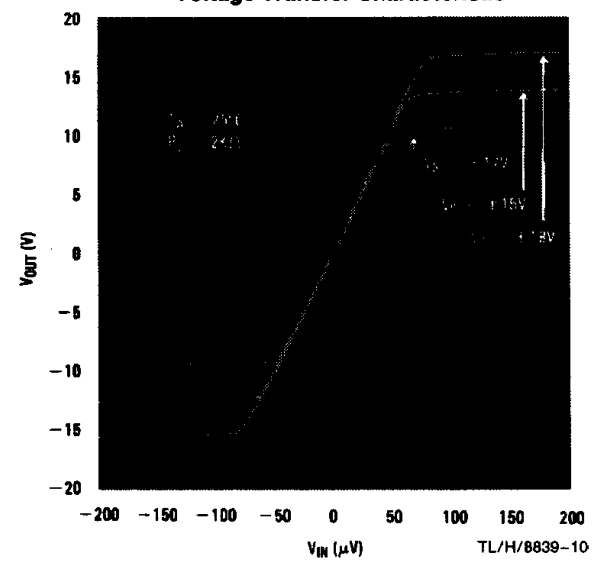
TL/H/8839–15

Common Mode Voltage Transfer Characteristic



TL/H/8839–14

Voltage Transfer Characteristic



TL/H/8839–10

Application Hints

The LF401 is a high-speed, low offset, low input bias current Bi-FET operational amplifier capable of settling to 0.01% of a 10V output swing in less than 400 ns. Input offset voltage at room temperature is less than 200 μV for LF401A. The rugged JFET inputs allow differential input voltages as high as 32V without a large increase in input current. However, the inputs should never be driven to voltages lower than the negative supply, as this can result in input currents large enough to damage the device. To prevent this from occurring when power is first applied, always turn the positive and negative power supplies on simultaneously, or turn the negative supply on first.

Exceeding the positive common-mode input range will not damage the device as long as the Absolute Maximum ratings are not violated, but if both inputs exceed the positive common-mode range the output voltage will go high. Latching will not occur, however, and when the offending signal is removed the LF401 will recover quickly.

The nominal power supply voltage is ±15V, but the LF401 will operate satisfactorily from ±10V to ±16V. The LF401 is functional down to ±5V, but performance will be degraded at low supply voltages. (See Typical Performance curves.)

SETTLING TIME CONSIDERATIONS

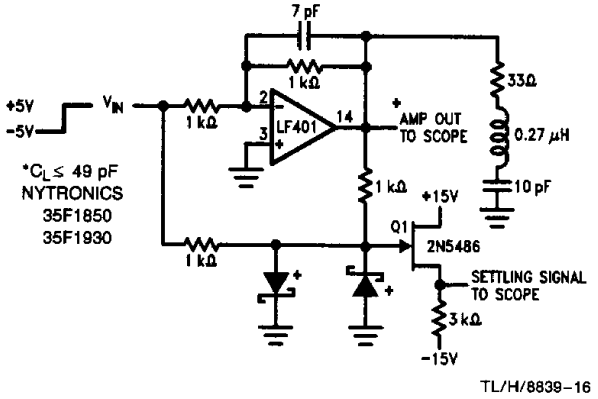
The settling performance of any fast operational amplifier is highly dependent on the external components and circuit board layout. Capacitance between the amplifier summing junction and ground affects the closed-loop transfer function and should be minimized. The compensation capacitor C_C between the output and the inverting input should be carefully chosen to counteract the effect of the input capacitance. Since input capacitance is made up of several stray capacitances that are difficult to predict, the compensation capacitor will generally have to be determined empirically for best settling time. A good starting point is around 10 pF for $A_V = -1$.

Settling time may be verified using a circuit similar to the one in *Figure 1*. The LF401 is connected for inverting operation, and the output voltage is summed with the input voltage step. When the LF401's output voltage is equal to the input voltage, the voltage on the gate of Q1 will be zero. Any voltage appearing at this point will represent an error. The FET source follower output is observed on an oscilloscope, and the settling time is equal to the time required for the error signal displayed on the oscilloscope to decay to less than one-half the necessary accuracy (see oscilloscope photos of "Settling Time — Positive Output Swing" and "Settling Time — Negative Output Swing"). For a 10V input signal, settling time to 0.01% (1 mV) will occur when the displayed error is less than 1/2 mV. Since settling time is strongly dependent on slew rate, settling will be faster for smaller signal swings. The LF401's inverting slew rate is faster than its non-inverting slew rate, so settling will be faster for inverting applications, as well.

It is important to note that the oscilloscope input amplifier will be overdriven during a settling time measurement, so the oscilloscope must be capable of recovering from overdrive very quickly. Very few oscilloscopes are suitable for this sort of measurement. The signal generator used for settling time testing must be able to drive 50Ω with a very clean ±5V square wave. For more information on measuring settling time, see Application Note AN-428.

OUTPUT COMPENSATION

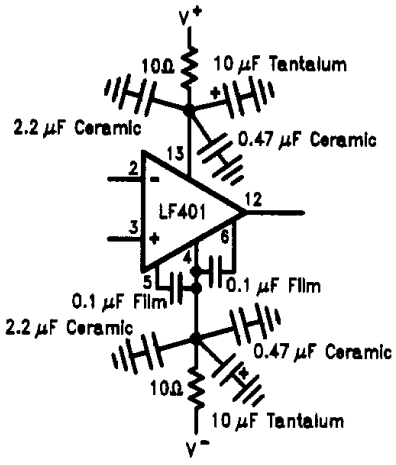
When operating at very low temperatures, a compensation network should be connected to the LF401's "raw" output pin. The 100Ω/22 pF network shown on the first page of this data sheet should be connected to pin 14 in applications where the junction temperature might go as low as 25°C (roughly 0°C ambient when the LF401 is "warmed up"). In applications where the device will be operating with a junction temperature down to 0°C, the output RLC network in *Figure 1* should be used. This network will provide a small (about 20 ns) improvement in settling time at higher temperatures, as well.



TL/H/8839–16

+H.P. 5082-2810

FIGURE 1. Simplified Settling Time Test Circuit (See Text)



TL/H/8839–17

FIGURE 2. Power Supply Bypassing (See Text)

SUPPLY BYPASSING

Power supply bypassing is extremely important for good high-speed performance. Ideally, multiple bypass capacitors as in *Figure 2* should be used. A 10 μF tanatalum, a 2.2 μF

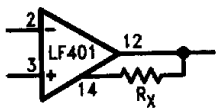
Application Hints (Continued)

ceramic, and a 0.47 μF ceramic work well. All bypass capacitor leads should be very short. For best results, the ground leads of the capacitors should be separated to reduce the inductance to ground. A ground plane layout approach will give the best results. For simplicity, bypass capacitors have been omitted from some of the schematics in this data sheet, but they should always be used.

Pins 5 through 10 are used to trim the LF401's input offset voltage during the manufacturing process. Always leave pins 7 through 10 open, as signals applied to these pins will affect the amplifier output and can permanently degrade V_{OS}. For fastest settling time to 0.01%, pins 5 and 6 should be bypassed to pin 4 with 0.1 μF capacitors; otherwise, the LF401 may take an additional 600 ns to settle. The bypass capacitors should be low-leakage film types; otherwise the offset voltage can be increased. Settling time to 0.1% will be unaffected by bypassing these pins, so they may be left unconnected in applications requiring less precision.

OUTPUT DRIVE AND CURRENT LIMIT

The LF401 can drive heavier resistive loads than most operational amplifiers. The output at pin 12 is internally current-limited when the voltage drop across the 25Ω output resistor reaches about 0.55V (I_{out} = 22 mA). When more output current is needed, pin 14 provides a means of increasing the maximum output current up to about 100 mA. A resistor may be connected from pin 12 to pin 14, paralleling the internal sense resistor and increasing the current limit threshold (*Figure 3*). Pins 12 and 14 may be shorted together to completely bypass the current limiting circuit. To avoid damaging the LF401, observe the power dissipation limitations mentioned in the Absolute Maximum Ratings and in Note 4.



TL/H/8839–18

FIGURE 3. Increasing the current limit using pin 14. Current limit is now determined by R_X in parallel with the internal 25Ω sense resistor.

The effective load impedance (including feedback resistance) should be kept above 500Ω for fastest settling. Load capacitance should also be minimized if good settling time is to be optimized. Large feedback resistors will make the circuit more susceptible to stray capacitance, so in high-speed applications keep the feedback resistors in the 1k to 2 kΩ range wherever practical. Avoid the use of inductive feedback resistors (some wirewounds for example) as these will degrade settling time.

V_{OS} ADJUSTMENT

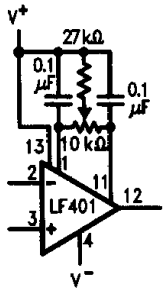
Offset voltage can be nulled using a 27k resistor and a 10k potentiometer connected to pins 1 and 11 as shown in *Figure 4a*. Bypassing the V_{OS} adjust pins with 0.1 μF capacitors will help to avoid noise pickup. When not used for offset adjustment, pins 1 and 11 can often be left open, but to minimize the possibility of noise pickup the unused V_{OS} trim pins should be connected to ground or V^-.

In very critical applications where a manual adjustment is impractical, the LMC669 Auto Zero circuit may be used to reduce the effective input offset voltage to around 5 μV as in *Figure 4b*. The LF401 will perform better than slower amplifiers in an auto zero loop, because its fast settling capability keeps its summing node voltage more stable. Therefore, the LMC669 is able to more accurately sample the summing node voltage before making an offset correction.

INPUT BIAS CURRENT

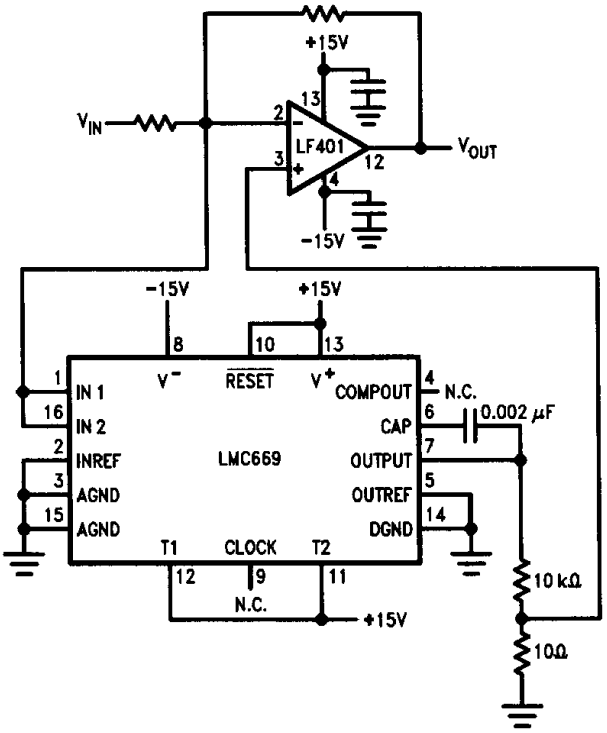
The JFET input stage of the LF401 ensures low input bias current (200 pA maximum) when the die is at room temperature, but this current approximately doubles for every 10°C increase in temperature. In applications that demand the lowest possible input bias current, a heat sink should be used with the LF401. "Slide on" heat sinks such as the AAVID 5602B can reduce the junction temperature by about 10°C.

Application Hints (Continued)



TL/H/8839–19

FIGURE 4a. V_{OS} Adjust Circuit

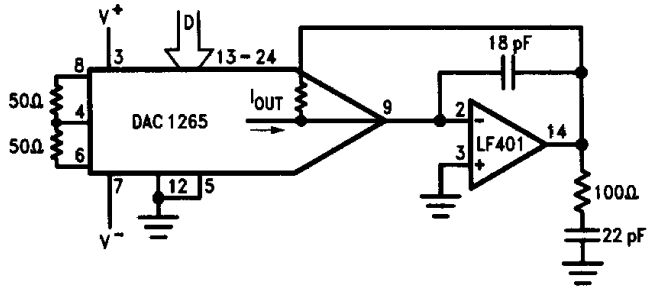


TL/H/8839–20

FIGURE 4b. Automatic Offset Adjustment Using LMC669

Typical Applications

High-Speed DAC with Voltage Output
(See *Figure 2* for Recommended Bypass Components)



TL/H/8839–21