National Semiconductor

LH4860
Super Fast 12-Bit Track-Hold Amplifier

General Description

The LH4860 is an extremely fast high resolution Sample-Hold (track-and-hold) amplifier. It guarantees acquisition time and sample-to-hold settling time to ±0.01%. The LH4860 will acquire a full 10V signal to ±0.01% full scale (or ±1 mV) in less than 200 ns. The bandwidth of the tracking amplifier is 16 MHz. In the track mode, offset error is typically ±0.5 mV and gain error is typically ±0.05%. The LH4860 is precisely laser trimmed for pedestal compensation. The "Hold" capacitor is internal for ease of use. Also, the bypassing power supply capacitors are inside the package.

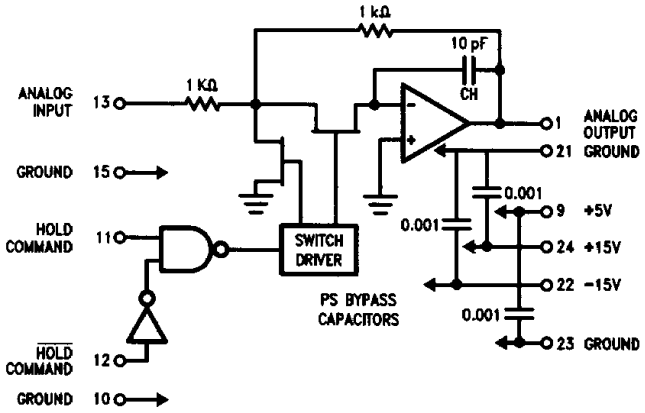
Features

- 200 ns max acquisition time 10V step to ±0.01% FS
- 100 ns max sample-to-hold settling time
- ±50 ps aperture jitter
- 74 dB feedthrough attenuation
- TTL compatible
- Direct replacement for HTC-0300, 4860, and HS9720

Applications

- Transient recorders
- Fast fourier analysis
- High speed DAS's
- High speed DDS's
- Analog delay and storage

Block and Connection Diagrams



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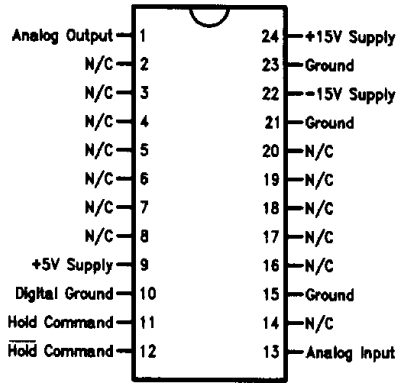

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Top View

Dual-In-Line Metal Package (D)
Order Number LH4860D or LH4860CD
See NS Package Number D24I

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_S^+ and V_S^-)	±18V
Logic Supply Voltage (V_D)	+7V
Analog Input Voltage	$\pm V_S$
Digital Input Voltage	−0.5V to +5.5V
Output Current (Note 1)	±65 mA
Output Short Circuit Duration	Continuous
Operating Temperature Range	
LH4860C	−25°C to +85°C
LH4860	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation (P_D) (See Graph)	2.4W
ESD (Note 6)	TBD

DC Electrical Characteristics V_S = ±15V and +5V, T_A = +25°C, unless otherwise noted (Note 1)

Symbol	Parameter	Conditions	LH4860C/LH4860			Units (Max Unless Otherwise Stated)
			Typ	Tested Limit (Note 8)	Design Limit (Note 9)	
	Input/Output Voltage Range		±11.5	±10.25		V (Min)
	Input Impedance		1			kΩ
	Output Current	(Note 1)		40		mA
	Output Impedance		0.1			Ω
	Maximum Capacitive Load		150			pF
	Logic High "1"	(Note 2)		2.0		V (Min)
				5.0		V
	Logic Low "0"	(Note 2)		0		V (Min)
				0.8		V
	Digital Input Loading		1			TTL Load
	Gain		−1.00			V/V
	Gain Accuracy		±0.05	±0.2		%
	Gain Linearity Error (Note 4)		±0.003	±0.01		% FS
	Offset Voltage	Sample Mode	±0.5	±5		mV
	Hold Step	Pedestal *Figure 1*	±2.5	±20		mV
	Gain Drift	(Note 7)	±0.5		**±5**	ppm of FSR/°C
	Offset Drift	Sample Mode (Note 4)	±3		**±15**	ppm of FSR/°C

AC Electrical Characteristics $V_S = \pm 15V$ and $+5V$, $T_A = +25°C$, unless otherwise noted (Note 1)

Symbol	Parameter	Conditions	LH4860C/LH4860			Units (Max Unless Otherwise Stated)
			Typ	Tested Limit (Note 8)	Design Limit (Note 9)	
	Acquisition Time (Notes 4, 5)	10V Step to ±0.01% FS (±1 mV)	150	200		ns
		10V Step to ±0.1% FS (±10 mV)	100	170		ns
		10V Step to ±1% FS (±100 mV)	90			ns
		1V Step to ±1% FS (±100 mV)	75			ns
	Settling Time Sample to Hold (Note 4)	to ±0.01% FS (1 mV)	60	100		ns
		to ±0.1% FS (10 mV)	40			ns
	Sample to Hold Transient		180			mV_{P-P}
	Aperture Delay Time		6			ns
	Aperture Jitter		±50			ps
	Output Slew Rate		300			V/μs
	Small Signal Bandwidth (−3 dB)		16			MHz
	Droop Rate		±0.5	±5		μV/μs
		+85°C	±55			μV/μs
		+125°C	±1.2			mV/μs
	Feedthrough	2.5 MHz, 20 V_{P-P} Input	74			dB
PSRR	Power Supply Rejection Ratio		±0.5			mV/V
	Quiescent Current Drain	+15V Supply	21	25		mA
		−15V Supply	−22	−25		mA
		+5V Supply	17	25		mA
	Power Consumption		730	875		mW

Note 1: The LH4860 output is current limited at approximately ±65 mA and the unit can withstand a sustained short-to-ground. For normal operation, load current should not exceed ±40 mA.

Note 2: See Application Information for use of Hold and $\overline{\text{Hold}}$ inputs.

Note 3: The Hold Command inputs appear as one TTL load and are defined as sinking 40 μA with logic "1" applied and sourcing 1.6 mA with logic "0" applied.

Note 4: FS means "Full Scale" and is equivalent to 10V. FSR means "Full Scale Range" and is equivalent to 20V. For a 12-bit system, 1 LSB = 0.024% FS.

Note 5: Acquisition time is tested with no load.

Note 6: The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Note 7: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range of LH4860C is −25°C to +85°C, and LH4860 is −55°C to +125°C.

Note 8: Tested limits are guaranteed and 100% production tested.

Note 9: Design limits are guaranteed (but not production tested) over the indicated temperature or temperature range. These limits are not used to calculate outgoing quality level.

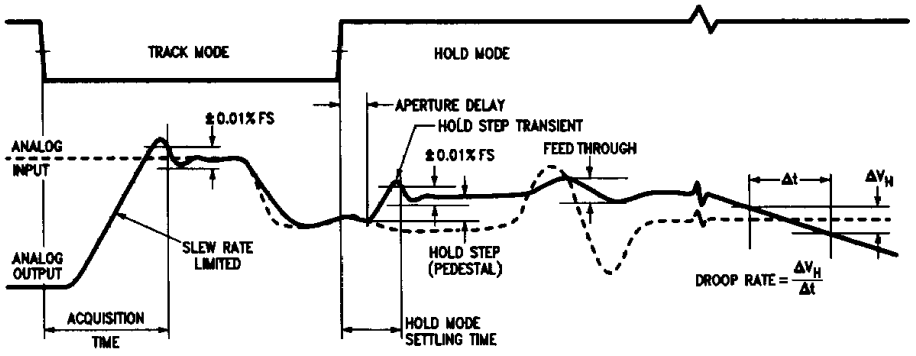
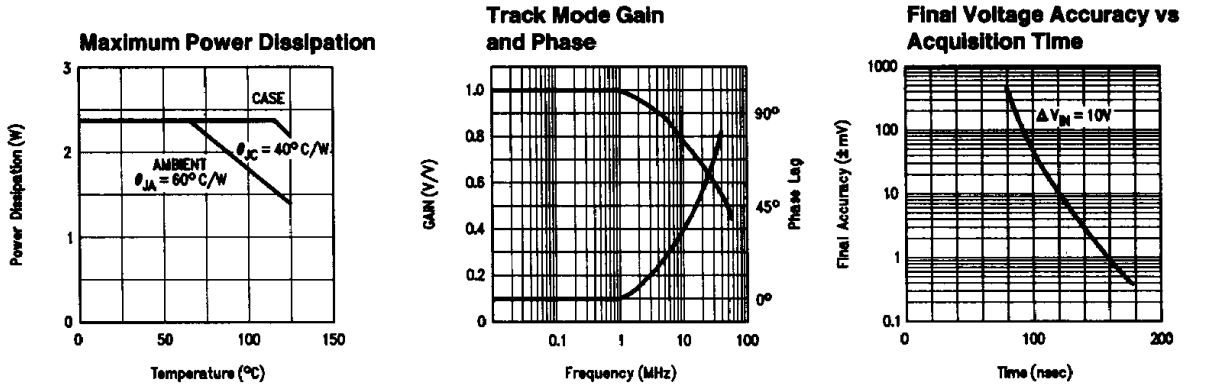


FIGURE 1. Timing Diagram

Typical Performance Characteristics



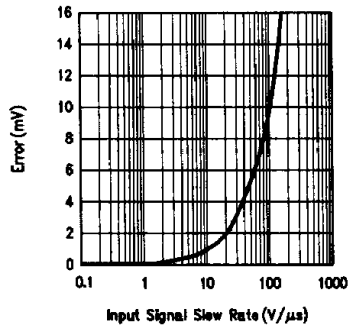


FIGURE 2. Accuracy Error Due to a ±50 ps Aperture Jitter at 10V Full Scale

Application Information

LAYOUT

The LH4860 is constructed in a way that with proper care in the layout it will meet its specifications without additional external components.

A large analog ground plane will provide uniform ground potential to the four ground pins (Pin 10, 15, 21 and 23). These pins should be connected to the ground plane with minimum lead length. Any difference in ground potential, due to ground current, will degrade the performance of the device.

The analog and digital grounds of the LH4860 should be connected together close to the device. The +5V digital logic supply needs to be well bypassed. Although both +5V and ±15V are internally decoupled with 0.001 μF, in critical applications, additional bypass capacitors are recommended (0.1 μF–1 μF tantalum).

LOGIC COMMANDS

A TTL logic "0" on Pin 11 (or a logic "1" on Pin 12) will put the LH4860 into the sample (track) mode. In this mode, the device acts as an inverting unity gain amplifier, and its output will track the input.

A logic "1" on Pin 11 and logic "0" on Pin 12 will put the device into the hold mode, where the output will be held constant at the level present when the command was given.

Application Information (Continued)

Unused logic pins need to be tied to a fixed logic level. When Pin 11 is used, then Pin 12 must be tied to ground; when Pin 12 is used as logic input, Pin 11 is to be tied to +5V through 1 kΩ.

Each Pin 11 or 12 represents one TTL load to the drive circuit.

Pin 11 (Hold)	Pin 12 ($\overline{\text{Hold}}$)	State
0	0	Track
0	1	Track
1	0	Hold
1	1	Track

In the tracking mode, the Track-Hold Amplifier operates as an inverting amplifier with unity gain. It is limited by its small signal bandwidth, typically 16 MHz, and the power bandwidth, typically 4.8 MHz.

LOADING

Some restrictions on the output load apply to avoid oscillations and performance variations over temperature.

... Recommended load resistance is 500Ω or above and capacitance up to 50 pF; load resistance down to 250Ω can be used without degrading the performance. Capacitive loads up to 150 pF will be free of oscillations, but acquisition and settling times will be extended due to slew rate limitations in the output.

APERTURE JITTER

In a typical DSP Application, an analog signal needs to be digitized. This can be done with an A/D Converter; which has the limitation that the signal needs to be fairly constant throughout the conversion time, therefore, only low frequency signals can be converted without loss of accuracy. To handle faster signals, a Track-Hold Amplifier can be used in front of the A/D.

In order not to lose accuracy, the standard rule of thumb is that the input signal should not change more than ±½ LSB during the conversion time. This determines the maximum frequency for accurate conversion.

For example, take a 12-bit 10 μs A/D Converter. If it is operated on a 0V to 10V input range, 1 LSB is equivalent to:

$$\frac{10V}{2^{12}} = \frac{10V}{4096} = 2.44\ mV$$

and ½ LSB is 1.22 mV. The maximum allowable rate of change becomes:

$$\frac{dV}{dt} = \frac{\frac{1}{2}\ LSB}{\text{Conversion Time}} = \frac{1.22\ mV}{10\ \mu s} = 122\ V/s$$

For a sinewave of v(t) = A sine 2π ft, the derivative is a rate of change vs. time.

$$\frac{d\ v(t)}{dt} = 2\pi f\ A\ Cos\ (2\pi\ ft)$$

The extreme value of this is at t = 0, and the maximum rate of change becomes 2πfA.

If the sinewave is chosen for 10 V_{P_P}, or A = 5V, the maximum rate of change becomes 10πf. If this is equated to the maximum allowable rate of change, the frequency that can be converted accurately becomes:

$$f = \frac{122\ V/s}{2\pi 5V} = 3.9\ Hz$$

If a track-hold amplifier is used in front of the A/D, then much faster signals can be accurately digitized. In this case, the input waveform has to be repetitive, and the hold pulse is shifted in phase every time a new conversion is made, until the whole signal has been captured. The limitation for accuracy is determined by the aperture jitter, which is the uncertainty of the moment when the signal is frozen. In this case, the maximum slew rate is 1.22 mV/100 ps = 12.2 V/μs and the highest frequency at which accurate conversion occurs becomes:

$$f = \frac{12.2V/\mu s}{2\pi 5V} = 338\ kHz$$

The fact that the LH4860 can digitize the fastest part of a 338 kHz sine wave does not mean it can digitize that signal for reconstruction purposes. Realistically a sample can only be taken in the time it takes to acquire (200 ns for the LH4860) plus the conversion time of the ADC.

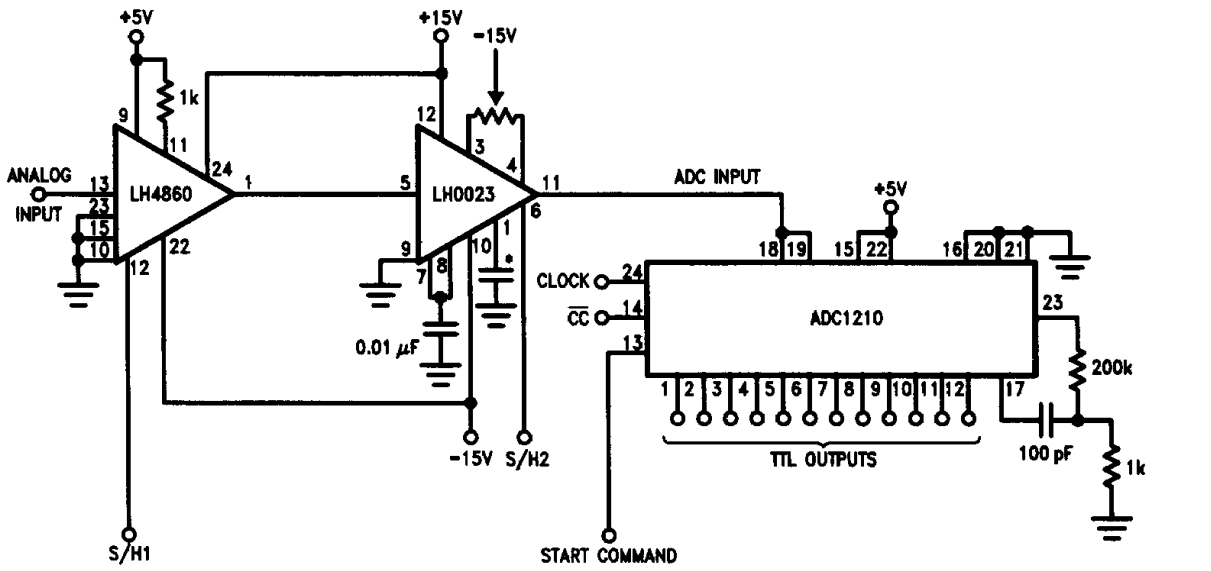
Other Considerations for Using the LH4860 with A/D Converters

There are several considerations for good match between track hold amplifier and A/D. One is that the output resistance of the T/H should be low compared to the input resistance of the A/D, up to frequencies 5 times the clockrate of the A/D. This is because of the digital nature of a successive approximation A/D its internal D/A changes its output momentarily and current transients occur at the A/D input. These should be sunk and settled before the next bit conversion. In the hold mode, the LH4860 has a typical output resistance of 0.1Ω; its output, typically, recovers to ±0.01% from 2 mA step in less than 100 ns.

Another consideration is the LH4860's track-to-hold transient settling time. Normally, the same timing pulse that initiates "hold" also starts the A/D conversion. The decision for the A/D's MSB, normally, takes place one clock cycle after the start signal, and at that time, the track-hold command pin can be driven directly (or inverted) from the successive approximation A/D's conversion status output. During conversion the T/H is in hold.

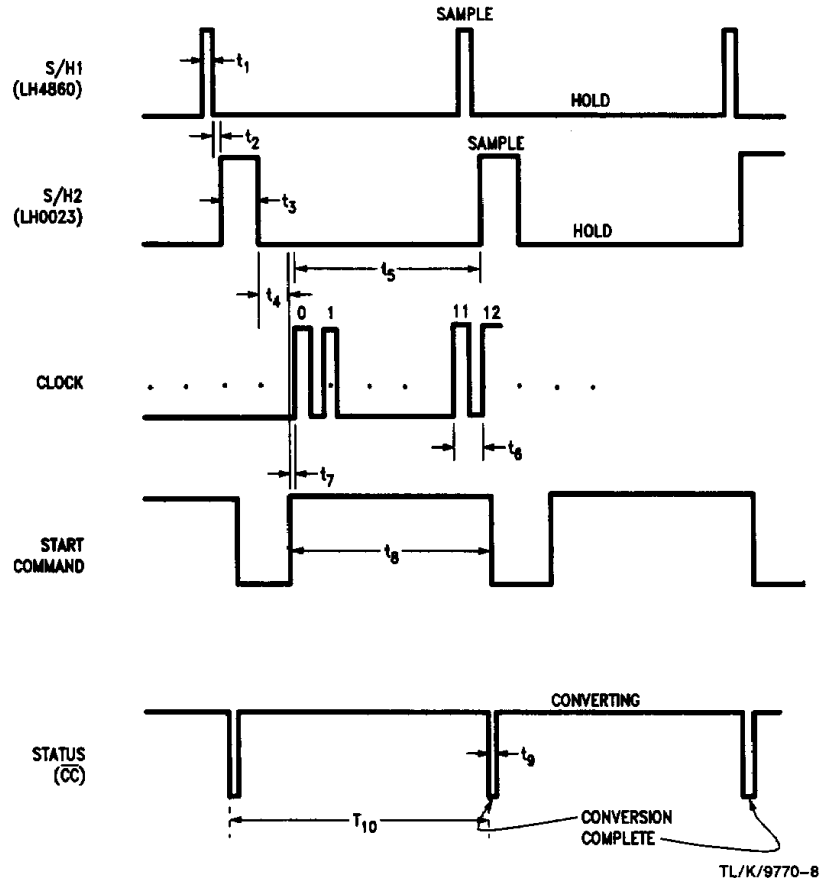
Many sampling A/D converter applications require that a signal be sampled fast but held for a long time so that a slow (inexpensive) A/D converter may be used. Such conflicting requirements place stringent demands on a S/H amplifier. Fortunately, cascading two S/H amplifiers, as in *Figure 3*, solves the problem. The LH4860 acquires the signal to within 0.01% F.S. in under 200 ns and holds it until the LH0023 acquires the sampled signal. The low droop rate of LH0023 allows it to hold the sampled signal to within 0.01% for as long as the conversion time of ADC1210 (100 μs). Note that the start pulse for the A/D converter should occur at the end of LH0023's hold mode settling time. *Figure 3's* circuit accepts a 0V to −5V full scale input signal and produces a complementary binary output. A typical timing dia-

Applications



*Polystyrene Cap 0.01 μF

FIGURE 3. Sampling A/D Converter



t_1 = S/H1 acquisition time = 200 ns
t_2 = S/H1 hold mode settling time = 100 ns
t_3 = S/H2 acquisition time = 20 μs
t_4 = S/H2 hold mode settling time = 15 μs
t_5 = Conversion time of ADC1210 = 100 μs
t_6 = Clock period = 7.7 μs
t_7 = Start pulse setup time = 30 ns
t_8 = Start pulse width = 105 μs
t_9 = Conversion complete time = 5 μs
t_{10} = Sampling period = $t_3 + t_4 + t_5 + t_7$ ≅ 135 μs

$f_s = \frac{1}{t_{10}} \cong 7.4$ kHz

FIGURE 4. Typical Timing Diagram for the Sampling A/D Converter (Not Drawn to Scale)

gram for the sampling A/D converter *(Figure 4)* shows a sampling frequency of 7.4 kHz, thus from Nyquist criteria, the input signal's maximum frequency should be limited to 3.52 kHz (i.e., half the sampling frequency). This circuit is well suited for capturing fast single shot events as well as repetitive signals and for operation at elevated temperatures at which the increased droop rate of LH4860 is compensated for by the low droop rate of LH0023.

Applications (Continued)

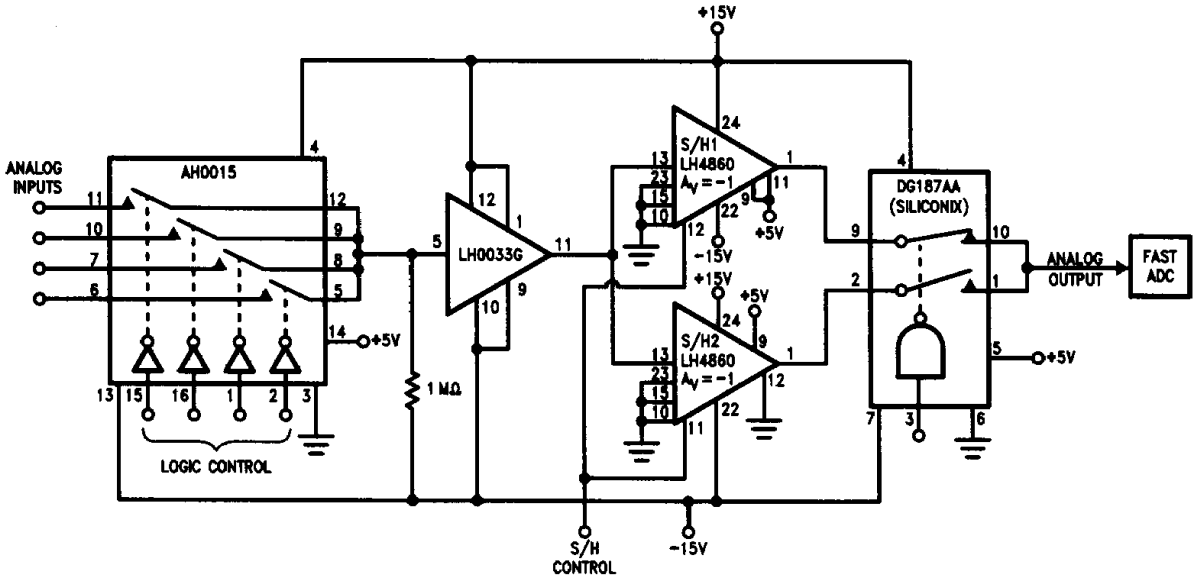


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FIGURE 5. Fast Data Acquisition Using Ping-Pong Switching

For ultrafast A/D converters with conversion time in the microsecond region, the S/H's acquisition and hold mode settling time can contribute significantly to the system's overall cycle time thus reducing system throughput. For example, an LH4860 at the front end of a 12-bit/1 μs ADC can add as much as 300 ns to the converter's conversion time thus increasing the sampling interval to 1300 ns; a 30% increase. However, by using two S/H amplifiers in a ping-pong switching configuration, the system's cycle time can be decreased to very nearly that of the ADC. *Figure 5* shows an ultrafast multi-channel data acquisition system. The AH0015 Mux allows the selection of 1 of 4 input signals in a process monitor application. Note that a logic "1" at AH0015's logic control pin closes the corresponding switch. Since LH4860's input impedance is only 1 kΩ, LH0033 buffers the input signal so as to prevent the S/H from loading the signal source, a 1 MΩ resistor at the buffer's input prevents the buffer's output from saturating when all Mux switches are open. The ping-pong switching scheme involves the use of a fast SPDT switch (DG187AA) to select the output of each S/H for half the sampling period. Thus, S/H1's output is selected when S/H1 is in the hold mode, the ADC meanwhile begins conversion. While the ADC is converting, S/H2 is acquiring a new sample of the input signal. As soon as the ADC's conversion is complete, S/H2 goes into hold mode and a new conversion can begin at the end of S/H2's hold mode settling time, S/H1 now goes into the sampling mode. This approach thus eliminates the S/H's acquisition time from the system's overall cycle time. Note that DG187AA's typical switch on and off times are less than the 100 ns hold mode settling time of the LH4860. Consequently, switching the S/H's output to the output channel at the instant the S/H goes from sample to hold mode eliminates the switch delay because the ADC's conversion does not begin until after the LH4860's hold mode settling time of 100 ns. Neglecting the minimal delay through LH0033G, a sampling interval of 1100 ns can be achieved, this is only a 10% increase over the minimum available sampling interval. It should be noted that since LH0033 and LH4860 do not have precisely unity gain, they introduce gain error in addition to voltage offset. The gain error and offset of the entire system can, however, be trimmed out by the ADC's gain and offset trim circuits. The circuit in *Figure 5* accepts −5V to +5V input signals and produces an inverted output. The circuit described is ideally suited for interface with flash ADCs having sub-microsecond conversion times, and, taking advantage of the ping-pong switching scheme allows significant improvement in system throughput compared to a single S/H and ADC combination.