National Semiconductor

LM1211 Broadband Demodulator System

General Description

The LM1211 is a high performance IF amplifier and product detection system for operation in the 20–80 MHz frequency range. It is suitable for data or video recovery from broadband local area networks and other communications systems.

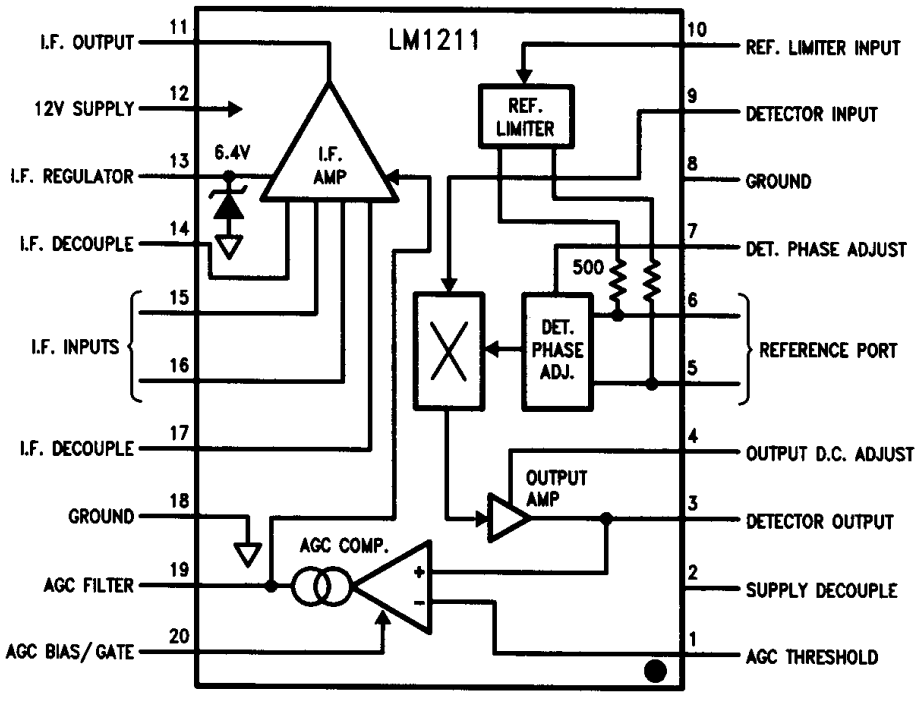
The high gain IF amplifier has a SAW filter compatible input and can be gain-controlled in excess of 40 dB. A flexible product detector is used in which the input signal is multiplied by a reference derived from limiting and phase-shifting the input. The signal input is separate from the reference path, which has a port for external connections. A DC-operated phase control is provided for detection phase adjustment.

The detector is followed by a 25 MHz bandwidth amplifier which has a symmetric output swing capability around 0V. A fast attack, peak-following AGC detector is also provided for use in AM systems.

Features

- Configurable for AM or FM based signals
- 20–80 MHz operating frequency range
- IF input SAW filter compatible
- >40 dB IF gain control range
- 25 MHz detector output bandwidth
- Linear output phase response
- Output swings ±3.5V referenced to ground
- Gateable peak-following AGC detector
- DC-adjustable detection phase
- DC-adjustable 0 carrier output level

Connection Diagram



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Order Number LM1211N
See NS Package Number N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage, V12	15V
IF Supply Current, I13	40 mA
Detector Output Current, I3	15 mA
Detector Input Signal, V9	1 Vrms
Ref. Limiter Input Signal, V10	1 Vrms
AGC Bias/Gate Current, I20	3 mA
Power Dissipation	1.67W
Thermal Resistance	60°C/W
Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	260°C
ESD Susceptibility (Note 1)	3000V

DC Electrical Characteristics

T_A = 25°C, Test Circuit, $V_{IF} = V_{Det} = 0$, $V_{AGC} = 0$, $V_{PH} = 4V$, $V_{OC} = 6V$, all switches open unless noted.

Symbol	Parameter	Test Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limit)
I_S	Supply Current	SW 3 closed, $V_{AGC} = 3V$	67	80		mA (max)
V_{13}	IF Regulator Voltage	SW 3 closed, $V_{AGC} = 3V$	6.5	5.8 7.0		V (min) V (max)
$V_{15/16}$	IF Input Voltage	SW 2, 3 closed	3.9	3.4 4.4		V (min) V (max)
$V_{14}-V_{17}$	IF Decouple V_{OS}	SW 2, 3 closed, measure $V_{14}-V_{17}$	0	±50		mV (max)
I_{11}	IF Output Current	SW 2, 3 closed, $V_{AGC} = 6V$, $I_{11} = \frac{12V - V_{11}}{50}$	4.0	2.5 5.0		mA (min) mA (max)
V_{10}	Limiter Input Bias	SW 1, 2, 3 closed	5.1	4.5 5.5		V (min) V (max)
V_9	Detector Input Bias	SW 1, 2, 3 closed	5.1	4.5 5.5		V (min) V (max)
$V_{5/6}$	Reference DC Voltage	SW 1, 2, 3 closed	4.6	4.0 5.2		V (min) V (max)
V_3	O Carrier Output Voltage	SW 1, 2, 3 closed	0	±0.5		V (max)
V_{OC}	O Carrier Adjust Voltage	SW 1, 2, 3 closed, adjust V_{OC} for V_3 = OV	6.0	1.0 11.0		V (min) V (max)
$I_{19(D)}$	AGC Discharge Current	SW 1, 3 closed, $V_{AGC} = 2V$	−11	−7 −16		µA (min) µA (max)
$I_{19(C)}$	AGC Charge Current	SW 1, 4 closed, $V_{AGC} = 6V$	1.0	0.7 1.3		mA (min) mA (max)
$I_{19(L)}$	AGC Leakage Current	SW 1, 2, 4 closed, $V_{AGC} = 4V$	−25	±200		nA (max)

Note 1: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 2: Tested limits are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed, but not 100% production tested. These limits are not used to determine outgoing quality levels.

Detector AC Set-up Procedure

T_A = 25°C, Test Circuit, Sw 1, 2, 3 closed, V_{AGC} = 0, V_{PH} = 4V.

1. With no input (V_{Det} = 0), adjust V_{OC} for V3 = 0V.
2. Apply V_{Det} = 100 mVrms, 60 MHz CW at the input. Tune L2 for maximum DC voltage at output Pin 3.

AC Electrical Characteristics

T_A = 25°C, Test Circuit, Follow AC set-up procedure, f = 60 MHz, V_{AGC} = 0, V_{PH} = 4V, V_{OC} as per set-up, all switches open unless noted.

Symbol	Parameter	Test Conditions	Typ	Tested Limit (Note 1)	Design Limit (Note 2)	Units (Limit)
Z15/16	IF Input Impedance	Measure Differential Impedance between Pins 15 and 16.	60		40 80	Ω (min) Ω (max)
Av(IF)	Maximum IF Gain (Note 3)	SW 2 Closed, V_{IF} = 0.5 mVrms, Measure V_{out}. Av(IF) = 20 log $\left(\frac{V_{out}}{5 \times 10^{-4}}\right)$	30	20		dB (min)
V_{AGC20}	20 dB Gain Reduction	SW 2 Closed, V_{IF} = 5 mVrms, Adjust V_{AGC} for Same V_{out} as in Av(IF) Test.	2.6	2.2 3.0		V (min) V (max)
V_{AGC40}	40 dB Gain Reduction	SW 2 Closed, V_{IF} = 50 mVrms, Adjust V_{AGC} for Same V_{out} as in Av(IF) Test.	3.8	3.3 4.3		V (min) V (max)
IM	IF Intermodulation (Note 3)	SW 2 Closed, f_1 = 60 MHz, f_2 = 65 MHz, V_{IF} = 10 mVrms Ea, Adjust V_{AGC} for V_{out} = 10 mVrms Ea, Measure IM Products Relative to V_{out}.	−40		−30	dB (min)
Z9	Detector Input Impedance	Measure Impedance into Pin 9	3.0		2.0 5.0	KΩ (min) pF (max)
Z10	Reference Limiter Input Impedance	Measure Impedance into Pin 10	2.0		1.3 5.0	KΩ (min) pF (max)
Av(D)	Detector Conversion Gain	SW 1, 2, 3 Closed, V_{Det} = 100 mVrms, Measure V_{3DC}. Av(D) = 20 log $\left(\frac{V_3}{0.1}\right)$	24	20 30		dB (min) dB (max)
LIN	Detector-6dB Linearity	SW 1, 3 Closed, V_{Det} = 50 mVrms, Measure V_3'. LIN = 20 log $\left(\frac{V_3'}{V_3}\right)$	−6	−5 −7		dB (min) dB (max)
$V_{3(Th)}$	AGC Threshold	SW 1, 3 Closed, Increase V_{Det} until I19 = 100 μA, Measure V_3.	2.8		2.6 3.0	V (min) V (max)
$V_{3(OL)}$	Detector Overload Capability	SW 1, 2, 3 Closed, V_{Det} = 1 Vrms, Measure V_3.	4.1	3.5		V (min)
PHA(+)	DC Phase Adjust (+)	SW 1, 2, 3 Closed, V_{Det} = 100 mVrms, Measure Ratio of V_3 with V_{PH} = 6V to V_3 with V_{PH} = 4V.	0.65	0.95		V/V (max)
PHA(−)	DC Phase Adjust (−)	SW 1, 2, 3 Closed, V_{Det} = 100 mVrms, Measure Ratio of V_3 with V_{PH} = 2V to V_3 with V_{PH} = 4V.	0.30	0.60		V/V (max)
$V_{3(-)}$	Negative Output Swing	SW 1, 2, 3 Closed, f = 70 MHz, V_{Det} = 300 mVrms, V_{PH} = 6V, Measure V_3.	−3.7	−3.0		V (min)
DBW	Detector Output Bandwidth	SW 1, 2, 3 Closed, Modulate V_{Det} with 30% AM Modulation. Increase Modulation Frequency Until Pin 3 Signal Drops 3 dB.	25		20	MHz (min)
DHL	Detector Harmonic Levels	SW 1, 2, 3 Closed, V_{Det} = 100 mVrms, Measure 60 MHz and 120 MHz Levels Relative to V_3	−35		−20	dB (min)

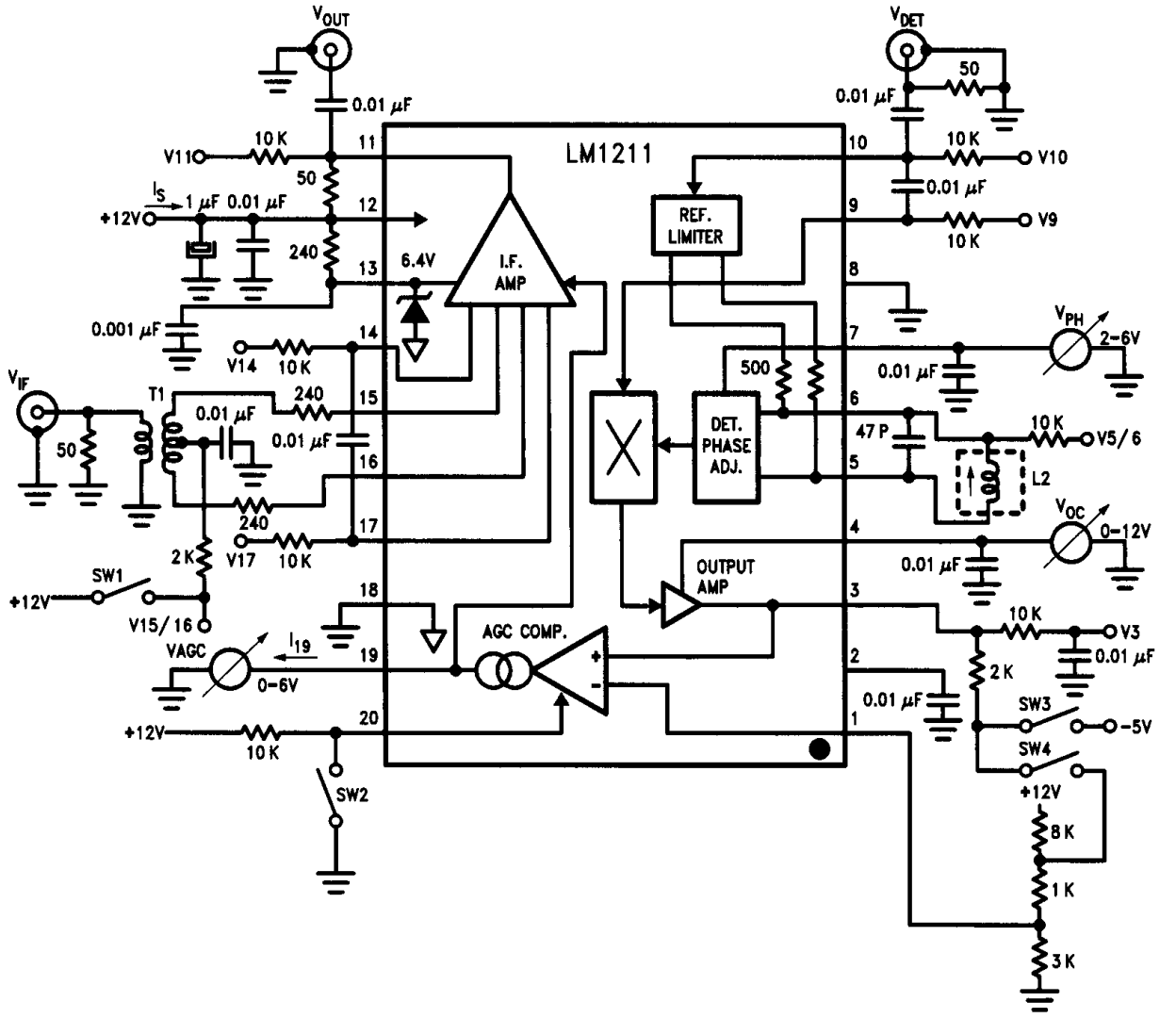
Note 1: Tested limits are guaranteed and 100% production tested.

Note 2: Design limits are guaranteed, but not 100% production tested. These limits are not used to determine outgoing quality levels.

Note 3: The IF amplifier output is measured with the IF output connected to a 50Ω measurement system resulting in a 25Ω loaded impedance. The gain in an actual application will typically be 20 dB higher.

Test Circuit

Measure Parameters at Indicated Test Points



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T1 = 50Ω unbal. to bal. Mini-circuits Lab TM01T-1T

L2 = 4½ T #22 wire on 3/16" form with HF core, shielded

Typical Performance Characteristics

(All characteristics apply to the typical application circuit. Figure numbers are referenced in the applications information.)

FIGURE 1
IF Amplifier Gain Reduction Characteristic

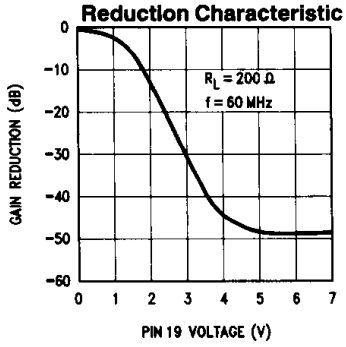


FIGURE 2
IF Amplifier Frequency Response

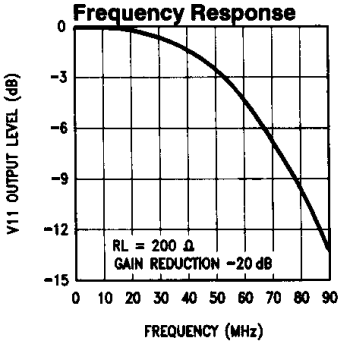


FIGURE 3
IF Amplifier Noise Figure vs. AGC

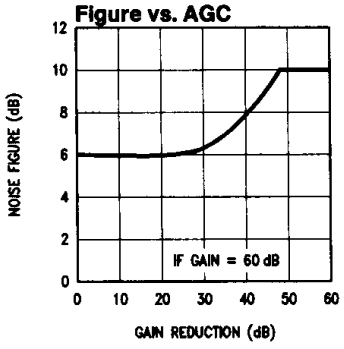


FIGURE 4
LM1211 Detection Phase

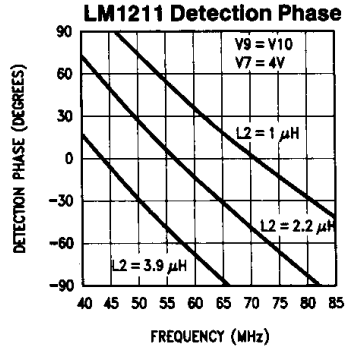


FIGURE 5
Detector Phase Adjust Characteristic

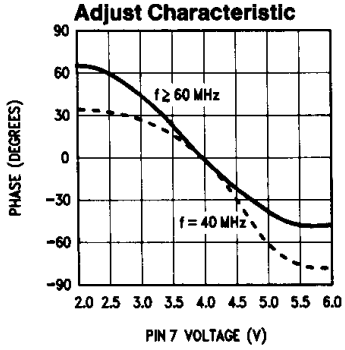
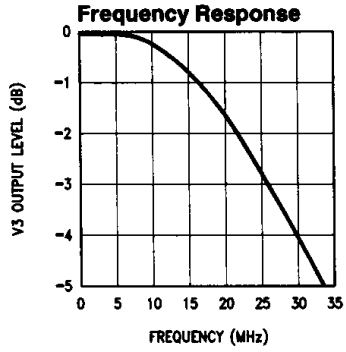


FIGURE 6
Output Amplifier Frequency Response



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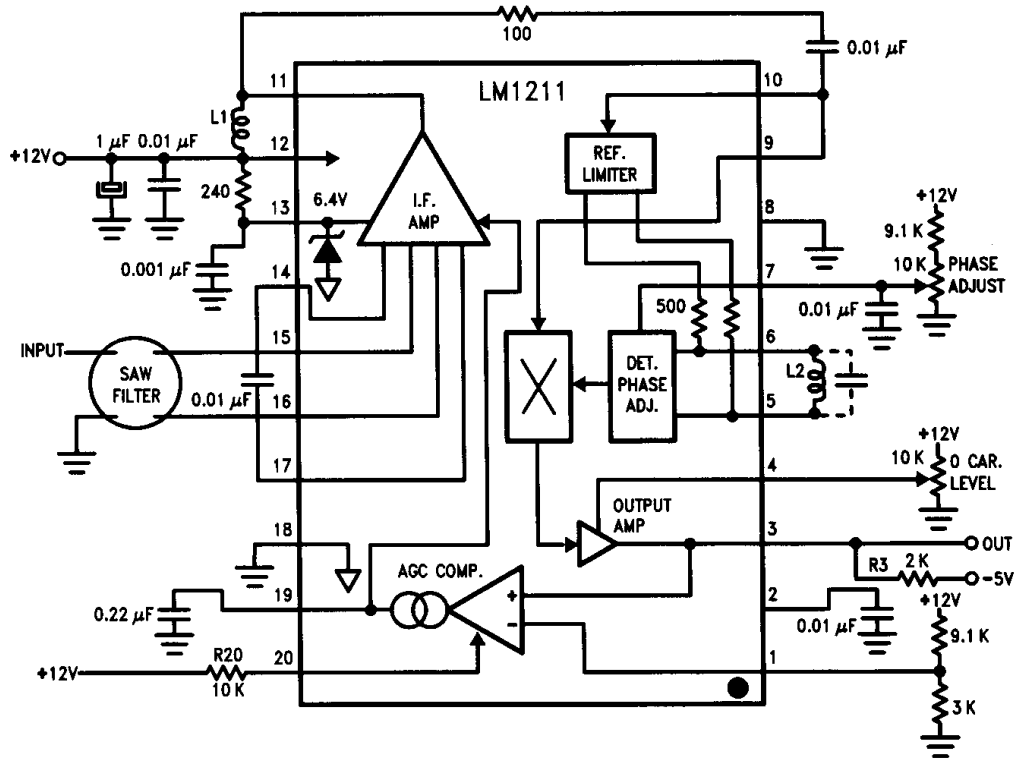
Typical Application Circuit



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Applications Information (Refer to Typical Performance Characteristics and Application Circuit.)

The LM1211 broadband demodulator system provides essentially independent IF amplifier and wideband detector blocks on the same integrated circuit. The IF amplifier consists of 5 differential stages, 3 of which have gain control capability. The detector is a highly flexible product detector with separate signal and reference input pins and a wideband output amplifier. An AGC comparator operating from the detector output is also provided. The operation of each of these blocks will now be described.

IF AMPLIFIER

The IF amplifier is powered from an internal shunt regulator between IF supply Pin 13 and IF ground Pin 18. The regulator has a nominal value of 6.5V and the IF amplifier current is delivered through a dropping resistor from the 12V rail supplying the remainder of the LM1211. The 0.001 μF ceramic RF decoupling capacitor at Pin 13 should be grounded through very short leads—preferably on the copper side of the PCB. A nominal current level into Pin 13 is 23 mA, set by a 240Ω resistor. This current should not exceed 40 mA and the minimum current is about 16 mA, below which the IF amplifier will start to lose gain as the Pin 13 voltage drops below the regulated level.

IF Amplifier Input Configuration

Circuit detail for the IF amplifier input Pins 14–17 is shown in *Figure 7.* The input stage is a common-base differential amplifier designed to give good rejection of unwanted IF output and detector reference signals that may be radiated back to the input.

The low differential input impedance of 60Ω ensures that SAW filters are terminated sufficiently to keep the triple transit echo (TTE) more than 40 dB below the signal level, even with low impedance SAW filters. Because it is a common base stage, the input stage gain is inversely proportional to the source impedance Zs presented to the input. A normal range for differential Zs is from 100Ω to 1 KΩ. As an example, a typical high impedance SAW filter has an output impedance that can be modeled as a 2 KΩ resistor in parallel with 6 pF capacitance, yielding Zs = 372Ω at 70 MHz. Alternatively, the IF may be used with a transformer input configuration similar to that shown in the Test Circuit, as long as the required source impedance is maintained.

A balanced input is extremely important since the input leads to Pins 14–17 are the most sensitive points in the system to unwanted IF coupling. For example, if the IF output or detector reference signals couple into these pins it can cause changes in the frequency response and can easily promote oscillation. A spectrum analyzer is invaluable for helping determine the system susceptibility to this phenomenon. With the input terminated by the IF filter (or an equivalent resistor), the IF amplifier output noise spectrum will show if oscillation is likely to occur at maximum gain. A good layout will have symmetrical input leads placed as close together as possible, shielded input coils (where used), and external components mounted as close to the I.C. as possible. The DC feedback decoupling capacitor connected between Pins 14 and 17 should be right against the pins.

Gain Control Stages

The second through fourth differential stages of the IF amplifier are gain controlled by the voltage at the AGC Filter Pin 19. 0V corresponds to maximum IF gain, while increasing the Pin 19 voltage results in the gain reduction curve shown in *Figure 1.*

In most AM applications, the Pin 19 voltage will be under control of the AGC detector (to be described later) in a closed feedback loop. If Pin 20 of the AGC detector is grounded, Pin 19 is tri-stated, allowing it to be externally controlled. In the tri-stated condition the typical input bias current at Pin 19 is only 25 nA, allowing small filter capacitors to be used in gated AGC systems. The *Figure 1* characteristics has a temperature dependence of approximately −0.1 dB/°C. While this has no bearing in a closed loop system, it precludes setting a temperature stable fixed gain via a resistive divider at Pin 19.

For FM applications, the IF amplifier may be locked at maximum gain by grounding Pin 19. Under these conditions none of the 5 stages saturate when overdriven, allowing the amplifier to function as a basic wideband limiter.

IF Amplifier Output

The fifth and final IF amplifier stage has a single-ended output, with no internal connection to the detector block. The output Pin 11 is an open collector NPN transistor which must be returned to Pin 12 via a DC path. Pin 11 is also a point at which any additional signal filtering may be applied. A resistive load connected to Pin 12 can be used, but the maximum value is limited in practice to less than 500Ω at intermediate frequencies because of stray capacitance and the loading of the detector stage input impedance.

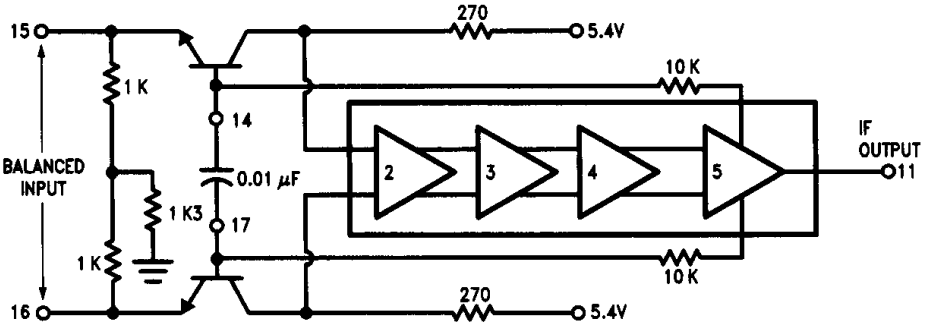

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FIGURE 7. Low Impedance Common Base Input Stage

Applications Information (Refer to Typical Performance Characteristics and Application Circuit.) (Continued)

The frequency response for the IF amplifier with a 200Ω load is shown in *Figure 2*. The high frequency rolloff gives rise to a potential problem called "tilt." This occurs in wide bandwidth signals when the upper frequency components are attenuated relative to the lower frequency components, which can cause amplitude distortion following demodulation. Tilt can be easily compensated at Pin 11 by using an inductive load to provide an increasing impedance with frequency. The impedance of inductive load L1, including the effects of stray capacitance, is given by:

$$|Z_L| = \frac{\omega L_1}{1 - \omega^2 L_1 C_S}$$

For example, a 0.33 μH coil with 8 pF stray capacitance at Pin 11 has an impedance of 300Ω at 70 MHz, and this impedance is on a frequency dependent slope of 0.4 dB/MHz. As the inductance is increased, the slope becomes steeper until resonance with the stray capacitance is reached. By using this technique, a flat IF response can be obtained over the frequency range of interest.

IF Amplifier Gain and Noise Figure

As described earlier, the maximum IF amplifier gain in the LM1211 is externally determined by the input source impedance, Zs, in conjunction with the output load impedance, Z_L. This gain is approximately given by:

$$A_V = \frac{(1000)|Z_L|}{|Z_S| + 60}$$

The IF amplifier noise figure (NF) as a function of gain reduction is shown in *Figure 3*. The contribution of IF NF to the overall system NF depends on the amount of gain ahead of the IF in the mixer and IF filter.

The SAW filter output mistermination, determined by the IF amplifier input impedance, is desirable from the viewpoint of keeping the TTE more than 40 dB below the signal. However, the mismatch at the input to the SAW filter is not so desirable as it simply increases the filter losses. Therefore a preferable solution is to use a low impedance SAW filter which will reduce losses, or to provide a pre-amplifier stage such as shown in *Figure 8* between the mixer and SAW filter. Since this stage can also be used to match the mixer output to the SAW filter input, the filter losses can be reduced.

To illustrate the effectiveness of this approach, a 10 dB gain pre-amp with a 4 dB NF will put the NF after the mixer stage at 23 dB, and the increase in NF with AGC action (by about 4 dB) will not contribute significantly to the system NF. A useful rule of thumb is that the total NF of the stages following the mixer should not exceed the mixer gain.

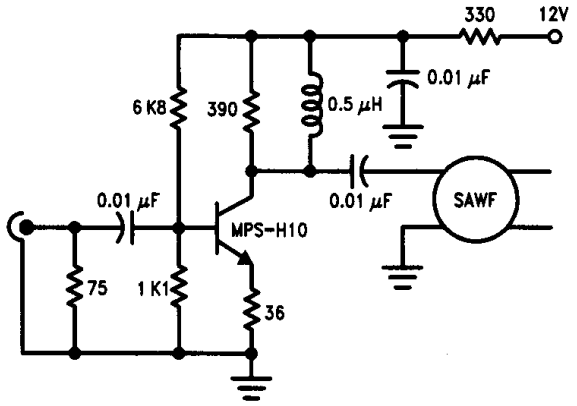

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FIGURE 8. SAW Filter Gain Stage

Detector

The detector section operates from a 12V supply between Pin 12 and ground Pin 8. The LM1211 uses a product detector comprised of a multiplier, reference limiter, detector phase adjuster, and wideband output amplifier (see block diagram). The demodulation process of multiplying the detector input by a limited version of the input is called quasi-synchronous detection. This process provides a wider reference bandwidth but reduced efficiency in carrier nulls relative to a true synchronous detector.

While the following description will apply to quasi-synchronous detection, the LM1211 can be made to function as a true synchronous detector if an external phase-locked loop (PLL) is used. In this mode, the reference limiter input Pin 10 is decoupled and the voltage-controlled oscillator (VCO) signal from the PLL is coupled into the reference port at Pins 5 and 6. Differential coupling of any external signal into the reference port is critical to minimize feedback to the IF amplifier inputs.

Multiplier

The heart of the product detector is the 6 transistor balanced multiplier shown in *Figure 9*. The detector input Vs(t) at Pin 9 is coupled to the linear differential pair, while the reference input Vr(t) switches the upper quad devices at the carrier rate.

If Vs(t) is an amplitude modulated carrier Fm(t)coswt and Vr(t) is a square wave of the same frequency w and relative phase ϕ, then the filtered output is given by:

$$V_{OUT} = \frac{2}{\pi}\frac{RL}{Re} Fm(t)\cos\phi$$

The output depends on the amplitude of Vs(t) and relative phase ϕ between Vs(t) and Vr(t). If ϕ is made 0 degrees so cosϕ is 1, then the multiplier acts as an amplitude detector and can be used to detect the amplitude modulation Fm(t) on the IF carrier. Note that around 0 degrees cos ϕ changes very little with phase. The multiplier can also be used as a

Detector (Continued)

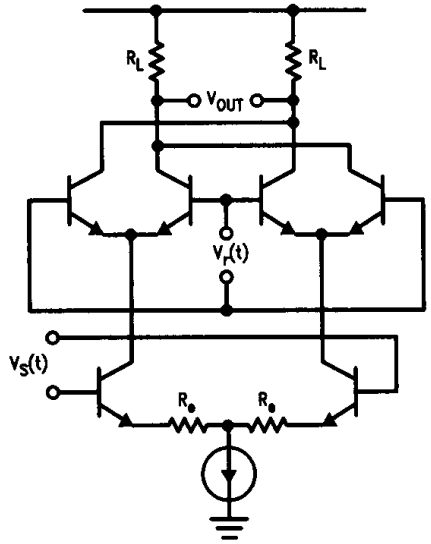

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FIGURE 9. Balanced Multiplier Circuit

phase or frequency detector if Vs(t) is limited to remove amplitude information and ϕ is centered at 90 degrees, where cosϕ produces the largest change in output for a given change in phase.

Thus a vital part of setting up the detector will be to obtain the correct relative phase for the type of demodulation desired.

Reference Limiter

The purpose of the reference limiter is to create the reference signal required for product detection by stripping AM modulation off the input signal. This should not be confused with the limiter required in an FM system, which is in the main signal path. FM limiting would be performed by locking the IF amplifier at maximum gain as previously described, in which case the reference limiter becomes redundant.

A single differential limiter stage is provided between Pin 10 and the reference port at Pins 5 and 6. Pin 10 is internally biased from a 5.1V source through a 3.3 KΩ resistor; the detector input Pin 9 is biased from the same source through 5 KΩ. By sharing a common bias point Pins 9 and 10 can be directly shorted together when fed from the same signal, thus saving a coupling capacitor. Alternatively, Pins 9 and 10 may be fed separately allowing phase and/or amplitude differences to be introduced.

The reference limiter output is a differential signal across the reference port Pins 5 and 6. Pins 5 and 6 are internally biased at 4.6V and have a 1 KΩ differential impedance. Limiting begins with 20 mVrms at Pin 10 and heavy limiting occurs above 100 mVrms input. The maximum limited output voltage is 350 mVrms.

Detector Phasing

As we have seen, the relative phase between the detector and reference inputs of the multiplier determines the LM1211 demodulation characteristic. The detector input phase is known since it connects directly to Pin 9. However, the reference phase depends on several factors: The external components at Pins 10, 5, and 6, the phase shift through the reference limiter, and lastly the setting of the detector phase adjust control at Pin 7. The general approach for phasing the detector is to first select the external components which produce the desired detection phase when the phase adjust control is in the center of its range (V7 = 4V), and then use the control to trim part-to-part and external component variations.

The curves of *Figure 4* give the multiplier detection phase versus frequency for different values of L2 with Pins 9 and 10 shorted together. These curves can be used to select the L2 value and to determine whether additional phase shift between Pins 9 and 10 is required. The detection phase versus temperature is approximately −0.25 degrees/°C.

A detection phase of ϕ = 0 degrees corresponds to maximum (+) amplitude detection efficiency, i.e. the detector output voltage increasing with Pin 9 input level. In the simplest case this can be obtained by choosing the L2 for which the *Figure 4* curve passes through 0 degrees at or near the IF frequency. When the proper phasing cannot be obtained by this means, phase lead or lag must be introduced at Pin 10 relative to Pin 9. A simple RC lead-lag network which can provide up to ±90 degrees phase shift is shown in *Figure 10.*

When XC1 = XC2 = 240Ω in the *Figure 10* circuit, approximately 90 degrees of phase difference between Pins 9 and 10 is produced with 3 dB additional attenuation. Pin 10 is shown lagging Pin 9, but the two pins could be reversed to produce phase lead. If C1 is increased or C2 is decreased, the phase difference is reduced.

A wideband FM quadrature detector is implemented in *Figure 11* by configuring the IF Amplifier for maximum gain and replacing L2 with an LC tank tuned to the IF frequency. Since the IF Amplifier performs the limiting function, the reference limiter is not used; rather, the quadrature signal is fed directly to the reference port via an RC phasing network. The DC offset at Pin 10 (13 KΩ to 12V) prevents signal leakage through the reference limiter to Pins 5 and 6.

The FM detector sensitivity depends on the phase slope of the LC tank, which is determined by the Q. For example, the tank in *Figure 11* is resonant around 70 MHz and has a Q ≅ 2 defined by the internal 1 KΩ resistance across Pins 5 and 6 in parallel with the external resistor. Deviating the input frequency produces an output characteristic given by:

$$V3 = V_{pk}[\cos(90 \pm \Delta 0)]$$

where V_{pk} is the theoretical peak output level set by the IF Pin 11 load impedance, and Δ0 is the combined phase swing produced by the tank and detector. For the *Figure 11* circuit, V_{pk} = 6V and Δ 0 ≅ 5 degrees/MHz, yielding an output swing of ±0.5 V/MHz.

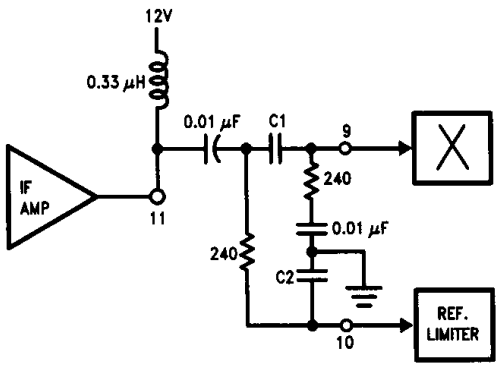

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FIGURE 10. Detector Input Phasing Network

Detector (Continued)

Phase Adjust Control

Once the external components have been selected for the correct nominal phasing, the detector phase adjust is used to perform the final set-up by monitoring the detector output either for maximum output in the case of AM detection or for 0V average level for FM detection. The phase adjust control Pin 7 is externally biased via a potentiometer and resistor from 12V and requires a 2V to 6V minimum range at Pin 7. The amount of phase lead or lag added to the reference path as a function of V_7 is given in *Figure 5.* For example, at 70 MHz a cumulative phase error of ±50 degrees could be compensated for by the phase adjust control.

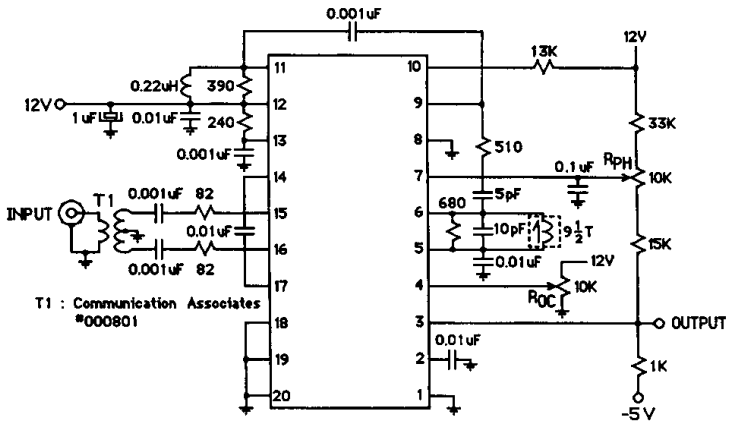
While the previously cited −0.25 degrees/°C detection phase temperature dependence is not noticeable in AM detection applications, it can cause the average DC level of the FM detector output to drift. This can be reduced by using the phase adjust control in a feedback loop as shown in *Figure 11.* Finally, it should be re-emphasized that the Pin 7 adjustment is intended as a trim rather than a substitute for correct detector phasing.

Detector Output

The LM1211 output amplifier has an NPN emitter follower driving Pin 3 through a 50Ω damping resistor as shown in *Figure 12.* The nominal 0 carrier (no input signal) output voltage is 0V, and a negative supply is required as a return point for the external load resistor R3. The output may be biased at up to 5 mA in order to maintain the (−) slew rate into capacitive loads.

The 0 carrier output voltage is adjusted by the control voltage on a potentiometer at Pin 4. The center of the Pin 4 range is ½ supply with an adjustment sensitivity of approximately 0.1 V/V. Thus on a 12V supply up to ±0.6V part-to-part output variation can be trimmed out. The Pin 3 output is capable of swinging up to ±4V; however, in certain AM detector applications the output will always remain above 0V. In these cases it may be possible to omit the negative supply and return the Pin 3 load resistor directly to ground. This will result in some degradation in linearity at low output voltages which can be minimized by pre-biasing the 0 carrier level high (V4 = 12V).

The output amplifier frequency response is shown in *Figure 6.* The output exhibits a linear phase response of approximately −5.5 degrees/MHz out to 30 MHz. The first 70 MHz carrier harmonic is approximately −46 dB and the second harmonic −40 dB referenced to a 3V peak output.



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ALIGNMENT SEQUENCE:

1. With no input, adjust R_{OC} for V3 = 0V.
2. Apply V_{in} ≥ 10 mVrms, Fo = 70 MHz ±5 MHz Dev, Fm = 100 kHz; Tune Quadrature coil for best output linearity.
3. Adjust R_{PH} for output DC centering.

FIGURE 11. 70 MHz FM Detector Application

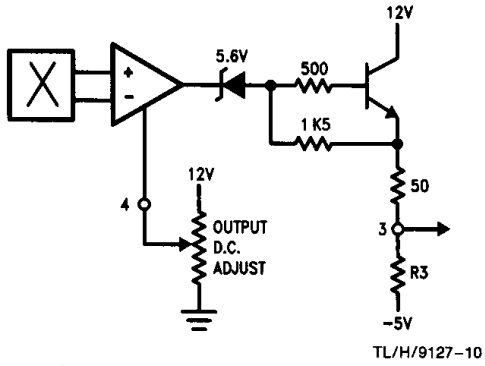

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FIGURE 12. Detector Output Amplifier

Detector (Continued)

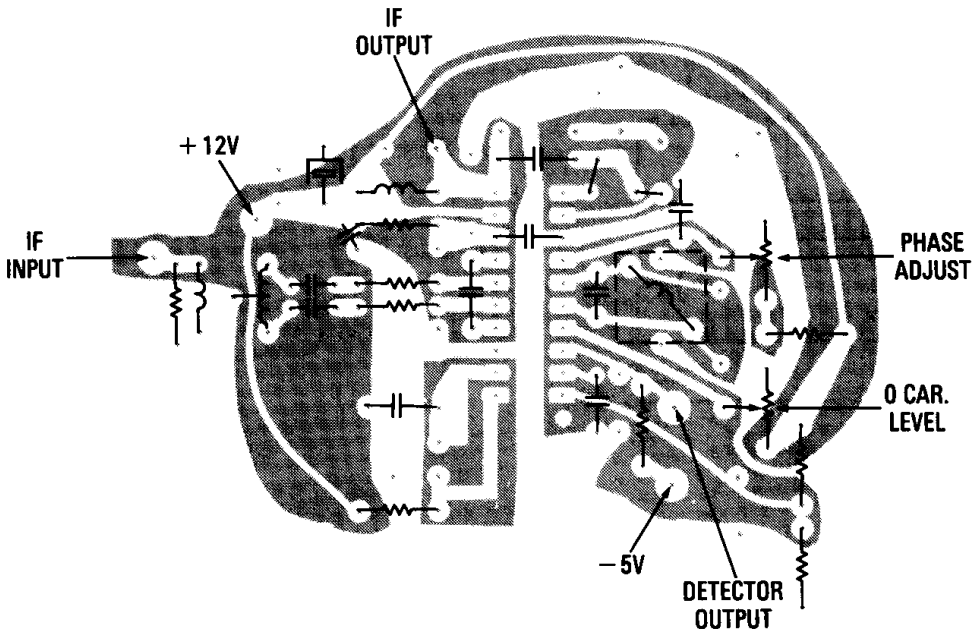
AGC Comparator

An AGC comparator is provided for use in AM systems. The (+) input is internally connected to the detector output Pin 3 while the (−) input is biased from an external resistive divider at AGC threshold Pin 1. An output current charges and discharges the AGC filter capacitor at Pin 19 to control the IF amplifier gain. The comparator is biased by a current into bias/gate Pin 20. Internally, Pin 20 has a diode in series with 1 KΩ to ground so that the current level from an external resistor R20 to 12V is given by:

$$I20 = \frac{11.3}{R20 + 1000}$$

Whenever the detector output exceeds the AGC threshold, a current equal to the Pin 20 bias current is delivered to Pin 19 to charge the AGC filter capacitor. When the detector output is below the AGC threshold, approximately 11 μA discharge current flows into Pin 19. Thus the charge to discharge current ratio at Pin 19 is given by I20/11 μA, or 90:1 for I20 = 1 mA. This large ratio creates a peak-detecting action in which the AGC loop holds the detector (+) output peaks at the AGC threshold voltage, typically 1-3V. Because of the large ratio of charge to discharge current, the LM1211 AGC has inherently faster recovery from a step increase in signal than from a decrease. The overall speed is inversely proportional to the AGC filter capacitor, with 0.05 μF being a practical lower limit for I20 = 1 mA. It is important to use a quality (low Rs) capacitor at Pin 19 to prevent AGC oscillation.

The AGC detector can be used at lower charge/discharge ratios by reducing I20 which has a direct effect on the charge current but only a second order effect on the discharge current. For I20 = 100 μA a 15:1 ratio is produced and a 0.01 μF minimum capacitor can be used. As the charge/discharge ratio is reduced, peak detection no longer occurs and gating of Pin 20 may be necessary. This requires an external gate pulse generator to turn on the Pin 20 bias current only during the time the detector output is to be sampled. In between gate pulses the Pin 19 output will be tri-stated and the filter capacitor will hold the previous voltage until the next gate pulse. Permanently grounding Pin 20 turns off the AGC comparator, allowing an external AGC signal at Pin 19 to control the IF amplifier gain.



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Printed Circuit Layout (component side)