National Semiconductor

LH4266 SPDT RF Switch

General Description

The LH4266 is a single pole double throw switch intended for RF and video switching applications. The device has a TTL compatible control signal and can be configured as a multiplexer or demultiplexer which will fulfill most switching needs.

The non-selected input may be terminated to provide a match to the source driving that port and prevent spurious oscillations that might occur from an unterminated transmission line.

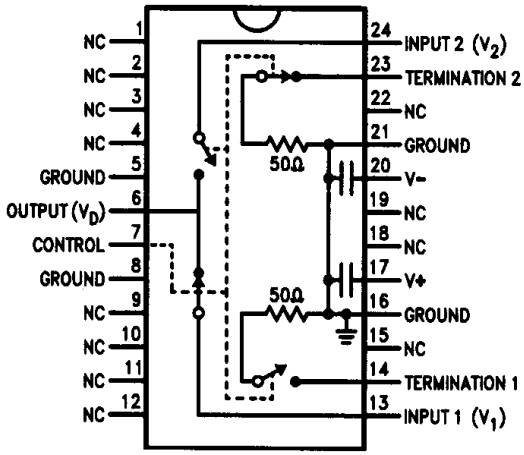
Features

- Single pole double throw (SPDT)
- DC to 150 MHz
- +27.5 dBm maximum signal (50Ω)
- Low insertion loss 1.5 dB (50Ω)
- Non-selected input terminated
- Break before make
- TTL compatible control signal
- Internal power supply bypassing

Applications

- ATE pin driver switch
- Computer RF switch
- Tester switching matrix
- RF voltage multiplexer

Connection Diagram



TL/K/9404-1

Top View

Note: NC means no internal connection.

Order Number LH4266CD or LH4266D
See NS Package Number D24I

3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, (V_S)	±18V
Power Dissipation, (P_D)(See Curve)	2.0W
Input Signal, (V_{IN})	$\pm V_S$
ESD	TBD
Control Voltage, (V_C)	V_S-2V
Storage Temperature Range, (T_{STG})	−65°C to +150°C
Operating Temperature Range, (T_A)	
LH4266CD	−25°C to +85°C
LH4266D	−55°C to +125°C
Lead Temperature (T_L) (Soldering, < 10 seconds)	300°C

DC Electrical Characteristics $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 50\Omega$, $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	LH4266C			Units (Max. unless otherwise noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
I_S	Supply Current	V^+	4.8	7		mA
		V^-	−47	−60		
V_{TH}	Logic High		1.5	2.0		V (Min)
V_{TL}	Logic Low		0.5	0.8		V
I_{IN}	Control Input Current	V_{IN} = 0V to 5V	2.0	3.0		µA
R_{ON}	On Resistance	$V_1 = V_2 = 0V$, I_D = 1 mA	15	18		Ω
Δ_r	Resistance Match			4		
	Leakage Current	$V_{1-2} = V_D = \pm 5V$, Switch On, Note 4		100		nA
		$V_{1-2} = V_D = \pm 5V$, Switch Off, Note 4		100		
		$V_{1-2} = V_D = \pm 5V$, Input to Input		100		

DC Electrical Characteristics

$V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 50\Omega$, $T_A = 25°C$ unless otherwise noted. (Note 1)

Symbol	Parameter	Conditions	LH4266			Units (Max. unless otherwise noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
I_S	Supply Current	V^+	4.8	**7**		mA
		V^-	−47	**−60**		
V_{TH}	Logic High		1.5	**1.8**		V (Min)
V_{TL}	Logic Low		0.5	**0.8**		V
I_{IN}	Control Input Current	V_{IN} = 0V to 5V	2.0	**3.0**		µA
R_{ON}	On Resistance	$V_1 = V_2 = 0V$, I_D = 1 mA	15		**30**	Ω
Δ_r	Resistance Match			**6**		
	Leakage Current	$V_{1-2} = V_D = \pm 5V$, Switch On, Note 4		**1**		µA
		$V_{1-2} = V_D = \pm 5V$, Switch Off, Note 4		**1**		
		$V_{1-2} = V_D = \pm 5V$, Input to Input		**1**		

AC Electrical Characteristics $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 50\Omega$, $T_A = 25°C$, unless otherwise noted.

Symbol	Parameter	Conditions	LH4266C/LH4266			Units (Max. unless otherwise noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
	Insertion Loss	10 MHz	1.0	1.5		dB
		100 MHz	2.0	2.3		
	Isolation Input to Output See Test Circuit	10 MHz	90	75		dB (Min)
		100 MHz	75	60		
	Isolation Input1 to Input2	10 MHz	90			
		100 MHz	60			
	Distortion	$V_{OUT} = 10\ V_{p-p}$	1.0			%
V_{SWR}		Unselected Input	1.5 : 1			Ratio
T_{SW}	Switching Speed		500			ns

Note 1: Boldface limits are guaranteed over full temperature range.

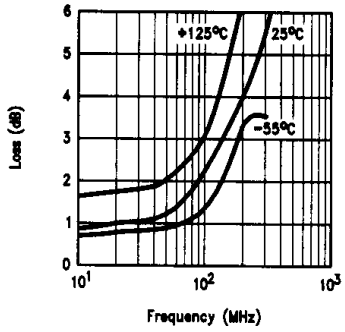
Note 2: Tested limits are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not production tested) over the indicated temperature range. These limits are not used to calculate outgoing quality level.

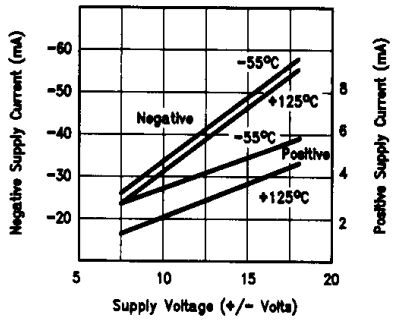
Note 4: Leakage current is measured with signal applied to each input. See test circuit.

Typical Performance Characteristics

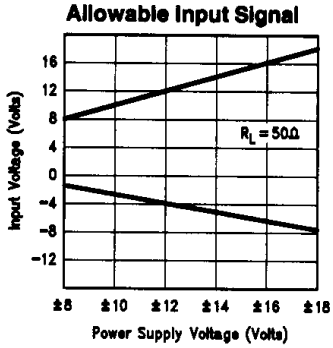
Insertion Loss



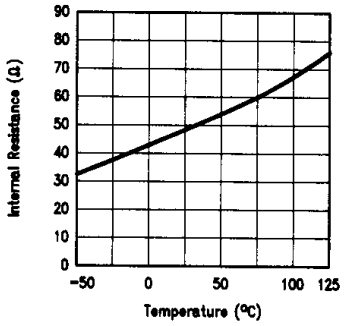
Supply Current



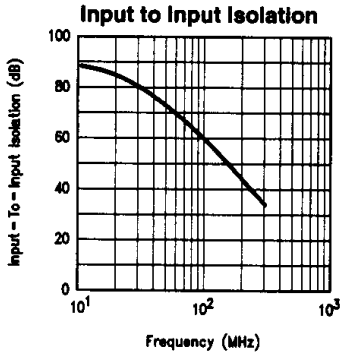
Allowable Input Signal



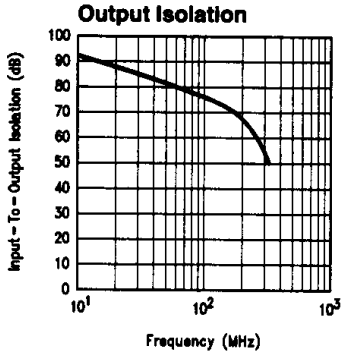
Internal Termination Resistance



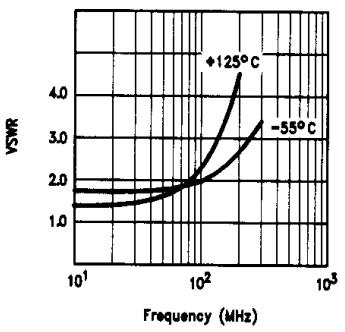
Input to Input Isolation



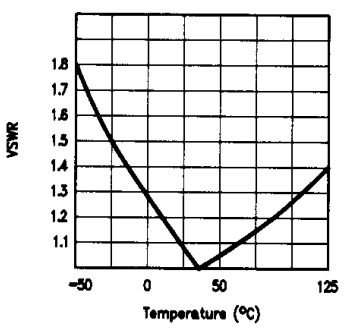
Input to Output Isolation



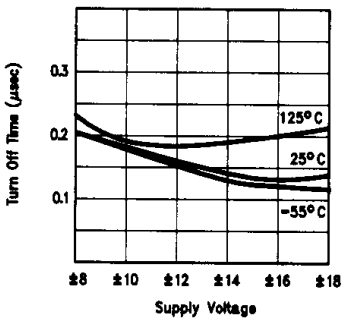
Termination VSWR



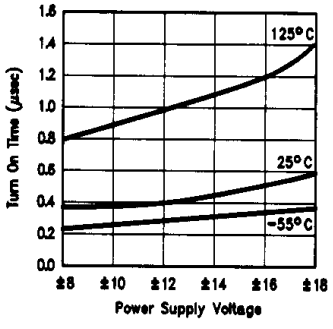
Termination VSWR



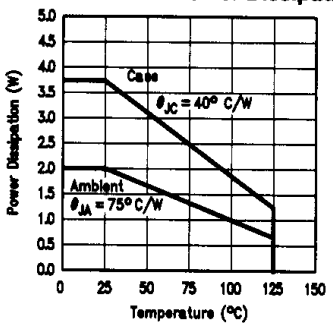
Turn Off Time



Turn On Time

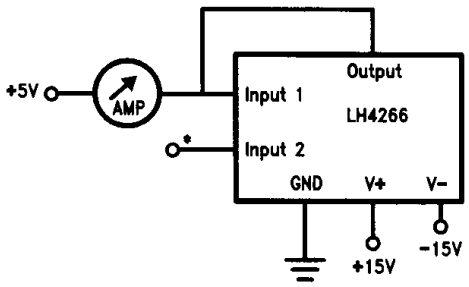


Maximum Power Dissipation



TL/K/9404-7

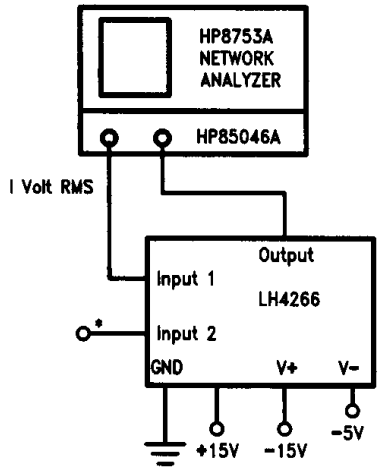
Leakage Current Equivalent Test Circuit



TL/K/9404-11

*Same test for Input 2.

Test Circuit for Isolation Input to Output



TL/K/9404-12

Applications Information, LH4266

The LH4266 uses hybrid technology to give increased circuit performance. In order to maintain its excellent cross talk and feedthru specifications, proper RF grounding and shielding should be incorporated in the printed circuit board layout. For example; the input traces should not run next to output traces and grounds should be provided by a ground plane under the device (see *Figure 1a, b* for suggested PC board layout).

The device contains two internal termination resistors and switches. If termination of the non-selected input is desired, connect the termination pin to the adjacement input pin and the deselected input will be terminated with approximately 50Ω.

Note that the internal termination resistors are internally connected to the device's ground pin. Thus if the internal termination resistors are used then the input ground planes should remain isolated from the output ground plane (as in *Figure 1*) so as not to form a ground loop. When using external termination resistors at the input, the resistors should be connected to their respective ground planes, and, pin 16 should be tied to input1's ground plane while pin 21 is tied to input2's ground plane. Since pins 16 and 21 are internally connected to the device ground pin, the input and output ground planes should remain isolated. LH4266's power supplies are internally bypassed with high frequency capacitors for ease of use. Thus for high frequency applications bypass capacitors are not required, however, at low frequencies (10 MHz or less) a 4.7 μF bypass capacitor for each supply is recommended.

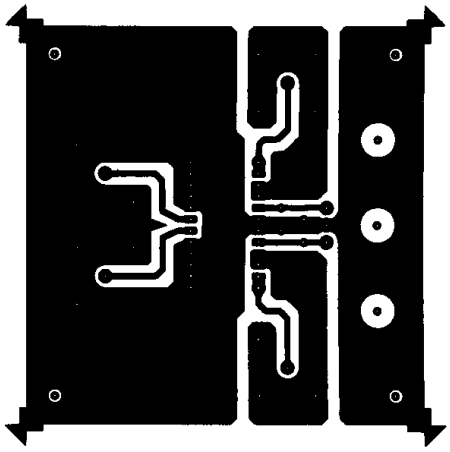
Due to the unique design of the LH4266 it can easily be used as a multiplexer or demultiplexer. In fact several units can be connected to give a 1 to 4 multiplexer or a 4 to 1 demultiplexer by simply adding the required units as shown in *Figures 2* to *5*.

The action of the switches can be seen in the following truth table.

LH4266 Truth Table

Control	Pin 24 Input 2	Pin 13 Input 1
Low = 0	On	Off
High = 1	Off	On

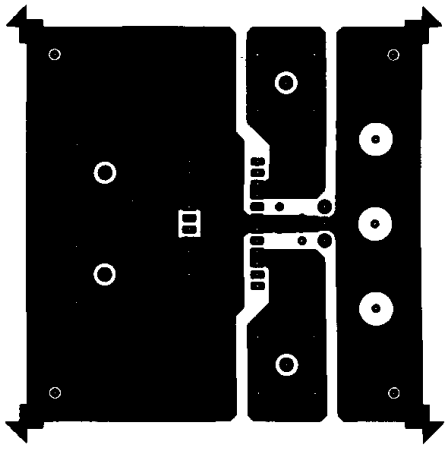
Double Sided Board, Bottom Side



TL/K/9404-2

FIGURE 1a. LH4266, Recommended Printed Circuit Board Layout

Double Sided Board, Top Side



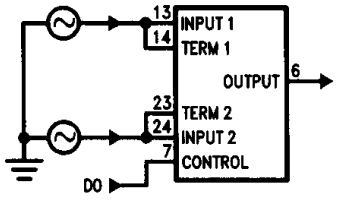
TL/K/9404-13

FIGURE 1b. LH4266, Recommended Printed Circuit Board Layout

Video Switch

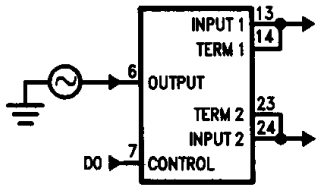
The LH4266 is ideally suited for video signal switching applications. *Figure 7* shows how the LH4266 may be used to select one of two video input signals while the LH4006 buffer allows driving four doubly terminated 75Ω cables. R1 biases the buffer's output to 0V and prevents the output stage from saturating when both switches are momentarily open. Meanwhile, R2 eliminates the offset voltage caused by the buffer's input bias current, and, a 10 pF capacitor across R2 prevents undesirable oscillations caused by stray capacitance at the buffers's inverting input. The circuit is capable of producing ±1V at the terminated ends of the 75Ω cables. To maintain LH4266's excellent input to output isolation and input to input crosstalk specifications, extreme care should be exercised while laying out the printed circuit board. From *Figure 1*'s recommended printed circuit board layout it can be observed that there are three separate ground planes. Each input signal should be referenced to it's respective ground plane while the output signal, control signal and power supplies are referenced to the output ground plane. Note that LH4266's internal termination resistors are internally connected to the device's ground pin. Consequently, if LH4266's internal termination resistors are used then the input and output ground planes should remain isolated (as in *Figure 1*) so as to prevent a ground loop from occurring. When an external termination resistor is used as in *Figure 7*, the resistor should be connected to its respective ground plane, while pin 16 is tied to input1's ground plane and pin 21 is tied to input2's ground plane. Moreover, all ground planes should remain isolated because pins 16 and 21 are internally connected to the device ground pin.

Application Circuits, LH4266



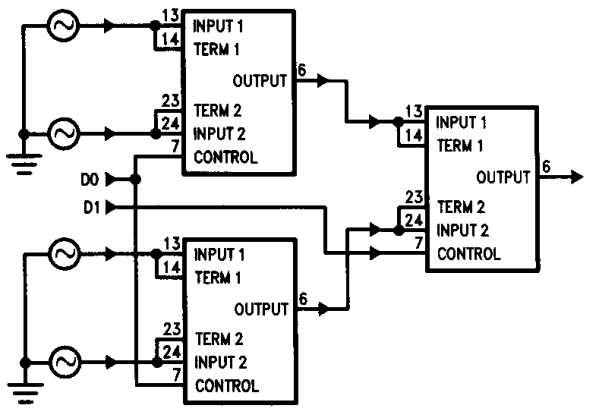
TL/K/9404-3

FIGURE 2. 2 to 1 Multiplexer



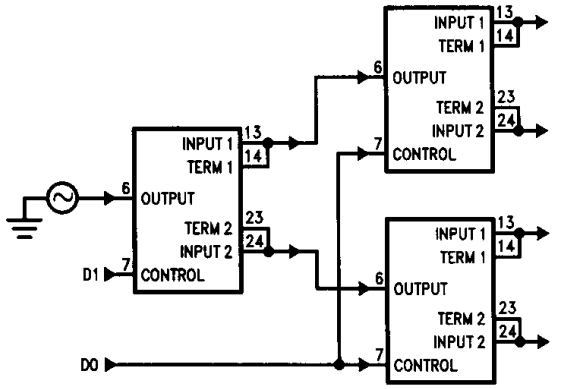
TL/K/9404-4

FIGURE 3. 1 to 2 Demultiplexer



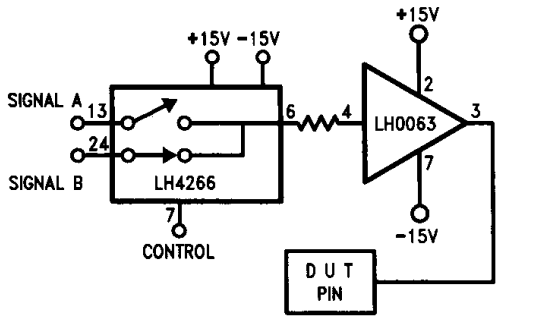
TL/K/9404-5

FIGURE 4. 4 to 1 Multiplexer



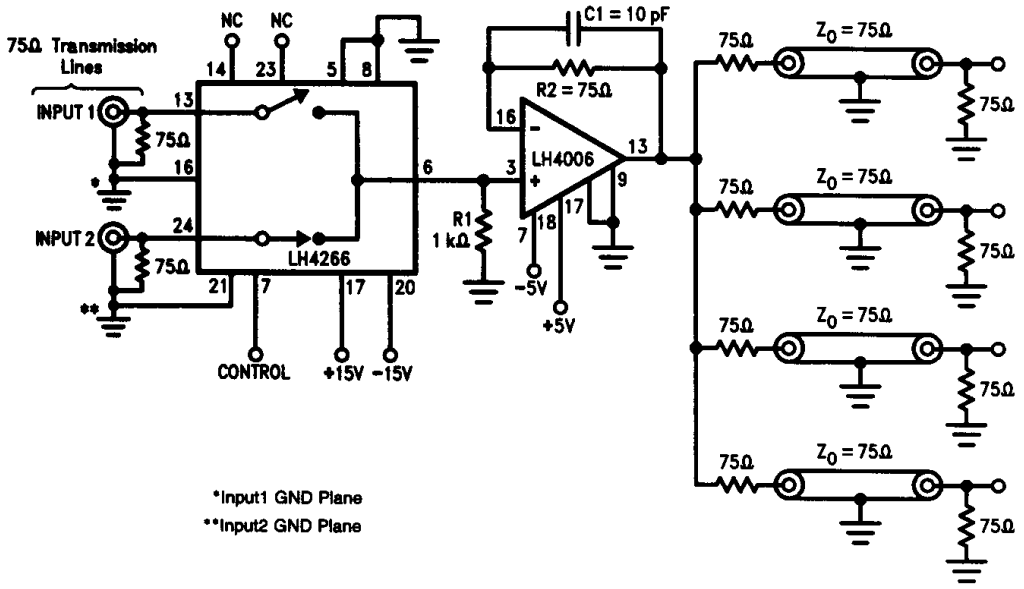
TL/K/9404-6

FIGURE 5. 1 to 4 Demultiplexer



TL/K/9404-8

FIGURE 6. ATE Pin Driver Switch



TL/K/9404–10

FIGURE 7. Video Switch