

# LM4911 Boomer® Audio Power Amplifier Series

## Stereo 40mW Low Noise Headphone Amplifier with Selectable Capacitive Coupled or OCL Output

### General Description

The LM4911 is an stereo audio power amplifier capable of delivering 40mW per channel of continuous average power into a 16Ω load or 25mW per channel into a 32Ω load at 1% THD+N from a 3V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. Since the LM4911 does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems. In addition, the LM4911 may be configured for either single-ended capacitively coupled outputs or for OCL outputs (patent pending).

The LM4911 features a low-power consumption shutdown mode and a power mute mode that allows for faster turn on time with less than 1mV voltage change at outputs on release. Additionally, the LM4911 features an internal thermal shutdown protection mechanism.

The LM4911 is unity gain stable and may be configured with external gain-setting resistors.

### Key Specifications

- PSRR at 217Hz and 1kHz 65dB (typ)
- Output Power at 1kHz with  $V_{DD} = 2.4V$ , 1% THD+N into a 16Ω load 25mW (typ)
- Output Power at 1kHz with  $V_{DD} = 3V$ , 1% THD+N into a 16Ω load 40mW (typ)
- Shutdown Current 2.0μA (max)
- Output Voltage change on release from Shutdown  $V_{DD} = 2.4V, R_L = 16\Omega$  (C-Coupled) 1mV (max)
- Mute Current 100μA (max)

### Features

- OCL or capacitively coupled outputs (patent pending)
- External gain-setting capability
- Available in space-saving MSOP and LD packages
- Ultra low current shutdown mode
- Mute mode allows fast turn-on (1ms) with less than 1mV change on outputs
- 2V - 5.5V operation
- Ultra low noise

### Applications

- Portable CD players
- PDAs
- Portable electronics devices

### Block Diagram

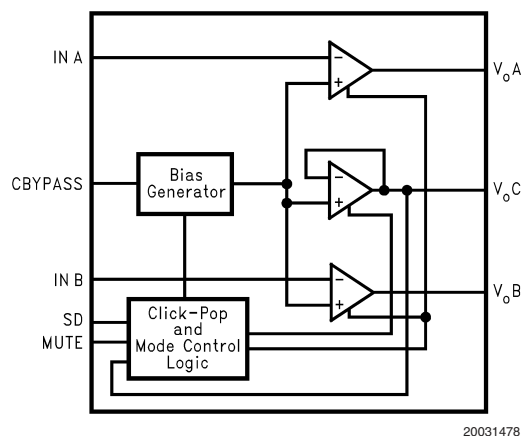
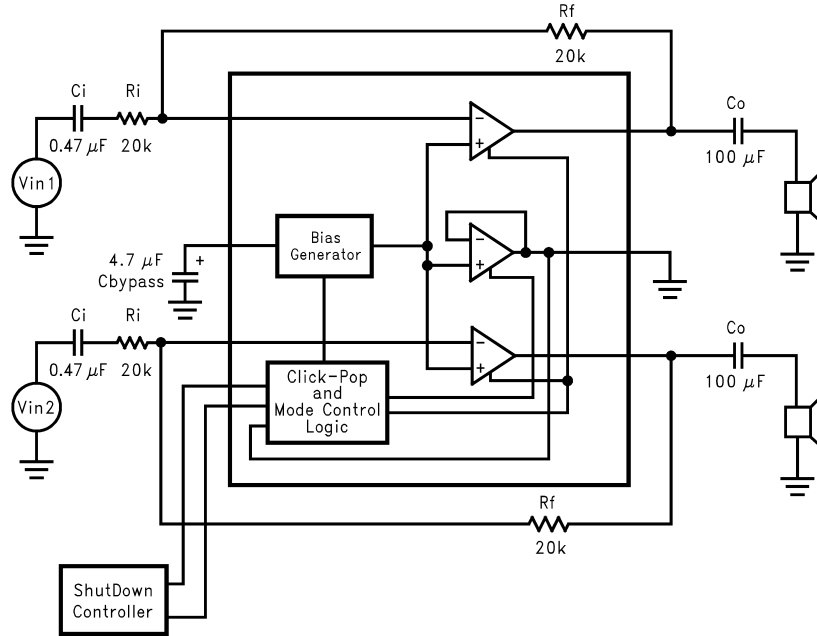


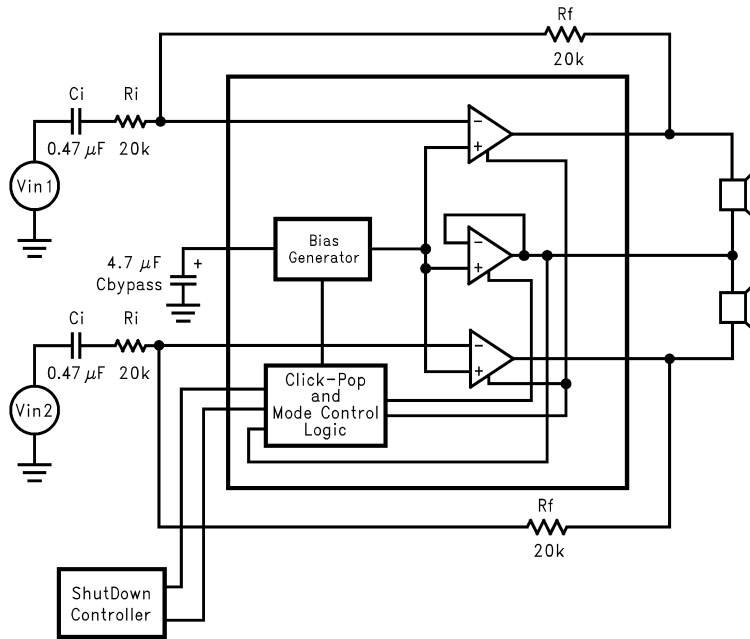
FIGURE 1. Block Diagram

# Typical Application



20031480

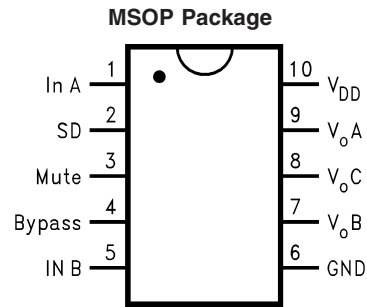
**FIGURE 2. Typical Capacitive Coupled Output Configuration Circuit**



20031481

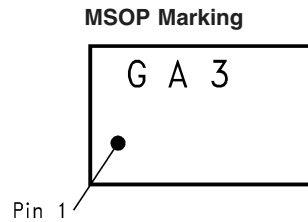
**FIGURE 3. Typical OCL Output Configuration Circuit**

# Connection Diagrams



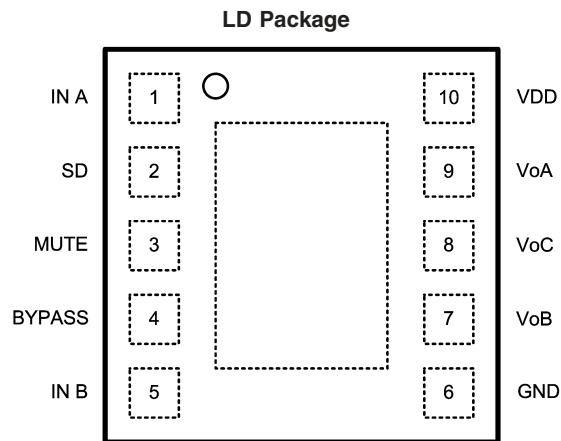
20031479

**Top View**  
**Order Number LM4911MM**  
**See NS Package Number MUB10A**



200314A9

**Top View**  
**G-Boomer Family**  
**A3 - LM4911MM**



200314C0

**Top View**  
**Order Number LM4911LD**  
**See NS Package Number LDA10A**

**Absolute Maximum Ratings** (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	-65°C to +150°C
Input Voltage	-0.3V to $V_{DD} + 0.3V$
Power Dissipation (Note 3)	Internally Limited
ESD Susceptibility (Note 4)	2000V
ESD Susceptibility (Note 5)	200V
Junction Temperature	150°C

## Thermal Resistance

$\theta_{JC}$ (MSOP)	56°C/W
$\theta_{JA}$ (MSOP)	190°C/W
$\theta_{JA}$ (LD) (Note 10)	63°C/W
$\theta_{JA}$ (LD) (Note 10)	12°C/W

**Operating Ratings**

## Temperature Range

$T_{MIN} \leq T_A \leq T_{MAX}$	-40°C $\leq T_A \leq$ 85°C
Supply Voltage ( $V_{DD}$ )	$2V \leq V_{CC} \leq 5.5V$

**Electrical Characteristics  $V_{DD} = 5V$**  (Notes 1, 2)

The following specifications apply for  $V_{DD} = 5V$ ,  $R_L = 16\Omega$ , and  $C_B = 4.7\mu F$  unless otherwise specified. Limits apply to  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	LM4911		Units (Limits)
			Typ (Note 6)	Limit (Note 7)	
$I_{DD}$	Quiescent Power Supply Current	$V_{IN} = 0V, I_O = 0A$	2	5	mA (max)
$I_{SD}$	Shutdown Current	$V_{SHUTDOWN} = GND$	0.1	2.0	$\mu A$ (max)
$I_M$	Mute Current	$V_{MUTE} = V_{DD}$ , C-Coupled	50	100	$\mu A$ (max)
$V_{SDIH}$	Shutdown Voltage Input High		1.8		V
$V_{SDIL}$	Shutdown Voltage Input Low		0.4		V
$V_{MIH}$	Mute Voltage Input High		1.8		V
$V_{MIL}$	Mute Voltage Input Low		0.4		V
$P_O$	Output Power	THD $\leq 1\%$ ; $f = 1$ kHz OCL, $R_L = 16\Omega$ LM4911LD OCL $R_L = 16\Omega$ (Note 10) OCL, $R_L = 32\Omega$ C-CUPL, $R_L = 16\Omega$ C-CUPL, $R_L = 32\Omega$	80 145 80 145 85		mW
$V_{ON}$	Output Noise Voltage	BW = 20Hz to 20kHz, A-weighted	10		$\mu V$
PSRR	Power Supply Rejection Ratio	$V_{RIPPLE} = 200mV$ sine p-p $f = 1kHz$ (Note 9)	65		dB

**Electrical Characteristics  $V_{DD} = 3.0V$**  (Notes 1, 2)

The following specifications apply for  $V_{DD} = 3.0V$ ,  $R_L = 16\Omega$ , and  $C_B = 4.7\mu F$  unless otherwise specified. Limits apply to  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	LM4911		Units (Limits)
			Typ (Note 6)	Limit (Note 7)	
$I_{DD}$	Quiescent Power Supply Current	$V_{IN} = 0V, I_O = 0A$	1.5	3	mA (max)
$I_{SD}$	Shutdown Current	$V_{SHUTDOWN} = GND$	0.1	2.0	$\mu A$ (max)
$I_M$	Mute Current	$V_{MUTE} = V_{DD}$ , C-Coupled	50	100	$\mu A$ (max)
$P_O$	Output Power	THD = 1%; $f = 1kHz$ $R = 16\Omega$ $R = 32\Omega$	40 25		mW
$V_{NO}$	Output Noise Voltage	BW = 20 Hz to 20kHz, A-weighted	10		$\mu V$
PSRR	Power Supply Rejection Ratio	$V_{RIPPLE} = 200mV$ sine p-p	65		dB

## Electrical Characteristics $V_{DD} = 2.4V$ (Notes 1, 2)

The following specifications apply for  $V_{DD} = 2.4V$ ,  $R_L = 16\Omega$ , and  $C_B = 4.7\mu F$  unless otherwise specified. Limits apply to  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	LM4911		Units (Limits)
			Typ (Note 6)	Limit (Note 7)	
$I_{DD}$	Quiescent Power Supply Current	$V_{IN} = 0V, I_O = 0A$	1.5	3	mA (max)
$I_{SD}$	Shutdown Current	$V_{SHUTDOWN} = GND$	0.1	2.0	$\mu A$ (max)
$I_M$	Mute Current	$V_{MUTE} = V_{DD}, C$ -Coupled	40	80	$\mu A$ (max)
$P_O$	Output Power	THD = 1%; f = 1kHz			mW
		R = 16 $\Omega$	25		
		R = 32 $\Omega$	12		
$V_{NO}$	Output Noise Voltage	BW = 20 Hz to 20kHz, A-weighted	10		$\mu V$
PSRR	Power Supply Rejection Ratio	$V_{RIPPLE} = 200mV$ sine p-p	65		dB
$T_{WU}$	Wake Up Time from Shutdown	OCL	0.5		s
		C-Coupled, $C_O = 100\mu F$	2		
$V_{OSD}$	Output Voltage Change on Release from Shutdown	C-Coupled, $C_O = 100\mu F$		1	mV (max)
$T_{UM}$	Time to Un-Mute	C-Coupled, $C_O = 100\mu F$	0.01	0.02	s (max)

**Note 1:** All voltages are measured with respect to the GND pin unless otherwise specified.

**Note 2:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

**Note 3:** The maximum power dissipation must be derated at elevated temperatures and is dictated by  $T_{JMAX}$ ,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable power dissipation is  $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$  or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4911, see power derating currents for more information.

**Note 4:** Human body model, 100pF discharged through a 1.5k $\Omega$  resistor.

**Note 5:** Machine Model, 220pF-240pF discharged through all pins.

**Note 6:** Typical values are measured at 25 $^\circ C$  and represent the parametric norm.

**Note 7:** Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

**Note 8:** Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

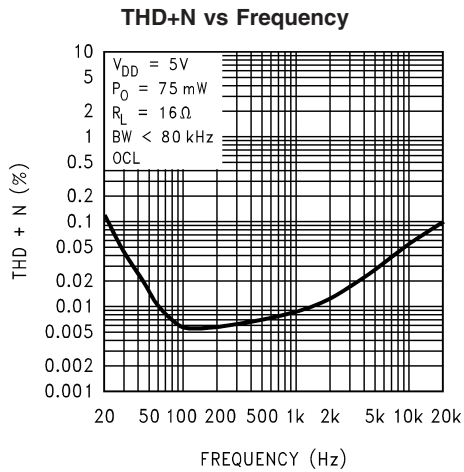
**Note 9:** 10 $\Omega$  Terminated input.

**Note 10:** The LDA10A package has its exposed-DAP soldered to an exposed 1.2in<sup>2</sup> area of 1oz. Printed circuit board copper.

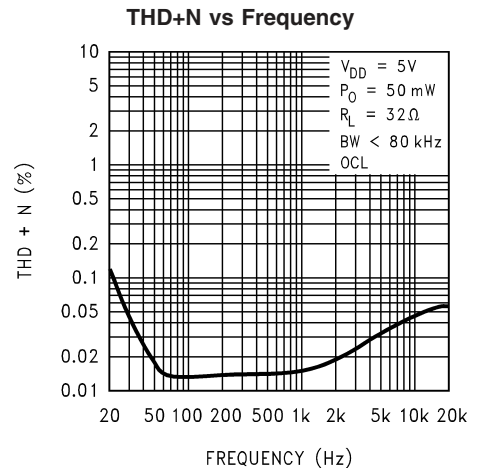
## External Components Description (Figure 2)

Components		Functional Description
1.	$R_i$	Inverting input resistance which sets the closed-loop gain in conjunction with $R_f$ . This resistor also forms a high-pass filter with $C_i$ at $f_c = 1/(2\pi R_i C_i)$ .
2.	$C_i$	Input coupling capacitor which blocks the DC voltage at the amplifier's input terminals. Also creates a high-pass filter with $R_i$ at $f_c = 1/(2\pi R_i C_i)$ . Refer to the section <b>Proper Selection of External Components</b> , for an explanation of how to determine the value of $C_i$ .
3.	$R_f$	Feedback resistance which sets the closed-loop gain in conjunction with $R_i$ .
4.	$C_S$	Supply bypass capacitor which provides power supply filtering. Refer to the <b>Power Supply Bypassing</b> section for information concerning proper placement and selection of the supply bypass capacitor.
5.	$C_B$	Bypass pin capacitor which provides half-supply filtering. Refer to the section, <b>Proper Selection of Proper Components</b> , for information concerning proper placement and selection of $C_B$ .
6.	$C_o$	Output coupling capacitor which blocks the DC voltage at the amplifier's output. Forms a high pass filter with $R_L$ at $f_o = 1/(2\pi R_L C_o)$ .

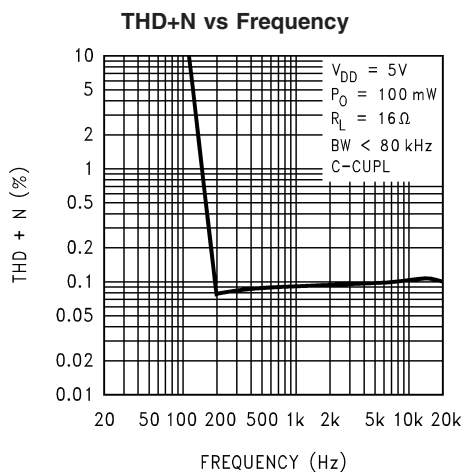
# Typical Performance Characteristics



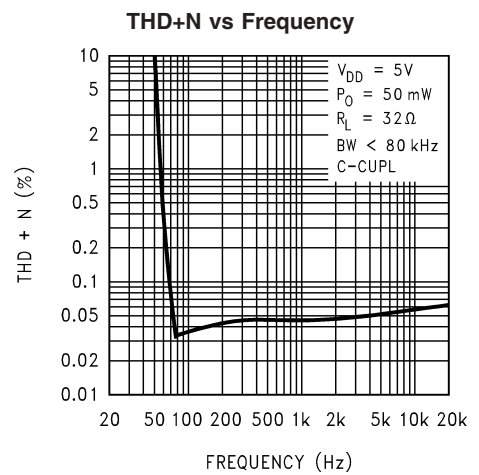
20031482



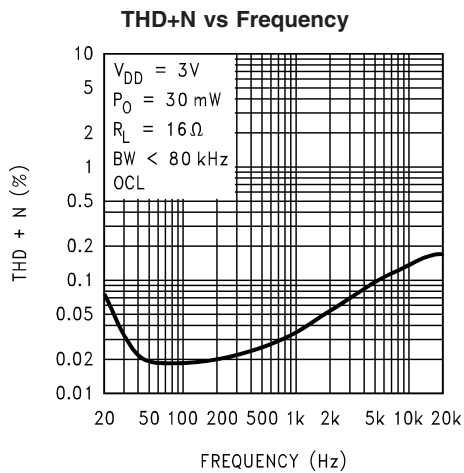
20031483



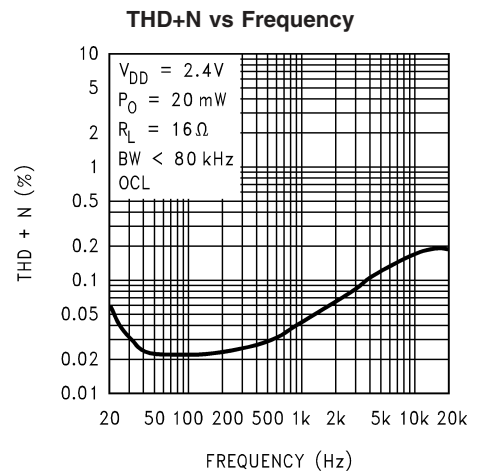
20031484



20031485

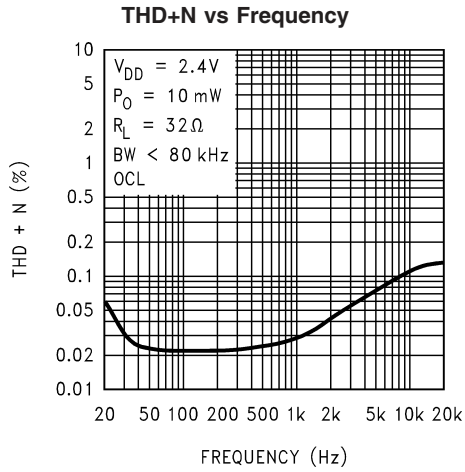


20031406

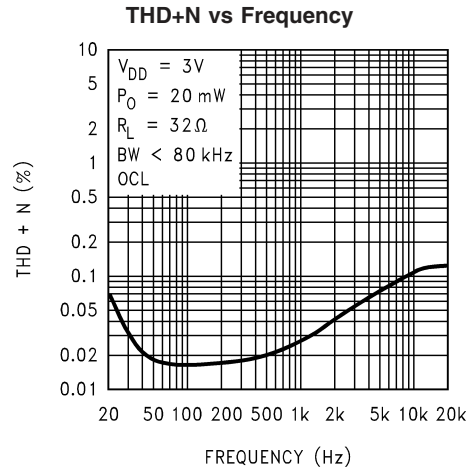


20031403

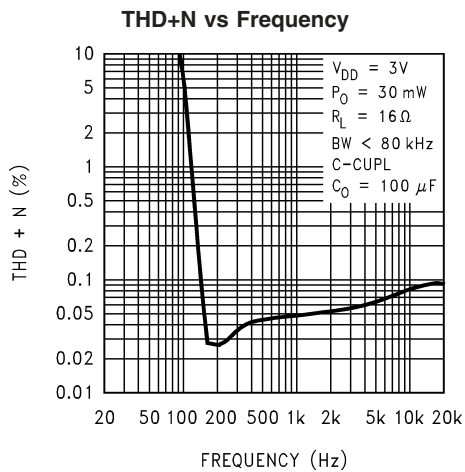
Typical Performance Characteristics (Continued)



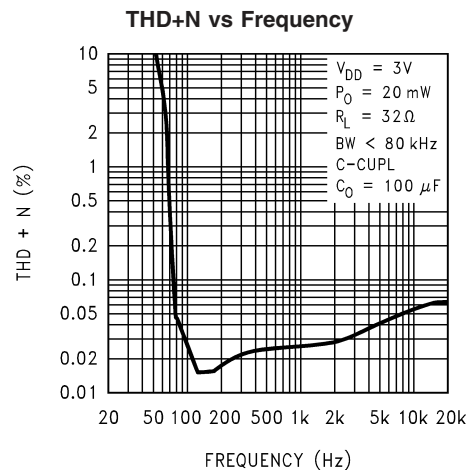
20031405



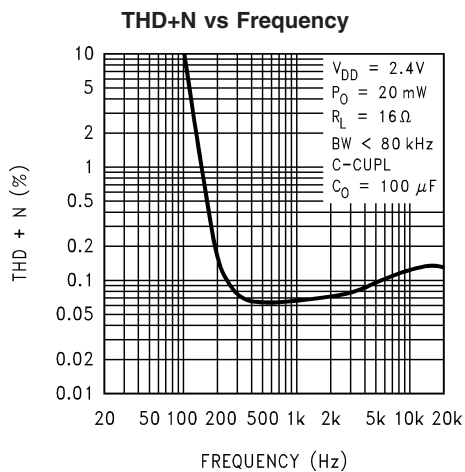
20031404



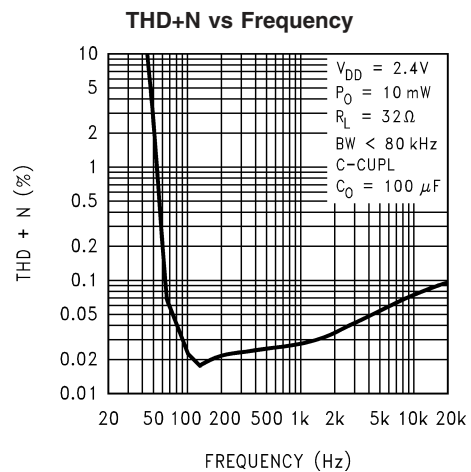
20031486



20031487

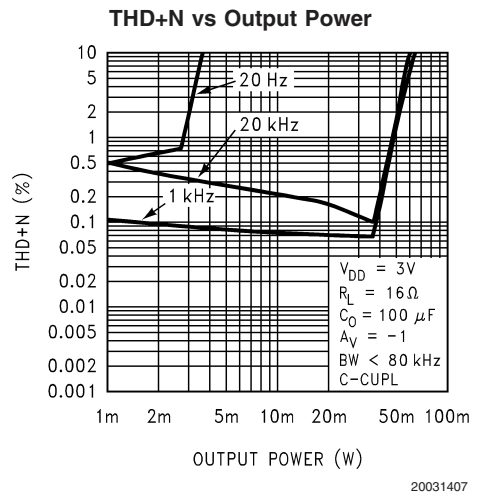
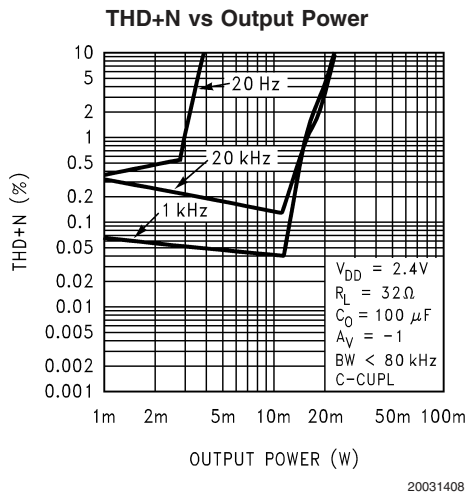
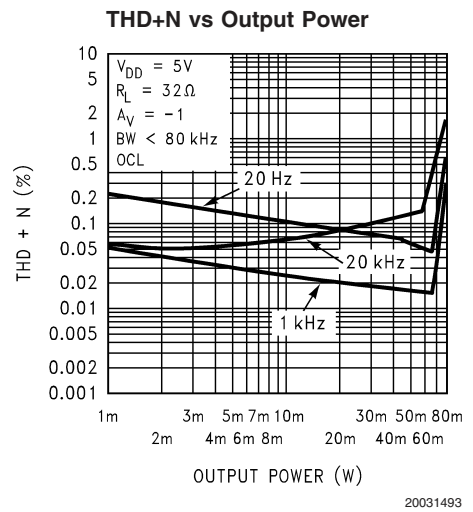
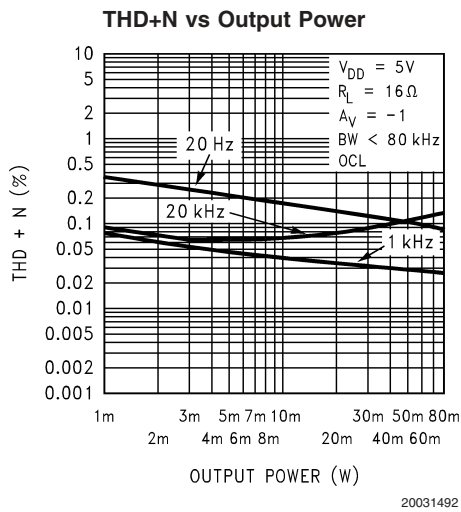
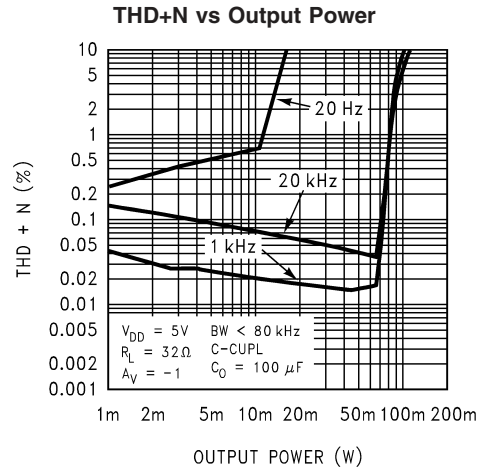
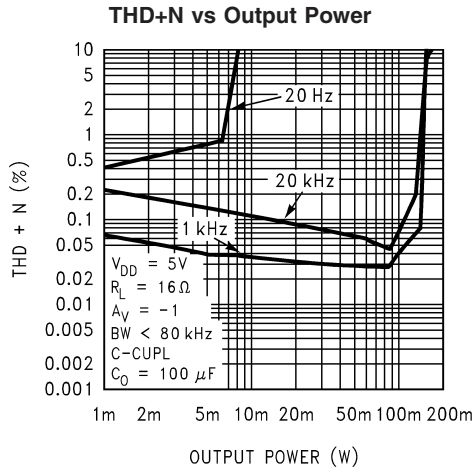


20031488



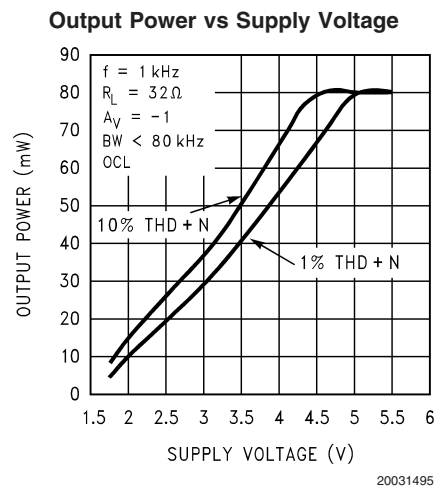
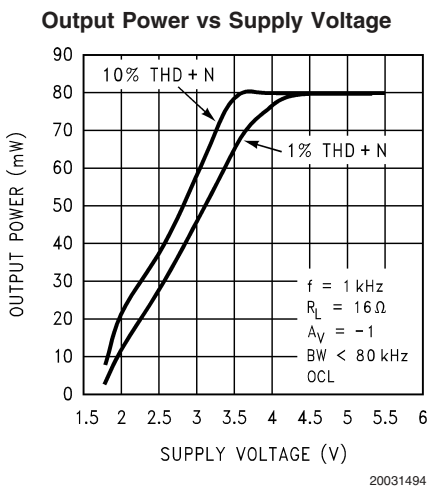
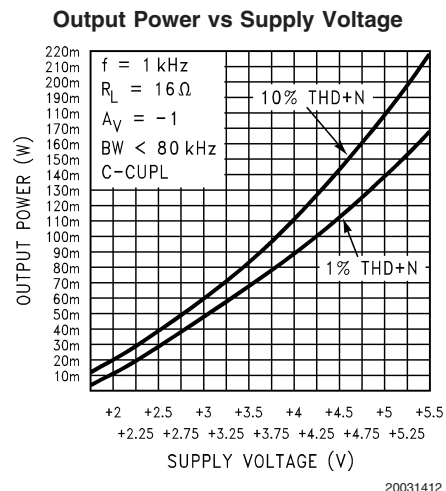
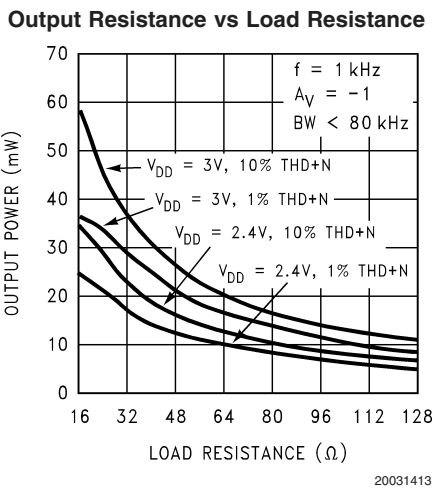
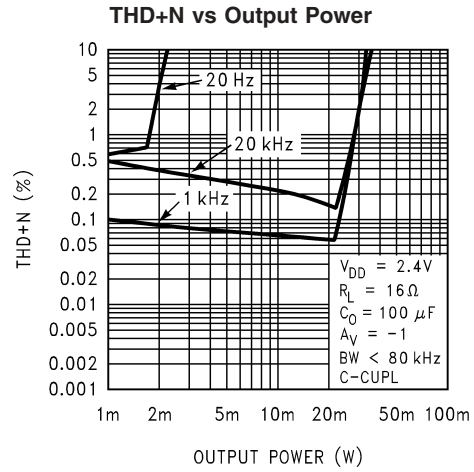
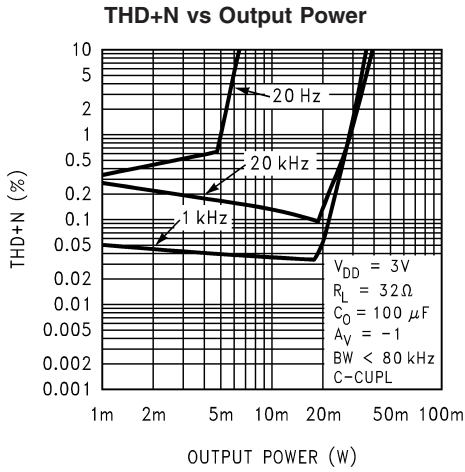
20031489

Typical Performance Characteristics (Continued)



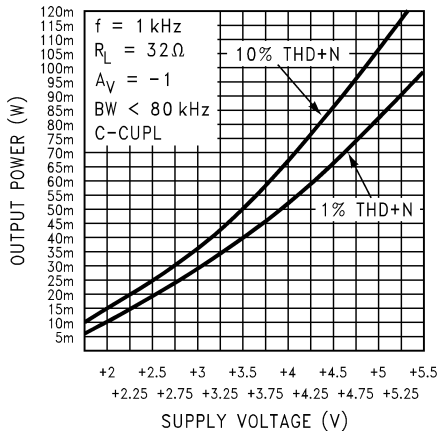


Typical Performance Characteristics (Continued)

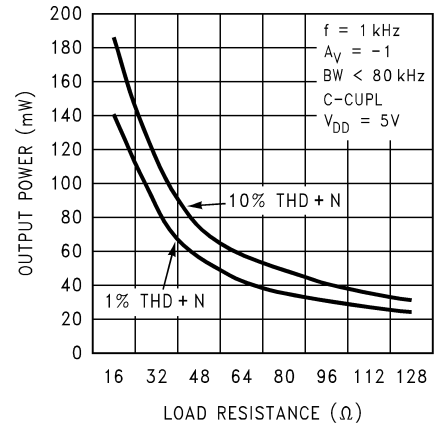


# Typical Performance Characteristics (Continued)

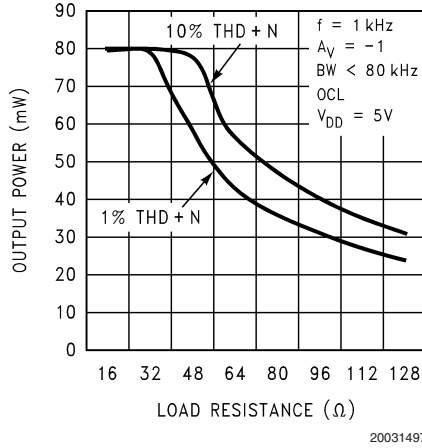
**Output Power vs Supply Voltage**



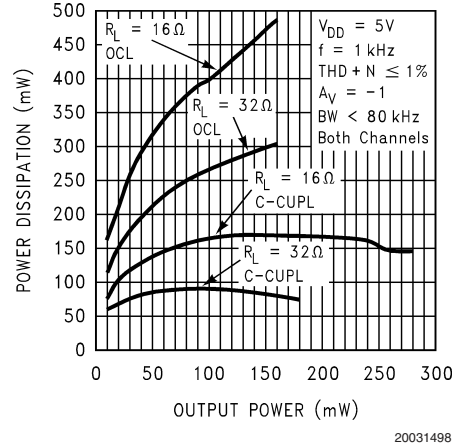
**Output Power vs Load Resistance**



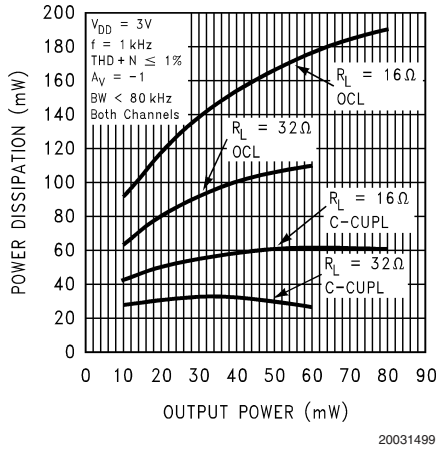
**Output Power vs Load Resistance**



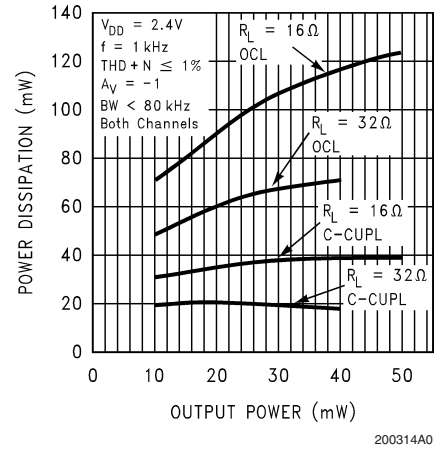
**Power Dissipation vs. Output Power**



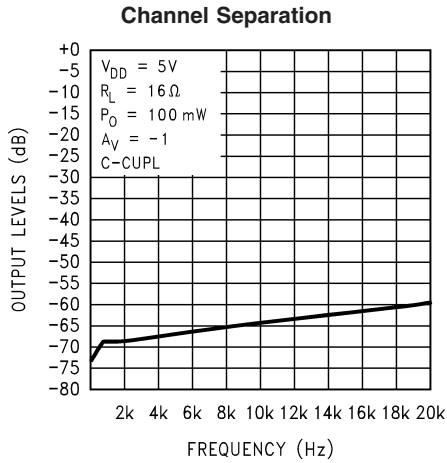
**Power Dissipation vs. Output Power**



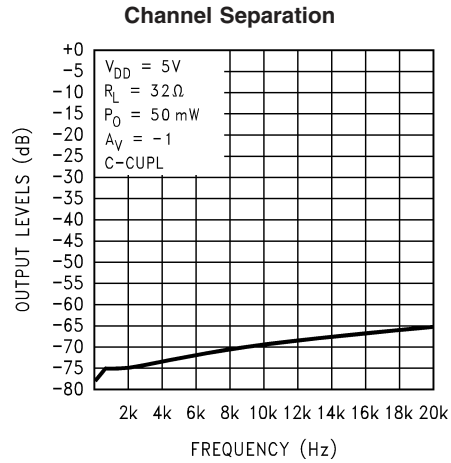
**Power Dissipation vs. Output Power**



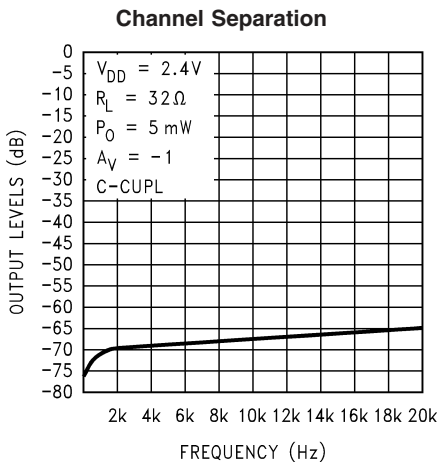
Typical Performance Characteristics (Continued)



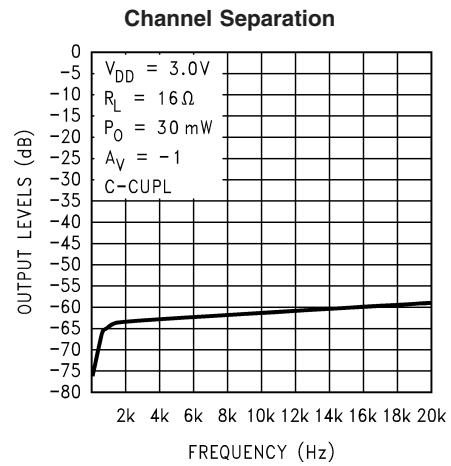
200314A1



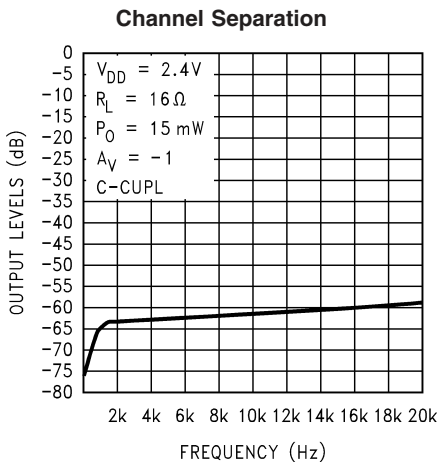
200314A2



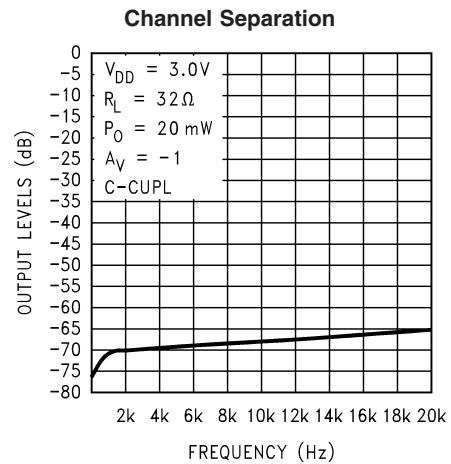
20031417



20031419



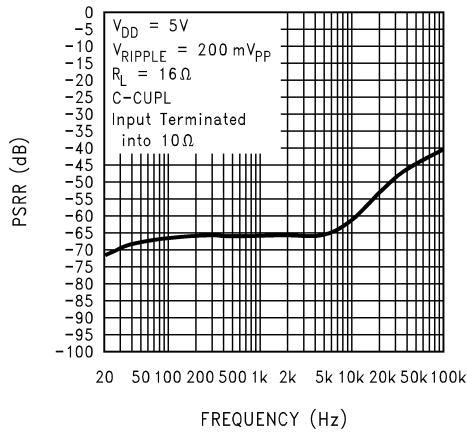
20031418



20031416

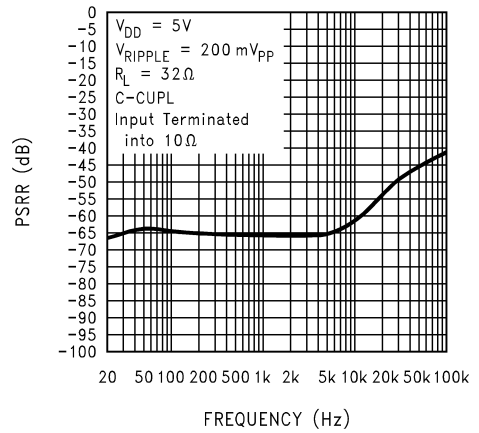
Typical Performance Characteristics (Continued)

Power Supply Rejection Ratio



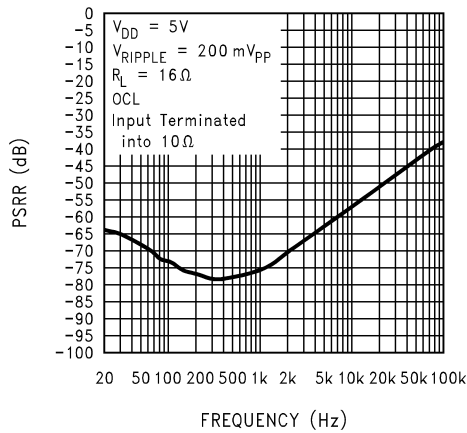
200314A3

Power Supply Rejection Ratio



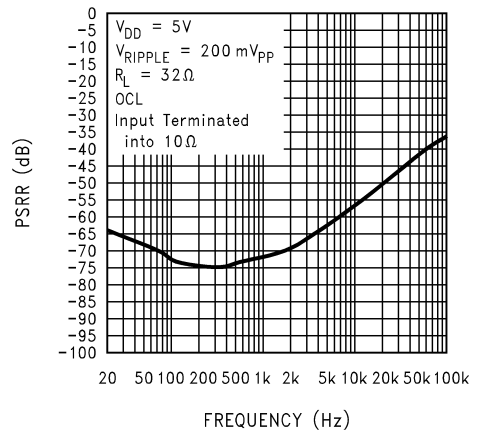
200314A4

Power Supply Rejection Ratio



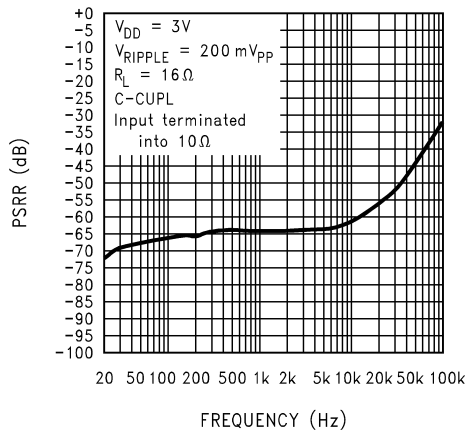
200314A5

Power Supply Rejection Ratio



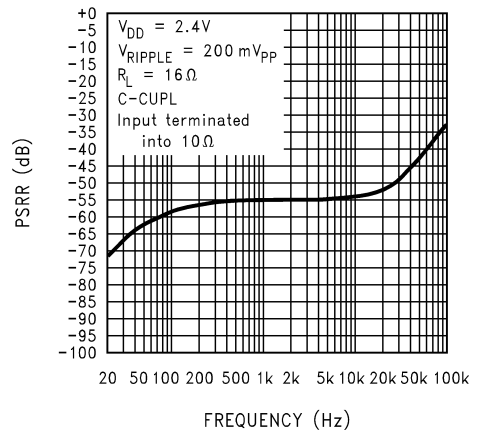
200314A6

Power Supply Rejection Ratio



20031420

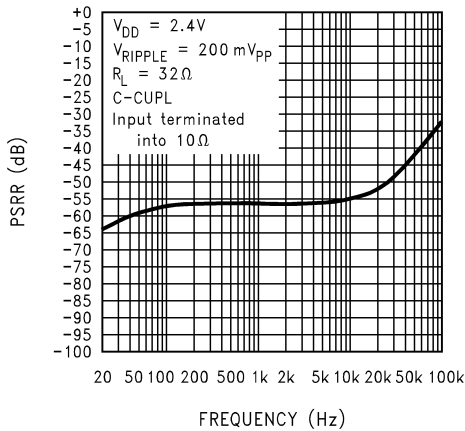
Power Supply Rejection Ratio



20031423

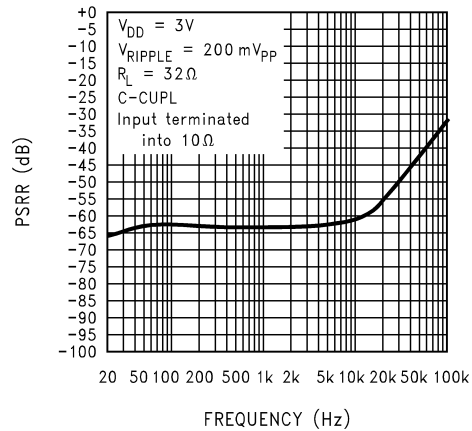
Typical Performance Characteristics (Continued)

Power Supply Rejection Ratio



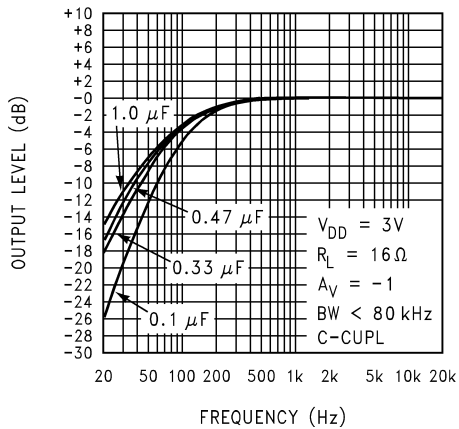
20031421

Power Supply Rejection Ratio



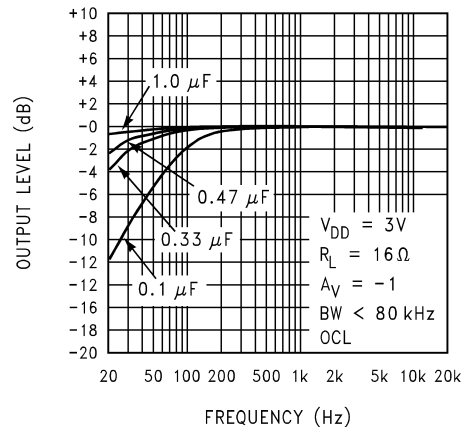
20031422

Frequency Response vs Input Capacitor Size



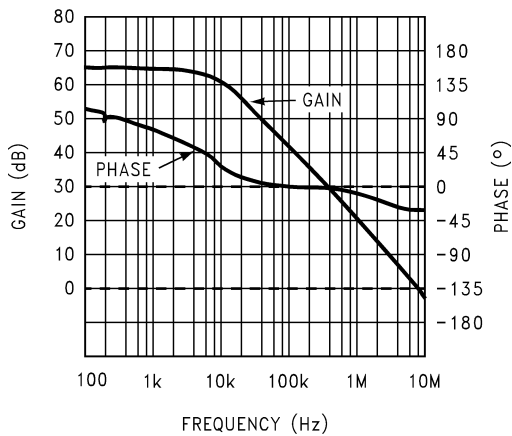
20031427

Frequency Response vs Input Capacitor Size



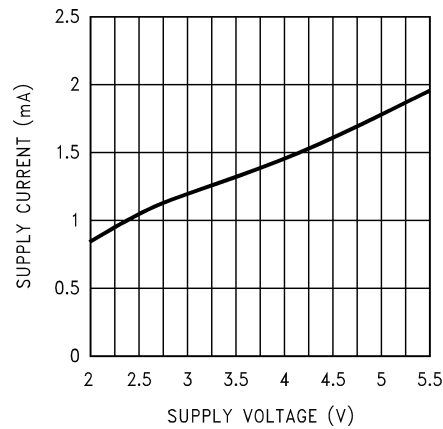
20031426

Open Loop Frequency Response



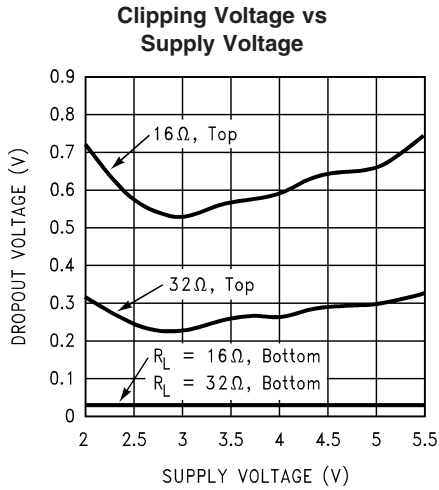
200314A7

Supply Voltage vs Supply Current

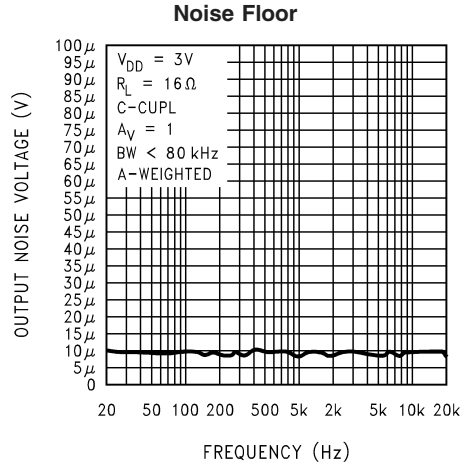


20031424

Typical Performance Characteristics (Continued)

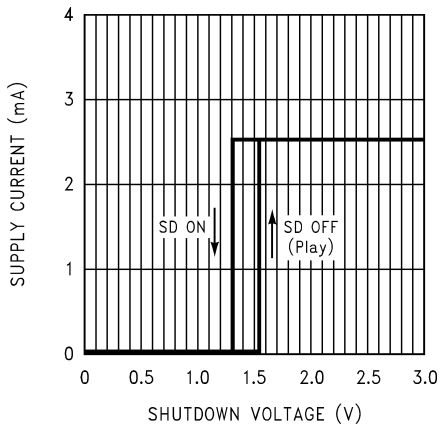


20031425



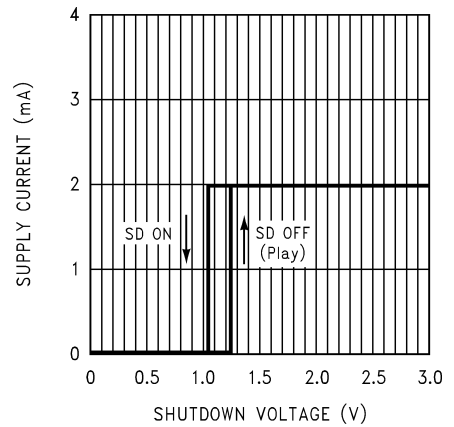
200314A8

Shutdown Hysteresis Voltage, V<sub>DD</sub>=5V



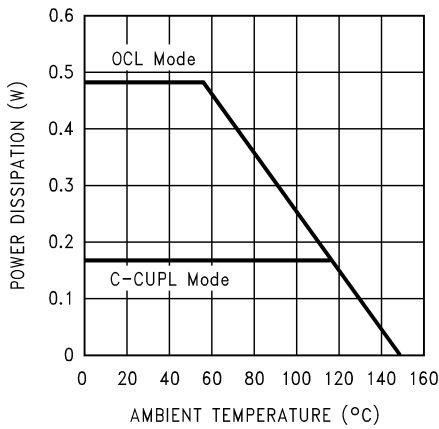
200314B1

Shutdown Hysteresis Voltage, V<sub>DD</sub>=3V



200314B2

Power Derating Curve

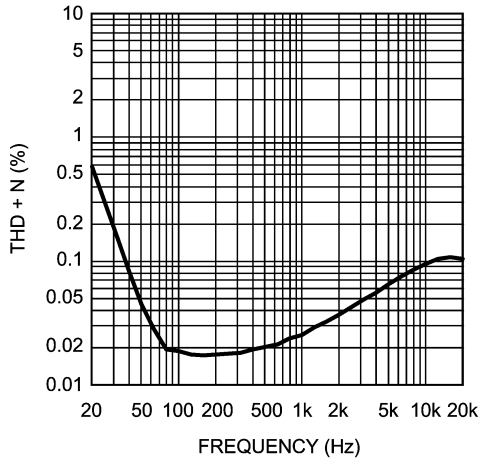


200314B3

# Typical Performance Characteristics

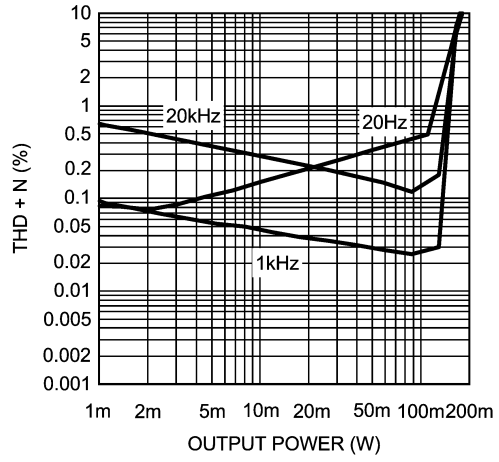
## LM4911LD Specific Characteristics (Note 10)

**THD+N vs Frequency**  
 at  $V_{DD} = 5V$ ,  $R_L = 16\Omega$   
 $P_O = 100mW$ , OCL



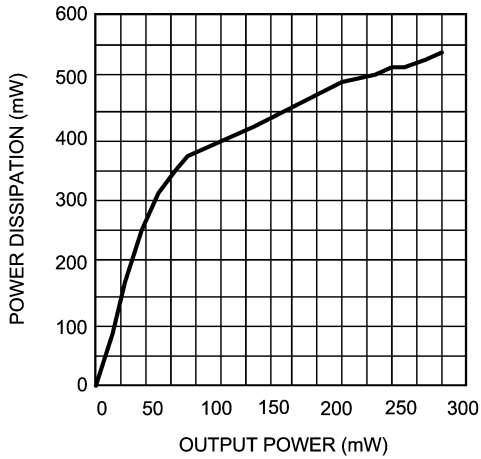
200314B7

**THD+N vs Output Power**  
 at  $V_{DD} = 5V$ ,  $R_L = 16\Omega$ , OCL



200314B8

**Power Dissipation vs Output Power**  
 at  $V_{DD} = 5V$ ,  $R_L = 16\Omega$   
 $THD+N \leq 1\%$ , OCL



200314B9

## Application Information

### AMPLIFIER CONFIGURATION EXPLANATION

As shown in *Figure 1*, the LM4911 has three operational amplifiers internally. Two of the amplifier's have externally configurable gain while the other amplifier is internally fixed at the bias point acting as a unity-gain buffer. The closed-loop gain of the two configurable amplifiers is set by selecting the ratio of  $R_f$  to  $R_i$ . Consequently, the gain for each channel of the IC is

$$A_{VD} = -(R_f / R_i)$$

By driving the loads through outputs  $V_{oA}$  and  $V_{oB}$  with  $V_{oC}$  acting as a buffered bias voltage the LM4911 does not require output coupling capacitors. The classical single-ended amplifier configuration where one side of the load is connected to ground requires large, expensive output coupling capacitors.

A configuration such as the one used in the LM4911 has a major advantage over single supply, single-ended amplifiers. Since the outputs  $V_{oA}$ ,  $V_{oB}$ , and  $V_{oC}$  are all biased at  $1/2 V_{DD}$ , no net DC voltage exists across each load. This eliminates the need for output coupling capacitors which are required in a single-supply, single-ended amplifier configuration. Without output coupling capacitors in a typical single-supply, single-ended amplifier, the bias voltage is placed across the load resulting in both increased internal IC power dissipation and possible loudspeaker damage.

### OUTPUT CAPACITOR vs. CAPACITOR COUPLED

The LM4911 is a stereo audio power amplifier capable of operating in two distinct output modes: capacitor coupled (C-CUPL) or output capacitor-less (OCL). The LM4911 may be run in capacitor coupled mode by using a coupling capacitor on each single-ended output ( $V_{oA}$  and  $V_{oB}$ ) and connecting  $V_{oC}$  to ground. This output coupling capacitor blocks the half supply voltage to which the output amplifiers are typically biased and couples the audio signal to the headphones or other single-ended (SE) load. The signal return to circuit ground is through the headphone jack's sleeve.

The LM4911 can also eliminate these output coupling capacitors by running in OCL mode. Unless shorted to ground,  $V_{oC}$  is internally configured to apply a  $1/2 V_{DD}$  bias voltage to a stereo headphone jack's sleeve. This voltage matches the bias voltage present on  $V_{oA}$  and  $V_{oB}$  outputs that drive the headphones. The headphones operate in a manner similar to a bridge-tied load (BTL). Because the same DC voltage is

applied to both headphone speaker terminals this results in no net DC current flow through the speaker. AC current flows through a headphone speaker as an audio signal's output amplitude increases on the speaker's terminal.

The headphone jack's sleeve is not connected to circuit ground when used in OCL mode. Using the headphone output jack as a line-level output will place the LM4911's  $1/2 V_{DD}$  bias voltage on a plug's sleeve connection. This presents no difficulty when the external equipment uses capacitively coupled inputs. For the very small minority of equipment that is DC coupled, the LM4911 monitors the current supplied by the amplifier that drives the headphone jack's sleeve. If this current exceeds  $500mA_{PK}$ , the amplifier is shutdown, protecting the LM4911 and the external equipment.

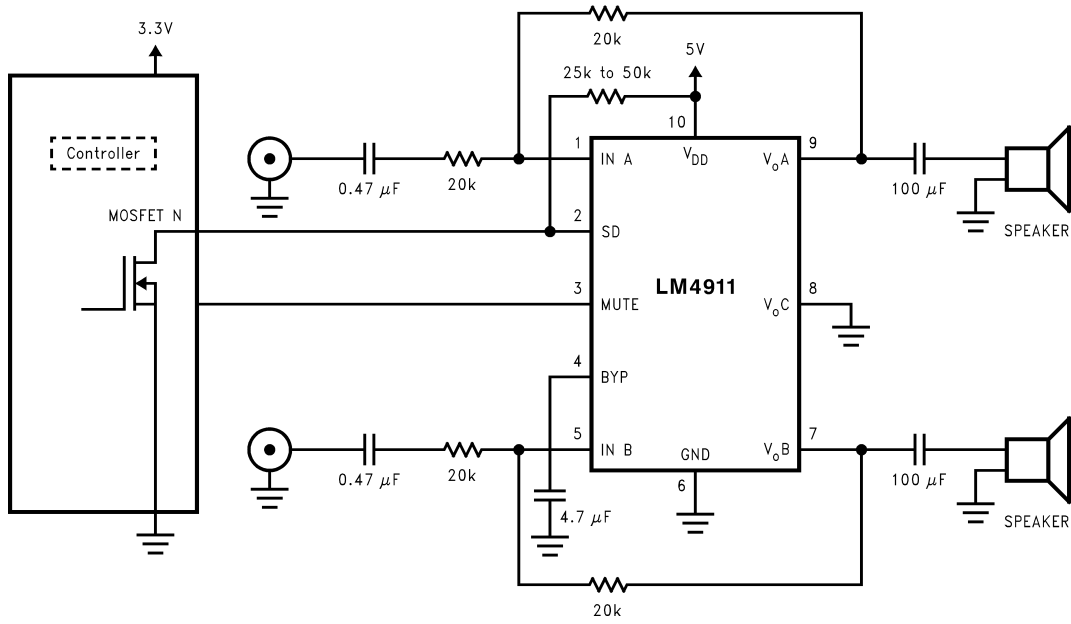
### MODE SELECT DETAIL

The LM4911 may be set up to operate in one of two modes: OCL and cap-coupled. The default state of the LM4911 at power up is cap-coupled. During initial power up or return from shutdown, the LM4911 must detect the correct mode of operation (OCL or cap-coupled) by sensing the status of the  $V_{oC}$  pin. When the bias voltage of the part ramps up to 60mV (as seen on the Bypass pin), an internal comparator detects the status of  $V_{oC}$ ; and at 80mV, latches that value in place. Ramp up of the bias voltage will proceed at a different rate from this point on depending upon operating mode. OCL mode will ramp up about 11 times faster than cap-coupled. Shutdown is not a valid command during this time period ( $T_{WU}$ ) and should not be enabled to ensure a proper power on reset (POR) signal. In addition, the slew rate of  $V_{DD}$  must be greater than 2.5V/ms to ensure reliable POR. Recommended power up timing is shown in *Figure 5* along with proper usage of Shutdown and Mute. The mode select circuit is suspended during  $C_B$  discharge time.

The circuit shown in *Figure 4* presents an applications solution to the problem of using different supply voltages with different turn-on times in a system with the LM4911. This circuit shows the LM4911 with a 25-50k $\Omega$  pull-up resistor connected from the shutdown pin to  $V_{DD}$ . The shutdown pin of the LM4911 is also being driven by an open drain output of an external microcontroller on a separate supply. This circuit ensures that shutdown is disabled when powering up the LM4911 by either allowing shutdown to be high before the LM4911 powers on (the microcontroller powers up first) or allows shutdown to ramp up with  $V_{DD}$  (the LM4911 powers up first). This will ensure the LM4911 powers up properly and enters the correct mode of operation (cap-coupled or OCL).

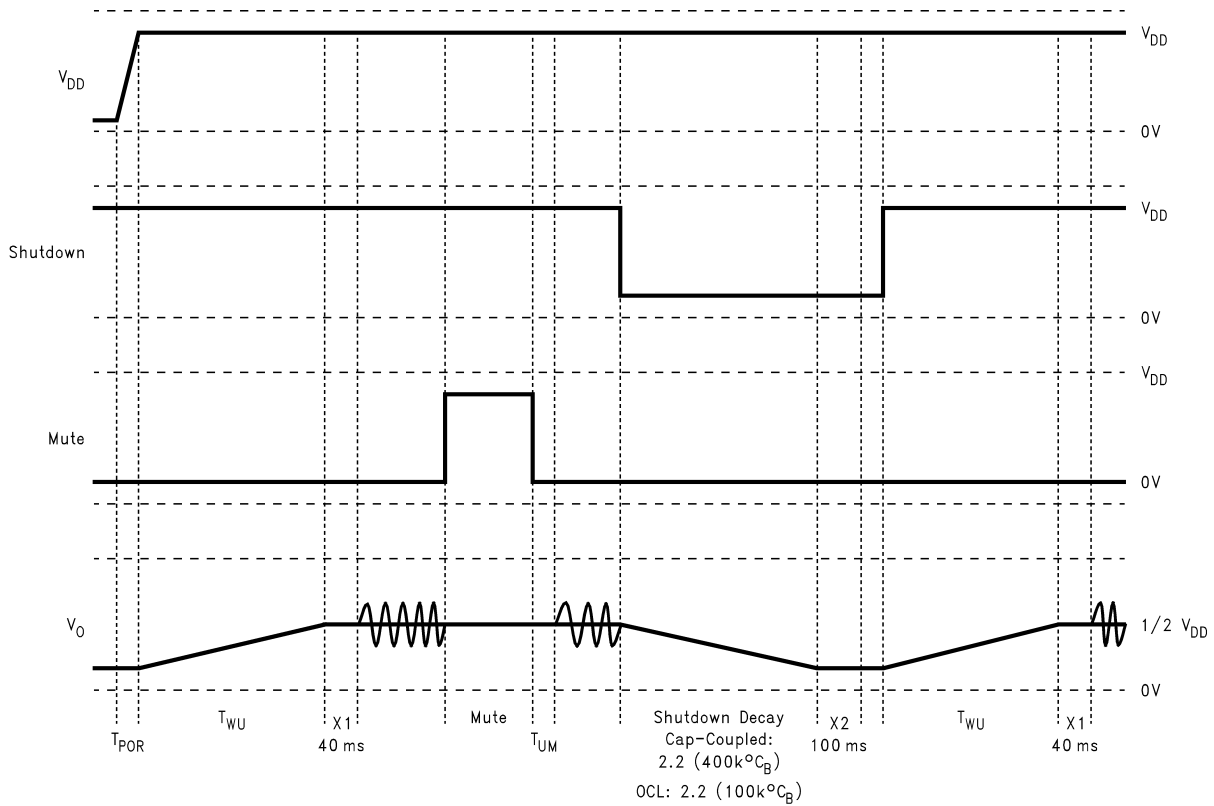


Application Information (Continued)



200314B6

FIGURE 4. Recommended Circuit for Different Supply Turn-On Timing



200314B5

FIGURE 5. Turn-On, Shutdown, and Mute Timing for Cap-Coupled Mode

## Application Information (Continued)

### POWER DISSIPATION

Power dissipation is a major concern when using any power amplifier and must be thoroughly understood to ensure a successful design. When operating in capacitor-coupled mode, Equation 1 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{\text{DMAX}} = (V_{\text{DD}})^2 / (2\pi^2 R_L) \quad (1)$$

Since the LM4911 has two operational amplifiers in one package, the maximum internal power dissipation point is twice that of the number which results from Equation 1. From Equation 1, assuming a 3V power supply and an  $32\Omega$  load, the maximum power dissipation point is 14mW per amplifier. Thus the maximum package dissipation point is 28mW.

When operating in OCL mode, the maximum power dissipation increases due to the use of the third amplifier as a buffer and is given in Equation 2:

$$P_{\text{DMAX}} = 4(V_{\text{DD}})^2 / (\pi^2 R_L) \quad (2)$$

The maximum power dissipation point obtained from either Equation 1 or 2 must not be greater than the power dissipation that results from Equation 3:

$$P_{\text{DMAX}} = (T_{\text{JMAX}} - T_A) / \theta_{\text{JA}} \quad (3)$$

For package MUB10A,  $\theta_{\text{JA}} = 190^\circ\text{C/W}$ ; for package LDA10A,  $\theta_{\text{JA}} = 63^\circ\text{C/W}$ .  $T_{\text{JMAX}} = 150^\circ\text{C}$  for the LM4911. Depending on the ambient temperature,  $T_A$ , of the system surroundings, Equation 3 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 1 or 2 is greater than that of Equation 3, then either the supply voltage must be decreased, the load impedance increased or  $T_A$  reduced. For the typical application of a 3V power supply, with a  $32\Omega$  load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately  $144^\circ\text{C}$  provided that device operation is around the maximum power dissipation point. Thus, for typical applications, power dissipation is not an issue. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature may be increased accordingly. Refer to the Typical Performance Characteristics curves for power dissipation information for lower output powers.

### EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATIONS

The LM4911's exposed-DAP (die attach paddle) package (LD) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane, and surrounding air.

The LD package should have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad may be connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area. Further detailed and specific information concerning PCB

layout, fabrication, and mounting an LD (LLP) package is available from National Semiconductor's Package Engineering Group under application note AN1187.

### POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is important for low noise performance and high power supply rejection. The capacitor location on the power supply pins should be as close to the device as possible.

Typical applications employ a 3V regulator with 10mF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4911. A bypass capacitor value in the range of  $0.1\mu\text{F}$  to  $1\mu\text{F}$  is recommended for  $C_S$ .

### MICRO POWER SHUTDOWN

The voltage applied to the SHUTDOWN pin controls the LM4911's shutdown function. Activate micro-power shutdown by applying a logic-low voltage to the SHUTDOWN pin. When active, the LM4911's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The trigger point varies depending on supply voltage and is shown in the Shutdown Hysteresis Voltage graphs in the Typical Performance Characteristics section. The low  $0.1\mu\text{A}$ (typ) shutdown current is achieved by applying a voltage that is as near as ground as possible to the SHUTDOWN pin. A voltage that is higher than ground may increase the shutdown current. There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external  $100\text{k}\Omega$  pull-up resistor between the SHUTDOWN pin and  $V_{\text{DD}}$ . Connect the switch between the SHUTDOWN pin and ground. Select normal amplifier operation by opening the switch. Closing the switch connects the SHUTDOWN pin to ground, activating micro-power shutdown.

The switch and resistor guarantee that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull-up resistor.

Shutdown enable/disable times are controlled by a combination of  $C_B$  and  $V_{\text{DD}}$ . Larger values of  $C_B$  results in longer turn on/off times from Shutdown. Smaller  $V_{\text{DD}}$  values also increase turn on/off time for a given value of  $C_B$ . Longer shutdown times also improve the LM4911's resistance to click and pop upon entering or returning from shutdown. For a 2.4V supply and  $C_B = 4.7\mu\text{F}$ , the LM4911 requires about 2 seconds to enter or return from shutdown. This longer shutdown time enables the LM4911 to have virtually zero pop and click transients upon entering or release from shutdown.

Smaller values of  $C_B$  will decrease turn-on time, but at the cost of increased pop and click and reduced PSRR. Since shutdown enable/disable times increase dramatically as supply voltage gets below 2.2V, this reduced turn-on time may be desirable if extreme low supply voltage levels are used as this would offset increases in turn-on time caused by the lower supply voltage. This technique is not recommended for OCL mode since shutdown enable/disable times are very fast (0.5s) independent of supply voltage.

When in cap-coupled mode, some restrictions on the usage of Mute are in effect when entering or returning from shutdown. These restrictions require Mute not be toggled immediately following a return or entrance to shutdown for a brief

## Application Information (Continued)

period. These periods are shown as X1 and X2 and are discussed in greater detail in the **Mute** section as well as shown in *Figure 5*.

### MUTE

When in C-CUPL mode, the LM4911 also features a mute function that enables extremely fast turn-on/turn-off with a minimum of output pop and click with a low current consumption ( $\leq 100\mu\text{A}$ ). The mute function leaves the outputs at their bias level, thus resulting in higher power consumption than shutdown mode, but also provides much faster turn on/off times. Mute mode is enabled by providing a logic high signal on the MUTE pin in the opposite manner as the shutdown function described above. Threshold voltages and activation techniques match those given for the shutdown function as well.

Mute may not appear to function when the LM4911 is used to drive high impedance loads. This is because the LM4911 relies on a typical headphone load ( $16\text{-}32\Omega$ ) to reduce input signal feedthrough through the input and feedback resistors. Mute attenuation can thus be calculated by the following formula:

$$\text{Mute Attenuation (dB)} = 20\text{Log}(R_L / (R_i + R_f))$$

Parallel load resistance may be necessary to achieve satisfactory Mute levels when the application load is known to be high impedance.

The mute function is not necessary when the LM4911 is operating in OCL mode since the shutdown function operates quickly in OCL mode with less power consumption than mute.

Mute may be enabled during shutdown transitions, but should not be toggled for a brief period immediately after exiting or entering shutdown. These brief time periods are labeled X1 (time after returning from shutdown) and X2 (time after entering shutdown) and are shown in the timing diagram given in *Figure 5*. X1 occurs immediately following a return from shutdown ( $T_{WU}$ ) and lasts  $40\text{ms} \pm 25\%$ . X2 occurs after the part is placed in shutdown and the decay of the bias voltage has occurred ( $2.2 \cdot 400\text{k} \cdot C_B$  for cap-coupled and  $2.2 \cdot 100\text{k} \cdot C_B$  for OCL) and lasts for  $100\text{ms} \pm 25\%$ . The timing of these transition periods relative to X1 and X2 is also shown in *Figure 5*. Mute should not be toggled during these time periods, but may be made during the shutdown transitions or any other time the part is in normal operation (while in cap-coupled mode - Mute is not valid in OCL mode). Failure to operate mute correctly may result in much higher click and pop values or failure of the device to mute at all.

### PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4911 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4911 is unity-gain stable which gives the designer maximum system flexibility. The LM4911 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than  $1V_{\text{rms}}$  are available

from sources such as audio codecs. Very large values should not be used for the gain-setting resistors. Values for  $R_i$  and  $R_f$  should be less than  $1\text{M}\Omega$ . Please refer to the section, **Audio Power Amplifier Design**, for a more complete explanation of proper gain selection

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in *Figure 2* and *Figure 3*. The input coupling capacitor,  $C_i$ , forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response and turn-on time.

### SELECTION OF INPUT CAPACITOR SIZE

Amplifying the lowest audio frequencies requires a high value input coupling capacitor,  $C_i$ . A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the headphones used in portable systems have little ability to reproduce signals below  $60\text{Hz}$ . Applications using headphones with this limited frequency response reap little improvement by using a high value input capacitor.

In addition to system cost and size, turn on time is affected by the size of the input coupling capacitor  $C_i$ . A larger input coupling capacitor requires more charge to reach its quiescent DC voltage. This charge comes from the output via the feedback. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on time can be minimized. A small value of  $C_i$  (in the range of  $0.1\mu\text{F}$  to  $0.39\mu\text{F}$ ), is recommended.

### AUDIO POWER AMPLIFIER DESIGN

#### A 25mW/32Ω AUDIO AMPLIFIER

Given:

Power Output	25mWrms
Load Impedance	32Ω
Input Level	1Vrms
Input Impedance	20kΩ

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the **Typical Performance Characteristics** section, the supply rail can be easily found.

3V is a standard voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4911 to reproduce peak in excess of 25mW without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the **Power Dissipation** section.

Once the power dissipation equations have been addressed, the required gain can be determined from Equation 2.

$$A_V \geq \sqrt{(P_O R_L) / (V_{IN})} = V_{\text{orms}} / V_{\text{inrms}} \quad (4)$$

From Equation 4, the minimum  $A_V$  is 0.89; use  $A_V = 1$ . Since the desired input impedance is  $20\text{k}\Omega$ , and with a  $A_V$  gain of 1, a ratio of 1:1 results from Equation 1 for  $R_f$  to  $R_i$ . The values are chosen with  $R_i = 20\text{k}\Omega$  and  $R_f = 20\text{k}\Omega$ . The final design step is to address the bandwidth requirements which

## Application Information (Continued)

must be stated as a pair of -3dB frequency points. Five times away from a -3dB point is 0.17dB down from passband response which is better than the required  $\pm 0.25$ dB specified.

$$f_L = 100\text{Hz}/5 = 20\text{Hz}$$

$$f_H = 20\text{kHz} * 5 = 100\text{kHz}$$

As stated in the **External Components** section,  $R_i$  in conjunction with  $C_i$  creates a

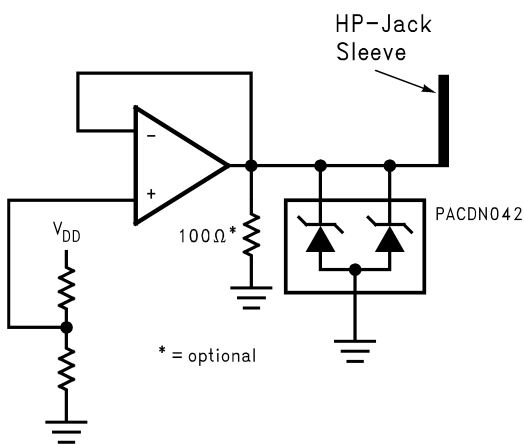
$$C_i \geq 1 / (2\pi * 20\text{k}\Omega * 20\text{Hz}) = 0.397\mu\text{F}; \text{ use } 0.39\mu\text{F}.$$

The high frequency pole is determined by the product of the desired frequency pole,  $f_H$ , and the differential gain,  $A_V$ . With an  $A_V = 1$  and  $f_H = 100\text{kHz}$ , the resulting GBWP = 100kHz which is much smaller than the LM4911 GBWP of 10MHz. This figure displays that is a designer has a need to design an amplifier with higher differential gain, the LM4911 can still be used without running into bandwidth limitations.

Figure 4 shows an optional resistor connected between the amplifier output that drives the headphone jack sleeve and ground. This resistor provides a ground path that suppressed power supply hum. This hum may occur in applications such as notebook computers in a shutdown condition and connected to an external powered speaker. The resistor's 100 $\Omega$  value is a suggested starting point. Its final value must be determined based on the tradeoff between the amount of noise suppression that may be needed and minimizing the additional current drawn by the resistor (25mA for a 100 $\Omega$  resistor and a 5V supply).

### ESD PROTECTION

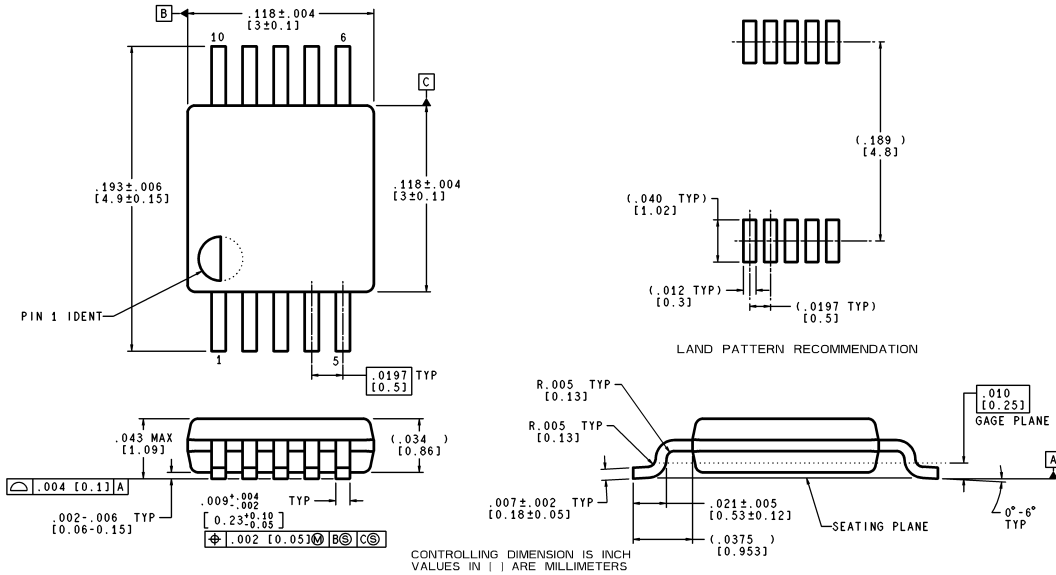
As stated in the Absolute Maximum Ratings, the LM4911 has a maximum ESD susceptibility rating of 2000V. For higher ESD voltages, the addition of a PCDN042 dual transil (from California Micro Devices), as shown in Figure 6, will provide additional protection.



200314B4

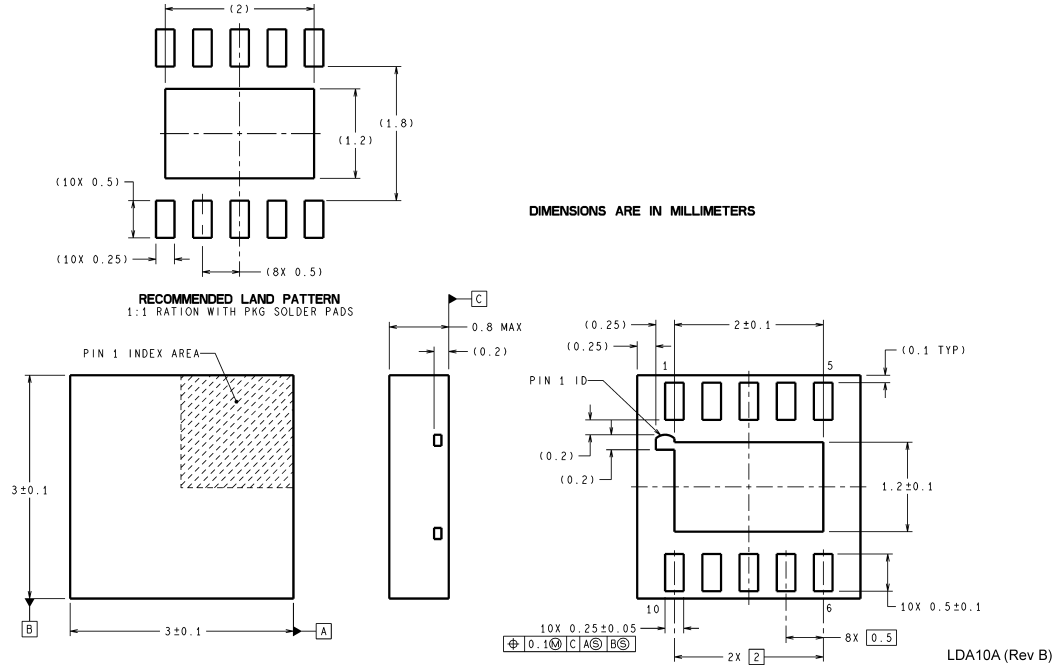
**FIGURE 6. The PCDN042 provides additional ESD protection beyond the 2000V shown in the Absolute Maximum Ratings for the  $V_{OC}$  output**

**Physical Dimensions** inches (millimeters) unless otherwise noted



MUB10A (Rev A)

**MSOP**  
**Order Number LM4911MM**  
**NS Package Number MUB10A**



LDA10A (Rev B)

**LLP**  
**Order Number LM4911LD**  
**NS Package Number LDA10A**

## Notes

### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



**National Semiconductor**  
Americas Customer  
Support Center  
Email: [new.feedback@nsc.com](mailto:new.feedback@nsc.com)  
Tel: 1-800-272-9959

[www.national.com](http://www.national.com)

**National Semiconductor**  
Europe Customer Support Center  
Fax: +49 (0) 180-530 85 86  
Email: [europa.support@nsc.com](mailto:europa.support@nsc.com)  
Deutsch Tel: +49 (0) 69 9508 6208  
English Tel: +44 (0) 870 24 0 2171  
Français Tel: +33 (0) 1 41 91 8790

**National Semiconductor**  
Asia Pacific Customer  
Support Center  
Fax: 65-6250 4466  
Email: [ap.support@nsc.com](mailto:ap.support@nsc.com)  
Tel: 65-6254 4466

**National Semiconductor**  
Japan Customer Support Center  
Fax: 81-3-5639-7507  
Email: [nsj.crc@jksmtp.nsc.com](mailto:nsj.crc@jksmtp.nsc.com)  
Tel: 81-3-5639-7560