February 2005

National Semiconductor

LM5105
100V Half Bridge Gate Driver with Programmable Dead-time

General Description

The LM5105 is a high voltage gate driver designed to drive both the high side and low side N –Channel MOSFETs in a synchronous buck or half bridge configuration. The floating high-side driver is capable of working with rail voltages up to 100V. The single control input is compatible with TTL signal levels and a single external resistor programs the switching transition dead-time through tightly matched turn-on delay circuits. A high voltage diode is provided to charge the high side gate drive bootstrap capacitor. The robust level shift technology operates at high speed while consuming low power and provides clean output transitions. Under-voltage lockout disables the gate driver when either the low side or the bootstrapped high side supply voltage is below the operating threshold. The LM5105 is offered in the thermally enhanced 10-pin LLP plastic package.

Features

- Drives both a high side and low side N-channel MOSFET
- 1.8A peak gate drive current
- Bootstrap supply voltage range up to 118V DC
- Integrated bootstrap diode
- Single TTL compatible Input
- Programmable turn-on delays (Dead-time)
- Enable Input pin
- Fast turn-off propagation delays (26ns typical)
- Drives 1000pF with 15ns rise and fall time
- Supply rail under-voltage lockout
- Low power consumption

Typical Applications

- Solid State motor drives
- Half and Full Bridge power converters
- Two switch forward power converters

Package

- LLP-10 (4 mm x 4 mm)

Simplified Block Diagram

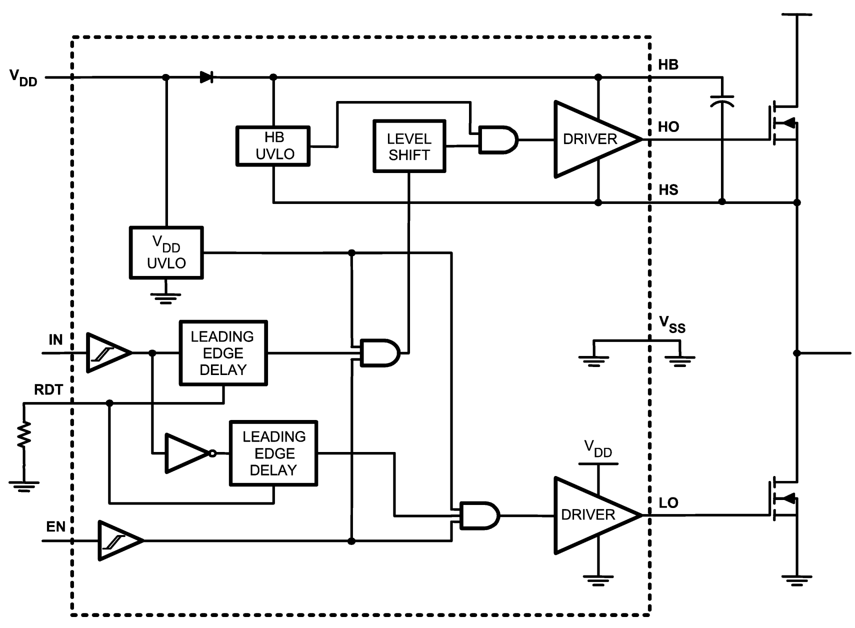
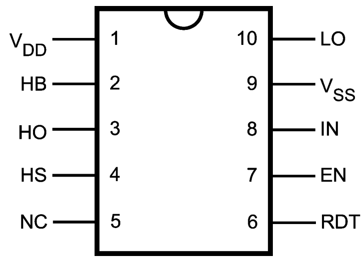


FIGURE 1.

Connection Diagram



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10-Lead LLP
See NS Number SDC10A

Ordering Information

Ordering Number	Package Type	NSC Package Drawing	Supplied As
LM5105SD	LLP-10	SDC10A	1000 shipped as Tape & Reel
LM5105SDX	LLP-10	SDC10A	4500 shipped as Tape & Reel

Pin Descriptions

Pin	Name	Description	Application Information
1	V_{DD}	Positive gate drive supply	Decouple VDD to VSS using a low ESR/ESL capacitor, placed as close to the IC as possible.
2	HB	High side gate driver bootstrap rail	Connect the positive terminal of bootstrap capacitor to the HB pin and connect negative terminal to HS. The Bootstrap capacitor should be placed as close to IC as possible.
3	HO	High side gate driver output	Connect to the gate of high side N-MOS device through a short, low inductance path.
4	HS	High side MOSFET source connection	Connect to the negative terminal of the bootststrap capacitor and to the source of the high side N-MOS device.
5	NC	Not Connected	
6	RDT	Deadtime programming pin	A resistor from RDT to VSS programs the turn-on delay of both the high and low side MOSFETs. The resistor should be placed close to the IC to minimize noise coupling from adjacent PC board traces.
7	EN	Logic input for driver Disable/Enable	TTL compatible threshold with hysteresis. LO and HO are held in the low state when EN is low.
8	IN	Logic input for gate driver	TTL compatible threshold with hysteresis. The high side MOSFET is turned on and the low side MOSFET turned off when IN is high.
9	V_{SS}	Ground return	All signals are referenced to this ground.
10	LO	Low side gate driver output	Connect to the gate of the low side N-MOS device with a short, low inductance path.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{DD} to V_{SS}	−0.3V to +18V
HB to HS	−0.3V to +18V
IN and EN to V_{SS}	−0.3V to V_{DD} + 0.3V
LO to V_{SS}	−0.3V to V_{DD} + 0.3V
HO to V_{SS}	HS − 0.3V to HB + 0.3V
HS to V_{SS} (Note 6)	−5V to +100V
HB to V_{SS}	118V
RDT to V_{SS}	−0.3V to 5V
Junction Temperature	+150˚C
Storage Temperature Range	−55˚C to +150˚C
ESD Rating HBM (Note 2)	2 kV

Recommended Operating Conditions

V_{DD}	+8V to +14V
HS (Note 6)	−1V to 100V
HB	HS + 8V to HS + 14V
HS Slew Rate	<50V/ns
Junction Temperature	−40˚C to +125˚C

Electrical Characteristics

Specifications in standard typeface are for T_J = +25˚C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = HB = 12V, V_{SS} = HS = 0V, EN = 5V. No load on LO or HO. RDT= 100kΩ(Note 4).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SUPPLY CURRENTS						
I_{DD}	V_{DD} Quiescent Current	IN = EN = 0V		0.34	**0.6**	mA
I_{DDO}	V_{DD} Operating Current	f = 500 kHz		1.65	**3**	mA
I_{HB}	Total HB Quiescent Current	IN = EN = 0V		0.06	**0.2**	mA
I_{HBO}	Total HB Operating Current	f = 500 kHz		1.3	**3**	mA
I_{HBS}	HB to V_{SS} Current, Quiescent	HS = HB = 100V		0.05	**10**	µA
I_{HBSO}	HB to V_{SS} Current, Operating	f = 500 kHz		0.1		mA
INPUT IN and EN						
V_{IL}	Low Level Input Voltage Threshold		**0.8**	1.8		V
V_{IH}	High Level Input Voltage Threshold			1.8	**2.2**	V
R_{pd}	Input Pulldown Resistance Pin IN and EN		**100**	200	**500**	kΩ
DEAD-TIME CONTROLS						
VRDT	Nominal Voltage at RDT		**2.7**	3	**3.3**	V
IRDT	RDT Pin Current Limit	RDT = 0V	**0.75**	1.5	**2.25**	mA
UNDER VOLTAGE PROTECTION						
V_{DDR}	V_{DD} Rising Threshold		**6.0**	6.9	**7.4**	V
V_{DDH}	V_{DD} Threshold Hysteresis			0.5		V
V_{HBR}	HB Rising Threshold		**5.7**	6.6	**7.1**	V
V_{HBH}	HB Threshold Hysteresis			0.4		V
BOOT STRAP DIODE						
V_{DL}	Low-Current Forward Voltage	I_{VDD-HB} = 100 µA		0.6	**0.9**	V
V_{DH}	High-Current Forward Voltage	I_{VDD-HB} = 100 mA		0.85	**1.1**	V
R_D	Dynamic Resistance	I_{VDD-HB} = 100 mA		0.8	**1.5**	Ω
LO GATE DRIVER						
V_{OLL}	Low-Level Output Voltage	I_{LO} = 100 mA		0.25	**0.4**	V
V_{OHL}	High-Level Output Voltage	I_{LO} = −100 mA, V_{OHL} = V_{DD} − V_{LO}		0.35	**0.55**	V
I_{OHL}	Peak Pullup Current	LO = 0V		1.8		A
I_{OLL}	Peak Pulldown Current	LO = 12V		1.6		A
HO GATE DRIVER						
V_{OLH}	Low-Level Output Voltage	I_{HO} = 100 mA		0.25	**0.4**	V
V_{OHH}	High-Level Output Voltage	I_{HO} = −100 mA, V_{OHH} = HB − HO		0.35	**0.55**	V
I_{OHH}	Peak Pullup Current	HO = 0V		1.8		A

Electrical Characteristics

Specifications in standard typeface are for T_J = +25˚C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = HB = 12V, V_{SS} = HS = 0V, EN = 5V. No load on LO or HO. RDT= 100kΩ(Note 4). (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OLH}	Peak Pulldown Current	HO = 12V		1.6		A
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient	(Note 3), (Note 5)		40		˚C/W

Switching Characteristics

Specifications in standard typeface are for T_J = +25˚C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = HB = 12V, V_{SS} = HS = 0V, No Load on LO or HO (Note 4).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LPHL}	Lower Turn-Off Propagation Delay			26	**56**	ns
t_{HPHL}	Upper Turn-Off Propagation Delay			26	**56**	ns
t_{LPLH}	Lower Turn-On Propagation Delay	RDT = 100k	**485**	595	**705**	ns
t_{HPLH}	Upper Turn-On Propagation Delay	RDT = 100k	**485**	595	**705**	ns
t_{LPLH}	Lower Turn-On Propagation Delay	RDT = 10k	**75**	105	**150**	ns
t_{HPLH}	Upper Turn-On Propagation Delay	RDT = 10k	**75**	105	**150**	ns
t_{en}, t_{sd}	Enable and Shutdown propagation delay			28		ns
DT1, DT2	Dead-time LO OFF to HO ON & HO OFF to LO ON	RDT = 100k		570		µs
		RDT = 10k		80		
MDT	Dead-time matching	RDT = 100k		50		
t_R, t_F	Either Output Rise/Fall Time	C_L = 1000pF		15		
t_{BS}	Bootstrap Diode Turn-On or Turn-Off Time	I_F = 20 mA, I_R = 200 mA		50		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. Pin 2, Pin 3 and Pin 4 are rated at 500V.

Note 3: 4 layer board with Cu finished thickness 1.5/1.0/1.0/1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50 x 50mm ground and power planes embedded in PCB. See Application Note AN-1187.

Note 4: Min and Max limits are 100% production tested at 25˚C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

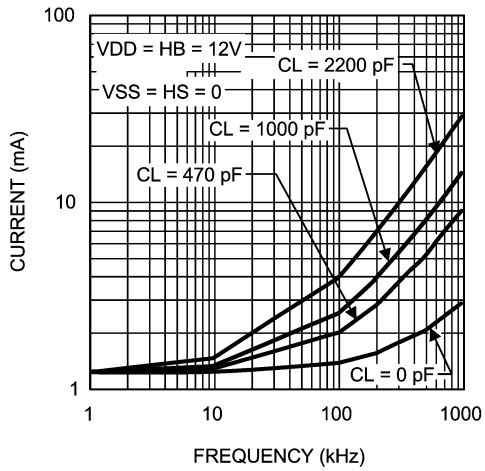
Note 5: The θ_{JA} is not a constant for the package and depends on the printed circuit board design and the operating conditions.

Note 6: In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed -1V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently.

If negative transients occur on HS, the HS voltage must never be more negative than V_{DD} - 15V. For example, if V_{DD} = 10V, the negative transients at HS must not exceed -5V.

Typical Performance Characteristics

V_{DD} Operating Current vs Frequency



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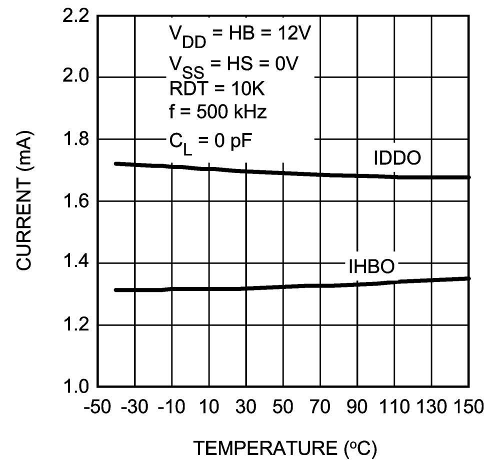
Operating Current vs Temperature



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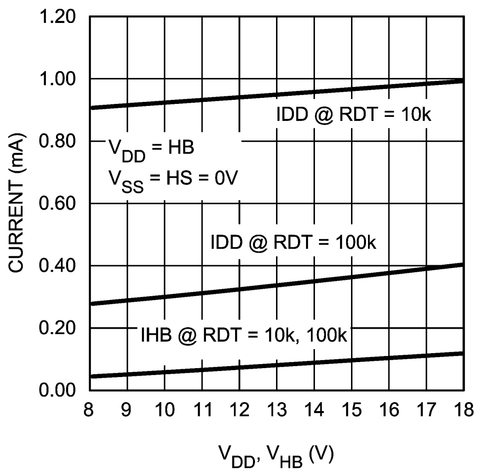
Quiescent Current vs Supply Voltage



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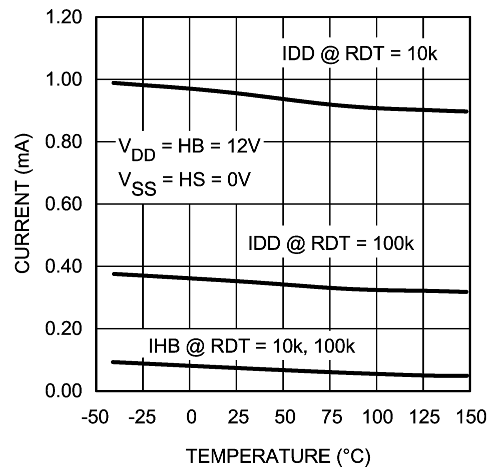
Quiescent Current vs Temperature



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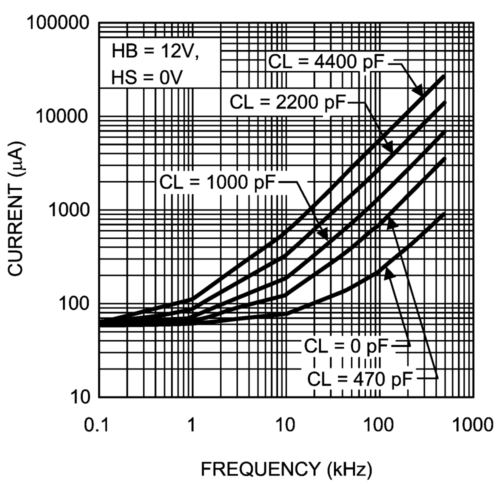
HB Operating Current vs Frequency



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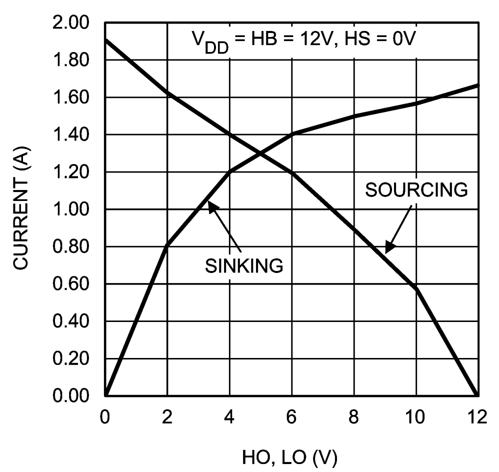
HO & LO Peak Output Current vs Output Voltage



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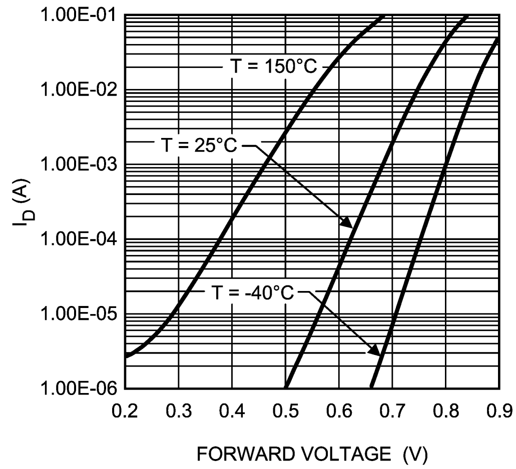
Typical Performance Characteristics (Continued)

Diode Forward Voltage



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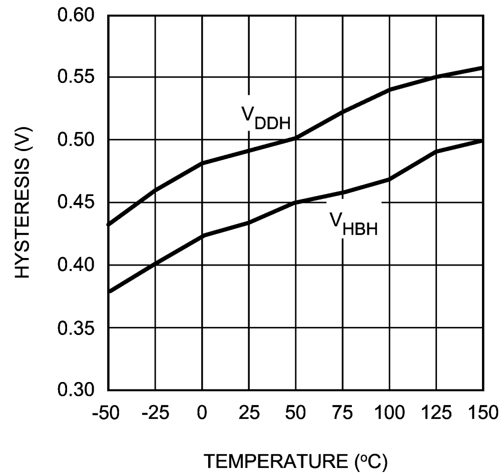
Undervoltage Hysteresis vs Temperature



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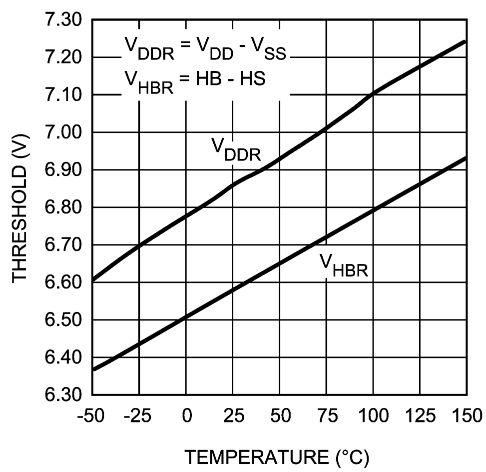
Undervoltage Rising Threshold vs Temperature



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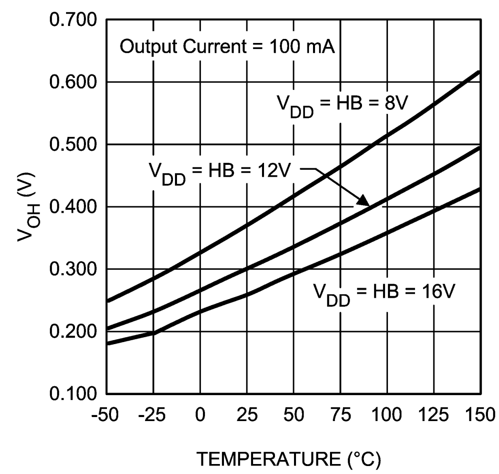
LO & HO - High Level Output Voltage vs Temperature



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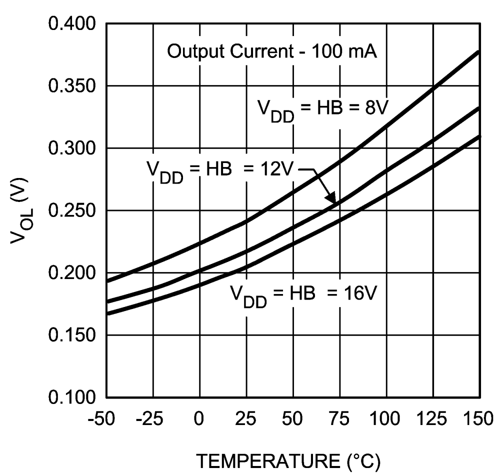
LO & HO - Low Level Output Voltage vs Temperature



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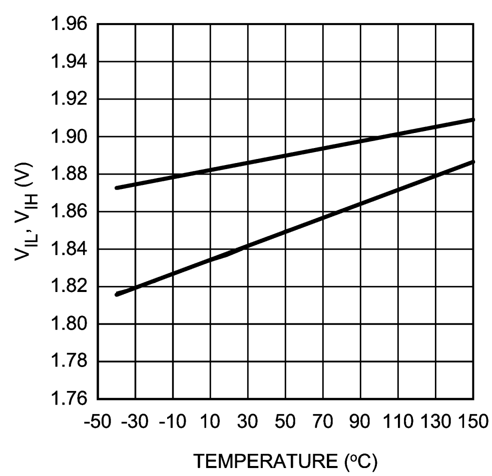
Input Threshold vs Temperature



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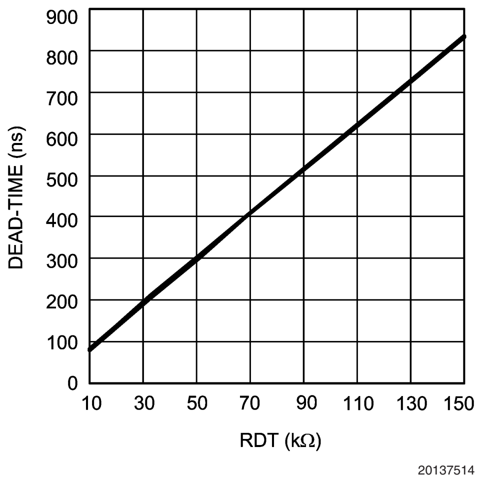
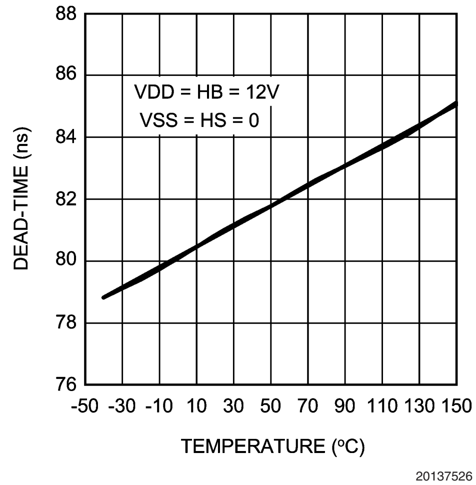
Typical Performance Characteristics (Continued)

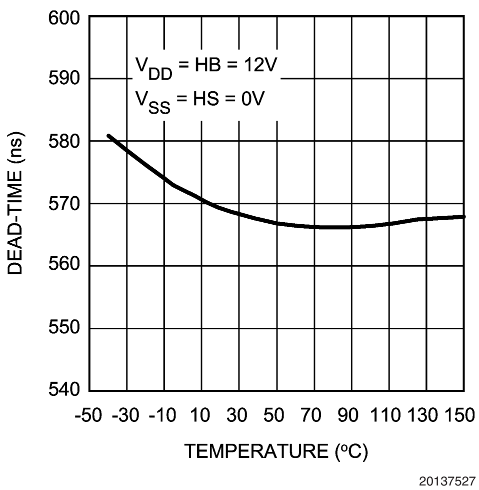
Dead-Time vs RT Resistor Value



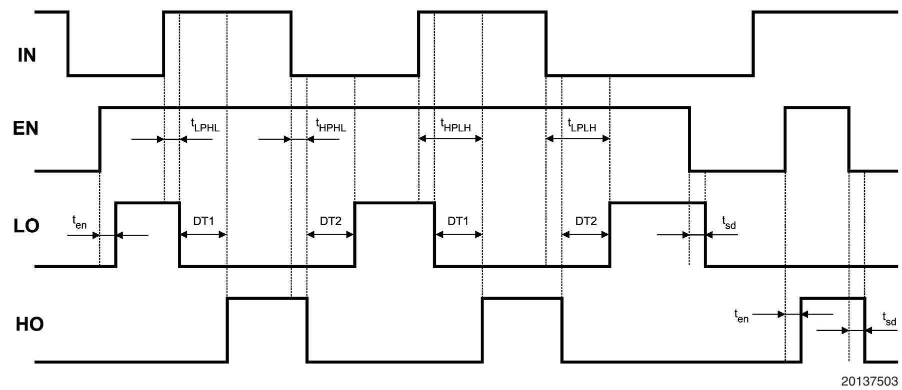
Dead-Time vs Temperature (RT = 10k)



Dead-Time vs Temperature (RT = 100k)

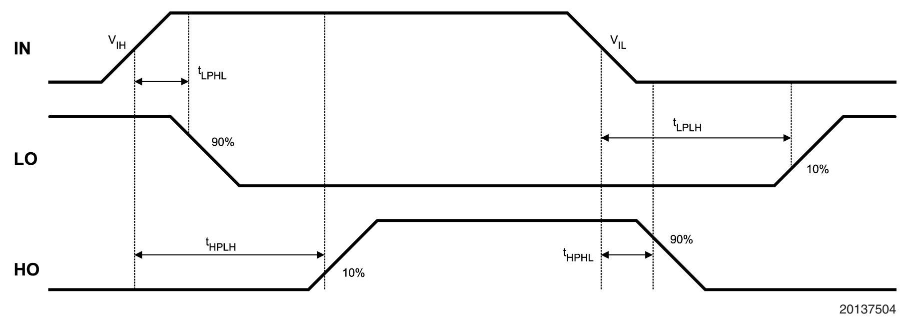


Timing Diagrams



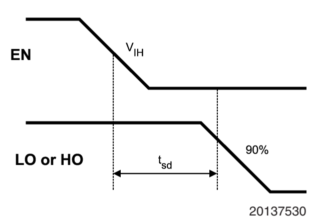
LM5105 Input - Output Waveforms

FIGURE 2.



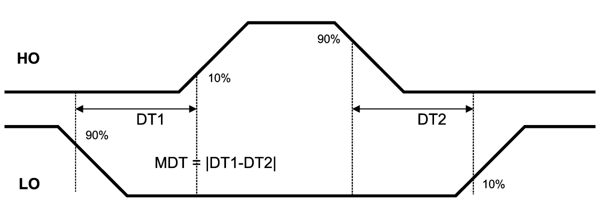
LM5105 Switching Time Definitions: t_{LPLH}, t_{LPHL}, t_{HPLH}, t_{HPHL}

FIGURE 3.



LM5105 Enable: t_{sd}

FIGURE 4.



LM5105 Dead-time: DT

FIGURE 5.

Operational Notes

The LM5105 is a single PWM input Gate Driver with Enable that offers a programmable deadtime. The deadtime is set with a resistor at the RDT pin and can be adjusted from 100ns to 600ns. The wide deadtime programming range provides the flexibility to optimize drive signal timing for a wide range of MOSFETS and applications.

The RDT pin is biased at 3V and current limited to 1 mA maximum programming current. The time delay generator will accommodate resistor values from 5k to 100k with a deadtime time that is proportional to the RDT resistance. Grounding the RDT pin programs the LM5105 to drive both outputs with minimum deadtime.

STARTUP AND UVLO

Both top and bottom drivers include under-voltage lockout (UVLO) protection circuitry which monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage (HB – HS) independently. The UVLO circuit inhibits each driver until sufficient supply voltage is available to turn-on the external MOSFETs, and the UVLO hysteresis prevents chattering during supply voltage transitions. When the supply voltage is applied to the V_{DD} pin of LM5105, the top and bottom gates are held low until V_{DD} exceeds the UVLO threshold, typically about 6.9V. Any UVLO condition on the bootstrap capacitor will disable only the high side output (HO).

Operational Notes (Continued)

LAYOUT CONSIDERATIONS

The optimum performance of high and low side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. A low ESR/ESL capacitor must be connected close to the IC, and between V_{DD} and V_{SS} pins and between HB and HS pins to support high peak currents being drawn from V_{DD} during turn-on of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (V_{SS}).
3. In order to avoid large negative transients on the switch node (HS) pin, the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding considerations:

   a) The first priority in designing grounding connections is to confine the high peak currents from charging and discharging the MOSFET gate in a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.

   b) The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low side MOSFET body diode. The bootstrap capacitor is recharged on the cycle-by-cycle basis through the bootstrap diode from the ground referenced V_{DD} bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.
5. The resistor on the RDT pin must be placed very close to the IC and seperated from high current paths to avoid noise coupling to the time delay generator which could disrupt timer operation.

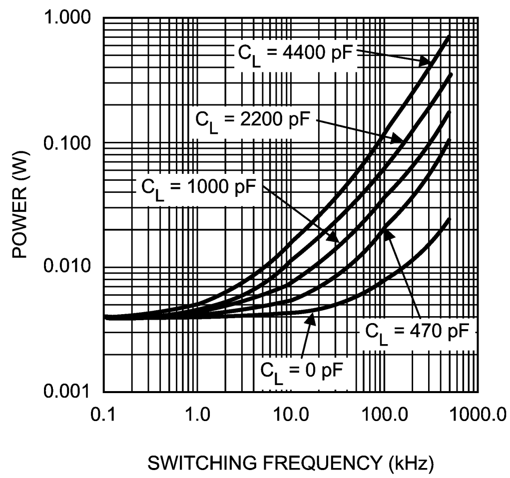
POWER DISSIPATION CONSIDERATIONS

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO (C_L), and supply voltage (V_{DD}) and can be roughly calculated as:

$$P_{DGATES} = 2 \bullet f \bullet C_L \bullet V_{DD}^2$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. The following plot shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the above equation. This plot can be used to approximate the power losses due to the gate drivers.

Gate Driver Power Dissipation (LO + HO)
V_{CC} = 12V, Neglecting Diode Losses



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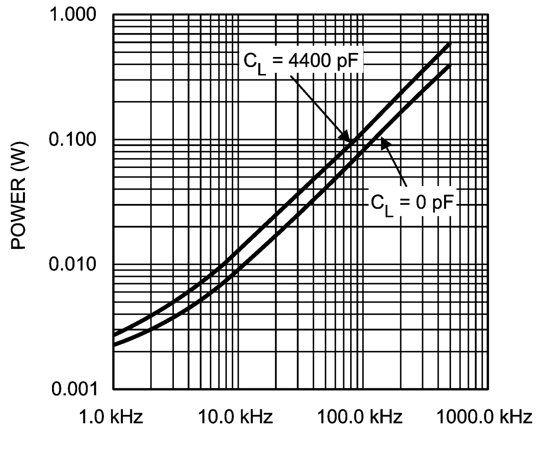
The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to frequency. Larger capacitive loads require more current to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge result in higher reverse recovery losses. The following plot was generated based on calculations and lab measurements of the diode recovery time and current under several operating conditions. This can be useful for approximating the diode power dissipation.

Operational Notes (Continued)

Diode Power Dissipation V_{IN} = 80V



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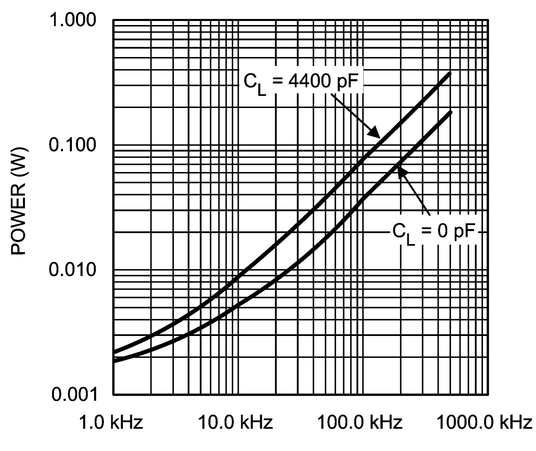
Diode Power Dissipation V_{IN} = 40V



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The total IC power dissipation can be estimated from the above plots by summing the gate drive losses with the bootstrap diode losses for the intended application. Because the diode losses can be significant, an external diode placed in parallel with the internal bootstrap diode (refer to *Figure 6*) and can be helpful in removing power from the IC. For this to be effective, the external diode must be placed close to the IC to minimize series inductance and have a significantly lower forward voltage drop than the internal diode.

HS Transient Voltages Below Ground

The HS node will always be clamped by the body diode of the lower external FET. In some situations, board resistances and inductances can cause the HS node to transiently swing several volts below ground. The HS node can swing below ground provided:

1. HS must always be at a lower potential than HO. Pulling HO more than -0.3V below HS can activate parasitic transistors resulting in excessive current to flow from the HB supply possibly resulting in damage to the IC. The same relationship is true with LO and VSS. If necessary, a Schottky diode can be placed externally between HO and HS or LO and GND to protect the IC from this type of transient. The diode must be placed as close to the IC pins as possible in order to be effective.
2. HB to HS operating voltage should be 15V or less . Hence, if the HS pin transient voltage is -5V, VDD should be ideally limited to 10V to keep HB to HS below 15V.
3. A low ESR bypass capacitor between HB to HS as well as VCC to VSS is essential for proper operation. The capacitor should be located at the leads of the IC to minimize series inductance. The peak currents from LO and HO can be quite large. Any series inductances with the bypass capacitor will cause voltage ringing at the leads of the IC which must be avoided for reliable operation.

Operational Notes (Continued)

LM5105 Driving MOSFETs Connected in Half-Bridge Configuration

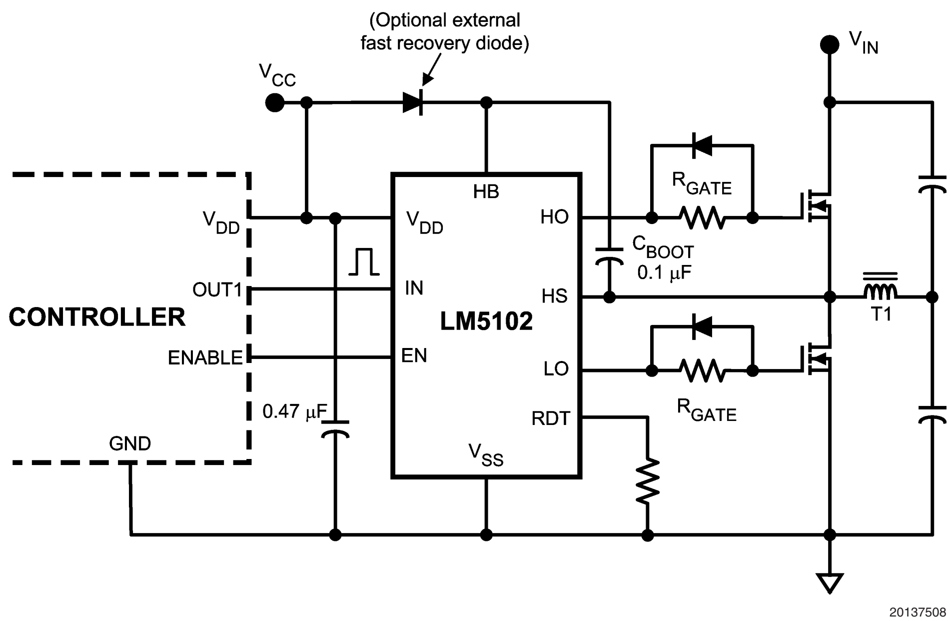
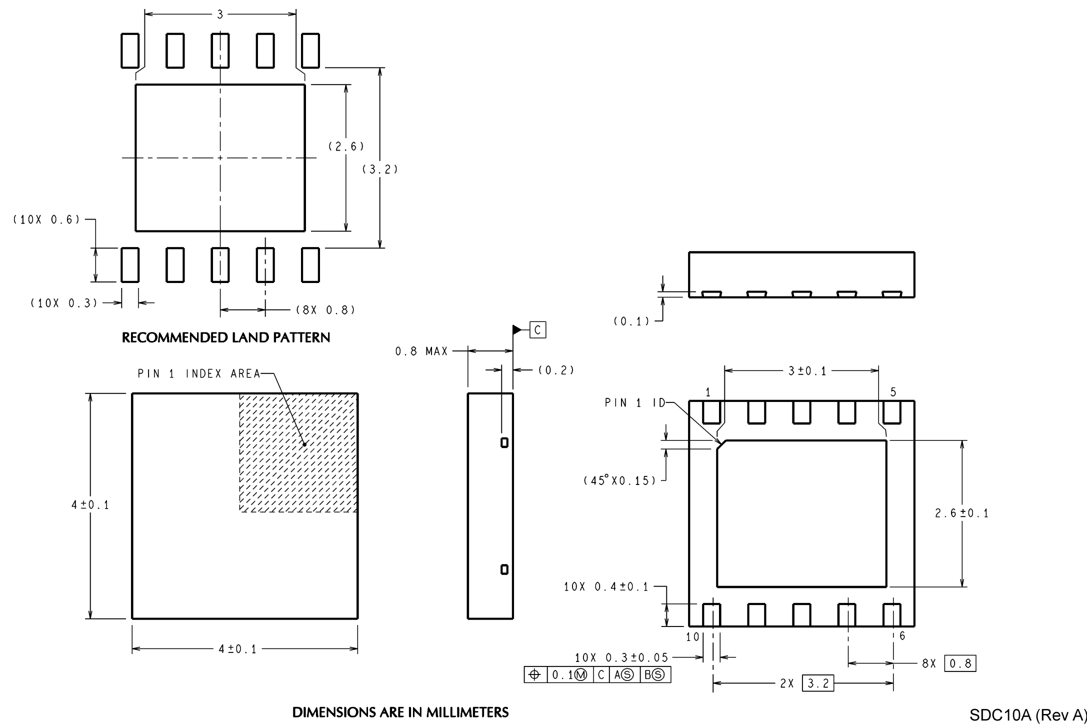


FIGURE 6.

Physical Dimensions inches (millimeters) unless otherwise noted



Notes: Unless otherwise specified

1. Standard lead finish to be 200 microinches/5.00 micrometers minimum tin/lead (solder) on copper.
2. Pin 1 identification to have half of full circle option.
3. No JEDEC registration as of Feb. 2000.

LLP-10 Outline Drawing
NS Package Number SDC10A

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