

# LM612

## Dual-Channel Comparator and Reference

### General Description

The dual-channel comparator consists of two individual comparators, having an input voltage range that extends down to the negative supply voltage  $V^-$ . The common open-collector output can be driven low by either half of the LM612. This configuration makes the LM612 ideal for use as a window comparator. The input stages of the comparator have lateral PNP input transistors which maintain low input currents for large differential input voltages and swings above  $V^+$ .

The 1.2V voltage reference, referred to the  $V^-$  terminal, is a two-terminal shunt-type band-gap similar to the LM185-1.2 series, with voltage accuracy of  $\pm 0.6\%$  available. The reference features operation over a shunt current range of  $17 \mu\text{A}$  to 20 mA, low dynamic impedance, and broad capacitive load range.

As a member of National's Super-Block™ family, the LM612 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

### Features

#### COMPARATORS

- Low operating current 300  $\mu\text{A}$
- Wide supply voltage range 4V to 36V
- Open-collector outputs
- Input common-mode range  $V^-$  to  $(V^+ - 1.8\text{V})$
- Wide differential input voltage  $\pm 36\text{V}$

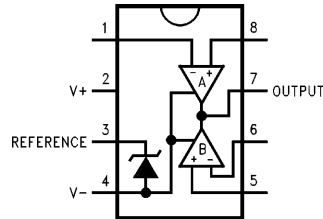
#### REFERENCE

- Fixed output voltage 1.24V
- Tight initial tolerance available  $\pm 0.6\%$  (25°C)
- Wide operating current range 17  $\mu\text{A}$  to 20 mA
- Tolerant of load capacitance

### Applications

- Voltage window comparator
- Power supply voltage monitor
- Dual-channel fault monitor

### Connection Diagram



Top View

TL/H/11058-1

### Ordering Information

For information about surface-mount packaging of this device, please contact the Analog Product Marketing group at National Semiconductor Corporation headquarters.

Reference Tolerances	Temperature Range		Package	NSC Package Number
	Military $-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$	Industrial $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$		
$\pm 0.6\%$ at 25°C, 80 ppm/°C Max	LM612AMN	LM612AIN	8-Pin Molded DIP	N08E
	LM612AMJ/883 (Note 13)		8-Pin Ceramic DIP	J08A
$\pm 2.0\%$ at 25°C, 150 ppm/°C Max	LM612MN	LM612IN	8-Pin Molded DIP	N08E
		LM612IM	8-Pin Narrow Surface Mount	M08A

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## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pin Except $V_R$ (referred to $V^-$ pin) (Note 2)	36V (Max)
(Note 3)	-0.3V (Min)
Current through Any Input Pin and $V_R$ Pin	$\pm 20$ mA
Differential Input Voltage	$\pm 36$ V
Output Short-Circuit Duration	(Note 4)
Storage Temperature Range	$-65^\circ\text{C} \leq T_J \leq +150^\circ\text{C}$
Maximum Junction Temperature	$150^\circ\text{C}$

Thermal Resistance, Junction-to-Ambient (Note 5)  
N Package  $100^\circ\text{C}/\text{W}$

Soldering Information  
N Package  
Soldering (10 seconds)  $260^\circ\text{C}$

ESD Tolerance (Note 6)  $\pm 1$  kV

## Operating Temperature Range

LM612AI, LM612I  $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$   
LM612AM, LM612M  $-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$

**Electrical Characteristics** These specifications apply for  $V^- = \text{GND} = 0\text{V}$ ,  $V^+ = 5\text{V}$ ,  $V_{\text{CM}} = V_{\text{OUT}} = V^+ / 2$ ,  $I_R = 100 \mu\text{A}$ , unless otherwise specified. Limits in standard typeface are for  $T_J = 25^\circ\text{C}$ ; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (Note 7)	LM612AM LM612AI Limits (Note 8)	LM612M LM612I Limits (Note 8)	Units
<b>COMPARATORS</b>						
$I_S$	Total Supply Current	$V^+$ Current, $R_{\text{LOAD}} = \infty$ , $3\text{V} \leq V^+ \leq 36\text{V}$	150 <b>170</b>	250 <b>300</b>	250 <b>300</b>	$\mu\text{A}$ Max $\mu\text{A}$ Max
$V_{\text{OS}}$	Offset Voltage over $V^+$ Range	$4\text{V} \leq V^+ \leq 36\text{V}$ , $R_L = 15 \text{ k}\Omega$	1.0 <b>2.0</b>	3.0 <b>6.0</b>	5.0 <b>7.0</b>	mV Max mV Max
$V_{\text{OS}}$	Offset Voltage over $V_{\text{CM}}$ Range	$0\text{V} \leq V_{\text{CM}} \leq (V^+ - 1.8\text{V})$ $V^+ = 30\text{V}$ , $R_L = 15 \text{ k}\Omega$	1.0 <b>1.5</b>	3.0 <b>6.0</b>	5.0 <b>7.0</b>	mV Max mV Max
$\frac{\Delta V_{\text{OS}}}{\Delta T}$	Average Offset Voltage Drift		<b>15</b>			$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current		5 <b>8</b>	25 <b>30</b>	35 <b>40</b>	nA Max nA Max
$I_{\text{OS}}$	Input Offset Current		0.2 <b>0.3</b>	4 <b>5</b>	4 <b>5</b>	nA Max nA Max
$A_V$	Voltage Gain	$R_L = 10 \text{ k}\Omega$ to $36\text{V}$ , $2\text{V} \leq V_{\text{OUT}} \leq 27\text{V}$	500 <b>100</b>	50	50	V/mV Min V/mV
$t_R$	Large Signal Response Time	$V_{+\text{IN}} = 1.4\text{V}$ , $V_{-\text{IN}} = \text{TTL}$ Swing, $R_L = 5.1 \text{ k}\Omega$	1.5 <b>2.0</b>			$\mu\text{s}$ $\mu\text{s}$
$I_{\text{SINK}}$	Output Sink Current	$V_{+\text{IN}} = 0\text{V}$ , $V_{-\text{IN}} = 1\text{V}$ , $V_{\text{OUT}} = 1.5\text{V}$ $V_{\text{OUT}} = 0.4\text{V}$	20 <b>13</b> 2.8 <b>2.4</b>	10 <b>8</b> 1.0 <b>0.5</b>	10 <b>8</b> 0.8 <b>0.5</b>	mA Min mA Min mA Min mA Min
$I_L$	Output Leakage Current	$V_{+\text{IN}} = 1\text{V}$ , $V_{-\text{IN}} = 0\text{V}$ , $V_{\text{OUT}} = 36\text{V}$	0.1 <b>0.2</b>	10	10	$\mu\text{A}$ Max $\mu\text{A}$

**Electrical Characteristics** These specifications apply for  $V^- = \text{GND} = 0\text{V}$ ,  $V^+ = 5\text{V}$ ,  $V_{\text{CM}} = V_{\text{OUT}} = V^+ / 2$ ,  $I_{\text{R}} = 100 \mu\text{A}$ , unless otherwise specified. Limits in standard typeface are for  $T_{\text{J}} = 25^\circ\text{C}$ ; limits in **boldface type** apply over the **Operating Temperature Range**. (Continued)

Symbol	Parameter	Conditions	Typical (Note 7)	LM612AM LM612AI Limits (Note 8)	LM612M LM612I Limits (Note 8)	Units
<b>VOLTAGE REFERENCE</b> (Note 9)						
$V_{\text{R}}$	Reference Voltage		1.244	1.2365 1.2515 ( $\pm 0.6\%$ )	1.2191 1.2689 ( $\pm 2\%$ )	V Min V Max
$\frac{\Delta V_{\text{R}}}{\Delta T}$	Average Drift with Temperature	(Note 10)	<b>18</b>	<b>80</b>	<b>150</b>	ppm/ $^\circ\text{C}$ Max
$\frac{\Delta V_{\text{R}}}{\text{kH}}$	Average Drift with Time	$T_{\text{J}} = 40^\circ\text{C}$ $T_{\text{J}} = 150^\circ\text{C}$	400 1000			ppm/kH ppm/kH
$\frac{\Delta V_{\text{R}}}{\Delta T_{\text{J}}}$	Hysteresis	(Note 11)	<b>3.2</b>			$\mu\text{V}/^\circ\text{C}$
$\frac{\Delta V_{\text{R}}}{\Delta I_{\text{R}}}$	$V_{\text{R}}$ Change with Current	$V_{\text{R}}[100 \mu\text{A}] - V_{\text{R}}[17 \mu\text{A}]$	0.05 <b>0.1</b>	1 <b>1.1</b>	1 <b>1.1</b>	mV Max mV Max
		$V_{\text{R}}[10 \text{ mA}] - V_{\text{R}}[100 \mu\text{A}]$ (Note 12)	1.5 <b>2.0</b>	5 <b>5.5</b>	5 <b>5.5</b>	mV Max mV Max
R	Resistance	$\Delta V_{\text{R}}[10 \text{ mA to } 0.1 \text{ mA}] / 9.9 \text{ mA}$	0.2	<b>0.56</b>	<b>0.56</b>	$\Omega$ Max
		$\Delta V_{\text{R}}[100 \mu\text{A to } 17 \mu\text{A}] / 83 \mu\text{A}$	0.6	<b>13</b>	<b>13</b>	$\Omega$ Max
$\frac{\Delta V_{\text{R}}}{\Delta V^+}$	$V_{\text{R}}$ Change with $V^+$ Change	$V_{\text{R}}[V^+ = 5\text{V}] - V_{\text{R}}[V^+ = 36\text{V}]$	0.1 <b>0.1</b>	1.2 <b>1.3</b>	1.2 <b>1.3</b>	mV Max mV Max
		$V_{\text{R}}[V^+ = 5\text{V}] - V_{\text{R}}[V^+ = 3\text{V}]$	0.01 <b>0.01</b>	1 <b>1.5</b>	1 <b>1.5</b>	mV Max mV Max
$e_{\text{n}}$	Voltage Noise	BW = 10 Hz to 10 kHz	30			$\mu\text{VRMS}$

**Note 1:** Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

**Note 2:** Input voltage above  $V^+$  is not allowed. As long as one input pin voltage remains inside the common-mode range, the comparator will deliver the correct output.

**Note 3:** More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below  $V^-$ , a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

**Note 4:** Shorting the Output to  $V^-$  will not cause power dissipation, so it may be continuous. However, shorting the Output to any more positive voltage (including  $V^+$ ), will cause 80 mA (typ.) to be drawn through the output transistor. This current multiplied by the applied voltage is the power dissipation in the output transistor. If this total power causes the junction temperature to exceed  $150^\circ\text{C}$ , degraded reliability or destruction of the device may occur. To determine junction temperature, see Note 5.

**Note 5:** Junction temperature may be calculated using  $T_{\text{J}} = T_{\text{A}} + P_{\text{D}} \theta_{\text{JA}}$ . The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal  $\theta_{\text{JA}}$  is  $90^\circ\text{C}/\text{W}$  for the N package.

**Note 6:** Human body model, 100 pF discharged through a 1.5 k $\Omega$  resistor.

**Note 7:** Typical values in standard typeface are for  $T_{\text{J}} = 25^\circ\text{C}$ ; values in **boldface type** apply for the full operating temperature range. These values represent the most likely parametric norm.

**Note 8:** All limits are guaranteed for  $T_{\text{J}} = 25^\circ\text{C}$  (standard type face) or over the full operating temperature range (**bold type face**).

**Note 9:**  $V_{\text{R}}$  is the reference output voltage, nominally 1.24V.

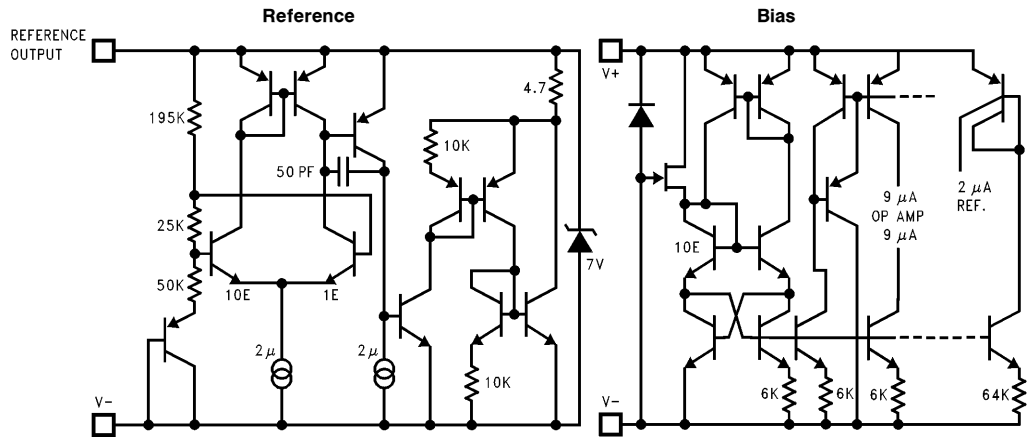
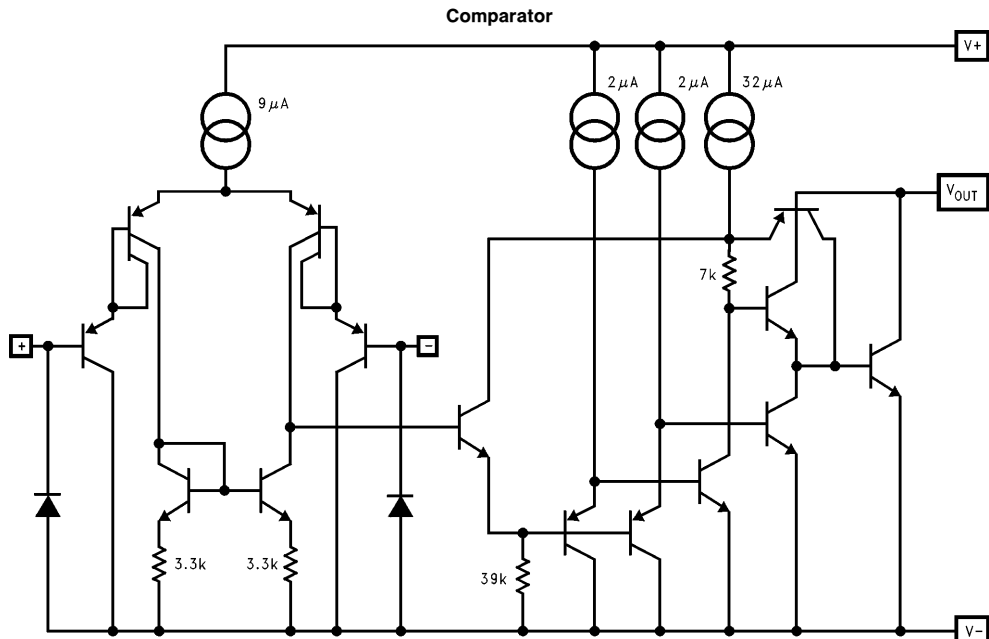
**Note 10:** Average reference drift is calculated from the measurement of the reference voltage at  $25^\circ\text{C}$  and at the temperature extremes. The drift, in ppm/ $^\circ\text{C}$ , is  $10^6 \cdot \Delta V_{\text{R}} / V_{\text{R}}[25^\circ\text{C}] \cdot \Delta T_{\text{J}}$ , where  $\Delta V_{\text{R}}$  is the lowest value subtracted from the highest,  $V_{\text{R}}[25^\circ\text{C}]$  is the value at  $25^\circ\text{C}$ , and  $\Delta T_{\text{J}}$  is the temperature range. This parameter is guaranteed by design and sample testing.

**Note 11:** Hysteresis is the change in  $V_{\text{R}}$  caused by a change in  $T_{\text{J}}$ , after the reference has been "dehysteresized". To dehysteresize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward  $25^\circ\text{C}$ :  $25^\circ\text{C}$ ,  $85^\circ\text{C}$ ,  $-40^\circ\text{C}$ ,  $70^\circ\text{C}$ ,  $0^\circ\text{C}$ ,  $25^\circ\text{C}$ .

**Note 12:** Low contact resistance is required for accurate measurement.

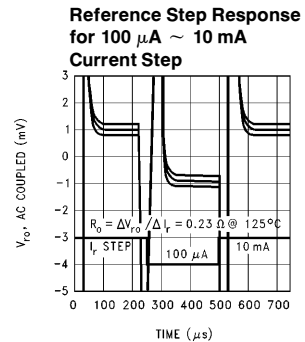
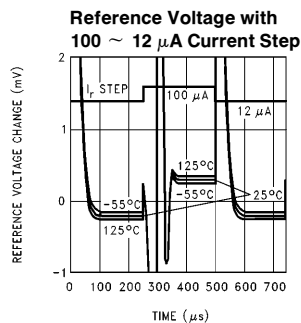
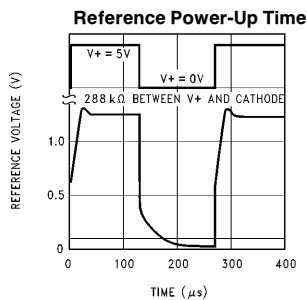
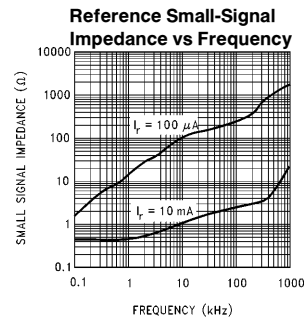
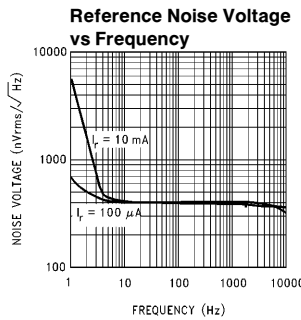
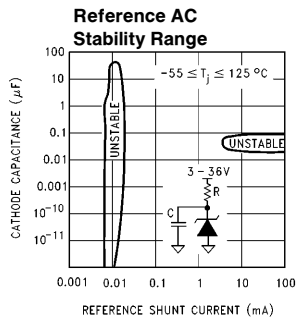
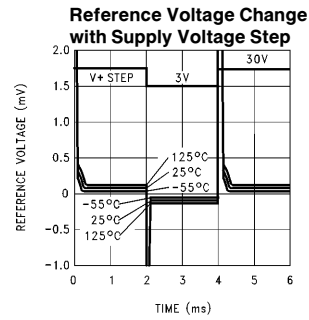
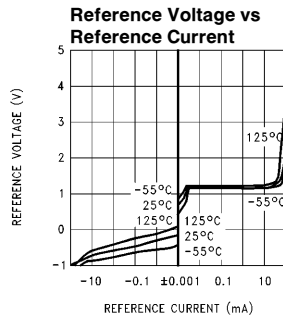
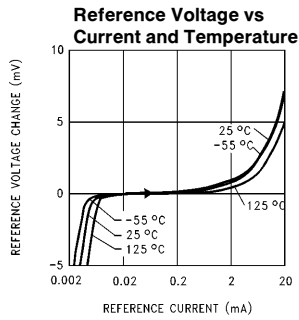
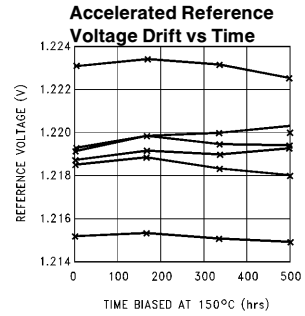
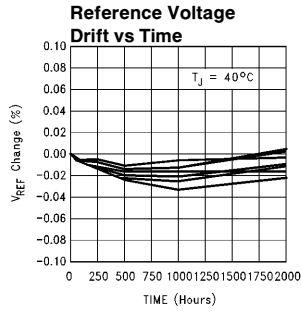
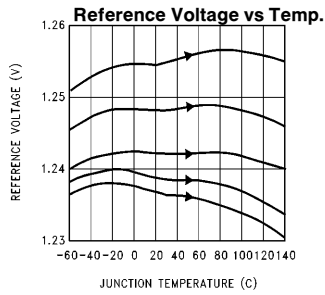
**Note 13:** A military RETS 612AMX electrical test specification is available on request. The military screened parts can also be procured as a Standard Military Drawing.

# Simplified Schematic Diagrams



# Typical Performance Characteristics (Reference)

$T_J = 25^\circ\text{C}$ ,  $V^- = 0\text{V}$ , unless otherwise noted

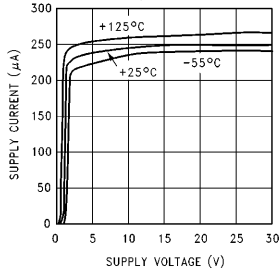


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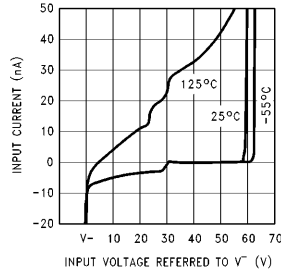
# Typical Performance Characteristics (Comparators)

$T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$

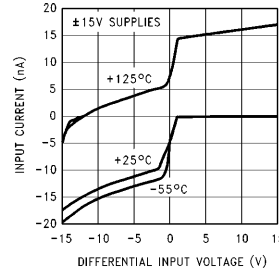
**Supply Current vs Supply Voltage**



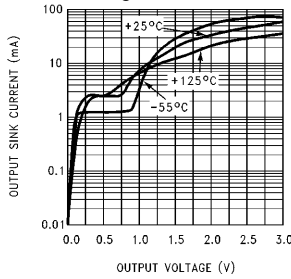
**Input Bias Current vs Common-Mode Voltage**



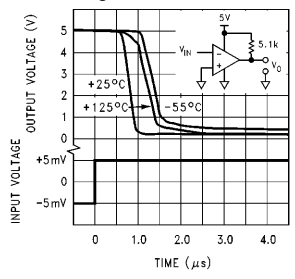
**Input Current vs Differential Input Voltage**



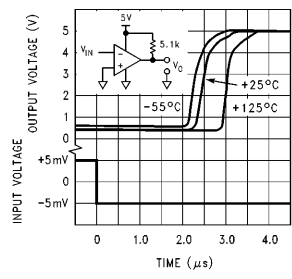
**Output Saturation Voltage vs Sink Current**



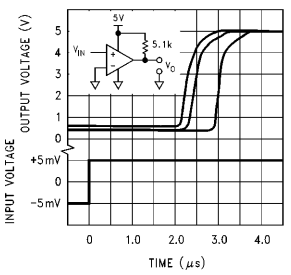
**Small-Signal Response Times—Inverting Input, Negative Transition**



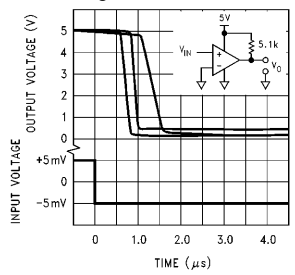
**Small-Signal Response Times—Inverting Input, Positive Transition**



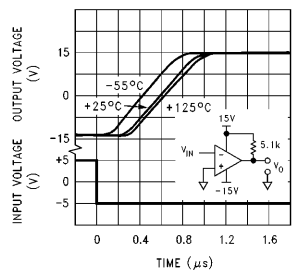
**Small-Signal Response Times—Non-Inverting Input, Positive Transition**



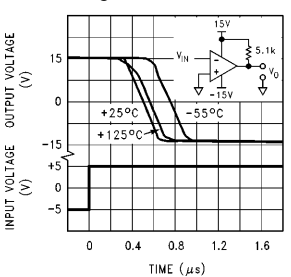
**Small-Signal Response Times—Non-Inverting Input, Negative Transition**



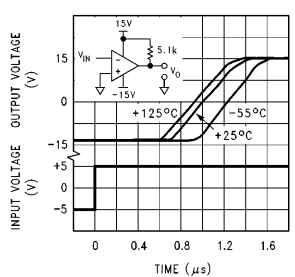
**Large-Signal Response Times—Inverting Input, Positive Transition**



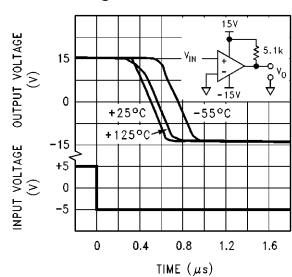
**Large-Signal Response Times—Inverting Input, Negative Transition**



**Large-Signal Response Times—Non-Inverting Input, Positive Transition**



**Large-Signal Response Times—Non-Inverting Input, Negative Transition**



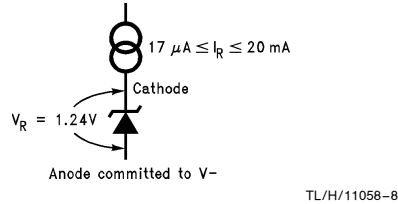
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## Application Information

### VOLTAGE REFERENCE

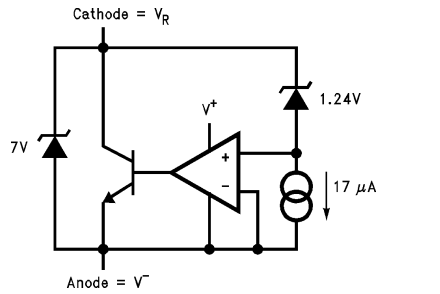
#### Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current  $I_R$  flowing in the “forward” direction there is the familiar diode transfer function.  $I_R$  flowing in the reverse direction forces the reference voltage to be developed from cathode to anode.



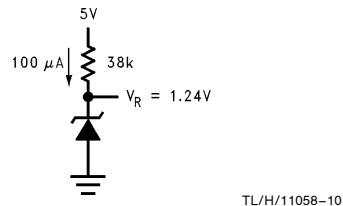
**FIGURE 1. 1.24V Reference is Developed between Cathode and Anode; Current Source  $I_R$  is External**

The reference equivalent circuit reveals how  $V_R$  is held at the constant 1.2V by feedback for a wide range of reverse current.



**FIGURE 2. Reference Equivalent Circuit**

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage to the Reference Output pin. Varying that voltage, and so varying  $I_R$ , has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate  $I_R$ .



**FIGURE 3. 1.2V Reference**

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20  $\mu\text{A}$  to 3 mA the reference is stable for any value of capacitance. With the reference’s wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering when necessary.

#### Reference Hysteresis

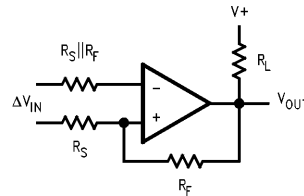
The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the datasheet for any given device. Do not assume that no specification means no hysteresis.

### COMPARATORS

Either comparator or the reference may be biased in any way with no effect on the other sections of the LM612, except when a substrate diode conducts (see Electrical Characteristics Note 3). For example, one or both inputs of one comparator may be outside the input voltage range limits, the reference may be unpowered, and the other comparator will still operate correctly. The inverting input of an unused comparator should be tied to  $V^-$  and the non-inverting tied to  $V^+$ .

#### Hysteresis

Any comparator may oscillate or produce a noisy output if the applied differential input voltage is near the comparator’s offset voltage. This usually happens when the input signal is moving very slowly across the comparator’s switching threshold. This problem can be prevented by the addition of hysteresis, or positive feedback, as shown in *Figure 4*.



**FIGURE 4.  $R_S$  and  $R_F$  Add Hysteresis to Comparator**

The amount of hysteresis added in *Figure 4* is

$$V_H = V^+ \times \frac{R_S}{(R_F + R_S)}$$

$$\approx V^+ \times \frac{R_S}{R_F} \quad \text{for } R_F \gg R_S$$

A good rule of thumb is to add hysteresis of at least the maximum specified offset voltage. More than about 50 mV

## Application Information (Continued)

of hysteresis can substantially reduce the accuracy of the comparator, since the offset voltage is effectively being increased by the hysteresis when the comparator output is high.

It is often a good idea to decrease the amount of hysteresis until oscillations are observed, then use three times that minimum hysteresis in the final circuit. Note that the amount of hysteresis needed is greatly affected by layout. The amount of hysteresis should be rechecked each time the layout is changed, such as changing from a breadboard to a P.C. board.

### Input Stage

The input stage uses lateral PNP input transistors which, unlike those of many op amps, have breakdown voltage  $BV_{EBO}$  equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

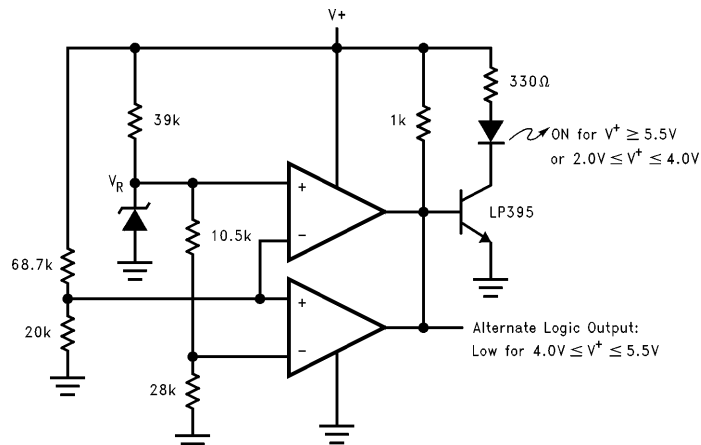
The guaranteed common-mode input voltage range for an LM612 is  $V^- \leq V_{CM} \leq (V^+ - 1.8V)$ , over temperature. This is the voltage range in which the comparisons must be made. If both inputs are within this range, the output will be at the correct state. If one input is within this range, and the other input is less than  $(V^- + 32V)$ , even if this is greater than  $V^+$ , the output will be at the correct state. If, however, either or both inputs are driven below  $V^-$ , and either input current exceeds  $10 \mu A$ , the output state is not guaranteed to be correct. If both inputs are above  $(V^+ - 1.8V)$ , the output state is also not guaranteed to be correct.

### Output Stage

The comparators have a common open-collector output stage which requires a pull-up resistor to a positive supply voltage for the output to switch properly. When the internal output transistor is off, the output (HIGH) voltage will be pulled up to this external positive voltage.

To ensure that the LOW output voltage is under the TTL-low threshold, the output transistor's load current must be less than  $0.8 \text{ mA}$  (over temperature) when it turns on. This impacts the minimum value of the pull-up resistor.

## Typical Applications

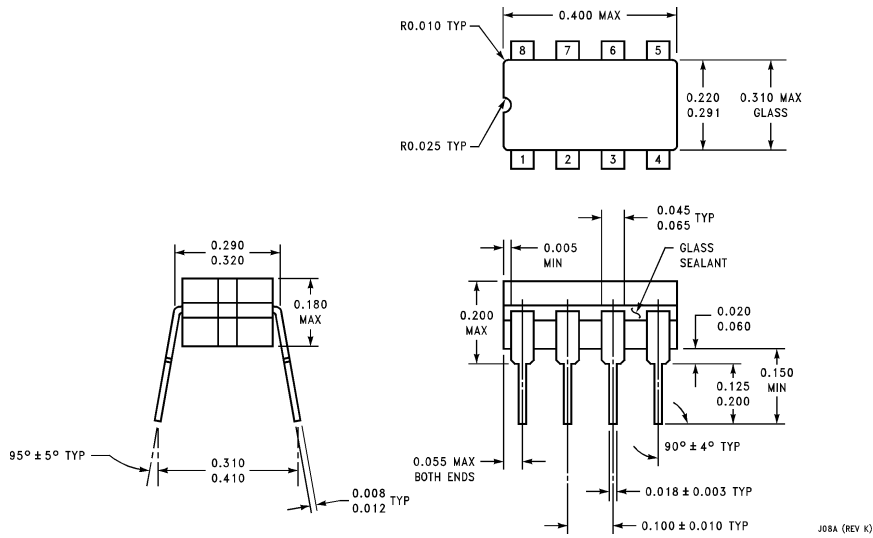


Power Supply Monitor with Indicator

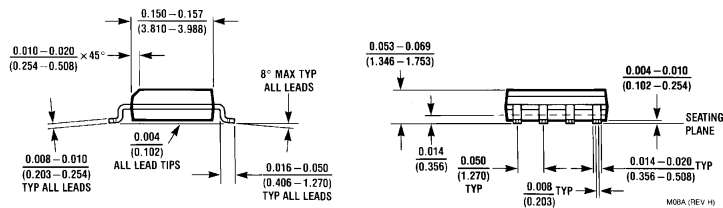
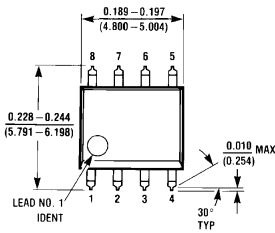
TL/H/11058-12



**Physical Dimensions** inches (millimeters)

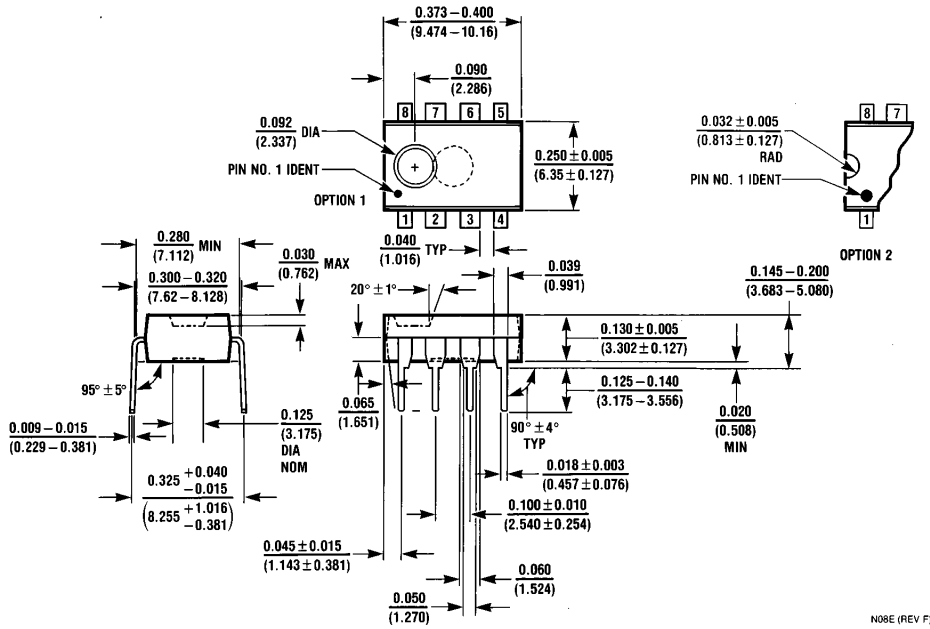


**8-Pin Ceramic Dual-In-Line Package (J)**  
**Order Number LM612AMJ/883**  
**NS Package Number J08A**



**8-Pin Surface Mount Package (M)**  
**Order Number LM612IM**  
**NS Package Number M08A**

**Physical Dimensions** inches (millimeters) (Continued)



**8-Pin Molded Dual-In-Line Package (N)**  
**Order Number LM612AMJ/883, LM612AMN, LM612AIN, LM612MN or LM612IN**  
**NS Package Number N08E**

N08E (REV F)

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