National Semiconductor

PRELIMINARY
April 2006

LMH1981
Multi-Format Video Sync Separator

General Description

The LMH1981 is a high performance multi-format sync separator ideal for use in a wide range of video applications, such as broadcast and professional video equipment and HDTV/DTV systems.

The input accepts standard analog video signals with either bi-level or tri-level sync, and the outputs provide all of the critical timing signals in CMOS logic, including composite, horizontal, and vertical syncs, burst/back porch timing, odd/even field, and video format outputs. The horizontal sync output features very low jitter, minimizing external circuitry needed to clean and reduce jitter in subsequent sync processing stages.

The LMH1981 automatically detects the input video format, eliminating the need for programming using a microcontroller or external R_{SET} resistor. The sync separator applies precise 50% sync slicing to ensure accurate sync extraction for inputs with irregular amplitude, offset, and noise conditions. Its unique video format feature (pin 9) outputs the total vertical scan lines per frame as an 11-bit binary serial bit stream, which can be decoded by the video system to determine the input video format and enable dynamic adjustment of system parameters, i.e.: color space or scaler conversions. The LMH1981 is available in a 14-pin TSSOP package and operates over the full commercial temperature range.

Features

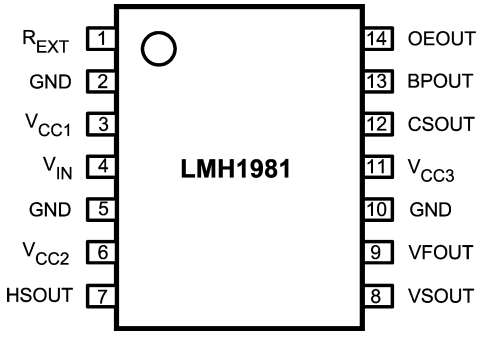
- Standard analog video sync separation for NTSC, PAL, SECAM, 480i/p, 576i/p, 720p, 1080i/p, and RGsB from composite (CVBS), S-Video (Y/C), component (YP_BP_R), and computer video interfaces
- Bi-level & tri-level sync compatible
- Composite, horizontal, and vertical sync outputs
- Burst/back porch timing, odd/even field, and video format Outputs
- Superior jitter performance on the H Sync negative-going edge reference
- Automatic video format detection
- 50% sync slicing of video inputs from 0.5 V_{PP} to 2 V_{PP}
- Macrovision compatible
- 3.3V to 5V supply operation

Applications

- Broadcast and professional video equipment
- HDTV/DTV systems
- Genlock systems
- Video capture & digitization
- Set-top boxes (STB) & digital video recorders (DVR)
- Video displays

Connection Diagram

14-Pin TSSOP



Top View

FIGURE 1. Pinout

Pin Descriptions

Pin No.	Pin Name	Pin Description
1	R_{EXT}	Bias Current External Resistor
2, 5, 10	GND	Ground
3, 6, 11	V_{CC}	Supply Voltage
4	V_{IN}	Video Input
7	HSOUT	Horizontal Sync Output
8	VSOUT	Vertical Sync Output
9	VFOUT	Video Format Output
12	CSOUT	Composite Sync Output
13	BPOUT	Burst/Back Porch Timing Output
14	OEOUT	Odd/Even Field Output

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
14-Pin TSSOP	LMH1981MT	LMH1981MT	94 Units/Rail	MTC14
	LMH1981MTX		2.5k Units Tape and Reel	

Absolute Maximum Ratings (Notes 1, 7)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	3.5 kV
Machine Model	350V
Supply Voltage V_S,	0V to 5.5V
Video Input, V_{IN}	−0.3V to V_S + 0.3V
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (soldering 10 sec.)	300˚C
Junction Temperature (T_{JMAX}) (Note 3)	+150˚C
Thermal Resistance (θ_{JA})	52˚C/W

Operating Ratings (Note 1)

Operating Temperature Range	0˚C to +70˚C
V_S	3.3V to 5V
V_{IN}	0V to 2.3V

Electrical Characteristics (Note 4)

Unless otherwise specified, $V_S = V_{CC1} = V_{CC2} = V_{CC3} = 3.3V$, $T_A = 25˚C$, R_{EXT} = 10 kΩ 0.1%. Output signals are measured on pins 7, 8, 9, 12, 13, and 14. (See *Figure 2* for Test Circuit)

Symbol	Parameter	Conditions		Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
I_{CC}	Supply Current	No Input Signal, Outputs at Logic 1	V_{CC} = 3.3V				mA
			V_{CC} = 5V				
Video Input Specifications							
$V_{IN-AMPL}$	Input Signal Amplitude	Input Signal Amplitude Required to Maintain Slice Level Spec		0.5		2.0	V_{PP}
$V_{IN-CLAMP}$	Input Sync Clamp Level	Unloaded					V
$V_{IN-SLICE}$	Input Sync Slice Level	Input Signal Amplitude 0.5 V_{PP} to 2 V_{PP} Between Sync Tip Clamp Level and Video Blank Level			50		%
Logic Output Specifications							
V_{OL}	Output Logic 0,	I_{OL} = TBD		−0.5		1.5	V
V_{OH}	Output Logic 1	I_{OH} = TBD	V_{CC} = 3.3V	3.0		3.8	V
			V_{CC} = 5V	4.5		5.5	
$T_{SYNC-LOCK}$	Sync Lock Time	Hold-Off Period Before Output Are Accurate			TBD		
	Composite Sync Output	See *Figures 9, 10* for SDTV, EDTV & HDTV Horizontal Interval Timing					
	Horizontal Sync Output	See *Figures 9, 10*					
	Burst/Back Porch Clamp Output	See *Figures 9, 10*					
T_{VSOUT}	Vertical Sync Output Pulse Width	See *Figures 3, 8* for SDTV, EDTV & HDTV Vertical Interval Timing			3		H Periods
	Odd/Even Field Output	See *Figures 3, 8*					
	Video Format Output	See *Figures 11, 12, 13*					

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

Note 2: Human Body Model is 1.5 kΩ in series with 100 pF. Machine Model is 0Ω in series with 200 pF.

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 4: Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

Note 5: Typical values represent the most likely parametric norm at the time of characterization.

Note 6: Limits are 100% production tested at 25˚C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.

Note 7: All voltages are measured with respect to GND, unless otherwise specified.

Note 8: Input amplitude range reduces if V_S = 3.3V.

Note 9: Outputs are active low signals, except for composite sync, odd/even field, and video format outputs.

LMH1981 Test Circuit

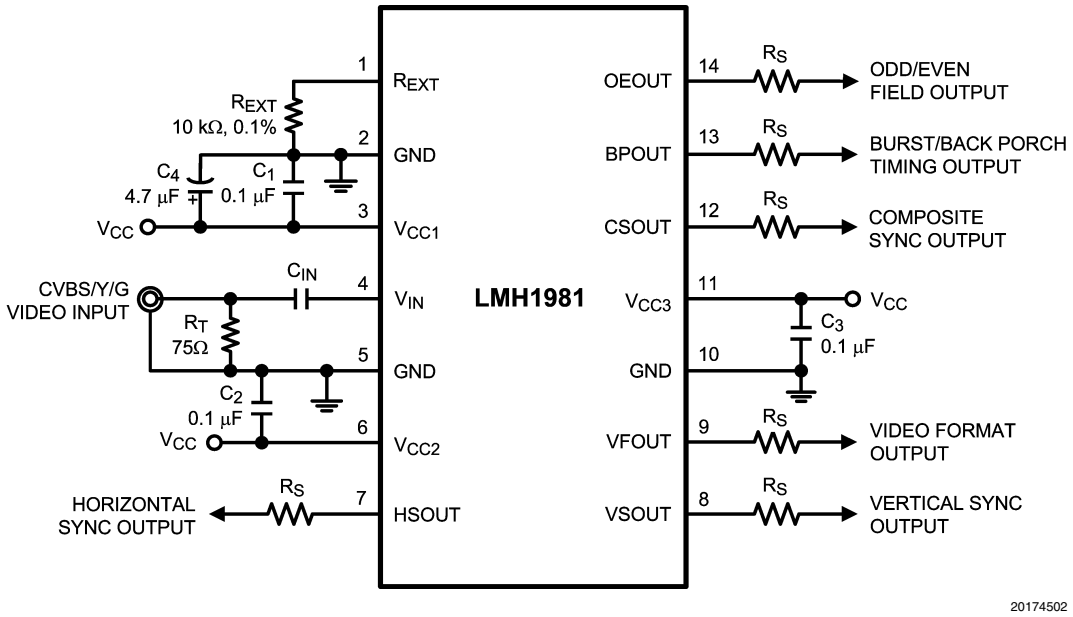


FIGURE 2. Test Circuit

The LMH1981 test circuit is shown in *Figure 2*. The video generator should be a clean 75Ω source to prevent unwanted reflections along the 75Ω coaxial cable. The output waveforms should be evaluated using a FET probe on an oscilloscope with at least 500 MHz bandwidth.

SDTV Vertical Interval Timing (NTSC, PAL SECAM, 480i, 576i)

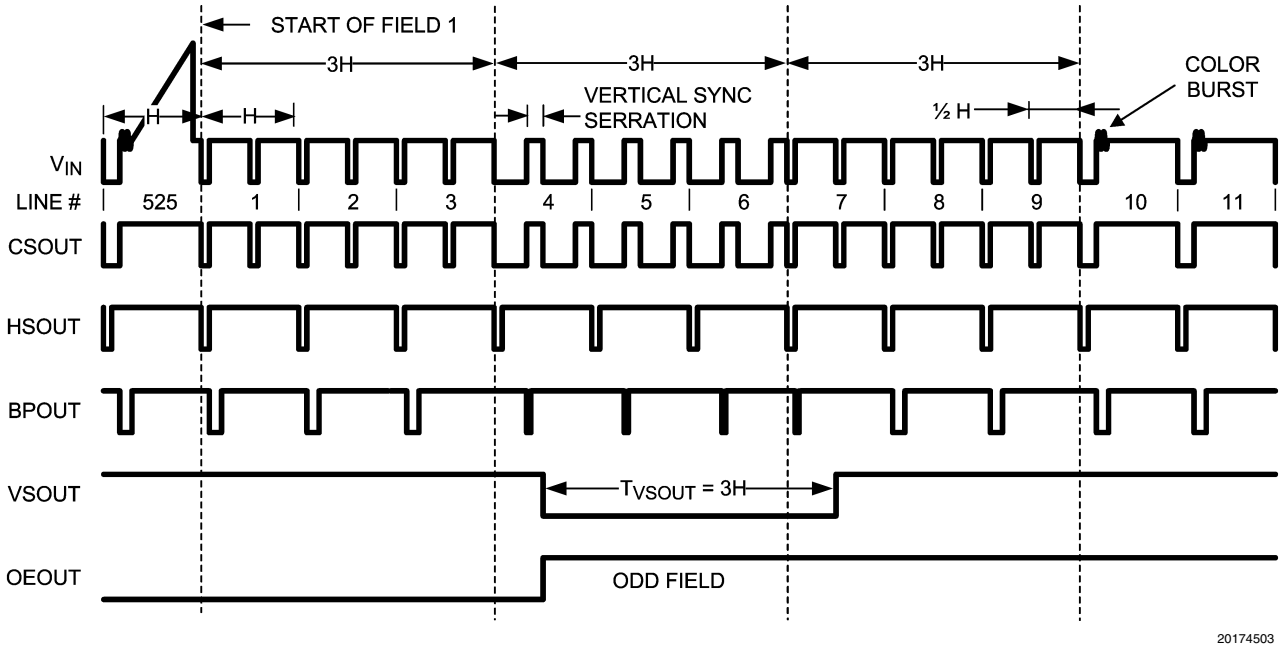


FIGURE 3. NTSC Odd Field Vertical Interval

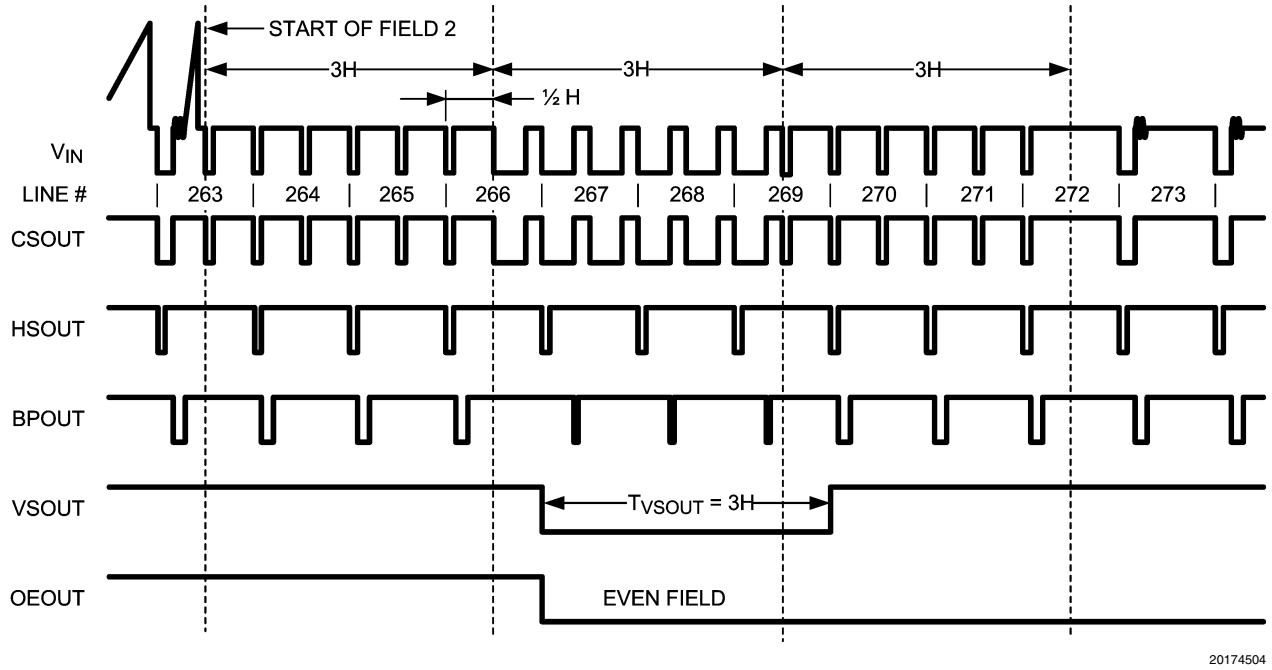


FIGURE 4. NTSC Even Field Vertical Interval

EDTV Vertical Interval Timing (480p, 576p)

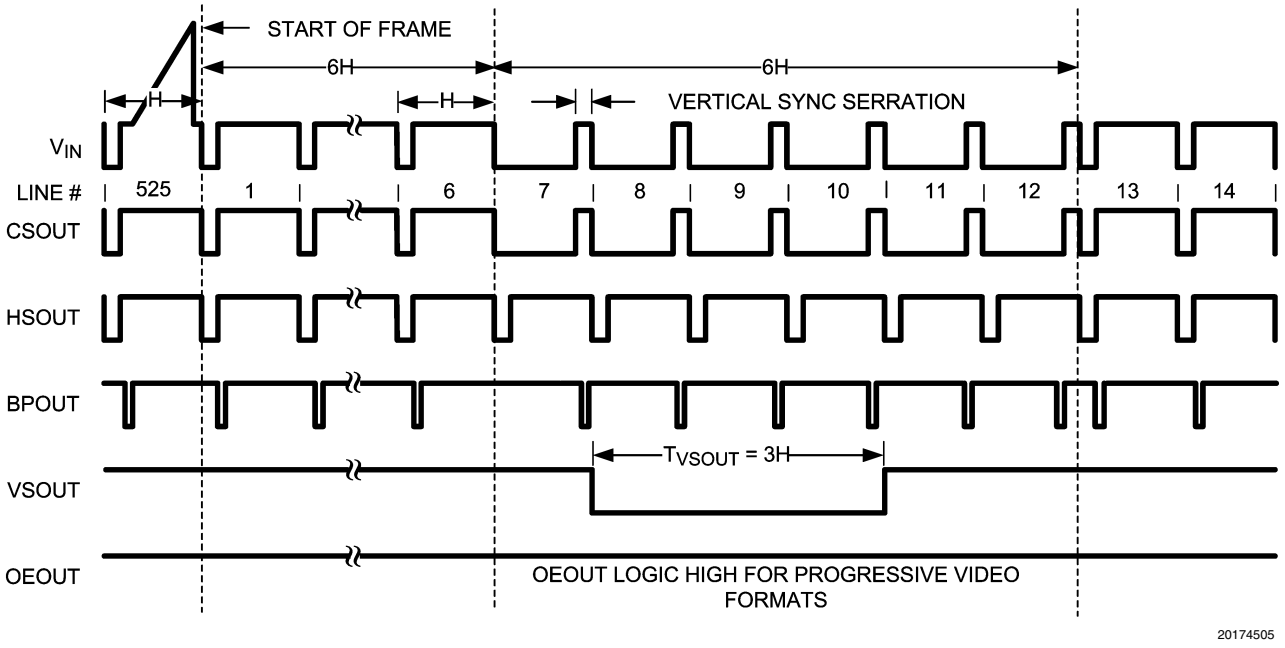


FIGURE 5. 480p Vertical Interval

HDTV Vertical Interval Timing (720p)

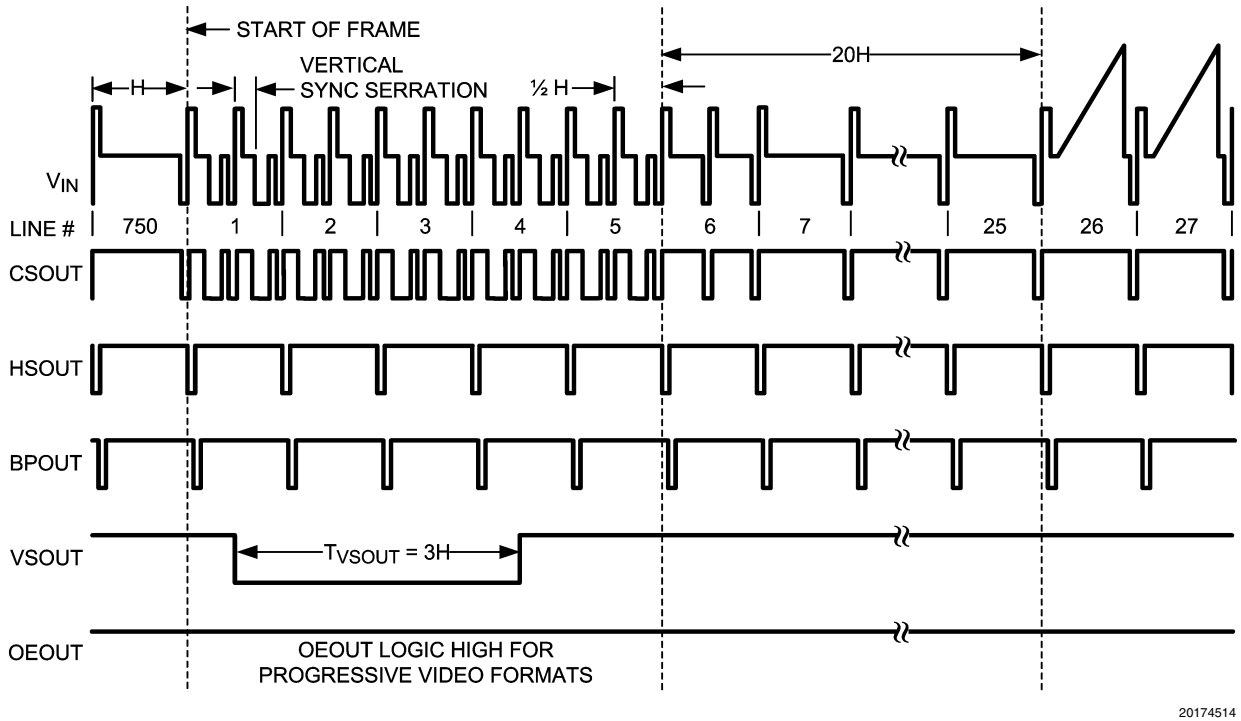


FIGURE 6. 720p Vertical Interval

HDTV Vertical Interval Timing (1080i)

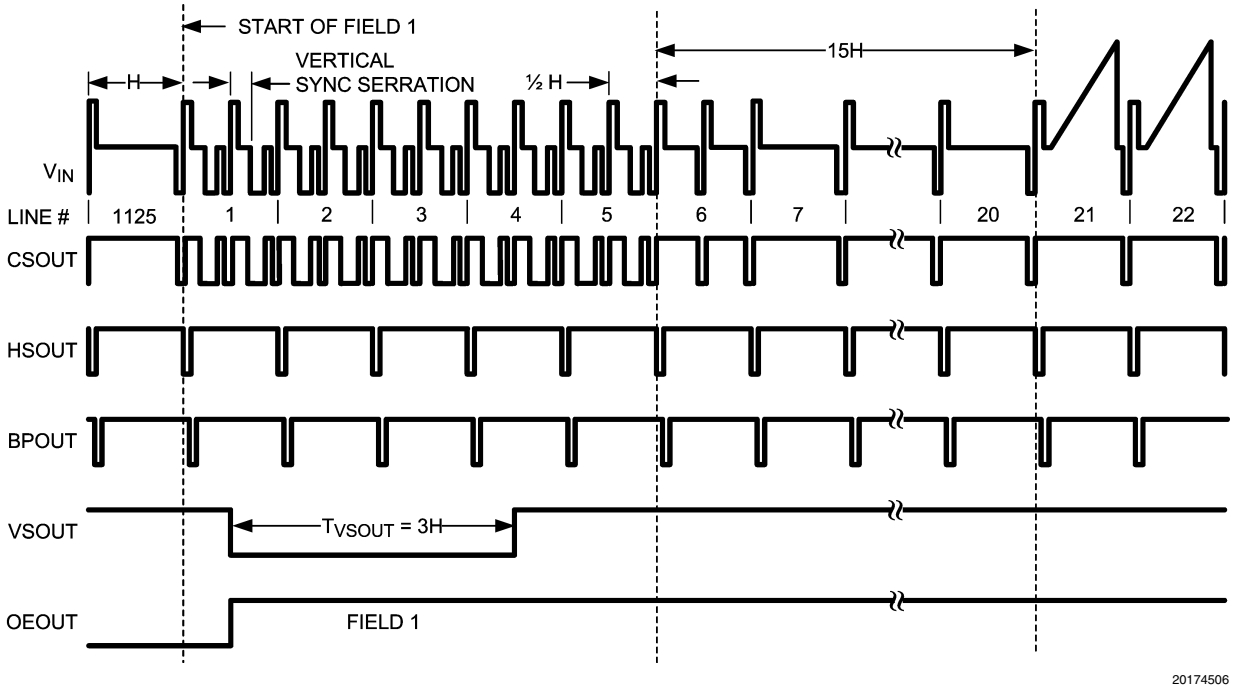


FIGURE 7. 1080i Field 1 Vertical Interval

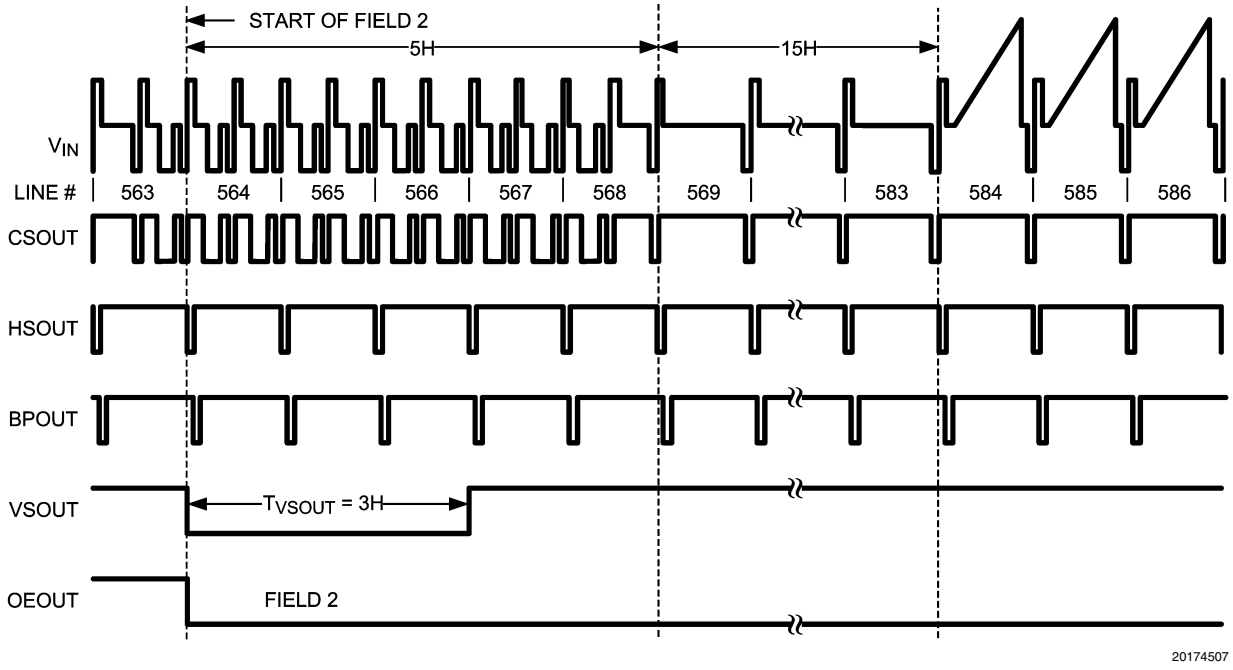


FIGURE 8. 1080i Field 2 Vertical Interval

SD/EDTV Horizontal Interval Timing

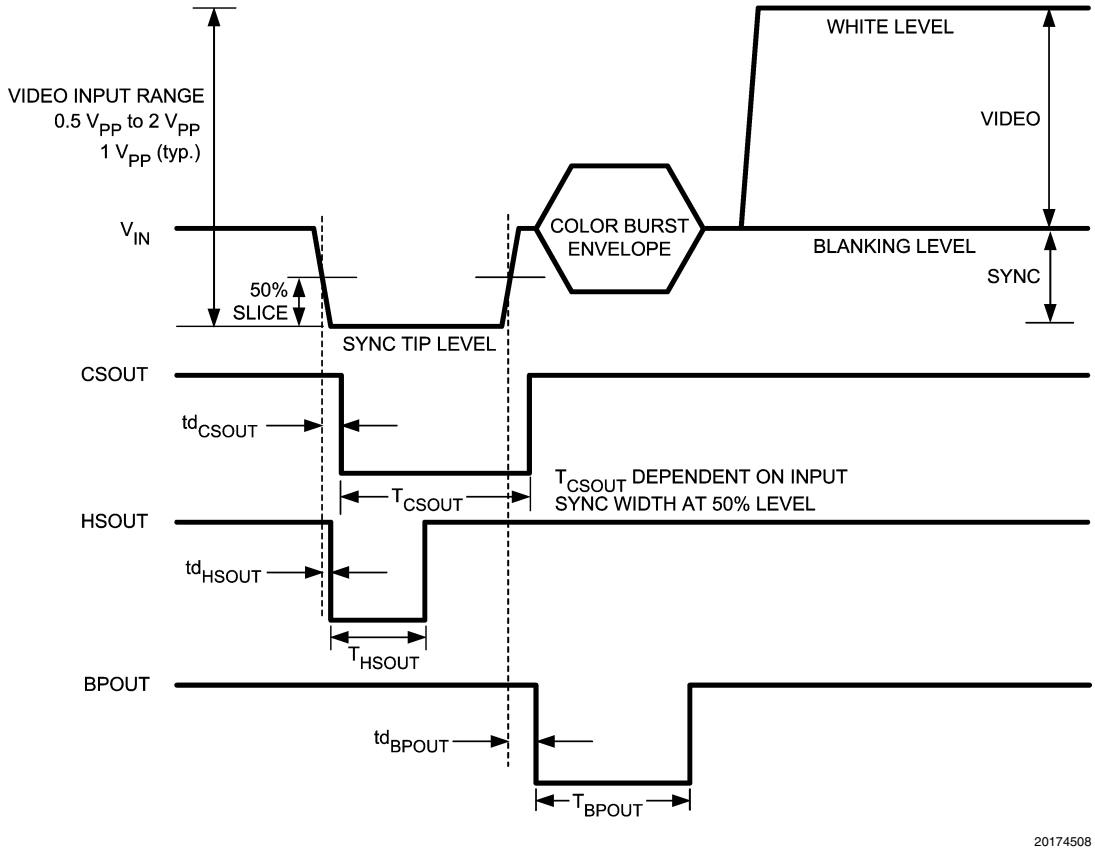


FIGURE 9. SD/EDTV Horizontal Interval with Bi-level Sync

HDTV Horizontal Interval Timing

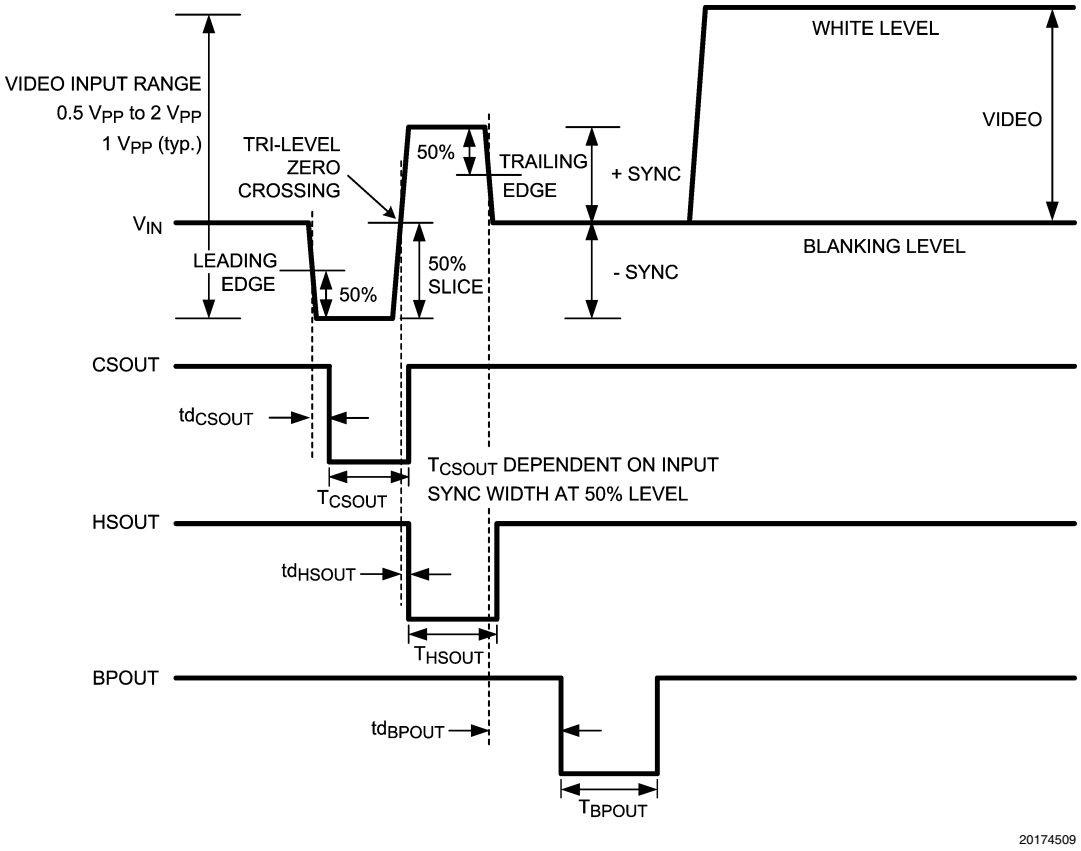


FIGURE 10. HDTV Horizontal Interval with Tri-Level Sync

Application Information

GENERAL DESCRIPTION

The LMH1981 is designed to extract the timing information from various video formats with vertical serration and output the syncs and relevant timing signals in CMOS logic. Its high performance, rich feature set, and easy application permit use in critical systems where low jitter is a crucial parameter, like in broadcast video and next-generation HDTV/DTV equipment. The device can operate from a supply voltage between 3.3V and 5V. The only required external components are bypass capacitors at the power supply pins, an input coupling capacitor at pin 4, and a R_{EXT} resistor at pin 1. Refer to the application circuit in *Figure 2*.

Internal Reference Voltage and R_{EXT}

The R_{EXT} external resistor establishes the internal bias current and precise reference voltage to assure proper operation of the LMH1981 over a wide temperature range. For optimal performance, R_{EXT} should be a 10 kΩ 0.1% resistor with a temperature coefficient under 100 ppm/˚C. See the **PCB LAYOUT CONSIDERATIONS** section for more information about the R_{EXT} component placement.

Note: The R_{EXT} resistor serves a different function than the "R_{SET} resistor" used in older generations of sync separators (i.e.: LM1881). Previously, the R_{SET} value was adjusted to accommodate different input scan line frequencies. The R_{SET} adjustment was outmoded for the LMH1981, which automatically detects the input line rate to support various video formats without electrical or physical intervention.

Automatic Format Detection and Switching

Automatic format detection eliminates the need for external programming via a microcontroller or R_{SET} resistor. The device outputs will respond correctly to video format switching after a hold-off period has been satisfied. Unlike other sync separators, the LMH1981 does not require the power to be cycled in order to guarantee correct outputs after switching between video formats. See the **Sync-Lock Condition for Output Accuracy** sub-section for details on sync-locking.

Advanced Video Sync Processing

The LMH1981 features 50% sync slicing to provide accurate and robust sync separation, even in the presence of irregular sync amplitudes from attenuated or improperly terminated sources and noise. Adaptive sync slicing provides excellent output timing jitter and stability against variations in input signal amplitude and temperature. The sync separator also supports SDTV, EDTV, and HDTV formats, and is compatible with bi-level and tri-level syncs. Bi-level syncs will be sliced at the 50% point between the sync tip and video blank level. Tri-level syncs will be sliced at the positive zero-crossing of the tri-level sync signal, which is the 50% point between the negative and positive sync tips.

Macrovision Compatibility

The LMH1981 is compatible with the Macrovision Video Copy Protection System commonly used in VHS and DVD video sources, which inserts pseudo-sync pulses in the video blanking signal. These Macrovision-embedded pulses will be effectively ignored by the sync separator, and the outputs will not be affected.

VIDEO INPUT

Video Standards Supported

The LMH1981 supports sync separation for the following standard video interfaces and formats:

- Composite (CVBS) and S-Video (Y/C): NTSC, PAL, SECAM
- Component (YP_BP_R):
  - SDTV with bi-level sync: 480i /60, 576i /50
  - EDTV with bi-level sync: 480p /60, 576p /50
  - HDTV with tri-level sync: 720p /60, 1080i /50/60, 1080p /24/25/30/50/60
- Computer Video: RGsB (Sync on green)

Video Input Requirements

The video input at pin 4 accepts Composite, Y from Y/C and YP_BP_R, and G from Sync on green, with negative-going bi-level sync or HD tri-level sync between 0.5 V_{PP} and 2 V_{PP}. The video input signal should be AC coupled through a coupling capacitor to minimize droop voltage and prevent the signal at V_{IN} from going below the input sync clamp level. The video source should be properly terminated with 75Ω to ensure correct input amplitude and minimize video & sync distortion due to reflections. In extreme cases, the LMH1981 can handle unterminated (2 V_{PP}) and double-terminated (0.5 V_{PP}) input conditions assuming a typical 1 V_{PP} video signal.

LOGIC OUTPUTS

Most of the logic outputs are held high in the absence of a video input signal, except for the odd/even field and video format outputs, which both have special logic signaling for different video formats, and composite sync output.

Sync-Lock Condition for Output Accuracy

When a new input signal is detected, the outputs will begin to produce timing signals; however, these signals may not be accurate until a hold-off period or "sync-lock condition" has been satisfied. The sync separator requires some time to identify the new video format and process the sync information before the outputs are accurate. $T_{SYNC\text{-}LOCK}$ is the maximum period from when the new input signal starts, to when the syncs are locked and the output signals are valid. It is recommended that the outputs are used only after $T_{SYNC\text{-}LOCK}$ condition has been satisfied.

Composite Sync Output

The composite sync output (pin 12) simply reproduces the video input sync pulses below 0 mV (specified video blanking level). This is obtained by clamping the video signal sync tip to the internal clamp voltage at V_{IN} and using 50% sync slicing to strip the sync signal. The resultant composite sync logic signal is buffered out to pin 12. For both bi-level and tri-level syncs, composite sync's negative- and positive-going edges are triggered from the 50% points of the input sync's leading negative- and positive-going edges, respectively, with a propagation delay.

Horizontal Sync Output

The horizontal sync output (pin 7) produces an active low horizontal sync logic signal with very low jitter on its leading negative-going edge (reference edge). For bi-level sync signals, the horizontal sync leading edge is triggered from the input sync leading edge reference with a propagation delay.

Application Information (Continued)

For tri-level sync, the horizontal sync leading edge is triggered from the positive zero-crossing reference of the tri-level sync input with a propagation delay.

The horizontal sync output has excellent jitter performance on its leading, negative-going edge reference because it was optimized for video systems, which are almost always negative-edge triggered. When the horizontal sync signal is used in a positive-edge triggered system, like FPGA PLL, the horizontal sync signal must be inverted beforehand to produce positive-going edges with low jitter. The horizontal sync trailing positive-going edge should **never** be used as the reference/triggered edge. This is because the horizontal sync trailing edges are reconstructed for the equalization and serration pulses during the vertical interval.

The LMH1981 horizontal sync edge-to-edge jitter is measured using the input-referred jitter test methodology on a real-time digital oscilloscope by triggering on the input sync reference edge and monitoring the horizontal sync leading edge reference with 4-sec. variable persistence. From there, the typical edge-to-edge jitter can be measured in the time domain.

Vertical Sync Output

The vertical sync output (pin 8) produces an active low vertical sync logic signal. For bi-level sync, the VSOUT leading negative-going edge is derived from the negative-going edge of the first vertical serration pulse with a propagation delay. For tri-level sync, the VSOUT leading edge is derived from the positive zero-crossing of the first vertical serration pulse with a propagation delay. The vertical sync output pulse width, T_{VSOUT}, spans approximately three horizontal periods (3H).

Burst/Back Porch Timing Output

The burst/back porch timing output (pin 13) provides an active low logic signal, which is pulsed low for a fixed width during the back porch interval following the horizontal sync pulse. This timing pulse is useful for applications that require black level clamping or DC restoring a video signal.

For composite video, the back porch leading negative-going edge is derived from the input sync trailing positive-going edge with a propagation delay, and the pulse width will span the entire color burst envelope. During the vertical interval, the back porch leading edge is aligned with the positive-going edge of the serration pulse with a propagation delay. For YP_BP_R with bi-level sync and RGsB, the back porch pulse behaves similar to the composite input case above, except the pulse width is shorter due to the absence of a color burst signal. For YP_BP_R with tri-level sync, the pulse is also derived from the input sync trailing negative-going edge with a propagation delay, and the pulse width is similar to the horizontal sync width. During the vertical interval, the back porch leading edge is aligned with the trailing edge of the serration pulse.

Odd/Even Field Output

The odd/even field output (pin 14) provides a special logic signal, which facilitates identification of odd and even fields of interlaced formats, i.e.: 480i and 1080i. For interlaced formats, the odd/even output is logic high during an odd field (field 1) and logic low during an even field (field 2). The odd/even output edge transitions align with the vertical sync leading edge to designate the start of odd and even fields. The output is held at logic high for progressive video formats.

Video Format Output (Lines-per-Frame Data)

The video format output counts the number of horizontal sync pulses per field and automatically doubles it (2 fields per frame) to approximate the total number of vertical scan lines per frame. This vertical line count data is output to VFOUT (pin 9) as 11-bit binary bit stream, clocked out on the 11 consecutive leading edges of horizontal sync after each vertical sync trailing edge. Because the line count is automatically doubled assuming 2 interlaced fields per frame, it must be divided by 2 to correct for progressive formats (1 field/frame). Refer to *Figure 11* and *Figure 12* to see the vertical format output timing for the 1080i interlaced format and *Figure 13* for the 480p progressive format. Outside of these active 11-bits of data, VFOUT is held at logic low.

A sample FPGA implementation to decode the lines-per-frame binary data and resolve the video format could be as follows. The signal from VFOUT could be fed into the serial input (SI) of a serial-to-parallel shift register in a FPGA. The horizontal sync signal may be used for the clock signal (CLK) and vertical sync for the enable (EN) and/or reset (CLR) signals. After the 11-bits are shifted into the register, the lines-per-frame data can be processed by the FPGA and the video format can be determined. This could be used to enable dynamic adjustment of various video system parameters, such as color space or scaler conversions.

Application Information (Continued)

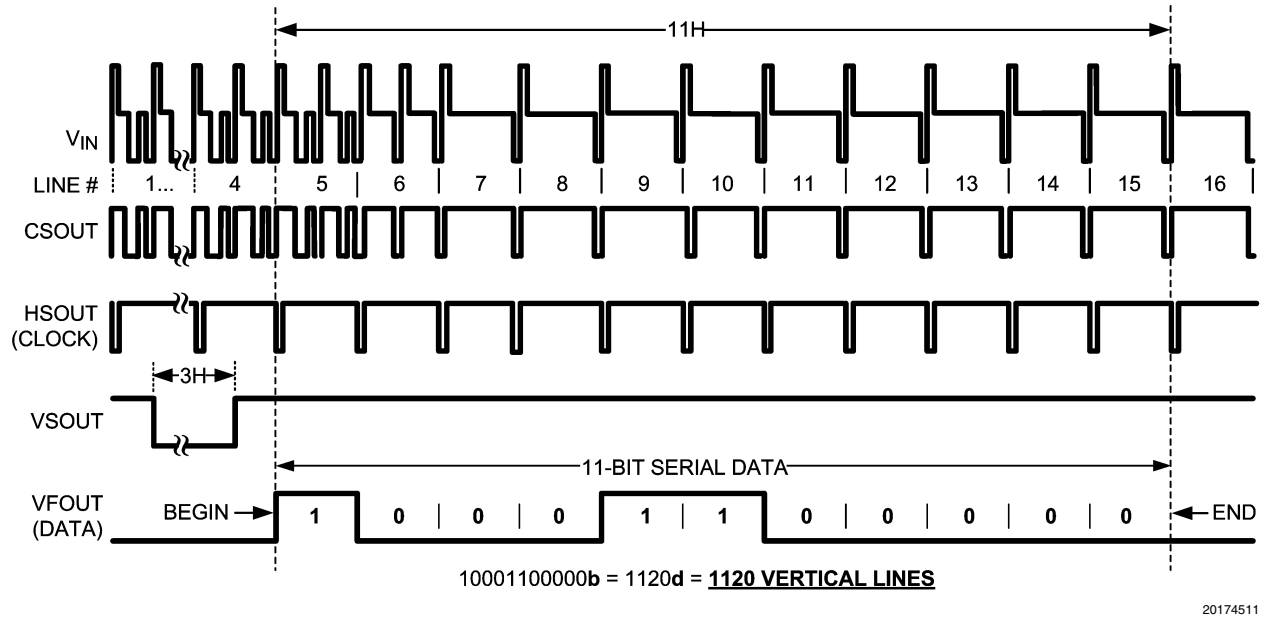


FIGURE 11. Video Format Output for Interlaced Format, 1080i Field 1

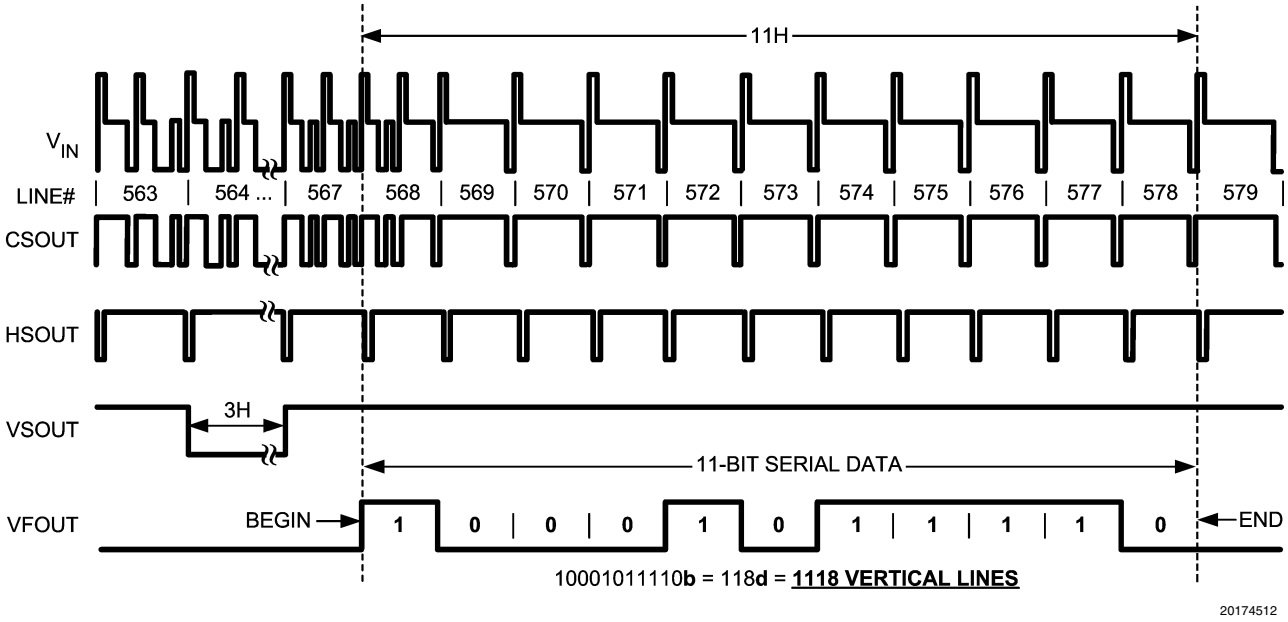


FIGURE 12. Video Format Output for Interlaced Format, 1080i Field 2

Application Information (Continued)

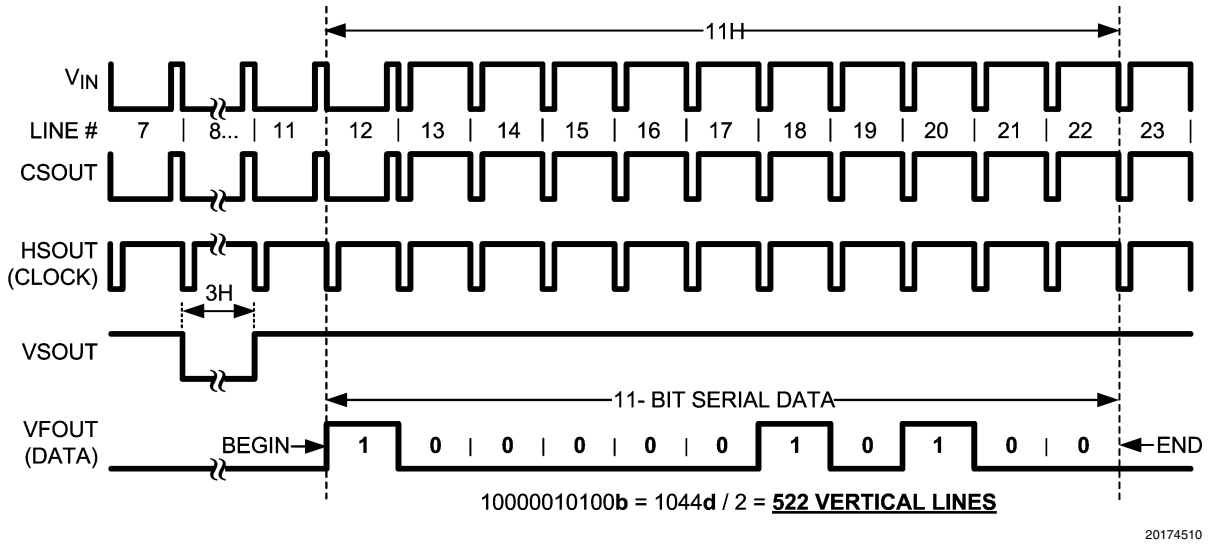


FIGURE 13. Video Format Output for Progressive Format, 480p

PCB LAYOUT CONSIDERATIONS

LMH1981 IC Placement

The LMH1981 should be placed such that critical signal paths are short and direct to minimize PCB parasitics from degrading the high-speed video input and logic output signals.

Ground Plane

A two-layer, FR-4 PCB is sufficient for this device. One of the PCB layers should be dedicated to a single, solid ground plane that runs underneath the device and connects the device GND pins together. The ground plane should be used to connect other components and serve as the common ground reference. It also helps to reduce trace inductances and minimize ground loops. Try to route supply and signal traces on another layer to maintain as much ground plane continuity as possible.

Power Supply Pins

The power supply pins should be connected together using short traces with minimal inductance. When routing the supply traces, be careful not to disrupt the solid ground plane.

For high frequency bypassing, place 0.1 µF SMD ceramic bypass capacitors with very short connections to power supply and GND pins. Two or three ceramic bypass capacitors can be used depending on how the supply pins are connected together. Place a 10 µF SMD tantalum bypass capacitor nearby all three power supply pins for low frequency supply bypassing.

R_{EXT} Resistor

The R_{EXT} resistor should be a 10 kΩ 0.1% SMD resistor with a temperature coefficient under 100 ppm/°C. Place R_{EXT} as close as possible to the device and connect to pin 1 and the ground plane using the shortest possible connections. All input and output signals must be kept away from this pin to prevent unwanted signals from coupling into this pin.

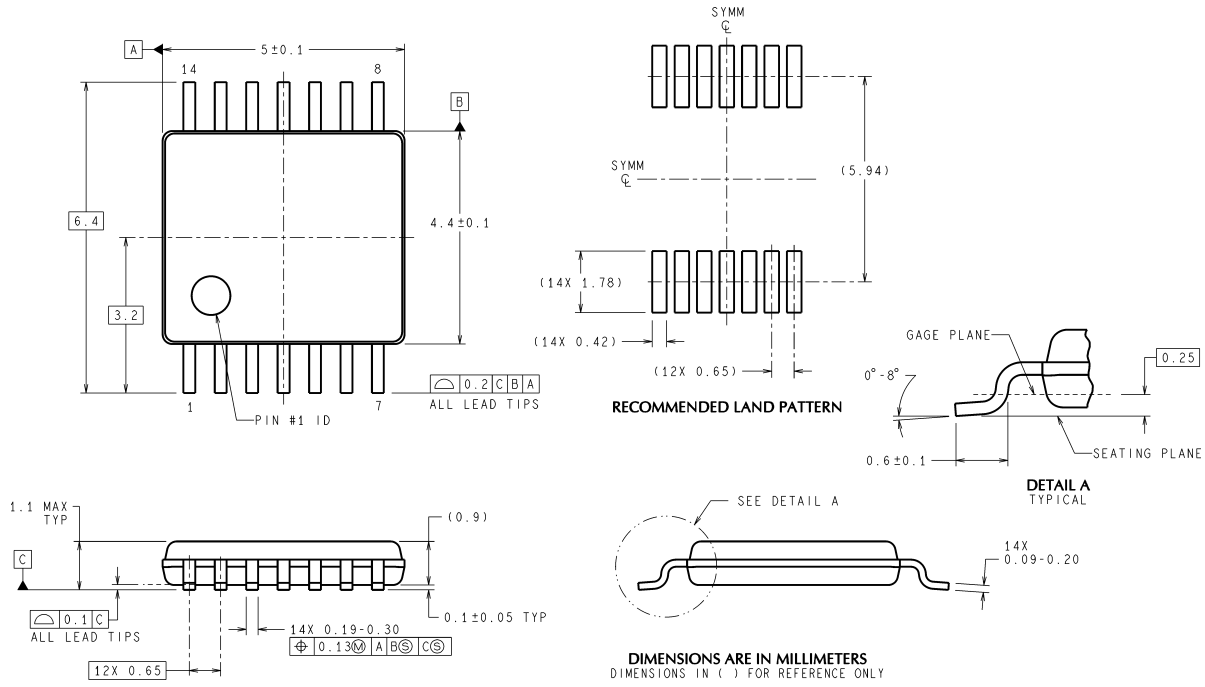
Video Input

The input signal path should be routed using short, direct traces between video source and input pin. Use a 75Ω input termination and a SMD capacitor for AC coupling the video input to pin 4.

Output Routing

The output signal paths should be routed using short, direct traces to minimize parasitic effects that may degrade these high-speed logic signals. This is especially important for the horizontal sync output, in which it is critical to minimize timing jitter. Each output can be protected by current limiting with a small series resistor, like 100Ω.

Physical Dimensions inches (millimeters) unless otherwise noted



MTC14 (Rev D)

14-Pin TSSOP
NS Package Number MTC14

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