National Semiconductor

PRELIMINARY
April 2006

LMH6582/LMH6583
16x8 500 MHz Analog Crosspoint Switch, Gain of 1/ Gain of 2

General Description

The LMH™ family of products is joined by the LMH6582/ LMH6583, a high speed, non-blocking, analog, crosspoint switch. The LMH6582 has a gain of 1 while the LMH6583 has a gain of two. The LMH6582/ LMH6583 is designed for high speed, DC coupled, analog signals like high resolution video (UXGA and higher). The LMH6582/ LMH6583 has 16 inputs and 8 outputs. The non-blocking architecture allows an output to be connected to any input, including an input that is already selected. With fully buffered inputs the LMH6582/ LMH6583 can be impedance matched to nearly any source impedance. The buffered outputs of the LMH6582/ LMH6583 can drive up to two back terminated video loads (75 Ohm load). The outputs and inputs also feature high impedance inactive states allowing high performance input and output expansion for array sizes such as 16 x 16 or 32 x 8 by combining two devices. The LMH6582/ LMH6583 is controlled with a 4 pin serial interface. Both single serial mode and addressed chain modes are available.

The LMH6582/ LMH6583 comes in a 64–pin thermally enhanced TQFP package. It also has diagonally symmetrical pin assignments to facilitate double sided board layouts and easy pin connections for expansion. The package has an exposed thermal pad on the bottom of the package.

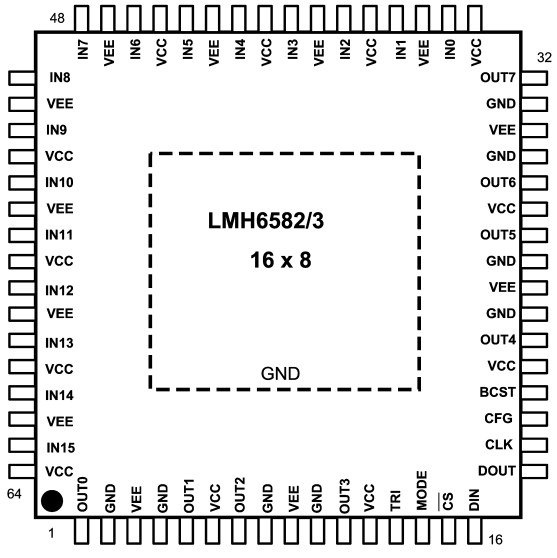
Features

- 16 inputs and 8 outputs
- 64-pin exposed pad TQFP package
- –3 dB bandwidth (V_{OUT} = 0.5V_{PP}) 500 MHz
- –3 dB bandwidth (V_{OUT} = 2V_{PP}) 400 MHZ
- Fast slew rate 3000 V/µs
- Low crosstalk (10 MHz / 100 MHz) –70 / –50 dBc
- Easy to use serial programming 4 wire bus
- Two programming modes Serial & addressed modes
- Symmetrical pinout facilitates expansion.
- Output current ±60 mA
- Two gain options A_V = 1 or A_V = 2

Applications

- Studio monitoring/production video systems
- Conference room mulitmedia video systems
- KVM (keyboard video mouse) systems
- Security/surveillance systems
- Multi antenna diversity radio
- Video test equipment
- Medical imaging
- Wide-band routers & switches

Connection Diagram



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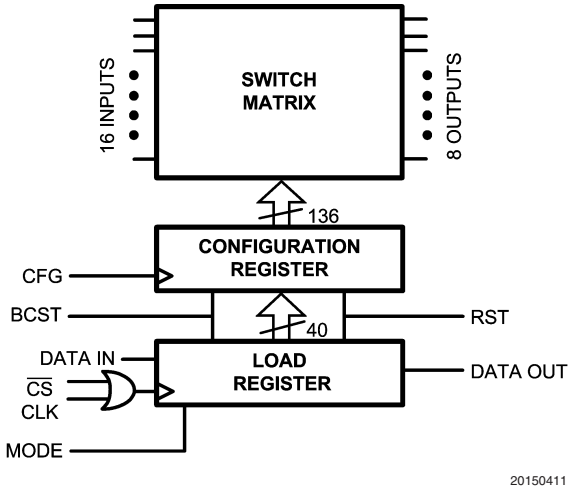
Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_S	±6.2V
I_{IN} (Input Pins)	±20mA
I_{OUT}	(Note 3)
Input Voltage Range	V^- to V^+
Maximum Junction Temperature	+150˚C
Storage Temperature Range	–65˚C to +150˚C
Soldering Information	
Infrared or Convection (20 sec.)	235˚C
Wave Soldering (10 sec.)	260˚C
ESD Tolerance (Note 5)	
Human Body Model	2000V
Machine Model	200V

Operating Ratings (Note 1)

Operating Temperature	–40˚C to	+85˚C
Supply Voltage Range	±3V to	±5.5V
Thermal Resistance	θ_{JA}	θ_{JC}
64–Pin Exposed Pad TQFP	27˚C/W	0.82˚C/W

±5V Electrical Characteristics (Note 2)

Unless otherwise specified, typical conditions are: T_A= 25˚C, A_V = +2, V_S = ±5V, R_L = 100Ω; **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
Frequency Domain Performance						
SSBW	-3dB Bandwidth	V_{OUT} =0.5V_{PP}(Note 11)		500		MHz
LSBW		V_{OUT} = 2V_{PP}		425		
GF	0.1dB Gain Flatness	V_{OUT} = 2V_{PP}		80		MHz
DG	Differential Gain	R_L =150Ω, 3.58MHz/4.43MHz				%
DP	Differential Phase	R_L = 150Ω, 3.58MHz/4.43MHz				deg
Time Domain Response						
t_r	RiseTime	0.5V Step, 10% to 90%				ns
		2V Step, 10% to 90%		1		ns
t_f	Fall Time	0.5V Step, 10% to 90%				ns
		2V Step, 10% to 90%		1		ns
OS	Overshoot	2V Step		5		%
SR	Slew Rate	6V_{PP}, 10% to 90% (Note 6)		3000		V/µs
t_s	Settling Time	4V Step, V_{out}within 0.1%				ns
Distortion And Noise Response						
HD2	2nd Harmonic Distortion	2V_{PP}, 5MHz				dBc
HD3	3rd Harmonic Distortion	2V_{PP}, 5MHz)				dBc
e_n	Input Referred Voltage Noise	>1MHz		7		nV/$\sqrt{Hz}$
i_n	Input Referred Noise Current	>1MHz		2		pA/$\sqrt{Hz}$
	Switching Time					ns
XTLK	CrossTalk	All Hostile, f=100MHz		–50		dBc
ISOL	Off Isolation	f=100MHz		–65		dBc
Static, DC Performance						
A_V	Gain	LMH6582	0.989	0.99	0.991	
A_V	Gain	LMH6583	1.98	2.00	2.02	
V_{os}	Output Offset Voltage			±7		mV
TCV_{os}	Output Offset Voltage Average Drift	(Note 10)				µV/˚C
I_B	Input Bias Current	Non-Inverting (Note 9)		–7		µA
TCI_B	Input Bias Current Average Drift	Non-Inverting (Note 10)				nA/˚C
V_O	Output Voltage Range	R_L = 100Ω		±3.5		V

±5V Electrical Characteristics (Note 2) (Continued)

Unless otherwise specified, typical conditions are: T_A= 25˚C, A_V = +2, V_S = ±5V, R_L = 100Ω; **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
PSRR	Power Supply Rejection Ratio			46		dB
I_S	Supply Current	$R_L = \infty$		110		mA
	Tri State Supply Current	TRI pin > 2.0V		25		mA
Miscellaneous Performance						
R_{IN}	Input Resistance	Non-Inverting				MΩ
C_{IN}	Input Capacitance	Non-Inverting				pF
R_O	Output Resistance	Closed Loop				mΩ
CMVR	Input Common ModeVoltage Range			±3.0		V
I_O	Output Current	Sourcing, V_O = 0 V		±60		mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Electrical Table typical values apply only for the conditions indicated. See Note 8 for limit specifications.

Note 3: The maximum output current (I_{OUT}) is determined by device power dissipation limitations.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is P_D= ($T_{J(MAX)}$ — T_A)/ θ_{JA}. All numbers apply for package soldered directly into a 2 layer PC board with zero air flow.

Note 5: Human body model: 1.5kΩ in series with 100pF. Machine model: 0Ω in series with 200pF.

Note 6: Slew Rate is the average of the rising and falling edges.

Note 7: Typical numbers are the most likely parametric norm.

Note 8: Room Temperature limits are 100% production tested at 25˚C. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

Note 9: Negative input current implies current flowing out of the device.

Note 10: Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

Note 11: Parameter is guaranteed by design.

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
64–Pin QFP	LMH6582YA	LMH6582YA	xx Units	VXE64A
	LMH6583YA	LMH6583YA	xx Units	

Application Section

INTRODUCTION

The LMH6582/ LMH6583 is a high speed, fully buffered, non blocking, analog crosspoint switch. Having fully buffered inputs allows the LMH6582/ LMH6583 to accept signals from low or high impedance sources without the worry of loading the signal source. The fully buffered outputs will drive 75 or 50 Ohm back terminated transmission lines with no external components other than the termination resistor. The LMH6582/ LMH6583 can have any input connected to any (or all) output(s). Conversely, a given output can have only one associated input.

INPUT AND OUTPUT EXPANSION

The LMH6582/ LMH6583 has high impedance inactive states for both inputs and outputs allowing maximum flexibility for Crosspoint expansion. In addition the LMH6582/ LMH6583 employs diagonal symmetry in pin assignments. The diagonal symmetry makes it easy to use direct pin to pin vias when the parts are mounted on opposite sides of a board. As an example two LMH6582/ LMH6583 chips can be combined on one board to form either an 16 x 16 crosspoint or a 32x8 crosspoint. To make a 16 x 16 cross-point all 16 input pins would be tied together (Input 0 on side 1 to input 15 on side 2 and so on) while the 8 output pins on each chip would be left separate. To make the 32 x 8 crosspoint, the 8 outputs would be tied together while all 32 inputs would remain independent. In the 32 x 8 configuration it is important not to have 2 connected outputs active at the same time. With the 16 x 16 configuration, on the other hand, having two connected inputs active is a valid state. Crosspoint expansion as detailed above has the advantage that the signal path has only one crosspoint in it at a time. Expansion methods that have cascaded stages will suffer bandwidth loss far greater than the small loading effect of parallel expansion.

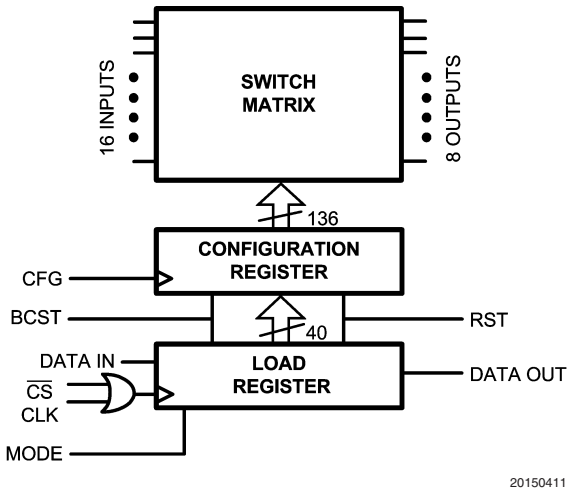
The LMH6582/ LMH6583 has fully buffered inputs and outputs. The inputs provide a low load, high impedance input and ensure maximum performance from a variety of signal sources. The fully buffered outputs will drive up to two back terminated video loads. When disabled, the outputs are in a high impedance state. When making thermal calculations the output loading conditions will be a key consideration. Please see the section on thermal management.

DRIVING CAPACITIVE LOADS

Capacitive output loading applications will benefit from the use of a series output resistor R_{OUT}. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. The chart “Suggested R_{OUT} vs. Cap Load” gives a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for 0.5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{OUT} can be reduced slightly from the recommended values. When driving transmission lines the 50 or 75 Ohm matching resistor makes the series output resistor unnecessary.

DIGITAL CONTROL

Block Diagram



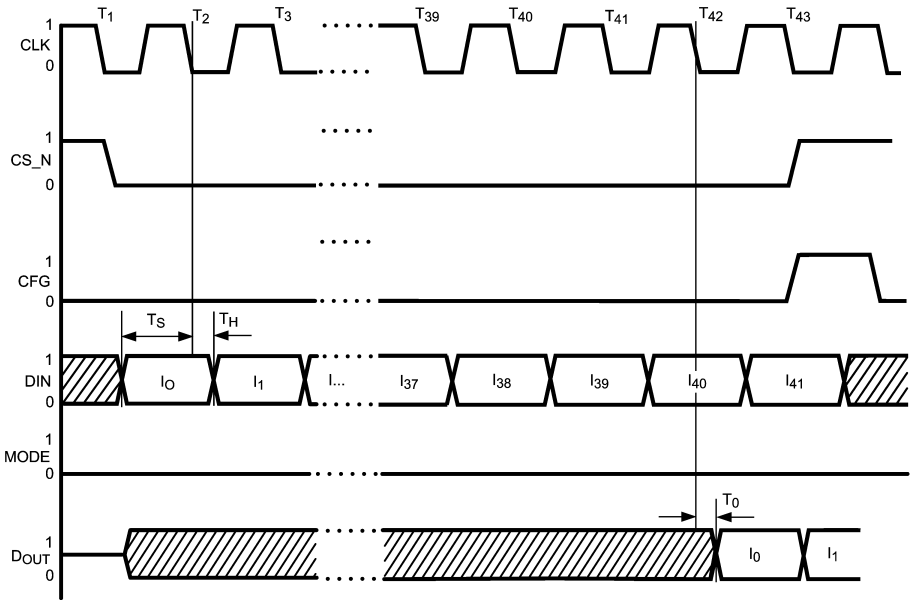
The LMH6582/ LMH6583 has internal control registers that store the programming states of the crosspoint switch. The logic is two staged to allow for maximum programming flexibility. The first stage of the control logic is tied directly to the crosspoint switching matrix. This logic consists of one register for each output that stores the on/off state and the address of which input to connect to. These registers are not directly accessible by the user. The second level of logic is another bank of registers identical to the first, but set up as shift registers. These registers are accessed by the user via the serial input bus. As described further below, there are two modes for programing the LMH6582, Serial Mode and Addressed Mode.

The LMH6582/ LMH6583is programmed via a serial input bus with the support of 4 other digital control pins. The Serial bus consists of a clock pin (CLK), a serial data in pin (DIN), and a serial data out pin (DOUT). The serial bus is gated by a chip select pin. The chip select pin is active low. While the chip select pin is high all data on the serial input pin and clock pins is ignored. When the chip select pin is brought low the internal logic is set to begin receiving data by the first positive transition (0 to 1) of the clock signal. The first data bit is clocked in on the next negative transition. All input data is read from the bus on the negative edge of the clock signal. Once the last valid data has been clocked in, either the chip select pin must go high or, the clock signal must stop. Otherwise invalid data will be clocked into the chip. The data clocked into the chip is not transferred to the crosspoint matrix until the CFG pin is pulsed high. This is the case regardless of the state of the Mode pin. The CFG pin is not dependent on the state of the Chip select pin. If no new data is clocked into the chip subsequent pulses on the CFG pin will have no effect on device operation.

The programming format of the incoming serial data is selected by the MODE pin. When the mode pin is HIGH the crosspoint can be programmed one output at a time by entering a string of data that contains the address of the output that is going to be changed (Addressed Mode). When the mode pin is LOW the crosspoint is in Serial Mode. In this mode the crosspoint accepts a 40 bit array of data that programs all of the outputs with the same data stream. In both modes the data fed into the chip does not change the

Application Section (Continued)

chip operation until the Configure pin is pulsed high. The configure and mode pins are independent of the chip select pin.



Timing Diagram for Serial Mode

Serial Mode Data Frame (First 2 Words)

Output 0					Output 1				
Input Address				On=0	Input Address				On=0
LSB			MSB	Off=1	LSB			MSB	Off=1
0	1	2	3	4	5	6	7	8	9

Off = TRI-STATE®, Bit 0 is first bit clocked into device.

Serial Mode Data Frame (Continued)

Output 2					Output 3				
Input Address				On=0	Input Address				On=0
LSB			MSB	Off=1	LSB			MSB	Off=1
10	11	12	13	14	15	16	17	18	19

Serial Mode Data Frame (Continued)

Output 4					Output 5				
Input Address				On=0	Input Address				On=0
LSB			MSB	Off=1	LSB			MSB	Off=1
20	21	22	23	24	25	26	27	28	29

Serial Mode Data Frame (Last 2 Words)

Output 6					Output 7				
Input Address				On=0	Input Address				On=0
LSB			MSB	Off=1	LSB			MSB	Off=1
30	31	32	33	34	35	36	37	38	39

Bit 39 is last bit clocked into device.

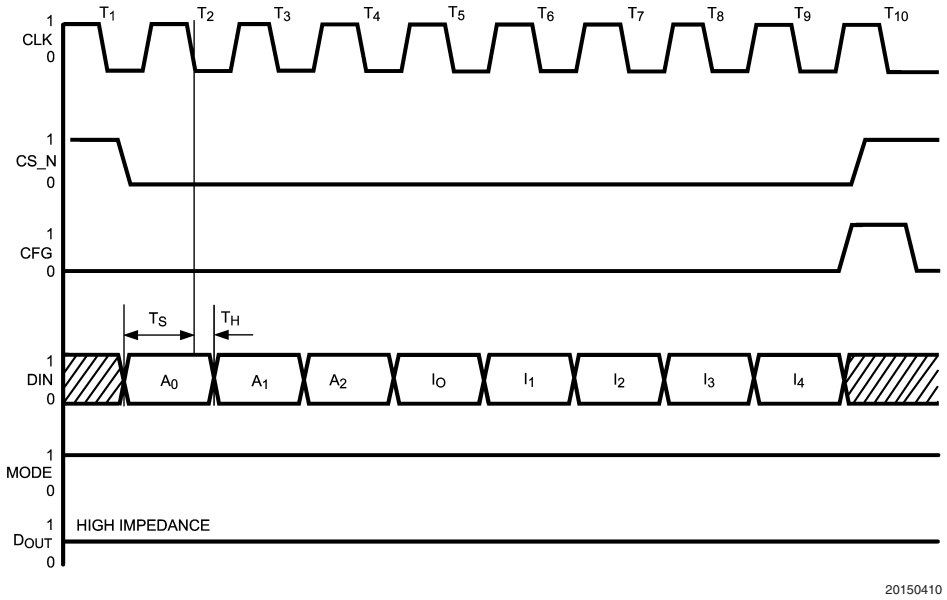
Application Section (Continued)

Serial programming mode is the mode selected by bringing the MODE pin low. In this mode a stream of 40 bits programs all 8 outputs of the crosspoint. The data is fed to the chip as shown in the table above. The table is arranged such that the first bit clocked into the crosspoint register is labeled bit number 0. The register labeled Load Register in the block diagram is a shift register. If the chip select pin is left low after the valid data is shifted into the chip and if the clock signal keeps running then additional data will be shifted into the register, and the desired data will be shifted out.

Addressed programming mode makes it possible to change only one output register at a time. To utilize this mode the mode pin must be High. All other pins function the same as in serial programming mode except that the word clocked in is much smaller and is directed only at the output specified. In addressed mode the data format is shown below in the table titled *Table Addressed Mode Word Format General Case*.

Timing Diagram

Addressed Mode Timing Diagram



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Addressed Mode Word Format General Case

Output Address			Input Address				TRI-STATE
LSB		MSB	LSB			MSB	1= TRI-STATE 0=On
0	1	2	3	4	5	6	7

Bit 0 is first bit clocked into device.

DAISY CHAIN OPTION IN SERIAL MODE

The LMH6582/ LMH6583 supports daisy chaining of the serial data stream between multiple chips. This feature is available only in the Serial programming mode. To use this feature serial data is clocked into the first chip DIN pin, and the next chip DIN pin is connected to the DOUT pin of the first chip. Both chips may share a chip select signal, or the second chip can be enabled separately. When the chip select pin goes low on both chips a double length word is clocked into the first chip. As the first word is clocking into the first chip the second chip is receiving the data that was originally in the shift register of the first chip. When a full 40 bits have been clocked into the first chip the next clock cycle begins moving the first frame of the new configuration data into the second chip. With a full 80 clock cycles both chips have valid data and the chip select pin of both chips should be brought high to prevent the data from overshooting. A configure pulse will activate the new configuration on both chips simultaneously, or each chip can be configured separately. The mode, chip select, configure and clock pins of both chips can be tied together and driven from the same sources. If more than 3 chips are daisy-chained in a row it will be necessary to lower the clock speed to compensate for data latency between the chips (unless the clock signal is delayed for the end of chain chips). 4 chips daisy chained should be clocked at no more than 5MHz.

SPECIAL CONTROL PINS

The LMH6582/ LMH6583 has two special control pins that function independent of the serial control bus. One of these pins is the TRI-STATE (TRI) pin. The TRI pin is active high meaning that a logic 1 level the chip is set to the TRI-STATE mode. In TRI-STATE mode all the registers are set to input address 0 and all the outputs are turned off. In this configuration the device draws only 20 mA. The TRI-STATE pin can used as a shutdown function to reduce power consumption. The other special control pin is the broadcas t(BCST) pin. The BCST pin is also active high and sets all the outputs to

Application Section (Continued)

the on state connected to input 0. This is sometimes referred to as broadcast mode, where input 0 is broadcast to all 8 outputs.

THERMAL MANAGEMENT

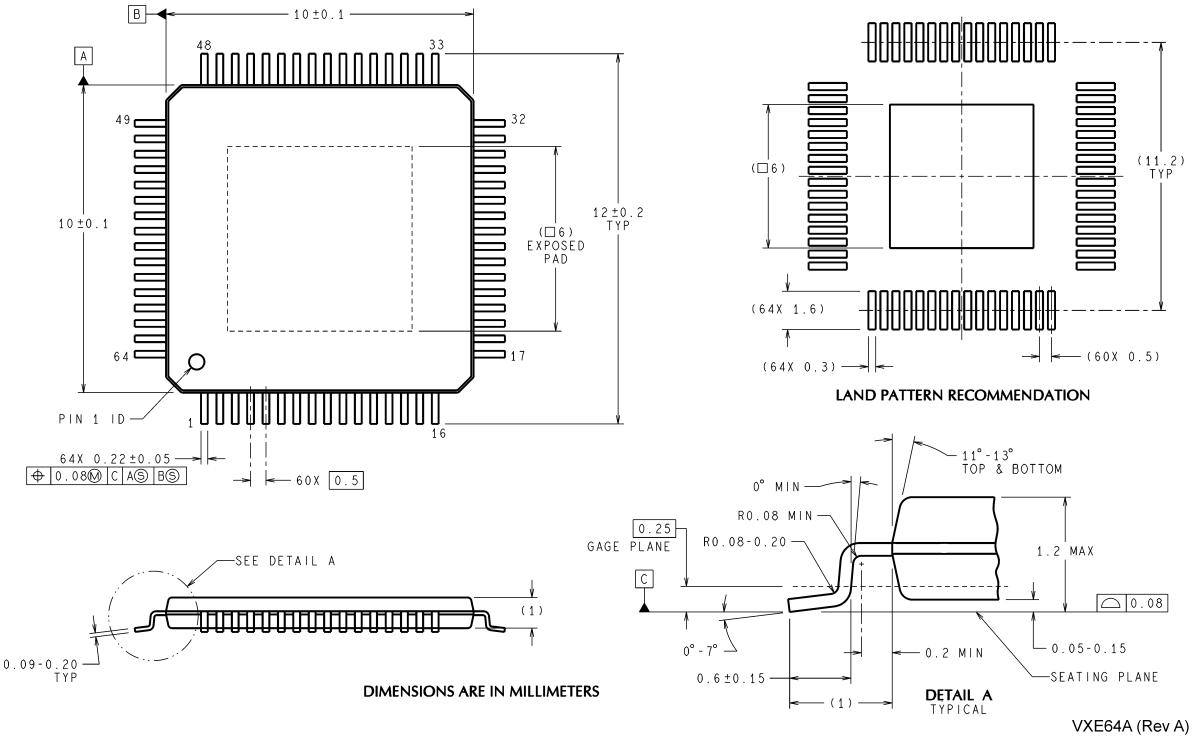
The LMH6582/ LMH6583 is packaged in a thermally enhanced Quad Flat Pack package. Even so, it is a high performance device that produces a significant amount of heat. With a ±5V supply, the LMH6582/ LMH6583 will dissipate approximately 1.1 W of idling power with all outputs enabled. In addition, each equivalent video load (150 Ohms) connected to the outputs should be budgeted 30mW of power. For a typical application with one video load for each output this would be a total power of 1.14 W. With a θJA of 35˚C/W this will result in the silicon being 40˚C over the ambient temperature. A more aggressive application would be two video loads per output which would result in 1.38 W of power dissipation. This would result in a 48˚C temperature rise. For heavier loading, the QFP package thermal performance can be significantly enhanced with an external heat sink and by providing for moving air ventilation. Also, be sure to calculate the increase in ambient temperature from all devices operating in the system case. Because of the high power output of this device, thermal management should be considered very early in the design process. Generous passive venting and vertical board orientation may avoid the need for fan cooling or heat sinks.

PRINTED CIRCUIT LAYOUT

Generally, a good high frequency layout will keep power supply and ground traces away from the input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). If digital control lines must cross analog signal lines (particularly inputs) it is best if they cross perpendicularly. National Semiconductor suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board Part Number
LMH6582 LMH6583	64–Pin TQFP	TBD

Physical Dimensions inches (millimeters) unless otherwise noted



64-Pin Exposed Pad QFP
NS Package Number VXE64A

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