National Semiconductor

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LP3972 Power Management Unit for Advanced Application Processors

General Description

The LP3972 is a multi-function, programmable Power Management Unit, designed especially for advanced application processors. The LP3972 is optimized for low power handheld applications and provides 6 low dropout, low noise linear regulators, three DC/DC magnetic buck regulators, a back-up battery charger and two GPIO's. A high speed serial interface is included to program individual regulator output voltages as well as on/off control.

Key Specifications

Buck Regulators

- Programmable V_{OUT} from 0.725 to 3.3V
- Up to 95% efficiency
- Up to 1.6A output current
- ±3% output voltage accuracy

LDO's

- Programmable V_{OUT} of 1.0V–3.3V
- ±3% output voltage accuracy
- 150/300/400 mA output currents
  - — LDO RTC 30 mA
  - — LDO 1 300 mA
  - — LDO 2 150 mA
  - — LDO 3 150 mA
  - — LDO 4 150 mA
  - — LDO 5 400 mA
- 100 mV (typ) dropout

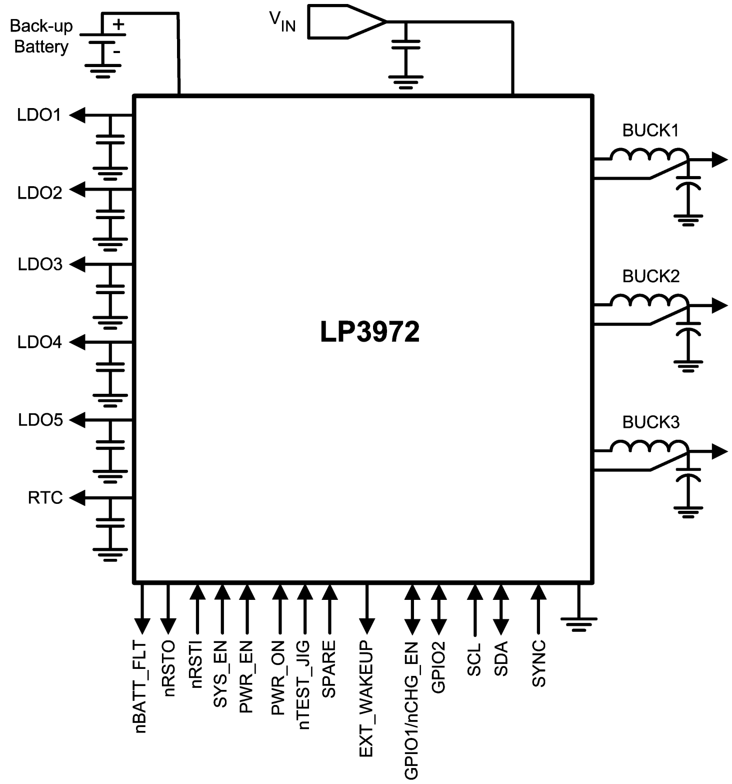
Features

- Compatible with advanced applications processors requiring DVM (Dynamic Voltage Management)
- Three buck regulators for powering high current processor functions or I/O's
- 6 LDO's for powering RTC, peripherals, and I/O's
- Backup battery charger with automatic switch for lithium-manganese coin cell batteries and Super capacitors
- I^2C compatible high speed serial interface
- Software control of regulator functions and settings
- Precision internal reference
- Thermal overload protection
- Current overload protection
- Tiny 40-pin 5x5 mm LLP package

Applications

- PDA phones
- Smart phones
- Personal Media Players
- Digital cameras
- Application processors
  - — Intel Xscale
  - — Freescale
  - — Samsung

Simplified Application Circuit



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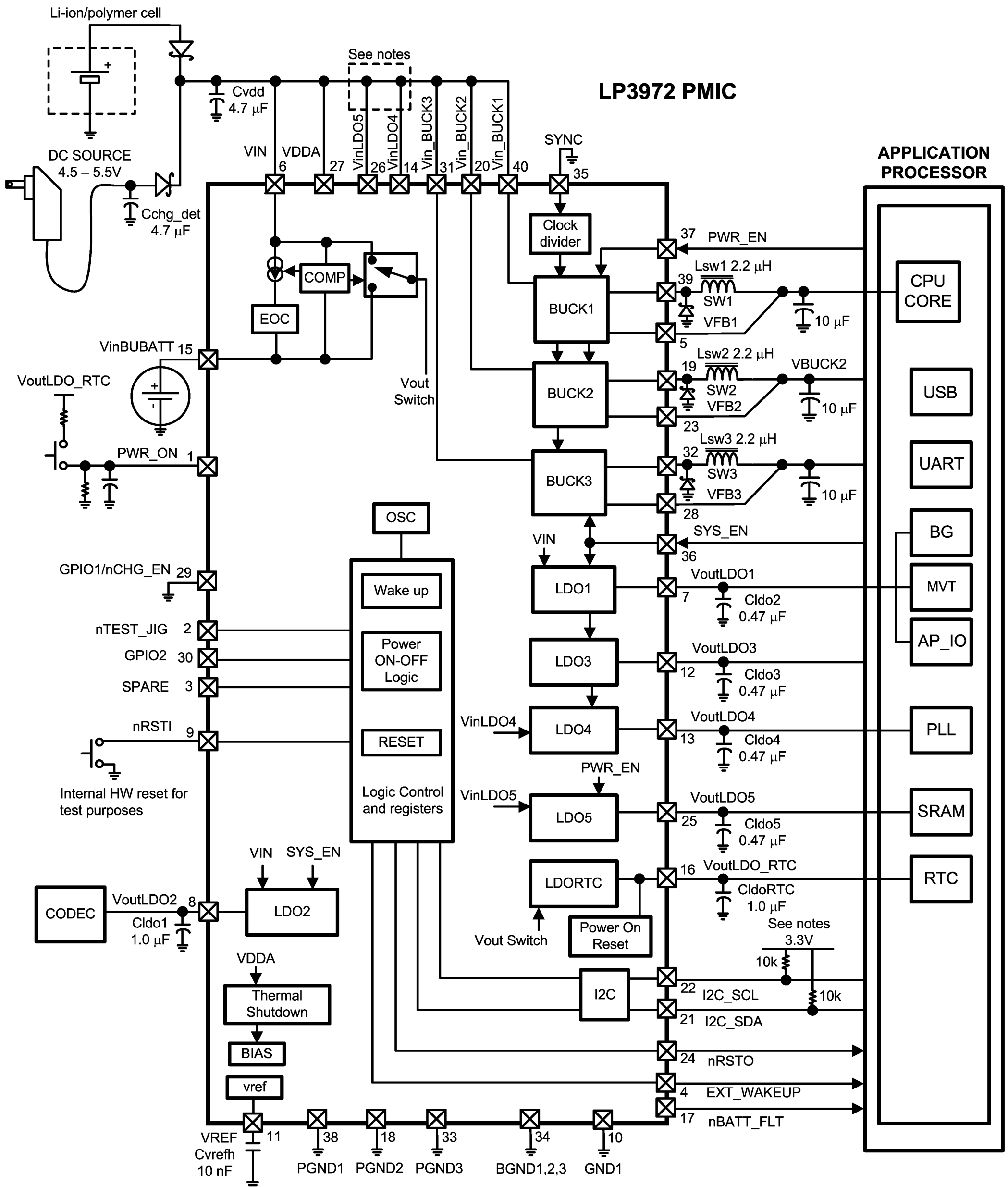
Simplified Application Circuit (Continued)



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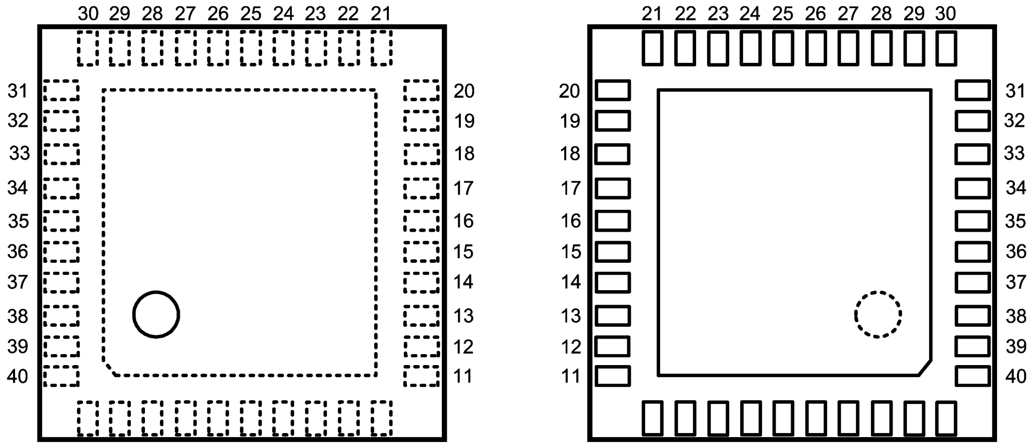
- The I^2C lines are pulled up via a I/O source
- V_{IN}LDO4, 5 can either be powered from main battery source, or by a buck regulator or V_{IN}.

Connection Diagrams and Package Mark Information

40-Pin Leadless Leadframe Package
NS Package Number SQF40A



Top View **Bottom View**

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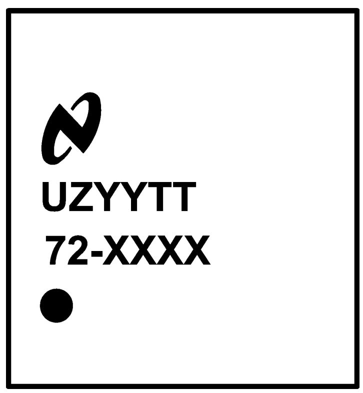
Note: Circle marks pin 1 position.

Package Mark



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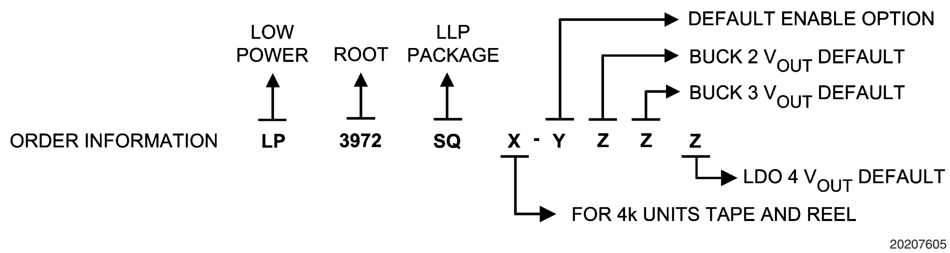
Top View

Note: The actual physical placement of the package marking will vary from part to part.
(*) UZTTYY format: 'U' — wafer fab code; 'Z' — assembly code; 'XY' 2 digit date code; 'TT' — die run code.
See http://www.national.com/quality/marking_convertion.html for more information on marking information.

Ordering Information

Voltage Option	Order Number	Package Type	NSC Package Drawing	Package Marking	Supplied As
Voltage A514	LP3972SQ-A514	40 lead LLP	SQF040A	72-A514	1000 tape & reel
Voltage A514	LP3972SQX-A514	40 lead LLP	SQF040A	72-A514	4500 tape & reel
Voltage A413	LP3972SQ-A413	40 lead LLP	SQF040A	72-A413	1000 tape & reel
Voltage A413	LP3972SQX-A413	40 lead LLP	SQF040A	72-A413	4500 tape & reel
Voltage E514	LP3972SQ-E514	40 lead LLP	SQF040A	72-E514	1000 tape & reel
Voltage E514	LP3972SQX-E514	40 lead LLP	SQF040A	72-E514	4500 tape & reel
Voltage I514	LP3972SQ-I514	40 lead LLP	SQF040A	72-I514	1000 tape & reel
Voltage I514	LP3972SQX-I514	40 lead LLP	SQF040A	72-I514	4500 tape & reel



Default V_{OUT} Coding

Z	Default V_{OUT}
0	1.3
1	1.8
2	2.5
3	2.8
4	3.0
5	3.3
6	1.0
7	1.4
8	1.2
9	1.25

Pin Descriptions

Pin #	Name	I/O	Type	Description
1	PWR_ON	I	D	CPU Wakeup input, this can be a push button event to indicate the device has been turned on. Phone / PDA main power button. Signal is debounced internally on the PMIC. If the POWER_ON is held low this will indicate to the PMIC to turn off. Active high Polarity
2	nTEST_JIG	I	D	This is a input signal used for a turn on event coming from the bed of nails tester during production. Active low polarity.
3	SPARE	I	D	CPU Wakeup input to indicate that a HW external event has occurred, i.e. flipping the cell phone to power up the display.
4	EXT_WAKEUP	O	D	This signal is asserted when DC POWER source has been asserted, or when the PWR_ON button is held down to turn off the PMIC. Wake up on power detection, and power down detection.
5	FB1	I	A	Buck1 input feedback terminal
6	V_{IN}	I	PWR	Battery Input (Internal circuitry and LDO1-3 power input)
7	V_{OUT} LDO1	O	PWR	LDO1 output
8	V_{OUT} LDO2	O	PWR	LDO2 output
9	nRSTI	I	D	Active low Reset pin. Signal used to reset the IC (by default is pulled high internally). Typically a push button reset.
10	GND1	G	G	Ground
11	VREF	O	A	Bypass Cap. for the high internal impedance reference.
12	V_{OUT} LDO3	O	PWR	LDO3 output
13	V_{OUT} LDO4	O	PWR	LDO4 output
14	V_{IN} LDO4	I	PWR	Power input to LDO4, this can be connected to either from a 1.8V supply to main Battery supply.
15	V_{IN} BUBATT	I	PWR	Back Up Battery input supply.
16	V_{OUT} LDO_RTC	O	PWR	LDO_RTC output supply to the RTC of the application processor.
17	nBATT_FLT	O	D	Main Battery fault output, indicates the main battery is low (discharged) or the dc source has been removed from the system. This gives the processor an indicator that the power will shut down. During this time the processor will operate from the back up coin cell.
18	PGND2	G	G	Buck2 NMOS Power Ground
19	SW2	O	PWR	Buck2 switcher output
20	V_{IN} Buck2	I	PWR	Battery input power to Buck2
21	SDA	I/O	D	I^2C Data (Bidirectional)
22	SCL	I	D	I^2C Clock
23	FB2	I	A	Buck2 input feedback terminal
24	nRSTO	O	D	Reset output from the PMIC to the processor
25	V_{OUT} LDO5	O	PWR	LDO5 output
26	V_{IN} LDO5	I	PWR	Power input to LDO5, this can be connected to V_{IN} or to a separate 1.8V supply.
27	VDDA	I	PWR	Analog Power for VREF, BIAS
28	FB3	I	A	Buck3 Feedback
29	GPIO1 / nCHG_EN	I/O	D	General Purpose I/O / Ext. backup battery charger enable pin. This pin enables the main battery / DC source power to charge the backup battery. This pin toggled via the application processor. By grounding this pin the DC source continuously charges the backup battery
30	GPIO2	I/O	D	General Purpose I/O
31	V_{IN} Buck3	I	PWR	Battery input power to Buck3

Pin Descriptions (Continued)

Pin #	Name	I/O	Type	Description
32	SW3	O	PWR	Buck3 switcher output
33	PGND3	G	G	Buck3 NMOS Power Ground
34	BGND1,2,3	G	G	Bucks 1, 2 and 3 analog Ground
35	SYNC	I	D	Frequency Synchronization: Connection to an external clock signal PLL to synchronize the PMIC internal oscillator.
36	SYS_EN	I	D	Input Digital enable pin for the high voltage power domain supplies. Output from the Monahans processor.
37	PWR_EN	I	D	Digital enable pin for the Low Voltage domain supplies. Output signal from the Monahans processor
38	PGND1	G	G	Buck1 NMOS Power Ground
39	SW1	O	PWR	Buck1 Switcher output
40	VIN Buck1	I	PWR	Battery input power to Buck1

A: Analog Pin D: Digital Pin G: Ground Pin P: Power Pin I: Input Pin I/O: Input/Output Pin O: Output Pin

Note: In this document active low logic items are prefixed with a lowercase “n”

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

All Inputs	−0.3V to +6.5V
GND to GND SLUG	±0.3V
Junction Temperature ($T_{J\text{-}MAX}$)	150˚C
Storage Temperature	−65˚C to +150˚C
Power Dissipation (T_A = 70˚C) (Note 3)	3.2W
Junction-to-Ambient Thermal Resistance θ_{JA} (Note 3)	25˚C/W
Maximum Lead Temp (Soldering)	260˚C

ESD Rating (Note 5)

Human Body Model	2 kV
Machine Model	200V

Operating Ratings

V_{IN} LDO 4,5	2.7V to 5.5V
V_{EN}	1.74 to (V_{IN}
Junction Temperature (T_J)	−40˚C to +125˚C
Operating Temperature (T_A)	−40˚C to +85˚C
Maximum Power Dissipation (T_A = 70˚C) (Notes 3, 4)	2.2W

General Electrical Characteristics

Typical values and limits appearing in normal type apply for T_J = 25˚C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40˚C to +125˚C. (Notes 2, 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}, VDDA, V_{IN} Buck1, 2 and 3	Battery Voltage		**2.7**	3.6	**5.5**	V
V_{IN}LDO4, V_{IN}LDO5	Power Supply for LDO 4 and 5		**1.74**	3.6	**5.5**	V
T_{SD}	Thermal Shutdown (Note 14)	Temperature		160		˚C
		Hysteresis		20		

**No input supply should be higher then VDDA

Supply Specifications (Notes 2, 5)

Supply	V_{OUT} (Volts)		I_{MAX} Maximum Current
	Range (V)	Resolution (mV)	Current (mA)
LDO_RTC	2.8V	N/A	**30 mA dc source 10 mA backup source**
LDO1 (V_{CC}_MVT)	1.7 to 2.0	25	300
LDO2	1.8 to 3.3	100	150
LDO3	1.8 to 3.3	100	150
LDO4	1.0 to 3.3	50-600	150
LDO5 (V_{CC}_SRAM)	0.850 to 1.5	25	400
BUCK 1 (V_{CC}_APPS)	0.725 to 1.5	25	1600
BUCK 2	0.8 to 3.3	50-600	1600
BUCK 3	0.8 to 3.3	50-600	1600

General Electrical Characteristics

Typical values and limits appearing in normal type apply for T_J = 25˚C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40˚C to +125˚C. (Notes 2, 6) (Continued)

Default Voltage Option (Notes 2, 5)

Version	**LP3972SQ-A514**		**LP3972SQ-A413**	
Enable	Version A		Version A	
LDO_RTC	—	2.8	—	2.8
LDO1	SYS_EN	1.8	SYS_EN	1.8
LDO2	SYS_EN	1.8D	SYS_EN	1.8D
LDO3	SYS_EN	3D	SYS_EN	3D
LDO4	SYS_EN	3D	SYS_EN	2.8D
LDO5	PWR_EN	1.4	PWR_EN	1.4
BUCK1	PWR_EN	1.4	PWR_EN	1.4
BUCK2	SYS_EN	3.3	SYS_EN	3
BUCK3	SYS_EN	1.8	SYS_EN	1.8
Version	**LP3972SQ-E514**		**LP3972SQ-I514**	
Enable	Version E		Version I	
LDO_RTC	—	2.8	—	2.8
LDO1	SYS_EN	1.8	SYS_EN	1.8
LDO2	SYS_EN	1.8E	SYS_EN	1.8E
LDO3	SYS_EN	3D	SYS_EN	3E
LDO4	SYS_EN	3D	SYS_EN	3E
LDO5	PWR_EN	1.4	PWR_EN	1.4
BUCK1	PWR_EN	1.4	PWR_EN	1.4
BUCK2	SYS_EN	3.3	SYS_EN	3.3
BUCK3	SYS_EN	1.8	SYS_EN	1.8

Note : E = Regulator is ENABLED during startup
D = Regulator is DISABLED during startup

LDO RTC

Unless otherwise noted, V_{IN} = 3.6V, C_{IN} = 1.0 µF, C_{OUT} = 0.47 µF, C_{OUT} (V_{RTC}) = 1.0 µF ceramic. Typical values and limits appearing in normal type apply for T_J = 25˚C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40˚C to +125˚C. (Notes 2, 6, 7) and (Note 10)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage Accuracy	V_{IN} Connected, Load Current = 1 mA	**2.632**	2.8	**2.968**	V
ΔV_{OUT}	Line Regulation	V_{IN} = (V_{OUT} nom + 1.0V) to 5.5V (Note 11) Load Current = 1 mA			**0.15**	%/V
	Load Regulation	From Main Battery Load Current = 1 mA to 30 mA			**0.05**	%/mA
		From Backup Battery V_{IN} = 3.0V Load Current = 1 mA to 10 mA			**0.5**	
I_{SC}	Short Circuit Current Limit	From Main Battery V_{IN} = V_{OUT} +0.3V to 5.5V		100		mA
		From Backup Battery		30		
V_{IN} - V_{OUT}	Dropout Voltage	Load Current = 10 mA			**375**	mV
I_Q_Max	Maximum Quiescent Current	I_{OUT} = 0 mA		30		µA
TP1	RTC LDO Input Switched from Main Battery to Backup Battery	V_{IN} Falling		2.9		V
TP2	RTC LDO Input Switched from Backup Battery to Main Battery	V_{IN} Rising		3.0		V
C_O	Output Capacitor	Capacitance for Stability	**0.7**	1.0		µF
		ESR	**5**		**500**	mΩ

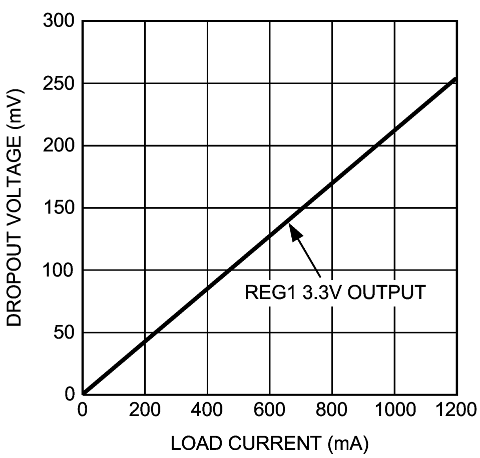
LDO 1 to 5

Unless otherwise noted, V_{IN} = 3.6V, C_{IN} = 1.0 µF, C_{OUT} = 0.47 µF, C_{OUT} (V_{RTC}) = 1.0 µF ceramic. Typical values and limits appearing in normal type apply for T_J = 25˚C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40˚C to +125˚C. (Notes 2, 6, 7, 10, 11, 15) and (Note 16).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage Accuracy (Default V_{OUT})	Load Current = 1 mA	**−3**		**3**	%
ΔV_{OUT}	Line Regulation	V_{IN} =3.1V to 5.0V, (Note 11) Load Current = 1 mA			**0.15**	%/V
	Load Regulation	V_{IN} = 3.6V, Load Current = 1 mA to I_{MAX}			**0.011**	%/mA
I_{SC}	Short Circuit Current Limit	LDO1−4, V_{OUT} = 0V		400		mA
		LDO5, V_{OUT} = 0V		500		
V_{IN} - V_{OUT}	Dropout Voltage	Load Current = 50 mA (Note 7)			**150**	mV
PSRR	Power Supply Ripple Rejection	f = 10 kHz, Load Current = I_{MAX}		45		dB
I_Q	Quiescent Current “On”	I_{OUT} = 0 mA		40		µA
	Quiescent Current “On”	I_{OUT} = I_{MAX}		60		
	Quiescent Current “Off”	EN is de-asserted		0.03		
T_{ON}	Turn On Time	Start up from Shut-down		300		µsec
C_{OUT}	Output Capacitor	Capacitance for Stability 0˚C ≤ T_J ≤ 125˚C	**0.33**	0.47		µF
		−40˚C ≤ T_J ≤ 125˚C	**0.68**	1.0		
		ESR	**5**		**500**	mΩ

LDO dropout voltage vs. Load Current collect data for all LDO's

Dropout Voltage vs. Load Current



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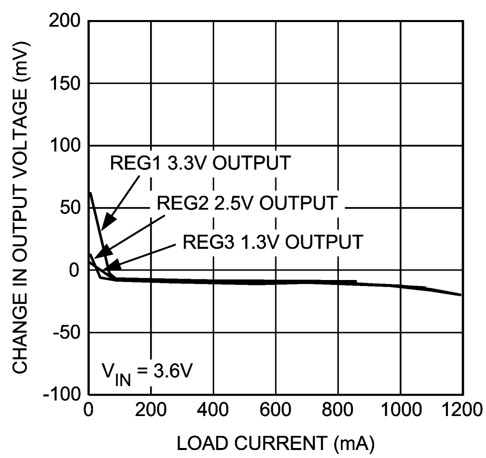
Change in Output Voltage vs. Load Current



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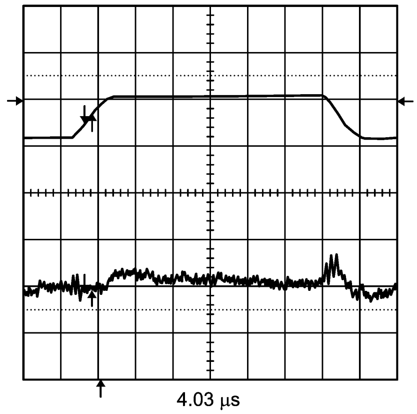
LDO 1 to 5 (Continued)

LDO1 Line Regulation
V_{OUT} = 1.8 volts V_{IN} 3 to 4 volts Load = 100 mA



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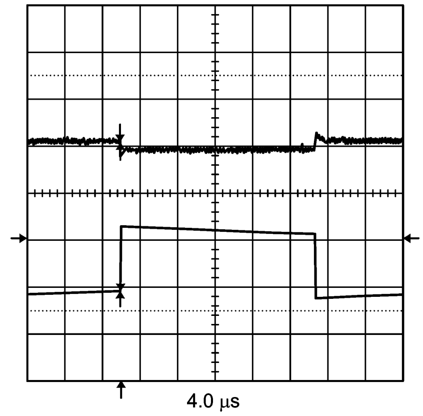
LDO1 Load Transient
V_{IN} = 4.1 volts V_{OUT} = 1.8 volts no-load-100 mA



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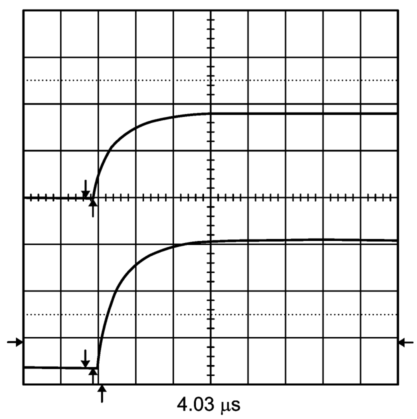
Enable Start-up time (LDO1)
LDO1 channel 2 LDO4 Channel 1 Sys_enable from 0 volts Load = 100mA



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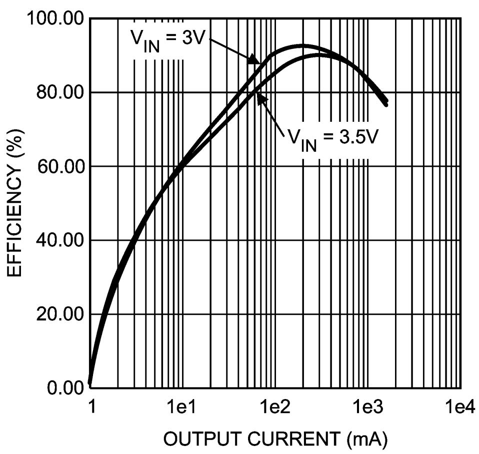
Buck Converters SW1, SW2, SW3

Unless otherwise noted, V_{IN} = 3.6V, C_{IN} = 10 µF, C_{OUT} = 10 µF, L_{OUT} = 2.2 µH ceramic. Typical values and limits appearing in normal type apply for T_J = 25˚C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40˚C to +125˚C. (Notes 2, 6, 12) and (Note 13).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT}	Output Voltage Accuracy	Default V_{OUT}	−3		+3	%
Eff	Efficiency	Load Current = 500 mA		95		%
I_{SHDN}	Shutdown Supply Current	EN is de-asserted		0.1		µA
	Sync Mode Clock Frequency	Synchronized from 13 MHz System Clock	10.4	13	15.6	MHz
f_{OSC}	Internal Oscillator Frequency			2.0		MHz
I_{PEAK}	Peak Switching Current Limit			2.1	2.4	A
I_Q	Quiescent Current “On”	No Load PFM Mode		21		µA
		No Load PWM Mode		200		
R_{DSON} (P)	Pin-Pin Resistance PFET			240		mΩ
R_{DSON} (N)	Pin-Pin Resistance NFET			200		mΩ
T_{ON}	Turn On Time	Start up from Shut-down		500		µsec
C_{IN}	Input Capacitor	Capacitance for Stability	8			µF
C_O	Output Capacitor	Capacitance for Stability	8			µF

Buck 1 Output Efficiency vs. Load Current Varied from 1mA to 1.5 Amps

V_{IN} = 3, 3.5 volts V_{OUT} = 1.4 volts Forced PWM



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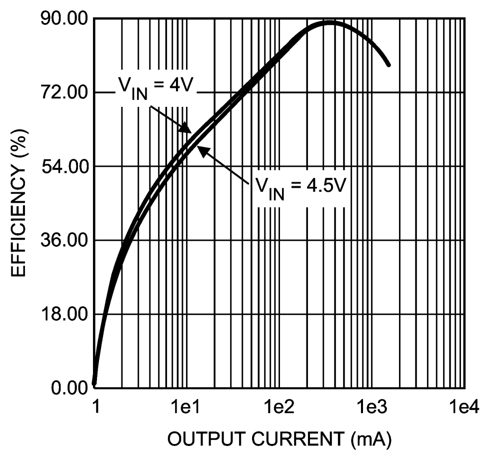
V_{IN} = 4.0-4.5 volts V_{OUT} = 1.4 volts Forced PWM



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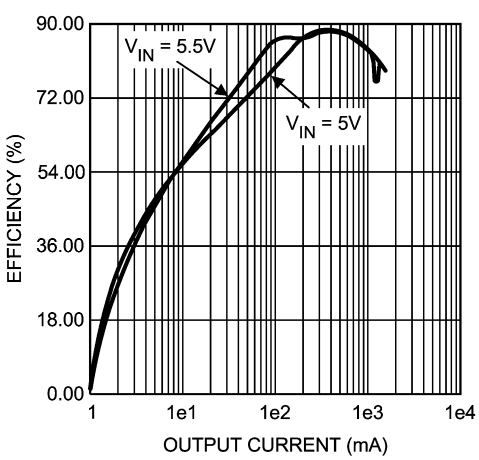
V_{IN} = 3, 3.5 volts V_{OUT} = 1.4 volts Forced PWM



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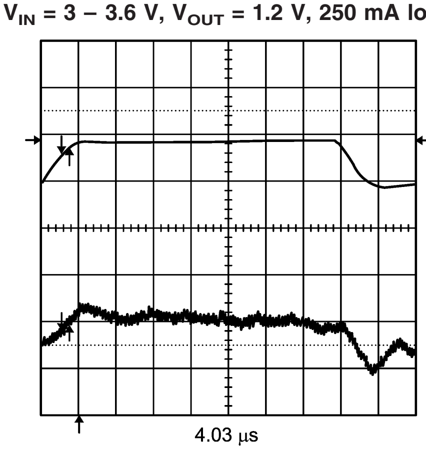
Line Transient Response
V_{IN} = 3 – 3.6 V, V_{OUT} = 1.2 V, 250 mA load



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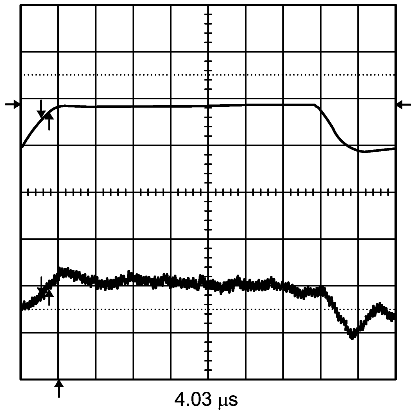
Buck Converters SW1, SW2, SW3 (Continued)

Load Transient
3.6 V_{IN}, 3.3 V_{OUT}, 0 – 100 mA load



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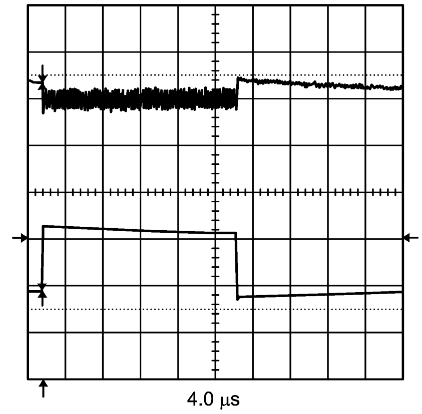
Mode Change
Load transients 20 mA to 560 mA
V_{OUT} = 1.4 volts [PFM to PWM] V_{IN} = 4.1 volts



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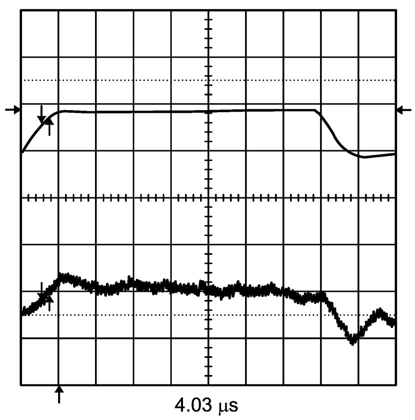
Startup
Startup into PWM Mode 980 mA [channel 2]
V_{OUT} = 1.4 volts V_{IN} = 4.1 volts



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Back-Up Charger Electrical Characteristics

Unless otherwise noted, $V_{IN} = V_{BATT} = 3.6V$. Typical values and limits appearing in normal type apply for $T_J = 25˚C$. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40˚C to +125˚C. (Notes 2, 6) and (Note 8).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Operational Voltage Range	Voltage at V_{IN}	**3.3**		**5.5**	V
I_{OUT}	Backup Battery Charging Current	V_{IN} = 3.6V, Backup_Bat = 2.5V, Backup Battery Charger Enabled (Note 8)		190		µA
V_{OUT}	Charger Termination Voltage	V_{IN} = 5.0V Backup Battery Charger Enabled. Programmable	**2.91**	3.1		V
	Backup Battery Charger Short Circuit Current	Backup_Bat = 0V, Backup Battery Charger Enabled		9		mA
PSRR	Power Supply Ripple Rejection Ratio	$I_{OUT} \leq 50$ µA, $V_{OUT} = 3.15V$ $V_{OUT} + 0.4 \leq V_{BATT} = V_{IN} \leq 5.0V$ f < 10 kHz		15		dB
I_Q	Quiescent Current	I_{OUT} < 50 µA		25		µA
C_{OUT}	Output Capacitance	0 µA ≤ I_{OUT} ≤ 100 µA		0.1		µF
	Output Capacitor ESR		**5**		**500**	mΩ

LP3972 BATTERY SWITCH OPERATION

The LP3972 has provisions for two battery connections, the main battery Vbat and Backup Battery

The function of the battery switch is to connect power to the RTC LDO from the appropriate battery, depending on conditions described below:

- If only the backup battery is applied, the switch will automatically connect the RTC LDO power to this battery.
- If only the main battery is applied, the switch will automatically connect the RTC LDO power to this battery
- If both batteries are applied, and the main battery is sufficiently charged (Vbat > 3.1V), the switch will automatically connect the RTC LDO power to the main battery.
- As the main battery is discharged a separate circuit called nBATT_FLT will warn the system. Then if no action is taken to restore the charge on the main battery, and discharging is continued the battery switch will disconnect the input of the RTC_LDO from the main battery and connect to the backup battery.
- The main battery voltage at which the RTC LDO is switched over from main to backup battery is 2.8V typically.
- There is a hysteric voltage in this switch operation so; the RTC LDO will not be reconnected to main battery until main battery voltage is greater than 3.1V typically.
- The system designer may wish to disable the battery switch when only a main battery is used. This is accomplished by setting the “no back up battery bit” in the control register 8h’0B bit 7 NBUB. With this bit set to “1”, the above described switching will not occur, that is the RTC LDO will remain connected to the main battery even as it is discharged below the 2.9V threshold. The Backup battery input should also be connected to main battery.

Logic Inputs and Outputs DC Operating Conditions (Note 2)

Logic Inputs (SYS_EN, PWR_EN, SYNC, nRSTI, PWR_ON, nTEST_JIG, SPARE and GPI's)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IL}	Low Level Input Voltage			**0.5**	V
V_{IH}	High Level Input Voltage		**V_{RTC} –0.5V**		V
I_{LEAK}	Input Leakage Current		**–1**	**+1**	µA

Logic Outputs (nRSTO, EXT_WAKEUP and GPO's)

Symbol	Parameter	Conditions	Min	Max	Units
V_{OL}	Output Low Level	Load = +0.2 mA = I_{OL} Max		**0.5**	V
V_{OH}	Output High Level	Load = –0.1 mA = I_{OL} Max	**V_{RTC} –0.5V**		V
I_{LEAK}	Output Leakage Current	V_{ON} = V_{IN}		**+5**	µA

Logic Output (nBATT_FLT)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	nBATT_FLT Threshold Voltage	Programmable via Serial Interface Default = 2.8V	**2.4**	2.8	**3.4**	V
V_{OL}	Output Low Level	Load = +0.4 mA = I_{OL} Max			**0.5**	V
V_{OH}	Output High Level	Load = –0.2 mA = I_{OH} Max	**V_{RTC} –0.5V**			V
I_{LEAK}	Input Leakage Current				**+5**	µA

I²C Compatible Serial Interface Electrical Specifications (SDA and SCL)

Unless otherwise noted, V_{IN} = 3.6V. Typical values and limits appearing in normal type apply for T_J = 25˚C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40˚C to +125˚C. (Notes 2, 6) and (Note 9)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage	(Note 14)	−0.5		0.3 V_{RTC}	V
V_{IH}	High Level Input Voltage	(Note 14)	0.7 V_{RTC}		V_{RTC}	
V_{OL}	Low Level Output Voltage	(Note 14)	0		0.2 V_{TRC}	
I_{OL}	Low Level Output Current	V_{OL} = 0.4V (Note 14)	3.0			mA
F_{CLK}	Clock Frequency	(Note 14)			400	kHz
t_{BF}	Bus-Free Time Between Start and Stop	(Note 14)	1.3			µs
t_{HOLD}	Hold Time Repeated Start Condition	(Note 14)	0.6			µs
t_{CLKLP}	CLK Low Period	(Note 14)	1.3			µs
t_{CLKHP}	CLK High Period	(Note 14)	0.6			µs
t_{SU}	Set Up Time Repeated Start Condition	(Note 14)	0.6			µs
$t_{DATAHLD}$	Data Hold Time	(Note 14)	0			µs
t_{CLKSU}	Data Set Up Time	(Note 14)	100			ns
T_{SU}	Set Up Time for Start Condition	(Note 14)	0.6			µs
T_{TRANS}	Maximum Pulse Width of Spikes that Must be Suppressed by the Input Filter of Both DATA & CLK Signals	(Note 14)		50		ns

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (TA-MAX) is dependent on the maximum operating junction temperature (TJ-MAX-OP = 125˚C), the maximum power dissipation of the device in the application (PD-MAX), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: TA-MAX = TJ-MAX-OP − (θ_{JA} x PD-MAX).

Note 4: Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51−7. The test board is a 4-layer FR-4 board measuring 102 mm x 76 mm x 1.6 mm with a 2x1 array of thermal vias. The ground plane on the board is 50 mm x 50 mm. Thickness of copper layers are 36 µm/1.8 µm/18 µm/36 µm (1.5 oz/1 oz/1 oz/1.5 oz). Ambient temperature in simulation is 22˚C, still air. Power dissipation is 1W. Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. The value of θ_{JA} of this product can vary significantly, depending on PCB material, layout, and environmental conditions. In applications where high maximum power dissipation exists (high V_{IN}, high I_{OUT}), special care must be paid to thermal dissipation issues. For more information on these topics, please refer to *Application Note 1187: Leadless Leadframe Package (LLP) and the Power Efficiency and Power Dissipation* section of this datasheet.

Note 5: The Human body model is a 100 pF capacitor discharged through a 1.5 k ??? resistor into each pin. (MIL-STD-883 3015.7) The machine model is a 200 pF capacitor discharged directly into each pin. (EAIJ)

Note 6: All limits guaranteed at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are production tested, guaranteed through statistical analysis or guaranteed by design. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Note 7: Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.

Note 8: Back-up battery charge current is programmable via the I²C compatible interface. Refer to the Application Section for more information.

Note 9: The I²C signals behave like open-drain outputs and require an external pull-up resistor on the system module in the 2 kΩ to 20 kΩ range.

Note 10: LDO_RTC voltage can track LDO3 voltage. LP3972 has a tracking function (nIO_TRACK). When enabled, LDO_RTC voltage will track LDO3 voltage within 200mV down to 2.8V when LDO3 is enabled

Note 11: V_{IN} minimum for line regulation values is 2.7V for LDOs 1–3 and 1.8V for LDOs 4 and 5. Condition does not apply to input voltages below the minimum input operating voltage.

Note 12: The input voltage range recommended for ideal applications performance for the specified output voltages is given below:

V_{IN} = 2.7V to 5.5V for 0.80V $< V_{OUT} <$ 1.8V

V_{IN} = (V_{OUT}+ 1V) to 5.5V for 1.8V $\leq V_{OUT} \leq$ 3.3V

Note 13: Test condition: for V_{OUT} less than 2.7V, V_{IN} = 3.6V; for V_{OUT} greater than or equal to 2.7V, V_{IN} = V_{OUT}+ 1V.

Note 14: This electrical specification is guaranteed by design.

Note 15: An increase in the load current results in a slight decrease in the output voltage and vice versa.

Note 16: Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply for input voltages below 2.7V for LDOs 1–3 and 1.8V for LDOs 4 and 5.

Buck Converter Operation

DEVICE INFORMATION

The LP3972 includes three high efficiency step down DC-DC switching buck converters. Using a voltage mode architecture with synchronous rectification, the buck converters have the ability to deliver up to 1600 mA depending on the input voltage, output voltage, ambient temperature and the inductor chosen.

There are three modes of operation depending on the current required - PWM, PFM, and shutdown. The device operates in PWM mode at load currents of approximately 100 mA or higher, having voltage tolerance of ±3% with 95% efficiency or better. Lighter load currents cause the device to automatically switch into PFM for reduced current consumption. Shutdown mode turns off the device, offering the lowest current consumption ($I_{Q,\ SHUTDOWN}$ = 0.01 µA typ).

Additional features include soft-start, under voltage protection, current overload protection, and thermal shutdown protection.

The part uses an internal reference voltage of 0.5V. It is recommended to keep the part in shutdown until the input voltage is 2.7V or higher.

CIRCUIT OPERATION

The buck converter operates as follows. During the first portion of each switching cycle, the control block turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of $(V_{IN}-V_{OUT})/L$, by storing energy in a magnetic field.

During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of $-V_{OUT}/L$.

The output filter stores charge when the inductor current is high, and releases it when inductor current is low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

PWM OPERATION

During PWM operation the converter operates as a voltage mode controller with input voltage feed forward. This allows the converter to achieve good load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced.

While in PWM (Pulse Width Modulation) mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

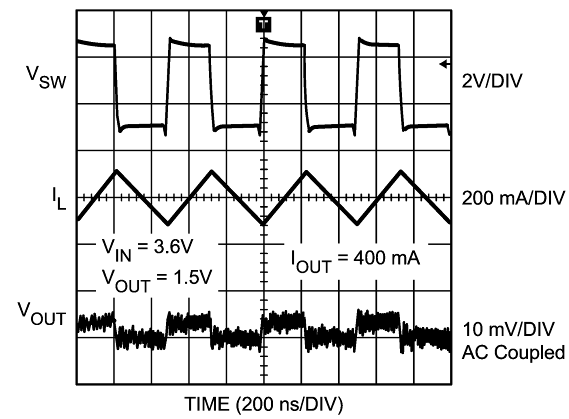


FIGURE 1. Typical PWM Operation

Internal Synchronous Rectification

While in PWM mode, the converters uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

Current Limiting

A current limit feature allows the converters to protect itself and external components during overload conditions. PWM mode implements current limiting using an internal comparator that trips at 2.0 A (typ). If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

PFM OPERATION

At very light loads, the converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency.

The part will automatically transition into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

A: The inductor current becomes discontinuous.

B: The peak PMOS switch current drops below the I_{MODE} level, (Typically I_{MODE} < 30 mA + $V_{IN}/42\Omega$).

Buck Converter Operation (Continued)

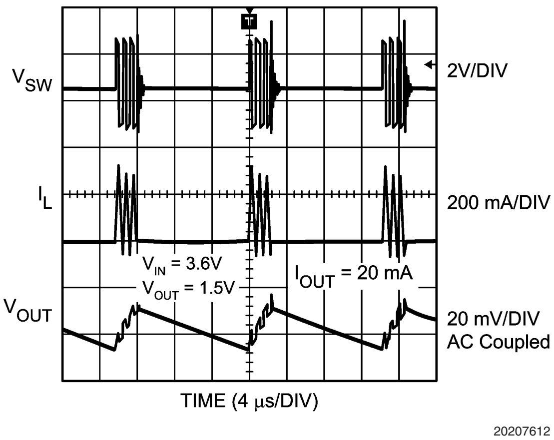


FIGURE 2. Typical PFM Operation

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between <0.6% and <1.7% above the nominal PWM output voltage. If the output voltage is below the "high" PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage reaches the 'high' PFM threshold or the peak current exceeds the IPFM level set for PFM mode. The typical peak current in PFM mode is: IPFM = 112 mA + V_{IN}/27Ω. Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold (see *Figure 3*), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this 'sleep' mode is 21 µA (typ), which allows the part to achieve high efficiencies under extremely light load conditions. When the output drops below the 'low' PFM threshold, the cycle repeats to restore the output voltage (average voltage in PFM mode) to <1.15% above the nominal PWM output voltage. If the load current should increase during PFM mode (see *Figure 3*) causing the output voltage to fall below the 'low2' PFM threshold, the part will automatically transition into fixed-frequency PWM mode. Typically when V_{IN} = 3.6V the part transitions from PWM to PFM mode at 100 mA output current .

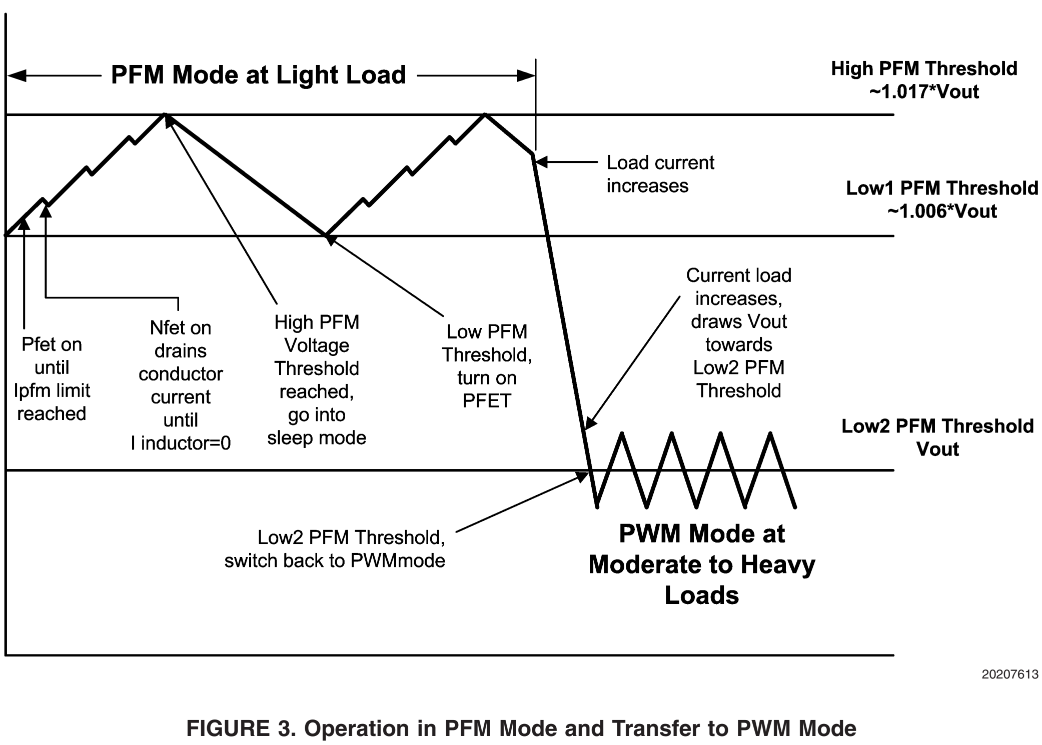


FIGURE 3. Operation in PFM Mode and Transfer to PWM Mode

SHUTDOWN MODE

During shutdown the PFET switch, reference, control and bias circuitry of the converters are turned off. The NFET switch will be open in shutdown to discharge the output. When the converter is enabled, EN, soft start is activated. It is recommended to disable the converter during the system power up and undervoltage conditions when the supply is less than 2.7V.

Buck Converter Operation (Continued)

SOFT START

The buck converter has a soft-start circuit that limits in-rush current during start-up. During start-up the switch current limit is increased in steps. Soft start is activated only if EN goes from logic low to logic high after V_{IN} reaches 2.7V. Soft start is implemented by increasing switch current limit in steps of 213 mA, 425 mA, 850 mA and 1700 mA (typ. Switch current limit). The start-up time thereby depends on the output capacitor and load current demanded at start-up. Typical start-up times with 10 µF output capacitor and 1000 mA load current is 390 µs and with 1 mA load current its 295 µs.

LDO - LOW DROP OUT OPERATION

The LP3672 can operate at 100% duty cycle (no switching; PMOS switch completely on) for low drop out support of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage. When the device operates near 100% duty cycle, output voltage ripple is approximately 25 mV. The minimum input voltage needed to support the output voltage is

$$V_{IN,\ MIN} = I_{LOAD} * (R_{DSON,\ PFET} + R_{INDUCTOR}) + V_{OUT}$$

- I_{LOAD} Load Current
- $R_{DSON,\ PFET}$ Drain to source resistance of PFET switch in the triode region
- $R_{INDUCTOR}$ Inductor resistance

SPREAD SPECTRUM FEATURE

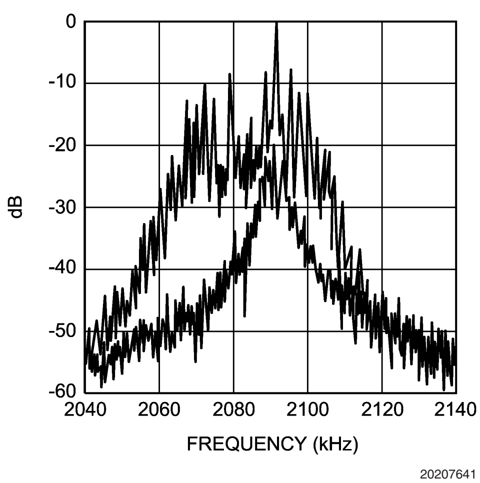
Periodic switching in the buck regulator is inherently a noisier function block compared to an LDO. It can be challenging in some critical applications to comply with stringent regulatory standards or simply to minimize interference to sensitive circuits in space limited portable systems. The regulator's switching frequency and harmonics can cause "noise" in the signal spectrum. The magnitude of this noise is measured by its power spectral density. The power spectral density of the switching frequency, F_C, is one parameter that system designers want to be as low as practical to reduce interference to the environment and subsystems within their products. The LP3972 has a user selectable function on chip, wherein a noise reduction technique known as "spread spectrum" can be employed to ease customer's design and production issues.

The principle behind spread spectrum is to modulate the switching frequency slightly and slowly, and spread the signal frequency over a broader bandwidth. Thus, its power spectral density becomes attenuated, and the associated interference electro-magnetic energy is reduced. The clock used to modulate the LP3972 buck regulator can be used as a spread spectrum clock via 2 I^2C control register (System Control Register 1 (SCR1) 8h'80) bits bk_ssen, and slomod. With this feature enabled, the intense energy of the clock frequency can be spread across a small band of frequencies in the neighborhood of the center frequency. The results in a reduction of the peak energy!

The LP3972 spread spectrum clock uses a triangular modulation profile with equal rise and fall slopes. The modulation has the following characteristics:

- The center frequency: F_C = 2 MHz, and
- The modulating frequency, f_M = 6.8 kHz or 12 kHz.
- Peak frequency deviation: Δ_f = ±100 kHz (or ±5%)
- Modulation index $\beta = \Delta\_f/f_M$ = 14.7 or 8.3

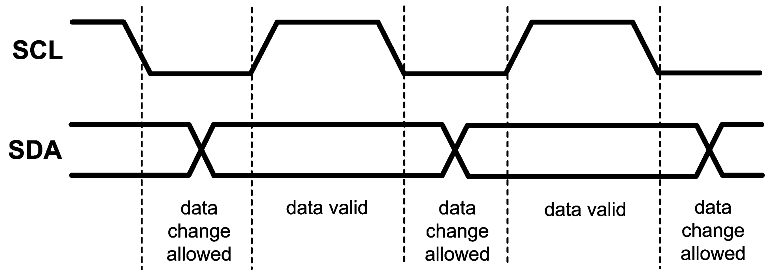
Switching Energy RBW = 300 Hz



I²C Compatible Interface

I²C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.



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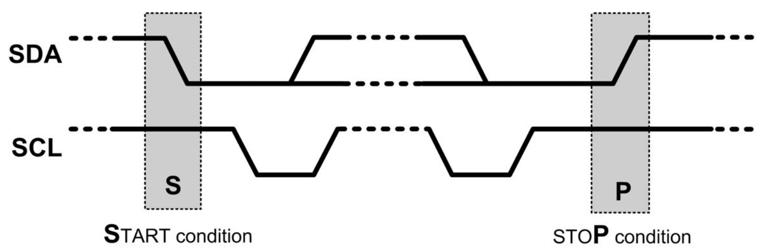
I²C START and STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.



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TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. The number of bytes that can be transmitted per transfer is unrestricted. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

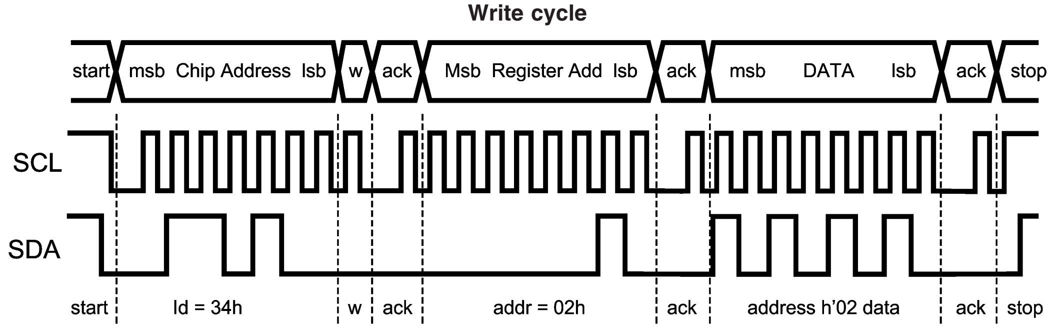
After the START condition, a chip address is sent by the I²C master. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LP3972 address is 34h. For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

I²C CHIP ADDRESS - 7h’34

MSB							
ADR6 Bit7	ADR5 Bit6	ADR4 Bit5	ADR3 Bit4	ADR2 Bit3	ADR1 Bit2	ADR0 Bit1	**R/W** Bit0
0	1	1	0	1	0	0	**R/W**

I²C Compatible Interface (Continued)

Write Cycle



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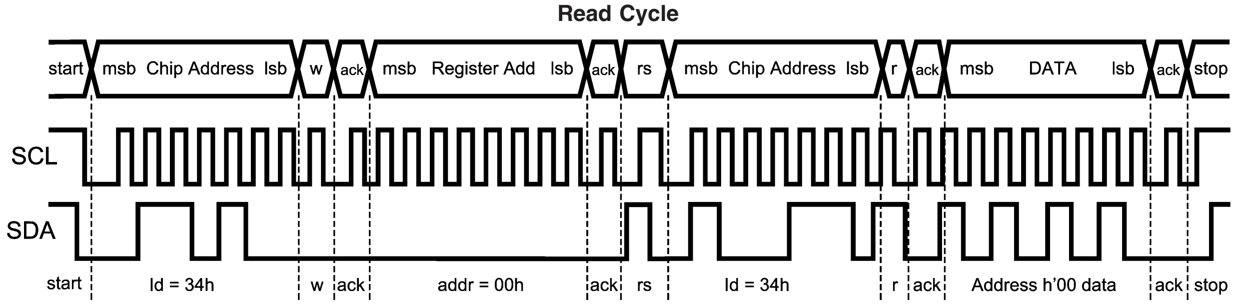
Read Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function as follows.



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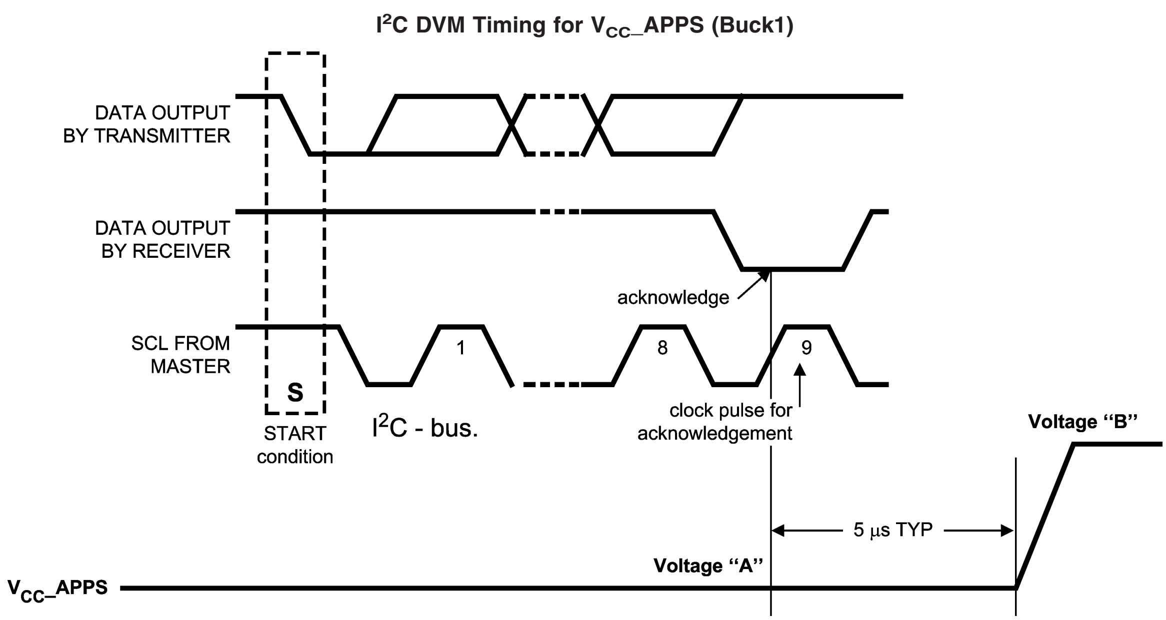
w = write (SDA = "0")

r = read (SDA = "1")

ack = acknowledge (SDA pulled down by either master or slave)

rs = repeated start

id = 34h (Chip Address)



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I^2C Compatible Interface (Continued)

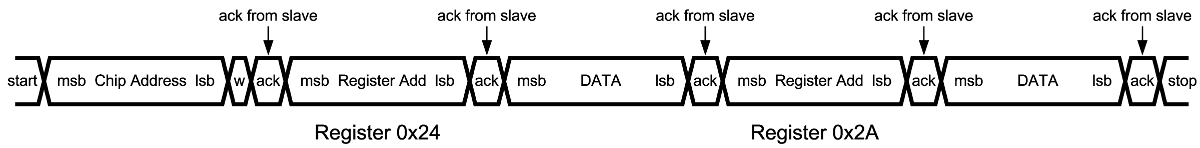
MULTI-BYTE I^2C COMMAND SEQUENCE

To correctly function with the Monahan's Power Management I^2C the LP3972's I^2C serial interface shall support Random register Multi-byte command sequencing: During a multi-byte write the Master sends the Start command followed by the Device address, which is sent only once, followed by the 8 Bit register address, then 8-bits of data. The I^2C slave must then accept the next random register address followed by 8 bits of data and continue this process until the master sends a valid stop condition.

A Typical Multi-byte random register transfer is outlined below:

Device Address, Register A Address, Ach, Register A Data, Ach Register M Address, Ach, Register M Data, Ach Register X Address, Ach, Register X Data, Ach Register Z Address, Ach, Register Z Data, Ach, Stop

Note: the PMIC is not required to see the I^2C device address for each transaction. A, M, X, and Z are Random numbers.



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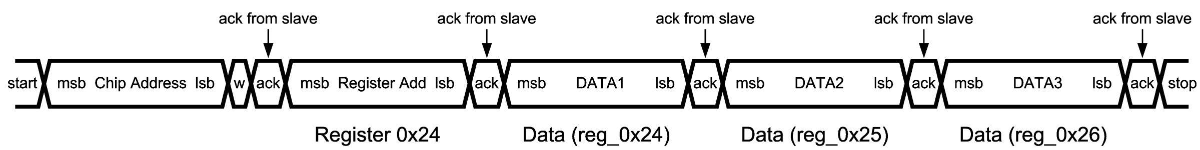
INCREMENTAL REGISTER I^2C COMMAND SEQUENCE

The LP3972 supports address increment (burst mode). When you have defined register address n data bytes can be sent and register address is incremented after each data byte has been sent. Address incrimination may be required for non XScale applications. User can define whether multi-byte (default) to random address or address incrimination will be used.



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I²C Compatible Interface (Continued)

LP3972 CONTROL REGISTER

Register Address	Register Name	Read/Write	Register Description
8h'07	SCR	R/W	System Control Register
8h'10	OVER1	R/W	Output Voltage Enable Register 1
8h'11	OVSR1	R	Output Voltage Status Register 1
8h'12	OVER2	R/W	Output Voltage Enable Register 2
8h'13	OVSR2	R	Output Voltage Status Register 2
8h'20	V_{CC}1	R/W	Voltage Change Control Register 1
8h'23	ADTV1	R/W	BUCK1 Target Voltage 1 Register
8h'24	ADTV2	R/W	BUCK1 DVM Target Voltage 2 Register
8h'25	AVRC	R/W	V_{CC}_APPS Voltage Ramp Control
8h'26	CDTC1	W	Dummy Register
8h'27	CDTC2	W	Dummy Register
8h'29	SDTV1	R/W	LDO5 Target Voltage 1
8h'2A	SDTV2	R/W	LDO5 Target Voltage 2
8h'32	MDTV1	R/W	LDO1 Target Voltage 1 Register
8h'33	MDTV2	R/W	LDO1 Voltage 2 Register
8h'39	L2VCR	R/W	LDO2 Voltage Control Registers
8h'3A	L34VCR	R/W	LDO3 & LDO4 Voltage Control Registers
8h'80	SCR1	R/W	System Control Register 1
8h'81	SCR2	R/W	System Control Register 2
8h'82	OEN3	R/W	Output Voltage Enable Register 3
8h'83	OSR3	R/W	Output Voltage Status Register 3
8h'84	LOER4	R/W	Output Voltage Enable Register 3
8h'85	B2TV	R/W	V_{CC}_Buck2 Target Voltage
8h'86	B3TV	R/W	V_{CC}_Buck3 Target Voltage
8h'87	B32RC	R/W	Buck 32 Voltage Ramp Control
8h'88	ISRA	R	Interrupt Status Register A
8h'89	BCCR	R/W	Backup Battery Charger Control Register
8h'8E	II1RR	R	Internal 1 Revision Register
8h'8F	II2RR	R	Internal 2 Revision Register

SERIAL INTERFACE REGISTER SELECTION CODES (Bold face voltages are default values)

System Control Status Register

Register is an 8 bit register which specifies the control bits for the PMIC clocks. This register works in conjunction with the SYNC pin where an external clock PLL buffer operating at 13 MHz is synchronized with the oscillators of the buck converters.

System Control Register (SCR) 8h'07

Bit	7	6	5	4	3	2	1	0
Designation	Reserved							CLK_SCL
Reset Value	0	0	0	0	0	0	0	0

System Control Register (SCR) 8h'07 Definitions

Bit	Access	Name	Description
7-1	—	—	Reserved
0	R/W	CLK_SCL	External Clock Select 0 = Internal Oscillator clock for Buck Converters 1 = External 13 MHz Oscillator clock for Buck Converters

I²C Compatible Interface (Continued)

OUTPUT VOLTAGE ENABLE REGISTER 1

This register enables or disables the low voltage supplies LDO1 and Buck1. See details below.

Output Voltage Enable Register 1 (OVER1) 8h'10

Bit	7	6	5	4	3	2	1	0
Designation	Reserved					S_EN	Reserved	A_EN
Reset Value	0	0	0	0	0	1	0	1

Output Voltage Enable Register 1 (OVER1) 8h'10 Definitions

Bit	Access	Name	Description
7-3	—	—	Reserved
2	R/W	S_EN	V_{CC}_SRAM (LDO5) Supply Output Enabled 0 = V_{CC}_SRAM (LDO5) Supply Output Disabled 1 = V_{CC}_SRAM (LDO5) Supply Output Enabled
1	—	—	Reserved
0	R/W	A_EN	V_{CC}_APPS (Buck1) Supply Output Enabled 0 = V_{CC}_APPS (BUCK1) Supply Output Disabled 1 = V_{CC}_APPS (BUCK1) Supply Output Enabled

OUTPUT VOLTAGE STATUS REGISTER

This 8 bit register is used to indicate the status of the low voltage supplies. By polling each of the specify supplies is within its specified operating range.

Output Voltage Status Register 1 (OVSR1) 8h'11

Bit	7	6	5	4	3	2	1	0
Designation	LP_OK	Reserved				S_OK	Reserved	A_OK
Reset Value	0	0	0	0	0	0	0	0

Output Voltage Status Register 1 (OVSR1) 8h'11 Definitions

Bit	Access	Name	Description
7	R	LP_OK	Low Voltage Supply Output Voltage Status 0 - V_{CC}_APPS (Buck1) & V_{CC}_SRAM (LDO5) output voltage < 90% of selected value 1 - V_{CC}_APPS (Buck1) & V_{CC}_SRAM (LDO5) output voltage > 90% of selected value
6:3	—	—	Reserved
2	R	S_OK	V_{CC}_SRAM Supply Output Voltage Status 0 - V_{CC}_SRAM (LDO5) output voltage < 90% of selected value 1 - V_{CC}_SRAM (LDO5) output voltage > 90% of selected value
1	—	—	Reserved
0	R	A_OK	V_{CC}_APPS Supply output Voltage Status 0 - V_{CC}_APPS(BUCK1) output voltage < 90% of selected value 1 - V_{CC}_APPS(BUCK1) output voltage > 90% of selected value

I²C Compatible Interface (Continued)

OUTPUT VOLTAGE ENABLE REGISTER 2

This 8 bit output register enables and disables the output voltages on the LDO 2,3,4 supplies.

Output Voltage Enable Register 2 (OVER2) 8h'12

Bit	**7**	**6**	**5**	**4****	**3****	**2****	**1**	**0**
Designation	Reserved			LDO4_EN	LDO3_EN	LDO2_EN	Reserved	
Reset Value	0	0	0	0	0	0	0	0

Note: ** denotes one time factory programmable EPROM registers for default values

Output Voltage Enable Register 2 (OVER2) 8h'12 Definitions

Bit	**Access**	**Name**	**Description**
7	—	—	Reserved
6	—	—	Reserved
5	—	—	Reserved
4	R/W	LDO4_EN	LDO_4 Output Voltage Enable 0 = LDO4 Supply Output Disabled, Default 1 = LDO4 Supply Output Enabled
3	R/W	LDO3_EN	LDO_3 Output Voltage Enable 0 = LDO3 Supply Output Disabled, Default 1 = LDO3 Supply Output Enabled
2	R/W	LDO2_EN	LDO_2 Output Voltage Enable 0 = LDO2 Supply Output Disabled, Default 1 = LDO2 Supply Output Enabled
1	—	—	Reserved
0	—	—	Reserved

OUTPUT VOLTAGE ENABLE REGISTER 2

Output Voltage Status Register 2 (OVSR2) 8h'13

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Designation	LDO_OK	N/A	N/A	LDO4_OK	LDO3_OK	LDO2_OK	N/A	N/A
Reset Value	0	0	0	0	0	0	0	0

Output Voltage Status Register 2 (OVSR2) 8h'13 Definitions

Bit	**Access**	**Name**	**Description**
7	R	LDO_OK	LDO 2-4 Supply Output Voltage Status 0 - (LDO 2-4) output voltage $<$ 90% of selected value 1 - (LDO 2-4) output voltage $>$ 90% of selected value
6	—	—	Reserved
5	—	—	Reserved
4	R	LDO4_OK	LDO_4 Output Voltage Status 0 - (V_{CC}_LDO4) output voltage $<$ 90% of selected value 1 - (V_{CC}_LDO4) output voltage $>$ 90% of selected value
3	R	LDO3_OK	LDO_3 Output Voltage Status 0 - (V_{CC}_LDO3) output voltage $<$ 90% of selected value 1 - (V_{CC}_LDO3) output voltage $>$ 90% of selected value
2	R	LDO2_OK	LDO_2 Output Voltage Status 0 - (V_{CC}_LDO2) output voltage $<$ 90% of selected value 1 - (V_{CC}_LDO2) output voltage $>$ 90% of selected value
1	—	—	Reserved
0	—	—	Reserved

I^2C Compatible Interface (Continued)

DVM VOLTAGE CHANGE CONTROL REGISTER 1

DVM Voltage Change Control Register 1 ($V_{CC}1$) 8h'20

Bit	7	6	5	4	3	2	1	0
Designation	MVS	MGO	SVS	SGO	Reserved		AVS	AGO
Reset Value	0	0	0	0	0	0	0	0

DVM Voltage Change Control Register 1 ($V_{CC}1$) 8h'20 Definitions

Bit	Access	Name	Description
7	R/W	MVS	V_{CC}_MVT (LDO1) Voltage Select 0 - Change V_{CC}_MVT Output Voltage to MDVT1 1 - Change V_{CC}_MVT Output Voltage to MDVT2
6	R/W	MGO	Start V_{CC}_MVT (LDO1) Voltage Change 0 - Hold V_{CC}_MVT Output Voltage at current Level 1 - Ramp V_{CC}_MVT Output Voltage as selected by MVS
5	R/W	SVS	V_{CC}_SRAM (LDO5) Voltage Select 0 - Change V_{CC}_SRAM Output Voltage to SDTV1 1 - Change V_{CC}_SRAM Output Voltage to SDTV2
4	R/W	SGO	Start V_{CC}_SRAM (LDO5) Voltage Change 0 - Hold V_{CC}_SRAM Output Voltage at current Level 1 - Change V_{CC}_SRAM Output Voltage as selected by SVS
3:2	—	—	Reserved
1	R/W	AVS	V_{CC}_APPS (Buck 1) Voltage Select 0 - Ramp V_{CC}_APPS Output Voltage to ADVT1 1 - Ramp V_{CC}_APPS Output Voltage to ADVT2
0	R/W	AGO	Start V_{CC}_APPS(Buck1) Voltage Change 0 - Hold V_{CC}_APPS Output Voltage at current Level 1 - Ramp V_{CC}_APPS Output Voltage as selected by AVS

I^2C Compatible Interface (Continued)

BUCK1 (V_{CC}_APPS) VOLTAGE 1

Buck1 (V_{CC}_APPS) Target Voltage 1 Register (ADTV1) 8h'23

Bit	7	6	5	4**	3**	2**	1**	0**
Designation	Reserved			Buck 1 Output Voltage (B1OV1)				
Reset Value	0	0	0	0	1	0	1	1

Note: ** denotes one time factory programmable

Buck1 (V_{CC}_APPS) Target Voltage 1 Register (ADTV1) 8h'23 Definitions

Bit	Access	Name	Description			
7:5	—	—	Reserved			
4:0	R/W	B1OV1	**Data Code**	**Output Voltage**	**Data Code**	**Output Voltage**
			5h'0	0.725	5h'10	1.125
			5h'1	0.750	5h'11	1.150
			5h'2	0.775	5h'12	1.175
			5h'3	0.800	5h'13	1.200
			5h'4	0.825	5h'14	1.225
			5h'5	0.850	5h'15	1.250
			5h'6	0.875	5h'16	1.275
			5h'7	0.900	5h'17	1.300
			5h'8	0.925	5h'18	1.325
			5h'9	0.950	5h'19	1.350
			5h'A	0.975	5h'1A	1.375
			5h'B	1.000	**5h'1B**	**1.400**
			5h'C	1.025	5h'1C	1.425
			5h'D	1.050	5h'1D	1.450
			5h'E	1.075	5h'1E	1.475
			5h'F	1.100	5h'1F	1.500

I²C Compatible Interface (Continued)

BUCK1 (V_{CC}_APPS) TARGET VOLTAGE 2 REGISTER

Buck1 (V_{CC}_APPS) Target Voltage 2 Register (ADTV2) 8h'24

Bit	7	6	5	4	3	2	1	0
Designation	Reserved			Buck 1 Output Voltage (B1OV2)				
Reset Value	0	0	0	0	1	0	1	1

Buck1 (V_{CC}_APPS) Target Voltage 2 Register (ADTV2) 8h'24 Definitions

Bit	Access	Name	Description			
7:5	—	—	Reserved			
4:0	R/W	B1OV2	**Data Code**	**Output Voltage**	**Data Code**	**Output Voltage**
			5h'0	0.725	5h'10	1.125
			5h'1	0.750	5h'11	1.150
			5h'2	0.775	5h'12	1.175
			5h'3	0.800	5h'13	1.200
			5h'4	0.825	5h'14	1.225
			5h'5	0.850	5h'15	1.250
			5h'6	0.875	5h'16	1.275
			5h'7	0.900	5h'17	1.300
			5h'8	0.925	5h'18	1.325
			5h'9	0.950	5h'19	1.350
			5h'A	0.975	5h'1A	1.375
			5h'B	1.000	5h'1B	1.400
			5h'C	1.025	5h'1C	1.425
			5h'D	1.050	5h'1D	1.450
			5h'E	1.075	5h'1E	1.475
			5h'F	1.100	5h'1F	1.500

I^2C Compatible Interface (Continued)

BUCK1 (V_{CC}_APPS) VOLTAGE RAMP CONTROL REGISTER

Buck1 (V_{CC}_APPS) Voltage Ramp Control Register (AVRC) 8h'25

Bit	7	6	5	4	3	2	1	0
Designation	Reserved			Ramp Rate (B1RR)				
Reset Value	0	0	0	0	1	0	1	0

Buck 1 (V_{CC}_APPS) Voltage Ramp Control Register (AVRC) 8h'25 Definitions

Bit	Access	Name	Description	
7:5	—	—	Reserved	
4:0	R/W	B1RR	DVM Ramp Speed	
			Data Code	**Ramp Rate (mV/uS)**
			5h'0	Instant
			5h'1	1
			5h'2	2
			5h'3	3
			5h'4	4
			5h'5	5
			5h'6	6
			5h'7	7
			5h'8	8
			5h'9	9
			5h'A	**10**
			4h'B-4h'1F	Reserved

I^2C Compatible Interface (Continued)

V_{CC}_COMM TARGET VOLTAGE 1 DUMMY REGISTER (CDTV1)

V_{CC}_COMM Target Voltage 1 Dummy Register (CDTV1) 8h'26 Write Only

Bit	7	6	5	4	3	2	1	0
Designation	Reserved			Output Voltage				
Reset Value	0	0	0	0	0	0	0	0

Note: CDTV1 must be writable by an I^2C controller. This is a dummy register

V_{CC}_COMM TARGET VOLTAGE 2 DUMMY REGISTER (CDTV2)

V_{CC}_COMM Target Voltage 2 Dummy Register (CDTV2) 8h'27 Write Only

Bit	7	6	5	4	3	2	1	0
Designation	Reserved			Output Voltage				
Reset Value	0	0	0	0	0	0	0	0

Note: CDTV2 must be writable by an I^2C controller. This is a dummy register and can not be read.

This is a variable voltage supply to the internal SRAM of the Application processor.

LDO 5 (V_{CC}_SRAM) TARGET VOLTAGE 1 REGISTER

LDO 5 (V_{CC}_SRAM) Target Voltage 1 Register (SDTV1) 8H'29

Bit	7	6	5	4**	3**	2**	1**	0**
Designation	Reserved			LDO 5 Output Voltage (L5OV)				
Reset Value	0	0	0	0	1	0	1	1

Note: ** denotes one time factory programmable EPROM registers for default values

LDO 5 (V_{CC}_SRAM) Target Voltage 1 Register (SDTV1) 8h'29 Definitions

Bit	Access	Name	Description			
7:5	—	—	Reserved			
4:0	R/W	B1OV	**Data Code**	**Output Voltage**	**Data Code**	**Output Voltage**
			5h'0	—	5h'10	1.125
			5h'1	—	5h'11	1.150
			5h'2	—	5h'12	1.175
			5h'3	—	5h'13	1.200
			5h'4	—	5h'14	1.225
			5h'5	0.850	5h'15	1.250
			5h'6	0.875	5h'16	1.275
			5h'7	0.900	5h'17	1.300
			5h'8	0.925	5h'18	1.325
			5h'9	0.950	5h'19	1.350
			5h'A	0.975	5h'1A	1.375
			5h'B	1.000	**5h'1B**	**1.400**
			5h'C	1.025	5h'1C	1.425
			5h'D	1.050	5h'1D	1.450
			5h'E	1.075	5h'1E	1.475
			5h'F	1.100	5h'1F	1.500

I^2C Compatible Interface (Continued)

LDO 5 (V_{CC}_SRAM) TARGET VOLTAGE 2 REGISTER

LDO 5 (V_{CC}_SRAM) Target Voltage 2 Register (SDTV2) 8h'2A

Bit	7	6	5	4	3	2	1	0
Designation	Reserved			LDO 5 Output Voltage (L5OV)				
Reset Value	0	0	0	0	1	0	1	1

LDO 5 (V_{CC}_SRAM) Target Voltage 2 Register (SDTV2) 8h'2A Definitions

Bit	Access	Name	Description			
7:5	—	—	Reserved			
4:0	R/W	B1OV	**Data Code**	**Output Voltage**	**Data Code**	**Output Voltage**
			5h'0	—	5h'10	1.125
			5h'1	—	5h'11	1.150
			5h'2	—	5h'12	1.175
			5h'3	—	5h'13	1.200
			5h'4	—	5h'14	1.225
			5h'5	0.850	5h'15	1.250
			5h'6	0.875	5h'16	1.275
			5h'7	0.900	5h'17	1.300
			5h'8	0.925	5h'18	1.325
			5h'9	0.950	5h'19	1.350
			5h'A	0.975	5h'1A	1.375
			5h'B	1.000	5h'1B	1.400
			5h'C	1.025	5h'1C	1.425
			5h'D	1.050	5h'1D	1.450
			5h'E	1.075	5h'1E	1.475
			5h'F	1.100	5h'1F	1.500

V_{CC}_MVT is low tolerance regulated power supply for the application processor ring oscillator and logic for communicating to the LP3972. V_{CC}_MVT is enabled when SYS_EN is asserted and disabled when SYS_EN is deasserted.

I^2C Compatible Interface (Continued)

LDO 1 (V_{CC}_MVT) TARGET VOLTAGE 1 REGISTER (MDTV1)

LDO 1 (V_{CC}_MVT) Target Voltage 1 Register (MDTV1) 8h'32

Bit	7	6	5	4**	3**	2**	1**	0**
Designation	Reserved			Output Voltage (OV)				
Reset Value	0	0	0	0	0	1	0	0

Note: ** denotes one time factory programmable EPROM registers for default values

LDO 1 (V_{CC}_MVT) Target Voltage 1 Register (MDTV1) 8h'32 Definitions

Bit	Access	Name	Description		
7:5	—	—	Reserved		
4:0	R/W	L1OV	**Data Code**	**Output Voltage**	Notes:
			5h'0	1.700	
			5h'1	1.725	
			5h'2	1.750	
			5h'3	1.775	
			5h'4	**1.800**	
			5h'5	1.825	
			5h'6	1.850	
			5h'7	1.875	
			5h'8	1.900	
			5h'9	1.925	
			5h'A	1.950	
			5h'B	1.975	
			5h'C	2.000	
			5h'D-5h'F	Reserved	

I^2C Compatible Interface (Continued)

LDO 1 (V_{CC}_MVT) TARGET VOLTAGE 2 REGISTER

LDO 1 (V_{CC}_MVT) Target Voltage 2 Register (MDTV2) 8h'33

Bit	7	6	5	4	3	2	1	0
Designation	Reserved			Output Voltage (OV)				
Reset Value	0	0	0	0	1	0	1	1

LDO 1 (V_{CC}_MVT) Target Voltage 2 Register (MDTV2) 8h'33 Definitions

Bit	Access	Name	Description		
7:5	—	—	Reserved		
4:0	R/W	L1OV	**Data Code**	**Output Voltage**	Notes:
			5h'0	1.700	
			5h'1	1.725	
			5h'2	1.750	
			5h'3	1.775	
			5h'4	**1.800**	
			5h'5	1.825	
			5h'6	1.850	
			5h'7	1.875	
			5h'8	1.900	
			5h'9	1.925	
			5h'A	1.950	
			5h'B	1.975	
			5h'C	2.000	
			5h'D-5h'F	Reserved	

I^2C Compatible Interface (Continued)

LDO2 VOLTAGE CONTROL REGISTER (L12VCR)

LDO2 Voltage Control Register (L12VCR) 8h'39

Bit	7**	6**	5**	4**	3	2	1	0
Designation	LDO 2 Output Voltage (L2OV)				Reserved			
Reset Value	0	0	0	0	0	0	0	0

Note: ** denotes one time factory programmable EPROM registers for default values

LDO2 Voltage Control Register (L12VCR) 8h'39 Definitions

Bit	Access	Name	Description		
7:4	R/W	L2OV	**Data Code**	**Output Voltage**	Notes:
			4h'0	**1.8**	Default
			4h'1	1.9	
			4h'2	2.0	
			4h'3	2.1	
			4h'4	2.2	
			4h'5	2.3	
			4h'6	2.4	
			4h'7	2.5	
			4h'8	2.6	
			4h'9	2.7	
			4h'A	2.8	
			4h'B	2.9	
			4h'C	3.0	
			4h'D	3.1	
			4h'E	3.2	
			4h'F	3.3	
3:0	—	—	Reserved		

I^2C Compatible Interface (Continued)

LDO4 – LDO3 VOLTAGE CONTROL REGISTER (L34VCR)

LDO4 – LDO3 Voltage Control Register (L34VCR) 8h'3A

Bit	7**	6**	5**	4**	3**	2**	1**	0**
Designation	LDO 4 Output Voltage (L4OV)				LDO 3 Output Voltage (L3OV)			
Reset Value	0	0	0	0	0	0	0	0

Note: ** denotes one time factory programmable EPROM registers for default values

LDO4 – LDO3 Voltage Control Register (L34VCR) 8h'3A Definitions

Bit	Access	Name	Description		
7:4	R/W	L4OV	**Data Code**	**Output Voltage**	Notes:
			4h'0	1.00	
			4h'1	1.05	
			4h'2	1.10	
			4h'3	1.15	
			4h'4	1.20	
			4h'5	1.25	
			4h'6	1.30	
			4h'7	1.35	
			4h'8	1.40	
			4h'9	1.50	
			4h'A	1.80	
			4h'B	1.90	
			4h'C	2.50	
			4h'D	2.80	
			4h'E	**3.00**	Default
			4h'F	3.30	
3:0	R/W	L3OV	**Data Code**	**Output Voltage**	Notes:
			4h'0	1.8	
			4h'1	1.9	
			4h'2	2.0	
			4h'3	2.1	
			4h'4	2.2	
			4h'5	2.3	
			4h'6	2.4	
			4h'7	2.5	
			4h'8	2.6	
			4h'9	2.7	
			4h'A	2.8	
			4h'B	2.9	
			4h'C	**3.0**	Default
			4h'D	3.1	
			4h'E	3.2	
			4h'F	3.3	

I^2C Compatible Interface (Continued)

NSC DEFINED CONTROL AND STATUS REGISTERS

SYSTEM CONTROL REGISTER 1 (SCR1)

System Control Register 1 (SCR1) 8h'80

Bit	7**	6**	5**	4	3	2	1	0
Designation	BPSEN	SENDL		FPWM3	FPWM2	FPWM1	BK_SLOMOD	BK_SSEN
Reset Value	0	1	0	0	0	0	0	0

Note: ** denotes one time factory programmable EPROM registers for default values

System Control Register 1 (SCR1) 8h'80 Definitions

Bit	Access	Name	Description
7	R/W	BPSEN	Bypass System enable safety Lock. Prevents activation of PWR_EN when SYS_EN is low. 0 = PWR_EN "AND" with SYS_EN signal, Default 1 = PWR_EN independent of SYS_EN
6:5	R/W	SENDL	Delay time for High Voltage Power Domains LDO2, LDO3, LDO4, Buck2, and Buck3 after activation of SYS_EN. V_{CC}_LDO1 has no delay. **Data Code** / **Delay mS** / Notes: 2h'0 / 0.0 2h'1 / 0.5 **2h'2** / **1.0** / Default 2h'3 / 1.4
4	R/W	FPWM3	Buck 3 PWM/PFM Mode select 0 - Auto Switch between PFM and PWM operation 1 - PWM Mode Only will not switch to PFM
3	R/W	FPWM2	Buck 2 PWM/PFM Mode select 0 - Auto Switch between PFM and PWM operation 1 - PWM Mode Only will not switch to PFM
2	R/W	FPWM1	Buck 1 PWM/PFM Mode select 0 - Auto Switch between PFM and PWM operation 1 - PWM Mode Only will not switch to PFM
1	R	BK_SLOMOD	Buck Spread Spectrum Modulation Buck 1-3 0 = 10 kHz triangular wave spread spectrum modulation 1 = 2 kHz triangular wave spread spectrum modulation
0	R	BK_SSEN	Spread spectrum function Buck 1-3 0 = SS Output Disabled 1 = SS Output Enabled

I²C Compatible Interface (Continued)

SYSTEM CONTROL REGISTER 2 (SCR2)

System Control Register 2 (SCR2) 8h'81

Bit	7	6	5**	4	3	2	1	0
Designation	BBCS	SHBU	BPTR	WUP3	GPIO2		GPIO1	
Reset Value	1	0	1	1	0	0	1	0

Note: ** denotes one time factory programmable EPROM registers for default values

System Control Register 2 (SCR2) 8h'81 Definitions

Bit	Access	Name	Description
7	R/W	BBCS	Sets GPIO1 as control input for Back Up battery charger 0 - Back Up battery Charger GPIO Disabled 1 - Back Up battery Charger GPIO Pin Enabled
6	R/W	SHBU	Shut down Back up battery to prevent battery drain during shipping 0 = Back up Battery Enabled 1 = Back up battery Disabled
5	R/W	BPTR	Bypass RTC_LDO Output Voltage to LDO 3 Output Voltage Tracking 0 - RTC-LDO 3 Tracking enabled 1 - RTC-LDO 3 Tracking disabled, Default
4	R/W	WUP3	Spare Wakeup control input 0 - Active High 1 - Active Low
3:2	R/W	GPIO2	Configure direction and output sense of GPIO2 Pin **Data Code** **GPIO2** 2h'00 Hi-Z 2h'01 Output Low 2h'02 Input 2h'03 Output high
1:0	R/W	GPIO1	Configure direction and output sense of GPIO1 Pin **Data Code** **GPIO1** 2h'00 Hi-Z 2h'01 Output Low 2h'02 Input 2h'03 Output high

I^2C Compatible Interface (Continued)

OUTPUT ENABLE 3 REGISTER (OEN3) 8H'82

Bit	7	6	5	4**	3	2**	1	0**
Designation	Reserved			B3EN	ENFLAG	B2EN	Reserved	L1EN
Reset Value	0	0	0	1	0	1	0	1

Note: ** denotes one time factory programmable EPROM registers for default values

OUTPUT ENABLE 3 REGISTER (OEN3) 8H'82 DEFINITIONS

Bit	Access	Name	Description
7:5	—	—	Reserved
4	R/W	B3EN	V_{CC}_Buck3 Supply Output Enabled 0 = V_{CC}_Buck3 Supply Output Disabled 1 = V_{CC}_Buck3 Supply Output Enabled, Default
3	R/W	ENFLAG	Enable for Temperature Flags (BCT) 0 = Temperature Flag Disabled 1 = Temperature Flag Enabled
2	R/W	B2EN	V_{CC}_Buck2 Supply Output Enabled 0 = V_{CC}_Buck2 Supply Output Disabled 1 = V_{CC}_Buck2 Supply Output Enabled, Default
1	—	—	Reserved
0	R/W	L1EN	LDO_1 (MVT)Output Voltage Enable 0 = LDO1 Supply Output Disabled 1 = LDO1 Supply Output Enabled, Default

STATUS REGISTER 3 (OSR3) 8H'83

Bit	7	6	5	4	3	2	1	0
Designation	BT_OK	B3_OK	B2_OK	LDO1_OK	Reserved	BCT2	BCT1	BCT0
Reset Value	0	0	0	0	0	0	0	0

STATUS REGISTER 3 (OSR3) DEFINITIONS 8H'83

Bit	Access	Name	Description
7	R	BT_OK	Buck 2-3 Supply Output Voltage Status 0 - (Buck 1-3) output voltage < 90% Default value 1 - (Buck 1-3) output voltage > 90% Default value
6	R	B3_OK	Buck 3 Supply Output Voltage Status 0 - (Buck 3) output voltage < 90% Default value 1 - (Buck 3) output voltage > 90% Default value
5	R	B2_OK	Buck 2 Supply Output Voltage Status 0 - (Buck 2) output voltage < 90% Default value 1 - (Buck 2) output voltage > 90% Default value
4	R	LDO1_OK	LDO_1 Output Voltage Status 0 - (V_{CC}_LDO1) output voltage < 90% of selected value 1 - (V_{CC}_LDO1) output voltage > 90% of selected value
3	—	—	Reserved

I²C Compatible Interface (Continued)

Bit	Access	Name	Description
2:0	R	BCT	Binary coded thermal management flag status register

Data Code	Temperature Ascending ˚C
000	40
001	60
010	80
011	100
100	120
101	140
110	160
111	Reserved

I^2C Compatible Interface (Continued)

LOGIC OUTPUT ENABLE REGISTER (LOER) 8H'84

Bit	7	6*	5*	4*	3*	2*	1*	0*
Designation	Reserved	B3ENC	B2ENC	B1ENC	L5EC	L4EC	L3EC	L2EC
Reset Value	0	1	1	0	0	1	1	1

Note: ** denotes one time factory programmable EPROM registers for default values

LOGIC OUTPUT ENABLE REGISTER (LOER) DEFINITIONS 8H'84

Bit	Access	Name	Description
7	—	—	Reserved
6	R/W	B3ENC	Connects Buck 3 enable to SYS_EN or PWR_EN Logic Control pin 0 - Buck 3 enable connected to PWR_EN 1 - Buck 3 enable connected to SYS_EN, Default
5	R/W	B2ENC	Connects Buck 2 enable to SYS_EN or PWR_EN Logic Control pin 0 - Buck 2 enable connected to PWR_EN 1 - Buck 2 enable connected to SYS_EN, Default
4	R/W	B1ENC	Connects Buck 1 enable to SYS_EN or PWR_EN Logic Control pin 0 - Buck 1 enable connected to PWR_EN, Default 1 - Buck 1 enable connected to SYS_EN
3	R/W	L5EC	Connects LDO5 enable to SYS_EN or PWR_EN Logic Control pin 0 - LDO 5 enable connected to PWR_EN, Default 1 - LDO 5 enable connected to SYS_EN
2	R/W	L4EC	Connects LDO4 enable to SYS_EN or PWR_EN Logic Control pin 0 - LDO 4 enable connected to PWR_EN 1 - LDO 4 enable connected to SYS_EN, Default
1	R/W	L3EC	Connects LDO3 enable to SYS_EN or PWR_EN Logic Control pin 0 - LDO 3 enable connected to PWR_EN 1 - LDO 3 enable connected to SYS_EN, Default
0	R/W	L2EC	Connects LDO2 enable to SYS_EN or PWR_EN Logic Control pin 0 - LDO 2 enable connected to PWR_EN 1 - LDO 2 enable connected to SYS_EN, Default

I^2C Compatible Interface (Continued)

V_{CC}_BUCK 2 TARGET VOLTAGE REGISTER (B2TV) 8H'85

Bit	7	6	5	4**	3**	2**	1**	0**
Designation	Reserved			Buck 2 Output Voltage (B2OV)				
Reset Value	0	0	0	1	1	0	0	1

Note: ** denotes one time factory programmable EPROM registers for default values

V_{CC}_BUCK 2 TARGET VOLTAGE REGISTER (B2TV) 8H'85 DEFINITIONS

Bit	Access	Name	Description			
7:5	—		Reserved			
4:0	R/W	B2OV	Output Voltage			
			Data Code	**(V)**	**Data Code**	**(V)**
			5h'01	0.80	5h'0D	1.40
			5h'02	0.85	5h'0E	1.45
			5h'03	0.90	5h'0F	1.50
			5h'04	0.95	5h'10	1.55
			5h'05	1.00	5h'11	1.60
			5h'06	1.05	5h'12	1.65
			5h'07	1.10	5h'13	1.70
			5h'08	1.15	5h'14	1.80
			5h'09	1.20	5h'15	1.90
			5h'0A	1.25	5h'16	2.50
			5h'0B	1.30	5h'17	2.80
			5h'0C	1.35	5h'18	3.00
					5h'19	**3.30**

BUCK 3 TARGET VOLTAGE REGISTER (B3TV) 8H'86

Bit	7	6	5	4**	3**	2**	1**	0**
Designation	Reserved			Buck 3 Output Voltage (B3OV)				
Reset Value	0	0	0	1	0	1	0	0

Note: ** denotes one time factory programmable EPROM registers for default values

BUCK 3 TARGET VOLTAGE REGISTER (B3TV) 8H'86 DEFINITIONS

Bit	Access	Name	Description				
7:5	—		Reserved				
4:0	R/W	B3OV	Output Voltage				
			Data Code	**(V)**	**Data Code**	**(V)**	
			5h'01	0.80	5h'0D	1.40	
			5h'02	0.85	5h'0E	1.45	
			5h'03	0.90	5h'0F	1.50	
			5h'04	0.95	5h'11	1.60	
			5h'05	1.00	5h'12	1.65	
			5h'06	1.05	5h'13	1.70	
			5h'07	1.10	**5h'14**	**1.80**	Default
			5h'08	1.15	5h'15	1.90	
			5h'09	1.20	5h'16	2.50	
			5h'0A	1.25	5h'17	2.80	
			5h'0B	1.30	5h'18	3.00	
			5h'0C	1.35	5h'19	3.30	

I^2C Compatible Interface (Continued)

V_{CC}_BUCK 3:2 VOLTAGE RAMP CONTROL REGISTER (B32RC)

V_{CC}_Buck 3:2 Voltage Ramp Control Register (B32RC) 8h’87

Bit	7	6	5	4	3	2	1	0
Designation	Ramp Rate (B3RR)				Ramp Rate (B2RR)			
Reset Value	1	0	1	0	1	0	1	0

Buck 3:2 Voltage Ramp Control Register (B3RC) 8h’87 Definitions

Bit	Access	Name	Description	
7:4	R/W	B3RR	**Data Code**	**Ramp Rate mV/µS**
			4h’0	Instant
			4h’1	1
			4h’2	2
			4h’3	3
			4h’4	4
			4h’5	5
			4h’6	6
			4h’7	7
			4h’8	8
			4h’9	9
			4h’A	**10**
3:0	R/W	B2RR	**Data Code**	**Ramp Rate mV/µS**
			4h’0	Instant
			4h’1	1
			4h’2	2
			4h’3	3
			4h’4	4
			4h’5	5
			4h’6	6
			4h’7	7
			4h’8	8
			4h’9	9
			4h’A	**10**

I^2C Compatible Interface (Continued)

INTERRUPT STATUS REGISTER ISRA

This register specifies the status bits for the interrupts generated by the PMIC. Thermal warning of the IC, GPIO1, GPIO2, PWR_ON pin, TEST_JIG factory programmable on signal, and the SPARE pin.

Interrupt Status Register ISRA 8h'88

Bit	7	6	5	4	3	2	1	0
Designation	Reserved	T125	GPI2	GPI1	WU3L	WUPS	WUPT	WUPS
Reset Value	0	0	0	0	0	0	0	0

Interrupt Status Register ISRA 8h'88 Definitions

Bit	Access	Name	Description
7	—	—	Reserved
6	R	T125	Status bit for thermal warning PMIC T>125C 0 = PMIC Temp. < 125˚C 1 = PMIC Temp. > 125˚C
5	R	GPI2	Status bit for the input read in from GPIO 2 when set as Input 0 = GPI2 Logic Low 1 = GPI2 Logic High
4	R	GPI1	Status bit for the input read in from GPIO 1 when set as Input 0 = GPI1 Logic Low 1 = GPI1 Logic High
3	R	WU3L	PWR_ON Pin long pulse Wake Up Status 0 = No wake up event 1 = Long pulse wake up event
2	R	WUPS	PWR_ON Pin Short pulse Wake Up Status 0 = No wake up event 1 = Short pulse wake up event
1	R	WUPT	TEST_JIG Pin Wake Up Status 0 = No wake up event 1 = Wake up event
0	R	WUPS	SPARE Pin Wake Up Status 0 = No wake up event 1 = Wake up event

I^{2}C Compatible Interface (Continued)

BACKUP BATTERY CHARGER CONTROL REGISTER (BCCR)

This register specifies the status of the main battery supply. NBUB bit

Backup Battery Charger Control Register (BCCR) 8h'89

Bit	7**	6	5**	4**	3**	2	1	0
Designation	NBUB	CNBFL	nBFLT			BUCEN	IBUC	
Reset Value	0	0	0	1	0	0	0	1

Note: ** denotes one time factory programmable EPROM registers for default values

Backup Battery Charger Control Register (BCCR) 8h'89 Definitions

Bit	Access	Name	Description			
7	R/W	NBUB	No back-up battery default setting. Logic will not allow switch over to back-up battery. 0 = Back up Battery Enabled, Default 1 = Back up Battery Disabled			
6	R/W	CNBFL	Control for nBATT_FLT output signal 0 = nBATT_FLT Enabled 1 = nBATT_FLT Disabled			
5:3	R/W	BFLT	nBATT_FLT monitors the battery voltage and can be set to the Assert voltages listed below.			
			Data Code	**Asserted**	**De-Asserted**	Note:
			3h'01	2.6	2.8	
			3h'02	**2.8**	**3.0**	Default
			3h'03	3.0	3.2	
			3h'04	3.2	3.4	
			3h'05	3.4	3.6	
2	R/W	BUCEN	Enables backup battery charger 0 = Back up Battery Charger Disabled 1 = Back up Battery Charger Enabled			
1:0	R/W	IBUC	Charger current setting for back-up battery			
			Data Code	**BU Charger I (µA)**		Note:
			2h'00	260		
			2h'01	**190**		Default
			2h'02	325		
			2h'03	390		

I²C Compatible Interface (Continued)

INTEL INTERNAL 1 REVISION REGISTER (II1RR) 8H'8E

Bit	7	6	5	4	3	2	1	0
Designation	II1RR							
Reset Value	0	0	0	0	0	0	0	0

INTEL INTERNAL 1 REVISION REGISTER (II1RR) 8H'8E DEFINITIONS

Bit	Access	Name	Description
7:0	R	II1RR	Intel internal usage register for revision information.

INTEL INTERNAL 2 REVISION REGISTER (II2RR) 8H'8F

Bit	7	6	5	4	3	2	1	0
Designation	II2RR							
Reset Value	0	0	0	0	0	0	0	0

INTEL INTERNAL 2 REVISION REGISTER (II2RR) 8H'8F DEFINITIONS

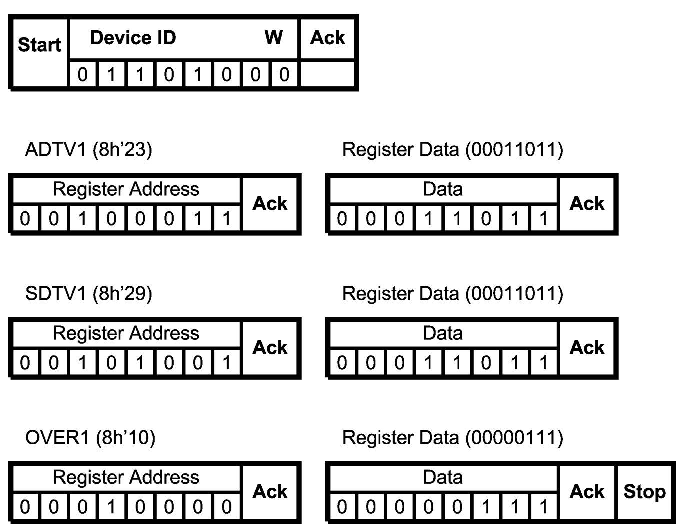
Bit	Access	Name	Description
7:0	R	II2RR	Intel internal usage register for revision information.

REGISTER PROGRAMMING EXAMPLES

Example 1) Start of Day Sequence

PMIC Register Address	PMIC Register Name	Register Data	Description
8h'23	ADTVI	00011011	Sets the SOD V_{CC}_APPS voltage
8h'29	SDTV1	00011011	Sets the SOD V_{CC}_SRAM voltage
8h'10	OVER1	00000111	Enables V_{CC}_SRAM and V_{CC}_APPS to their programmed values.

SODI Multi-byte random register transfer is outlined below:



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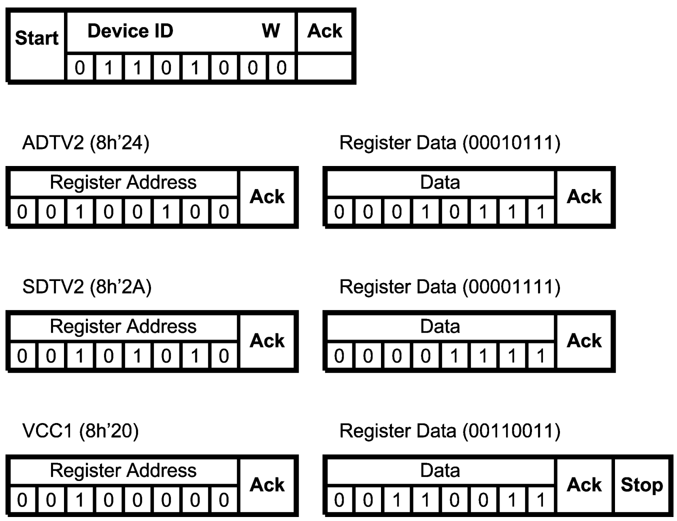
Device Address, Register A Address, Ach, Register A Data, Ach Register M Address, Ach, Register M Data, Ach Register X Address, Ach, Register X Data, Ach Register Z Address, Ach, Register Z Data, Ach, Stop

I²C Compatible Interface (Continued)

Example 2) Voltage change Sequence

PMIC Register Address	PMIC Register Name	Register Data	Description
8h’24	ADTV2	00010111	Sets the V_{CC}_APPS target voltage 2 to 1.3 V
8h’2A	SDTV2	00001111	Sets the V_{CC}_SRAM target voltage 2 to 1.1 V
8h’20	V_{CC}1	00110011	Enable V_{CC}_SRAM and V_{CC}_APPS to change to their programmed target values.

I²C DATA EXCHANGE BETWEEN MASTER AND SLAVE DEVICE



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LP3972 Controls

DIGITAL INTERFACE CONTROL SIGNALS

Signal	Definition	Active State	Signal Direction
SYS_EN	High Voltage Power Enable	High	Input
PWR_EN	Low Voltage Power Enable	High	Input
SCL	Serial Bus Clock Line	Clock	Input
SDA	Serial Bus Data Line		Bidirectional
nRSTI	Forces an unconditional hardware reset	Low	Input
nRSTO	Forces an unconditional hardware reset	Low	Output
nBATT_FLT	Main Battery removed or discharged indicator	Low	Output
PWR_ON	Wakeup Input to CPU	High	Input
nTEST_JIG	Wakeup Input to CPU	Low	Input
SPARE	Wakeup Input to CPU	High	Input
EXT_WAKEUP	Wake-Up Output for application processor	High	Output
GPIO1 / nCHG_EN	General Purpose I/O /External Back-up Battery Charger enable	—	Bidirectional /Input
GPIO2	General Purpose I/O	—	Bidirectional

POWER DOMAIN ENABLES

PMU Output	HW Enable	SW Enable
LDO_RTC	—	—
LDO 1 (V_{CC}_MVT)	SYS_EN	LDO1_EN
LDO2	SYS_EN	LDO2_EN
LDO3	SYS_EN	LDO3_EN
LDO4	SYS_EN	LDO4_EN
LDO5 (V_{CC}_SRAM)	PWR_EN	S_EN
Buck1 (V_{CC}_APPS)	PWR_EN	A_EN
BUCK2	SYS_EN	B2_EN
BUCK3	SYS_EN	B3_EN

POWER DOMAINS SEQUENCING (DELAY)

By default SYS_EN must be on to have PWR_EN enable but this feature can be switched off by register bit BP_SYS.

By default SYS_EN enables LDO1 always first and after a typical of 1 ms delay others. Also when SYS_EN is set off the LDO1 will go off last. This function can be switched off or delay can be changed by DELAY bits via serial interface as seen on table below.

8h'80 Bit 5:4

DELAY bits	'00'	'01'	**'10'**	'11'
Delay, ms	0	0.5	**1.0**	1.5

LDO_RTC TRACKING (nIO_TRACK)

LP3972 has a tracking function (nIO_TRACK). When enabled, LDO_RTC voltage will track LDO3 voltage within 200 mV down to 2.8V when LDO3 is enabled. This function can be switched on/off by nIO_TRACK register bit BPTR.

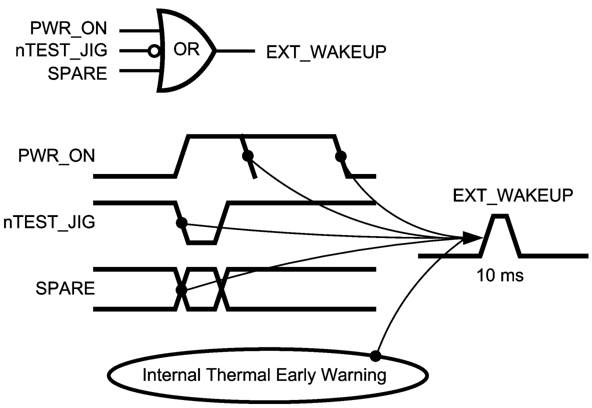
POWER SUPPLY ENABLE

SYS_EN and PWR_EN can be changed by programmable register bits.

LP3972 Controls (Continued)

WAKE-UP FUNCTIONALITY (PWR_ON, nTEST_JIG, SPARE AND EXT_WAKEUP)

Three input pins can be used to assert wakeup output for 10 ms for application processor notification to wakeup. SPARE Input can be programmed through I^{2}C compatible interface to be active low or high (SPARE bit, Default is active low ‘1’). A reason for wakeup event can be read through I^{2}C compatible interface also. Additionally wakeup inputs have 30 ms de-bounce filtering. Furthermore PWR_ON have distinguishing between short and long (~1s) pulses (push button input). LP3972 also has an internal Thermal Shutdown early warning that generates a wakeup to the system also. This is generated usually at 125˚C.



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WAKEUP register bits	Reason for WAKEUP
WUP0	SPARE
WUP1	TEST_JIG
WUP2	PWR_ON short pulse
WUP3	PWR_ON long pulse
TSD_EW	TSD Early Warning

INTERNAL THERMAL SHUTDOWN PROCEDURE

Thermal shutdown is build to generate early warning (typ. 125˚C) which triggers the EXT_WAKEUP for the processor acknowledge. When a thermal shutdown triggers (typ. 160˚C) the PMU will reset the system until the device cools down.

BATTERY SWITCH AND BACK UP BATTERY CHARGER

When Back-Up battery is connected but the main battery has been removed or its supply voltage too low, LP3972 uses Back-Up Battery for generating LDO_RTC voltage. When Main Battery is available the battery fet switches over to the main battery for LDO_RTC voltage. When Main battery voltage is too low or removed nBATT_FLT is asserted. If no back up battery exists, the battery switch to back up can be switched off by nBU_BAT_EN bit. User can set the battery fault determination voltage and battery charger current via I^{2}C compatible interface. Enabling of back up battery charger can be done via serial interface (nBAT_CHG_EN) or external charger enable pin (nCHG_EN). Pin 29 is set as external charger enable input by default.

LP3972 Controls (Continued)

GENERAL PURPOSE I/O FUNCTIONALITY (GPIO1 AND GPIO2)

LP3972 has 2 general purpose I/Os for system control. I^2C compatible interface will be used for setting any of the pins to input, output or hi-Z mode. Inputs value can be read via serial interface (GPI1,2 bits). The pin 29 functionality needs to be set to GPIO by serial interface register bit nEXTCHGEN. (GPIO/CHG)

Controls				Port Function	Reg	batmonchg
GPIO<1>	**GPIO<1>**	**Nextchgen_sel**	**bucen**	**GPIO1**	**Gpin 1**	**Function**
X	X	1	0	Input = 0	0	Enabled
X	X	1	0	Input = 1	0	Not Enabled
1	0	1	X	X	0	
X	X	X	1	X		Enabled
0	0	0	X	HiZ		
1	0	0	X	Input (dig)->	Input	
0	1	0	X	Output = 0	0	
1	1	0	X	Output = 1	0	

GPIO<1>	GPIO<1>	Factory fm disabled	GPIO_tstiob	GPIO2	gpin2
0	0		1	HiZ	0
1	0		1	Input (dig)->	input
0	1		1	Output = 0	0
1	1		1	Output = 1	0

The LP3972 has provision for two battery connections, the main battery Vbat and Backup Battery (See Applications Schematic Diagrams 1 & 2 of the LP3972 Data Sheet).

The function of the battery switch is to connect power to the RTC LDO from the appropriate battery, depending on conditions described below:

- If only the backup battery is applied, the switch will automatically connect the RTC LDO power to this battery.
- If only the main battery is applied, the switch will automatically connect the RTC LDO power to this battery.
- If both batteries are applied, and the main battery is sufficiently charged (V_{BAT} > 3.1V), the switch will automatically connect the RTC LDO power to the main battery.
- As the main battery is discharged by use, the user will be warned by a separate circuit called nBATT_FLT. Then if no action is taken to restore the charge on the main battery, and discharging is continued the battery switch will protect the RTC LDO by disconnecting from the main battery and connecting to the backup battery.
  - — The main battery voltage at which the RTC LDO is switched from main to backup battery is 2.9V typically.
  - — There is a hysterisis voltage in this switch operation so, the RTC LDO will not be reconnected to main battery until main battery voltage is greater than 3.1V typically.
- Additionally, the user may wish to disable the battery switch, such as, in the case when only a main battery is used. This is accomplished by setting the “no back up battery bit” in the control register 8h’0B bit 7 NBUB. With this bit set to “1”, the above described switching will not occur, that is the RTC LDO will remain connected to the main battery even as it is discharged below the 2.9 Volt threshold.

REGULATED VOLTAGES OK

All the power domains have own register bit (X_OK) that processor can read via serial interface to be sure that enabled powers are OK (regulating). Note that these read only bits are only valid when regulators are settled (avoid reading these bits during voltage change or power up).

LP3972 Controls (Continued)

THERMAL MANAGEMENT

Application: There is a mode wherein all 6 comparators (flags) can be turned on via the “enallflags” control register bit. This mode allows the user to interrogate the device or system temperature under the set operating conditions. Thus, the rate of temperature change can also be estimated. The system may then negotiate for speed and power trade off, or deploy cooling maneuvers to optimize system performance. The “enallflags” bit needs enabled only when the “bct<2:0> bits are read to conserve power.

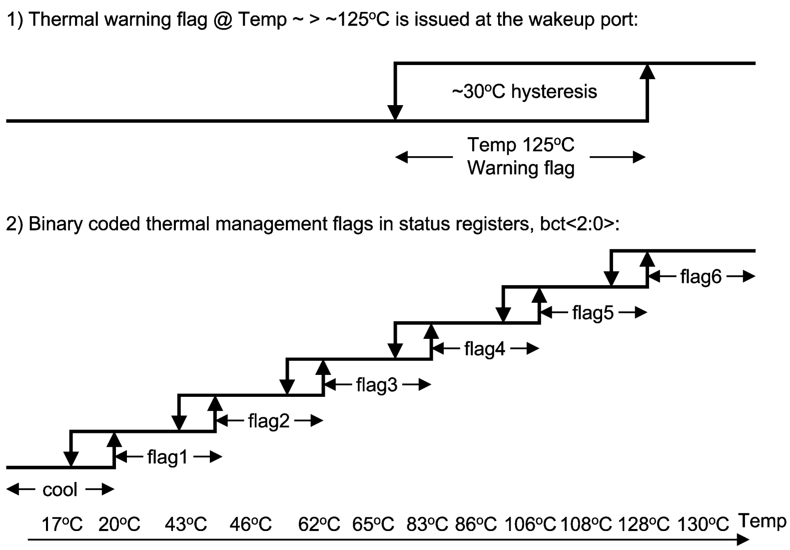
Note: The thermal management flags have been verified functional. Presently these registers are accessible by factory only. If there is a demand for this function, the relevant register controls may be shifted into the user programmable bank; the temperature range and resolution of these flags, might also be refined/redefined.

THERMAL WARNING

2 of 6 low power comparators, each consumes less than 1 µA, are always enabled to operate the “T=125˚C warning flag with hysteresis. This allows continuous monitoring of a thermal-warning flag feature with very low power consumption.

LP3972 THERMAL FLAGS FUNCTIONAL DIAGRAM, DATA FROM INITIAL SILICON

The following functions are extra features from the thermal shutdown circuit:



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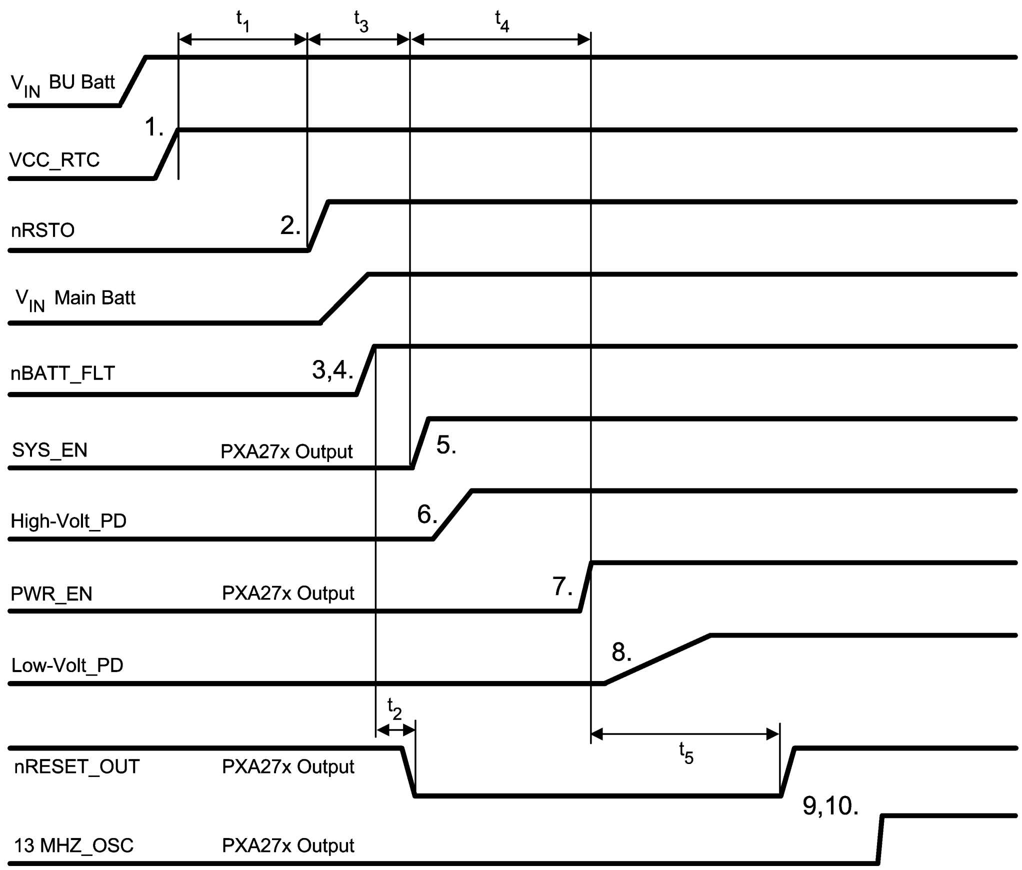
Application Note - LP3972 Reset Sequence

INITIAL COLD START POWER ON SEQUENCE

1. The Back up battery is connected to the PMU, power is applied to the back-up battery pin, the RTC_LDO turns on and supplies a stable output voltage to the V_{CC}_BATT pin of the Applications processor (initiating the power-on reset event) with nRSTO asserted from the LP3972 to the processor.
2. nRSTO de-asserts after a minimum of 50 mS.
3. The Applications processor waits for the de-assertion of nBATT_FLT to indicate system power (V_{IN}) is available.
4. After system power (V_{IN}) is applied, the LP3972 de-asserts nBATT_FLT. Note that BOTH nRSTO and nBATT_FLT need to be de-asserted before SYS_EN is enabled. The sequence of the two signals is independent of each other.
5. The Applications processor asserts SYS_EN, the LP3972 enables the system high-voltage power supplies. The Applications processor starts its countdown timer set to 125 mS.
6. The LP3972 enables the high-voltage power supplies.
   — LDO1 power for V_{CC}_MVT (Power for internal logic and I/O Blocks), BG (Bandgap reference voltage), OSC13M (13 MHz oscillator voltage) and PLL enabled first, followed by others if delay is on.
7. Countdown timer expires; the Applications processor asserts PWR_EN to enable the low-voltage power supplies. The processor starts the countdown timer set to 125 mS period.
8. The Applications processor asserts PWR_EN (ext. pin or I^2C), the LP3972 enables the low-voltage regulators.
9. Countdown timer expires; If enabled power domains are OK (I^2C read) the power up sequence continues by enabling the processors 13 MHz oscillator and PLL's.
10. The Applications processor begins the execution of code.



* Note that BOTH nRSTO and nBATT_FLT need to be de-asserted before SYS_EN is enabled. The sequence of the two signals is independent of each other and can occur is either order.

Application Note - LP3972 Reset Sequence (Continued)

POWER-ON TIMING

Symbol	Description	Min	Typ	Max	Units
t1	Delay from V_{CC}_RTC assertion to nRSTO de-assertion	50			mS
t2	Delay from nBATT_FLT de-assertion to nRSTI assertion		100		µS
t3	Delay from nRST de-assertion to SYS_EN assertion		10		mS
t4	Delay from SYS_EN assertion to PWR_EN assertion		125		mS
t5	Delay from PWR_EN assertion to nRSTO de-assertion		125		mS

HARDWARE RESET SEQUENCE

Hardware reset initiates when the nRSTI signal is asserted (low). Upon assertion of nRST the processor enters hardware reset state. The LP3972 holds the nRST low long enough (50 ms typ.) to allow the processor time to initiate the reset state.

RESET SEQUENCE

1. nRSTI is asserted.
2. nRSTO is asserted and will de-asserts after a minimum of 50 mS
3. The Applications processor waits for the de-assertion of nBATT_FLT to indicate system power (V_{IN}) is available.
4. After system power (V_{IN}) is turned on, the LP3972 de-asserts nBATT_FLT.
5. The Applications processor asserts SYS_EN, the LP3972 enables the system high-voltage power supplies. The Applications processor starts its countdown timer.
6. The LP3972 enables the high-voltage power supplies.
7. Countdown timer expires; the Applications processor asserts PWR_EN to enable the low-voltage power supplies. The processor starts the countdown timer.
8. The Applications processor asserts PWR_EN, the LP3972 enables the low-voltage regulators.
9. Countdown timer expires; If enabled power domains are OK (I^2C read) the power up sequence continues by enabling the processors 13 MHz oscillator and PLL's.
10. The Applications processor begins the execution of code.

Application Hints

LDO CONSIDERATIONS

External Capacitors

The LP3972's regulators require external capacitors for regulator stability. These are specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

Input Capacitor

An input capacitor is required for stability. It is recommended that a 1.0 µF capacitor be connected between the LDO input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain approximately 1.0 µF over the entire operating temperature range.

Output Capacitor

The LDO's are designed specifically to work with very small ceramic output capacitors. A 1.0 µF ceramic capacitor (temperature types Z5U, Y5V or X7R) with ESR between 5 mΩ to 500 mΩ, are suitable in the application circuit.

For this device the output capacitor should be connected between the V_{OUT} pin and ground.

It is also possible to use tantalum or film capacitors at the device output, C_{OUT} (or V_{OUT}), but these are not as attractive for reasons of size and cost (see the section Capacitor Characteristics).

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5 mΩ to 500 mΩ for stability.

No-Load Stability

The LDO's will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

Capacitor Characteristics

The LDO's are designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1.0 µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LDO's.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type. In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, *Figure 4* shows a typical graph comparing different capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, increasing the DC Bias condition can result in the capacitance value falling below the minimum value given in the recommended capacitor specifications table. Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

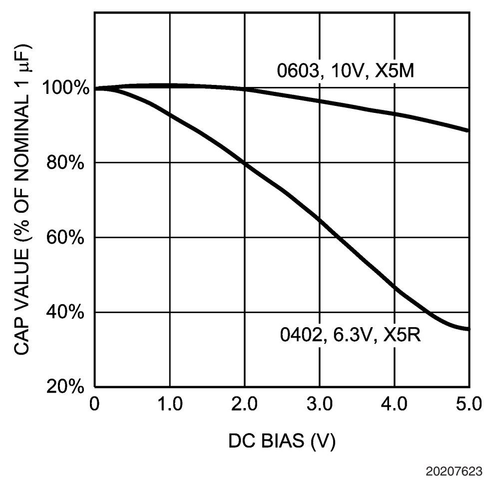


FIGURE 4. Graph Showing a Typical Variation in Capacitance vs. DC Bias

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55˚C to +125˚C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55˚C to +85˚C. Many large value ceramic capacitors, larger than 1 µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25˚C to 85˚C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25˚C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47 µF to 4.7 µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical

Application Hints (Continued)

tantalum will increase about 2:1 as the temperature goes from 25˚C down to –40˚C, so some guard band must be allowed.

BUCK CONSIDERATIONS

Inductor Selection

There are two main considerations when choosing an inductor; the inductor should not saturate, and the inductor current ripple is small enough to achieve the desired output voltage ripple. Different saturation current rating specs are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25˚C so ratings at max ambient temperature of application should be requested from manufacturer.

There are two methods to choose the inductor saturation current rating.

Method 1:

The saturation current is greater than the sum of the maximum load current and the worst case average to peak inductor current. This can be written as

$$I_{SAT} > I_{OUTMAX} + I_{RIPPLE}$$

$$\text{where } I_{RIPPLE} = \left(\frac{V_{IN} - V_{OUT}}{2 * L}\right) * \left(\frac{V_{OUT}}{V_{IN}}\right) * \left(\frac{1}{f}\right)$$

- I_{RIPPLE}: Average to peak inductor current
- I_{OUTMAX}: Maximum load current (1500 mA)
- V_{IN}: Maximum input voltage in application
- L: Min inductor value including worst case tolerances (30% drop can be considered for method 1)
- f: Minimum switching frequency (1.6 MHz)
- V_{OUT}: Output voltage

Method 2:

A more conservative and recommended approach is to choose an inductor that has saturation current rating greater than the max current limit of TBD mA.

A 2.2 µH inductor with a saturation current rating of at least TBD mA is recommended for most applications. The inductor's resistance should be less than 0.3Ω for a good efficiency. *Table 1* lists suggested inductors and suppliers. For low-cost applications, an unshielded bobbin inductor could be considered. For noise critical applications, a toroidal or shielded bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise shielded inductor, in the event that noise from low-cost bobbin models is unacceptable.

Input Capacitor Selection

A ceramic input capacitor of 10 µF, 6.3V is sufficient for most applications. Place the input capacitor as close as possible to the V_{IN} pin of the device. A larger value may be used for improved input voltage filtering. Use X7R or X5R types, do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. The input filter capacitor supplies current to the PFET switch of the converter in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select a capacitor with sufficient ripple current rating. The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}} + \frac{r^2}{12}\right)}$$

$$\text{where } r = \frac{(V_{IN} - V_{OUT}) * V_{OUT}}{L * f * I_{OUTMAX} * V_{IN}}$$

The worst case is when $V_{IN} = 2 * V_{OUT}$

TABLE 1. Suggested Inductors and Their Suppliers

Model	Vendor	Dimensions LxWxH (mm)	D.C.R (Typ)
FDSE0312-2R2M	Toko	3.0 x 3.0 x 1.2	160 mΩ
DO1608C-222	Coilcraft	6.6 x 4.5 x 1.8	80 mΩ

Output Capacitor Selection

Use a 10 µF, 6.3V ceramic capacitor. Use X7R or X5R types, do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer and dc bias curves should be requested from them as part of the capacitor selection process. The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its ESR and can be calculated as:

$$V_{PP\text{-}C} = \frac{I_{RIPPLE}}{4 * f * C}$$

Voltage peak-to-peak ripple due to ESR can be expressed as follows

$$V_{PP\text{-}ESR} = (2 * I_{RIPPLE}) * R_{ESR}$$

Because these two components are out of phase the rms value can be used to get an approximate value of peak-to-peak ripple.

Application Hints (Continued)

Voltage peak-to-peak ripple, root mean squared can be expressed as follows

$$V_{PP\text{-}RMS} = \sqrt{V_{PP\text{-}C}^2 + V_{PP\text{-}ESR}^2}$$

Note that the output voltage ripple is dependent on the inductor current ripple and the equivalent series resistance of the output capacitor (R_{ESR}).

The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for calculations is at the switching frequency of the part.

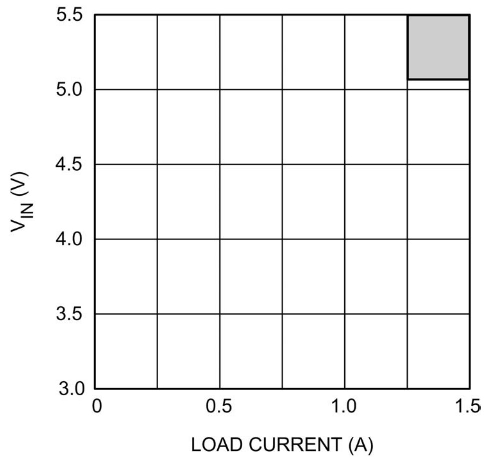
TABLE 2. Suggested Capacitor and Their Suppliers

Model	Type	Vendor	Voltage	Case Size Inch (mm)
GRM21BR60J106K	Ceramic, X5R	Murata	6.3V	0805 (2012)
JMK212BJ106K	Ceramic, X5R	Taiyo-Yuden	6.3V	0805 (2012)
C2012X5R0J106K	Ceramic, X5R	TDK	6.3V	0805 (2012)

Application Hints (Continued)

Buck Output Ripple Management

If V_{IN} and I_{LOAD} increase, the output ripple associated with the Buck Regulators also increases. The figure below shows the safe operating area. To ensure operation in the area of concern it is recommended that the system designer circumvents the output ripple issues to install schottky diodes on the Bucks(s) that are expected to perform under these extreme corner conditions. (Schottky diodes are recommended to reduce the output ripple, if system requirements include this shaded area of operation. V_{IN} > 1.5V and I_{LOAD} > 1.24)



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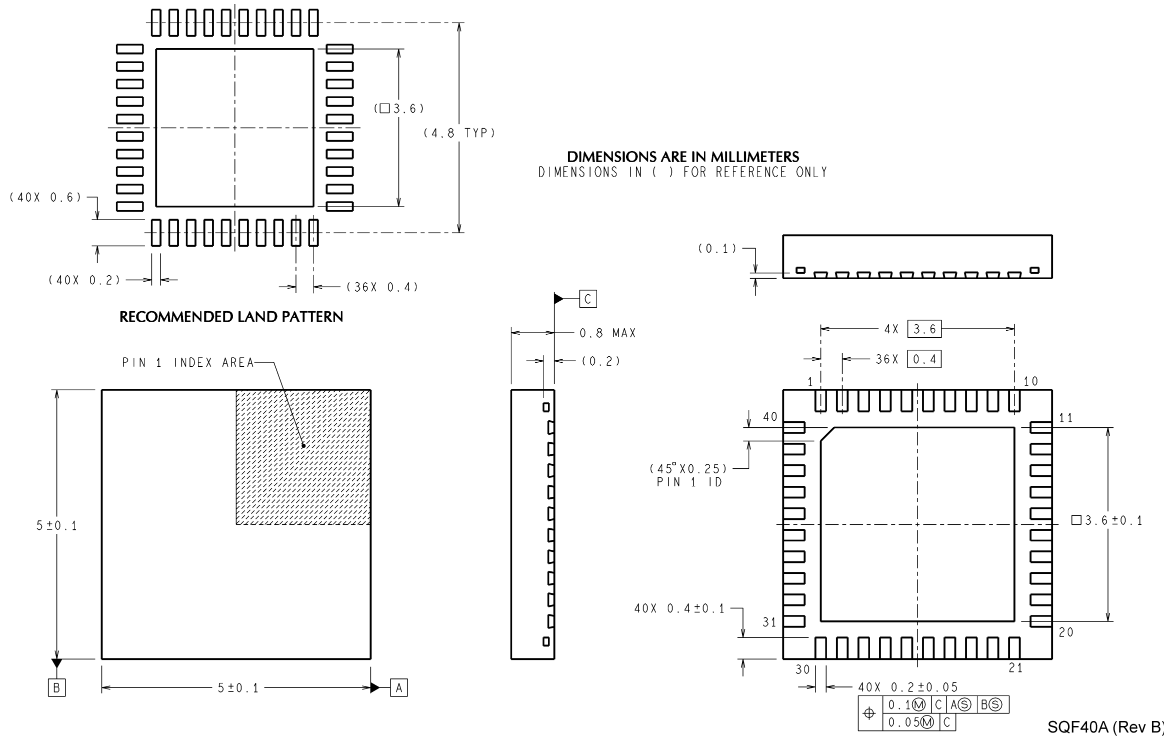
Board Layout Considerations

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability.

Good layout for the converters can be implemented by following a few simple design rules.

1. Place the converters, inductor and filter capacitors close together and make the traces short. The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Special care must be given to place the input filter capacitor very close to the V_{IN} and GND pin.
2. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor through the converter and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground through the converter by the inductor to the output filter capacitor and then back through ground forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
3. Connect the ground pins of the converter and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias. This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the converter by giving it a low-impedance ground connection.
4. Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces.
5. Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components. The voltage feedback trace must remain close to the converter circuit and should be direct but should be routed opposite to noisy components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and layer on which the feedback trace is routed. In the same manner for the adjustable part it is desired to have the feedback dividers on the bottom layer.
6. Place noise sensitive circuitry, such as radio RF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry. Interference with noise-sensitive circuitry in the system can be reduced through distance.

Physical Dimensions inches (millimeters) unless otherwise noted



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