National Semiconductor

PRELIMINARY
June 2004

LP3993
Low I_Q, 80mA Linear Regulator for Digital Applications

General Description

The LP3993 is a linear regulator capable of supplying 80mA output current. The LP3993 is designed to meet the requirements of digital systems where low I_Q, fast start up, and good load transient response are important.

The device has been designed to work with small ceramic capacitors of 1.0µF and above.

This device is available with outputs in the range 1.5V to 3.3V outputs. Please contact your local sales office for availability of particular voltage options.

Features

- Stable with Low-Value Ceramic Input and Output Capacitors
- No Noise Bypass Capacitor Required
- Fast Turn-On
- Logic Controlled Enable
- Thermal-Overload and Short-Circuit Protection
- -40 to +125˚C junction temperature range for operation

Key Specifications

■ Input Voltage Range	2.5 to 6.0V
■ Output Voltage Range	1.5 to 3.3V
■ Output Current	80mA
■ Output Stable - Capacitors	1.0uF
■ Virtually Zero I_Q (Disabled)	<1µA
■ Very Low I_Q (Enabled)	10µA at 1mA I_{OUT}
■ Output Voltage Noise	250µV_{RMS}
■ PSRR	40dB at 1kHz
■ Start Up Time	150µs
■ Low Dropout (where applic.)	160mV typ.
■ Load Transient Response	60mV

Packages

micro SMD (4 Pin)

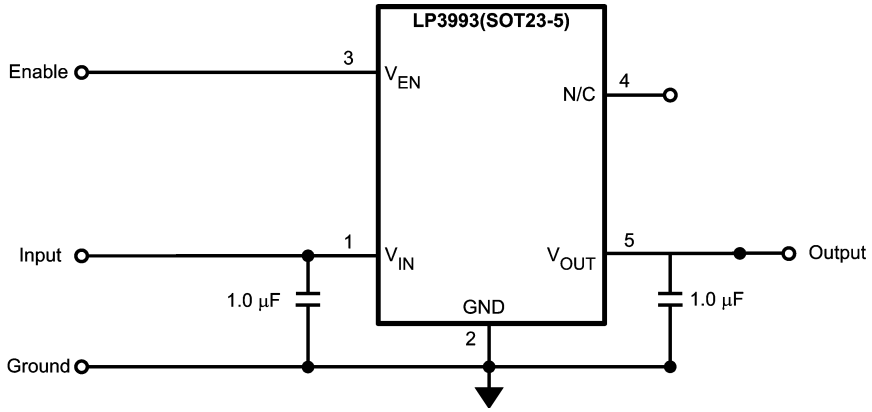
SOT23 - 5

For other package options contact your NSC sales office.

Applications

- Cellular Phones
- PDA Handsets
- Wireless LAN devices

Typical Application Circuit



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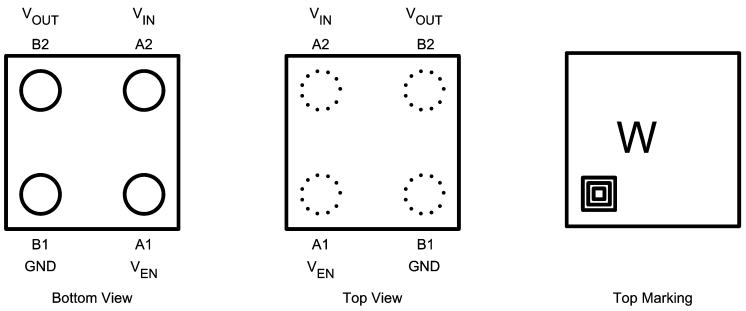
Pin Descriptions

Packages

Pin No		Symbol	Name and Function
SOT23	micro SMD		
1	A2	V_{IN}	Voltage Supply Input, A 1.0µF ceramic capacitor should be connected to this input pin.
2	B1	GND	Common Ground
3	A1	V_{EN}	Enable Input; An internal 400kΩ resistor connects this pin to ground Enables the Regulator when ≥ 1.2V. Disables the Regulator when ≤ 0.4V
4		N/C	No Connection to this pin. Do not connect this pin to any other pin.
5	B2	V_{OUT}	Voltage output. Connect a 1.0µF low ESR capacitor to this Pin. Connect this output to the load circuit.

Connection Diagrams

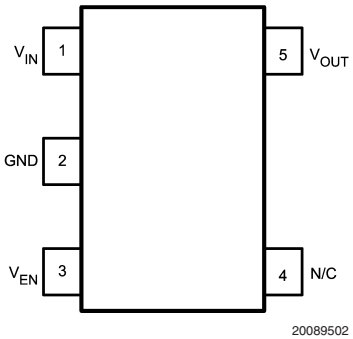
Micro SMD, 4 Bump Package



See NS package number TLA04

Note: The actual physical placement of the package marking will vary from part to part. The package marking "X" designates the date code.

SOT23 - 5 Package (MF)



See NS package number MF05A

Ordering Information

For micro SMD Package

Please contact Sales Office for Availability

Output Voltage (V)	Grade	LP3993 Supplied as 250 Units, Tape and Reel	LP3993 Supplied as 3000 Units, Tape and Reel	Package Marking
1.5	STD	LP3993ITL-1.5	LP3993ITLX-1.5	
1.8	STD	LP3993ITL-1.8	LP3993ITLX-1.8	
2.5	STD	LP3993ITL-2.5	LP3993ITLX-2.5	
2.8	STD	LP3993ITL-2.8	LP3993ITLX-2.8	
2.85	STD	LP3993ITL-2.85	LP3993ITLX-2.85	
3.0	STD	LP3993ITL-3.0	LP3993ITLX-3.0	
3.1	STD	LP3993ITL-3.1	LP3993ITLX-3.1	
3.3	STD	LP3993ITL-3.3	LP3993ITLX-3.3	

For SOT23 - 5 Package

Please contact Sales Office for Availability

Output Voltage (V)	Grade	LP3993 Supplied as 1000 Units, Tape and Reel	LP3993 Supplied as 3000 Units, Tape and Reel	
1.5	STD	LP3993IMF-1.5	LP3993IMFX-1.5	
1.8	STD	LP3993IMF-1.8	LP3993IMFX-1.8	
2.5	STD	LP3993IMF-2.5	LP3993IMFX-2.5	
2.8	STD	LP3993IMF-2.8	LP3993IMFX-2.8	
2.85	STD	LP3993IMF-2.85	LP3993IMFX-2.85	
3.0	STD	LP3993IMF-3.0	LP3993IMFX-3.0	
3.1	STD	LP3993IMF-3.1	LP3993IMFX-3.1	
3.3	STD	LP3993IMF-3.3	LP3993IMFX-3.3	

Absolute Maximum Ratings

(Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN} Pin; Input Voltage	-0.3 to 6.5V
V_{OUT} Pin; Output Voltage	-0.3 to (V_{IN} + 0.3V) to 6.5V (max)
V_{EN} Pin; Enable Input	-0.3 to (V_{IN} + 0.3V) to 6.5V (max)
Junction Temperature	150˚C
Lead/Pad Temp. (Note 3)	
SOT23	260˚C
micro SMD	265˚C
Storage Temperature	-65 to 150˚C
Continuous Power Dissipation	Internally Limited(Note 4)

ESD (Note 5)

Human Body Model	2KV
Machine Model	200V

Operating Ratings(Note 1)

V_{IN}; Input Voltage	2.5V to 6V
V_{EN}; Enable Input Voltage	0 to (V_{IN} + 0.3V) to 6.0V (max)
Recommended Load C urrent	0mA to 80mA
Junction Temperature (T_J)	-40˚C to 125˚C
Ambient Temperature (T_A) Range(Note 6)	-40˚C to 85˚C

Thermal Properties(Note 1)

Junction To Ambient Thermal Resistance θ ($_{JA}$)(Note 7)	
microSMD (MFA05 package)	220˚C/W
SOT23-5 (TLA04 package)	220˚C/W

Electrical Characteristics

Unless otherwise noted, specifications apply to the LP3993 Typical Application Circuit (pg. 1) with: $V_{IN} = V_{OUT} + 0.5V$, V_{EN} =1.2V,C_{IN} = 1 µF, C_{OUT} = 1.0µF, I_{OUT} = 1 mA. Typical values and limits appearing in normal type apply for T_J = 27˚C. Limits appearing in **boldface** type apply over the full temperature range for operation, –40 to +125˚C. (Note 15)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
V_{IN}	Input Voltage			2.5	6	V
ΔV_{OUT}	Output Voltage Tolerance	I_{OUT} = 1mA, V_{OUT} = 1.5V		**-53**	**+53**	mV
		I_{OUT} = 1mA		-3	+3	%
				-3.5	**+3.5**	
	Line Regulation Error	V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) to 6.0V, I_{OUT} = 1mA	0.083		**0.4**	%/V
	Load Regulation Error	I_{OUT} = 1mA to 80mA	0.020		**0.1**	%/mA
V_{DO}	Dropout Voltage	I_{OUT} = 50mA (Note 11)	160		**250**	mV
I_Q	Quiescent Current (Note 12)	V_{EN} = 1.2V, I_{OUT} = 0mA	10		**30**	µA
		V_{EN} = 1.2V, I_{OUT} = 80mA	30		**50**	
		V_{EN} = 0.4V	0.005		**1**	
I_G	Ground Current (Note 13)	I_{OUT} = 0mA	13			µA
I_{SC}	Short Circuit Current Limit	(Note 10)	400		**650**	mA
I_{OUT}	Maximum Output Current			**80**		mA
PSRR	Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 1mA	40			dB
		f = 10kHz, I_{OUT} = 1mA	30			
E_N	Output noise Voltage (Note 14)	BW = 10Hz to 100kHz, V_{IN} = 4.2V	250			μV_{RMS}
$T_{SHUTDOWN}$	Thermal Shutdown	Temperature	160			˚C
		Hysteresis	20			
Enable Control Characteristics						
I_{EN}	Input Current at V_{EN} Input	V_{EN} = 6.0V, V_{IN} = 6.0V (Note 14)	15			µA
V_{IL}	Low Input Threshold	V_{IN} = 2V to 6V			**0.4**	V
V_{IH}	High Input Threshold	V_{IN} = 2V to 6V		**1.2**		V

Electrical Characteristics (Continued)

Unless otherwise noted, specifications apply to the LP3993 Typical Application Circuit (pg. 1) with: $V_{IN} = V_{OUT} + 0.5V$, V_{EN} =1.2V,C_{IN} = 1 µF, C_{OUT} = 1.0µF, I_{OUT} = 1 mA. Typical values and limits appearing in normal type apply for T_J = 27˚C. Limits appearing in **boldface** type apply over the full temperature range for operation, −40 to +125˚C. (Note 15)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
Timing Characteristics						
T_{ON}	Turn On Time (Note 9)	To 95% Level	150		**300**	µs

Note 1: Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All Voltages are with respect to the potential at the GND pin.

Note 3: For further information on these packages please refer to the following application notes;AN-1112 Micro SMD Package Wafer Level Chip Scale Package,AN-1187 Leadless Leadframe Package.

Note 4: Internal thermal shutdown circuitry protects the device from permanent damage.

Note 5: The human body model is 100pF discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Note 6: The maximum ambient temperature ($T_{A(max)}$) is dependant on the maximum operating junction temperature ($T_{J(max-op)}$ = 125˚C), the maximum power dissipation of the device in te application ($P_{D(max)}$), and the junction to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max-op)} - (\theta_{JA} \times P_{D(max)})$.

Note 7: Junction to ambient thermal resistance is dependant on the application and board layout. In applications where high maximum power dissipation is possible, special care must be paid to thermal dissipation issues in board design.

Note 8: The device maintains the regulated output voltage without the load.

Note 9: This electrical specification is guaranteed by design.

Note 10: Short circuit current is measured on the input supply line at the point when the short circuit condition reduces the output voltage to 5% of its nominal value.

Note 11: Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100mV below its nominal value. This parameter only applies to output voltages above 2.5V.

Note 12: Quiescent current is defined here as the difference in current between the input pin and the output pin of the device.

Note 13: Ground current is defined here as the total current flowing to ground as a result of all inputs applied to the device.

Note 14: The enable Pin has a 400KΩ (typical) resistor connected to GND.

Note 15: All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production at T_J = 25˚C or correlated using Statistical Quality Control methods. Operation over the temperature specification is guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Output Capacitor, Recommended Specifications

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
C_o	Output Capacitor	Capacitance(Note 16)	1.0	**0.7**		µF
		ESR		**5**	**500**	mΩ

Note 16: The minimum capacitance should be greater than 0.7µF over the full range of operating conditions. The Capacitor tolerance should be ±30% over the full temperature range. The full range of operating conditions for the capacitor in the application should be considered during device selection to ensure this minimum capacitance specification is met. X7R capacitor types are recommended to meet the full device temperature range, however X5R, Y5V, and Z5U types may be used with careful consideration of the application and its operating conditions. (See Capacitor Sections in Application Hints.)

Application Hints

POWER DISSIPATION AND DEVICE OPERATION

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air.

As stated in (Note 6) in the electrical specification section, the allowable power dissipation for the device in a given package can be calculated using the equation:

$$P_D = \frac{(T_{J(max)} - T_A)}{\theta_{JA}}$$

With a θ_{JA} = 220˚C/W, the device in the SOT23 package returns a value of 455 mW with a junction temperature of 25˚C.

The actual power dissipation across the device can be represented by the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

This establishes the relationship between the power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

EXTERNAL CAPACITORS

In common with most regulators, the LP3993 requires external capacitors for regulator stability. The LP3993 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitor is required for stability. It is recommended that a 1.0µF capacitor be connected between the LP3993 input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain ≅ 1.0µF over the entire operating temperature range.

OUTPUT CAPACITOR

Correct selection of the output capacitor is critical to ensure stable operation in the intended application.

The output capacitor must meet all the requirements specified in the recommended capacitor table over all conditions in the application. These conditions include DC-bias, frequency and temperature. Unstable operation will result if the capacitance drops below the minimum specified value.

The LP3993 is designed specifically to work with very small ceramic output capacitors. A 1.0µF ceramic capacitor (dielectric type X7R) with ESR between 5mohm to 500mohm, is suitable in the LP3998 application circuit. X5R type capacitors may be used but have a narrower temperature range. With these capacitors and others types (Y5V, Z6U) that may be used, selection of the capacitor for any application is dependant on the range of operating conditions and temperature range for that application. (See section on Capacitor Characteristics).

It is also recommended that the output capacitor be placed within 1cm from the output pin and returned to a clean ground line.

It may also be possible to use tantalum or film capacitors at the device output, C_{OUT} (or V_{OUT}), but these are not as attractive for reasons of size and cost (see the section Capacitor Characteristics).

NO-LOAD STABILITY

The LP3993 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

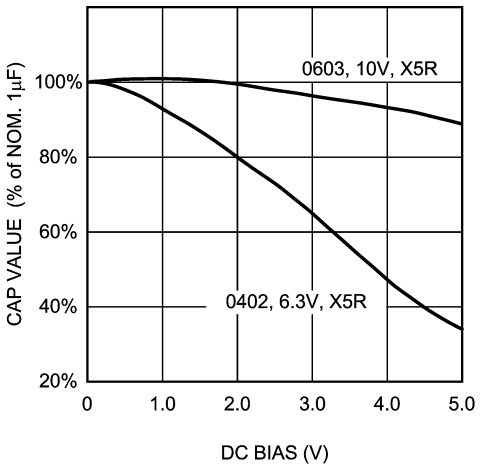
CAPACITOR CHARACTERISTICS

The LP3998 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values around 1µF, ceramic capacitors give the circuit designer the best design options in terms of low cost and minimal area.

For both input and output capacitors careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly dependant on the conditions of operation and capacitor type.

In particular to ensure stability, the output capacitor selection should take account of all the capacitor parameters to ensure that the specification is met within the application. Capacitance value can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size with smaller sizes giving poorer performance figures in general. As an example shows a typical graph showing a comparison of capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, as a result of the DC Bias condition the capacitance value may drop below the minimum capacitance value given in the recommended capacitor table (0.7µF in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

Application Hints (Continued)



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Graph Showing a Typical Variation in Capacitance vs DC Bias

Ceramic capacitors have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1µF ceramic capacitor is in the range of 20mΩ to 40mΩ, which easily meets the ESR requirement for stability for the LP3998.

The temperature performance of ceramic capacitors varies by type. Capacitor type X7R is specified with a tolerance of ±15% over the temperature range -55°C to +125°C. The X5R has a similar tolerance over the reduced temperature range of -55°C to +85°C. Most large value ceramic capacitors (≥2.2µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C. Therefore X7R is recommended over these other capacitor types in applications where the temperature will change significantly above or below 25˚C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1µF to 4.7µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25˚C down to -40˚C, so some guard band must be allowed.

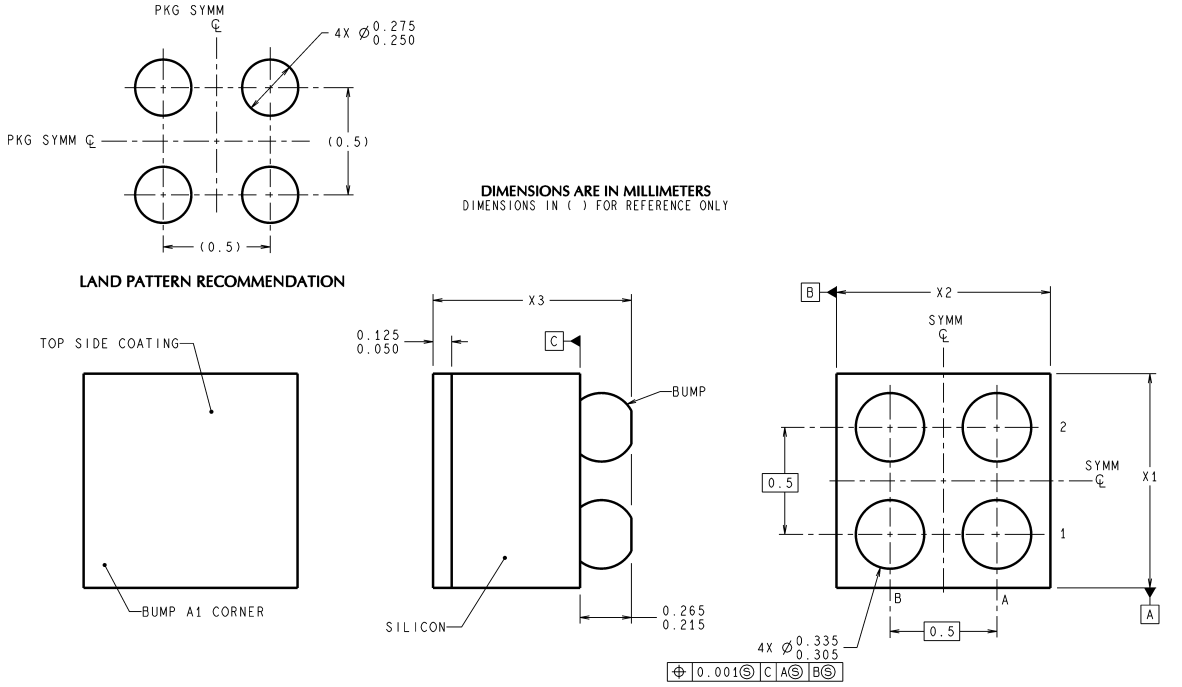
ENABLE CONTROL

The LP3993 features an active high Enable pin, V_{EN}, which turns the device on when pulled high. When not enabled the regulator output is off and the device typically consumes 5nA.

If the application does not require the Enable switching feature, the V_{EN} pin should be tied to V_{IN} to keep the regulator output permanently on.

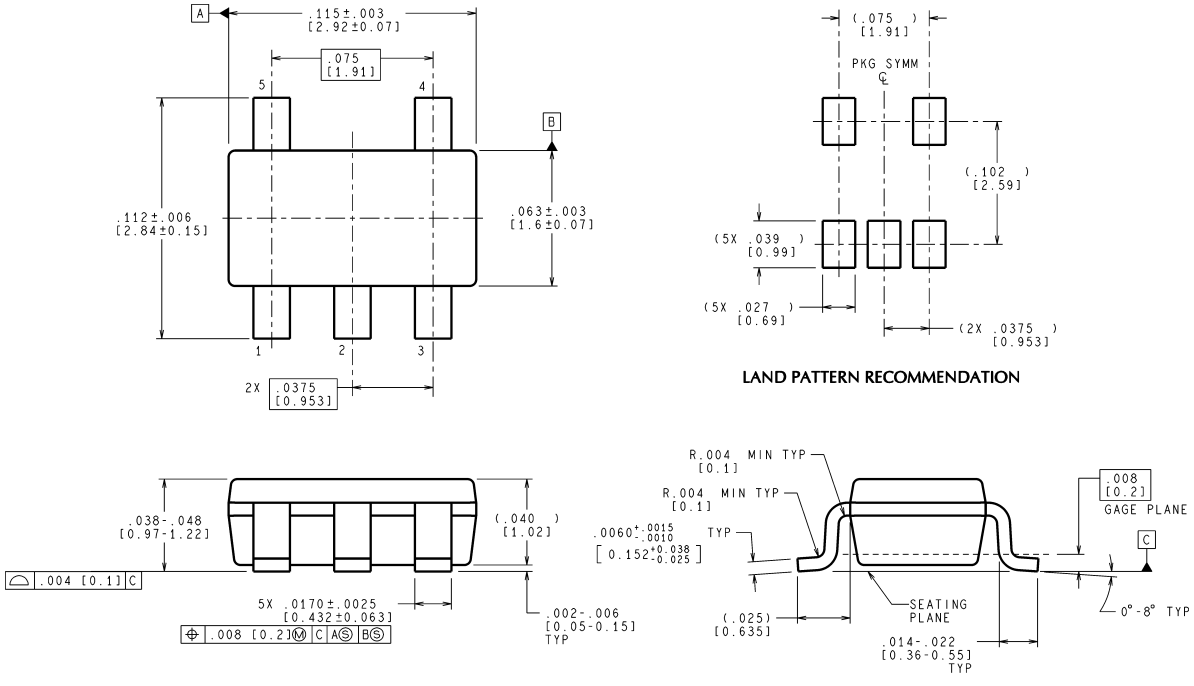
To ensure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

Physical Dimensions inches (millimeters) unless otherwise noted



TLA04XXX (Rev C)

micro SMD, 4 Bump, Package (TLA04)
NS Package Number TLA04xxx
The dimensions for X1, X2 and X3 are given as:
X1 = 1.040 +/– 0.03mm
X2 = 1.065 +/– 0.03mm
X3 = 0.600 +/– 0.075mm



MF05A (Rev B)

SOT23 - 5 Package
NS Package Number MF05A

Notes

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