National Semiconductor

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TP3064, TP3067
"Enhanced" Serial Interface CMOS CODEC/Filter COMBO®

General Description

The TP3064 (μ-law) and TP3067 (A-law) are monolithic PCM CODEC/Filters utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (microCMOS).

Similar to the TP305X family, these devices feature an additional Receive Power Amplifier to provide push-pull balanced output drive capability. The receive gain can be adjusted by means of two external resistors for an output level of up to ±6.6V across a balanced 600Ω load.

Also included is an Analog Loopback switch and a $\overline{TS_X}$ output.

See also AN-370, "Techniques for Designing with CODEC/Filter COMBO Circuits."

Features

- Complete CODEC and filtering system including:
  - — Transmit high-pass and low-pass filtering
  - — Receive low-pass filter with sin x/x correction
  - — Active RC noise filters
  - — μ-law or A-law compatible COder and DECoder
  - — Internal precision voltage reference
  - — Serial I/O interface
  - — Internal auto-zero circuitry
  - — Receive push-pull power amplifiers
- μ-law—TP3064
- A-law—TP3067
- Designed for D3/D4 and CCITT applications
- ±5V operation
- Low operating power—typically 70 mW
- Power-down standby mode—typically 3 mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density

Block Diagram

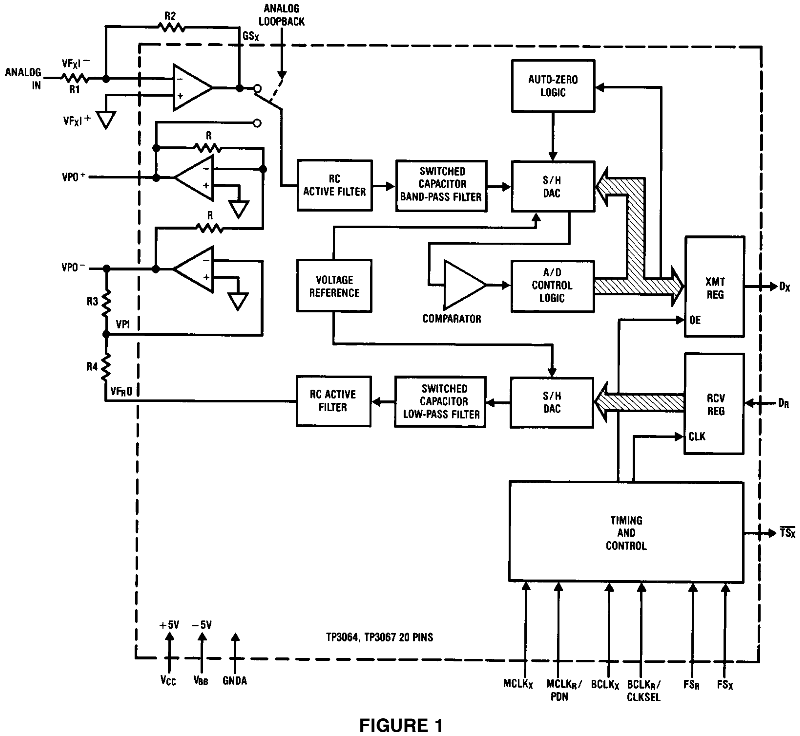

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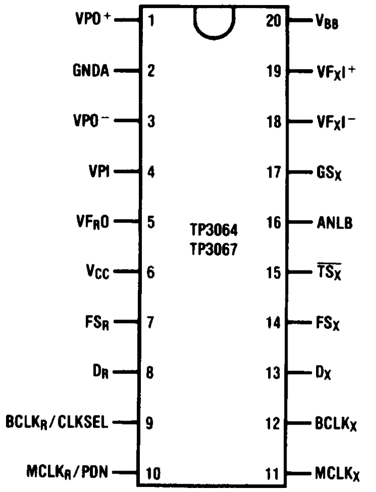
FIGURE 1

Connection Diagrams

Dual-In-Line Package



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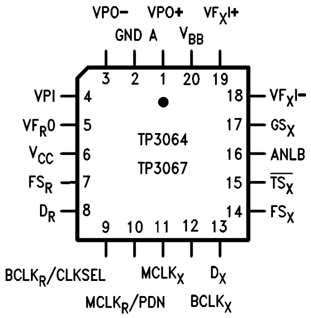
Top View

Plastic Chip Carrier



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Top View

Order Number TP3064J or TP3067J
See NS Package J20A

Order Number TP3064WM or TP3067WM
See NS Package M20B

Order Number TP3064N or TP3067N
See NS Package N20A

Order Number TP3064V or TP3067V
See NS Package V20A

Pin Description

Symbol	Function
VPO+	The non-inverted output of the receive power amplifier.
GNDA	Analog ground. All signals are referenced to this pin.
VPO−	The inverted output of the receive power amplifier.
VPI	Inverting input to the receive power amplifier.
VF_RO	Analog output of the receive filter.
V_{CC}	Positive power supply pin. $V_{CC} = +5V \pm 5\%$.
FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See *Figures 2* and *3* for timing details.
D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/ CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see Table I).
$MCLK_R$/ PDN	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
$MCLK_X$	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$. Best performance is realized from synchronous operation.
$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	The TRI-STATE® PCM data output which is enabled by FS_X.
FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train, see *Figures 2* and *3* for timing details.
$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
ANLB	Analog Loopback control input. Must be set to logic '0' for normal operation. When pulled to logic '1', the transmit filter input is disconnected from the output of the transmit preamplifier and connected to the VPO+ output of the receive power amplifier.
GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
VF_XI^-	Inverting input of the transmit input amplifier.
VF_XI^+	Non-inverting input of the transmit input amplifier.
V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$.

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO™ and places it into a power-down state. All non-essential circuits are deactivated and the D$_X$, VF$_R$O, VPO$^-$ and VPO$^+$ outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the MCLK$_R$/PDN pin *and* FS$_X$ and/or FS$_R$ pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the MCLK$_R$/PDN pin high; the alternative is to hold both FS$_X$ and FS$_R$ inputs continuously low—the device will power-down approximately 2 ms after the last FS$_X$ or FS$_R$ pulse. Power-up will occur on the first FS$_X$ or FS$_R$ pulse. The TRI-STATE PCM data output, D$_X$, will remain in the high impedance state until the second FS$_X$ pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to MCLK$_X$ and the MCLK$_R$/PDN pin can be used as a power-down control. A low level on MCLK$_R$/PDN powers up the device and a high level powers down the device. In either case, MCLK$_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to BCLK$_X$ and the BCLK$_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the BCLK$_R$/CLKSEL pin, BLCK$_X$ will be selected as the bit clock for both the transmit and receive directions. Table I indicates the frequencies of operation which can be selected, depending on the state of BCLK$_R$/CLKSEL. In this synchronous mode, the bit clock, BCLK$_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with MCLK$_X$.

Each FS$_X$ pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D$_X$ output on the positive edge of BCLK$_X$. After 8 bit clock periods, the TRI-STATE D$_X$ output is returned to a high impedance state. With an FS$_R$ pulse, PCM data is latched via the D$_R$ input on the negative edge of BCLK$_X$ (or BCLK$_R$ if running). FS$_X$ and FS$_R$ must be synchronous with MCLK$_{X/R}$.

TABLE I. Selection of Master Clock Frequencies

BCLK$_R$/CLKSEL	Master Clock Frequency Selected	
	TP3067	**TP3064**
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1	2.048 MHz	1.536 MHz or 1.544 MHz

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. MCLK$_X$ and MCLK$_R$ must be 2.048 MHz for the TP3067, or 1.536 MHZ, 1.544 MHz for the TP3064, and need not be synchronous. For best transmission performance, however, MCLK$_R$ should be synchronous with MCLK$_X$, which is easily achieved by applying only static logic levels to the MCLK$_R$/PDN pin. This will automatically connect MCLK$_X$ to all internal MCLK$_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS$_X$ starts each encoding cycle and must be synchronous with MCLK$_X$ and BCLK$_X$. FS$_R$ starts each decoding cycle and must be synchronous with BCLK$_R$. BCLK$_R$ must be a clock, the logic levels shown in Table I are not valid in asynchronous mode. BCLK$_X$ and BCLK$_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse (the same as the TP3020/21 CODECs) or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS$_X$ and FS$_R$, must be one bit clock period long, with timing relationships specified in *Figure 2*. With FS$_X$ high during a falling edge of BCLK$_X$, the next rising edge of BCLK$_X$ enables the D$_X$ TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D$_X$ output. With FS$_R$ high during a falling edge of BCLK$_R$ (BCLK$_X$ in synchronous mode), the next falling edge of BCLK$_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. All devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long (TP5116A/56 CODECs) frame mode, both the frame sync pulses, FS$_X$ and FS$_R$, must be three or more bit clock periods long, with timing relationships specified in *Figure 3*. Based on the transmit frame sync, FS$_X$, the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The D$_X$ TRI-STATE output buffer is enabled with the rising edge of FS$_X$ or the rising edge of BCLK$_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven BCLK$_X$ rising edges clock out the remaining seven bits. The D$_X$ output is disabled by the falling BCLK$_X$ edge following the eighth rising edge, or by FS$_X$ going low, whichever comes later. A rising edge on the receive frame sync pulse, FS$_R$, will cause the PCM data at D$_R$ to be latched in on the next eight falling edges of BCLK$_R$(BCLK$_X$ in synchronous mode). All devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 4*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-law (TP3064) or A-law (TP3067) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t$_{MAX}$) of nominally 2.5V peak (see

Functional Description (Continued)

table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (TP3067) or μ-law (TP3064) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter with its output at VF_RO. The receive section is unity-gain, but gain can be added by using the power amplifiers. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 180 μs.

RECEIVE POWER AMPLIFIERS

Two inverting mode power amplifiers are provided for directly driving a matched line interface transformer. The gain of the first power amplifier can be adjusted to boost the ±2.5V peak output signal from the receive filter up to ±3.3V peak into an unbalanced 300Ω load, or ±4.0V into an unbalanced 15 kΩ load. The second power amplifier is internally connected in unity-gain inverting mode to give 6 dB of signal gain for balanced loads.

Maximum power transfer to a 600Ω subscriber line termination is obtained by differentially driving a balanced transformer with a $\sqrt{2}$:1 turns ratio, as shown in *Figure 4*. A total peak power of 15.6 dBm can be delivered to the load plus termination.

ENCODING FORMAT AT D_X OUTPUT

	TP3064 μ-Law								**TP3067 A-Law (Includes Even Bit Inversion)**							
V_{IN} = +Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} = 0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} = −Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GNDA	7V
V_{BB} to GNDA	$-7V$
Voltage at any Analog Input or Output	$V_{CC}+0.3V$ to $V_{BB}-0.3V$
Voltage at any Digital Input or Output	$V_{CC}+0.3V$ to GNDA$-0.3V$
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	300°C
ESD (Human Body Model) J	1000V
ESD (Human Body Model) N	1500V
Latch-Up Immunity	100 mA on Any Pin

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; $T_A = 0°C$ to $70°C$ by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at $V_{CC} = +5.0V$, $V_{BB} = -5.0V$, $T_A = 25°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION (ALL DEVICES)						
$I_{CC}0$	Power-Down Current	(Note)		0.5	**1.5**	mA
$I_{BB}0$	Power-Down Current	(Note)		0.05	**0.3**	mA
$I_{CC}1$	Active Current	VPI=0V; VF_RO, VPO^+ and VPO^- unloaded		7.0	**10.0**	mA
$I_{BB}1$	Active Current	VPI=0V; VF_RO, VPO^+ and VPO^- unloaded		7.0	**10.0**	mA
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	D_X, $I_L=3.2$ mA $\overline{TS}_X$, $I_L=3.2$ mA, Open Drain			**0.4** **0.4**	V V
V_{OH}	Output High Voltage	D_X, $I_H=-3.2$ mA	**2.4**			V
I_{IL}	Input Low Current	GNDA$\leq V_{IN} \leq V_{IL}$, All Digital Inputs	**−10**		**10**	μA
I_{IH}	Input High Current	$V_{IH} \leq V_{IN} \leq V_{CC}$	**−10**		**10**	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	D_X, GNDA$\leq V_O \leq V_{CC}$	**−10**		**10**	μA

Note: I_{CC0} and I_{BB0} are measured after first achieving a power-up state.

Electrical Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at $V_{CC} = +5.0V$, $V_{BB} = -5.0V$, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)						
I_IXA	Input Leakage Current	$-2.5V \leq V \leq +2.5V$, VF_XI^+ or VF_XI^-	**−200**		**200**	nA
R_IXA	Input Resistance	$-2.5V \leq V \leq +2.5V$, VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Dynamic Range	GS_X, $R_L \geq 10$ kΩ	**−2.8**		**+2.8**	V
A_VXA	Voltage Gain	VF_XI^+ to GS_X	**5000**			V/V
F_UXA	Unity-Gain Bandwidth		1	2		MHz
V_{OS}XA	Offset Voltage		**−20**		**20**	mV
V_{CM}XA	Common-Mode Voltage	CMRRXA > 60 dB	**−2.5**		**2.5**	V
CMRRXA	Common-Mode Rejection Ratio	DC Test	**60**			dB
PSRRXA	Power Supply Rejection Ratio	DC Test	**60**			dB
ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)						
R_ORF	Output Resistance	Pin VF_RO		1	3	Ω
R_LRF	Load Resistance	$VF_RO = \pm 2.5V$	10			kΩ
C_LRF	Load Capacitance	Connect from VF_RO to GNDA			25	pF
VOS_RO	Output DC Offset Voltage	Measure from VF_RO to GNDA	**−200**		**200**	mV
ANALOG INTERFACE WITH POWER AMPLIFIERS (ALL DEVICES)						
IPI	Input Leakage Current	$-1.0V \leq VPI \leq 1.0V$	**−100**		**100**	nA
RIPI	Input Resistance	$-1.0V \leq VPI \leq 1.0V$	10			MΩ
VIOS	Input Offset Voltage		**−25**		**25**	mV
ROP	Output Resistance	Inverting Unity-Gain at VPO^+ or VPO^-		1		Ω
F_C	Unity-Gain Bandwidth	Open Loop (VPO^-)		400		kHz
C_LP	Load Capacitance				100	pF
GA_P^+	Gain from VPO^- to VPO^+	$R_L = 600\Omega$ VPO^+ to VPO^- Level at $VPO^- = 1.77$ Vrms		−1		V/V
$PSRR_P$	Power Supply Rejection of V_{CC} or V_{BB}	VPO^- Connected to VPI 0 kHz−4 kHz 4 kHz−50 kHz	 60 36			 dB dB
R_LP	Load Resistance	Connect from VPO^+ to VPO^-	600			Ω

Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$, $T_A = 0°C$ to 70°C by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals are referenced to GNDA. Typicals specified at $V_{CC} = +5.0V$, $V_{BB} = -5.0V$, $T_A = 25°C$. All timing parameters are measured at $V_{OH} = 2.0V$ and $V_{OL} = 0.7V$.

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Frequency of Master Clock	MCLK$_X$ and MCLK$_R$		1.536 1.544 **2.048**		MHz MHz MHz
t_{RM}	Rise Time of Master Clock	MCLK$_X$ and MCLK$_R$			50	ns
t_{FM}	Fall Time of Master Clock	MCLK$_X$ and MCLK$_R$			50	ns
t_{PB}	Period Bit of Clock		485	**488**	15725	ns
t_{RB}	Rise Time of Bit Clock	BCLK$_X$ and BCLK$_R$			50	ns
t_{FB}	Fall Time of Bit Clock	BCLK$_X$ and BCLK$_R$			50	ns
t_{WMH}	Width of Master Clock High	MCLK$_X$ and MCLK$_R$	**160**			ns
t_{WML}	Width of Master Clock Low	MCLK$_X$ and MCLK$_R$	**160**			ns
t_{SBFM}	Set-Up Time from BCLK$_X$ High to MCLK$_X$ Falling Edge		**100**			ns
t_{SFFM}	Set-Up Time from FS$_X$ High to MCLK$_X$ Falling Edge	Long Frame Only	**100**			ns
t_{WBH}	Width of Bit Clock High		**160**			ns
t_{WBL}	Width of Bit Clock Low		**160**			ns
t_{HBFL}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	**0**			ns
t_{HBFS}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	**0**			ns
t_{SFB}	Set-Up Time for Frame Sync to Bit Clock Low	Long Frame Only	**80**			ns
t_{DBD}	Delay Time from BCLK$_X$ High to Data Valid	Load = 150 pF plus 2 LSTTL Loads	0		180	ns
t_{DBTS}	Delay Time to $\overline{TS}_X$ Low	Load = 150 pF plus 2 LSTTL Loads			140	ns
t_{DZC}	Delay Time from BCLK$_X$ Low to Data Output Disabled		50		165	ns
t_{DZF}	Delay Time to Valid Data from FS$_X$ or BCLK$_X$, Whichever Comes Later	$C_L = 0$ pF to 150 pF	20		165	ns
t_{SDB}	Set-Up Time from D$_R$ Valid to BCLK$_{R/X}$ Low		**50**			ns
t_{HBD}	Hold Time from BCLK$_{R/X}$ Low to D$_R$ Invalid		**50**			ns
t_{SF}	Set-Up Time from FS$_{X/R}$ to BCLK$_{X/R}$ Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	**50**			ns
t_{HF}	Hold Time from BCLK$_{X/R}$ Low to FS$_{X/R}$ Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	**100**			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS$_X$ or FS$_R$)	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	**100**			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	**160**			ns

Timing Diagrams

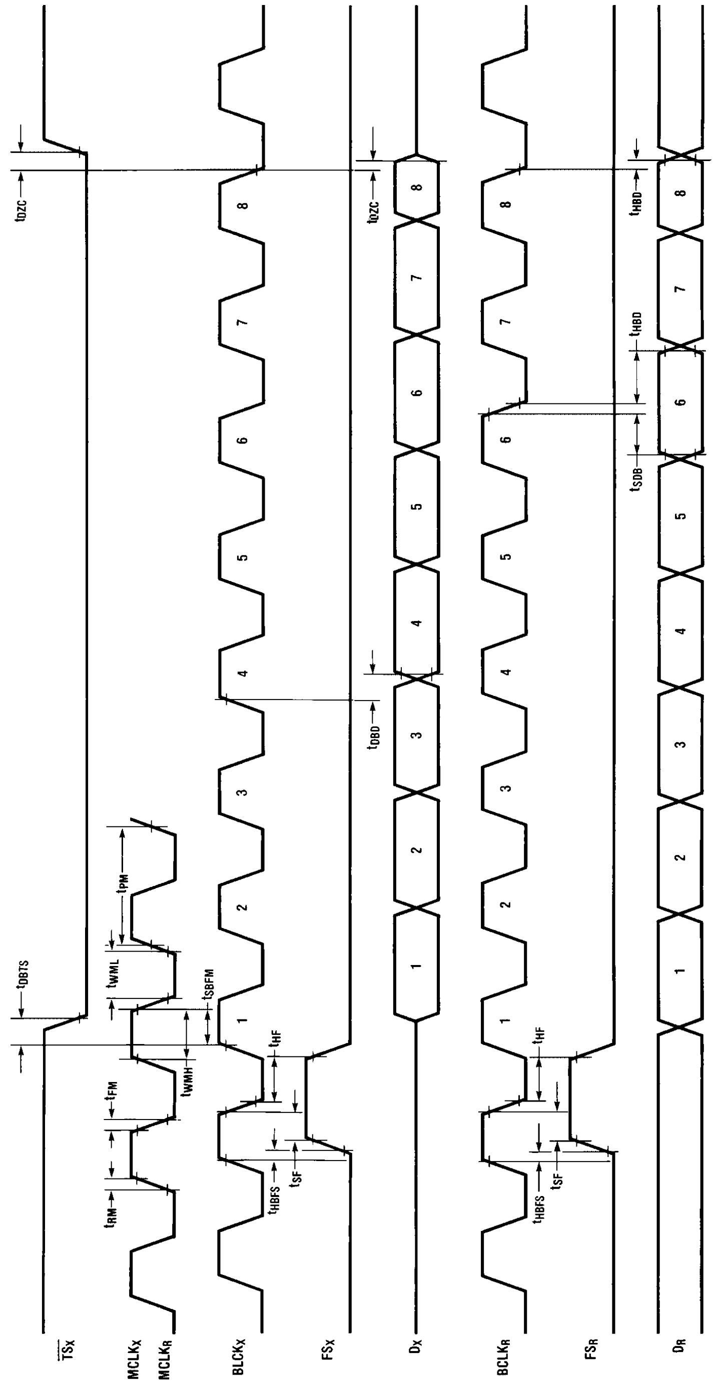

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FIGURE 2. Short Frame Sync Timing

Timing Diagrams (Continued)

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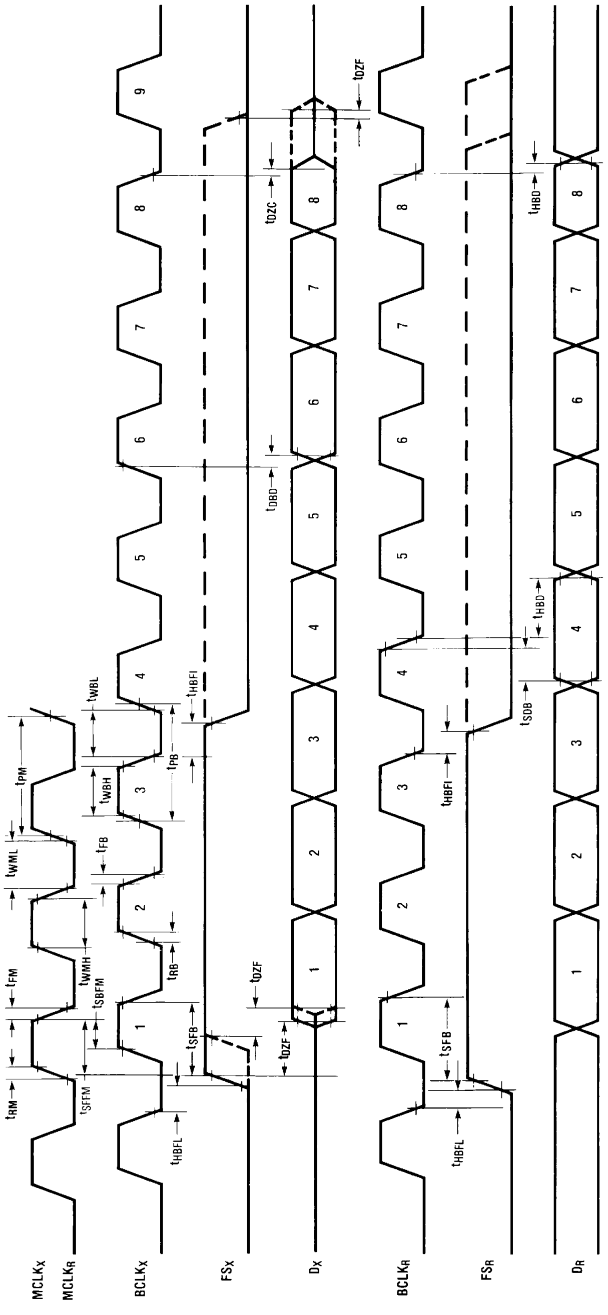


FIGURE 3. Long Frame Sync Timing

Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; $T_A =$ 0°C to 70°C by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dbm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at $V_{CC} = +5.0V$, $V_{BB} = -5.0V$, $T_A = 25°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels (Definition of nominal gain)	Nominal 0 dBm0 Level is 4 dBm (600Ω)				
		0 dBm0		1.2276		Vrms
t_{MAX}	Virtual Decision Value Defined per CCITT Rec. G711	Max Transmit Overload Level				
		TP3064 (3.17 dBm0)		2.501		V_{PK}
		TP3067 (3.14 dBm0)		2.492		V_{PK}
G_{XA}	Transmit Gain, Absolute	$T_A = 25°C$, $V_{CC} = 5V$, $V_{BB} = -5V$	**−0.15**		**0.15**	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f = 16 Hz			−40	dB
		f = 50 Hz			−30	dB
		f = 60 Hz			**−26**	dB
		f = 200 Hz	**−1.8**		**−0.1**	dB
		f = 300 Hz-3000 Hz	**−0.15**		**0.15**	dB
		f = 3300 Hz	**−0.35**		**0.05**	dB
		f = 3400 Hz	**−0.7**		**0**	dB
		f = 4000 Hz			**−14**	dB
		f = 4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz			**−32**	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	Relative to G_{XA}	−0.1		0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	Relative to G_{XA}	**−0.05**		**0.05**	dB
G_{XRL}	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level = −10 dBm0				
		$VF_XI^+ = -40$ dBm0 to $+3$ dBm0	**−0.2**		**0.2**	dB
		$VF_XI^+ = -50$ dBm0 to -40 dBm0	**−0.4**		**0.4**	dB
		$VF_XI^+ = -55$ dBm0 to -50 dBm0	**−1.2**		**1.2**	dB
G_{RA}	Receive Gain, Absolute	$T_A = 25°C$, $V_{CC} = 5V$, $V_{BB} = -5V$ Input = Digital Code Sequence for 0 dBm0 Signal	**−0.15**		**0.15**	dB
G_{RR}	Receive Gain, Relative to G_{RA}	f = 0 Hz to 3000 Hz	**−0.15**		**0.15**	dB
		f = 3300 Hz	**−0.35**		**0.05**	dB
		f = 3400 Hz	**−0.7**		**0**	dB
		f = 4000 Hz			**−14**	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	Relative to G_{RA}	−0.1		0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	Relative to G_{RA}	**−0.05**		**0.05**	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded − 10 dBm0 Signal				
		PCM Level = −40 dBm0 to +3 dBm0	**−0.2**		**0.2**	dB
		PCM Level = −50 dBm0 to −40 dBm0	**−0.4**		**0.4**	dB
		PCM Level = −55 dBm0 to −50 dBm0	**−1.2**		**1.2**	dB
V_{RO}	Receive Filter Output at VF_RO	RL = 10 kΩ	−2.5		2.5	V

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dbm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f=1600 Hz		290	315	µs
D_{XR}	Transmit Delay, Relative to D_{XA}	f=500 Hz−600 Hz		195	220	µs
		f=600 Hz−800 Hz		120	145	µs
		f=800 Hz−1000 Hz		50	75	µs
		f=1000 Hz−1600 Hz		20	40	µs
		f=1600 Hz−2600 Hz		55	75	µs
		f=2600 Hz−2800 Hz		80	105	µs
		f=2800 Hz−3000 Hz		130	155	µs
D_{RA}	Receive Delay, Absolute	f=1600 Hz		180	200	µs
D_{RR}	Receive Delay, Relative to D_{RA}	f=500 Hz−1000 Hz	−40	−25		µs
		f=1000 Hz−1600 Hz	−30	−20		µs
		f=1600 Hz−2600 Hz		70	90	µs
		f=2600 Hz−2800 Hz		100	125	µs
		f=2800 Hz−3000 Hz		145	175	µs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted	TP3064 (Note 1)		12	**15**	dBrnC0
N_{XP}	Transmit Noise, Psophometric Weighted	TP3067 (Note 1)		−74	−**67**	dBm0p
N_{RC}	Receive Noise, C Message Weighted	PCM Code Equals Alternating Positive and Negative Zero TP3064		8	**11**	dBrnCO
N_{RP}	Receive Noise, Psophometric Weighted	PCM Code Equals Positive Zero TP3067		−82	−**79**	dBm0p
N_{RS}	Noise, Single Frequency	f=0 kHz to 100 kHz, Loop Around Measurement, VF_XI^+=0 Vrms			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	V_{CC}=5.0 V_{DC}+100 mVrms f=0 kHz−50 kHz (Note 2)	**40**			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	V_{BB}=−5.0 V_{DC}+ 100 mVrms f=0 kHz−50 kHz (Note 2)	**40**			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{CC}=5.0 V_{DC}+100 mVrms Measure VF_RO				
		f=0 Hz−4000 Hz	**38**			dBC
		f=4 kHz−50 kHz	**25**			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{BB}=−5.0 V_{DC}+100 mVrms Measure VF_RO				
		f=0 Hz−4000 Hz	**40**			dBC
		f=4 kHz−25 kHz	**40**			dB
		f=25 kHz−50 kHz	**36**			dB
SOS	Spurious Out-of-Band Signals at the Channel Output	0 dBm0, 300 Hz−3400 Hz Input PCM Code Applied at DR Measure Individual Image Signals at VF_RO				
		4600 Hz–7600 Hz			−**32**	dB
		7600 Hz–8400 Hz			−40	dB
		8400 Hz–100,000 Hz			−**32**	dB

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dbm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DISTORTION						
STD_X, STD_R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method (Note 3)				
		Level=3.0 dBm0	**33**			dBC
		=0 dBm0 to −30 dBm0	**36**			dBC
		=−40 dBm0 XMT	**29**			dBC
		RCV	**30**			dBC
		=−55 dBm0 XMT	**14**			dBC
		RCV	**15**			dBC
SFD_X	Single Frequency Distortion, Transmit				**−46**	dB
SFD_R	Single Frequency Distortion, Receive				**−46**	dB
IMD	Intermodulation Distortion	Loop Around Measurement, VF_XI^+ = −4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz−3400 Hz			−41	dB
CROSSTALK						
$CT_{X\text{-}R}$	Transmit to Receive Crosstalk	f=300 Hz−3000 Hz D_R=Quiet PCM Code		−90	**−75**	dB
$CT_{R\text{-}X}$	Receive to Transmit Crosstalk	f=300 Hz−3000 Hz, VF_XI=0V (Note 2)		−90	**−70**	dB
POWER AMPLIFIERS						
V_OPA	Maximum 0 dBm0 Level (Better than ±0.1 dB Linearity over the Range −10 dBm0 to +3 dBm0)	Balanced Load, R_L Connected Between VPO^+ and VPO^-.				
		R_L=600Ω	**3.3**			Vrms
		R_L=1200Ω	3.5			Vrms
S/D_P	Signal/Distortion	R_L=600Ω	50			dB

Note 1: Measured by extrapolation from the distortion test result at −50 dBm0.

Note 2: $PPSR_X$, $NPSR_X$, and CT_{R-X} are measured with a −50 dBm0 activation signal applied to VF_XI^+.

Note 3: TP3064 is measured using C message weighted filter. TP3067 is measured using psophometric weighted filter.

Applications Information

POWER SUPPLIES

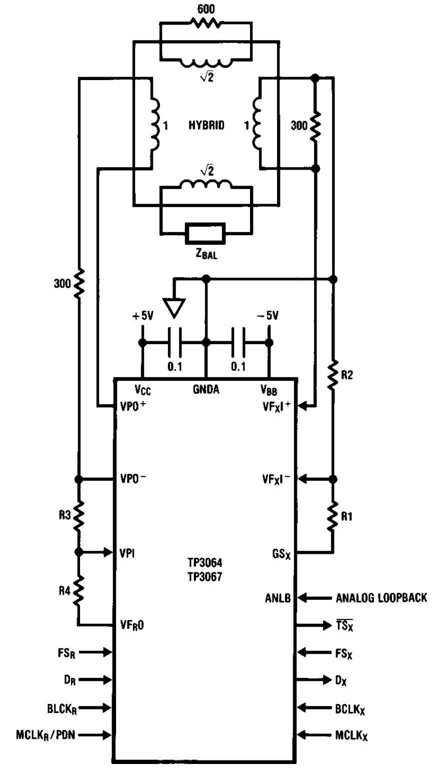
While the pins of the TP3060 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}, as close to the device as possible.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in "STAR" formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

Note: See Application Note 370 for further details

Typical Asynchronous Application



TL/H/5070-5

Note 1: Transmit gain $= 20 \times \log \left(\frac{R1 + R2}{R2}\right)$, $(R1 + R2) \geq 10\ k\Omega$

Note 2: Receive gain $= 20 \times \log \left(\frac{2 \times R3}{R4}\right)$, $R4 \geq 10\ k\Omega$

FIGURE 4

Definitions and Timing Conventions

DEFINITIONS

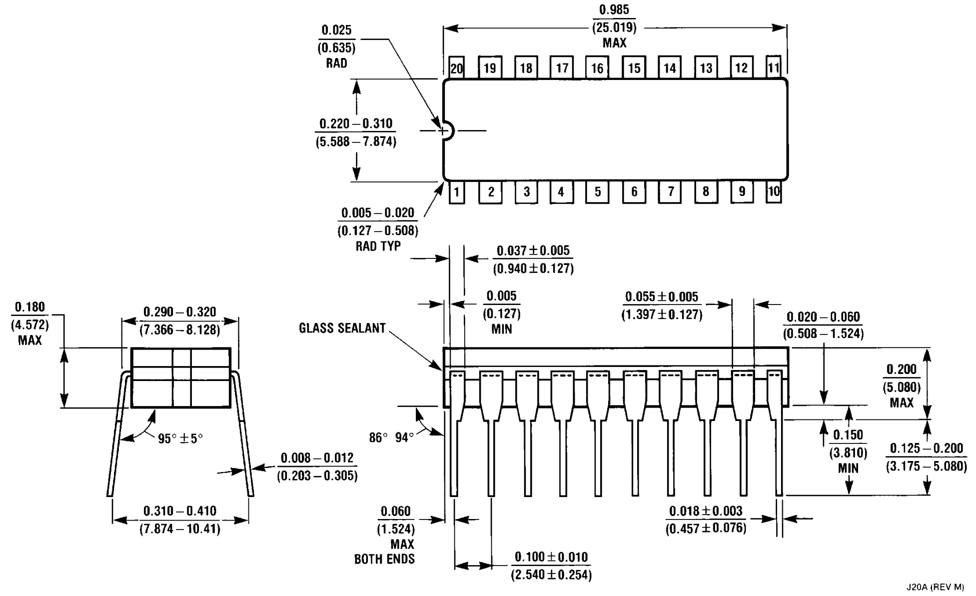
V_{IH}	V_{IH} is the d.c. input level above which an input level is guaranteed to appear as a logical one. This parameter is to be measured by performing a functional test at reduced clock speeds and nominal timing, (i.e. not minimum setup and hold times or output strobes), with the high level of all driving signals set to V_{IH} and maximum supply voltages applied to the device
V_{IL}	V_{IL} is the d.c. input level below which an input level is guaranteed to appear as a logical zero to the device. This parameter is measured in the same manner as V_{IH} but with all driving signal low levels set to V_{IL} and minimum supply voltages applied to the device.
V_{OH}	V_{OH} is the minimum d.c. output level to which an output placed in a logical one state will converge when loaded at the maximum specified load current.
V_{OL}	V_{OL} is the maximum d.c. output level to which an output placed in a logical zero state will converge when loaded at the maximum specified load current.
Threshold Region	The threshold region is the range of input voltages between V_{IL} and V_{IH}.
Valid Signal	A signal is Valid if it is in one of the valid logic states, (i.e. above V_{IH} or below V_{IL}). In timing specifiations, a signal is deemed valid at the instant it enters a valid state.
Invalid Signal	A signal is Invalid if it is not in a valid logic state, i.e. when it is in in the threshold region between V_{IL} and V_{IH}. In timing specifications, a signal is deemed Invalid at the instant it enters the threshold region.

TIMING CONVENTIONS

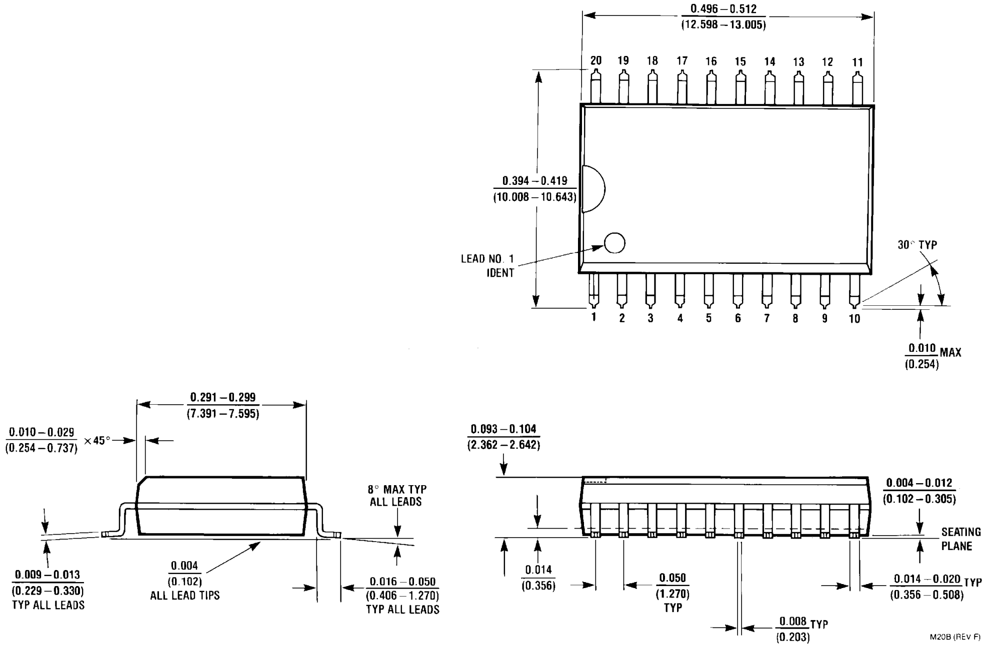
For the purposes of this timing specification, the following conventions apply:

Input Signals	All input signals may be characterized as: $V_L = 0.4V$, $V_H = 2.4V$, $t_R < 10$ ns, $t_F < 10$ ns.
Period	The period of clock signal is designated as t_{Pxx} where xx represents the mnemonic of the clock signal being specified.
Rise Time	Rise times are designated as t_{Ryy}, where yy represents a mnemonic of the signal whose rise time is being specified. t_{Ryy} is measured from V_{IL} to V_{IH}.
Fall Time	Fall times are designated as t_{Fyy}, where yy represents a mnemonic of the signal whose fall time is being specified. t_{Fyy} is measured from V_{IH} to V_{IL}.
Pulse Width High	The high pulse width is designated as t_{WzzH}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. High pulse widths are measured from V_{IH} to V_{IH}.
Pulse Width Low	The low pulse width is designated as t_{WzzL}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. Low pulse widths are measured from V_{IL} to V_{IL}.
Setup Time	Setup times are designated as t_{Swwxx}, where ww represents the mnemonic of the input signal whose setup time is being specified relative to a clock or strobe input represented by mnemonic xx. Setup times are measured from the ww Valid to xx Invalid.
Hold Time	Hold times are designated as t_{Hxxww}, where ww represents the mnemonic of the input signal whose hold time is being specified relative to a clock or strobe input represented by mnemonic xx. Hold times are measured from xx Valid to ww Invalid.
Delay Time	Delay times are designated as t_{Dxxyy} Hi to Low, where xx represents the mnemonic of the input reference signal and yy represents the mnemonic of the output signal whose timing is being specified relative to xx. The mnemonic may optionally be terminated by an H or L to specify the high going or low going transition of the output signal. Maximum delay times are measured from xx Valid to yy Valid. Minimum delay times are measured from xx Valid to yy Invalid. This parameter is tested under the load conditions specified in the Conditions column of the Timing Specifications section of this data sheet.

Physical Dimensions inches (millimeters)

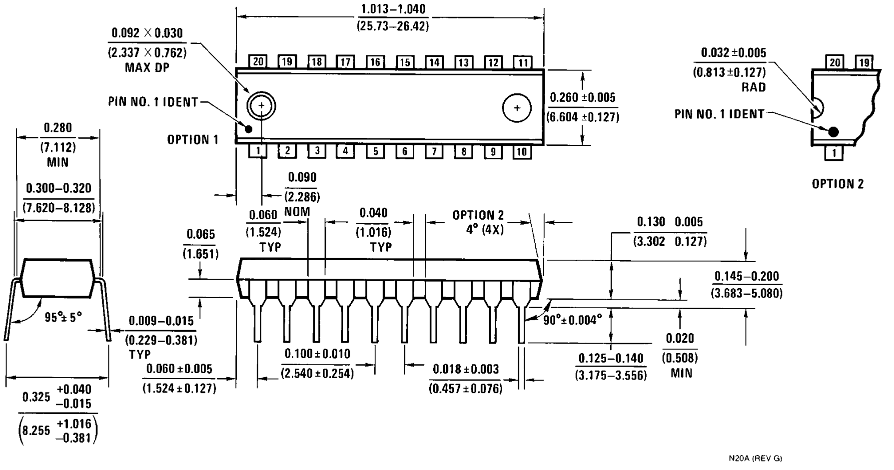


Cavity Dual-In-Line Package (J)
Order Number TP3064J or TP3067J
NS Package Number J20A



Molded Small Outline Package (WM)
Order Number TP3064WM or TP3067WM
NS Package Number M20B

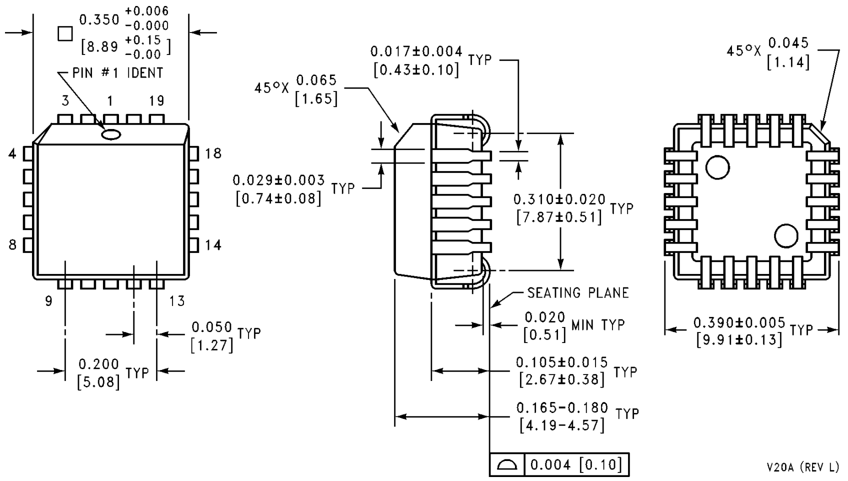
Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number TP3064N or TP3067N
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)

Lit. # 113975



Plastic Chip Carrier (V)
Order Number TP3064V or TP3067V
NS Package Number V20A

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