National Semiconductor

PRELIMINARY
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TP3464/TP3465 MICROWIRE™ Interface Device (MID)

General Description

The MICROWIRE™ Interface Device MID gives a general microprocessor (such as National Series 32000® processors, Intel 80C188, 80C86 or 80286, Motorola 6800 and 68000 family of processors) the ability to communicate efficiently with up to eight peripheral devices via the serial MICROWIRE interface. The MID causes each of the peripheral devices to appear to the μP as memory mapped locations, by performing all the data serialization and transfer protocols to and from the peripherals.

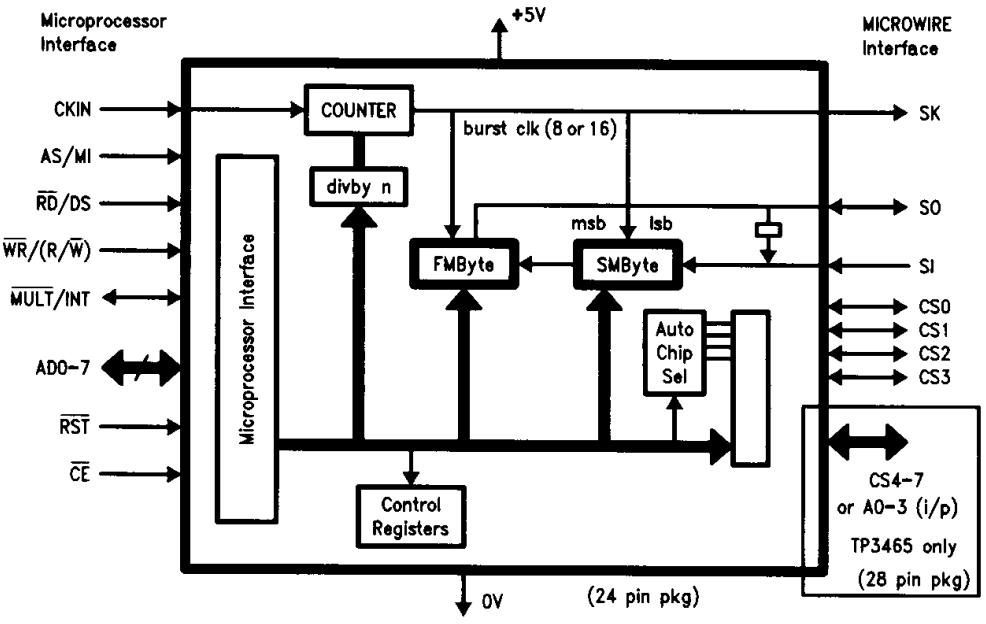
Applications

- ISDN Terminal Adapters
- Digital Line cards (ISDN and Non ISDN)
- Analog Linecards using National COMBO II™
- Interfacing to industry standard serial EEPROMs
- Interfacing to industry standard MICROWIRE peripheral devices such as Analog to Digital Converters, LCD drivers, clock generators

Features

- Multiplexed and Non-multiplexed microprocessor bus compatible
- National/Intel and Motorola microprocessor bus compatible
- Microprocessor Clock (CKIN) up to 20 MHz
- MICROWIRE clock speeds up to 5 MHz
- Directly compatible with 8- and 16-bit MICROWIRE peripherals
- TP3464 for 4 Chip Select outputs (24-pin)
- TP3465 for 8 Chip Select outputs (28-pin)
- Memory mapped peripherals
- Programmable MICROWIRE Clock to communicate with devices of different speeds
- Operates as MICROWIRE bus master or slave
- 24-pin Skinny-DIP pkg or 28-pin PLCC, DIP
- CMOS, Low Power

Block Diagram



TL/H/10803–1

FIGURE 1. MICROWIRE Interface Device MID

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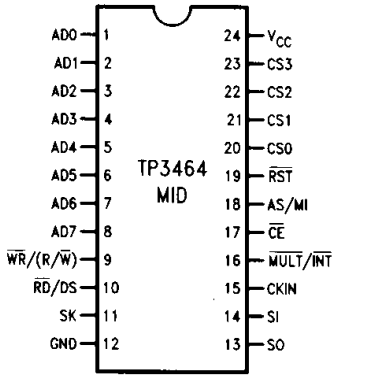
COMBO II™ and MICROWIRE™ are trademarks of National Semiconductor Corporation.

Connection Diagrams

24-Pin Skinny DIP



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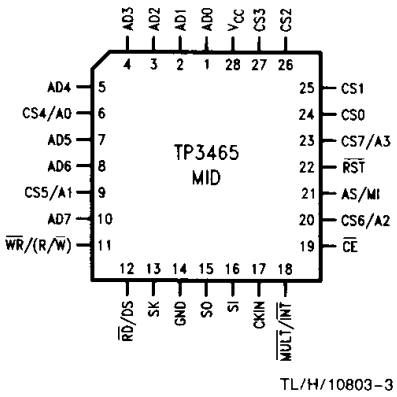
Top View

Order Number TP3464N
See NS Package Number N24C

28-Pin PLCC



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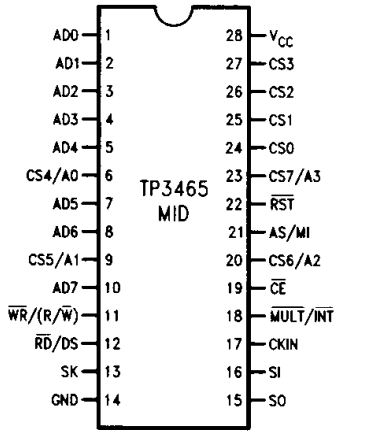
Top View

Order Number TP3465V
See NS Package Number V28A

28-Pin DIP



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Top View

Order Number TP3465N
See NS Package Number N28B

FIGURE 2. MICROWIRE Interface Device MID TP3464/65 Pinouts

Pin Description

Name	Pin No. 24 Pkg.	Pin No. 28 Pkg.	Type	Function
V_{CC}	24	28	I	+ 5V Supply
GND	12	14	I	0V
CKIN	15	17	I	Master Clock Input Used to Derive the SK Clock

MICROWIRE Interface

The MICROWIRE Interface consists of SK (clock out), SO (data out), SI (data in) and up to 8 chip select output lines.

Name	Pin No. 24 Pkg.	Pin No. 28 Pkg.	Type	Function
SK	11	13	O	MICROWIRE clock output.
SO	13	15	O/I	MICROWIRE data output. Can also be used for MICROWIRE data input when communicating with special devices. See application section.
SI	14	16	I	MICROWIRE data input.
CS0–CS3	20–23	24–27	I/O	Four input/output lines, normally used as outputs for chip selects to MICROWIRE peripherals
CS4–CS7		6, 9, 20, 23	I/O	Four additional chip select lines accessible only in 28-pin package and when using the Multiplexed bus mode.

Multiplexed Microprocessor Bus Interface

The $\overline{MULT}/\overline{INT}$ pin is sampled on power-up and, if LOW, the microprocessor bus format is assumed to be Multiplexed and the pin is considered an input pin to indicate Multiplexed bus format. The pin has an internal pull-up and thus if pin is left floating, it will be considered as in Non-multiplexed mode. The interface consists of an eight bit multiplexed Address/Data microprocessor bus (only the A0, A1, A2 and A3 address lines are decoded), and six control lines ($\overline{CE}$, $\overline{RST}$, AS/MI, $\overline{RD}$/DS, $\overline{WR}$/(R/$\overline{W}$) and the $\overline{MULT}$ input) which should be tied LOW.

Name	Pin No. 24 Pkg.	Pin No. 28 Pkg.	Type	Function
AD0–AD7	1–8	1, 2, 3, 4, 5, 7, 8, 10	I/O	Address/Data bus. Transfers addresses and data between the microprocessor and the MID.
$\overline{CE}$	17	19	I	Chip Enable. A LOW on this signal selects the MID for a Read/Write operation.
$\overline{WR}$/ R/$\overline{W}$	9	11	I	Write or Read-Write direction. This signal indicates a Write operation or Read/Write direction signal.
$\overline{RD}$/DS	10	12	I	Read or Data Strobe. This signal indicates a Read operation or a Data strobe signal.
AS/MI	18	21	I	Address Latch Enable or Address Strobe. A HIGH on this line indicates an address on the external A/D bus. When MULT = 1 (non-multiplexed bus), the pin indicates the type of bus, MI = 1 for NSC/Intel format and MI = 0, for Motorola format.
$\overline{RST}$	19	22	I	The $\overline{RST}$ is the master Reset input, when LOW forces the device in the RESET condition (same as Power-on-Reset).
$\overline{MULT}$/ $\overline{INT}$	16	18	I	Multiplexed Bus input or INTerrupt output. It is internally pulled HIGH to indicate a Non-Multiplexed bus format and needs to be pulled LOW externally to indicate the Multiplexed bus format.

Non-Multiplexed Microprocessor Interface

The $\overline{MULT}/\overline{INT}$ pin is sampled on power-up and, if not LOW, the microprocessor bus format is assumed to be Non-multiplexed. This interface consists of a four-bit Address bus, an eight-bit Data bus and six control lines ($\overline{CE}$ $\overline{RST}$, AS/MI, $\overline{RD}$/DS, $\overline{WR}$/(R/$\overline{WR}$) and the $\overline{INT}$ signal if enabled).

Name	Pin No. 28 Pkg.	Type	Function
A0–A3	6, 9, 20, 23	I	Address bus. These 4 pins (accessible in the 28-pin package) are used to address the 16 registers.
D0–D7	1, 2, 3, 4, 5, 7, 8, 10	I/O	Data bus for data transfer between the microprocessor and the MID.
$\overline{CE}$	19	I	Chip Enable. A LOW on this signal selects the MID for a Read/Write operation.
$\overline{WR}$/ (R/$\overline{W}$)	11	I	Write or Read-Write direction. This signal indicates a Write operation or Read/Write direction signal.
$\overline{RD}$/DS	12	I	Read or Data Strobe. This signal indicates a Read operation or a Data Strobe signal.
AS/MI	21	I	Address Latch Enable or Address Strobe. A HIGH on this line indicates an address on the external A/D bus. When MULT = 1 (non-multiplexed bus), the pin indicates the type of bus, MI = 1 for NSC/Intel format and MI = 0 for Motorola format.

Non-Multiplexed Microprocessor Interface (Continued)

The $\overline{MULT}/\overline{INT}$ pin is sampled on power-up and, if not LOW, the microprocessor bus format is assumed to be Non-multiplexed. This interface consists of a four-bit Address bus, an eight-bit Data bus and six control lines ($\overline{CE}$ $\overline{RST}$, AS/MI, $\overline{RD}$/DS, $\overline{WR}$/(R/$\overline{WR}$) and the $\overline{INT}$ signal if enabled).

Name	Pin No. 28 Pkg.	Type	Function
$\overline{RST}$	22	I	The $\overline{RST}$ is the master Reset input; when LOW, it forces the device in the RESET condition (same as Power-on-Reset).
$\overline{MULT}$/ $\overline{INT}$	18	I O	Multiplexed Bus input or INTerrupt output. It is internally pulled HIGH to indicate a Non-multiplexed bus format and the pin can be an $\overline{INT}$ output pin if enabled by setting the **Inten** bit in the CKR register. $\overline{INT}$ pulls low to indicate the completion of a MICROWIRE transfer operation.

Functional Description

The block diagram of the MICROWIRE Interface Device (MID) is shown in *Figure 1*. It essentially consists of a very flexible microprocessor bus interface, a serial MICROWIRE interface and a Chip Select (output) port. Internally it contains a programmable clock divider to derive the MICROWIRE clock speed from a system clock.

MICROPROCESSOR INTERFACE

The Microprocessor bus interface supports both National/Intel and Motorola bus formats in the Multiplexed and Non-multiplexed bus modes.

The $\overline{MULT}/\overline{INT}$ pin is sampled on power-up and, if LOW, the microprocessor bus format is assumed to be Multiplexed and the pin is considered an input pin to indicate Multiplexed bus format. The pin is internally pulled HIGH. Upon sampling, if the pin is not LOW, the bus format is assumed to be Non-multiplexed.

The microprocessor interface supports multiplexed Address/Data Formats for the Intel 8088/80188 and Motorola 6803 families to work in 8-bit mode. Non-multiplexed busses of the National 32000, Intel 80286 and Motorola 68000, series processors and similar are supported in the TP3465 28-pin part. Four address lines allow access to all MID registers.

The MID incorporates a flexible bus interface logic to support the different address and data strobes required by the different bus formats. The timing specifications are shown in a later section. The following table shows microprocessor bus control pin functions:

MID Pin	NSC/Intel Bus		Motorola Bus	
	MUXed	Non-MUXed	MUXed	Non-MUXed
AS/MI	ALE	MI = 1	AS	MI = 0
$\overline{RD}$/DS	$\overline{RD}$	$\overline{RD}$	DS	DS
$\overline{WR}$/(R/$\overline{W}$)	$\overline{WR}$	$\overline{WR}$	(R/$\overline{W}$)	(R/$\overline{W}$)

MICROWIRE COMMUNICATION MODES

The MID provides a MICROWIRE port to the main processor having two modes of operation with the MICROWIRE peripherals. **Software controlled chip select** and **hardware generated chip select** modes.

In the first scheme, besides the 2 data byte registers, there is a third register which maps directly with the output CS Chip Selects pins (4 in the TP3464 24-pin package and 8 in the TP3465 28-pin package). The software in the microprocessor then writes to the CS register to select and deselect individual bits (corresponding to pins).

In the second scheme, the CS pins are activated by a hardware state machine when triggered by accessing the data registers through other address locations (see section on Register description). In this case the hardware will activate the chip select pin, send the appropriate number of MICROWIRE data bits (8 or 16) and then deselect the pin. This enhanced mode of communication allows the MICROWIRE peripheral devices to appear as if I/O mapped in the microprocessor's memory space.

CONTROL AND DATA REGISTERS

There are 6 control registers (PD, MWM, SKP, SKR, ST and CS), and **1 set of Data registers (First MICROWIRE Byte FMB and Second MICROWIRE Byte SMB)** for data communication to MICROWIRE devices. In normal mode, the Chip select pins CS0–C7 are controlled (via the CS register) by software and data is transferred via the FMB and SMB registers located at address 01h and 00h (see Table I).

Eight additional addresses (FMBD0–7) access the same data register (FMB) but provide additional information to an internal state machine which drives appropriate chip select pins (e.g., FMBD0 at address 02h controls CS0 pin, FMBD1 at address 03h controls CS1 pin etc.). **There is only 1 set of Data registers (FMB and SMB) which handle the MICROWIRE communication.** This latter method of allocating special addresses to provide pin-select information facilitates an enhanced MICROWIRE interface to the host processor.

Table I summarizes the Control and Data Registers and the addresses at which they are accessed.

Functional Description (Continued)

TABLE I. Control and Data Registers

Address	Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	SMB	d7	d6	d5	d4	d3	d2	d1	d0
01h	FMB	d7	d6	d5	d4	d3	d2	d1	d0
02h	FMBD0	d7	d6	d5	d4	d3	d2	d1	d0
03h	FMBD1	d7	d6	d5	d4	d3	d2	d1	d0
04h	FMBD2	d7	d6	d5	d4	d3	d2	d1	d0
05h	FMBD3	d7	d6	d5	d4	d3	d2	d1	d0
06h	FMBD4	d7	d6	d5	d4	d3	d2	d1	d0
07h	FMBD5	d7	d6	d5	d4	d3	d2	d1	d0
08h	FMBD6	d7	d6	d5	d4	d3	d2	d1	d0
09h	FMBD7	d7	d6	d5	d4	d3	d2	d1	d0
0Ah	CS	cs7	cs6	cs5	cs4	cs3	cs2	cs1	cs0
0Bh	SKP	skp7	skp6	skp5	skp4	skp3	skp2	skp1	skp0
0Ch	MWM	mwm7	mwm6	mwm5	mwm4	mwm3	mwm2	mwm1	mwm0
0Dh	SKR	inten	soi	ms	0	0	div2	div1	div0
0Eh	ST	uwdone	0	0	0	0	0	0	0
0Fh	PD	pd7	pd6	pd5	pd4	pd3	pd2	pd1	pd0

PD—Pin Definition Register: W Register

RESET condition is FFhex (all pins as Inputs)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
pd7	pd6	pd5	pd4	pd3	pd2	pd1	pd0

pd0–7 bits configure the CS0–7 pins as inputs or outputs. For example **pd0** = 1, sets the CS0 pin as an input; **pd0** = 0, sets CS0 pin as an output. Upon chip RESET, the **pd0–7** bits are set to 1.

SKP—MICROWIRE Clock (SK) Polarity: W Register

RESET condition is 00hex (Normal MICROWIRE clock)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
skp7	skp6	skp5	skp4	skp3	skp2	skp1	skp0

skp 0–7 bits set the polarity of the SK MICROWIRE clock when communicating with device connected to each of the pins CS0–7. For example **skp0** = 0, normal MICROWIRE mode (i.e., SO data output on negative edge of SK clock) when sending data to device controlled by CS0 pin; **skp1** = 1, NSC COMBO II clock format for device controlled by CS1 (i.e., SO data output on the positive edge of SK clock).

MWM—MICROWIRE Mode Register: W Register

RESET condition is 00hex

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
mwm7	mwm6	mwm5	mwm4	mwm3	mwm2	mwm1	mwm0

mwm0–7 bits specify whether 8 or 16 clocks are generated for devices connected to CS0–7 pins. For example **mwm1** = 1, 16 clocks will be generated for device controlled by CS1, (16 data bits will be shifted out and 16 data bits will be strobed in); **mwm0** = 0, 8 clocks will be generated for device controlled by CS0 (8 data bits will be shifted out and strobed in).

SKR—MICROWIRE Clock (SK) Rate Register: W Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
inten	soi	ms	0	0	div2	div1	div0

The 3 bits **div0–2** give the divide-by value for deriving the SK clock output rate from the CKIN. The maximum CKIN rate is 20 MHz, and the slowest MICROWIRE peripheral works at 256 kHz. Table 2 below gives the division ratios and some examples:

div2	div1	div0	SK Ratio	e.g., CKIN = 5 MHz	e.g., CKIN = 20 MHz
0	0	0	SK = CKIN	SK = 5 MHz	
0	0	1	SK = CKIN/2	SK = 2.5 MHz	
0	1	0	SK = CKIN/4	= 1.25 MHz	SK = 5 MHz
0	1	1	SK = CKIN/8	= 625 kHz	= 2.5 MHz
1	0	0	SK = CKIN/16	= 312.5 kHz	= 1.25 MHz
1	0	1	SK = CKIN/32	= 156.25 kHz	= 625 kHz
1	1	0	SK = CKIN/64	= 78.125 kHz	= 312.5 kHz
1	1	1	SK = CKIN/128	= 39.06 kHz	= 156.25 kHz

TABLE 2. SK Clock Rate Control

Functional Description (Continued)

The **uwdone** bit in the ST register can be connected to the INTerrupt pin of the MID to alert the host processor when MICROWIRE transmission is completed by setting the **inten** bit in this SKR register. The $\overline{INT}$ pin will only be functional as an INTerrupt in the Non-multiplexed bus mode in the 28-pin TP3465 device.

The **soi** bit configures the SO pin to be output (**soi** = 0) or input (**soi** = 1). This bit function is used to perform a Read operation on a device such as NSC TP3071 COMBI II because the TP3071 sends data back on the SO pin. When **soi** = 1, the SO pin functions as the SI input pin, internally, and feeds the data registers. See applications diagrams and software procedures for more details.

The **ms** bit configures the MID device as a Master of MICROWIRE (**ms** = 0) or Slave of MICROWIRE (**ms** = 1). MICROWIRE Slave mode is described and illustrated in the applications section.

CS—Chip Select Port Register: R/W Register

RESET condition, CS pins are inputs and the register contains the state of these pins.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
cs7	cs6	cs5	cs4	cs3	cs2	cs1	cs0

cs0–7 bits control the 8, CS input/output port pins. Only **cs0–3** are available in TP3464 24-pin package and in the TP3465 device when used in the non-multiplexed bus format. In the multiplexed bus format in TP3465, all 8 CS pins are accessible.

Writing to this register will affect the pins (configured as outputs in PD register) directly. Similarly, the state of the pins which are configured as inputs in the PD registers can be Read via the same (CS) register. When reading the pins designated as outputs, the bits will have a "1" condition. Writing to bits corresponding to input pins will have no effect on the pins.

The state of an output chip select pin may also be controlled by the chip hardware state machine if the user writes to the FMBD0–7 registers. The hardware can only bring the appropriate pin LOW for the duration of the MICROWIRE transfer and will attempt to set it HIGH at the end of the transfer. If the user has, however, set this pin to be LOW by writing to this register, it will over-ride the action of the hardware and the pin will remain LOW. Thus the user must write a "1" in the bits that will be controlled by hardware, and the pins must be set as outputs in the PD register.

ST—MICROWIRE Status Register: R Register

RESET Condition, Read 80 Hex

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
uwdone	0	0	0	0	0	0	0

The **uwdone** bit (read only) in the ST register can be polled by the software to determine the end of the MICROWIRE transmission (**uwdone** = 1). **uwdone** = 0 during transmission.

FMB—First MICROWIRE Byte: R/W Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
d7	d6	d5	d4	d3	d2	d1	d0

SMB—Second MICROWIRE Byte: R/W Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
d7	d6	d5	d4	d3	d2	d1	d0

The SMB and the FMB data registers are used to communicate to any MICROWIRE device 0–7 (connected to pins CS0–7) when controlling the chip select lines via CS register (using software). The MICROWIRE parameters for this mode of operation are defined by the parameters for device 7, i.e., **skp7** in SKP register, and **mwm7** in MWM register. So when communicating with peripherals requiring different formats, the skp7 and mwm7 bits may need to be re-configured before sending data to each of these devices. Example of communication to 8-bit and 16-bit peripherals are described below:

Example 1: Communicating with an 8-bit MICROWIRE peripheral at CS1:

Set the **skp7** bit to 0 (normal MICROWIRE polarity), and set the **mwm7** to 0 for 1 byte operation). Set **cs1** bit to 0 to select the device. Write the data into the FMB byte location and it gets shifted out after the trailing edge of the Write strobe signal. At the end of the MICROWIRE transmission. Set the **cs1** bit to 1 to de-select the device. The 8-bit STATUS from the peripheral is Read from the FMByte location.

Example 2: Communicating with a 16-bit MICROWIRE peripheral at CS3:

MICROWIRE protocol specifies that the Most Significant Bit is transmitted first. Thus the HIGH byte of data becomes the First MICROWIRE Byte to be sent out.

Set the **skp7** bit to 0 (normal MICROWIRE polarity), and set the **mwm7** to 1 for 2 byte operation). Set **cs3** bit to 0 to select the device. Write the LOW data byte in the SMB register and then write the HIGH data byte into the FMB byte location. All 16 data bits get shifted out after the trailing edge of the Write strobe for the FMB register. At the end of the MICROWIRE transmission. Set the **cs3** bit to 1 to de-select the device. The 16-bit STATUS from the peripheral is Read from the FMB (HIGH data byte) and the SMB (LOW data byte) locations.

FMBD0—First MICROWIRE Byte Dev0: R/W Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
d7	d6	d5	d4	d3	d2	d1	d0

There is *only one set of data registers (FMB and SMB)* which handle the MICROWIRE data communication. *The FMBD0 address accesses the data register FMB but also provides information for the internal state machine to control the CS0 pin.* The MICROWIRE parameters for device 0 are indicated by the state of bits **skp0** and **mwm0**, etc.

Functional Description (Continued)

Example 1: Communicating with 8-bit peripheral—device 0:

The **mwm0** bit must be set to 0. Write the MICROWIRE data in to the FMBD0 address and the 8-bit data is shifted out after the trailing edge of the write pulse. The Chip Select (CS0) is automatically activated (LOW) and deactivated (HIGH) by hardware before and after the data transfer (see timing diagrams). The 8-bit STATUS from the peripheral is read from the FMBD0 byte location.

Example 2: Communicating with 16-bit peripheral—device 0:

The **mwm0** bit must be set to 1. Write the LOW byte of MICROWIRE data into the SMB data register and then write the HIGH byte in to the FMBD0 address. The 16-bit data is then shifted out after the trailing edge of the write strobe signal for this FMBD0 address. The Chip Select 0 (CS0) pin is automatically activated (LOW) and deactivated (HIGH) by hardware before and after the data transfer (see timing diagrams). The 16-bit STATUS from the peripheral is Read from the FMBD0 (HIGH data byte) and the SMB (LOW data byte) locations.

FMBD1—First MICROWIRE Byte Dev1: R/W Register

Same function as FMBD0 except this refers to Device 1 and Chip Select 1 (CS1).

FMBD2—First MICROWIRE Byte Dev2: R/W Register

Same function as FMBD0 except this refers to Device 2 and Chip Select 2 (CS2).

FMBD3—First MICROWIRE Byte Dev3: R/W Register

Same function as FMBD0 except this refers to Device 3 and Chip Select 3 (CS3).

FMBD4—First MICROWIRE Byte Dev4: R/W Register

Same function as FMBD0 except this refers to Device 4 and Chip Select 4 (CS4).

FMBD5—First MICROWIRE Byte Dev5: R/W Register

Same function as FMBD0 except this refers to Device 5 and Chip Select 5 (CS5).

FMBD6—First MICROWIRE Byte Dev6: R/W Register

Same function as FMBD0 except this refers to Device 6 and Chip Select 6 (CS6).

FMBD7—First MICROWIRE Byte Dev7: R/W Register

Same function as FMBD0 except this refers to Device 7 and Chip Select 7 (CS7).

MICROWIRE Master/Slave Modes

MICROWIRE MASTER MODE

The primary application for MID is as a master of MICROWIRE bus (**ms** bit in CKR register set to 0), and as such it provides the SK clock out to the peripheral devices. It transmits data on the SO pin and receives data on the SI pin. The CS0–7 pins are used as chip select pins for the peripherals and have predefined relationship with the SK clock output. Writing to the FMB pin causes the most significant bit to be output immediately to the SO pin and the **uwdone** bit is reset to 0 by hardware. Upon completion of transfer of either 8 bits (**mwm7** = 0) or 16 bits (**mwm7** = 1), the **uwdone** bit is set to 1 by hardware. The SO pin is then set to TRI-STATE® condition. Note that when using the FMB and SMB registers, the communication mode is determined by the parameters for channel 7 (mwm7 and skp7).

MICROWIRE SLAVE MODE

The MID can be set to work in MICROWIRE Slave mode by setting the **ms** bit to 1. The MICROWIRE clock from the master is connected to the CKIN pin of this MID device. The SK output is ignored. Normally the SO pin is in TRI-STATE condition and while the uwdone bit is 1, any CKIN clock inputs are ignored. Writing to the FMB register causes the most significant bit to be output immediately to the SO pin and the **uwdone** bit is reset to 0 by hardware. The SK clock input is then enabled to clock data into SI and out of SO pins. After receiving SK clock pulses; either 8 (**mwm7** = 0) or 16 bits (**mwm7** = 1); the **uwdone** bit is set to 1 by hardware. The SO pin is then set to TRI-STATE condition. Note that when using the FMB and SMB registers, the communication mode is determined by the parameters of channel 7 (mwm7 and skp7).

FMBD0–7 addresses are not used in the slave mode. The CS register, however, can be used as a general I/O port control register.

See applications section for an example of the Slave operation *(Figure 6)*.

MICROWIRE BUS FORMATS

MID supports devices which implement the two MICROWIRE bus formats; a 3-pin format and a 4-pin format. *Figure 3* shows a MID connected to devices supporting each of these formats.

The standard 4-pin format† consists of the CCLK clock pin, CO and CI as the data out and data in pins, and CS to select the MICROWIRE peripheral. ISDN transceivers and other intelligent peripherals also have an INTerrupt signal from the peripheral to the local microprocessor. NSC MICROWIRE devices with this 4-pin format include ISDN transceivers, COMBO II, LCD display drivers and EEPROMs.

There are, however, some MICROWIRE peripherals (e.g., TP3071 COMBO II, and some EEPROMs) which support a 3-pin bus format because of package pin limitations. The format consists of the CCLK clock signal, a bi-directional data signal CO/CI, and a CS chip select signal. The direction of the data transferred on the CO/CI pin is determined by a protocol between the Master and the Slave of the MICROWIRE bus. For example, the TP3071 implements a two-byte protocol. The first byte into the TP3071 indicates a Read or a Write operation and thus defines the direction of the next byte to the device.

Software Driver Procedures

This section describes the steps for software driver routines to communicate with different MICROWIRE devices (8-bit, 16-bit, or more) and those supporting the 3-pin or 4-pin MICROWIRE bus formats.

INITIALIZATION

1. Write to PD (Pin Definition) register to set the desired chip select control pins (CS0–7) as outputs. (All CS pins are set to inputs on chip RESET.)
2. Write to SKP (SK polarity), to select the polarity of the SK clock for each of the MICROWIRE devices connected to CS0–7 pins.
3. Write to MWM (MICROWIRE Mode) register to select whether 8- or 16-bit devices are attached to the CS0–7 pins. Devices needing more than 16-bits may still be configured as 8-bit mode (if multiple of 8) or 16-bit mode (if multiple of 16 bits).

Software Driver Procedures (Continued)

4. Write to SKR to set the **div** bits to support the fastest SK clock rate supported by the peripherals. Set the **inten** bit if the **uwdone** status is to set an INTerrupt to the host processor (available only in the Non-multiplexed bus implementation of TP3465, 28-pin package). The **ms** and the **soi** bit are set to 0 upon power up and indicate that the MID is in MICROWIRE Master mode, with SO as an output pin as normal.

SENDING DATA TO PERIPHERALS (Normal Mode)

Assume sending 16-bit data to a MICROWIRE based device connected to any one of CS0 to CS7.

1. Write to CS (Chip Select) register and RESET the appropriate bit and thus activate the corresponding CS pin.
2. Write LOW byte data to SMB (Second MICROWIRE Byte) register and then HIGH byte data to FMB (First MICROWIRE Byte) register.
3. Read the ST (Status) register and stay in a loop until **uwdone** bit is set.
4. Write to CS register and Set the bit to deactivate the appropriate chip select pin.

SENDING DATA TO PERIPHERALS (Hardware Assisted Chip Select)

Assuming sending 16-bit data to dev3 connected to CS3 pin.

1. Write LOW byte data to address SMB and then HIGH byte data to FMBD3.
2. Read the ST register and stay in a loop until **uwdone** bit is set.

Communicating with an NSC TP3071 COMBO II Type Device

The NSC TP3071 COMBO II device has a modified MICROWIRE port. It shares a single pin (called CO/CI) for incoming and outgoing data. The MID's SO pin may be tied to this pin, as shown in *Figure 3*, and the following steps are followed to Read from and Write to this device. Assume that the chip select for TP3071 is connected to CS1 pin.

TP3071 **Write** Operation:

a. Initialization states: **skp1** = 1, **mwm1** = 1, and **soi** = 0

b. Data transfer options:

i. Set **cs1** bit to 0, write LOW byte to SMB, and HIGH byte to FMB and then set **cs1** bit to 1 after **uwdone** bit is set to 1. *OR*

ii. Write LOW byte to SMB, and HIGH byte to FMBD1.

TP3071 **Read** Operation:

a. Initialization states: **skp1** = 1, **mwm1** = 0, and **soi** = 0.

b. Data transfer options:

i. Set **cs1** bit to 0, write HIGH byte to FMB, wait until **uwdone** bit is set to 1 by hardware. Set **soi** bit to 1. Write dummy LOW byte (e.g., 00h) to FMB, wait until **uwdone** bit is set to 1 by hardware. Read STATUS from FMB address. Set **soi** to 0 and **cs1** to 1.

OR

ii. Write HIGH byte to FMBD1, wait until **uwdone** bit is set to 1 by hardware. Set **soi** bit to 1. Write a dummy LOW byte (e.g., 00h) to FMBD1 and wait until **uwdone** bit is set to 1 by hardware. Read STATUS from FMBD1 address. Set **soi** bit to 0.

Applications

The TP3464/TP3465 MICROWIRE Interface Device can be used in a number of applications involving MICROWIRE peripheral devices that need to be controlled using a standard microprocessor which only has a parallel bus structure.

ISDN TERMINAL ADAPTER

The MID can be used in ISDN terminal adapters (see *Figure 4*) interfacing to ISDN components such as TP3420 SID, as well as non-ISDN components such as LCD display drivers (e.g., COP470) and serial EEPROMs (COP494). In this application the MID signals SK, SO and SI are bussed to all peripheral devices. Chip selects lines (4 in the 24-pin package and 8 in the 28-pin package) are individually connected to each of the devices. Status Interrupt from the peripherals such as SID are connected directly to the main processor.

ANALOG OR DIGITAL LINECARDS

The MID can also be used in analog and digital (ISDN and Non-ISDN) linecard applications (see *Figure 5*). Up to 8 MICROWIRE peripheral devices (TP3070 COMBO II, or TP3420 SIDs, TP3410 UIDs or TP3401 DASLs) can be connected to one MID device. The Interrupts from the transceivers may be wire-ORed and fed into one interrupt line of the main processor, in which case all the devices will need to be polled after an interrupt. The efficient interface between the MID and microprocessor allows this process to be accomplished with minimum overhead.

In a given application, if any of the chip select pins are not used to perform chip select for peripherals, then it may be used as a general purpose input/output pin under software control.

MID SUPPORTING MASTER AND SLAVE MICROWIRE OPERATION

The MICROWIRE serial data bus is often used as a means of inter-processor communication. The MID may be used either as the Master of the MICROWIRE clock SK or as a Slave to the SK clock fed via CKIN pin. *Figure 6* shows an application in which two general microprocessors communicate with each other over the MICROWIRE bus. At the same time other peripherals are also connected to the serial bus. External handshaking between the two processors is required before the MICROWIRE Byte data transfer is executed by the master of the MICROWIRE bus.

Applications (Continued)

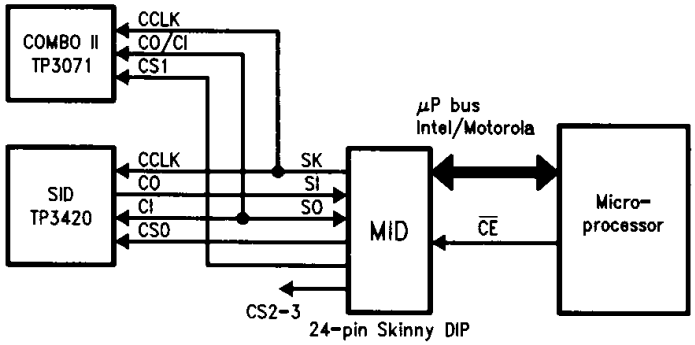

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FIGURE 3. MID, Two Types of Microwire Formats; 3-Pin (e.g., TP3071 COMBO II) and 4-Pin (e.g., TP3420, SID)

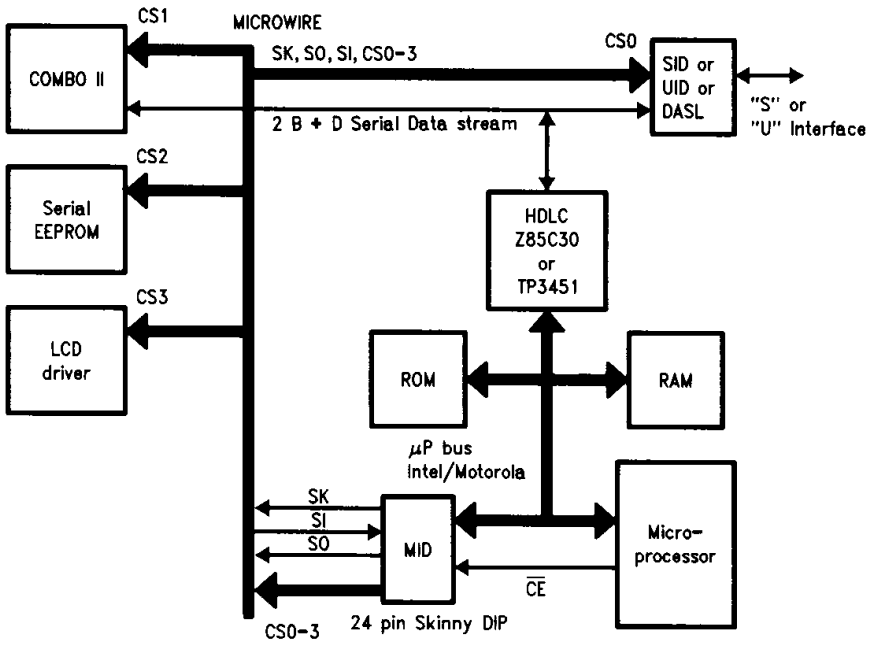

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FIGURE 4. MID, TERMINAL EQUIPMENT Application

†The nomenclature for MICROWIRE signal names is as follows:

MICROWIRE controller—SK (clock), SO (data out), SI (data in)

MICROWIRE peripheral—CCLK (clock), CO (data out), CI (data in).

Applications (Continued)

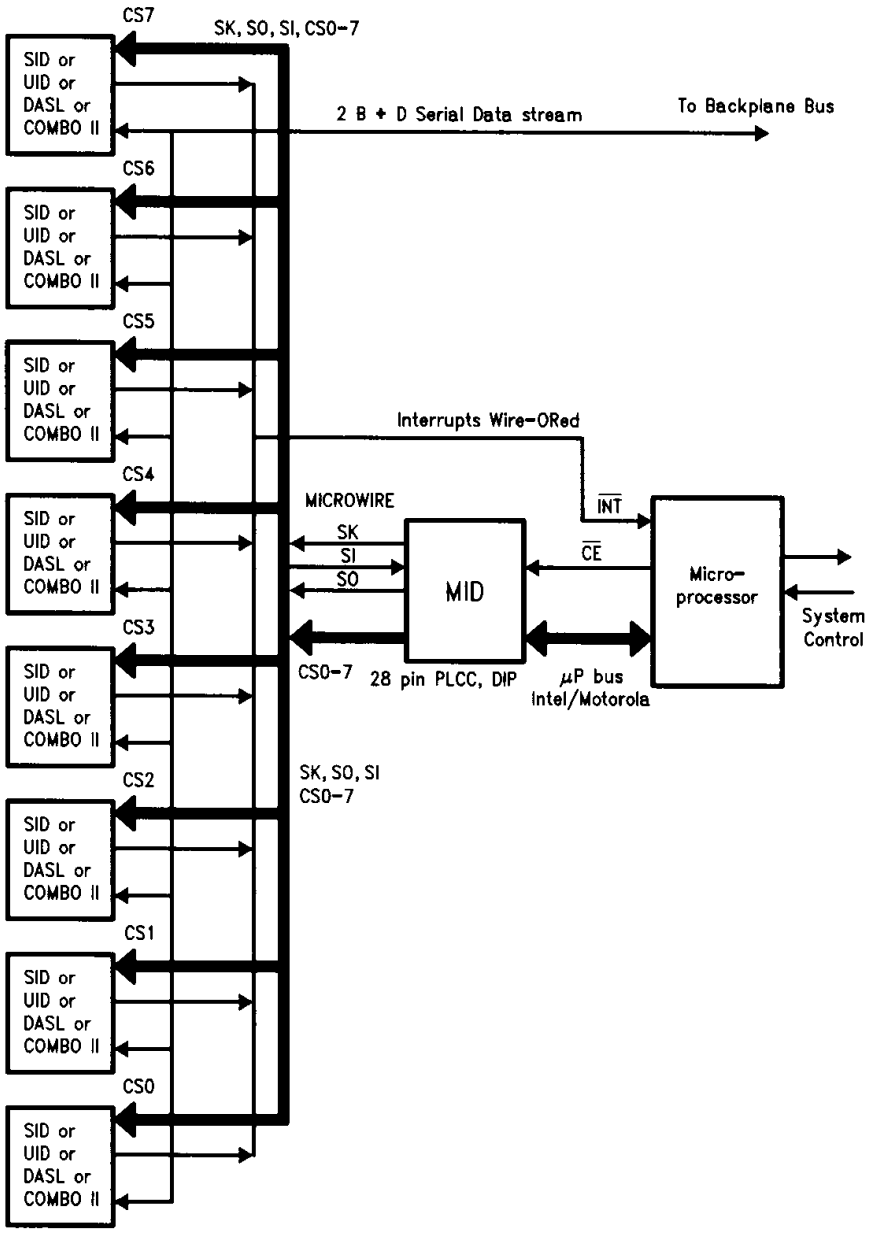

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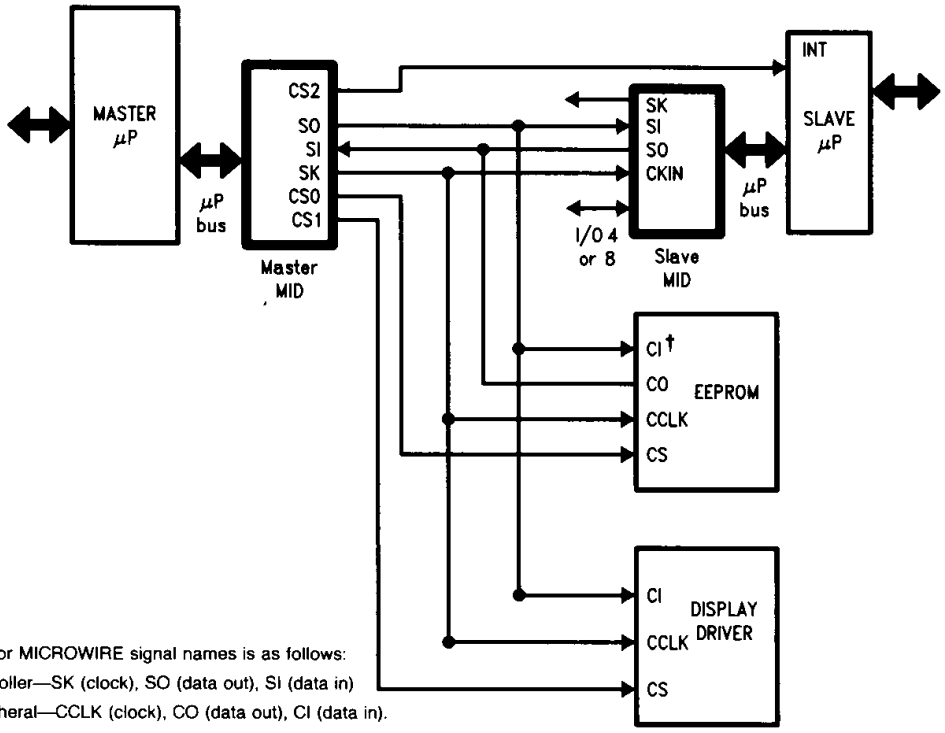
FIGURE 5. MID, LINECARD Application—Digital (ISDN/Non-ISDN) or Analog

Applications (Continued)



†The nomenclature for MICROWIRE signal names is as follows:
MICROWIRE controller—SK (clock), SO (data out), SI (data in)
MICROWIRE peripheral—CCLK (clock), CO (data out), CI (data in).

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FIGURE 6. Example of MID in Master or Slave MICROWIRE Operation

Device Electrical Characteristics

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GND	7V
Input Voltage	−0.3V to V_{CC} + 0.3V
DC Input Current	I_I ± 50 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 Sec.)	300°C
ESD Rating, to be determined	

Electrical Characteristics

Unless otherwise noted, limits in **BOLD** characters are electrical testing limits at V_{CC} = 0.5V and T_A = +25°C. All other limits are design goals for V_{CC} = 5.0V ±5% and T_A = 0°C to +70°C. All signals are referenced to GND. This data sheet is still preliminary and parameter limits are not indicative of characterization data with respect to power supply or temperature variations. Please contact your National Semiconductor Sales Office for the most current product information.

Symbol	Parameter	Conditions	Limits		Units
			Min	Max	
V_{IL}	Input Low Voltage	All Inputs		0.8	V
V_{IH}	Input High Voltage	All Inputs	2.0		V
V_{OL}	Output Low Voltage	CS0–7: I_{OL} = 1 mA SK, SO: I_{OL} = 4 mA AD(7:0): I_{OL} = 2 mA		**0.4**	V
V_{OH}	Output High Voltage	CS0–7: I_{OH} = 1 mA SK, SO: I_{OH} = 4 mA AD(7:0): I_{OH} = 2 mA	**2.4**		V
I_{IH}	High Level Input Current	All Inputs, GND < V_{IN} < V_{CC}		**−10**	μA
I_{IL}	Low Level Input Current	All Inputs		**+10**	μA
I_{OZ}	Output Current in High-Z	AD(7:0), SO		**±20**	μA
I_{CC}	Dynamic Supply Current	CKIN = SK = 1 MHz CKIN = SK = 20 MHz		0.7 4	mA

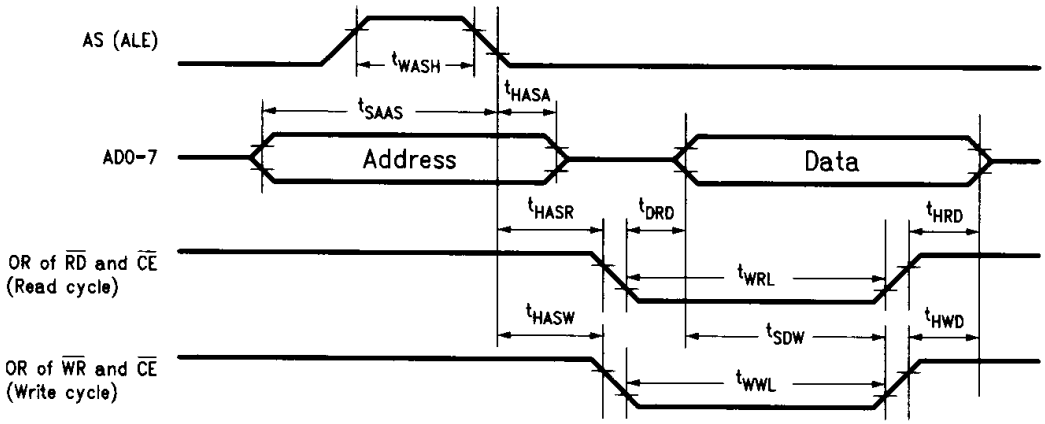
Timing Characteristics

This section contains timing diagrams for the microprocessor bus interface, MICROWIRE port interface and the Control and Clock timings relationships.

Timing characteristics are guaranteed from worst-case simulations plus guardbanding. Production testing is limited to device functionality.

NSC/Intel Bus Format

MULTIPLEXED MICROPROCESSOR BUS



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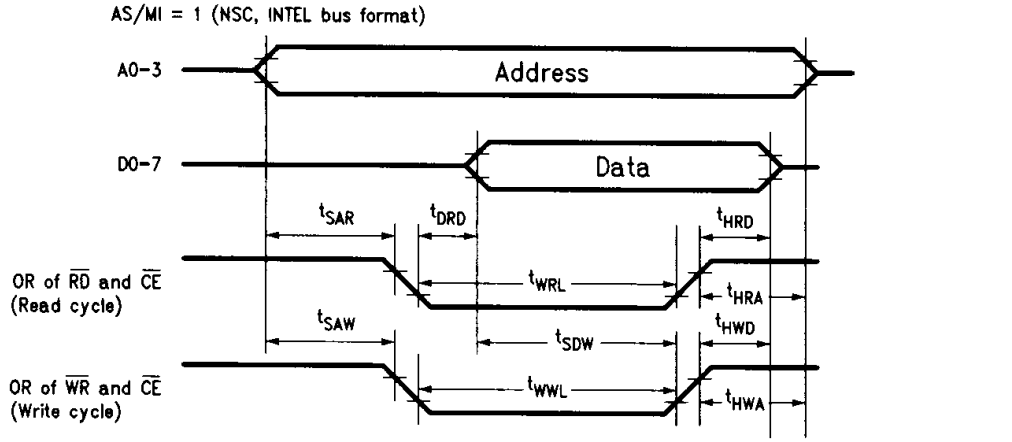
NON-MULTIPLEXED MICROPROCESSOR BUS



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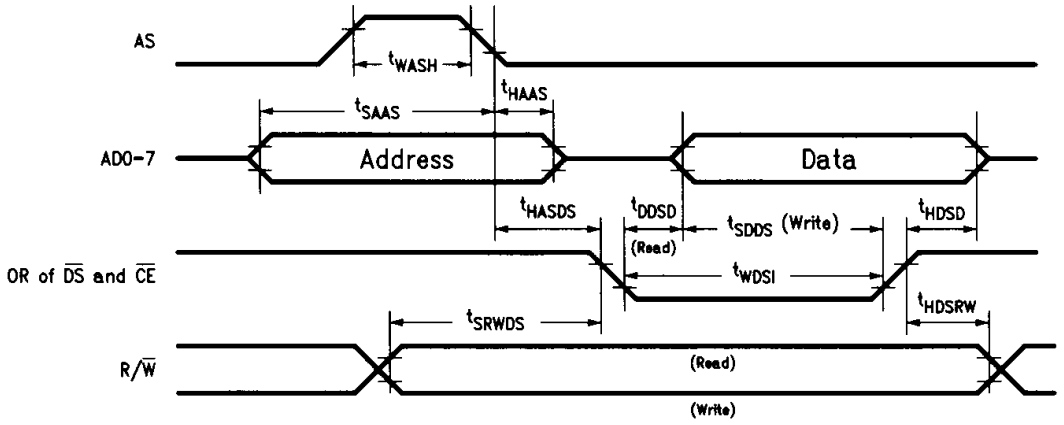
Symbol	Parameter	Conditions	Min	Max	Units
t_{WASH}	Width, Address Strobe High		20		ns
t_{SAAS}	Setup, Address to Address Strobe		10		ns
t_{HASA}	Hold, Address Strobe Low to Address		10		ns
t_{hASR}	Hold, Address Strobe to Read Strobe		10		ns
t_{DRD}	Delay, Read Low to Data	100 pF Load		70	ns
t_{HRD}	Hold, Read High to Data		5	40	ns
t_{WRL}	Width, Read Strobe Low		20		ns
t_{SDW}	Setup, Data to Write High		30		ns
t_{HWD}	Hold, Write High to Data		10		ns
t_{WWL}	Width, Write Strobe Low		20		ns
t_{SAR}	Setup, Address to Read Low	Non-Muxed, MI = 1	10		ns
t_{HRA}	Hold, Read High to Address	Non-Muxed, MI = 1	10		ns
t_{SAW}	Setup, Address to Write Low	Non-Muxed, MI = 1	10		ns
t_{HWA}	Hold, Write High to Address	Non-Muxed, MI = 1	10		ns

Motorola Bus Format

MULTIPLEXED MICROPROCESSOR BUS



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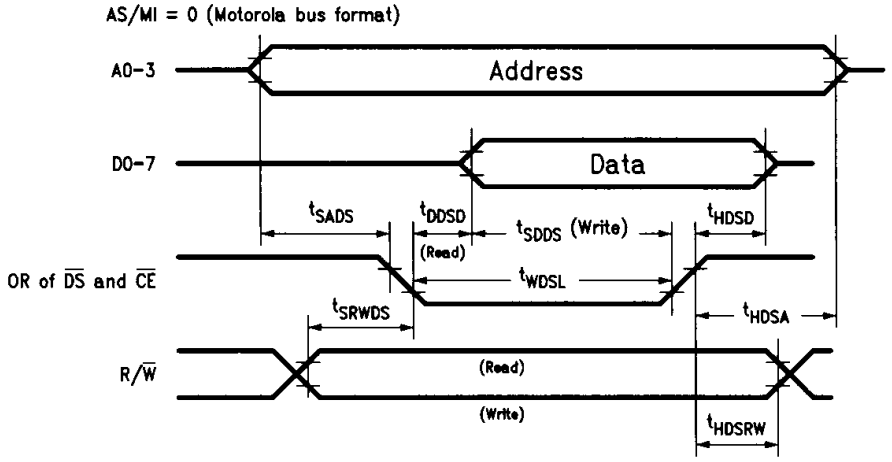
NON-MULTIPLEXED MICROPROCESSOR BUS



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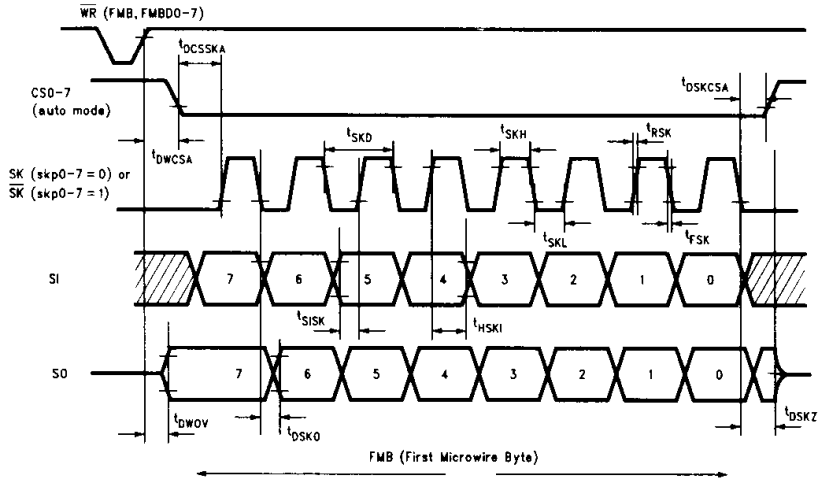
Symbol	Parameter	Conditions	Min	Max	Units
t_{WASH}	Width, Address Strobe High		20		ns
t_{SAAS}	Setup, Address to Address Strobe		10		ns
t_{HASA}	Hold, Address Strobe Low to Address		10		ns
t_{HASDS}	Hold, Address Strobe to Data Strobe		10		ns
t_{DDSD}	Delay, $\overline{\text{Data Strobe}}$ Low to Data (Read)	100 pF Load		70	ns
t_{HDSD}	Hold, $\overline{\text{Data Strobe}}$ High to Data		5	40	ns
t_{WDSL}	Width, $\overline{\text{Data Strobe}}$ Low		20		ns
t_{SDDS}	Setup, Data to $\overline{\text{Data Strobe}}$ High (Write)		30		ns
t_{SRWDS}	Setup, R/W Strobe to Data Strobe		10		ns
t_{HDSRW}	Hold, Data Strobe to R/W		10		ns
t_{SADS}	Setup, Address to $\overline{\text{Data Strobe}}$ Low	Non-Muxed, MI = 0	10		ns
t_{HDSA}	Hold, $\overline{\text{Data Strobe}}$ High to Address	Non-Muxed, MI = 0	10		ns

MICROWIRE Timing Diagrams

Symbol	Parameter	Conditions	Min	Max	Units
f_{CKIN}	CKin Frequency			20	MHz
f_{SK}	SK Frequency			5	MHz
t_{SKD}	SK Clock Duration		200		ns
t_{SKH}	SK High Duration		70		ns
t_{SKL}	SK Low Duration		70		ns
t_{RSK}	Rise Time, SK	100 pF Load		30	ns
t_{FSK}	Fall Time, SK	100 pF Load		30	ns
t_{SISK}	Setup Time, SI Valid to SK Edge		20		ns
t_{HSKI}	Hold Time, SK High to SI Invalid		20		ns
t_{DSKO}	Delay, SK Edge to SO Data Valid Output			20	ns
t_{DSKZ}	Delay, Last SK to SO TRI-STATE			30	ns
t_{DWOV}	Delay, WR to SO Valid	FMB or FMBD0–7		50	ns

MICROWIRE Timing for 1 Byte Transfer



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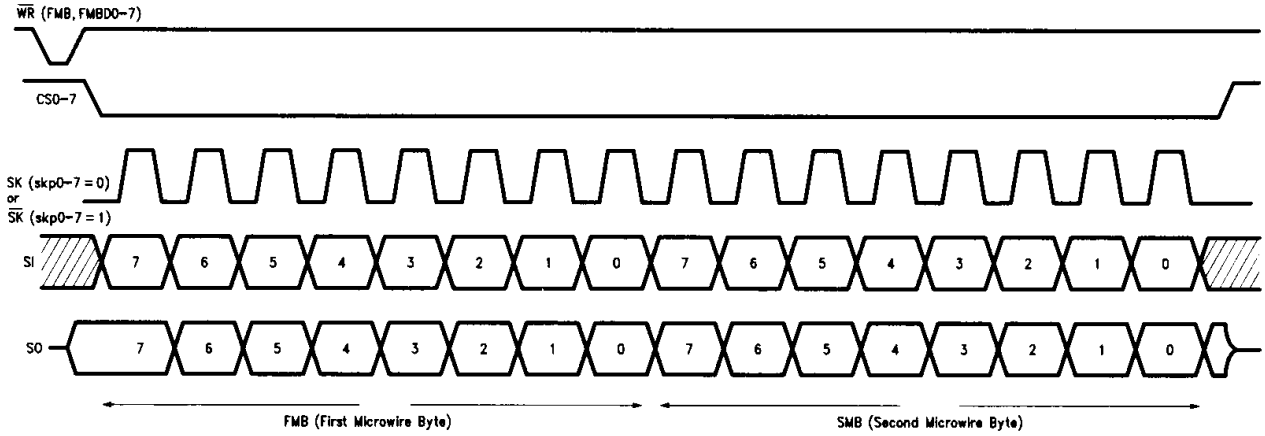
MICROWIRE Timing for 2 Byte Transfers



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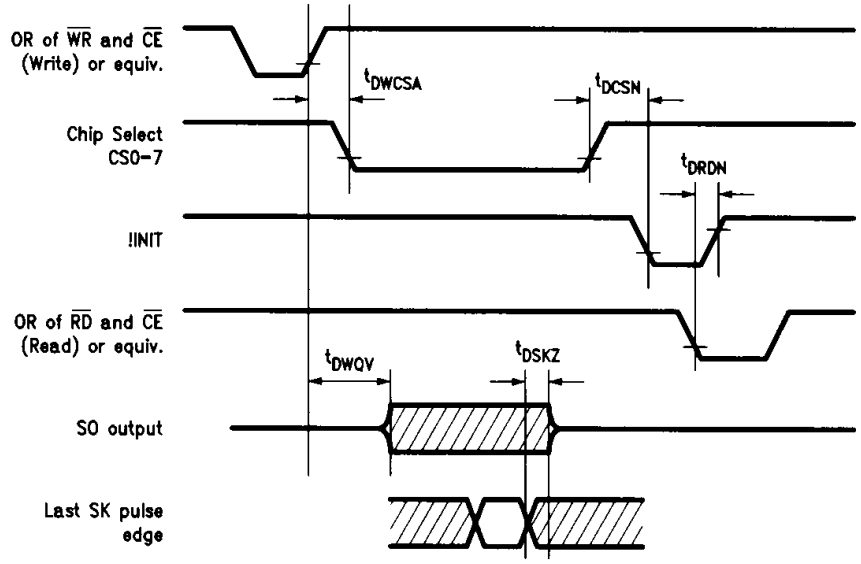
Control Interface Timing Relationships

Symbol	Parameter	Conditions	Min	Max	Units
t_{DWCSA}	Delay, Write Strobe to CS Asserted	Auto Mode		2	SK Cycle
t_{DCSSKA}	Delay, CS Active to first SK Edge	Auto Mode	0.5 SK − 50 ns	0.5 SK	ns
t_{DSKCSA}	Delay, Last SK Edge to CS Inactivate	Auto Mode	0.5 SK − 50 ns	0.5 SK	ns
t_{DWCSS}	Delay, Write Strobe (CS Register) to CS Asserted	Software		30	ns
t_{DCSN}	Delay, CS High to $\overline{INT}$ Low			50	ns
t_{DRDN}	Delay, $\overline{RD}$ Low to $\overline{INT}$ High	ST Register		80	ns



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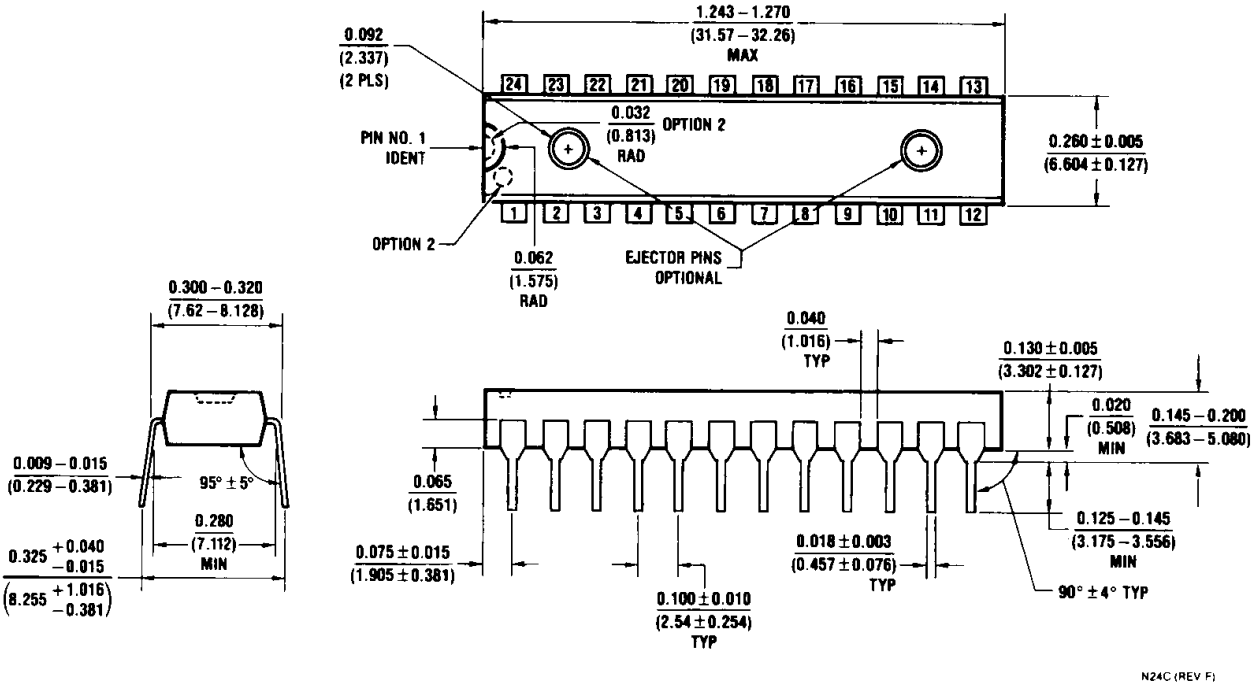
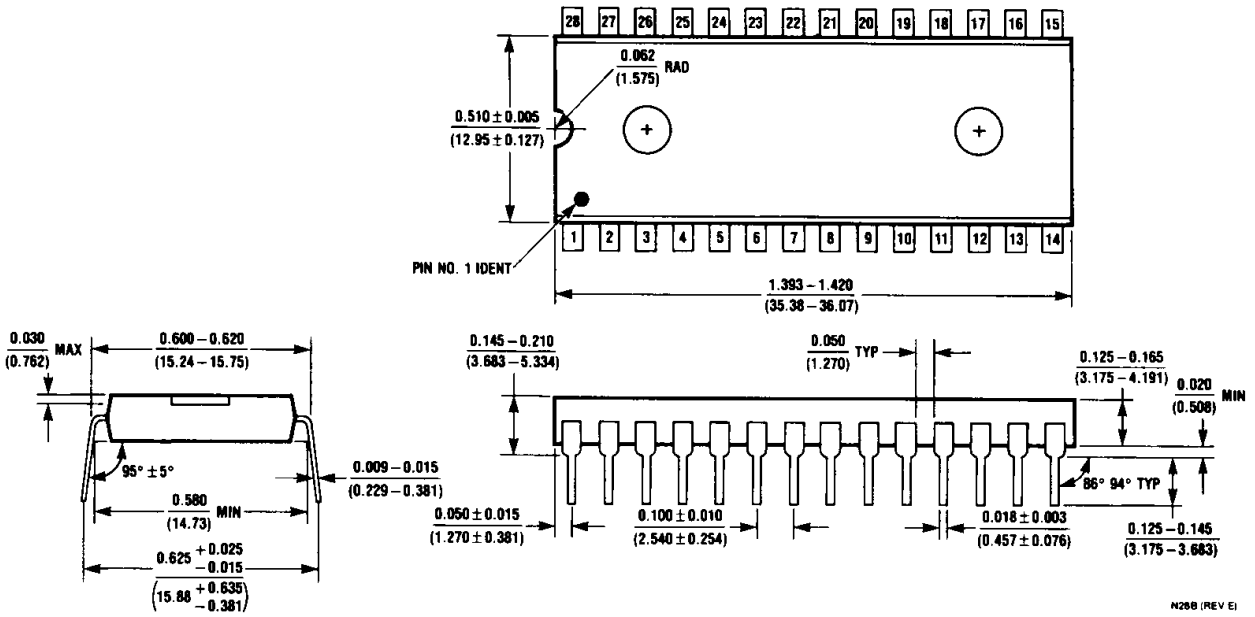
Physical Dimensions inches (millimeters)

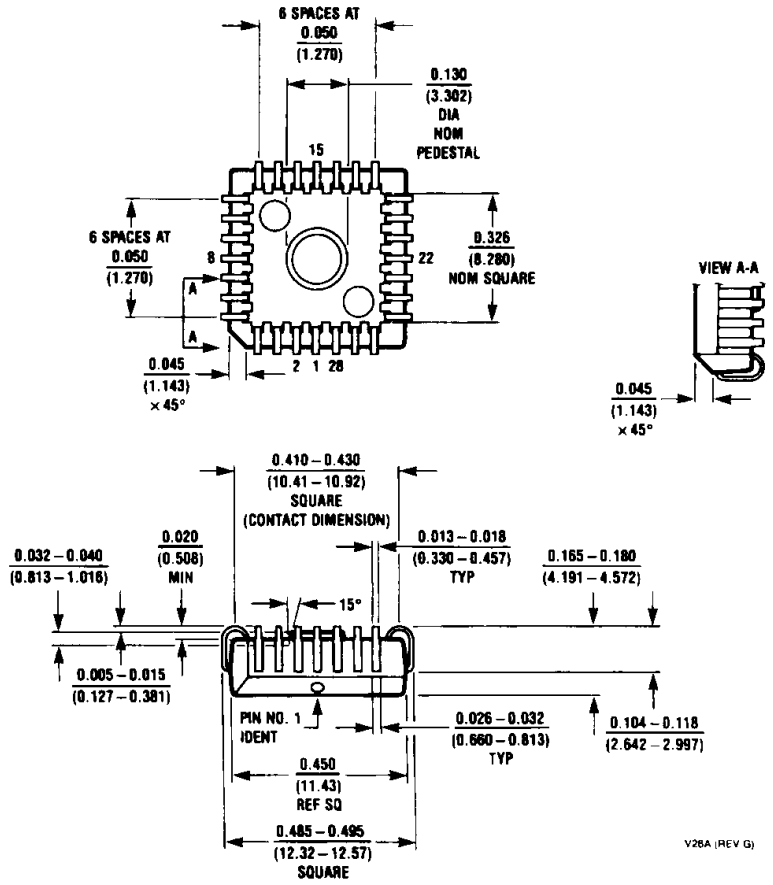


Molded Dual-In-Line Package (N)
Order Number TP3464N
NS Package Number N24C



Molded Dual-In-Line Package (N)
Order Number TP3465N
NS Package Number N28B

Physical Dimensions inches (millimeters) (Continued)



Plastic Chip Carrier (V)
Order Number TP3465V
NS Package Number V28A

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