Nordic VLSI ASA

315/433 MHz Single Chip RF Transceiver **nRF403**

FEATURES

- True single chip FSK transceiver
- Few external components required
- No set up or configuration
- No coding of data required
- 20kbit/s data rate
- 2 frequency bands
- Wide supply range
- Very low power consumption
- Standby mode

APPLICATIONS

- Alarm and Security Systems
- Automatic Meter Reading (AMR)
- Home Automation
- Remote Control
- Surveillance
- Automotive
- Telemetry
- Toys
- Wireless Communication

GENERAL DESCRIPTION

nRF403 is a true single chip UHF transceiver designed to operate in the 433MHz ISM (Industrial, Scientific and Medical) and 315 MHz frequency band. It features Frequency Shift Keying (FSK) modulation and demodulation capability. nRF403 operates at bit rates up to 20kbit/s. Transmit power can be adjusted to a maximum of 10dBm. Antenna interface is differential and suited for low cost PCB antennas. nRF403 features a standby mode which makes power saving easy and efficient. nRF403 operates from a single +3 V DC supply.
As a primary application, nRF403 is intended for UHF radio equipment in compliance with the European Telecommunication Standard Institute (ETSI) specification EN 300 220-1, the US Federal Communications Commission (FCC) standard CFR47 and Weak Power Radio in Japan.

QUICK REFERENCE DATA

Parameter	Value	Unit
Frequency bands	433.93 315.16	MHz
Modulation	FSK	
Frequency deviation	±15	kHz
Max. RF output power @ 400Ω, 3V	10	dBm
Sensitivity @ 400Ω, BR=20 kbit/s, BER<10^{-3}	-105	dBm
Maximum bit rate	20	kbit/s
Supply voltage	2.7 – 3.6	V
Receive supply current	250*	µA
Transmit supply current @ -10 dBm output power	8	mA
Standby supply current	8	µA

Table 1. nRF403 quick reference data**.**

ORDERING INFORMATION

Type number	Description	Version
nRF403-IC	20 pin SSOIC	A
nRF403-EVKIT	Evaluation kit (2 test PCB)	1.1

Table 2. nRF403 ordering information.

* The PWR_UP pin is used for power duty cycling. The duty-cycle is 2 % with a period of 200msec.

BLOCK DIAGRAM

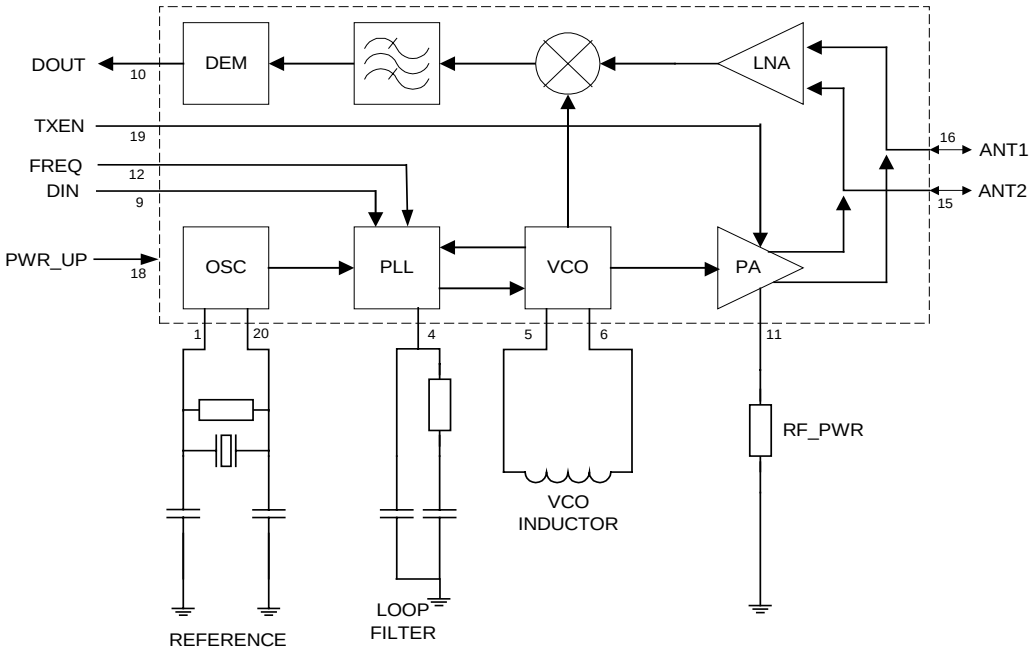


Figure 1. nRF403 block diagram with external components.

PIN FUNCTIONS

Pin	Name	Pin function	Description
1	XC1	Input	Crystal oscillator input
2	VDD	Power	Power supply (+3V DC)
3	VSS	Ground	Ground (0V)
4	FILT1	Input	Loop filter
5	VCO1	Input	External inductor for VCO
6	VCO2	Input	External inductor for VCO
7	VSS	Ground	Ground (0V)
8	VDD	Power	Power supply (+3V DC)
9	DIN	Input	Data input
10	DOUT	Output	Data output
11	RF_PWR	Input	Transmit power setting
12	FREQ	Input	Channel selection FREQ="0" ⇒ 433.93MHz FREQ="1" ⇒ 315.16MHz
13	VDD	Power	Power supply (+3V DC)
14	VSS	Ground	Ground (0V)
15	ANT2	Input/Output	Antenna terminal
16	ANT1	Input/Output	Antenna terminal
17	VSS	Ground	Ground (0V)
18	PWR_UP	Input	Power on/off PWR_UP = "1" ⇒ Power up (Operating mode) PWR_UP = "0" ⇒ Power down (Standby mode)
19	TXEN	Input	Transmit enable TXEN = "1" ⇒ Transmit mode TXEN = "0" ⇒ Receive mode
20	XC2	Output	Crystal oscillator output

Table 3. nRF403 pin functions.

ELECTRICAL SPECIFICATIONS

Conditions: VDD = +3V DC, VSS = 0V, T_A= -25°C to +85°C

Symbol	Parameter (condition)	Min.	Typ.	Max.	Units
VDD	Supply voltage	2.7	3	3.6	V
VSS	Ground		0		V
I_{DD}	Total current consumption Receive mode Transmit mode @ -10 dBm RF power Stand by mode		 11 8 8		 mA mA µA
P_{RF}	Max. RF output power @ 400Ω load		10		dBm
V_{IH}	Logic "1" input voltage	$0.7 \cdot V_{DD}$		V_{DD}	V
V_{IL}	Logic "0" input voltage	0		$0.3 \cdot V_{DD}$	V
V_{OH}	Logic "1" output voltage (I_{OH} = - 1.0mA)	$0.7 \cdot V_{DD}$		V_{DD}	V
V_{OL}	Logic "0" output voltage (I_{OL} = 1.0mA)	0		$0.3 \cdot V_{DD}$	V
I_H	Logic "1" input current (V_I = VDD)			+20	µA
I_L	Logic "0" input current (V_I = VSS)			-20	µA
f_1	433 MHz frequency band		433.93		MHz
f_2	315 MHz frequency band		315.16		MHz
	Dynamic range	90			dB
	Modulation type		FSK		
Δf	Frequency deviation		±15		kHz
f_{IF}	IF frequency		400		kHz
BW_{IF}	IF bandwidth	65		85	kHz
f_{XTAL}	Crystal frequency		4.0		MHz
	Crystal frequency stability requirement [1]			±45	ppm
	Loop filter voltage [3]	0.9	1.1	1.3	V
	Sensitivity @ 400Ω,BR=20 kbit/s, BER < 10^{-3}		-105		dBm
	Bit rate	0		20	kbit/s
Z_I	Recommended antenna port differential impedance		400		Ω
	Spurious emission	Compliant with EN 300-220-1 V1.2.1 [2]			

Table 4. nRF403 electrical specifications.

[1] Maximum 5dB sensitivity degradation at temperature extremes. See also page 11 Freq. difference.
[2] With a PCB loop antenna or a differential to single ended matching network to a 50Ω antenna.
[3] See also page 9, Loop filter.

ABSOLUTE MAXIMUM RATINGS

Supply voltages

VDD .....- 0.3V to +6V
VSS 0V

Input voltage

V_I.....- 0.3V to VDD + 0.3V

Output voltage

V_O.....- 0.3V to VDD + 0.3V

Power dissipation

P_D (T_A=25°C) 250mW

Temperatures

Operating Temperature…. -25°C to +85°C
Storage Temperature….. -40°C to +125°C

Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.

ATTENTION!
Electrostatic Sensitive Device
Observe Precaution for handling

PIN ASSIGNMENT

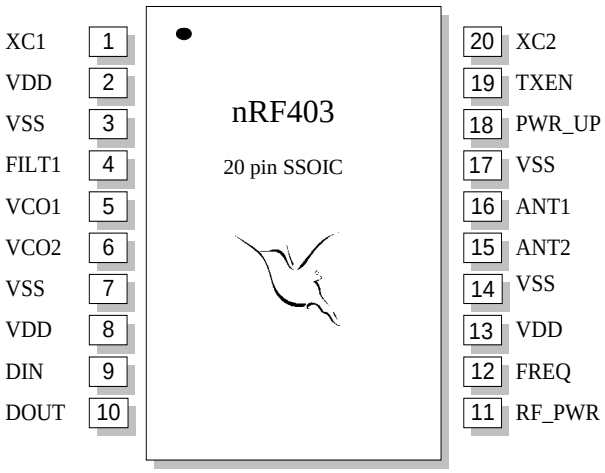
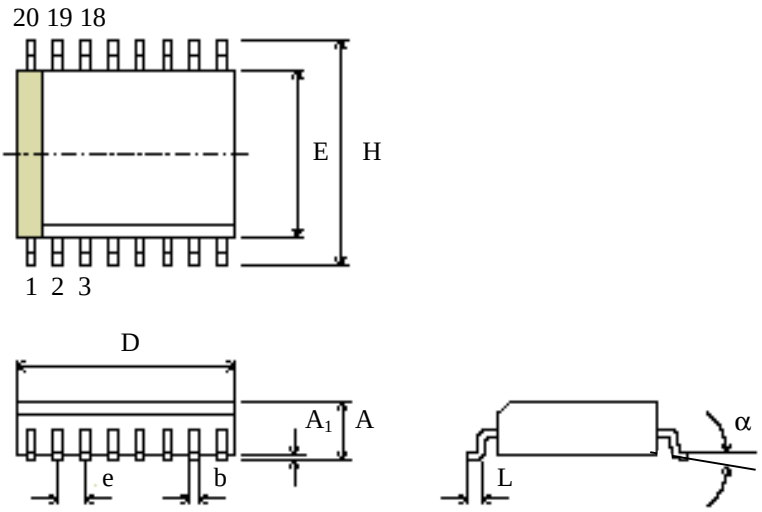


Figure 2. nRF403 pin assignment.

PACKAGE OUTLINE

nRF403, 20 pin SSOIC. (Dimensions in mm.)



Package Type		D	E	H	A	A_1	e	b	L	Copl.	α
20 pin SSOIC (Wide)	**Min**	6.90	5.00	7.40		0.05	0.65	0.22	0.55		0°
	Max	7.50	5.60	8.20	2.00			0.38	0.95	0.10	8°

Figure 3. SSOIC-20 Package outline.

IMPORTANT TIMING DATA

Timing information

The timing information for the different operations is summarised in Table 5.
(TX is transmit mode, RX is receive mode and Std.by is Standby mode.)

Change of Mode	Name	Max Delay	Condition
TX ➔ RX	t_{TR}	3ms	Operational mode
RX ➔ TX	t_{RT}	1ms	
Std.by➔ TX	t_{ST}	2ms	
Std.by➔ RX	t_{SR}	3ms	
V_{DD}=0 ➔ TX	t_{VT}	4ms	Start-up
V_{DD} =0 ➔ RX	t_{VR}	5ms	

Table 5 Switching times for nRF403.

Switching TX ↔ RX (operational mode).

When switching from RX-mode to TX-mode data (DIN) may not be sent before the TXEN-input has been high for at least 1ms, see Figure 4(a).
When switching from TX-mode to RX-mode the receiver may not receive data (DOUT) before the TXEN-input has been low for at least 3ms, see Figure 4(b).

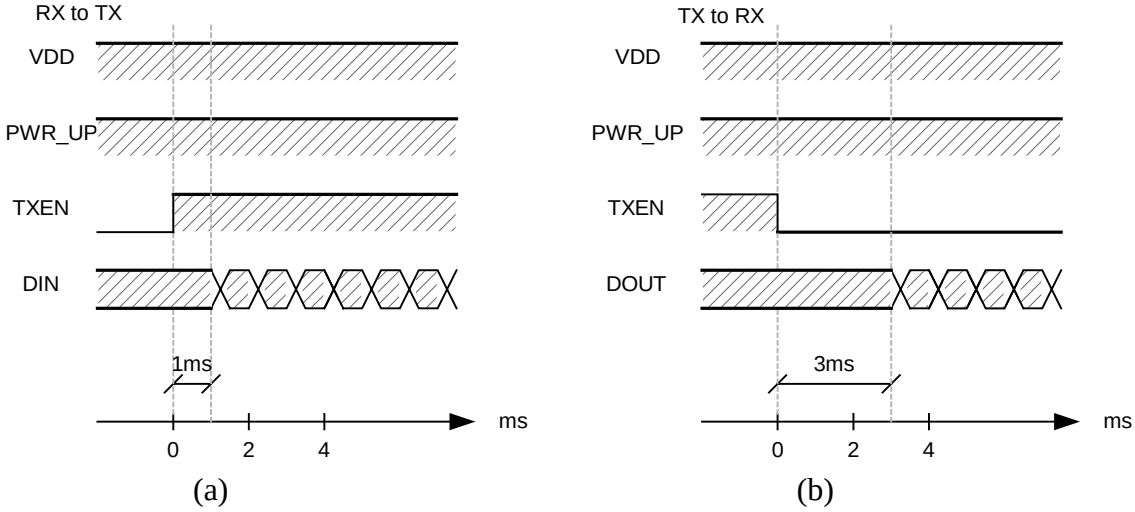


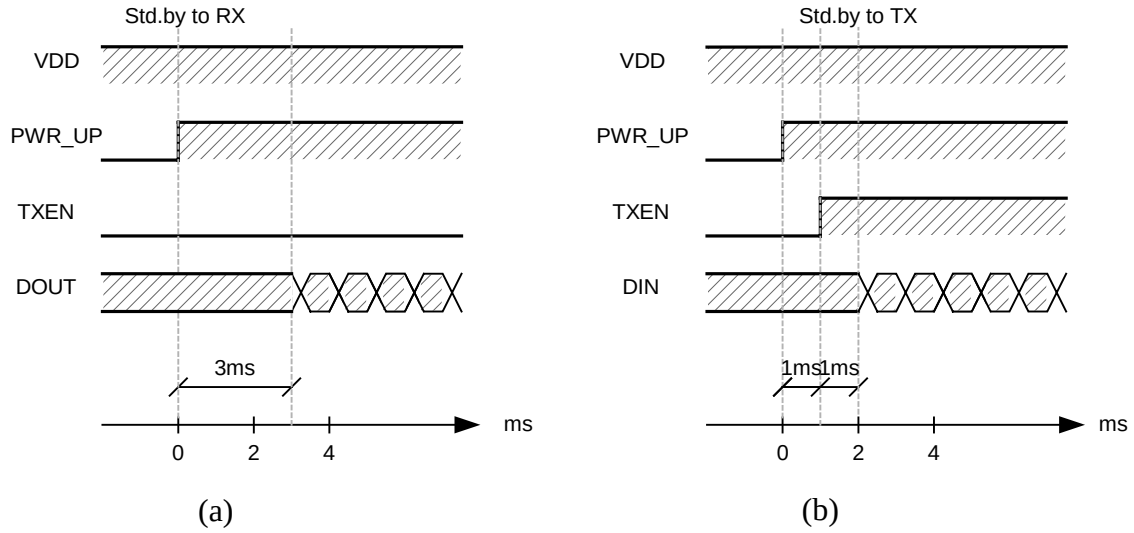
Figure 4. Timing diagram for nRF403for switching from RX to TX (a) and TX to RX (b).

Switching between standby and RX-mode (operational mode).

The time from the PWR_UP input is set to “1”, until the data (DOUT) is valid is $t_{SR,}$, see Table 5. Worst case t_{SR} is 3ms for nRF403 as can be seen in Figure 5 (a).

Switching between standby and TX-mode (operational mode).

The time from the PWR_UP input is set to “1”, until the synthesised frequency is stable is t_{ST}, see Table 5.

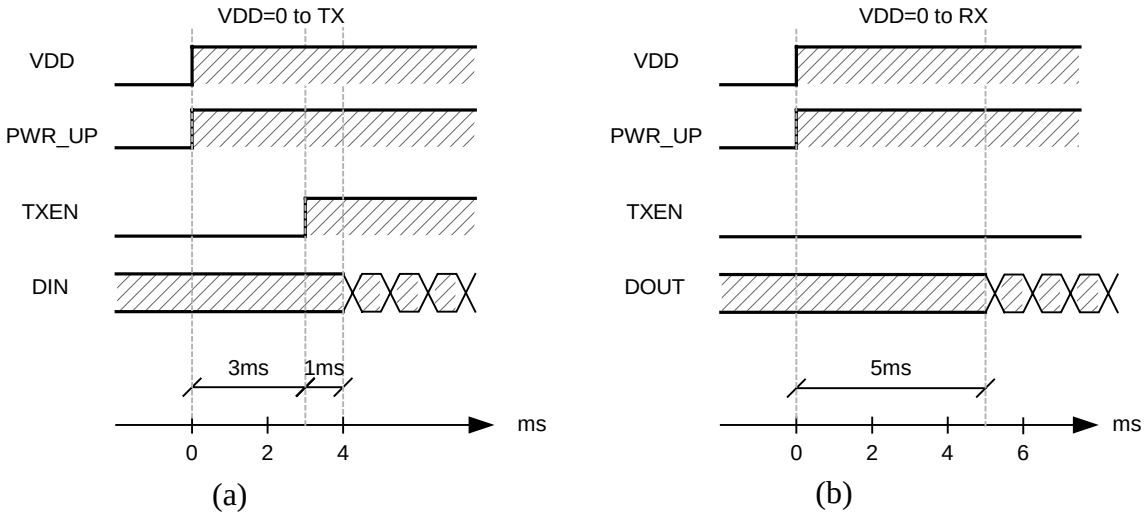


(a) (b)

Figure 5 Timing diagram for nRF403 when going from standby to RX-mode (a) or TX-mode (b).

Power up to transmit-mode (start-up).
To avoid spurious emission outside the ISM-band when the power supply is switched on, the TXEN-input must be kept low until the synthesised frequency is stable, see Figure 6 (a).

When enabling transmit-mode, TXEN-input should be high for at least 1 ms before data (DIN) is transmitted, see Figure 6 (a).



(a) (b)

Figure 6. Timing diagram for nRF403 when powering up to TX-mode (a) or RX-mode (b).

Power up to receive mode (start up).
In transition from power up to receive mode, the receiver may not receive data (DOUT) until VDD has been stable (VDD > 2.7 V) for at least 5ms, see Figure 6(b). If an external reference oscillator is used, the receiver may receive data (DOUT) after 3ms.

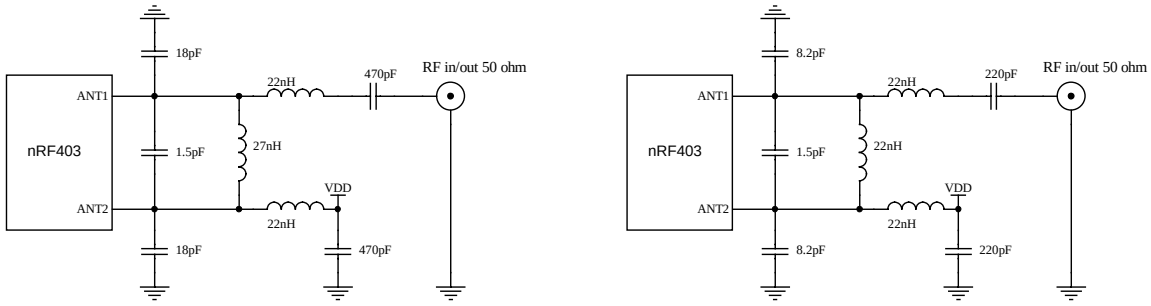
APPLICATION INFORMATION

Antenna input/output

The ANT1 and ANT2 pins provide RF input to the LNA (Low Noise Amplifier) when nRF403 is in receive mode, and RF output from the PA (Power Amplifier) when nRF403 is in transmit mode. The antenna connection to nRF403 is differential and the recommended load impedance at the antenna port is 400Ω.

Figure 14 shows a typical application schematic with a differential loop antenna on a Printed Circuit Board (PCB). The output stage (PA) consists of two open collector transistors in a differential pair configuration. VDD to the PA must be supplied through the collector load. When connecting a differential loop antenna to the ANT1/ANT2 pins, VDD should be supplied through the centre of the loop antenna as shown in Figure 14.

A 50Ω single ended antenna or 50Ω test instrument may be connected to nRF403 by using a differential to single ended matching network (BALUN) as shown in Figure 7, 433 MHz and 315 MHz operation.



a) 315MHz b) 433MHz

Figure 7. Connection of nRF403 to single ended antenna by using a differential to single ended matching network for 433 and 315 MHz.

The value of the capacitor connected between ANT1 and ANT2 is dependent on parasitics in the layout. 1.5 pF is the optimal value when using Nordic VLSI layout and 1.6 mm, 2 layer, FR4 printed circuit board, see application note AN400-05.

The 22 nH inductor to VDD in Figure 7, need to have a Self-Resonance Frequency (SRF) above 630/868 MHz to be effective. Suitable inductors are listed in Table 6.

Vendors	WWW address	Part. no., 22 nH inductors, 0603 size
Pulse	http://www.pulseeng.com	PE-0603CD220GTT
Coilcraft	http://www.coilcraft.com	0603CS-22NXGBC
muRata	http://www.murata.com	LQW1608A22NG00
Stetco	http://www.stetco.com	0603G220GTE
KOA	http://www.koaspeer.com	KQ0603TE22NG
Predan	http://www.predan.com	CS0603W-220G

Table 6. Vendors and part. no. for suitable 22 nH inductors.

A single ended antenna may also be connected to nRF403 using an 8:1 impedance RF transformer, both 315/433 MHz operation. The RF transformer must have a centre tap at the primary side for VDD supply.

RF output power

The external bias resistor R3 connected between the RF_PWR pin and VSS sets the output power. The RF output power may be set to levels up to +10dBm. In Figure 8 the output power is plotted for power levels down to, but not limited to, -8.5dBm for a differential load of 400Ω. DC power supply current versus external bias resistor value is shown in Figure 9.

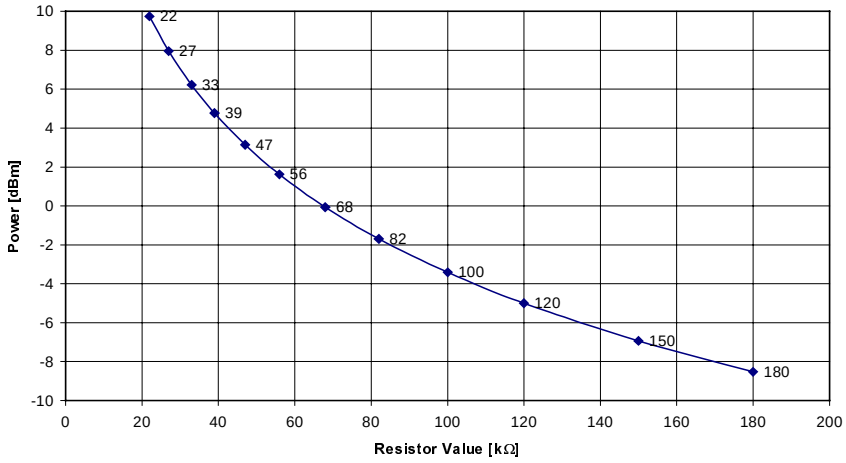


Figure 8. RF output power vs. external power setting resistor (R3) for nRF403.

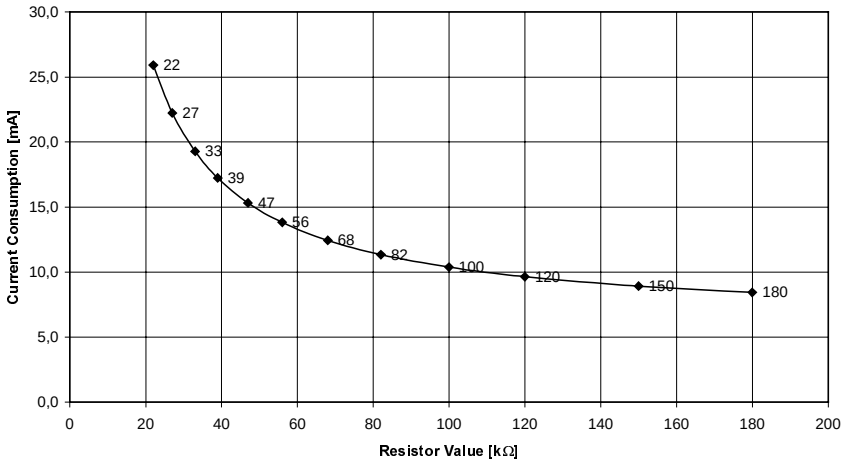


Figure 9. Total chip current consumption vs. external power setting resistor (R3) for nRF403.

Output power can be reduced below –8.5dBm by increasing the bias resistor R3 above 180 kΩ. The current consumption will be approx. 9 mA for also for R3 > 180 kΩ.

PLL loop filter

The synthesiser loop filter is an external, single-ended second order lag-lead filter. The recommended filter component values are: C3 = 820 pF, C4 =15 nF, and R2 = 4.7 kΩ, see Figure 12.

The loop filter voltage, measured at pin 4, should be 1.1 ± 0.2 V. Measuring the specified loop filter voltage verifies that the VCO inductor value and placement are correct. This means optimal nRF403 performance.

VCO inductor

An external 22nH (433 MHz operation) or 47nH (315 MHz operation) inductor connected between the VCO1 and VCO2 pins is required for the on-chip voltage controlled oscillator (VCO). This inductor must be a high quality chip inductor, Q > 45 @ 433 MHz or 315 MHz, with a maximum tolerance of ± 2%. The following 22 nH and 47nH inductors (0603) are suitable for use with nRF403.

Vendors	**WWW address**	**Part. no., 22 nH inductors, 0603**	**Part. no., 47 nH inductors, 0603**
Pulse	http://www.pulseeng.com	PE-0603CD220GTT	PE-0603CD470GTT
Coilcraft	http://www.coilcraft.com	0603CS-22NXGBC	0603CS-47NXGBC
muRata	http://www.murata.com	LQW1608A22NG00	LQW1608A47NG00
Stetco	http://www.stetco.com	0603G220GTE	0603G470GTE
KOA	http://www.koaspeer.com	KQ0603TE22NG	KQ0603TE47NG
Predan	http://www.predan.com	CS0603W-220G	CS0603W-470G

Table 7. Vendors and part no. for suitable 22nH and 47nH inductors.

The VCO inductor placement is important. The optimum placement of the VCO inductor gives a PLL loop filter voltage of 1.1 ±0.2 V, which can be measured at FILT1 (pin4). For a 0603 size inductor, the length between the centre of the VCO1/VCO2 pad and the centre of the inductor pad should be 5.4 mm,
see Figure 13 (c) (layout, top view), for a 2 layer, 1.6 mm thick FR4 PCB.

Crystal specification

To achieve an active crystal oscillator (XOSC) with low power consumption, certain requirements apply for crystal loss and capacitive load.

The crystal specification is:

$f = 4.0000\ MHz$	Crystal parallel resonant frequency
$Co \le 7\ pF$	Crystal parallel equivalent capacitance
$ESR \le 150\ ohm$.	Crystal equivalent series resistance
$C_L \le 14\ pF$	Total crystal load capacitance, including capacitance in PCB layout.

For the crystal oscillator shown in Figure 10 the load capacitance is given by:

$$C_L = \frac{C1' \cdot C2'}{C1' + C2'},$$ Where C1´ = C1 + C_{PCB1} and C2´ = C2 + C_{PCB2}

C1 and C2 are 0603 SMD capacitors as shown in the application schematic, see Figure 12, Table 9 for 315 MHz operation and Figure 14, Table 10 for 433 MHz operation. C_{PCB1} and C_{PCB2} are the layout parasitic capacitance on the circuit board. Layout parasitics are significant when using SMD crystals on PCBs with ground planes. Changes in C_L leads to changes in crystal frequency.

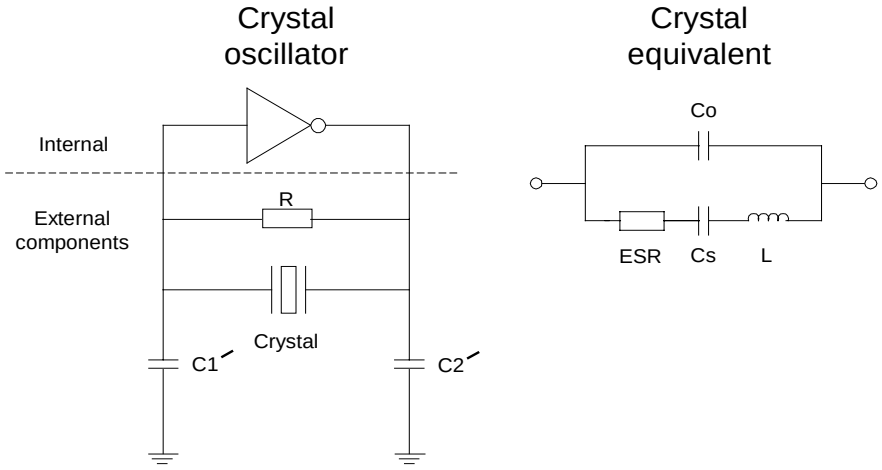


Figure 10. Crystal oscillator and crystal equivalent.

Sharing a reference crystal with a micro-controller

Figure 11 shows circuit diagram of a typical application where nRF403 and a micro controller share the reference crystal.

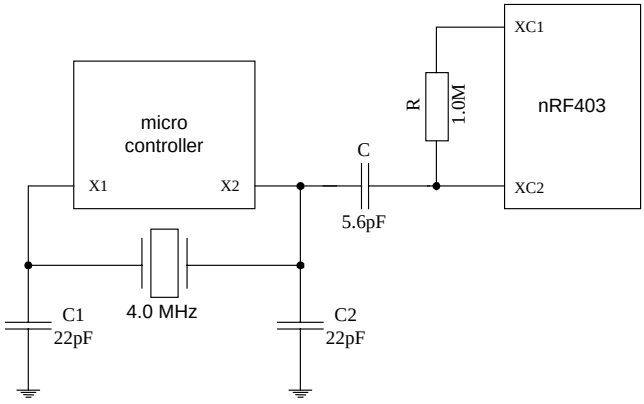


Figure 11. nRF403 and a micro-controller sharing the reference crystal.

The crystal reference line from the micro-controller must be shielded from noise, e.g. not be routed close to full swing digital data or control signals.

When sharing crystal, frequency (f) and frequency tolerance of the crystal is set by nRF403 specifications. C_L, C_0 and ESR are set by the microcontroller (MCU) specifications. The voltage amplitude at XC2 should be > 300 mV_{PP}. Changing the value of C, see figure 11, changes the XC2 voltage amplitude.

Frequency difference between transmitter and receiver

For optimum performance, the total frequency difference between transmitter and receiver should not exceed 70 ppm (30 kHz). This yields a crystal stability requirement of ±35 ppm for the transmitter and receiver. Frequency difference exceeding this will result in a -12dB/octave drop in receiver sensitivity. The functional frequency window of the transmission link is typically 450 ppm (200 kHz).

Example: A crystal with ±20 ppm frequency tolerance and ±25 ppm frequency stability over the operating temperature has a worst case frequency difference of ±45 ppm. If the transmitter and receiver operate in different temperature environments, the resulting worst-case frequency difference may be as high as 90 ppm. Resulting drop in sensitivity due to the extra 20 ppm, is then approx. 5dB.

Transmit/receive mode selection

TXEN is a digital input for selection of transmit or receive mode.
TXEN = "1" selects transmit mode.
TXEN = "0" selects receive mode.

Frequency band (315/433 MHz) selection

FREQ is a digital input for selection of either 433MHz or 315MHz frequency band operation.
FREQ = "0" selects 433.93 MHz.
FREQ = "1" selects 315.16 MHz.

Power up

PWR_UP is a digital input for selection of normal operating mode or standby mode.
PWR_UP = "1" selects normal operating mode.
PWR_UP = "0" selects standby mode.

Input			Response	
TXEN	**FREQ**	**PWR_UP**	**Frequency**	**Mode**
0	0	1	433 MHz	RX
0	1	1	315 MHz	RX
1	0	1	433 MHz	TX
1	1	1	315 MHz	TX
X	X	0	--	Standby

Table 8. Required setting for standby and frequency band selection in RX and TX.

D_{IN} (data input) and D_{OUT} (data output)

The DIN pin is the input to the digital modulator of the transmitter. The input signal to this pin should be standard CMOS logic level at data rates up to 20 kbit/s. No coding of data is required.

DIN = "1" $\rightarrow f = f_0 + \Delta f$
DIN = "0" $\rightarrow f = f_0 - \Delta f$

The demodulated digital output data appear at the D_{OUT} pin at standard CMOS logic levels.

$f_0 + \Delta f \rightarrow$ DOUT="1",
$f_0 - \Delta f \rightarrow$ DOUT="0".

PCB layout and decoupling guidelines
A well-designed PCB is necessary to achieve good RF performance. A PCB with a minimum of two layers including a ground plane is recommended for optimum performance.

The nRF403 DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors, see Table 9 and 10. It is preferable to mount a large surface mount capacitor (e.g. 4.7 µF tantalum) in parallel with the smaller value capacitors. The nRF403 supply voltage should be filtered and routed separately from the supply voltages of any digital circuitry (star routed).

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections and VDD bypass capacitors must be connected as close as possible to the nRF403 IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have via holes as close as possible to the VSS pads.

Full swing digital data or control signals should not be routed close to the PLL loop filter components or the external VCO inductor.

The VCO inductor placement is important. The optimum placement of the VCO inductor gives a PLL loop filter voltage of 1.1 ±0.2 V, which can be measured at FILT1 (pin4). For a 0603 size inductor the length between the centre of the VCO1/VCO2 pad and the centre of the inductor pad should be 5.4 mm,
see Figure 13 (c) (layout, top view), for a 2 layer, 1.6 mm thick FR4 PCB.

PCB layout example
Figure 13 shows a PCB layout example for the application schematic in Figure 12, 315.16 MHz operation. A double-sided FR-4 board of 1.6mm thickness is used. This PCB has a ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. A large number of via holes connect the top layer ground areas to the bottom layer ground plane.

Figure 15 shows a PCB layout example for the application schematic in Figure 14, 433 MHz operation. Please note that there must **NOT** be a ground plane shielding the radiation from the antenna.

For more layout information, please refer to application note nAN400-05, "nRF401 RF and antenna layout".

APPLICATION SCHEMATIC, 315 MHz

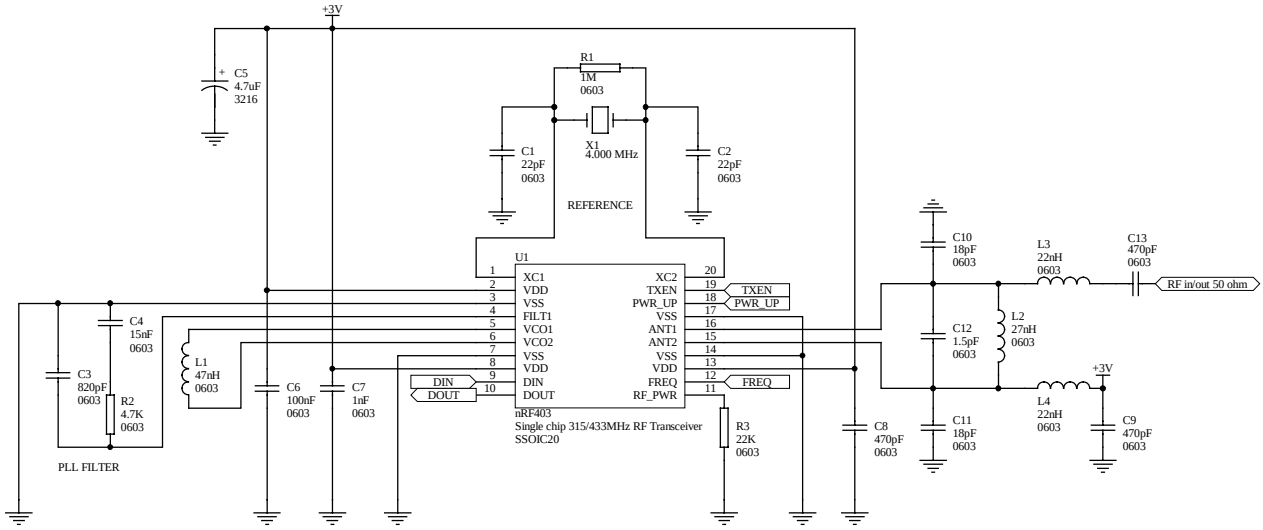
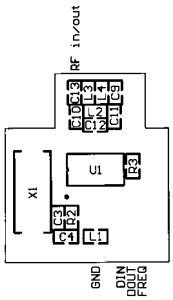


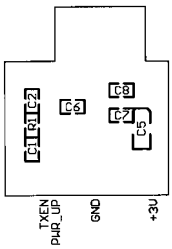
Figure 12. nRF403 application schematic (315 MHz).

Component	Description	Size	Value	Tolerance	Units
C1	NP0 ceramic chip capacitor, (Crystal oscillator)	0603	22		pF
C2	NP0 ceramic chip capacitor, (Crystal oscillator)	0603	22		pF
C3	X7R ceramic chip capacitor, (PLL loop filter)	0603	820		pF
C4	X7R ceramic chip capacitor, (PLL loop filter)	0603	15		nF
C5	Tantalum chip capacitor, (Supply decoupling)	3216	4.7		µF
C6	X7R ceramic chip capacitor, (Supply decoupling)	0603	100		nF
C7	X7R ceramic chip capacitor, (Supply decoupling)	0603	1		nF
C8	NP0 ceramic chip capacitor, (Supply decoupling)	0603	470		pF
C9	NP0 ceramic chip capacitor, (Supply decoupling)	0603	470		pF
C10	NP0 ceramic chip capacitor, (Impedance matching)	0603	18	±1%	pF
C11	NP0 ceramic chip capacitor, (Impedance matching)	0603	18	±1%	pF
C12	NP0 ceramic chip capacitor, (Impedance matching)	0603	1.5	±0.1	pF
C13	NP0 ceramic chip capacitor, (Impedance matching)	0603	470		pF
L1	VCO inductor, Q>45 @ 315 MHz	0603	47	±2%	nH
L2	Chip inductor, SRF>630 MHz (Impedance matching)	0603	27	±2%	nH
L3	Chip inductor, SRF>630 MHz (Impedance matching)	0603	22	±2%	nH
L4	Chip inductor, SRF>630 MHz (Impedance matching)	0603	22	±2%	nH
R1	0.1W chip resistor, (Crystal oscillator)	0603	1.0		MΩ
R2	0.1W chip resistor, (PLL loop filter)	0603	4.7		kΩ
R3	0.1W chip resistor, (Transmitter power setting)	0603	22		kΩ
X1	Crystal	-	4.000		MHz

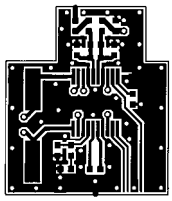
Table 9. External Component Specification (315 MHz).



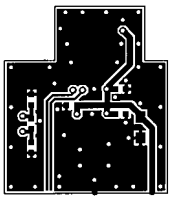
a) Top silk screen



b) Bottom silk screen



c) Top view



d) Bottom view

Figure 15. PCB layout (example) for nRF403 with single ended connection to 50Ω antenna by using a differential to single ended matching network (315 MHz).

APPLICATION SCHEMATIC, 433 MHz

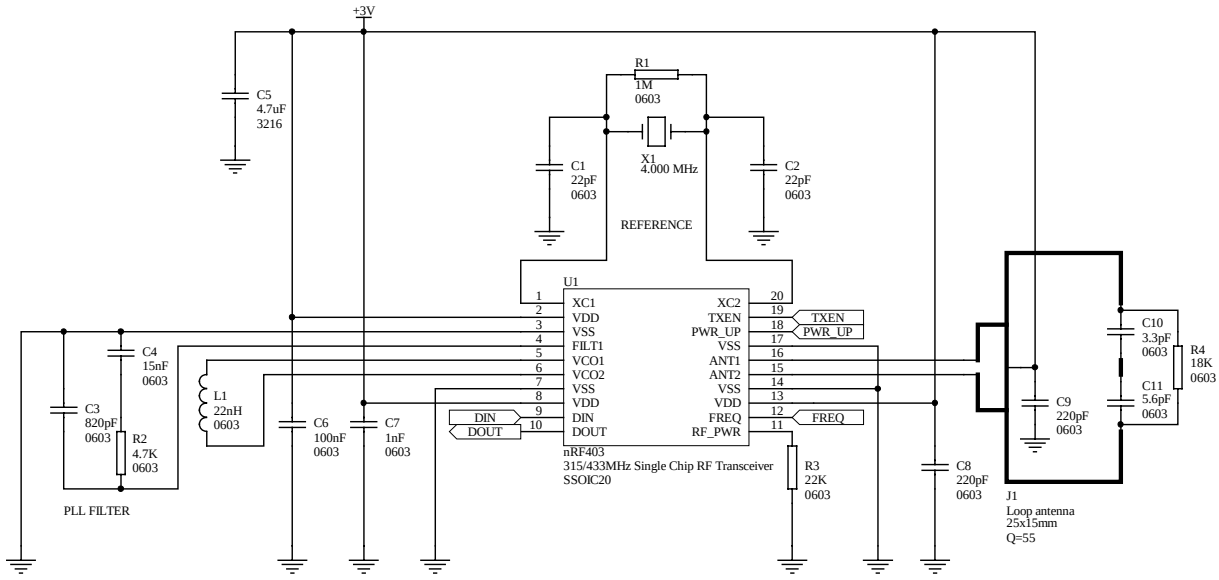


Figure 14. nRF403 application schematic (433 MHz).

Component	Description	Size	Value	Tolerance	Units
C1	NP0 ceramic chip capacitor, (Crystal oscillator)	0603	22		pF
C2	NP0 ceramic chip capacitor, (Crystal oscillator)	0603	22		pF
C3	X7R ceramic chip capacitor, (PLL loop filter)	0603	820		pF
C4	X7R ceramic chip capacitor, (PLL loop filter)	0603	15		nF
C5	Tantalum chip capacitor, (Supply decoupling)	3216	4.7		µF
C6	X7R ceramic chip capacitor, (Supply decoupling)	0603	100		nF
C7	X7R ceramic chip capacitor, (Supply decoupling)	0603	1		nF
C8	NP0 ceramic chip capacitor, (Supply decoupling)	0603	220		pF
C9	NP0 ceramic chip capacitor, (Supply decoupling)	0603	220		pF
C10	NP0 ceramic chip capacitor, (Antenna tuning)	0603	3.3	±0.1	pF
C11	NP0 ceramic chip capacitor, (Antenna tuning)	0603	5.6	±0.1	pF
L1	VCO inductor, Q>45 @ 433 MHz	0603	22	±2%	nH
R1	0.1W chip resistor, (Crystal oscillator)	0603	1.0		MΩ
R2	0.1W chip resistor, (PLL loop filter)	0603	4.7		kΩ
R3	0.1W chip resistor, (Transmitter power setting)	0603	22		kΩ
R4	0.1W chip resistor, (Antenna Q reduction)	0603	18		kΩ
X1	Crystal	-	4.000		MHz

Table 10. External Component Specification (433 MHz).

a) Top silk screen

b) Bottom silk screen

c) Top view

d) Bottom view

Figure 15. PCB layout (example) for nRF403 with loop antenna (433 MHz).

DEFINITIONS

Data sheet status	
Objective product specification	This datasheet contains target specifications for product development.
Preliminary product specification	This datasheet contains preliminary data; supplementary data may be published from Nordic VLSI ASA later.
Product specification	This datasheet contains final product specifications. Nordic VLSI ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 11. Definitions**.**

Nordic VLSI ASA reserves the right to make changes without further notice to the product to improve reliability, function or design. Nordic VLSI does not assume any liability arising out of the application or use of any product or circuits described herein.

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Product specification: Revision Date: 08.11.2002.

Datasheet order code: 081102nRF403

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