

# MSM63P180

## 4-Bit Microcontroller with Built-in 16K Word PROM and 1024-Dot Matrix LCD Drivers

### GENERAL DESCRIPTION

The MSM63P180 is an M6318x series one-time-programmable ROM version product of OLMS-63K family, which employs Oki's original CPU core nX-4/250.

The MSM63P180 has one-time PROM as internal program memory.

The MSM63188 and other mask ROM-version products have mask ROM as internal program memory.

The specifications of the MSM63P180 are equal to those of the MSM63188 except for electrical characteristics, packaging, and some functions.

The MSM63P180 is used for evaluating the software development of M6318x series products.

### FEATURES

- Rich instruction set  
439 instructions  
Transfer, rotate, increment/decrement, arithmetic operations, comparison, logic operations, mask operations, bit operations, ROM table reference, external memory transfer, stack operations, flag operations, branch, conditional branch, call/return, control.
- Rich selection of addressing modes  
Indirect addressing of four data memory types, with current bank register, extra bank register, HL register and XY register.  
Data memory bank internal direct addressing mode.
- Processing speed  
Two clocks per machine cycle, with most instructions executed in one machine cycle.  
Minimum instruction execution time : 61  $\mu$ s (@ 32.768 kHz system clock)  
1  $\mu$ s (@ 2 MHz system clock)
- Clock generation circuit  
Low-speed clock : 32.768 kHz crystal oscillator  
High-speed clock : 2 MHz (Max.) RC or ceramic oscillator select
- Program memory space  
16K words (PROM)  
Basic instruction length is 16 bits/1 word
- Data memory space  
3584 nibbles
- External data memory space  
64 Kbytes (expandable by using an I/O port)

- Stack level
  - Call stack level : 16 levels
  - Register stack level : 16 levels
- I/O ports
  - Input ports: Selectable as input with pull-up resistance/input with pull-down resistance/high-impedance input
  - Output ports: Selectable as P-channel open drain output/N-channel open drain output/CMOS output
  - Input-output ports: Selectable as input with pull-up resistance/input with pull-down resistance/high-impedance input  
Selectable as P-channel open drain output/N-channel open drain output/CMOS output
  - Can be interfaced with external peripherals that use a different power supply than this device uses.
  - Number of ports:
    - Input port : 2 ports × 4 bits
    - Output port : 6 ports × 4 bits
    - Input-output port : 8 ports × 4 bits
- Buzzer function
  - Buzzer output : 0.946 to 5.461 kHz (adjustable in 15 steps)
  - Buzzer output modes : Intermittent sound 1, 2; simple sound; continuous sound
- Melody output function
  - Melody sound frequency : 529 to 2979 Hz
  - Tone length : 63 types
  - Tempo : 15 types
  - Note data : Resides in the program memory
- LCD driver
  - Number of segments : 1024 Max. (64 SEG × 16 COM)
  - 1/1 to 1/16 duty
  - 1/4 or 1/5 bias (regulator built-in)
  - Selectable as all-on mode/all-off mode/power down mode/normal display mode
  - Adjustable contrast
- Multiplier/divider circuits
  - Multiplier : (8 bits) × (8 bits) → Product (16 bits)
  - Divider : (16 bits) ÷ (8 bits) → Quotient (16 bits), Remainder (8 bits)
- Reset function
  - Reset through RESET pin
  - Power-on reset
  - Reset by low-speed oscillation halt
- Battery check
  - Low-voltage supply check
  - Criterion voltage : Selectable as 2.2 V or 2.8 V

- Power supply backup  
Backup circuit (voltage multiplier) enables operation at 1.45 V minimum
- Timers and counter
  - 8-bit timer × 4  
Selectable as auto-reload mode/capture mode/clock frequency measurement mode
  - Watchdog timer × 1  
Overflows in 2 sec.
  - 100 Hz timer × 1  
Measurable in steps of 1/100 sec.
  - 15-bit time base counter × 1  
1, 2, 4, 8, 16, 32, 64, and 128 Hz signals can be read
- Time base capture function  
Captures the time base counter output values (32, 64, 128, and 256 Hz) upon the rise (fall) of P1.0 and P1.1
- Serial port
 

|                                     |                                                              |
|-------------------------------------|--------------------------------------------------------------|
| Mode                                | : UART mode, synchronous mode                                |
| UART communication speed            | : 1200 bps, 2400 bps, 4800 bps, 9600 bps                     |
| Clock frequency in synchronous mode | : 32.768 kHz (internal clock mode), external clock frequency |
| Data length                         | : 5 to 8 bits                                                |
- Shift register
 

|             |                                                             |
|-------------|-------------------------------------------------------------|
| Shift clock | : 1x or 1/2x system clock, timer 1 overflow, external clock |
| Data length | : 8 bits                                                    |
- Interrupt sources
 

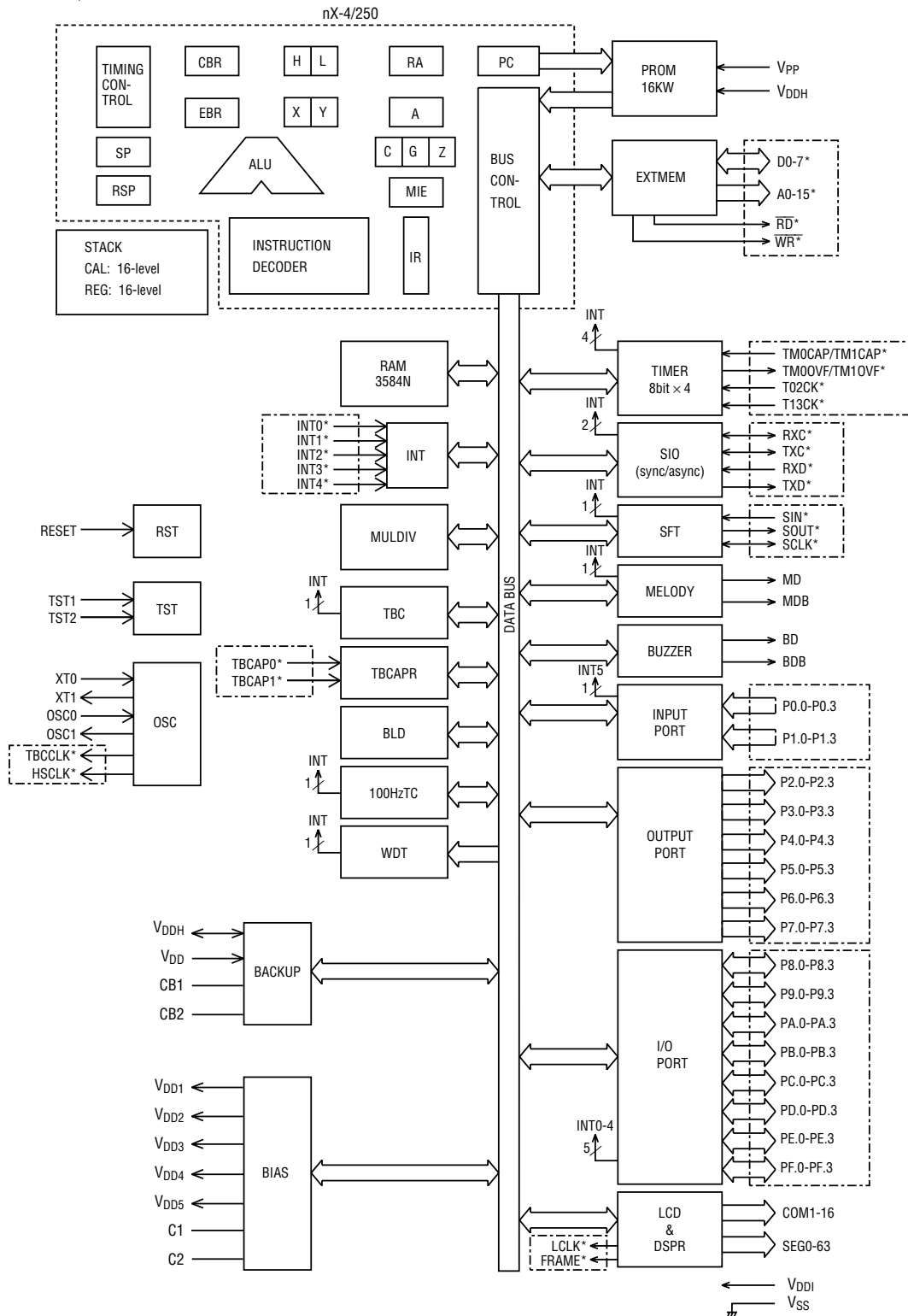
|                    |                                                            |
|--------------------|------------------------------------------------------------|
| External interrupt | : 6                                                        |
| Internal interrupt | : 14 (watchdog timer interrupt is a nonmaskable interrupt) |
- Operating voltage
 

|                      |                            |
|----------------------|----------------------------|
| When backup used     | : $V_{DD} = 1.45$ to 2.7 V |
| When backup not used | : $V_{DD} = 2.7$ to 5.5 V  |
- Package:
 

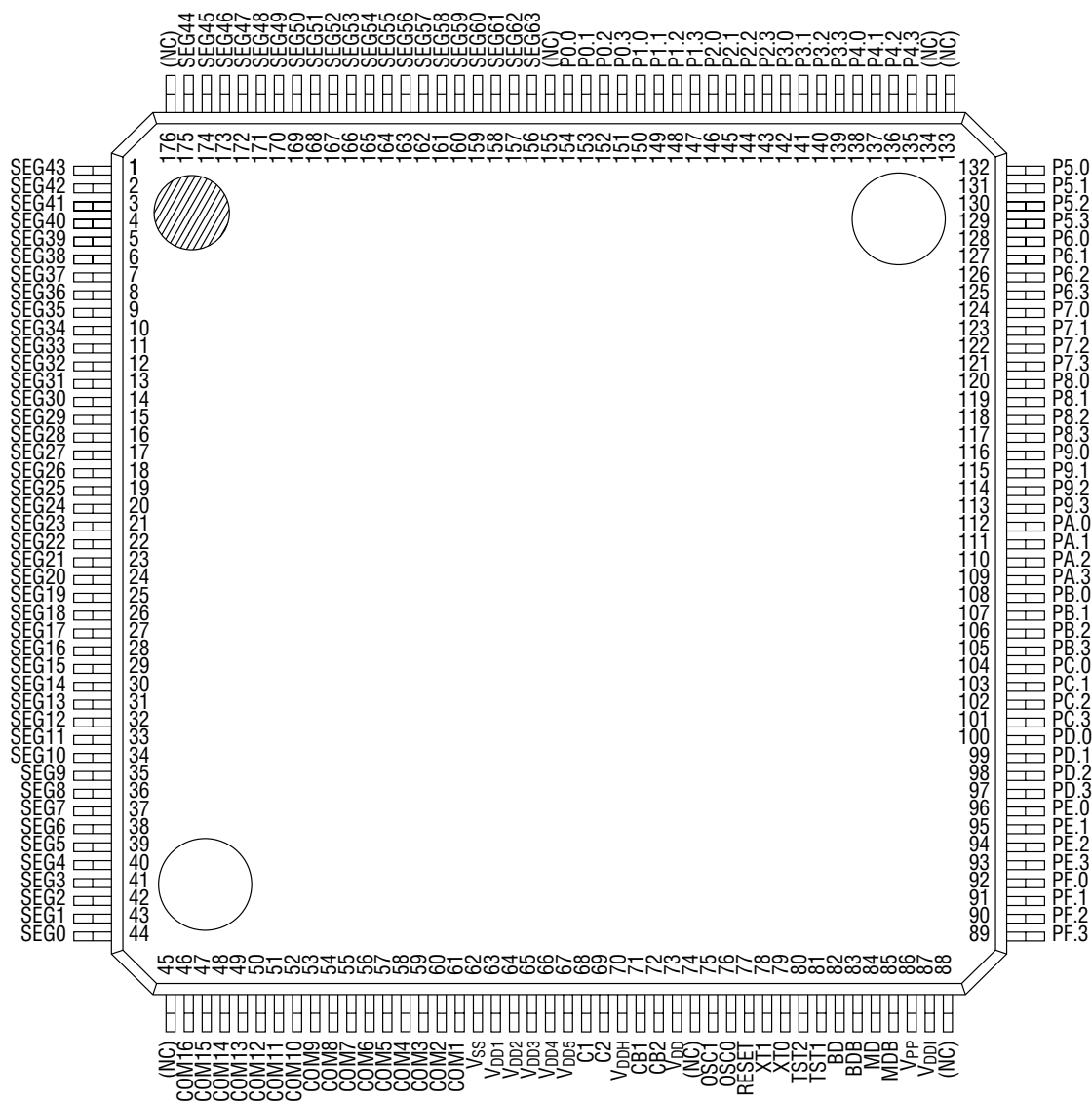
|                                               |                                                                                                        |
|-----------------------------------------------|--------------------------------------------------------------------------------------------------------|
| 176-pin plastic LQFP (LQFP176-P-2424-0.50-BK) |                                                                                                        |
| Product name                                  | : MSM63P180-xxxGS-BK (written PROM)<br>MSM63P180-NGS-BK (blanked PROM)<br>xxx indicates a code number. |

## BLOCK DIAGRAM

An asterisk (\*) indicates the port secondary function.  indicates that the power is supplied to the circuits corresponding to the signal names inside  from V<sub>DDI</sub> (power supply for interface).



## PIN CONFIGURATION (TOP VIEW)



## 176-Pin Plastic LQFP

Note: Pins marked as (NC) are no-connection pins which are left open.

## PIN DESCRIPTIONS

The basic functions of each pin of the MSM63P180 are described in Table 1.

A symbol with a slash (/) denotes a pin that has a secondary function.

Refer to Table 2 for secondary functions.

For type, "—" denotes a power supply pin, "I" an input pin, "O" an output pin, and "I/O" an input-output pin.

**Table 1 Pin Descriptions (Basic Functions)**

| Function     | Symbol           | Pin | Type | Description                                                                                                                                                                                                                                 |
|--------------|------------------|-----|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Power Supply | V <sub>PP</sub>  | 86  | —    | Power supply (+12.5 V) for PROM writing                                                                                                                                                                                                     |
|              | V <sub>DD</sub>  | 73  | —    | Positive power supply                                                                                                                                                                                                                       |
|              | V <sub>SS</sub>  | 62  | —    | Negative power supply                                                                                                                                                                                                                       |
|              | V <sub>DD1</sub> | 63  | —    | Power supply pins for LCD bias (internally generated). Capacitors (0.1 μF) should be connected between these pins and V <sub>SS</sub> .                                                                                                     |
|              | V <sub>DD2</sub> | 64  |      |                                                                                                                                                                                                                                             |
|              | V <sub>DD3</sub> | 65  |      |                                                                                                                                                                                                                                             |
|              | V <sub>DD4</sub> | 66  |      |                                                                                                                                                                                                                                             |
|              | V <sub>DD5</sub> | 67  |      |                                                                                                                                                                                                                                             |
|              | C1               | 68  | —    | Capacitor connection pins for LCD bias generation. A capacitor (0.1 μF) should be connected between C1 and C2.                                                                                                                              |
|              | C2               | 69  |      |                                                                                                                                                                                                                                             |
|              | V <sub>DDI</sub> | 87  | —    | Positive power supply pin for external interface (power supply for input, output, and input-output ports)                                                                                                                                   |
|              | V <sub>DDH</sub> | 70  | —    | Voltage multiplier pin for power supply backup (internally generated).                                                                                                                                                                      |
|              | CB1              | 71  | —    | Pins to connect a capacitor for voltage multiplier.                                                                                                                                                                                         |
|              | CB2              | 72  | —    | A capacitor (0.1 μF) should be connected between CB1 and CB2.                                                                                                                                                                               |
| Oscillation  | XT0              | 79  | I    | Low-speed clock oscillation pins.                                                                                                                                                                                                           |
|              | XT1              | 78  | O    | A 32.768 kHz crystal should be connected between XT0 and XT1, and C <sub>G</sub> (12 to 30 pF) should be connected between XT0 and V <sub>SS</sub> .                                                                                        |
|              | OSC0             | 76  | I    | High-speed clock oscillation pins.                                                                                                                                                                                                          |
|              | OSC1             | 75  | O    | A ceramic resonator and capacitors (C <sub>L0</sub> , C <sub>L1</sub> ) or external oscillation resistor (R <sub>OS</sub> ) should be connected to these pins.                                                                              |
| Test         | TST1             | 81  | I    | Input pins for testing.                                                                                                                                                                                                                     |
|              | TST2             | 80  | I    | A pull-down resistor is internally connected to these pins. The user cannot use these pins.                                                                                                                                                 |
| Reset        | RESET            | 77  | I    | Reset input pin.<br>Setting this pin to "H" level puts this device into a reset state. Then, setting this pin to "L" level starts executing an instruction from address 0000H.<br>A pull-down resistor is internally connected to this pin. |
| Buzzer       | BD               | 82  | O    | Buzzer output pin (non-inverted output)                                                                                                                                                                                                     |
|              | BDB              | 83  | O    | Buzzer output pin (inverted output)                                                                                                                                                                                                         |
| Melody       | MD               | 84  | O    | Melody output pin (non-inverted output)                                                                                                                                                                                                     |
|              | MDB              | 85  | O    | Melody output pin (inverted output)                                                                                                                                                                                                         |

Table 1 Pin Descriptions (Basic Functions) (continued)

| Function | Symbol    | Pin | Type | Description                                                  |
|----------|-----------|-----|------|--------------------------------------------------------------|
| Port     | P0.0/INT5 | 154 | I    | 4-bit input ports.                                           |
|          | P0.1/INT5 | 153 |      | Pull-up resistor input, pull-down resistor input, or         |
|          | P0.2/INT5 | 152 |      | high-impedance input is selectable for each bit.             |
|          | P0.3/INT5 | 151 |      |                                                              |
|          | P1.0/INT5 | 150 | I    |                                                              |
|          | P1.1/INT5 | 149 |      |                                                              |
|          | P1.2/INT5 | 148 |      |                                                              |
|          | P1.3/INT5 | 147 |      |                                                              |
|          | P2.0      | 146 | O    | 4-bit output ports.                                          |
|          | P2.1      | 145 |      | P-channel open drain output, N-channel open drain output,    |
|          | P2.2      | 144 |      | CMOS output, or high-impedance output is selectable for each |
|          | P2.3      | 143 |      | bit.                                                         |
|          | P3.0      | 142 | O    |                                                              |
|          | P3.1      | 141 |      |                                                              |
|          | P3.2      | 140 |      |                                                              |
|          | P3.3      | 139 |      |                                                              |
|          | P4.0/A0   | 138 | O    |                                                              |
|          | P4.1/A1   | 137 |      |                                                              |
|          | P4.2/A2   | 136 |      |                                                              |
|          | P4.3/A3   | 135 |      |                                                              |
|          | P5.0/A4   | 132 | O    |                                                              |
|          | P5.1/A5   | 131 |      |                                                              |
|          | P5.2/A6   | 130 |      |                                                              |
|          | P5.3/A7   | 129 |      |                                                              |
|          | P6.0/A8   | 128 | O    |                                                              |
|          | P6.1/A9   | 127 |      |                                                              |
|          | P6.2/A10  | 126 |      |                                                              |
|          | P6.3/A11  | 125 |      |                                                              |
|          | P7.0/A12  | 124 | O    |                                                              |
|          | P7.1/A13  | 123 |      |                                                              |
|          | P7.2/A14  | 122 |      |                                                              |
|          | P7.3/A15  | 121 |      |                                                              |

Table 1 Pin Descriptions (Basic Functions) (continued)

| Function | Symbol                          | Pin | Type | Description                                                                                                                                 |
|----------|---------------------------------|-----|------|---------------------------------------------------------------------------------------------------------------------------------------------|
| Port     | P8.0/ $\overline{RD}$           | 120 | I/O  | 4-bit input-output ports.                                                                                                                   |
|          | P8.1/ $\overline{WR}$           | 119 |      | In input mode, pull-up resistor input, pull-down resistor input, or high-impedance input is selectable for each bit.                        |
|          | P8.2                            | 118 |      |                                                                                                                                             |
|          | P8.3/INT4                       | 117 |      | In output mode, P-channel open drain output, N-channel open drain output, CMOS output, or high-impedance output is selectable for each bit. |
|          | P9.0/D0                         | 116 | I/O  |                                                                                                                                             |
|          | P9.1/D1                         | 115 |      |                                                                                                                                             |
|          | P9.2/D2                         | 114 |      |                                                                                                                                             |
|          | P9.3/D3                         | 113 |      |                                                                                                                                             |
|          | PA.0/D4                         | 112 | I/O  |                                                                                                                                             |
|          | PA.1/D5                         | 111 |      |                                                                                                                                             |
|          | PA.2/D6                         | 110 |      |                                                                                                                                             |
|          | PA.3/D7                         | 109 |      |                                                                                                                                             |
|          | PB.0/INT0/<br>TMOCAP/<br>TMOVF  | 108 | I/O  |                                                                                                                                             |
|          | PB.1/INT0/<br>TM1CAP/<br>TM1OVF | 107 |      |                                                                                                                                             |
|          | PB.2/INT0/T02CK                 | 106 |      |                                                                                                                                             |
|          | PB.3/INT0/T13CK                 | 105 |      |                                                                                                                                             |
|          | PC.0/INT1/RXD                   | 104 | I/O  |                                                                                                                                             |
|          | PC.1/INT1/TXC                   | 103 |      |                                                                                                                                             |
|          | PC.2/INT1/RXC                   | 102 |      |                                                                                                                                             |
|          | PC.3/INT1/TXD                   | 101 |      |                                                                                                                                             |
|          | PD.0/FRAME                      | 100 | I/O  |                                                                                                                                             |
|          | PD.1/LCLK                       | 99  |      |                                                                                                                                             |
|          | PD.2/TBCCLK                     | 98  |      |                                                                                                                                             |
|          | PD.3/HSCLK                      | 97  |      |                                                                                                                                             |
|          | PE.0/SIN                        | 96  | I/O  |                                                                                                                                             |
|          | PE.1/SOUT                       | 95  |      |                                                                                                                                             |
|          | PE.2/SCLK                       | 94  |      |                                                                                                                                             |
|          | PE.3/INT2                       | 93  |      |                                                                                                                                             |
|          | PF.0/INT3                       | 92  | I/O  |                                                                                                                                             |
|          | PF.1/INT3                       | 91  |      |                                                                                                                                             |
|          | PF.2/INT3                       | 90  |      |                                                                                                                                             |
|          | PF.3/INT3                       | 89  |      |                                                                                                                                             |



Table 1 Pin Descriptions (Basic Functions) (continued)

| Function | Symbol | Pin | Type | Description                    |
|----------|--------|-----|------|--------------------------------|
| LCD      | COM1   | 61  | 0    | LCD common signal output pins  |
|          | COM2   | 60  |      |                                |
|          | COM3   | 59  |      |                                |
|          | COM4   | 58  |      |                                |
|          | COM5   | 57  |      |                                |
|          | COM6   | 56  |      |                                |
|          | COM7   | 55  |      |                                |
|          | COM8   | 54  |      |                                |
|          | COM9   | 53  |      |                                |
|          | COM10  | 52  |      |                                |
|          | COM11  | 51  |      |                                |
|          | COM12  | 50  |      |                                |
|          | COM13  | 49  |      |                                |
|          | COM14  | 48  |      |                                |
|          | COM15  | 47  |      |                                |
|          | COM16  | 46  |      |                                |
|          | SEG0   | 44  | 0    | LCD segment signal output pins |
|          | SEG1   | 43  |      |                                |
|          | SEG2   | 42  |      |                                |
|          | SEG3   | 41  |      |                                |
|          | SEG4   | 40  |      |                                |
|          | SEG5   | 39  |      |                                |
|          | SEG6   | 38  |      |                                |
|          | SEG7   | 37  |      |                                |
|          | SEG8   | 36  |      |                                |
|          | SEG9   | 35  |      |                                |
|          | SEG10  | 34  |      |                                |
|          | SEG11  | 33  |      |                                |
|          | SEG12  | 32  |      |                                |
|          | SEG13  | 31  |      |                                |
|          | SEG14  | 30  |      |                                |
|          | SEG15  | 29  |      |                                |
|          | SEG16  | 28  |      |                                |
|          | SEG17  | 27  |      |                                |
|          | SEG18  | 26  |      |                                |
|          | SEG19  | 25  |      |                                |
|          | SEG20  | 24  |      |                                |
|          | SEG21  | 23  |      |                                |
|          | SEG22  | 22  |      |                                |
|          | SEG23  | 21  |      |                                |
|          | SEG24  | 20  |      |                                |

Table 1 Pin Descriptions (Basic Functions) (continued)

| Function | Symbol | Pin | Type | Description                    |
|----------|--------|-----|------|--------------------------------|
| LCD      | SEG25  | 19  | 0    | LCD segment signal output pins |
|          | SEG26  | 18  |      |                                |
|          | SEG27  | 17  |      |                                |
|          | SEG28  | 16  |      |                                |
|          | SEG29  | 15  |      |                                |
|          | SEG30  | 14  |      |                                |
|          | SEG31  | 13  |      |                                |
|          | SEG32  | 12  |      |                                |
|          | SEG33  | 11  |      |                                |
|          | SEG34  | 10  |      |                                |
|          | SEG35  | 9   |      |                                |
|          | SEG36  | 8   |      |                                |
|          | SEG37  | 7   |      |                                |
|          | SEG38  | 6   |      |                                |
|          | SEG39  | 5   |      |                                |
|          | SEG40  | 4   |      |                                |
|          | SEG41  | 3   |      |                                |
|          | SEG42  | 2   |      |                                |
|          | SEG43  | 1   |      |                                |
|          | SEG44  | 175 |      |                                |
|          | SEG45  | 174 |      |                                |
|          | SEG46  | 173 |      |                                |
|          | SEG47  | 172 |      |                                |
|          | SEG48  | 171 |      |                                |
|          | SEG49  | 170 |      |                                |
|          | SEG50  | 169 |      |                                |
|          | SEG51  | 168 |      |                                |
|          | SEG52  | 167 |      |                                |
|          | SEG53  | 166 |      |                                |
|          | SEG54  | 165 |      |                                |
|          | SEG55  | 164 |      |                                |
|          | SEG56  | 163 |      |                                |
|          | SEG57  | 162 |      |                                |
|          | SEG58  | 161 |      |                                |
|          | SEG59  | 160 |      |                                |
|          | SEG60  | 159 |      |                                |
|          | SEG61  | 158 |      |                                |
|          | SEG62  | 157 |      |                                |
|          | SEG63  | 156 |      |                                |

Table 2 shows the secondary functions of each pin of the MSM63P180.

**Table 2 Pin Descriptions (Secondary Functions)**

| Function           | Symbol      | Pin | Type | Description                                                                                                                                                                                                                                |
|--------------------|-------------|-----|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| External Interrupt | PB.0/INT0   | 108 | I    | External 0 interrupt input pins.<br>The change of input signal level causes an interrupt to occur.<br>The Port B Interrupt Enable register (PBIE) enables or disables an interrupt for each bit.                                           |
|                    | PB.1/INT0   | 107 |      |                                                                                                                                                                                                                                            |
|                    | PB.2/INT0   | 106 |      |                                                                                                                                                                                                                                            |
|                    | PB.3/INT0   | 105 |      |                                                                                                                                                                                                                                            |
|                    | PC.0/INT1   | 104 | I    | External 1 interrupt input pins.<br>The change of input signal level causes an interrupt to occur.<br>The Port C Interrupt Enable register (PCIE) enables or disables an interrupt for each bit.                                           |
|                    | PC.1/INT1   | 103 |      |                                                                                                                                                                                                                                            |
|                    | PC.2/INT1   | 102 |      |                                                                                                                                                                                                                                            |
|                    | PC.3/INT1   | 101 |      |                                                                                                                                                                                                                                            |
|                    | PE.3/INT2   | 93  | I    | External 2 interrupt input pin.<br>The change of input signal level causes an interrupt to occur.                                                                                                                                          |
|                    | PF.0/INT3   | 92  | I    | External 3 interrupt input pins.<br>The change of input signal level causes an interrupt to occur.<br>The Port F Interrupt Enable register (PFIE) enables or disables an interrupt for each bit.                                           |
|                    | PF.1/INT3   | 91  |      |                                                                                                                                                                                                                                            |
|                    | PF.2/INT3   | 90  |      |                                                                                                                                                                                                                                            |
|                    | PF.3/INT3   | 89  |      |                                                                                                                                                                                                                                            |
|                    | P8.3/INT4   | 117 | I    | External 4 interrupt input pin.<br>The change of input signal level causes an interrupt to occur.                                                                                                                                          |
|                    | P0.0/INT5   | 154 | I    | External 5 interrupt input pins.<br>The change of input signal level causes an interrupt to occur.<br>The Port 0 Interrupt Enable register (P0IE) and Port 1 Interrupt Enable register (P1IE) enable or disable an interrupt for each bit. |
|                    | P0.1/INT5   | 153 |      |                                                                                                                                                                                                                                            |
|                    | P0.2/INT5   | 152 |      |                                                                                                                                                                                                                                            |
|                    | P0.3/INT5   | 151 |      |                                                                                                                                                                                                                                            |
|                    | P1.0/INT5   | 150 |      |                                                                                                                                                                                                                                            |
|                    | P1.1/INT5   | 149 |      |                                                                                                                                                                                                                                            |
|                    | P1.2/INT5   | 148 |      |                                                                                                                                                                                                                                            |
|                    | P1.3/INT5   | 147 |      |                                                                                                                                                                                                                                            |
| Capture            | P1.0/TBCAP0 | 150 | I    | Time base counter capture trigger input pins                                                                                                                                                                                               |
|                    | P1.1/TBCAP1 | 149 | I    |                                                                                                                                                                                                                                            |
|                    | PB.0/TM0CAP | 108 | I    | Timer 0 capture trigger input pin                                                                                                                                                                                                          |
|                    | PB.1/TM1CAP | 107 | I    | Timer 1 capture trigger input pin                                                                                                                                                                                                          |

**Table 2 Pin Descriptions (Secondary Functions) (continued)**

| Function                     | Symbol      | Pin | Type | Description                                                                                                                                                                              |
|------------------------------|-------------|-----|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Timer                        | PB.0/TM0OVF | 108 | 0    | Timer 0 overflow flag output pin.                                                                                                                                                        |
|                              | PB.1/TM1OVF | 107 | 0    | Timer 1 overflow flag output pin.                                                                                                                                                        |
|                              | PB.2/T02CK  | 106 | I    | External clock input pin for timer 0 and timer 2.                                                                                                                                        |
|                              | PB.3/T13CK  | 105 | I    | External clock input pin for timer 1 and timer 3.                                                                                                                                        |
| LCD<br>External<br>Expansion | PD.0/FRAME  | 100 | 0    | Frame output pin for LCD driver expansion                                                                                                                                                |
|                              | PD.1/LCLK   | 99  | 0    | Clock output pin for LCD driver expansion                                                                                                                                                |
| Oscillation<br>Output        | PD.2/TBCCLK | 98  | 0    | Low-speed oscillation clock output pin                                                                                                                                                   |
|                              | PD.3/HSCLK  | 97  | 0    | High-speed oscillation clock output pin                                                                                                                                                  |
| Serial<br>Port               | PC.0/RXD    | 104 | I    | Serial port receive data input pin                                                                                                                                                       |
|                              | PC.1/TXC    | 103 | I/O  | Sync serial port clock input-output pin.<br>Transmit clock output when this device is used as a master processor.<br>Transmit clock input when this device is used as a slave processor. |
|                              | PC.2/RXC    | 102 | I/O  | Sync serial port clock input-output pin.<br>Receive clock output when this device is used as a master processor.<br>Receive clock input when this device is used as a slave processor.   |
|                              | PC.3/TXD    | 101 | 0    | Serial port transmit data output pin.                                                                                                                                                    |
| Shift<br>Register            | PE.0/SIN    | 96  | I    | Shift register receive data input pin                                                                                                                                                    |
|                              | PE.1/SOUT   | 95  | 0    | Shift register transmit data output pin                                                                                                                                                  |
|                              | PE.2/SCLK   | 94  | I/O  | Shift register clock input-output pin.<br>Clock output when this device is used as a master processor.<br>Clock input when this device is used as a slave processor.                     |

Table 2 Pin Descriptions (Secondary Functions) (continued)

| Function        | Symbol                | Pin | Type | Description                                                  |
|-----------------|-----------------------|-----|------|--------------------------------------------------------------|
| External Memory | P4.0/A0               | 138 | 0    | Address output bus for external memory                       |
|                 | P4.1/A1               | 137 |      |                                                              |
|                 | P4.2/A2               | 136 |      |                                                              |
|                 | P4.3/A3               | 135 |      |                                                              |
|                 | P5.0/A4               | 132 |      |                                                              |
|                 | P5.1/A5               | 131 |      |                                                              |
|                 | P5.2/A6               | 130 |      |                                                              |
|                 | P5.3/A7               | 129 |      |                                                              |
|                 | P6.0/A8               | 128 |      |                                                              |
|                 | P6.1/A9               | 127 |      |                                                              |
|                 | P6.2/A10              | 126 |      |                                                              |
|                 | P6.3/A11              | 125 |      |                                                              |
|                 | P7.0/A12              | 124 |      |                                                              |
|                 | P7.1/A13              | 123 |      |                                                              |
|                 | P7.2/A14              | 122 |      |                                                              |
|                 | P7.3/A15              | 121 |      |                                                              |
|                 | P9.0/D0               | 116 | I/O  | Data bus for external memory                                 |
|                 | P9.1/D1               | 115 |      |                                                              |
|                 | P9.2/D2               | 114 |      |                                                              |
|                 | P9.3/D3               | 113 |      |                                                              |
|                 | PA.0/D4               | 112 |      |                                                              |
|                 | PA.1/D5               | 111 |      |                                                              |
|                 | PA.2/D6               | 110 |      |                                                              |
|                 | PA.3/D7               | 109 |      |                                                              |
|                 | P8.0/ $\overline{RD}$ | 120 | 0    | Read signal output pin for external memory (negative logic)  |
|                 | P8.1/ $\overline{WR}$ | 119 | 0    | Write signal output pin for external memory (negative logic) |

## ABSOLUTE MAXIMUM RATINGS

(V<sub>SS</sub> = 0 V)

| Parameter              | Symbol            | Condition                          | Rating                         | Unit |
|------------------------|-------------------|------------------------------------|--------------------------------|------|
| Power Supply Voltage 1 | V <sub>DD1</sub>  | Ta = 25°C                          | −0.3 to +1.6                   | V    |
| Power Supply Voltage 2 | V <sub>DD2</sub>  | Ta = 25°C                          | −0.3 to +2.9                   | V    |
| Power Supply Voltage 3 | V <sub>DD3</sub>  | Ta = 25°C                          | −0.3 to +4.2                   | V    |
| Power Supply Voltage 4 | V <sub>DD4</sub>  | Ta = 25°C                          | −0.3 to +5.5                   | V    |
| Power Supply Voltage 5 | V <sub>DD5</sub>  | Ta = 25°C                          | −0.3 to +6.8                   | V    |
| Power Supply Voltage 6 | V <sub>DD</sub>   | Ta = 25°C                          | −0.3 to +6.0                   | V    |
| Power Supply Voltage 7 | V <sub>DDI</sub>  | Ta = 25°C                          | −0.3 to +6.0                   | V    |
| Power Supply Voltage 8 | V <sub>DDH</sub>  | Ta = 25°C                          | −0.3 to +6.0                   | V    |
| Power Supply Voltage 9 | V <sub>DDL</sub>  | Ta = 25°C                          | −0.3 to +6.0                   | V    |
| Input Voltage 1        | V <sub>IN1</sub>  | V <sub>DD</sub> Input, Ta = 25°C   | −0.3 to V <sub>DD</sub> + 0.3  | V    |
| Input Voltage 2        | V <sub>IN2</sub>  | V <sub>DDI</sub> Input, Ta = 25°C  | −0.3 to V <sub>DDI</sub> + 0.3 | V    |
| Output Voltage 1       | V <sub>OUT1</sub> | V <sub>DD1</sub> Output, Ta = 25°C | −0.3 to V <sub>DD1</sub> + 0.3 | V    |
| Output Voltage 2       | V <sub>OUT2</sub> | V <sub>DD2</sub> Output, Ta = 25°C | −0.3 to V <sub>DD2</sub> + 0.3 | V    |
| Output Voltage 3       | V <sub>OUT3</sub> | V <sub>DD3</sub> Output, Ta = 25°C | −0.3 to V <sub>DD3</sub> + 0.3 | V    |
| Output Voltage 4       | V <sub>OUT4</sub> | V <sub>DD4</sub> Output, Ta = 25°C | −0.3 to V <sub>DD4</sub> + 0.3 | V    |
| Output Voltage 5       | V <sub>OUT5</sub> | V <sub>DD5</sub> Output, Ta = 25°C | −0.3 to V <sub>DD5</sub> + 0.3 | V    |
| Output Voltage 6       | V <sub>OUT6</sub> | V <sub>DD</sub> Output, Ta = 25°C  | −0.3 to V <sub>DD</sub> + 0.3  | V    |
| Output Voltage 7       | V <sub>OUT7</sub> | V <sub>DDI</sub> Output, Ta = 25°C | −0.3 to V <sub>DDI</sub> + 0.3 | V    |
| Output Voltage 8       | V <sub>OUT8</sub> | V <sub>DDH</sub> Output, Ta = 25°C | −0.3 to V <sub>DDH</sub> + 0.3 | V    |
| Storage Temperature    | T <sub>STG</sub>  | —                                  | −55 to +150                    | °C   |

## RECOMMENDED OPERATING CONDITIONS

- When backup is used

(V<sub>SS</sub> = 0 V)

| Parameter                         | Symbol           | Condition                            | Range       | Unit |
|-----------------------------------|------------------|--------------------------------------|-------------|------|
| Operating Temperature             | T <sub>op</sub>  | —                                    | 0 to +65    | °C   |
| Operating Voltage                 | V <sub>DD</sub>  | —                                    | 1.45 to 2.7 | V    |
|                                   | V <sub>DDI</sub> | —                                    | 1.5 to 5.5  | V    |
| Crystal Oscillation Frequency     | f <sub>XT</sub>  | —                                    | 30 to 35    | kHz  |
| Ceramic Oscillation Frequency     | f <sub>CM</sub>  | V <sub>DD</sub> = 1.45 to 2.7 V (*1) | 200k to 1M  | Hz   |
| External RC Oscillator Resistance | R <sub>OS</sub>  | V <sub>DD</sub> = 1.45 to 2.7 V (*1) | 50 to 300   | kΩ   |

\*1 A voltage of 2.7 V or more must be applied to V<sub>DDH</sub>.

- When backup is not used

(V<sub>SS</sub> = 0 V)

| Parameter                         | Symbol           | Condition                      | Range      | Unit |
|-----------------------------------|------------------|--------------------------------|------------|------|
| Operating Temperature             | T <sub>op</sub>  | —                              | 0 to +65   | °C   |
| Operating Voltage                 | V <sub>DD</sub>  | —                              | 2.7 to 5.5 | V    |
|                                   | V <sub>DDI</sub> | —                              | 1.8 to 5.5 | V    |
| Crystal Oscillation Frequency     | f <sub>XT</sub>  | —                              | 30 to 35   | kHz  |
| Ceramic Oscillation Frequency     | f <sub>CM</sub>  | V <sub>DD</sub> = 2.7 to 5.5 V | 300k to 1M | Hz   |
|                                   |                  | V <sub>DD</sub> = 2.9 to 5.5 V | 200k to 2M |      |
| External RC Oscillator Resistance | R <sub>OS</sub>  | V <sub>DD</sub> = 2.7 to 5.5 V | 50 to 300  | kΩ   |
|                                   |                  | V <sub>DD</sub> = 2.9 to 5.5 V | 30 to 300  |      |

## ELECTRICAL CHARACTERISTICS

### DC Characteristics

( $V_{DD} = V_{DD1} = 1.45$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = 0$  to  $+65^\circ\text{C}$  unless otherwise specified)

| Parameter                                      | Symbol             | Condition                                                          | Min.      | Typ.                   | Max.      | Unit  | Measuring Circuit |
|------------------------------------------------|--------------------|--------------------------------------------------------------------|-----------|------------------------|-----------|-------|-------------------|
| V <sub>DD2</sub> Voltage                       | V <sub>DD2</sub>   | 1/5 bias, 1/4 bias<br>(T <sub>a</sub> = 25°C)                      | 1.7       | 1.8                    | 1.9       | V     | 1                 |
| V <sub>DD2</sub> Voltage Temperature Deviation | ΔV <sub>DD2</sub>  | —                                                                  | —         | −4                     | —         | mV/°C |                   |
| V <sub>DD1</sub> Voltage                       | V <sub>DD1</sub>   | 1/5 bias, 1/4 bias                                                 | Typ.− 0.2 | 1/2 × V <sub>DD2</sub> | Typ.+ 0.2 | V     |                   |
| V <sub>DD3</sub> Voltage                       | V <sub>DD3</sub>   | 1/5 bias                                                           | Typ.− 0.3 | 3/2 × V <sub>DD2</sub> | Typ.+ 0.2 | V     |                   |
|                                                |                    | 1/4 bias (connect<br>V <sub>DD3</sub> and V <sub>DD2</sub> )       | Typ.− 0.2 | V <sub>DD2</sub>       | Typ.+ 0.2 |       |                   |
| V <sub>DD4</sub> Voltage                       | V <sub>DD4</sub>   | 1/5 bias                                                           | Typ.− 0.4 | 2 × V <sub>DD2</sub>   | Typ.+ 0.2 | V     |                   |
|                                                |                    | 1/4 bias                                                           | Typ.− 0.3 | 3/2 × V <sub>DD2</sub> | Typ.+ 0.2 |       |                   |
| V <sub>DD5</sub> Voltage                       | V <sub>DD5</sub>   | 1/5 bias                                                           | Typ.− 0.5 | 5/2 × V <sub>DD2</sub> | Typ.+ 0.2 | V     |                   |
|                                                |                    | 1/4 bias                                                           | Typ.− 0.4 | 2 × V <sub>DD2</sub>   | Typ.+ 0.2 |       |                   |
| V <sub>DDH</sub> Voltage<br>(backup used)      | V <sub>DDH</sub>   | High-speed clock oscillation<br>stopped<br>V <sub>DD</sub> = 1.5 V | 2.8       | —                      | 3.0       | V     |                   |
| Crystal Oscillation Start Voltage              | V <sub>STA</sub>   | Oscillation start time:<br>within 5 seconds                        | 1.40      | —                      | —         | V     |                   |
| Crystal Oscillation Hold Voltage               | V <sub>HOLD</sub>  | —                                                                  | 1.35      | —                      | —         | V     |                   |
| Crystal Oscillation Stop Detect Time           | T <sub>STOP</sub>  | —                                                                  | 0.1       | —                      | 5.0       | ms    |                   |
| External Crystal Oscillator Capacitance        | C <sub>G</sub>     | —                                                                  | 12        | —                      | 30        | pF    |                   |
| Internal Crystal Oscillator Capacitance        | C <sub>D</sub>     | —                                                                  | 12        | 15                     | 20        | pF    |                   |
| External Ceramic Oscillator<br>Capacitance     | C <sub>L0, 1</sub> | CSA2.00MG (Murata<br>MFG.-make) used<br>V <sub>DD</sub> = 3.0 V    | —         | 30                     | —         | pF    |                   |
| Internal RC Oscillator Capacitance             | C <sub>OS</sub>    | —                                                                  | 8         | 12                     | 16        | pF    |                   |
| POR Voltage                                    | V <sub>POR1</sub>  | V <sub>DD</sub> = 1.5 V                                            | 0.0       | —                      | 0.4       | V     |                   |
|                                                |                    | —                                                                  | 0.0       | —                      | 0.7       | V     |                   |
| Non-POR Voltage                                | V <sub>POR2</sub>  | V <sub>DD</sub> = 1.5 V                                            | 1.2       | —                      | 1.5       | V     |                   |
|                                                |                    | —                                                                  | 2.0       | —                      | 3.0       | V     |                   |

- Notes: 1. " $T_{STOP}$ " indicates that if the crystal oscillator stops over the value of  $T_{STOP}$ , the system reset occurs.
2. "POR" denotes Power On Reset.
3. " $V_{POR1}$ " indicates that POR occurs when  $V_{DD}$  falls from  $V_{DD}$  to  $V_{POR1}$  and again rises up to  $V_{DD}$ .
4. " $V_{POR2}$ " indicates that POR does not occur when  $V_{DD}$  falls from  $V_{DD}$  to  $V_{POR2}$  and again rises up to  $V_{DD}$ .



## DC Characteristics

- When backup is used

( $V_{DD} = V_{DD1} = 1.5\text{ V}$ ,  $V_{DDH} = 3.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = 0\text{ to }+65^\circ\text{C}$  unless otherwise specified)

| Parameter        | Symbol    | Condition                                                                                        | Min. | Typ. | Max. | Unit          | Measuring Circuit |
|------------------|-----------|--------------------------------------------------------------------------------------------------|------|------|------|---------------|-------------------|
| Supply Current 1 | $I_{DD1}$ | CPU is in HALT state.<br>(High-speed clock oscillation stopped)                                  | —    | 10   | 20   | $\mu\text{A}$ | 1                 |
| Supply Current 2 | $I_{DD2}$ | CPU is in HALT state.<br>LCD is in Power Down mode.<br>(High-speed clock oscillation stopped)    | —    | 8    | 16   | $\mu\text{A}$ |                   |
| Supply Current 3 | $I_{DD3}$ | CPU is in operating state.<br>(High-speed clock oscillation stopped)                             | —    | 100  | 140  | $\mu\text{A}$ |                   |
| Supply Current 4 | $I_{DD4}$ | CPU is in operation at high-speed oscillation<br>(RC oscillation, $R_{OS} = 51\text{ k}\Omega$ ) | —    | 1.5  | 2    | $\text{mA}$   |                   |
| Supply Current 5 | $I_{DD5}$ | CPU is in operation at high-speed oscillation<br>(Ceramic oscillation, 1 MHz)                    | —    | 2    | 3    | $\text{mA}$   |                   |

- When backup is not used

( $V_{DD} = V_{DD1} = V_{DDH} = 3.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = 0\text{ to }+65^\circ\text{C}$  unless otherwise specified)

| Parameter        | Symbol    | Condition                                                                                        | Min. | Typ. | Max. | Unit          | Measuring Circuit |
|------------------|-----------|--------------------------------------------------------------------------------------------------|------|------|------|---------------|-------------------|
| Supply Current 1 | $I_{DD1}$ | CPU is in HALT state.<br>(High-speed clock oscillation stopped)                                  | —    | 5    | 10   | $\mu\text{A}$ | 1                 |
| Supply Current 2 | $I_{DD2}$ | CPU is in HALT state.<br>LCD is in Power Down mode.<br>(High-speed clock oscillation stopped)    | —    | 4    | 7    | $\mu\text{A}$ |                   |
| Supply Current 3 | $I_{DD3}$ | CPU is in operating state.<br>(High-speed clock oscillation stopped)                             | —    | 60   | 120  | $\mu\text{A}$ |                   |
| Supply Current 4 | $I_{DD4}$ | CPU is in operation at high-speed oscillation<br>(RC oscillation, $R_{OS} = 51\text{ k}\Omega$ ) | —    | 1.5  | 2    | $\text{mA}$   |                   |
| Supply Current 5 | $I_{DD5}$ | CPU is in operation at high-speed oscillation<br>(Ceramic oscillation, 2 MHz)                    | —    | 3.5  | 5    | $\text{mA}$   |                   |

DC Characteristics (continued)

( $V_{DD} = V_{DD1} = V_{DDH} = 3.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $V_{DD1} = 1.1\text{ V}$ ,  $V_{DD2} = 2.2\text{ V}$ ,  $V_{DD3} = 3.3\text{ V}$ ,  
 $V_{DD4} = 4.4\text{ V}$ ,  $V_{DD5} = 5.5\text{ V}$ ,  $T_a = 0\text{ to }+65^\circ\text{C}$  unless otherwise specified)

| Parameter                                                                                     | Symbol      | Condition                                                    |                                   | Min. | Typ. | Max. | Unit | Measuring Circuit |
|-----------------------------------------------------------------------------------------------|-------------|--------------------------------------------------------------|-----------------------------------|------|------|------|------|-------------------|
| Output Current 1<br>(P2.0 to P2.3)<br>(P3.0 to P3.3)<br>(P4.0 to P4.3)<br>⋮<br>(PF.0 to PF.3) | $I_{OH1}$   | $V_{OH1} = V_{DD1} - 0.5\text{ V}$                           | $V_{DD1} = 1.5\text{ V}$          | -2.1 | -1.0 | -0.2 | mA   | 2                 |
|                                                                                               |             |                                                              | $V_{DD1} = 3.0\text{ V}$          | -5.0 | -2.5 | -1.0 | mA   |                   |
|                                                                                               |             |                                                              | $V_{DD1} = 5.0\text{ V}$          | -8.0 | -4.0 | -2.0 | mA   |                   |
|                                                                                               | $I_{OL1}$   | $V_{OL1} = 0.5\text{ V}$                                     | $V_{DD1} = 1.5\text{ V}$          | 0.2  | 1.0  | 2.1  | mA   |                   |
|                                                                                               |             |                                                              | $V_{DD1} = 3.0\text{ V}$          | 1.0  | 2.5  | 5.0  | mA   |                   |
|                                                                                               |             |                                                              | $V_{DD1} = 5.0\text{ V}$          | 2.0  | 4.0  | 8.0  | mA   |                   |
| Output Current 2<br>(BD, BDB)<br>(MD, MDB)                                                    | $I_{OH2}$   | $V_{OH2} = V_{DD} - 0.7\text{ V}$                            | $V_{DD} = 1.5\text{ V}$           | -1.8 | -1.0 | -0.2 | mA   |                   |
|                                                                                               |             |                                                              | $V_{DD} = 3.0\text{ V}$           | -5.0 | -3.0 | -1.0 | mA   |                   |
|                                                                                               |             |                                                              | $V_{DD} = V_{DDH} = 5.0\text{ V}$ | -9.0 | -5.5 | -4.0 | mA   |                   |
|                                                                                               | $I_{OL2}$   | $V_{OL2} = 0.7\text{ V}$                                     | $V_{DD} = 1.5\text{ V}$           | 0.2  | 1.0  | 1.8  | mA   |                   |
|                                                                                               |             |                                                              | $V_{DD} = 3.0\text{ V}$           | 1.0  | 3.0  | 5.0  | mA   |                   |
|                                                                                               |             |                                                              | $V_{DD} = V_{DDH} = 5.0\text{ V}$ | 4.0  | 5.5  | 9.0  | mA   |                   |
| Output Current 3<br>(SEG0 to SEG63)<br>(COM1 to COM16)                                        | $I_{OH3}$   | $V_{OH3} = V_{DD5} - 0.2\text{ V}$ ( $V_{DD5}$ level)        |                                   | —    | —    | -4   | μA   |                   |
|                                                                                               | $I_{OHM3}$  | $V_{OHM3} = V_{DD4} + 0.2\text{ V}$ ( $V_{DD4}$ level)       |                                   | 4    | —    | —    | μA   |                   |
|                                                                                               | $I_{OHM3S}$ | $V_{OHM3S} = V_{DD4} - 0.2\text{ V}$ ( $V_{DD4}$ level)      |                                   | —    | —    | -4   | μA   |                   |
|                                                                                               | $I_{OMH3}$  | $V_{OMH3} = V_{DD3} + 0.2\text{ V}$ ( $V_{DD3}$ level)       |                                   | 4    | —    | —    | μA   |                   |
|                                                                                               | $I_{OMH3S}$ | $V_{OMH3S} = V_{DD3} - 0.2\text{ V}$ ( $V_{DD3}$ level)      |                                   | —    | —    | -4   | μA   |                   |
|                                                                                               | $I_{OML3}$  | $V_{OML3} = V_{DD2} + 0.2\text{ V}$ ( $V_{DD2}$ level)       |                                   | 4    | —    | —    | μA   |                   |
|                                                                                               | $I_{OML3S}$ | $V_{OML3S} = V_{DD2} - 0.2\text{ V}$ ( $V_{DD2}$ level)      |                                   | —    | —    | -4   | μA   |                   |
|                                                                                               | $I_{OLM3}$  | $V_{OLM3} = V_{DD1} + 0.2\text{ V}$ ( $V_{DD1}$ level)       |                                   | 4    | —    | —    | μA   |                   |
|                                                                                               | $I_{OLM3S}$ | $V_{OLM3S} = V_{DD1} - 0.2\text{ V}$ ( $V_{DD1}$ level)      |                                   | —    | —    | -4   | μA   |                   |
|                                                                                               | $I_{OL3}$   | $V_{OL3} = V_{SS} + 0.2\text{ V}$ ( $V_{SS}$ level)          |                                   | 4    | —    | —    | μA   |                   |
| Output Current 4<br>(OSC1)                                                                    | $I_{OH4R}$  | $V_{OH4R} = V_{DDH} - 0.5\text{ V}$<br>(RC oscillation)      | $V_{DD} = V_{DDH} = 3.0\text{ V}$ | -2.0 | -1.2 | -0.6 | mA   |                   |
|                                                                                               |             |                                                              | $V_{DD} = V_{DDH} = 5.0\text{ V}$ | -3.5 | -2.0 | -1.0 | mA   |                   |
|                                                                                               | $I_{OL4R}$  | $V_{OL4R} = 0.5\text{ V}$<br>(RC oscillation)                | $V_{DD} = V_{DDH} = 3.0\text{ V}$ | 0.6  | 1.2  | 2.0  | mA   |                   |
|                                                                                               |             |                                                              | $V_{DD} = V_{DDH} = 5.0\text{ V}$ | 1.0  | 2.0  | 3.5  | mA   |                   |
|                                                                                               | $I_{OH4C}$  | $V_{OH4C} = V_{DDH} - 0.5\text{ V}$<br>(ceramic oscillation) | $V_{DD} = V_{DDH} = 3.0\text{ V}$ | -200 | -100 | -50  | μA   |                   |
|                                                                                               |             |                                                              | $V_{DD} = V_{DDH} = 5.0\text{ V}$ | -400 | -200 | -100 | μA   |                   |
|                                                                                               | $I_{OL4C}$  | $V_{OL4C} = 0.5\text{ V}$<br>(ceramic oscillation)           | $V_{DD} = V_{DDH} = 3.0\text{ V}$ | 50   | 100  | 200  | μA   |                   |
|                                                                                               |             |                                                              | $V_{DD} = V_{DDH} = 5.0\text{ V}$ | 100  | 200  | 400  | μA   |                   |
| Output Leakage<br>(P2.0 to P2.3)<br>(P3.0 to P3.3)<br>(P4.0 to P4.3)<br>⋮<br>(PF.0 to PF.3)   | $I_{OOH}$   | $V_{OH} = V_{DD1}$                                           |                                   | —    | —    | 0.3  | μA   |                   |
|                                                                                               | $I_{OOL}$   | $V_{OL} = V_{SS}$                                            |                                   | -0.3 | —    | —    | μA   |                   |

# DC Characteristics (continued)

( $V_{DD} = V_{DD1} = V_{DDH} = 3.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $V_{DD1} = 1.1\text{ V}$ ,  $V_{DD2} = 2.2\text{ V}$ ,  $V_{DD3} = 3.3\text{ V}$ ,  
 $V_{DD4} = 4.4\text{ V}$ ,  $V_{DD5} = 5.5\text{ V}$ ,  $T_a = 0\text{ to }+65^{\circ}\text{C}$  unless otherwise specified)

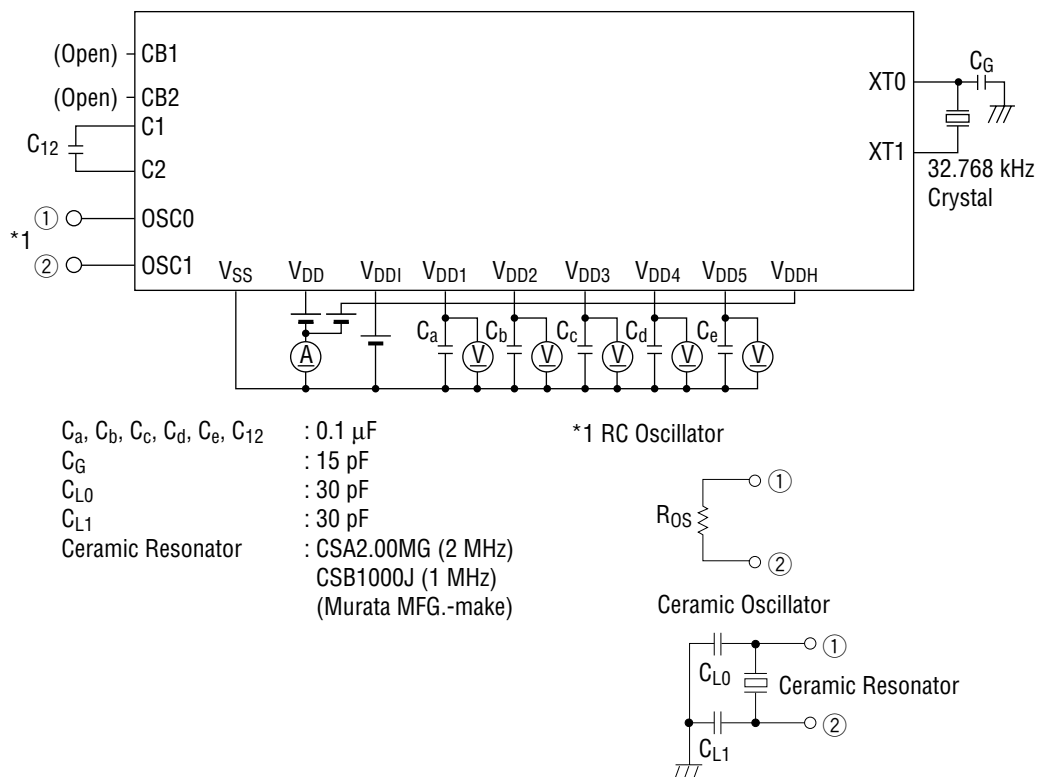
| Parameter                                                                                                      | Symbol     | Condition                                       |                                   | Min. | Typ. | Max.  | Unit          | Measuring Circuit |
|----------------------------------------------------------------------------------------------------------------|------------|-------------------------------------------------|-----------------------------------|------|------|-------|---------------|-------------------|
| Input Current 1<br>(P0.0 to P0.3)<br>(P1.0 to P1.3)<br>(P8.0 to P8.3)<br>(P9.0 to P9.3)<br>⋮<br>(PF.0 to PF.3) | $I_{IH1}$  | $V_{IH1} = V_{DD1}$<br>(when pulled down)       | $V_{DD1} = 1.5\text{ V}$          | 2    | 10   | 30    | $\mu\text{A}$ | 3                 |
|                                                                                                                |            |                                                 | $V_{DD1} = 3.0\text{ V}$          | 30   | 90   | 180   | $\mu\text{A}$ |                   |
|                                                                                                                |            |                                                 | $V_{DD1} = 5.0\text{ V}$          | 100  | 250  | 500   | $\mu\text{A}$ |                   |
|                                                                                                                | $I_{IL1}$  | $V_{IL1} = V_{SS}$<br>(when pulled up)          | $V_{DD1} = 1.5\text{ V}$          | -30  | -10  | -2    | $\mu\text{A}$ |                   |
|                                                                                                                |            |                                                 | $V_{DD1} = 3.0\text{ V}$          | -180 | -90  | -30   | $\mu\text{A}$ |                   |
|                                                                                                                |            |                                                 | $V_{DD1} = 5.0\text{ V}$          | -500 | -250 | -100  | $\mu\text{A}$ |                   |
|                                                                                                                | $I_{IH1Z}$ | $V_{IH1} = V_{DD1}$ (in a high impedance state) |                                   | 0.0  | —    | 1.0   | $\mu\text{A}$ |                   |
|                                                                                                                | $I_{IL1Z}$ | $V_{IL1} = V_{SS}$ (in a high impedance state)  |                                   | -1.0 | —    | 0.0   | $\mu\text{A}$ |                   |
| Input Current 2<br>(OSC0)                                                                                      | $I_{IL2}$  | $V_{IL2} = V_{SS}$<br>(when pulled up)          | $V_{DD} = V_{DDH} = 3.0\text{ V}$ | -200 | -110 | -30   | $\mu\text{A}$ |                   |
|                                                                                                                |            |                                                 | $V_{DD} = V_{DDH} = 5.0\text{ V}$ | -600 | -350 | -150  | $\mu\text{A}$ |                   |
|                                                                                                                | $I_{IH2R}$ | $V_{IH2} = V_{DDH}$ (RC oscillation)            |                                   | 0.0  | —    | 1.0   | $\mu\text{A}$ |                   |
|                                                                                                                | $I_{IL2R}$ | $V_{IL2} = V_{SS}$ (RC oscillation)             |                                   | -1.0 | —    | 0.0   | $\mu\text{A}$ |                   |
|                                                                                                                | $I_{IH2C}$ | $V_{IH2} = V_{DDH}$<br>(ceramic oscillation)    | $V_{DD} = V_{DDH} = 3.0\text{ V}$ | 0.1  | 0.5  | 1.0   | $\mu\text{A}$ |                   |
|                                                                                                                |            |                                                 | $V_{DD} = V_{DDH} = 5.0\text{ V}$ | 0.75 | 1.5  | 3.0   | $\mu\text{A}$ |                   |
|                                                                                                                | $I_{IL2C}$ | $V_{IL2} = V_{SS}$<br>(ceramic oscillation)     | $V_{DD} = V_{DDH} = 3.0\text{ V}$ | -1.0 | -0.5 | -0.1  | $\mu\text{A}$ |                   |
|                                                                                                                |            |                                                 | $V_{DD} = V_{DDH} = 5.0\text{ V}$ | -3.0 | -1.5 | -0.75 | $\mu\text{A}$ |                   |
| Input Current 3<br>(RESET)                                                                                     | $I_{IH3}$  | $V_{IH3} = V_{DD}$                              | $V_{DD} = 1.5\text{ V}$           | 10   | 40   | 80    | $\mu\text{A}$ |                   |
|                                                                                                                |            |                                                 | $V_{DD} = 3.0\text{ V}$           | 150  | 350  | 600   | $\mu\text{A}$ |                   |
|                                                                                                                |            |                                                 | $V_{DD} = V_{DDH} = 5.0\text{ V}$ | 0.5  | 1.0  | 2.0   | $\text{mA}$   |                   |
|                                                                                                                | $I_{IL3}$  | $V_{IL3} = V_{SS}$                              |                                   | -1.0 | —    | 0.0   | $\mu\text{A}$ |                   |
| Input Current 4<br>(TST1, TST2)                                                                                | $I_{IH4}$  | $V_{IH4} = V_{DD}$                              | $V_{DD} = 1.5\text{ V}$           | 30   | 120  | 300   | $\mu\text{A}$ |                   |
|                                                                                                                |            |                                                 | $V_{DD} = 3.0\text{ V}$           | 0.3  | 0.75 | 1.5   | $\text{mA}$   |                   |
|                                                                                                                |            |                                                 | $V_{DD} = V_{DDH} = 5.0\text{ V}$ | 1.25 | 2.5  | 4.0   | $\text{mA}$   |                   |
|                                                                                                                | $I_{IL4}$  | $V_{IL4} = V_{SS}$                              |                                   | -1.0 | —    | 0.0   | $\mu\text{A}$ |                   |

DC Characteristics (continued)

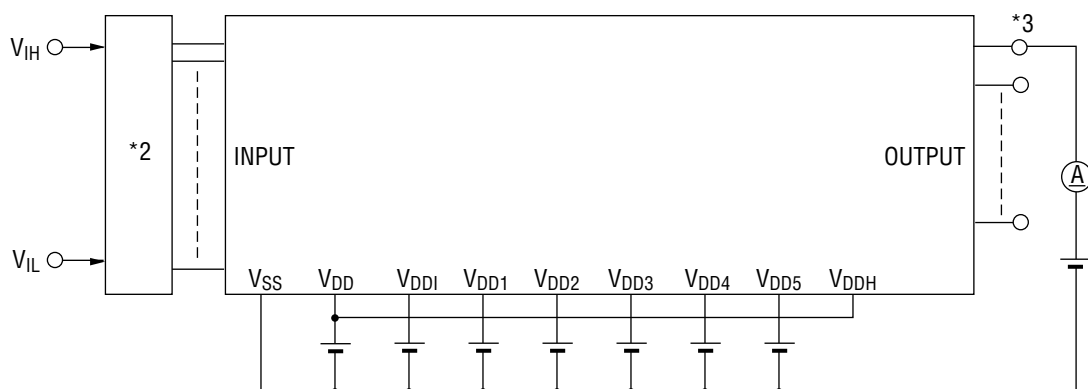
( $V_{DD} = V_{DD1} = V_{DDH} = 3.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $V_{DD1} = 1.1\text{ V}$ ,  $V_{DD2} = 2.2\text{ V}$ ,  $V_{DD3} = 3.3\text{ V}$ ,  
 $V_{DD4} = 4.4\text{ V}$ ,  $V_{DD5} = 5.5\text{ V}$ ,  $T_a = 0\text{ to }+65^\circ\text{C}$  unless otherwise specified)

| Parameter                                                                                                            | Symbol          | Condition                         | Min. | Typ. | Max. | Unit | Measuring Circuit |
|----------------------------------------------------------------------------------------------------------------------|-----------------|-----------------------------------|------|------|------|------|-------------------|
| Input Voltage 1<br>(P0.0 to P0.3)<br>(P1.0 to P1.3)<br>(P8.0 to P8.3)<br>(P9.0 to P9.3)<br>⋮<br>(PF.0 to PF.3)       | $V_{IH1}$       | $V_{DD1} = 1.5\text{ V}$          | 1.2  | —    | 1.5  | V    | 4                 |
|                                                                                                                      |                 | $V_{DD1} = 3.0\text{ V}$          | 2.4  | —    | 3.0  | V    |                   |
|                                                                                                                      |                 | $V_{DD1} = 5.0\text{ V}$          | 4.0  | —    | 5.0  | V    |                   |
|                                                                                                                      | $V_{IL1}$       | $V_{DD1} = 1.5\text{ V}$          | 0.0  | —    | 0.3  | V    |                   |
|                                                                                                                      |                 | $V_{DD1} = 3.0\text{ V}$          | 0.0  | —    | 0.6  | V    |                   |
|                                                                                                                      |                 | $V_{DD1} = 5.0\text{ V}$          | 0.0  | —    | 1.0  | V    |                   |
| Input Voltage 2<br>(OSC0)                                                                                            | $V_{IH2}$       | $V_{DD} = V_{DDH} = 3.0\text{ V}$ | 2.4  | —    | 3.0  | V    |                   |
|                                                                                                                      |                 | $V_{DD} = V_{DDH} = 5.0\text{ V}$ | 4.0  | —    | 5.0  | V    |                   |
|                                                                                                                      | $V_{IL2}$       | $V_{DD} = V_{DDH} = 3.0\text{ V}$ | 0.0  | —    | 0.6  | V    |                   |
|                                                                                                                      |                 | $V_{DD} = V_{DDH} = 5.0\text{ V}$ | 0.0  | —    | 1.0  | V    |                   |
| Input Voltage 3<br>(RESET, TST1, TST2)                                                                               | $V_{IH3}$       | $V_{DD} = 1.5\text{ V}$           | 1.35 | —    | 1.5  | V    |                   |
|                                                                                                                      |                 | $V_{DD} = 3.0\text{ V}$           | 2.4  | —    | 3.0  | V    |                   |
|                                                                                                                      |                 | $V_{DD} = V_{DDH} = 5.0\text{ V}$ | 4.0  | —    | 5.0  | V    |                   |
|                                                                                                                      | $V_{IL3}$       | $V_{DD} = 1.5\text{ V}$           | 0.0  | —    | 0.15 | V    |                   |
|                                                                                                                      |                 | $V_{DD} = 3.0\text{ V}$           | 0.0  | —    | 0.6  | V    |                   |
|                                                                                                                      |                 | $V_{DD} = V_{DDH} = 5.0\text{ V}$ | 0.0  | —    | 1.0  | V    |                   |
| Hysteresis Width 1<br>(P0.0 to P0.3)<br>(P1.0 to P1.3)<br>(P8.0 to P8.3)<br>⋮<br>(PF.0 to PF.3)                      | $\Delta V_{T1}$ | $V_{DD1} = 1.5\text{ V}$          | 0.05 | 0.1  | 0.3  | V    | 1                 |
|                                                                                                                      |                 | $V_{DD1} = 3.0\text{ V}$          | 0.2  | 0.5  | 1.0  | V    |                   |
|                                                                                                                      |                 | $V_{DD1} = 5.0\text{ V}$          | 0.25 | 1.0  | 1.5  | V    |                   |
| Hysteresis Width 2<br>(RESET, TST1, TST2)                                                                            | $\Delta V_{T2}$ | $V_{DD} = 1.5\text{ V}$           | 0.05 | 0.1  | 0.3  | V    |                   |
|                                                                                                                      |                 | $V_{DD} = 3.0\text{ V}$           | 0.2  | 0.5  | 1.0  | V    |                   |
|                                                                                                                      |                 | $V_{DD} = V_{DDH} = 5.0\text{ V}$ | 0.25 | 1.0  | 1.5  | V    |                   |
| Input Pin Capacitance<br>(P0.0 to P0.3)<br>(P1.0 to P1.3)<br>(P8.0 to P8.3)<br>(P9.0 to P9.3)<br>⋮<br>(PF.0 to PF.3) | $C_{IN}$        | —                                 | —    | —    | 5    | pF   |                   |

## Measuring circuit 1



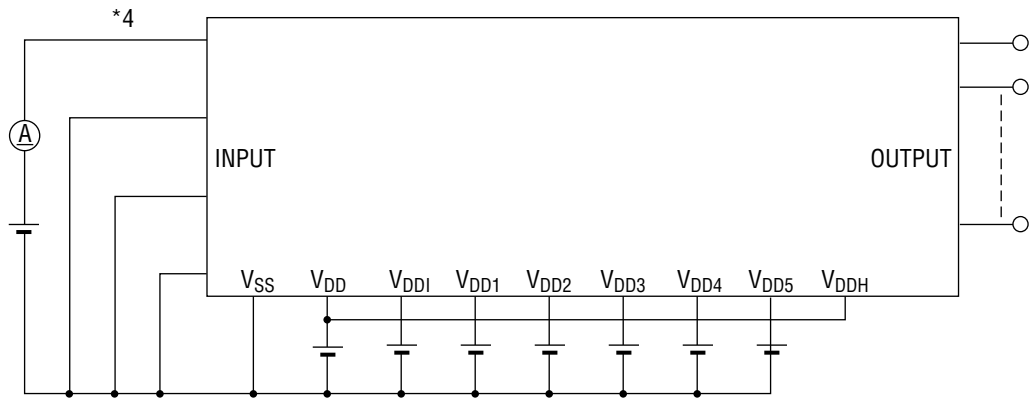
## Measuring circuit 2



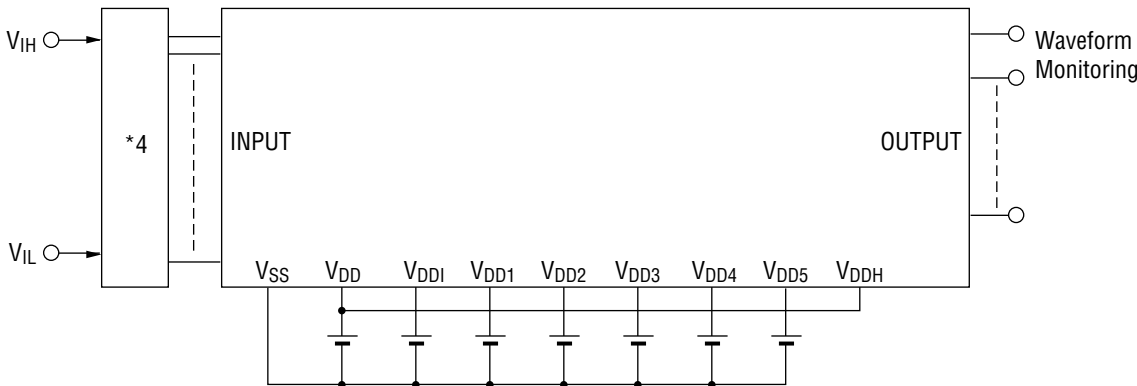
\*2 Input logic circuit to determine the specified measuring conditions.

\*3 Measured at the specified output pins.

Measuring circuit 3



Measuring circuit 4



\*4 Measured at the specified input pins.

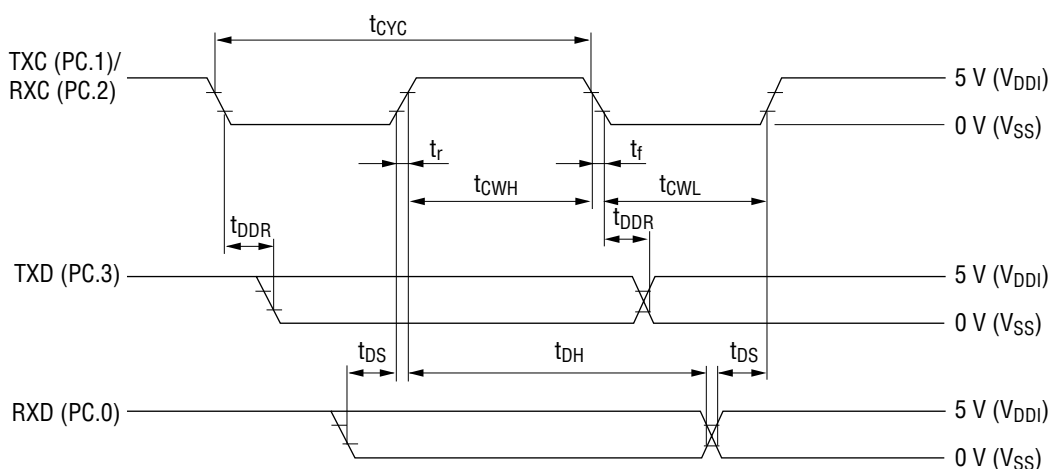
## AC Characteristics (Serial Interface, Serial Port)

( $V_{DD} = 1.45$  to  $5.5$  V,  $V_{DDH} = 2.7$  to  $5.5$  V,  $V_{SS} = 0$  V,  $V_{DDI} = 5.0$  V,  $T_a = 0$  to  $+65^\circ\text{C}$  unless otherwise specified)

### (1) Synchronous Communication

| Parameter                           | Symbol        | Condition                                                          | Min. | Typ. | Max. | Unit          |
|-------------------------------------|---------------|--------------------------------------------------------------------|------|------|------|---------------|
| TXC/RXC Input Fall Time             | $t_f$         | —                                                                  | —    | —    | 1.0  | $\mu\text{s}$ |
| TXC/RXC Input Rise Time             | $t_r$         | —                                                                  | —    | —    | 1.0  | $\mu\text{s}$ |
| TXC/RXC Input "L" Level Pulse Width | $t_{CWL}$     | —                                                                  | 0.8  | —    | —    | $\mu\text{s}$ |
| TXC/RXC Input "H" Level Pulse Width | $t_{CWH}$     | —                                                                  | 0.8  | —    | —    | $\mu\text{s}$ |
| TXC/RXC Input Cycle Time            | $t_{CYC}$     | —                                                                  | 2.0  | —    | —    | $\mu\text{s}$ |
| TXC/RXC Output Cycle Time           | $t_{CYC1(0)}$ | CPU in operation state at 32 kHz                                   | —    | 30.5 | —    | $\mu\text{s}$ |
|                                     | $t_{CYC2(0)}$ | CPU in operation at 2 MHz<br>$V_{DD} = V_{DDH} = 2.9$ V to $5.5$ V | —    | 0.5  | —    | $\mu\text{s}$ |
| TXD Output Delay Time               | $t_{DDR}$     | Output load capacitance 10 pF                                      | —    | —    | 0.4  | $\mu\text{s}$ |
| RXD Input Setup Time                | $t_{DS}$      | —                                                                  | 0.5  | —    | —    | $\mu\text{s}$ |
| RXD Input Hold Time                 | $t_{DH}$      | —                                                                  | 0.8  | —    | —    | $\mu\text{s}$ |

Synchronous communication timing  
("H" level = 4.0 V, "L" level = 1.0 V)



(2) UART Communication

| Parameter          | Symbol    | Condition                                     | Min.                  | Typ.      | Max.                  | Unit |
|--------------------|-----------|-----------------------------------------------|-----------------------|-----------|-----------------------|------|
| Transmit Baud Rate | $T_{BRT}$ | $T_{BRT} = 1/f_{BRT}$<br>$T_{CR} = 1/f_{OSC}$ | $T_{BRT} - T_{CR}$    | $T_{BRT}$ | $T_{BRT} + T_{CR}$    | s    |
| Receive Baud Rate  | $R_{BRT}$ | $R_{BRT} = 1/f_{BRT}$                         | $R_{BRT} \times 0.97$ | $R_{BRT}$ | $R_{BRT} \times 1.03$ | s    |

$f_{BRT}$ : Baud rates (1200, 2400, 4800, 9600 bps)

UART communication timing  
("H" level = 4.0 V, "L" level = 1.0 V)





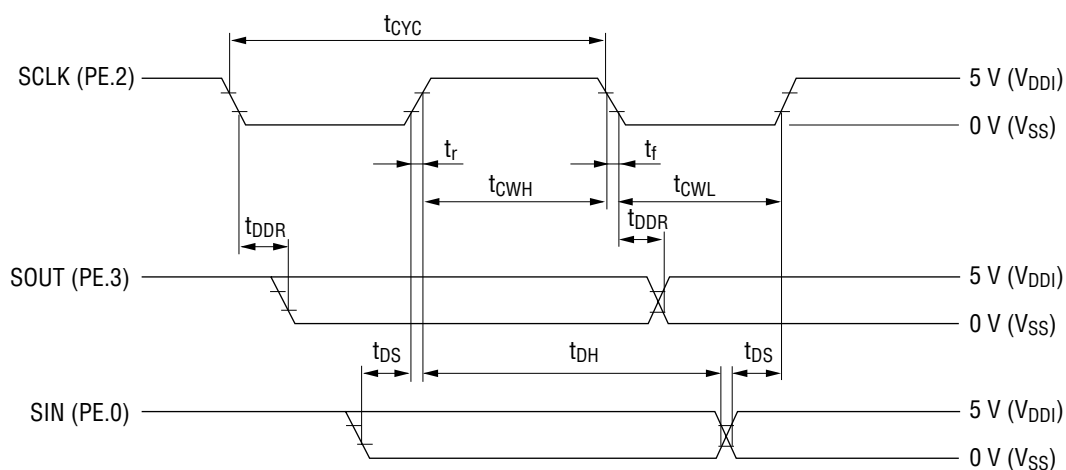
# AC Characteristics (Serial Interface, Shift Register)

( $V_{DD} = 1.45$  to  $5.5$  V,  $V_{DDH} = 2.7$  to  $5.5$  V,  $V_{SS} = 0$  V,  $V_{DDI} = 5.0$  V,  $T_a = 0$  to  $+65^{\circ}\text{C}$  unless otherwise specified)

| Parameter                        | Symbol        | Condition                                                          | Min. | Typ. | Max. | Unit          |
|----------------------------------|---------------|--------------------------------------------------------------------|------|------|------|---------------|
| SCLK Input Fall Time             | $t_f$         | —                                                                  | —    | —    | 1.0  | $\mu\text{s}$ |
| SCLK Input Rise Time             | $t_r$         | —                                                                  | —    | —    | 1.0  | $\mu\text{s}$ |
| SCLK Input "L" Level Pulse Width | $t_{CWL}$     | —                                                                  | 0.8  | —    | —    | $\mu\text{s}$ |
| SCLK Input "H" Level Pulse Width | $t_{CWH}$     | —                                                                  | 0.8  | —    | —    | $\mu\text{s}$ |
| SCLK Input Cycle Time            | $t_{CYC}$     | —                                                                  | 2.0  | —    | —    | $\mu\text{s}$ |
| SCLK Output Cycle Time           | $t_{CYC1(0)}$ | CPU in operation state at 32 kHz                                   | —    | 30.5 | —    | $\mu\text{s}$ |
|                                  | $t_{CYC2(0)}$ | CPU in operation at 2 MHz<br>$V_{DD} = V_{DDH} = 2.9$ V to $5.5$ V | —    | 0.5  | —    | $\mu\text{s}$ |
| SOUT Output Delay Time           | $t_{DDR}$     | $C_L = 10$ pF                                                      | —    | —    | 0.4  | $\mu\text{s}$ |
| SIN Input Setup Time             | $t_{DS}$      | —                                                                  | 0.5  | —    | —    | $\mu\text{s}$ |
| SIN Input Hold Time              | $t_{DH}$      | —                                                                  | 0.8  | —    | —    | $\mu\text{s}$ |

## AC characteristics timing

("H" level = 4.0 V, "L" level = 1.0 V)



## AC Characteristics (External Memory Interface)

( $V_{DD} = 1.45$  to  $5.5$  V,  $V_{DDH} = 2.7$  to  $5.5$  V,  $V_{SS} = 0$  V,  $V_{DDI} = 5.0$  V,  $T_a = 0$  to  $+65^{\circ}\text{C}$  unless otherwise specified)

### (1) Reading from External Memory

(a) When CPU operates at 32.768 kHz

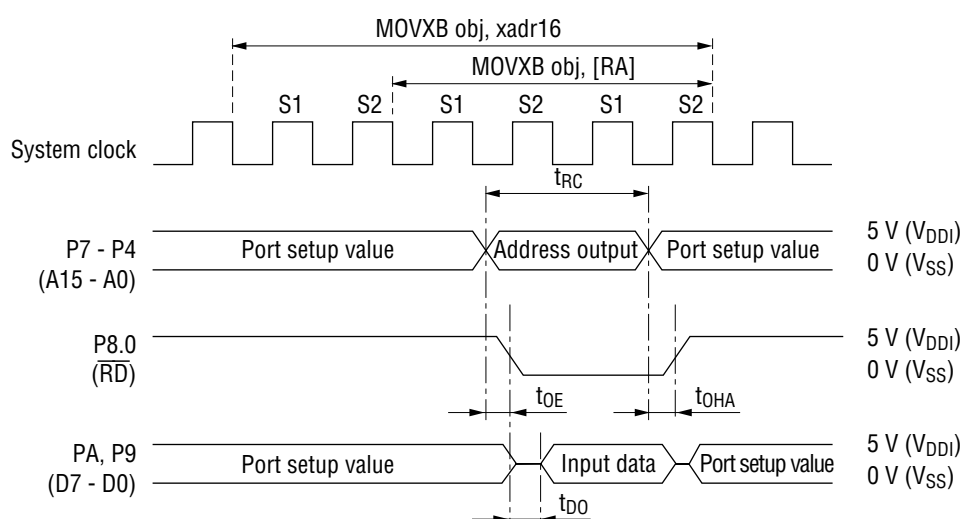
| Parameter                                | Symbol    | Condition | Min. | Typ. | Max. | Unit          |
|------------------------------------------|-----------|-----------|------|------|------|---------------|
| Read Cycle Time                          | $t_{RC}$  | —         | —    | 61.0 | —    | $\mu\text{s}$ |
| $\overline{\text{RD}}$ Output Delay Time | $t_{OE}$  | —         | —    | —    | 5.0  | $\mu\text{s}$ |
| Output Valid Time                        | $t_{OHA}$ | —         | —    | —    | 5.0  | $\mu\text{s}$ |
| External Memory Output Delay Time        | $t_{DO}$  | —         | —    | —    | 5.0  | $\mu\text{s}$ |

(b) When CPU operates at 2 MHz ( $V_{DDH} = 2.9$  to  $5.5$  V)

| Parameter                                | Symbol    | Condition | Min. | Typ. | Max. | Unit          |
|------------------------------------------|-----------|-----------|------|------|------|---------------|
| Read Cycle Time                          | $t_{RC}$  | —         | 1.0  | —    | —    | $\mu\text{s}$ |
| $\overline{\text{RD}}$ Output Delay Time | $t_{OE}$  | —         | —    | —    | 100  | ns            |
| Output Valid Time                        | $t_{OHA}$ | —         | —    | —    | 100  | ns            |
| External Memory Output Delay Time        | $t_{DO}$  | —         | —    | —    | 150  | ns            |

### AC characteristics timing

("H" level =  $4.0$  V, "L" level =  $1.0$  V)



## (2) Writing to External Memory

(a) When CPU operates at 32.768 kHz

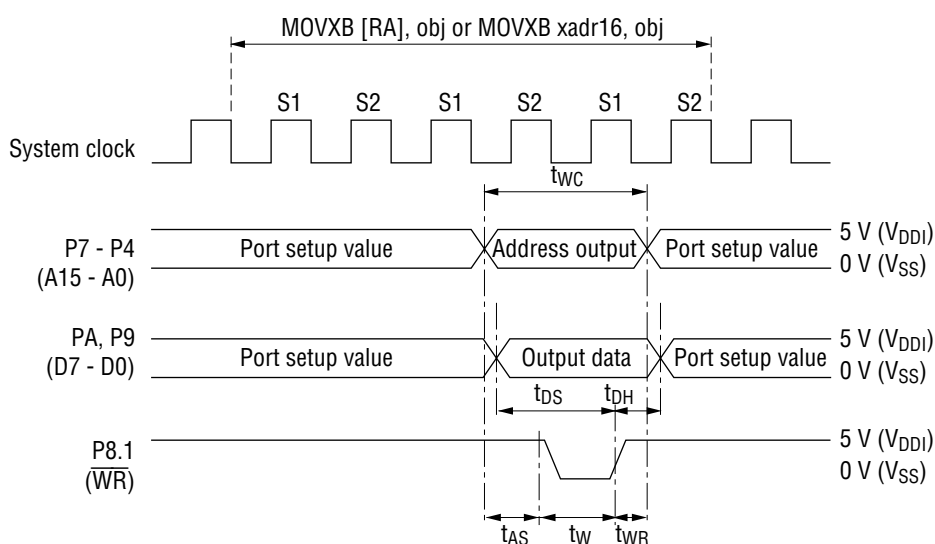
| Parameter           | Symbol   | Condition | Min. | Typ. | Max. | Unit    |
|---------------------|----------|-----------|------|------|------|---------|
| Write Cycle Time    | $t_{WC}$ | —         | —    | 61.0 | —    | $\mu s$ |
| Address Setup Time  | $t_{AS}$ | —         | —    | 30.5 | —    | $\mu s$ |
| Write Time          | $t_W$    | —         | —    | 15.3 | —    | $\mu s$ |
| Write Recovery Time | $t_{WR}$ | —         | —    | 15.3 | —    | $\mu s$ |
| Data Setup Time     | $t_{DS}$ | —         | —    | 45.8 | —    | $\mu s$ |
| Data Hold Time      | $t_{DH}$ | —         | —    | 15.3 | —    | $\mu s$ |

(b) When CPU operates at 2 MHz ( $V_{DDH} = 2.9$  to 5.5 V)

| Parameter           | Symbol   | Condition | Min. | Typ. | Max. | Unit    |
|---------------------|----------|-----------|------|------|------|---------|
| Write Cycle Time    | $t_{WC}$ | —         | 1.0  | —    | —    | $\mu s$ |
| Address Setup Time  | $t_{AS}$ | —         | 0.4  | —    | —    | $\mu s$ |
| Write Time          | $t_W$    | —         | 0.2  | —    | —    | $\mu s$ |
| Write Recovery Time | $t_{WR}$ | —         | 0.2  | —    | —    | $\mu s$ |
| Data Setup Time     | $t_{DS}$ | —         | 0.7  | —    | —    | $\mu s$ |
| Data Hold Time      | $t_{DH}$ | —         | 0.2  | —    | —    | $\mu s$ |

## AC characteristics timing

("H" level = 4.0 V, "L" level = 1.0 V)



(3) PROM Operations (Applies to Both the Cases of Using and Not Using Backup)

## ABSOLUTE MAXIMUM RATINGS

( $V_{SS} = 0\text{ V}$ )

| Parameter                 | Symbol    | Condition                                                         | Rating                 | Unit             |
|---------------------------|-----------|-------------------------------------------------------------------|------------------------|------------------|
| PROM Power Source Voltage | $V_{CC}$  | $V_{CC} = V_{DD} = V_{DDH} = V_{DDI}$<br>$T_a = 25^\circ\text{C}$ | -0.3 to +6.7           | V                |
| Program Voltage           | $V_{PP}$  | $T_a = 25^\circ\text{C}$                                          | -0.3 to +14.0          | V                |
| PROM Input Voltage        | $V_I$     | $V_{CC}$ input<br>$T_a = 25^\circ\text{C}$                        | -0.3 to $V_{CC} + 0.3$ | V                |
| PROM Output Voltage       | $V_O$     | $V_{CC}$ output<br>$T_a = 25^\circ\text{C}$                       | -0.3 to $V_{CC} + 0.3$ | V                |
| Storage Temperature       | $T_{STG}$ | —                                                                 | -55 to +150            | $^\circ\text{C}$ |

## RECOMMENDED OPERATING CONDITIONS

( $V_{SS} = 0\text{ V}$ )

| Parameter                     | Symbol     | Condition            | Range           | Unit             |
|-------------------------------|------------|----------------------|-----------------|------------------|
| Operating Temperature         | $T_{OPEP}$ | —                    | 0 to +65        | $^\circ\text{C}$ |
| $V_{CC}$ Power Supply Voltage | $V_{CC}$   | —                    | 4.75 to 5.25    | V                |
| $V_{PP}$ Power Supply Voltage | $V_{PP}$   | When data is read    | 4.75 to 5.25    | V                |
|                               |            | When data is written | 12.0 to 13.5    | V                |
| Input Voltage                 | $V_{IH}$   | —                    | 4.0 to $V_{CC}$ | V                |
|                               | $V_{IL}$   | —                    | 0 to 1.0        | V                |

## ELECTRICAL CHARACTERISTICS

### (1) Read Operation

#### DC Characteristics

( $V_{CC} = V_{PP} = 5\text{ V} \pm 5\%$ ,  $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$  unless otherwise specified)

| Parameter                                 | Symbol    | Condition                        | Min. | Typ. | Max.     | Unit |
|-------------------------------------------|-----------|----------------------------------|------|------|----------|------|
| $V_{CC}$ Power Supply Current (Standby)   | $I_{CC1}$ | $\overline{CE} = V_{IH}$         | —    | —    | 35       | mA   |
| $V_{CC}$ Power Supply Current (Operating) | $I_{CC2}$ | $\overline{CE} = V_{IL}$         | —    | —    | 100      | mA   |
| Input Voltage                             | $V_{IH}$  | —                                | 4.0  | —    | $V_{CC}$ | V    |
|                                           | $V_{IL}$  | —                                | 0    | —    | 1.0      | V    |
| Output Current                            | $I_{OH}$  | $V_{OH} = V_{CC} - 0.5\text{ V}$ | -8   | -4   | -2       | mA   |
|                                           | $I_{OL}$  | $V_{OL} = 0.5\text{ V}$          | 2    | 4    | 8        | mA   |

#### AC Characteristics

( $V_{CC} = 5\text{ V} \pm 5\%$ ,  $V_{PP} = V_{CC}$ ,  $T_a = 0\text{ to }+65^\circ\text{C}$  unless otherwise specified)

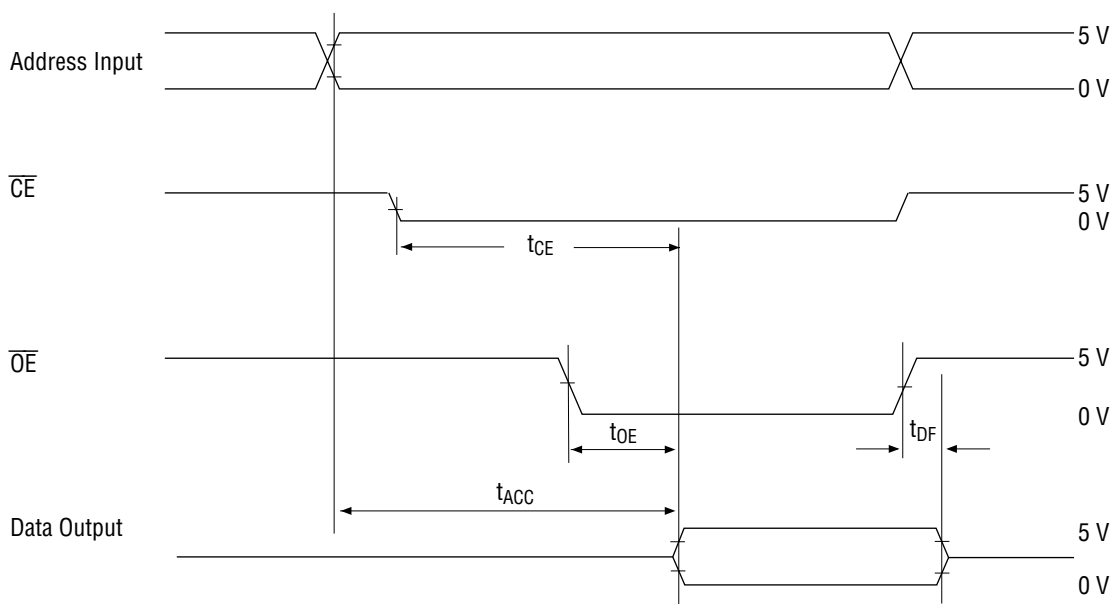
| Parameter                   | Symbol    | Condition                                | Min. | Typ. | Max. | Unit |
|-----------------------------|-----------|------------------------------------------|------|------|------|------|
| Address Access Time         | $t_{ACC}$ | $\overline{OE} = \overline{CE} = V_{IL}$ | —    | —    | 120  | ns   |
| $\overline{CE}$ Access Time | $t_{CE}$  | $\overline{OE} = V_{IL}$                 | —    | —    | 120  | ns   |
| $\overline{OE}$ Access Time | $t_{OE}$  | $\overline{CE} = V_{IL}$                 | —    | —    | 50   | ns   |
| Output Disable Time         | $t_{DF}$  | $\overline{CE} = V_{IL}$                 | 0    | —    | 40   | ns   |

Measurement conditions:

Input pulse level ..... 0.45 V to 4.55 V

Input rise/fall time ..... 5 ns

Threshold level ..... input 0.8 V, 2 V/output 0.8 V, 2 V



## (2) Write Operation

**DC Characteristics**(V<sub>SS</sub> = 0 V, V<sub>CC</sub> = 5 V ±5%, V<sub>PP</sub> = 12.5 V ±0.5 V, T<sub>a</sub> = 25°C ±5°C unless otherwise specified)

| Parameter                            | Symbol          | Condition                                 | Min. | Typ. | Max.            | Unit |
|--------------------------------------|-----------------|-------------------------------------------|------|------|-----------------|------|
| V <sub>PP</sub> Power Supply Current | I <sub>PP</sub> | $\overline{CE} = V_{IH}$                  | —    | —    | 50              | mA   |
| V <sub>CC</sub> Power Supply Current | I <sub>CC</sub> | —                                         | —    | —    | 100             | mA   |
| Input Voltage                        | V <sub>IH</sub> | —                                         | 4.0  | —    | V <sub>CC</sub> | V    |
|                                      | V <sub>IL</sub> | —                                         | 0    | —    | 1.0             | V    |
| Output Current                       | I <sub>OH</sub> | V <sub>OH</sub> = V <sub>CC</sub> − 0.5 V | −8   | −4   | −2              | mA   |
|                                      | I <sub>OL</sub> | V <sub>OL</sub> = 0.5 V                   | 2    | 4    | 8               | mA   |

**AC Characteristics**(V<sub>SS</sub> = 0 V, V<sub>CC</sub> = 5 V ±5%, V<sub>PP</sub> = 12.5 V ±0.5 V, T<sub>a</sub> = 25°C ±5°C unless otherwise specified)

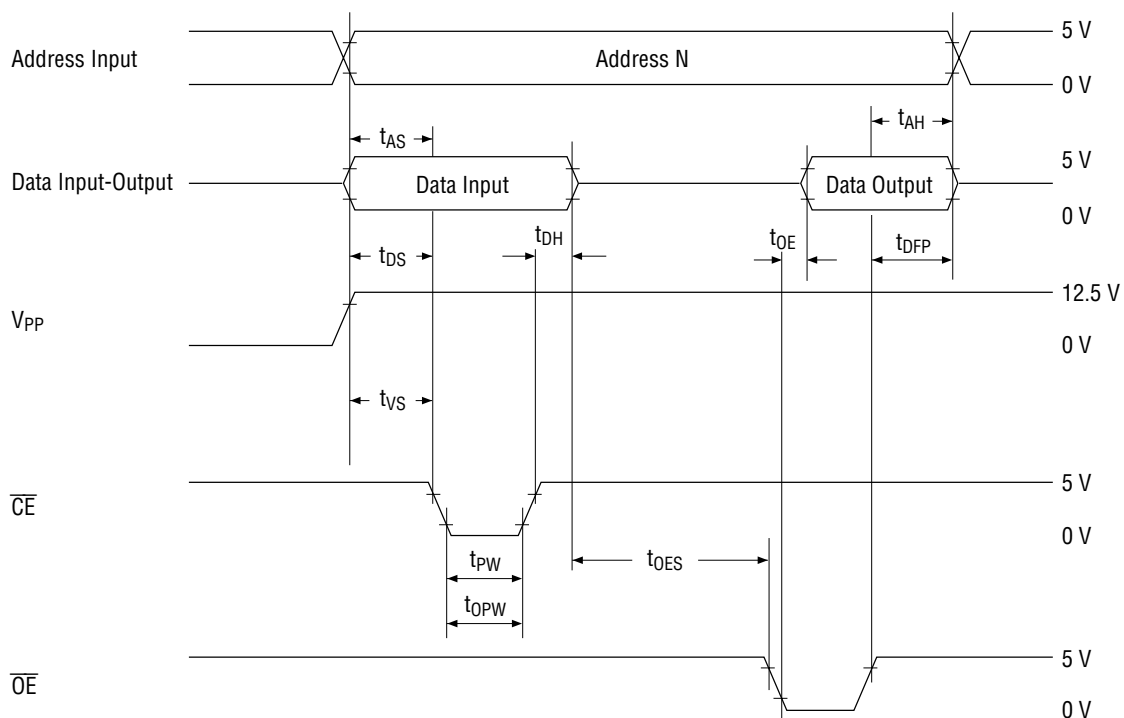
| Parameter                                   | Symbol           | Condition   | Min. | Typ. | Max.  | Unit |
|---------------------------------------------|------------------|-------------|------|------|-------|------|
| Address Setup Time                          | t <sub>AS</sub>  | —           | 2.0  | —    | —     | μs   |
| $\overline{OE}$ Setup Time                  | t <sub>OES</sub> | —           | 2.0  | —    | —     | μs   |
| Data Setup Time                             | t <sub>DS</sub>  | —           | 2.0  | —    | —     | μs   |
| Address Hold Time                           | t <sub>AH</sub>  | —           | 0    | —    | —     | μs   |
| Data Hold Time                              | t <sub>DH</sub>  | —           | 2.0  | —    | —     | μs   |
| $\overline{OE}$ Output Floating Delay Time  | t <sub>DFP</sub> | —           | 0    | —    | 130   | ns   |
| V <sub>PP</sub> Power Source Setup Time     | t <sub>VS</sub>  | —           | 2.0  | —    | —     | μs   |
| Initial Program Pulse Width                 | t <sub>PW</sub>  | 6 V ±0.25 V | 0.95 | 1.0  | 1.05  | ms   |
| Additional Program Pulse Width              | t <sub>OPW</sub> | 6 V ±0.25 V | 2.85 | —    | 78.75 | ms   |
| $\overline{OE}$ Output Effective Delay Time | t <sub>OE</sub>  | —           | —    | —    | 150   | ns   |

Measurement conditions:

Input pulse level ..... 0.45 V to 4.55 V

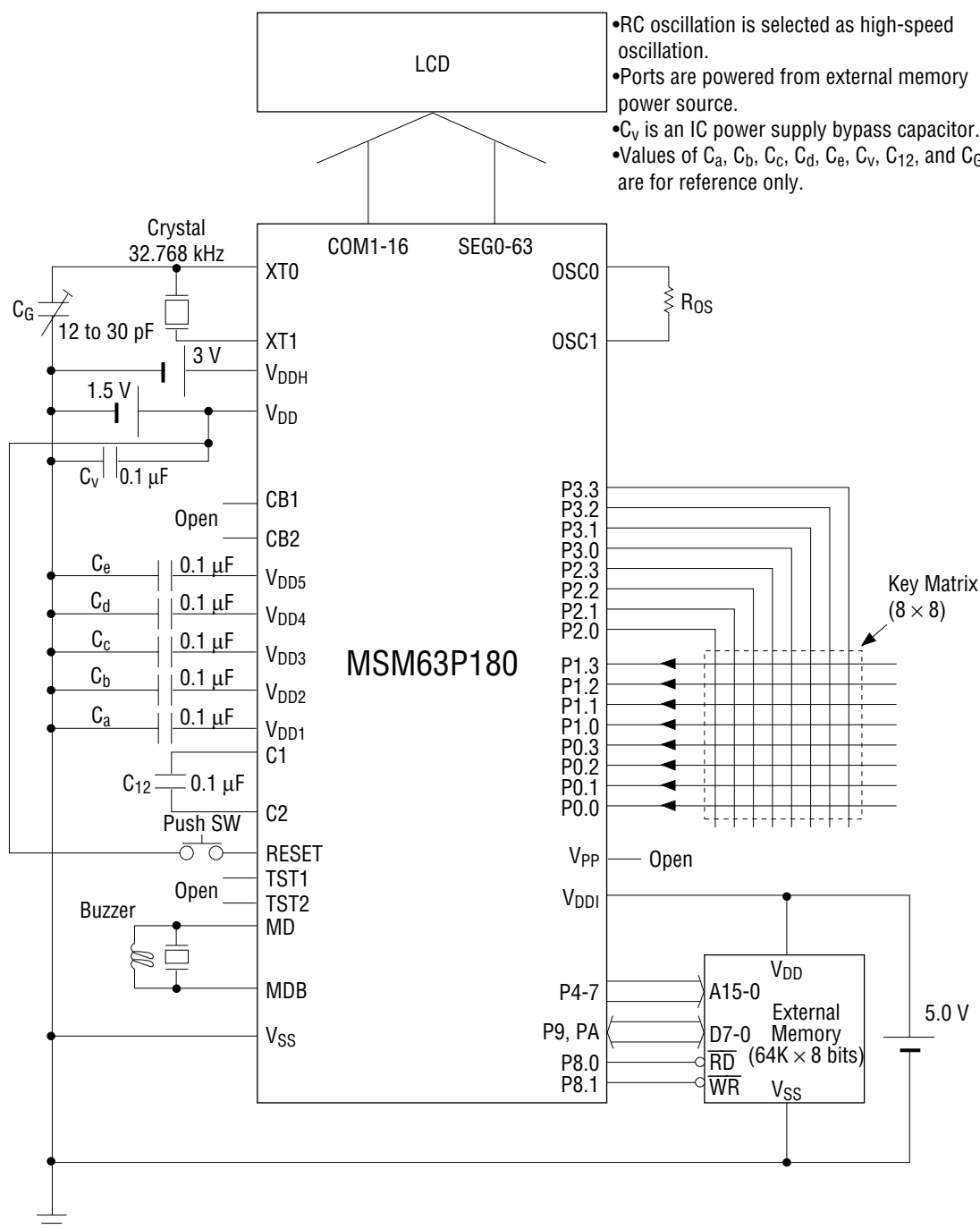
Input rise/fall time ..... less than 20 ns

Threshold level ..... input 0.8 V, 2 V/output 0.8 V, 2 V





## APPLICATION CIRCUITS

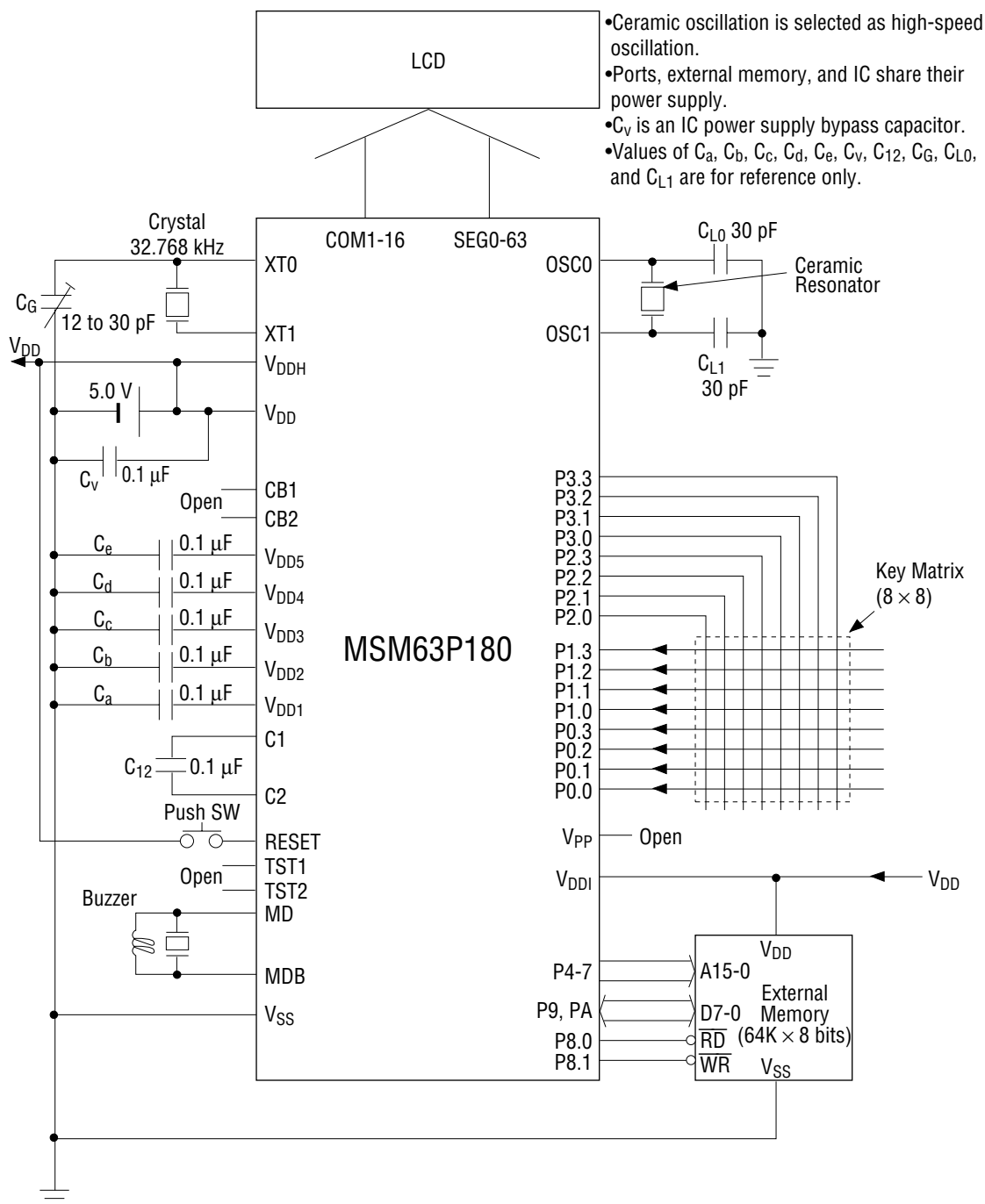


- RC oscillation is selected as high-speed oscillation.
- Ports are powered from external memory power source.
- $C_V$  is an IC power supply bypass capacitor.
- Values of  $C_a$ ,  $C_b$ ,  $C_c$ ,  $C_d$ ,  $C_e$ ,  $C_V$ ,  $C_{12}$ , and  $C_G$  are for reference only.

Note:  $V_{DDI}$  is the power supply pin for the input, output, and input-output ports. Be sure to connect the  $V_{DDI}$  pin either to the positive power supply pin ( $V_{DD}$ ) of this device or to the positive power supply pin of the external memory.

### Application Circuit Example with Power Supply Backup

# APPLICATION CIRCUITS (continued)



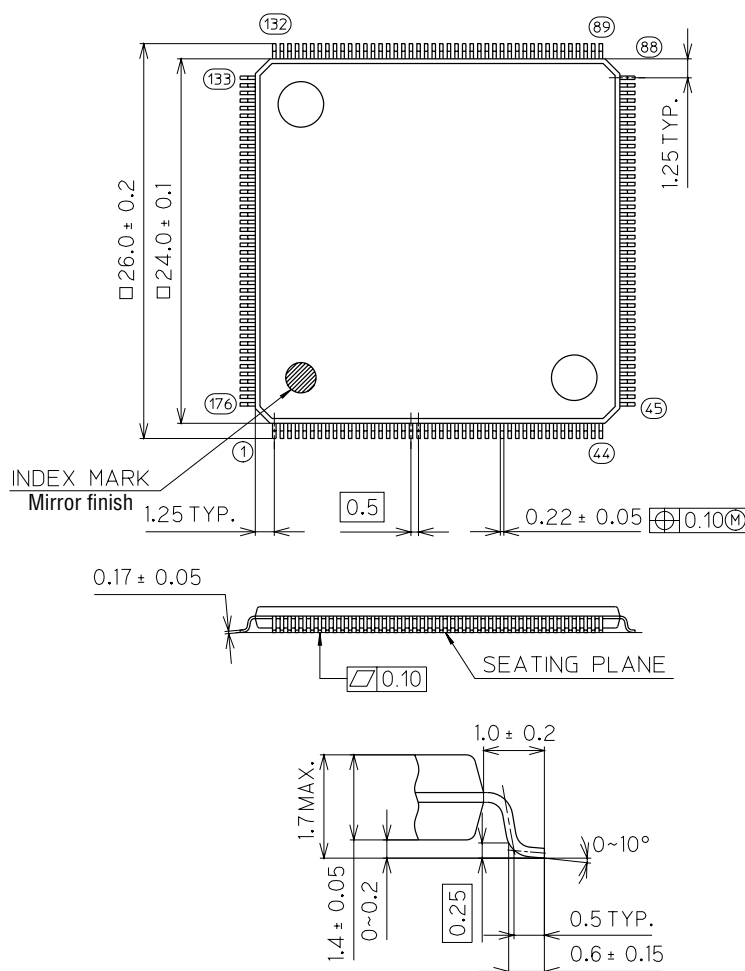
Note:  $V_{DDI}$  is the power supply pin for the input, output, and input-output ports. Be sure to connect the  $V_{DDI}$  pin either to the positive power supply pin ( $V_{DD}$ ) of this device or to the positive power supply pin of the external memory.

## Application Circuit Example with No Power Supply Backup

## PACKAGE DIMENSIONS

(Unit : mm)

LQFP176-P-2424-0.50-BK



|                        |                         |
|------------------------|-------------------------|
| Package material       | Epoxy resin             |
| Lead frame material    | 42 alloy                |
| Pin treatment          | Solder plating          |
| Solder plate thickness | 5 $\mu\text{m}$ or more |
| Package weight (g)     | 1.87 TYP.               |

## Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).