CS8240

500 mA High Side (PNP) Driver with On-Chip Flyback Diode

The CS8240 is a fast, PNP high side driver capable of delivering up to 500 mA into a resistive or inductive load in harsh automotive or industrial environments. An internal flyback diode clamp is incorporated for inductive loads. The input (V_{IN}) is TTL and CMOS compatible and has hysteresis to minimize the effects of noise. When the input is high, the output is on. When the input is low, the output is off and the supply voltage quiescent current is very low (< 1.0 μA, typ). For device protection, the CS8240 incorporates thermal shutdown, short circuit current limiting, overvoltage shutdown, and reverse battery protection. The CS8240 can withstand supply voltage transients of 60 V (min) and –50 V.

The CS8240 is available in an overmolded 5 lead TO–220 package and is a competitive replacement for the LM–1921, LM–1951, LM–1952, MC–3399, and L–9350.

Features

- Low Output Saturation Voltage
  - 0.22 V at I_{OUT} = 125 mA
  - 0.33 V at I_{OUT} = 225 mA
- Overmolded Package
- On–Chip Flyback Diode
- Fault Protection
  - Over Voltage Shutdown (32 V, typ)
  - Thermal Shutdown (165°C, typ)
  - Short Circuit Limiting (1.1 A typ)
  - –50 V Reverse Transient Protection
  - 60 V Load Dump Protection
  - Reverse Battery
- Low Quiescent Current (Off State)
- ESD Protected

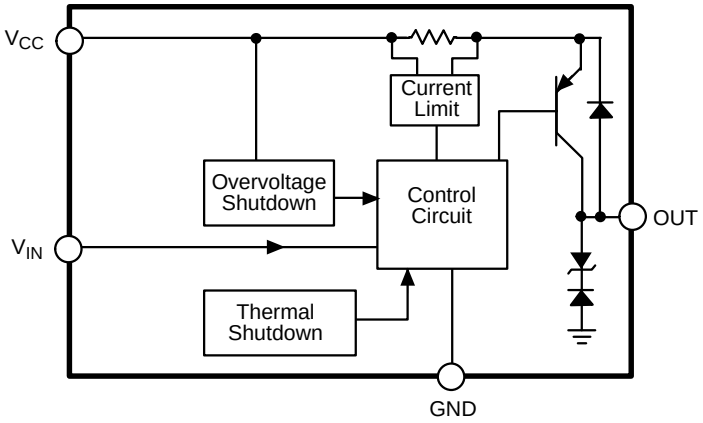

Figure 1. Block Diagram

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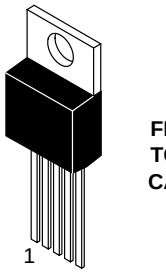
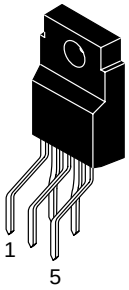


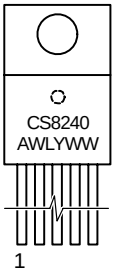
TO–220
FIVE LEAD
TQ SUFFIX
CASE 314D



TO–220
FIVE LEAD
TQVA SUFFIX
CASE 314N

Pin 1. V_{CC}
2. OUT
3. NC
4. GND
5. V_{IN}

MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
CS8240YTQ5	TO–220 FIVE LEAD STRAIGHT	50 Units/Rail
CS8240YTQVA5	TO–220 FIVE LEAD VERTICAL	50 Units/Rail

MAXIMUM RATINGS*

Rating		Value	Unit
Supply Voltage		6.0 to 26	V
Overvoltage Protection		60	V
Reverse Voltage:	DC Transient	–16 –50	V V
Internal Power Dissipation		Internally limited	–
Logic Input Voltage		–0.3 to +7.0	V
Junction Temperature Range, T_J		–40 to150	°C
Storage Temperature Range, T_S		–55 to +165	°C
Lead Temperature Soldering:	Wave Solder (through hole styles only) (Note 1)	260 peak	°C
Electrostatic Discharge (Human Body Model)		2.0	kV

1. 10 second maximum.

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ($-40°C \le T_A \le 125°C$; $-40°C \le T_J \le 150°C$, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
General Characteristics					
Operating Supply Voltage	–	6.0	–	–	V
Quiescent Current	V_{CC} = 12V, $V_{IN} \le V_{IN(LOW)}$ $V_{IN} \ge V_{IN(HI)}$, R_{LOAD} = 50 Ω, 6.0 V ≤ V_{CC} ≤ 20 V 20 V ≤ V_{CC} ≤ 24 V	– – –	1.0 16 25	100 30 50	μA mA mA
Output Stage					
Output Saturation Voltage	$V_{IN} \le V_{IN(HI)}$, V_{CC} = 6.0 V, I_{LOAD} = 125 mA V_{CC} = 14 V, I_{LOAD} = 225 mA	– –	0.22 0.33	0.5 0.7	V V
Output Leakage Current	Input ≤ $V_{IN(L)}$, V_{CC} = 12 V, V_{OUT} = 0 V	–	1.0	150	μA
Negative Output Clamp	I_{CLAMP} = 100 mA, V_{CC} = 12 V	–18	–15.5	–12	V
Turn On Delay Time	V_{CC} = 12 V, I_{LOAD} = 150 mA	–	5.0	20	μs
Turn Off Delay Time	V_{CC} = 12 V, I_{LOAD} = 150 mA	–	5.0	20	μs
Input Stage					
Input Voltage	Logic = High, V_{CC} = 12 V Turn ON Logic = Low, V_{CC} = 12 V Turn OFF	0.8 –	1.45 1.2	– 2.0	V V
Input Current	V_{IN} = 5.5 V V_{IN} = 0.8 V	– –	100 15	200 50	μA μA
Protection Circuitry					
Overvoltage Shutdown	$V_{IN} \ge V_{IN(HI)}$	26	32	–	V
Output Short Circuit Current	$V_{IN} \ge V_{IN(HI)}$, V_{CC} = 12 V, V_{OUT} = 0 V	0.55	1.1	2.5	A
Thermal Shutdown	–	150	165	–	°C

PACKAGE PIN DESCRIPTION

PACKAGE PIN # 5 Lead TO–220	PIN SYMBOL	FUNCTION
1	V_{CC}	Supply Voltage to the IC. Supplies load current through PNP.
2	OUT	Collector of output PNP, current to load is sourced from this lead.
3	NC	No connection.
4	GND	Ground.
5	V_{IN}	Input voltage to control output. Logic high turns output on. Logic low turns output off.

TYPICAL PERFORMANCE CHARACTERISTICS

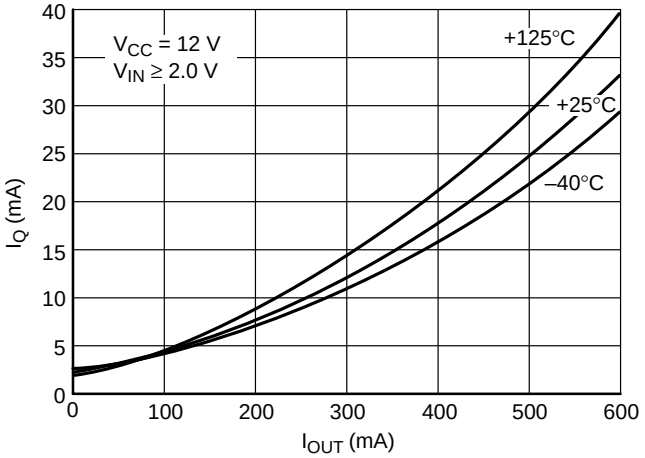


Figure 2. Quiescent Current vs. I_{OUT}

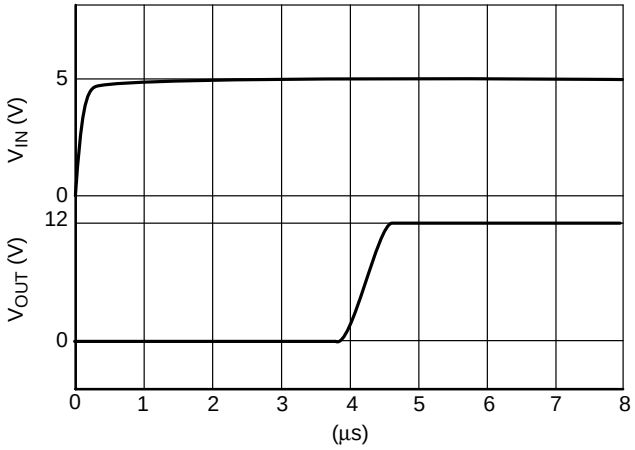


Figure 3. Turn–On Delay Time

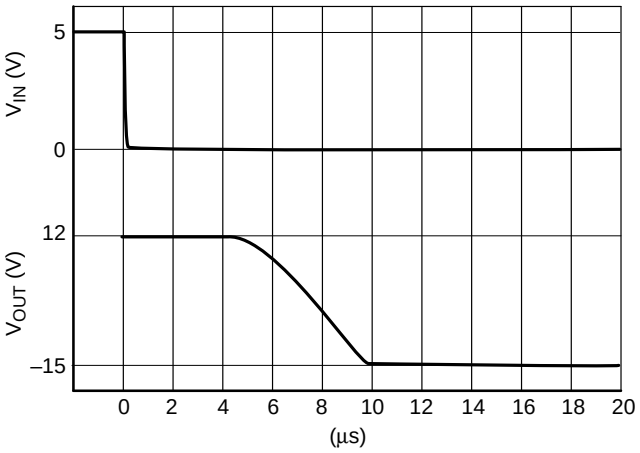


Figure 4. Turn Off Delay Time

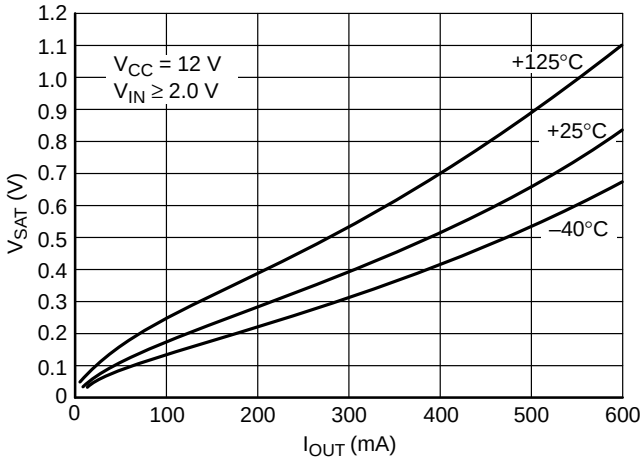


Figure 5. Output Saturation Voltage vs. I_{OUT}

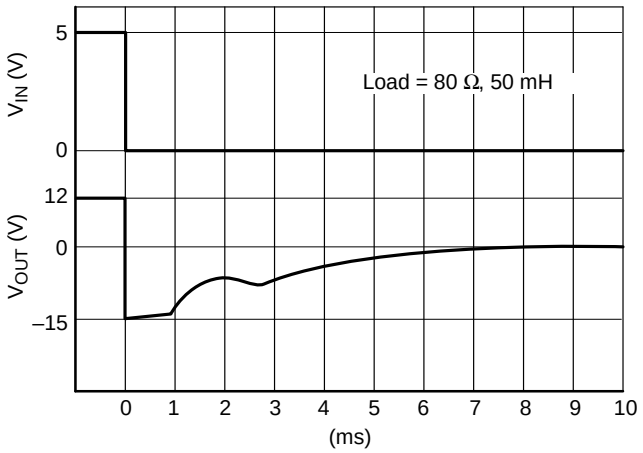


Figure 6. Flyback Clamp Characteristics

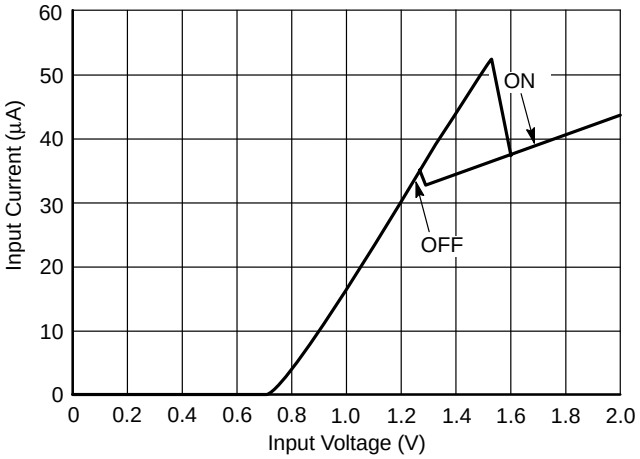


Figure 7. I_{IN} vs. V_{IN}

CIRCUIT DESCRIPTION

Input Stage

The input stage is a self biased band gap based circuit with a positive going trip point of 1.45 V (typ) and a negative going trip point of 1.20 V (typ) (250 mV of hysteresis). When the input voltage is below the positive trip point, the quiescent current of the supply voltage line is less than 1.0 μA, (typ). When the input voltage exceeds the positive trip point (1.45 V, typ), the input stage “wakes up” the rest of the CS8240 circuitry and turns on the output stage.

Output Stage

The output stage is built around a high current PNP output transistor. A control amplifier monitors the saturation voltage of the output PNP and maintains a balance of low saturation voltage and minimum base drive to the PNP for the given output current. The base drive of the PNP is the dominant component of the quiescent current of the CS8240 and is dependent on the level of output current.

Short circuit protection (1.1 A, typ) is also incorporated in the output stage.

Protection Circuitry

In addition to the short circuit protection mentioned above, the CS8240 also incorporates a thermal shutdown circuit (165°C, typ) and a high voltage shutdown circuit (33 V, typ), both of which cut off the drive to the PNP output transistor when excessive current is drawn. Inherent in the design of the CS8240 is transient protection to +60 V and –50 V on the supply line. The CS8240 is ESD protected in excess of 2.0 kV (Human Body Model).

TYPICAL APPLICATION CIRCUITS

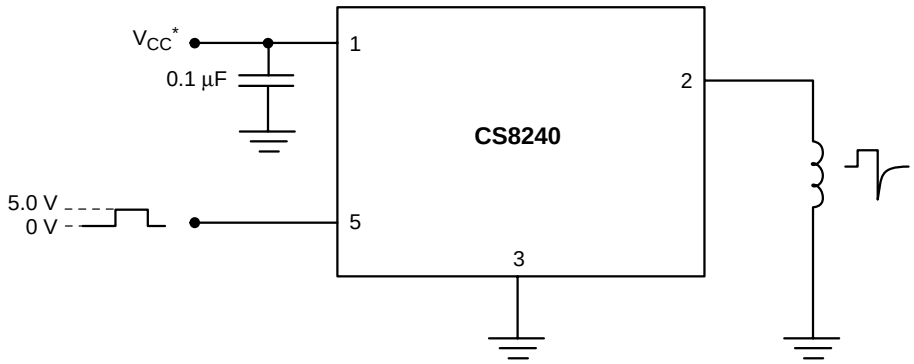


Figure 8. Solenoid Driver

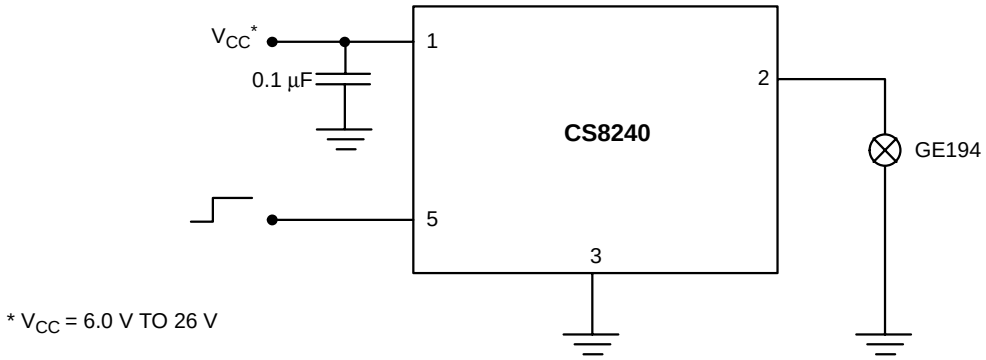


Figure 9. Lamp Driver

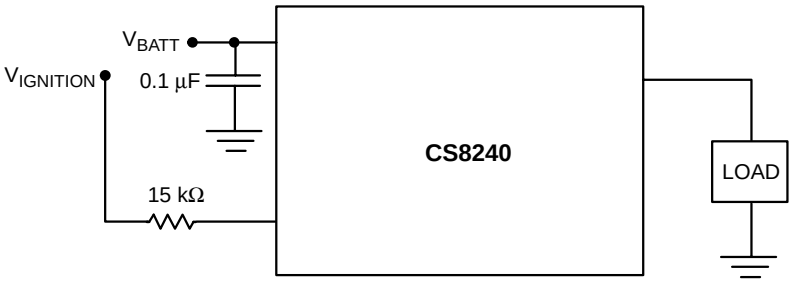
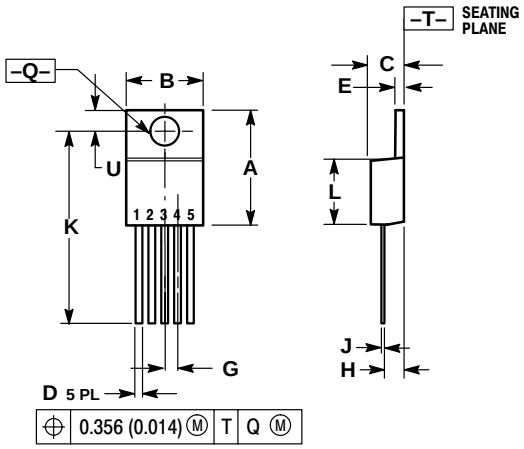


Figure 10. Controlled High Side Switch

PACKAGE DIMENSIONS

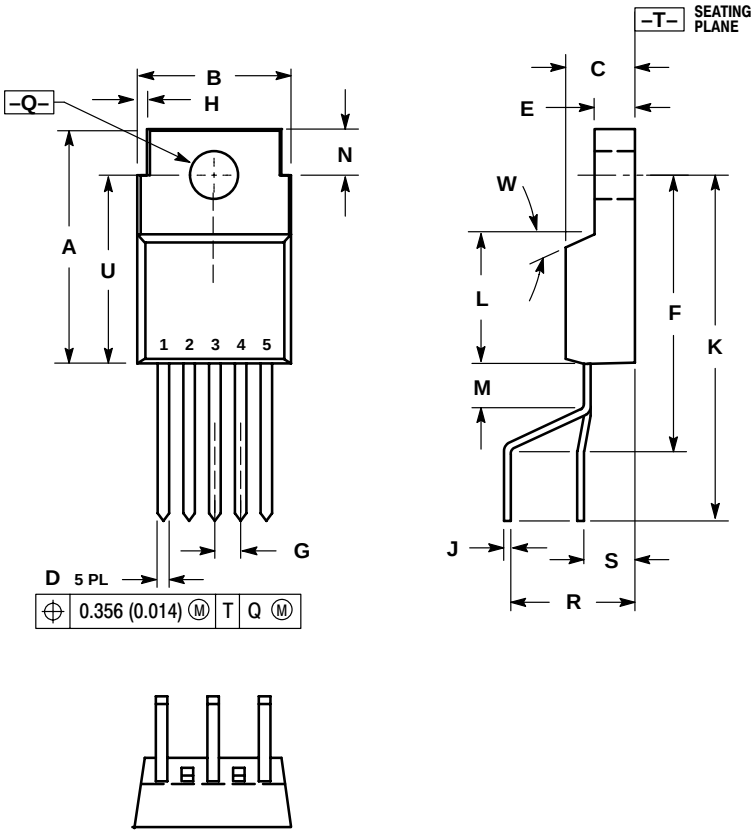
TO–220
FIVE LEAD
TQ SUFFIX
CASE 314D–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
G	0.067 BSC		1.702 BSC	
H	0.087	0.112	2.210	2.845
J	0.015	0.025	0.381	0.635
K	0.990	1.045	25.146	26.543
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
U	0.105	0.117	2.667	2.972

TO–220
FIVE LEAD
TQVA SUFFIX
CASE 314N–01
ISSUE O



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3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.
4. LEADS MAINTAIN A RIGHT ANGLE WITH RESPECT TO THE PACKAGE BODY TO WITHIN ± 0.015 ".

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.604	0.614	15.34	15.60
B	0.395	0.405	10.03	10.29
C	0.175	0.185	4.44	4.70
D	0.027	0.037	0.69	0.94
E	0.100	0.110	2.54	2.79
F	0.712	0.727	18.08	18.47
G	0.067 BSC		1.70 BSC	
H	0.020	0.030	0.51	0.76
J	0.014	0.022	0.36	0.56
K	0.889	0.904	22.58	22.96
L	0.324	0.339	8.23	8.61
M	0.115	0.130	2.92	3.30
N	0.115	0.125	2.92	3.17
Q	0.120	0.130	3.05	3.30
R	0.292	0.342	7.42	8.69
S	0.133	0.183	3.38	4.65
U	0.480	0.495	12.19	12.57
W	5 °		5 °	

PACKAGE THERMAL DATA

Parameter		TO−220, Five Lead	Unit
$R_{\Theta JC}$	Typical	4.0	°C/W
$R_{\Theta JA}$	Typical	50	°C/W

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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