DTC114E SERIES

Preferred Devices

Bias Resistor Transistor

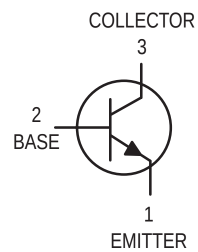
NPN Silicon Surface Mount Transistor with Monolithic Bias Resistor Network

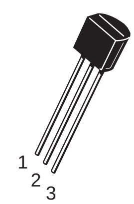
This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base–emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the TO–92 package which is designed for through hole applications.

ON Semiconductor

http://onsemi.com

NPN SILICON BIAS RESISTOR TRANSISTOR





CASE 29
TO–92 (TO–226)
STYLE 1

Preferred devices are recommended choices for future use and best overall value.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc
Total Power Dissipation @ T_A = 25°C (1.) Derate above 25°C	P_D	 350 2.81	 mW mW/°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Ambient (surface mounted)	$R_{\theta JA}$	357	°C/W
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to +150	°C
Maximum Temperature for Soldering Purposes, Time in Solder Bath	T_L	260 10	°C Sec

DEVICE MARKING AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Shipping
DTC114E	DTC114E	10	10	5000/Box
DTC124E	DTC124E	22	22	
DTC144E	DTC144E	47	47	
DTC114Y	DTC114Y	10	47	
DTC114T	DTC114T	10	∞	
DTC143T	DTC143T	4.7	∞	
DTD113E	DTD113E	1.0	1.0	
DTC123E	DTC123E	2.2	2.2	
DTC143E	DTC143E	4.7	4.7	
DTC143Z	DTC143Z	4.7	47	

1. Device mounted on a FR–4 glass epoxy printed circuit board using the minimum recommended footprint.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Base Cutoff Current (V_{CB} = 50 V, I_E = 0)		I_{CBO}	—	—	100	nAdc
Collector–Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)		I_{CEO}	—	—	500	nAdc
Emitter–Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0)	DTC114E	I_{EBO}	—	—	0.5	mAdc
	DTC124E		—	—	0.2	
	DTC144E		—	—	0.1	
	DTC114Y		—	—	0.2	
	DTC114T		—	—	0.9	
	DTC143T		—	—	1.9	
	DTD113E		—	—	4.3	
	DTC123E		—	—	2.3	
	DTC143E		—	—	1.5	
	DTC143Z		—	—	0.18	
Collector–Base Breakdown Voltage (I_C = 10 µA, I_E = 0)		$V_{(BR)CBO}$	50	—	—	Vdc
Collector–Emitter Breakdown Voltage (2.) (I_C = 2.0 mA, I_B = 0)		$V_{(BR)CEO}$	50	—	—	Vdc
ON CHARACTERISTICS (2.)						
DC Current Gain (V_{CE} = 10 V, I_C = 5.0 mA)	DTC114E	h_{FE}	35	60	—	
	DTC124E		60	100	—	
	DTC144E		80	140	—	
	DTC114Y		80	140	—	
	DTC114T		160	350	—	
	DTC143T		160	350	—	
	DTD113E		3.0	5.0	—	
	DTC123E		8.0	15	—	
	DTC143E		15	30	—	
	DTC143Z		80	200	—	
Collector–Emitter Saturation Voltage (I_C = 10 mA, I_E = 0.3 mA) DTC144E/DTC114Y DTD113E/DTC143E (I_C = 10 mA, I_B = 5 mA) DTC123E (I_C = 10 mA, I_B = 1 mA) DTC114T/DTC143T/ DTC143Z/DTC124E		$V_{CE(sat)}$	—	—	0.25	Vdc
Output Voltage (on)		V_{OL}				Vdc
(V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	DTC114E		—	—	0.2	
	DTC124E		—	—	0.2	
	DTC114Y		—	—	0.2	
	DTC114T		—	—	0.2	
	DTC143T		—	—	0.2	
	DTD113E		—	—	0.2	
	DTC123E		—	—	0.2	
	DTC143E		—	—	0.2	
	DTC143Z		—	—	0.2	
(V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kΩ)	DTC144E		—	—	0.2	

2. Pulse Test: Pulse Width < 300 µs, Duty Cycle < 2.0%

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Voltage (off)		V_{OH}	4.9	—	—	Vdc
(V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)	DTC114E DTC124E DTC144E DTC114Y DTC123E DTC143E					
(V_{CC} = 5.0 V, V_B = 0.05 V, R_L = 1.0 kΩ)	DTD113E					
(V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ)	DTC114T DTC143T DTC143Z					
Input Resistor	DTC114E	R1	7.0	10	13	kΩ
	DTC124E		15.4	22	28.6	
	DTC144E		32.9	47	61.1	
	DTC114Y		7.0	10	13	
	DTC114T		7.0	10	13	
	DTC143T		3.3	4.7	6.1	
	DTD113E		0.7	1.0	1.3	
	DTC123E		1.5	2.2	2.9	
	DTC143E		3.3	4.7	6.1	
	DTC143Z		3.3	4.7	6.1	
Resistor Ratio	DTC114E/DTC124E/DTC144E	R_1/R_2	0.8	1.0	1.2	
	DTC114Y		0.17	0.21	0.25	
	DTC114T/DTC143T		—	—	—	
	DTD113E/DTC123E/DTC143E		0.8	1.0	1.2	
	DTC143Z		0.055	0.1	0.185	

TYPICAL ELECTRICAL CHARACTERISTICS
DTC114E

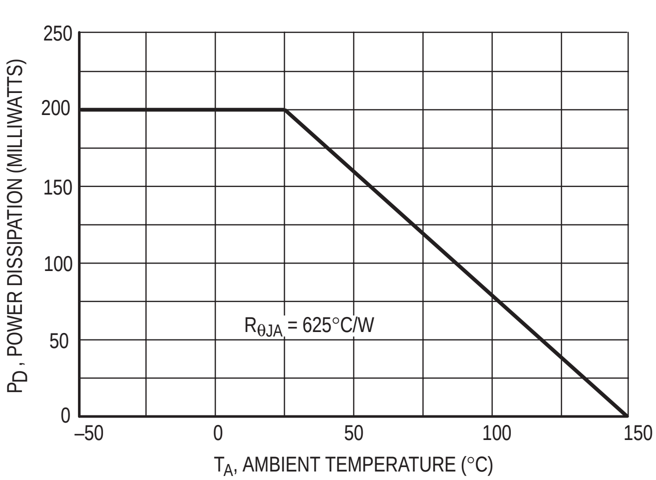


Figure 1. Derating Curve

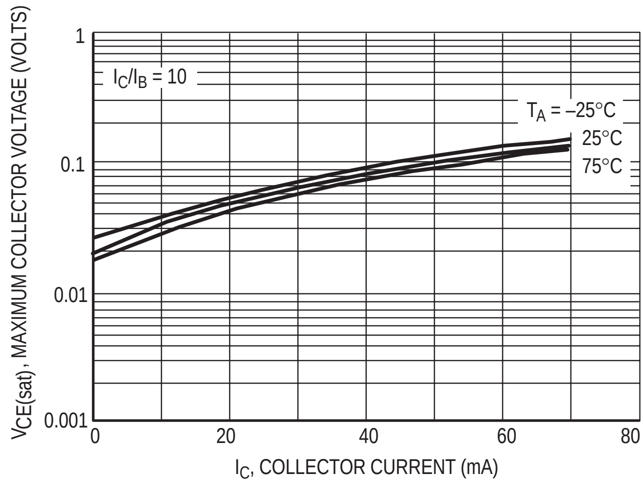


Figure 2. $V_{CE(sat)}$ versus I_C

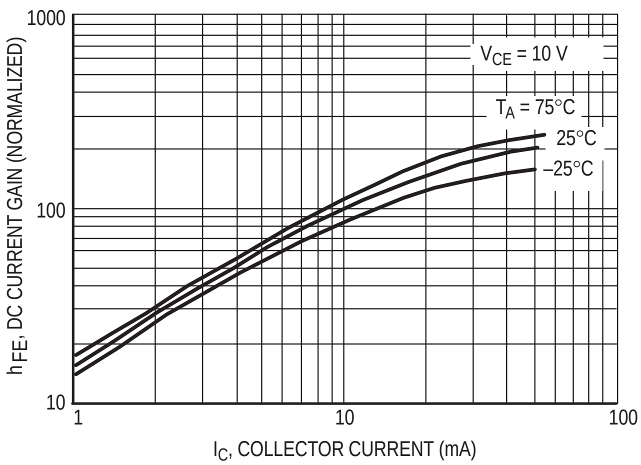


Figure 3. DC Current Gain

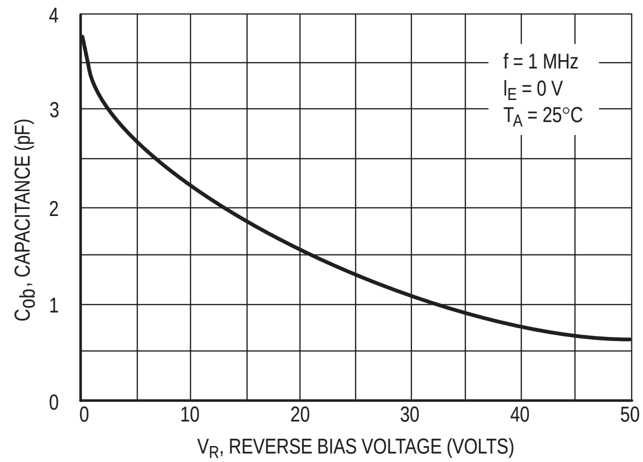


Figure 4. Output Capacitance

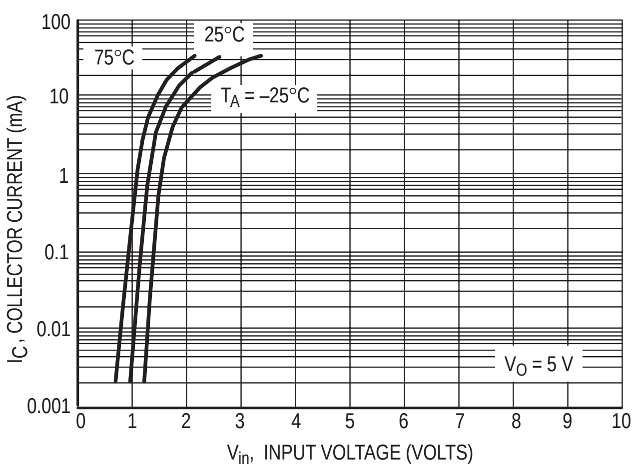


Figure 5. $V_{CE(sat)}$ versus I_C

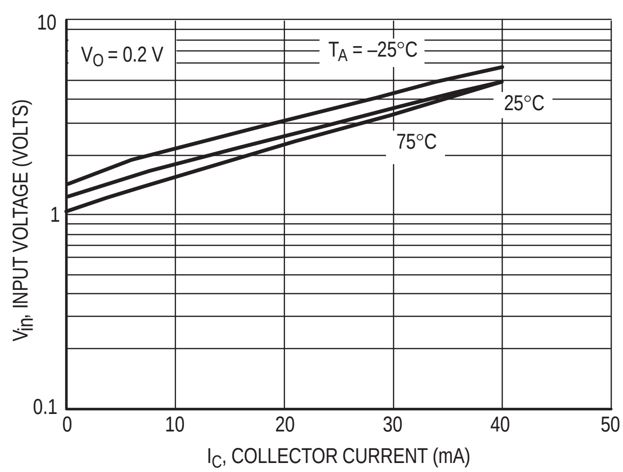


Figure 6. $V_{CE(sat)}$ versus I_C

TYPICAL ELECTRICAL CHARACTERISTICS
DTC124E

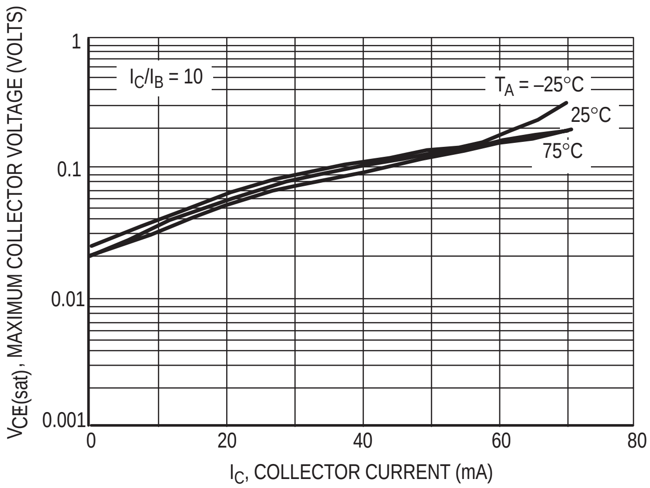


Figure 7. $V_{CE(sat)}$ versus I_C

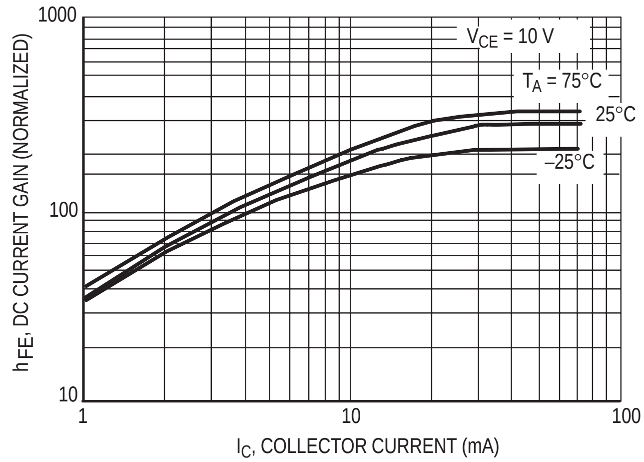


Figure 8. DC Current Gain

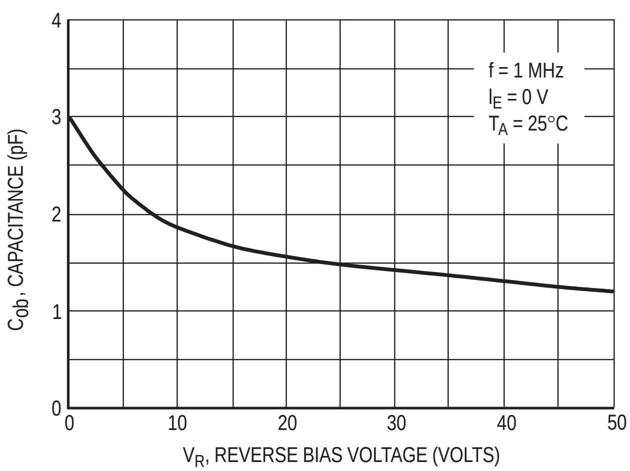


Figure 9. Output Capacitance

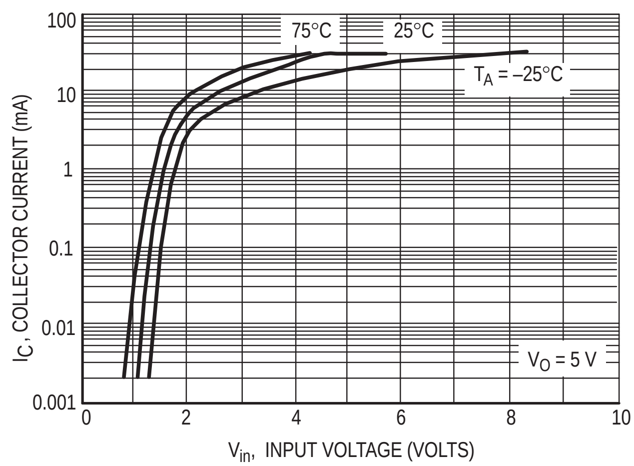


Figure 10. Output Current versus Input Voltage

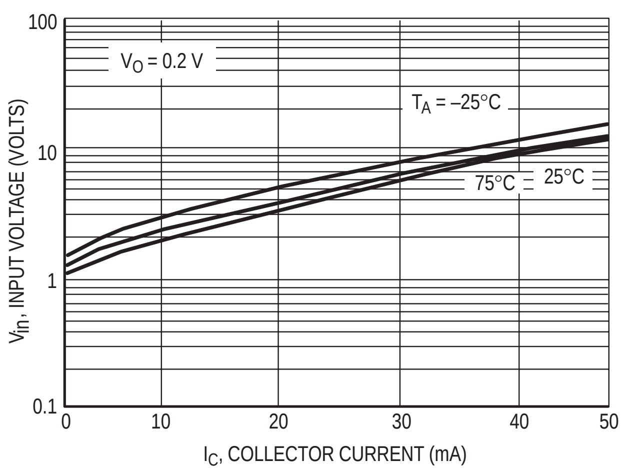


Figure 11. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS
DTC144E

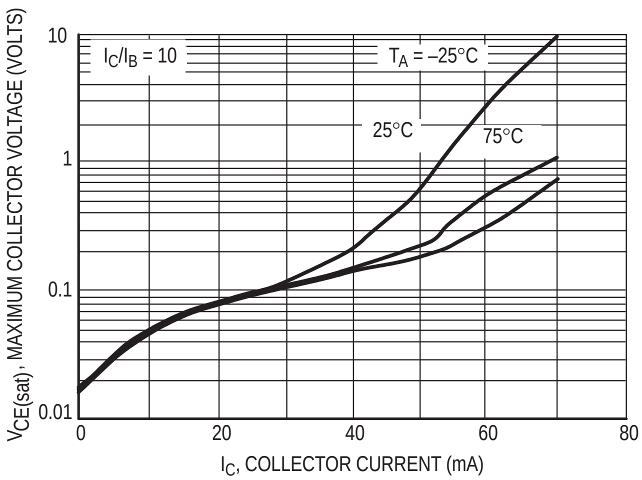


Figure 12. $V_{CE(sat)}$ versus I_C

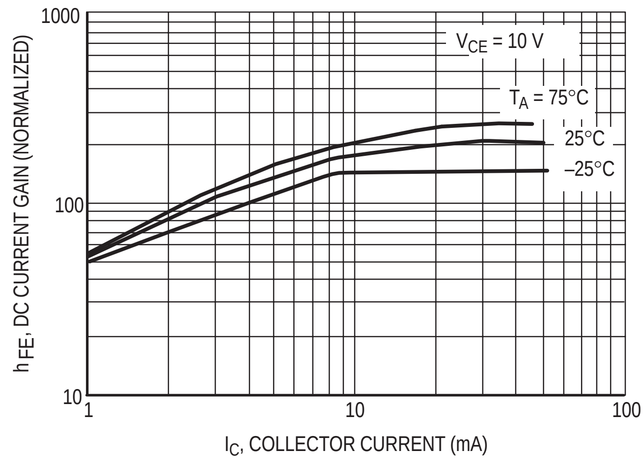


Figure 13. DC Current Gain

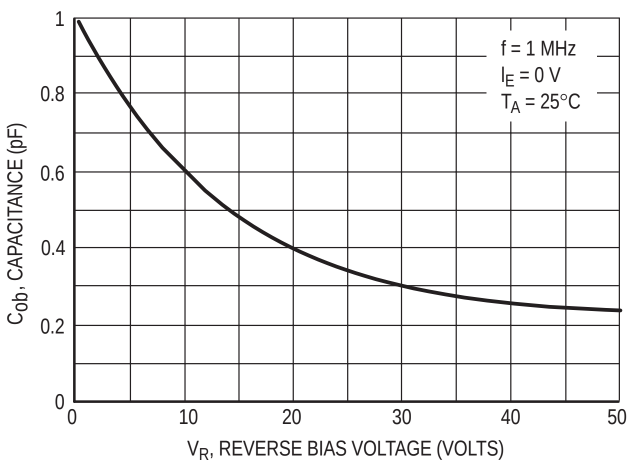


Figure 14. Output Capacitance

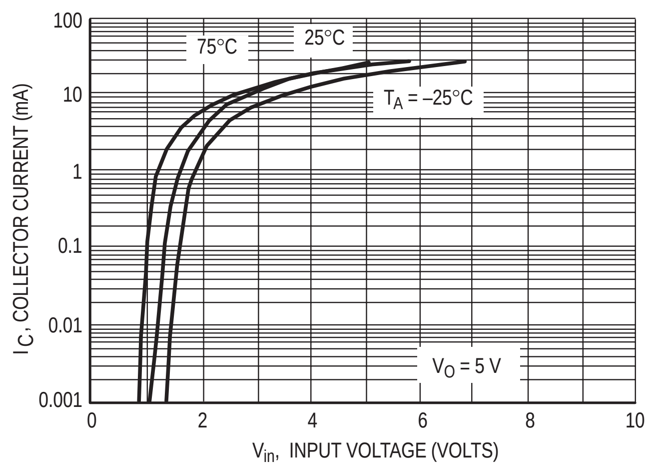


Figure 15. Output Current versus Input Voltage

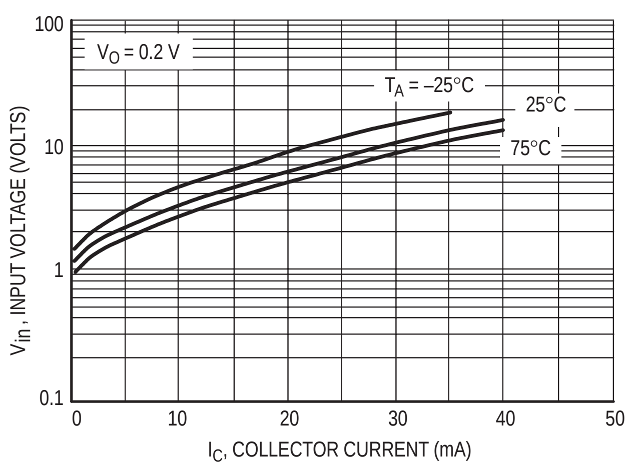


Figure 16. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS
DTC114Y

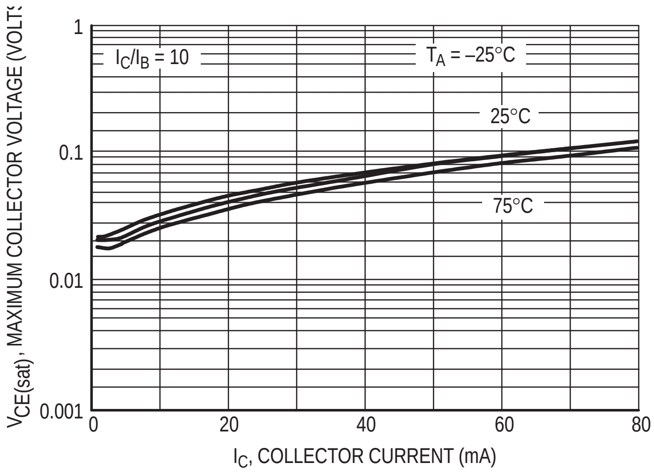


Figure 17. $V_{CE(sat)}$ versus I_C

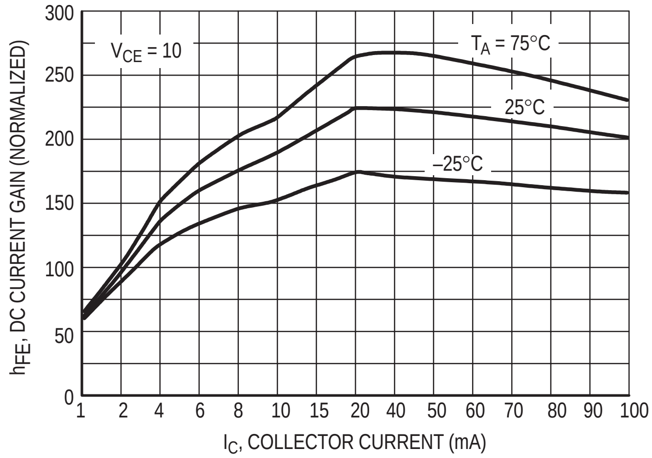


Figure 18. DC Current Gain

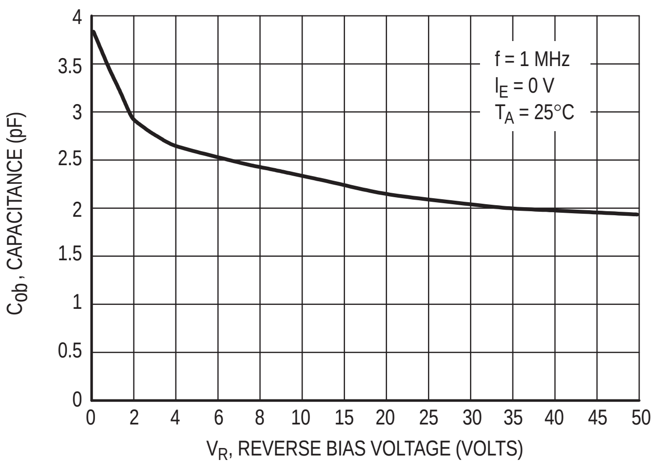


Figure 19. Output Capacitance

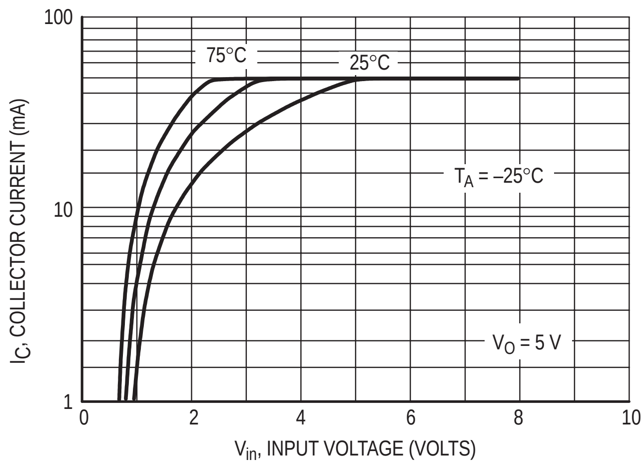


Figure 20. Output Current versus Input Voltage

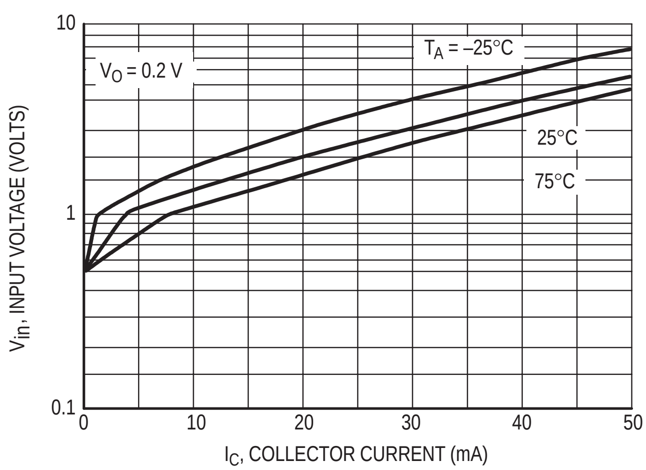


Figure 21. Input Voltage versus Output Current

TYPICAL APPLICATIONS FOR NPN BRTs

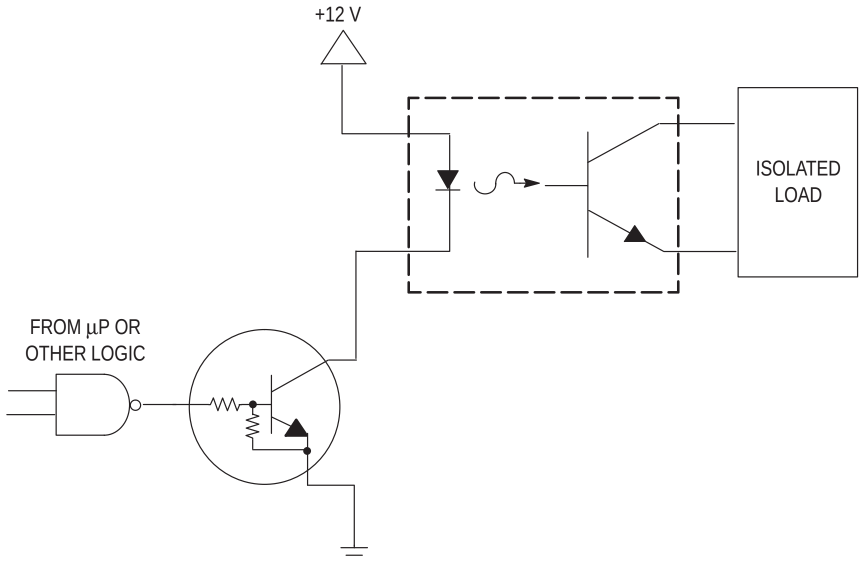


Figure 22. Level Shifter: Connects 12 or 24 Volt Circuits to Logic

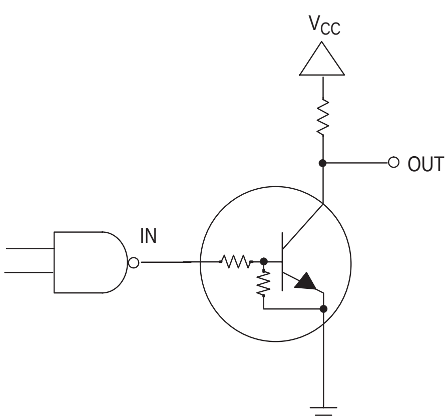


Figure 23. Open Collector Inverter: Inverts the Input Signal

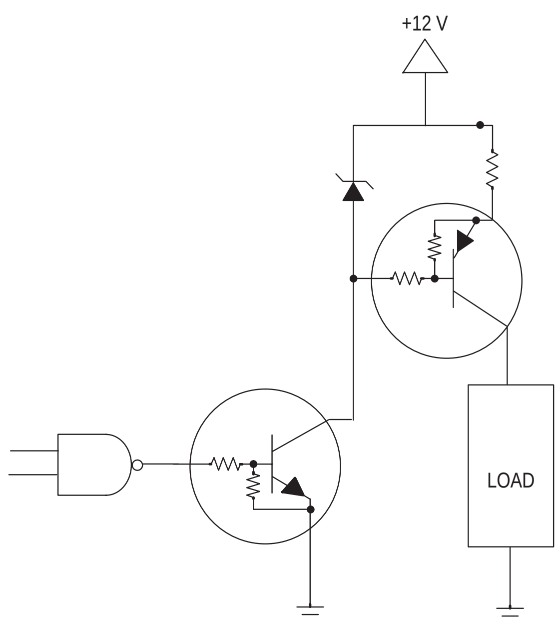
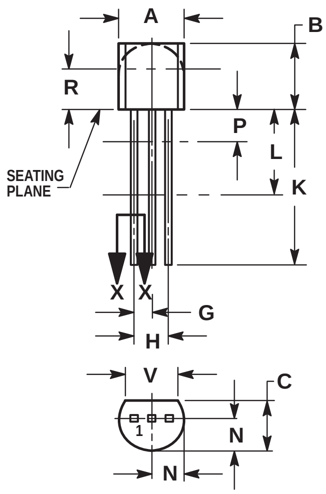
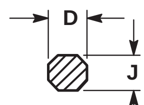


Figure 24. Inexpensive, Unregulated Current Source

PACKAGE DIMENSIONS

TO–92
(TO–226)
CASE 29–11
ISSUE AL





SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

Notes

Notes

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