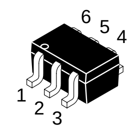
Dual Schottky Barrier Diodes

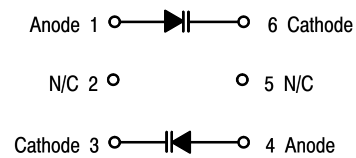
MBD110DWT1
MBD330DWT1
MBD770DWT1

ON Semiconductor Preferred Devices

Application circuit designs are moving toward the consolidation of device count and into smaller packages. The new SOT–363 package is a solution which simplifies circuit design, reduces device count, and reduces board space by putting two discrete devices in one small six–leaded package. The SOT–363 is ideal for low–power surface mount applications where board space is at a premium, such as portable products.



CASE 419B–01, STYLE 6
SOT–363



Surface Mount Comparisons:

	SOT–363	SOT–23
Area (mm^2)	4.6	7.6
Max Package P_D (mW)	120	225
Device Count	2	1

Space Savings:

Package	1 × SOT–23	2 × SOT–23
SOT–363	40%	70%

The MBD110DW, MBD330DW, and MBD770DW devices are spin–offs of our popular MMBD101LT1, MMBD301LT1, and MMBD701LT1 SOT–23 devices. They are designed for high–efficiency UHF and VHF detector applications. Readily available to many other fast switching RF and digital applications.

- Extremely Low Minority Carrier Lifetime
- Very Low Capacitance
- Low Reverse Leakage

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Reverse Voltage	MBD110DWT1 MBD330DWT1 MBD770DWT1	V_R	7.0 30 70	Vdc
Forward Power Dissipation T_A = 25°C		P_F	120	mW
Junction Temperature		T_J	–55 to +125	°C
Storage Temperature Range		T_{stg}	–55 to +150	°C

DEVICE MARKING

MBD110DWT1 = M4 MBD330DWT1 = T4 MBD770DWT1 = H5

Thermal Clad is a trademark of the Bergquist Company.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage		$V_{(BR)R}$				Volts
(I_R = 10 μA)	MBD110DWT1		7.0	10	—	
	MBD330DWT1		30	—	—	
	MBD770DWT1		70	—	—	
Diode Capacitance		C_T				pF
(V_R = 0, f = 1.0 MHz, Note 1)	MBD110DWT1		—	0.88	1.0	
Total Capacitance		C_T				pF
(V_R = 15 Volts, f = 1.0 MHz)	MBD330DWT1		—	0.9	1.5	
(V_R = 20 Volts, f = 1.0 MHz)	MBD770DWT1		—	0.5	1.0	
Reverse Leakage		I_R				
(V_R = 3.0 V)	MBD110DWT1		—	0.02	0.25	μA
(V_R = 25 V)	MBD330DWT1		—	13	200	nAdc
(V_R = 35 V)	MBD770DWT1		—	9.0	200	nAdc
Noise Figure		NF				dB
(f = 1.0 GHz, Note 2)	MBD110DWT1		—	6.0	—	
Forward Voltage		V_F				Vdc
(I_F = 10 mA)	MBD110DWT1		—	0.5	0.6	
(I_F = 1.0 mAdc)	MBD330DWT1		—	0.38	0.45	
(I_F = 10 mA)			—	0.52	0.6	
(I_F = 1.0 mAdc)	MBD770DWT1		—	0.42	0.5	
(I_F = 10 mA)			—	0.7	1.0	

TYPICAL CHARACTERISTICS
MBD110DWT1

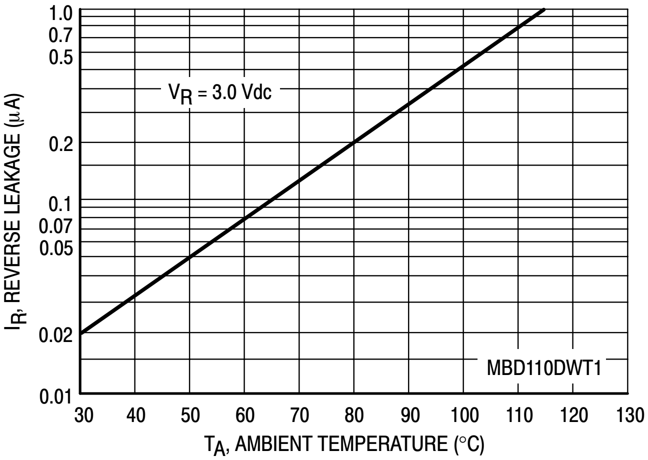


Figure 1. Reverse Leakage

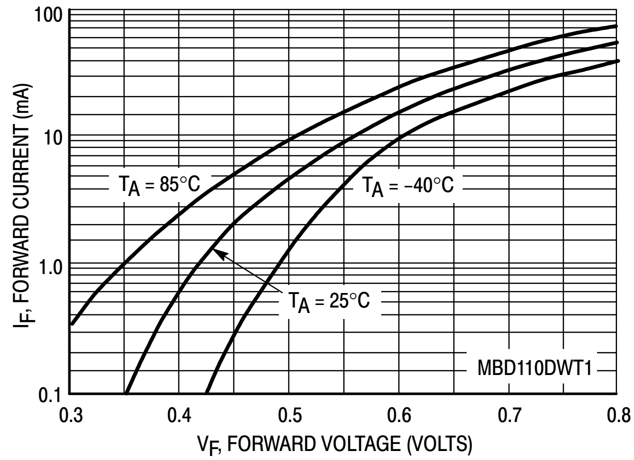


Figure 2. Forward Voltage

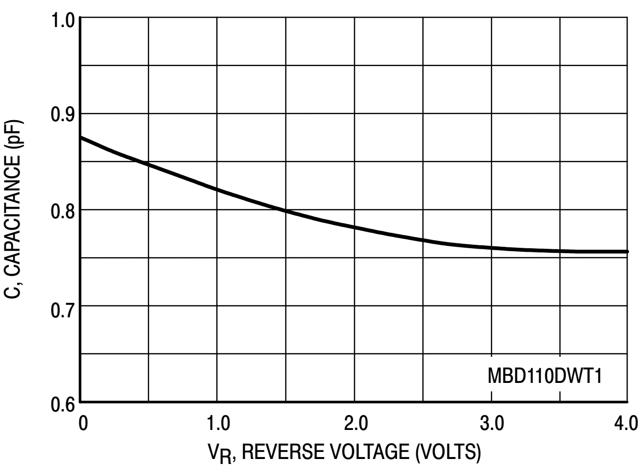


Figure 3. Capacitance

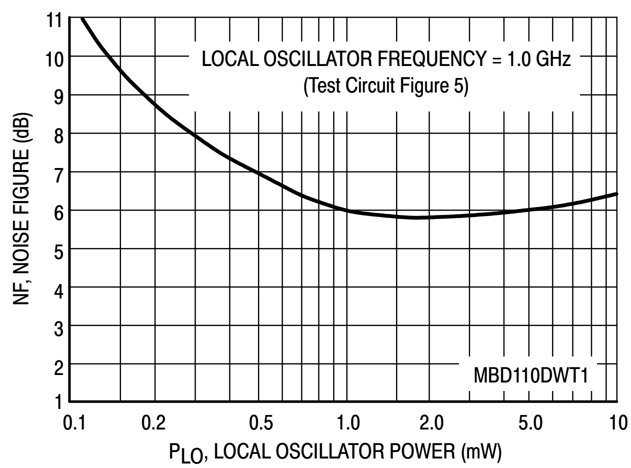


Figure 4. Noise Figure

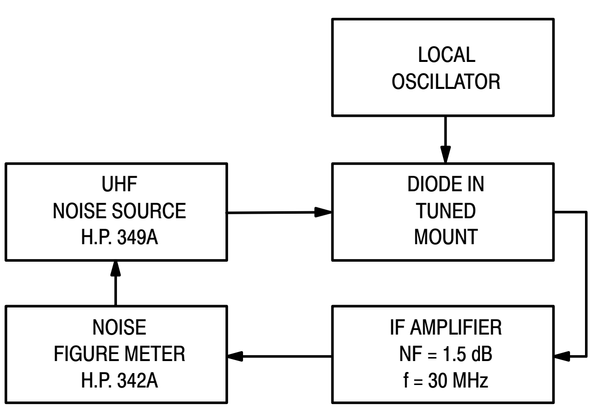


Figure 5. Noise Figure Test Circuit

NOTES ON TESTING AND SPECIFICATIONS

Note 1 – C_C and C_T are measured using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

Note 2 – Noise figure measured with diode under test in tuned diode mount using UHF noise source and local oscillator (LO) frequency of 1.0 GHz. The LO power is adjusted for 1.0 mW. IF amplifier NF = 1.5 dB, f = 30 MHz, see Figure 5.

Note 3 – L_S is measured on a package having a short instead of a die, using an impedance bridge (Boonton Radio Model 250A RX Meter).

TYPICAL CHARACTERISTICS
MBD330DWT1

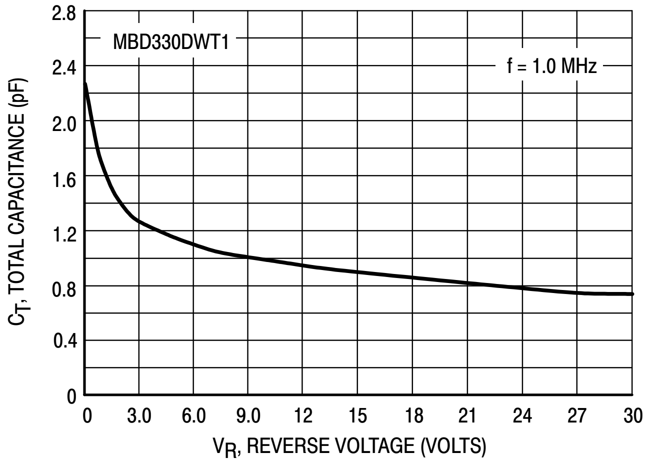


Figure 6. Total Capacitance

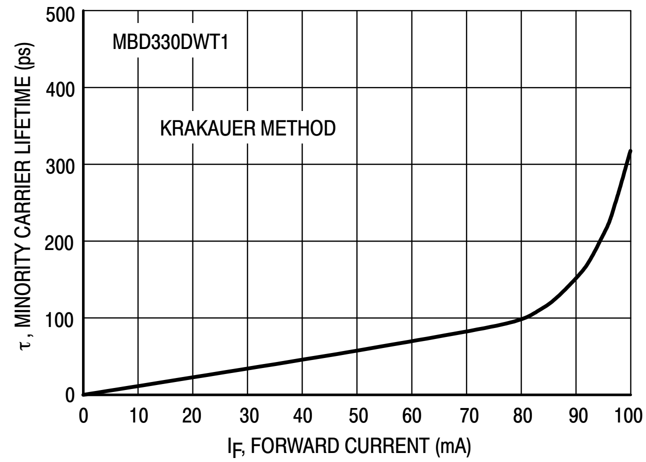


Figure 7. Minority Carrier Lifetime

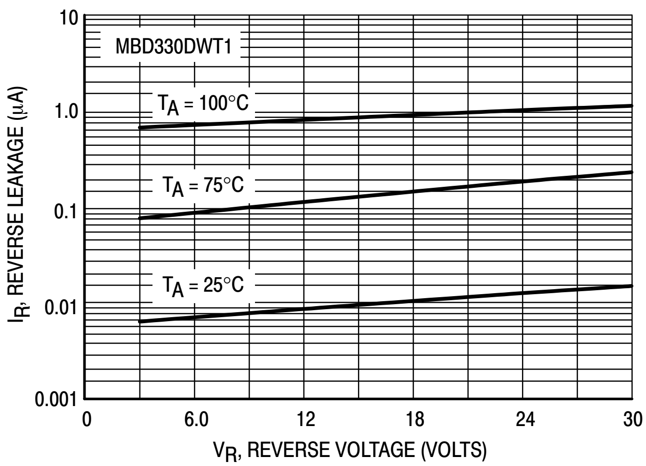


Figure 8. Reverse Leakage

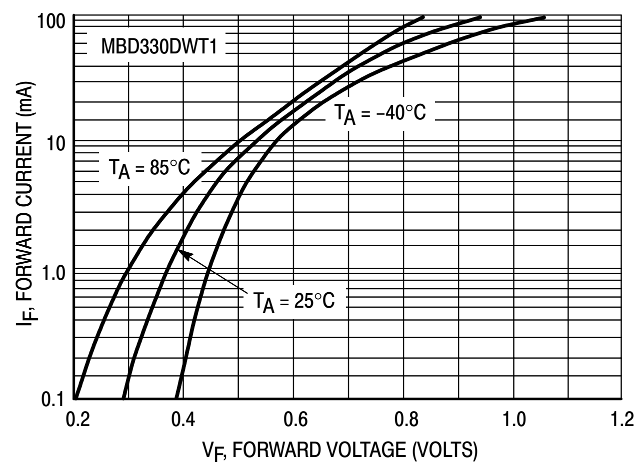


Figure 9. Forward Voltage

TYPICAL CHARACTERISTICS
MBD770DWT1

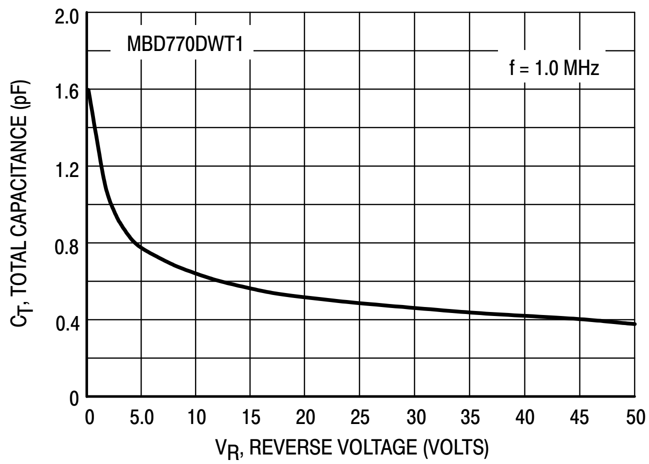


Figure 10. Total Capacitance

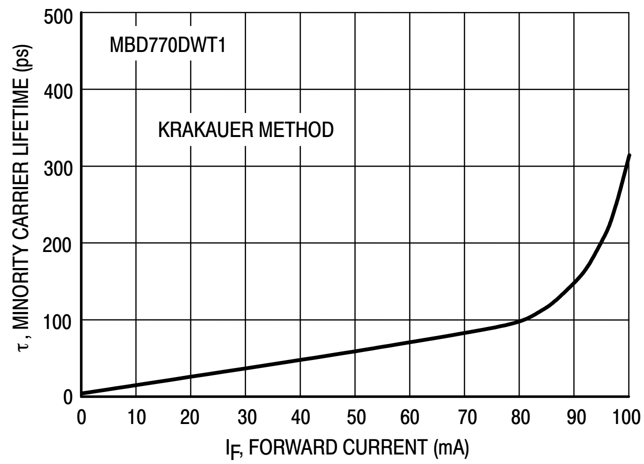


Figure 11. Minority Carrier Lifetime

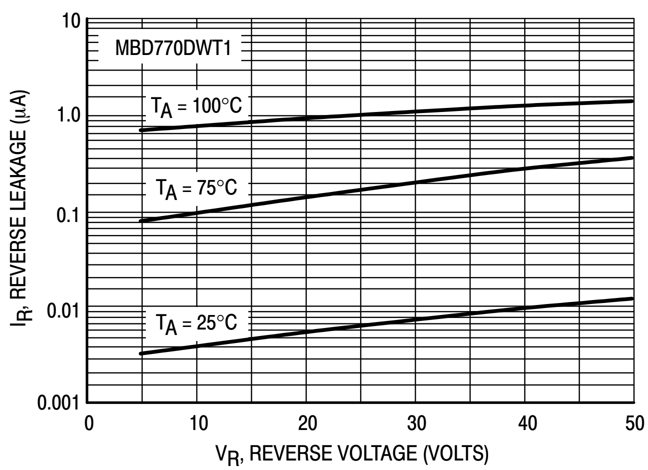


Figure 12. Reverse Leakage

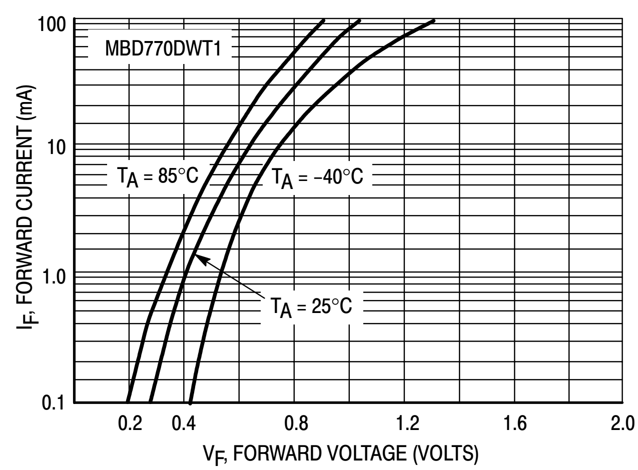
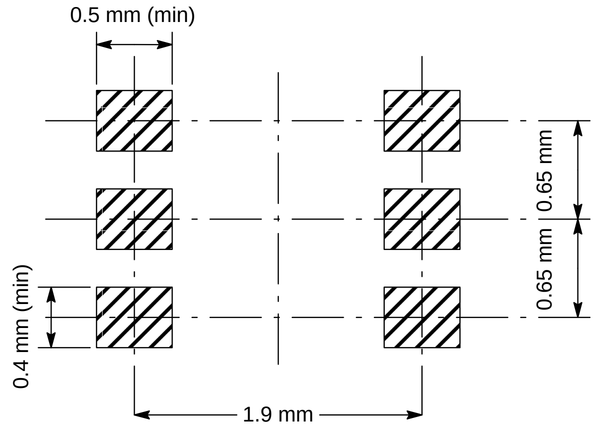


Figure 13. Forward Voltage

INFORMATION FOR USING THE SOT–363 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT–363

SOT–363 POWER DISSIPATION

The power dissipation of the SOT–363 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT–363 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 150 milliwatts.

$$P_D = \frac{150°C - 25°C}{833°C/W} = 150 \text{ milliwatts}$$

The 833°C/W for the SOT–363 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 150 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–363 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

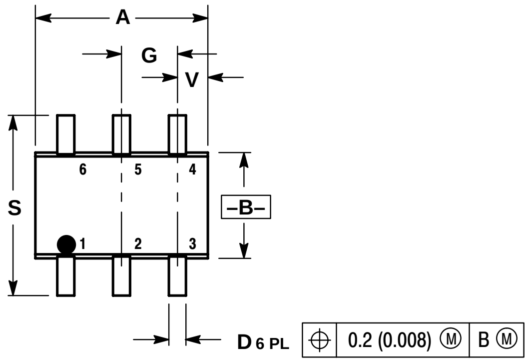
The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

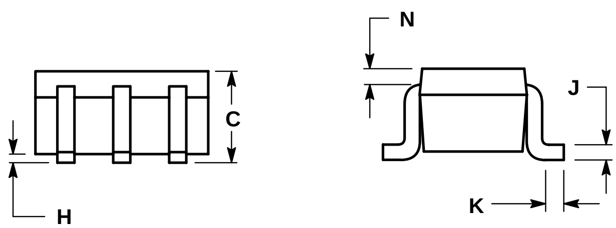
- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS

SC–88 (SOT–363)
CASE 419B–01
ISSUE G





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

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